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Signal Acquisition Challenges in Mobile Systems

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Dedicated to my family.

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Signal Acquisition Challenges in Mobile Systems

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In recent decades, the advent of mobile computing has changed human lives by providing information that was not available in the past. The mobile computing platform opens a new door to the connected world in which various forms of hand-held and wearable systems are ubiquitous. A single mobile device plays multiple roles and shapes human lives towards a better future. In these systems, sensor-based data acquisition plays an essential role in generating and providing useful information. The increased number of sensors is embedded in a single device in order to process various signal modalities. In practice, more than 30 data converters are required in designing a mobile system in which the data-converting blocks become among the most power-hungry components in battery-operated systems. Due to the increased variety of sensors, mobile systems are meant to face several obstacles. For example, the increased number of sensors increase system power consumption during the system operation. The increased power consumption directly affects operation time because mobile systems are powered by a limited energy source.

Moreover, an increased amount of information also gives rise to bandwidth problems in communication due to the increased volume of data transmission. Also, this system design requires a larger area in a silicon die so that multiple signal paths can be placed without cross-channel interference. Therefore, the system design has presented a challenge in terms of trying to resolve the design constraints such as power consumption, bandwidth usage, storage space, and design complexity issues.

To overcome these obstacles, in this dissertation, efficient data acquisition and processing methods are investigated. Specifically, this thesis considers the problems of energy-efficient sampling and binary event detection.

This dissertation begins by presenting a new signal sampling scheme that enables higher precision signal conversion in compressed-sensing-based signal acquisition. The proposed scheme is based on the popular successive approximation register and employs a modified compressive sensing technique to increase the resolution of successive-approximation-register (SAR) analog-to-digital converter (ADC) architecture. Circuit-level architecture is discussed to implement the proposed scheme using the SAR ADC architecture. A non-uniform quantization scheme is proposed and it improves data quality after data acquisition. The proposed scheme is expected to be used for medium- or high- frequency data conversion.

Secondly, the possibility of using fewer ADCs than channels is studied by leveraging sparse-signal representation and blind-source-separation (BSS) techniques. In particular, this dissertation examines the problem of using a

single ADC or quantizer system for digitizing multi-channel inputs. Mixing and de-mixing strategies are extensively studied for sampling frequency-sparse signals and the proposed multi-channel architecture can be easily implemented using today's analog/mixed-signal circuits.

The third part of this dissertation investigates a binary hypothesis testing problem. In mobile devices such as smartphones and tablet PCs, a major portion of energy is consumed in user interfaces (LCD display and touch input processing). For accurate detection and better user interface, energy-efficient sensing and detection schemes are necessary to manage multiple sensor inputs. A highly efficient detection scheme is presented that can detect binary events reliably with a fraction of the energy consumption required in the conventional energy detection.

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Chapter 1

Introduction

In signal sampling, Shannon and Nyquist have shown that the sampling rate must be more than double the signal bandwidth to avoid information loss. The Shannon-Nyquist sampling theorem [3] has been regarded as a golden rule in data sampling and conversion since it was developed in the late 1940. The Shannon-Nyquist theorem formed the theoretical foundation for modern signal acquisition system such as analog-to-digital converters (ADCs), which become among the essential elements of modern mixed-signal systems.

Today's advanced wireless technologies increasingly rely on a high frequency band to overcome all voice and data traffic bottlenecks. For this reason, millimeter wave (30-300Ghz) is considered to reduce data traffic congestion for recent 5G wireless networks. In high frequency signal acquisition, there exists a trade-off between the sampling speed and data resolution, in which both cannot be enhanced simultaneously when designing data-converting systems. To overcome the quantization depth constraint for high speed signals, a new sampling frame work is required.

On the other hand, with the increase in system complexity, recent signal-processing applications require information from multiple sensors such

as sensor arrays, physiological signal monitoring, and brain-machine interfaces. In these systems, it is common to sample up to 128 channels of simultaneous data. The increased number of sampling channels requires complex system design to improve the operating power in the system. Thus, it is worthwhile to explore efficient ways of reducing the system complexity with a new form of converter architecture. In other words, the question that arises here is whether it is possible to use fewer data converters than channels by leveraging recent achievements in signal processing.

Recently, compressed/compressive sampling theory has been extensively studied in the field of applied mathematics. The major theoretic foundation was accomplished by Emmanuel Cándes, Torrence Tao, and David Donoho in the early 2000s [4]. The random sampling theory is regarded as the most outstanding achievement in sampling theory such that it potentially renders the sub-Nyquist rate sampling applicable to the expensive sampling in measurements. Motivated by the advent of compressed sensing, in this dissertation, efficient data conversion schemes for single and multi-channel signals are explored, with a focus on mobile and wearable system applications.

The first part of this dissertation begins by introducing the possibility of increasing the resolution of a successive-approximation-register (SAR) ADC in medium- or high-bandwidth signal sampling. The sampling rate-resolution limitation is a challenging problem in SAR ADC design, even with recent advanced technology. The conventional compressive sensing scheme has only a fixed resolution conversion. Thus, a means of non-uniform, quantization-based

random sampling is introduced; it is deliberately designed to promote the precision of sampled data through a tailored recovery algorithm. The proposed non-uniform quantization scheme is expected to be useful for medium and high frequency data conversion. In particular, the proposed quantization scheme is applied to the popular successive approximation register architecture.

Next, the possibility of using fewer ADCs than channels is studied by leveraging sparse representation of signals as an extension of mixing and de-mixing multi-channel sparse signals. Specifically, this work considers the problem of using a single ADC or quantizer system to digitize multi-channel inputs that consist of an unknown number of sinusoids in unknown frequencies. The mixing and de-mixing strategies are deliberately designed for frequency-sparse signals. The proposed multi-channel architecture is readily implementable using current analog/mixed-signal circuit designs. In the proposed solution, the multi-channel signals are sampled at the Nyquist rate which is identical to the single-channel sampling case. However, they can be recovered without sacrificing the input signal bandwidths.

Lastly, an efficient binary hypothesis testing problem is investigated. A sequential energy detection scheme is proposed that requires a lower number of samples to determine the existence of the signal of interest over the measurements. As the volume of sampled data has increased, high power consumption and/or increased sensing latency are expected during the data processing. To facilitate system performance with reduced operating power, a fast detection protocol is required. Fast sensing circuits can be designed

using highly complex designs. However, the circuits mentioned above increase operating power which is not desirable for systems operated by stored energy. Thus, the trade-off between sensing latency and power consumption needs to be reviewed to meet the system requirements. The proposed sequential detection scheme requires far fewer samples to determine the existence of a signal of interest, which can be translated as energy savings.

1.1 Contributions of the study

Throughout this thesis, innovative solutions for single and multiple-channel signal sampling and detection are studied, which can overcome the energy, bandwidth, and area obstacles in mobile systems. The major contributions are outlined in the following subsections.

1.1.1 Non-uniform quantization random signal sampler

A new form of SAR ADC architecture is introduced that is capable of improving the resolution of the sampled data in medium- or high-bandwidth signal sampling. A non-uniform quantization scheme, which is combined with random sampling procedures, is presented and the scheme makes use of the system properties of SAR ADC architecture. Signal acquisition and recovery models are presented, and simulation is performed to gauge the advantages of the proposed architecture. By performing simulations, the recovery of sampled signals demonstrates improved resolution compared to that of conventional compressive sensing cases. To realize the proposed scheme incorporated with

the SAR ADC architecture, block level circuit realization is also discussed.

1.1.2 Multi-channel sparse data conversion

The next contribution of this thesis is in the architecture of the multi-channel sparse data converter. The converter architecture aims to sample multiple channels using a single quantizer. Specifically, various pseudo-random sequences are compared. An optimal mixing scheme is extensively studied to design the analog front-end side to combine multi-channel inputs. Multiple channels are sampled at the Nyquist rate, which is identical to the single-channel sampling case. Realistic signal-mixing strategies and recovery algorithms are proposed that enable the sampling of multiple-channel sparse signals with a single quantization unit. Based on the system model, a new form of ADC architecture with switched-capacitor-based sample-and-hold (S/H) circuits is proposed, which can be easily implemented. The prototype implementation of the proposed architecture is designed and fabricated in 130nm complementary metaloxidesemiconductor (CMOS) process. The prototype ADC demonstrates that the proposed architecture can successfully sample up to four channel frequency-sparse signals.

1.1.3 Energy-efficient sequential detector

An efficient binary hypothesis testing problem is investigated. A new sequential energy-detection scheme is proposed that requires far fewer samples to determine the existence of a signal of interest over the measurements.

The proposed detection strategy divides the conventional hypothesis testing steps into two phases: 1) a summing phase and 2) a sequential detection phase. By separating the detection steps, the total computation and number of test samples is reduced. This reduction can be translated into energy savings which could help extend operating time in energy-limited mobile systems. The proposed sequential detection scheme shows robust detection performance under low signal-to-noise conditions compared with the conventional detection scheme, which is based on a fixed sample size. The proposed scheme can be combined with the compressed sensing (CS) and sparse-signal sampling methods as a form of post-processing to detect a binary event. It can also work independently with general detector systems.

1.2 Organization

This dissertation is organized into the following chapters: Chapter 2 introduces a new form of ADC architecture that is capable of sensing multi-channel frequency-sparse signals using a single quantizer, and circuit-level details on how to realize the proposed architecture in a mixed-signal circuit. Chapter 3 introduces a new form of ADC architecture which is capable of sensing multi-channel frequency-sparse signals using a single quantizer, and circuit level details on how to realize the proposed architecture in a mixed-signal circuit. Chapter 4 proposes a highly efficient detection scheme to determine binary event status based on a sequential energy detector. Numerical analysis of the proposed sequential detection scheme is presented. This disser-

tation concludes with a summary of the contributions of the proposed signal acquisition and processing schemes. Future directions for extending this thesis are discussed in Chapter 5.

Chapter 2

A Randomly Sampled Non-uniform Resolution Data Converter

Analog-to-digital converters are among the essential elements of modern mixed-signal systems. In the market, there are many different types of ADC architecture, including sigma-delta, successive approximation register, pipeline, time-interleaving, and flash [5, 6]. With the improvements in scaling technology, SAR ADC is becoming increasingly popular due to its high power-efficiency and easy scaling with the technology because most of its design is performed in the digital domain. Fig. 2.1 illustrates the sampling rate and resolution in different types of ADC architecture.

However, for a SAR ADC, each conversion cycle only produces one more bit at a time and the SAR ADC is limited to medium resolution and medium speed. When the sampling speed reaches around 1GHz, the resolution of SAR ADC is limited to about 6-bit using the most advanced circuit technologies (Fig. 2.2). To overcome this limitation, sampling and signal conversion schemes are proposed that are based on the SAR ADC architecture. The proposed SAR architecture takes advantage of a random sampling scheme to increase the resolution of SAR ADC in the high-speed region.

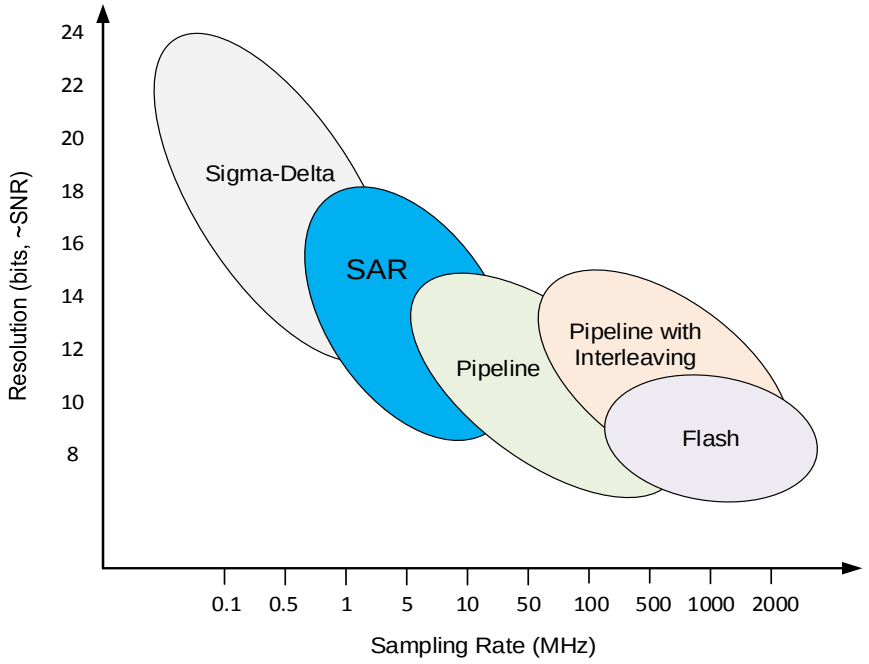


Figure 2.1: Architecture of analog-to-digital converters, resolution, and sampling rate [1].

Several studies [7, 8] have proposed SAR ADC based systems that are capable of sampling and reconstructing multi-channel information; the circuit level implementation and measurement results are reported [9]. Yet, the architecture does not necessarily leads to better resolution.

Recently, compressed sensing (CS) based ADC design has been actively studied to acquire wide-band signal with a non-uniform sampling strategy [10]. 1-bit compressive sensing acquires coarsely quantized measurements to detect the active frequency components [11]. Another approach [12] also investigates the trade-off between bit-depth and measurement-rate in CS in the context

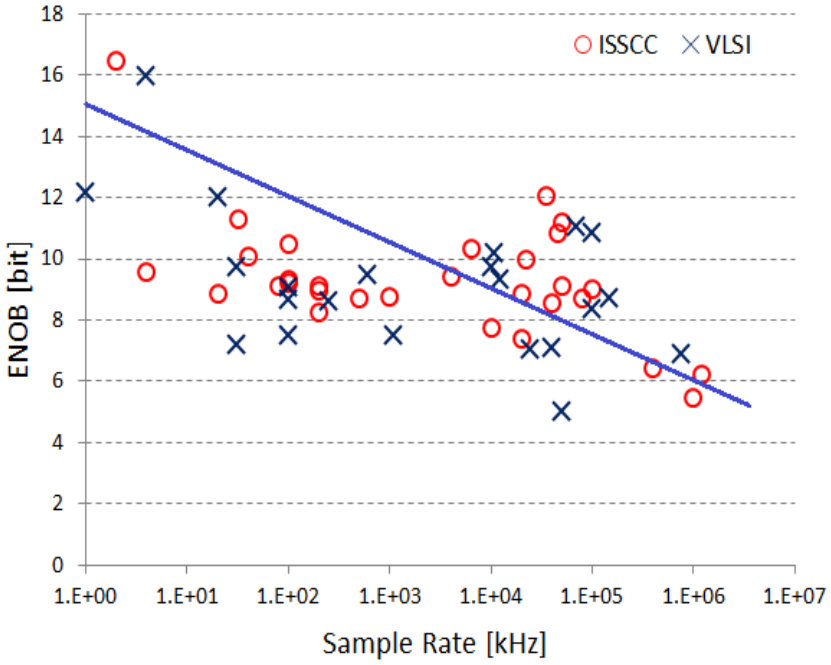


Figure 2.2: Sample rate and ENOB survey in SAR ADC [2].

of limited store memory or data transmission rate. However, all these works have continued to make use of uniform quantization, which is different from the non-uniform resolution case that this dissertation is investigating. There is a similar approach that uses a non-uniform quantization scheme with few measurements [13], and the approach is relatively effective for signals with high signal-to-noise ratio (SNR). However, the conversion scheme includes several limitations. The work is focused on the low speed sampling cases ($\leq$ 1kHz) with lower numbers of measurements rather than high-speed sampling applications. The highly compressed CS strategy limits the allowable signal sparseness of interest in the sparse domain. Furthermore, the work does not fully

utilize the SAR ADC architecture by varying quantization depth from 1-bit to 16-bit, which possibly generates a wide range of variance in the sampled resolution and leads to sub-optimal efficiency in terms of utilizing system resources. Lastly, the study only gives reconstruction error performance with the non-uniform quantization strategy while the proposed scheme leads to a concrete analysis on ADC architecture, which is more practical in circuit design. A new reconstruction algorithm is presented and is formulated by an element-wise constraint that is shown to be more efficient than the reconstruction method using weighted constraint [13]. The simulation results present a better reconstruction performance than through coarse quantization.

This chapter is organized as follows: Section 2.1 introduces fundamental backgrounds in SAR ADC architecture and CS-based sampling. Section 2.2 presents our signal acquisition and recovery strategy that enables high-resolution sampling in high-frequency signals. Section 2.3 discusses details about implementation of the proposed non-uniform quantization scheme. Simulation results are demonstrated in Section 2.4. Finally, the advantages and highlight areas for future research are summarized in Section 2.5.

2.1 Background

2.1.1 Data conversion in SAR ADC

A data converter or signal acquisition system requires a quantization unit to convert input voltage to a finite number of bits. The SAR ADC architecture is becoming increasingly popular in practice for its high power-

efficiency, and easy scaling with current technology since most of circuitry is designed in the digital domain. SAR ADCs produce one more bit at a time in each conversion cycle, and a block diagram of the architecture is displayed in Fig. 2.3.

The analog-to-digital conversion starts with enabling sample and hold (S/H) circuit to latch the input voltage V_{in} during the conversion cycle. The SAR logic directs the DAC to generate outputs through binary outputs which range the most significant bit (MSB) to the least significant bit (LSB). With the latched the input and DAC output, a comparator decides whether DAC output DAC_{out} is greater the latched V_{in} or not. The DAC starts producing DAC_{out} which is initialized by 1/2 V_{ref}. If DAC_{out} is larger than V_{in}, then the most significant bit (MSB) is set to zero which reduces DAC_{out} by half (1/4 V_{ref}) in the next iteration. If DAC_{out} is smaller than V_{in}, then the MSB is set to one and the MSB remains to the rest of process. This binary search process is continuing iteratively from MSB to LSB. The CTRL logic controls time instances when the conversion starts and completes, and the iteration interval. Because of the iterative binary search process, to obtain more bits, SAR ADCs require longer conversion time and it causes sample rate vs. quantization depth constraint in high speed sampling.

Therefore, the applications of SAR ADC is limited to medium resolution and medium speed. We hope to overcome this hardware constraint by making use of sub-Nyquist sampling strategy which randomly samples a sparse signal of interest in the frequency or DFT domain.

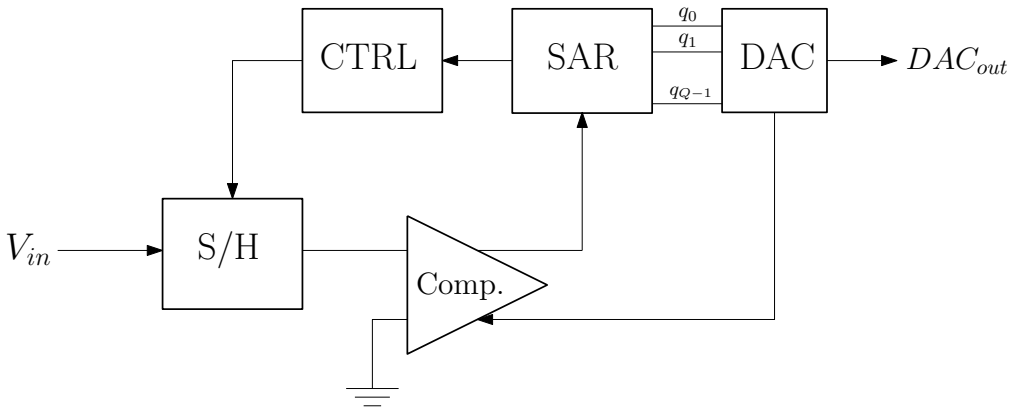


Figure 2.3: Typical SAR ADC architecture.

2.1.2 Compressive sensing

Recent study in the field of CS shows the other way to take fewer samples than those from Nyquist criteria. For the class of sparse signal, CS pursuits acquiring $M < N$ samples rather than N samples of a signal at Nyquist rate with linear measurement. Let $N \times 1$ input signal vector $\vec{x} \in \Re^N$ is K-sparse in a transform basis Ψ. One can rewrite it as $\vec{x} = \Psi\vec{\alpha}$, where $||\vec{\alpha}|\,|_0 = K$. In CS, a $M \times 1$ measurement $\vec{y}$ which is sufficient to represent the input signal $\vec{x}$ with measurement operator Φ:

$$\vec{y} = \mathbf{\Phi}\vec{x} = \mathbf{\Phi}\mathbf{\Psi}\vec{\alpha}. \tag{2.1}$$

Let us define a matrix $\mathbf{A} = \mathbf{\Phi}\mathbf{\Psi}$, and one can recover the input vector $\vec{x}$ without loss of information by solving a minimization problem:

$$\begin{aligned} &\text{minimize} \quad ||\vec{\alpha}||_1 \\ &\text{subject to} \quad \vec{y} = \mathbf{A}\vec{\alpha} \end{aligned} \tag{2.2}$$

where $\vec{\alpha} = [\alpha_1, \alpha_2, \cdots, \alpha_N]^T$ and $||\vec{\alpha}||_1 = \sum_{r=1}^{N} |\alpha_r|$.

After sampling, the rest problem is to solve $\vec{\alpha}$ and reconstruct $\vec{x}$ via nonlinear optimization. One popular way to get $\vec{y}$ is randomly sampling $\vec{x}$. In this case, the $M \times N$ sampling matrix Φ is a diagonal matrix which consists of the random canonical basis (delta functions). For frequency-sparse signal, if Ψ is a IDFT matrix with $N \times N$ dimension, $\mathbf{A}$ is a matrix consisting of randomly sub-sampled rows of the IDFT matrix. Such a matrix has a high probability of satisfying the Restricted Isometry Property (RIP) [14], and thus is suitable for compressive sensing operations. Applying to frequency-sparse signal, the matrix $\mathbf{A}$ is sampling randomly in time domain, and the best theoretic result of Fourier sampling shows that $M = O(K \log^4 N)$ is sufficient to satisfy the RIP condition [15]. To find the sparsest solution, the problem becomes a ℓ_1 minimization problem. Considering ADC's quantization noise, the minimization problem can be modified as,

$$\begin{aligned} &\text{minimize} \quad ||\vec{\alpha}||_1 \\ &\text{subject to} \quad ||\vec{y} - \mathbf{A}\vec{\alpha}||_2 \leq \epsilon, \end{aligned} \tag{2.3}$$

where the constant ϵ which bounds the measurement distortion. Without considering other noise effects, ϵ can be treated as the quantization noise sigma value.

2.2 Signal acquisition and recovery

In this section, we introduce our sampling and recovery schemes which enable high resolution signal acquisition in high speed sampling. First, we employ random sampling operator which is the same as CS and it is applied

to the SAR ADC architecture, but the quantization depth is varied by the consecutive non-sampling period. If the sampling operator is one (*1*) at corresponding sampling time instance, the input signal is sampled and latched until the SAR unit finds the finite bit description: quantization stage. The quantization depth is decided by the number of following zeros (*0*s) which corresponds to non-sampling period in the sampling stage, so that the SAR unit makes use of the time budget to convert the input signal into high resolution bit description. Thus, the more consecutive zeros allow more precise signal description with higher quantization depth. With the sampling and quantization strategies, every sampled signal can be translated into different precision which is illustrated in Fig. 2.4.

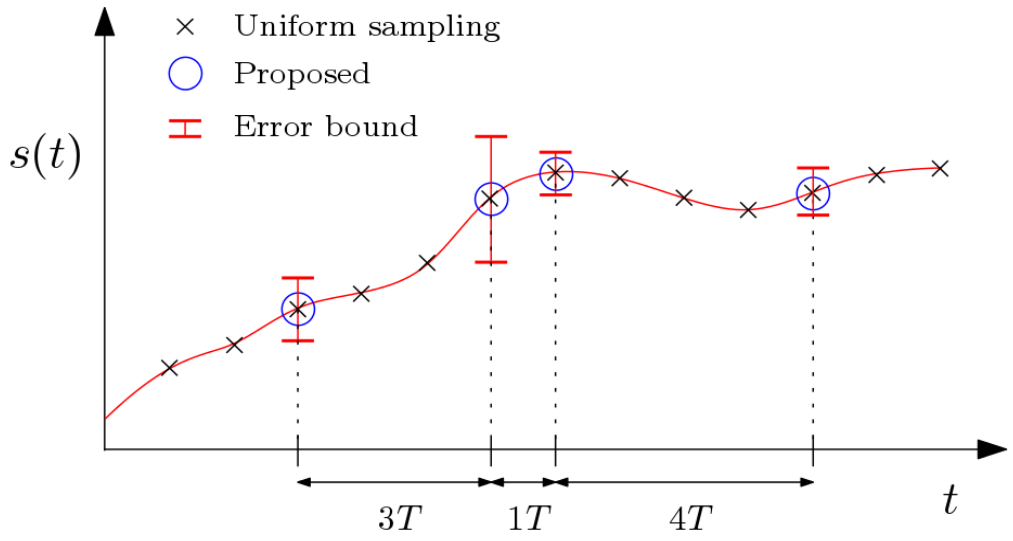


Figure 2.4: Comparison of sampling schemes.

The sampling and quantization schemes require a more efficient recovery algorithm to fully facilitate the sampled signals with non-uniform quanti-

zation levels. Since each sample has different approximation error bound, one can set tighter constraints for the recovery. Leveraging the error bounds, we propose an element-wise constraint which is modelled as,

$$\begin{aligned} &\text{minimize} \quad ||\vec{\alpha}||_1 \\ &\text{subject to} \quad |y_r - (\mathbf{A}\vec{\alpha})_r| \leq \epsilon_r, \end{aligned} \tag{2.4}$$

where $r = 1, 2, \cdots, M$, and the subscript r means the r-th entry of the vector. The error vector is defined as $\vec{\epsilon} = [\epsilon_1, \epsilon_2, \cdots, \epsilon_M]^T$ which allows to bound the quantization error. For example, in uniform quantization, the error constraint vector becomes $\epsilon_1 = \epsilon_2 = \cdots = \epsilon_M$. The constraint will give the same result as the ℓ_2 norm case. For non-uniform quantization, ϵ_r depends on the instantaneous resolution, which produces more accurate results than the ℓ_2 norm constraint by solving the minimization problem with the element-wise constraint vector.

2.3 Implementation consideration

In this section, more details about the proposed scheme will be discussed to consider a real circuit implementation. The proposed scheme can be implemented in two ways: 1) using two or multiple ADCs (low and high resolution ADCs), and 2) single ADC with a high-bit DAC architecture. We choose the later approach due to its simpler architecture and lower power design capability The simulation results are demonstrated in the following section.

2.3.1 Sampling sequences

We employ pseudo-random binary sequences (PRBS) with the same probability for one and zero which imply $M = N/2$. Assume that the SAR ADC resolution is limited to 6-bit in high-speed sampling. With conventional uniform sampling and traditional CS quantization schemes, there are 50% samples quantized to be 6-bit. With non-uniform quantization scheme, the quantization depth will be varying depending on the following *1*s and *0*s. PRBS are useful selection for the proposed SAR ADC architecture because the sequences can be pre-defined so that they can be stored in non-volatile memory space. The stored sequences are not only used in the sampling phase to determine the corresponding quantization depth, but also used to represent the compressively sampled signals in the recovery afterwords. We note here that the proposed scheme can be realized in a fully-passive CS framework. The proposed CS SAR ADC operates in discrete time rather than continuous time using switch capacitor circuit. In real implementation, the switch capacitor circuit in the SAR ADC operates with the pre-defined PRBS which allows to achieve high efficient sampling. Readers may refer to the architecture of switch-capacitor-based sample-and-hold architecture in [8, 9] which differs from previous random-modulator-based CS ADC architecture.

2.3.2 Quantization depth

The sampling period is equivalent to the symbol status of the measurement matrix Φ which can be easily implemented by turning on and off the

switch capacitor circuit. The quantization happens whenever sampling takes place (*1* in the matrix Φ), but just the quantization bit depends on the number of following *0*s. Before sampling the next sample, the input signal is quantized in successive manner the same as the conventional SAR ADC does.

To be more specific, the proposed quantization scheme starts quantizing with b_0-bit and keeps increasing the quantization depth depending on the number of following zero. Defining quantization operator $\mathbb{Q}$, the input signal x_r is to be converted with quantization operator as $y(r) = \mathbb{Q}(\mathbf{\Phi} x_r, b_r)$, where $b_r = b_0 + step \times z_{c,r}$ bit (e.g., $b_0 = 6$ bit in our simulation), $step$ is the step increase in quantization bits, and $z_{c,r}$ is the zero count after the sampling instance of *1* at r. Since the sampling power is usually negligible in a SAR ADC design, the quantization phase takes far less time compared to a conventional SAR ADC which quantizes every sample with the maximum quantization bits meaning that the proposed architecture can save the total power consumption in sampling and quantizing phases, and allows savings in memory space after conversion.

In Table 2.1, for the sake of better understanding, we list the expected resolution of the uniform randomly generated measurement matrix $\mathbf{\Phi}$ in the case of $step = 1$, $b_0 = 6$-bit, and the maximum quantization bit $b_{max} = 12$-bit. We choose $b_0 = 6$-bit from the trend graph in Fig. 2.2 which shows that 6-bit precision is the maximum resolution at gigahertz sampling with SAR ADC architecture using the latest technology.

Ideally, the possible range of $step$ can be set $step = b_0$ in theory, but it

Table 2.1: Expected resolution

Sequence	Probability	Resolution
0	1/2	0
11	1/4	6
101	1/8	7
1001	1/16	8
⋮	⋮	⋮
1000001	1/128	11
10000001	1/256	$b_{max} = 12$
Other	1/256	$b_{max} = 12$

would be better to keep it more conservative manner such as $step < b_0$ considering delay factors in circuit realization. Most of samples will be translated into low-bit depth (e.g., 6-8 bits), but quantization with high-bit depth will be taken by selecting lengthy random sequences.

For simple presentation, without taking into account other additive noise, the error constraint is equivalent to the quantization noise which is not uniform. The recovery model of input signal is formulated in (2.4), and it makes use of the error constraint which bounds the representation error solving the minimization problem. The quantization noise is a function of bit depth, thus the error constraint can be replaced by $\epsilon_r = V_{ref}/2^{b_r}$.

2.3.3 Architecture for the proposed ADC

Since the frequencies of most natural signals are in the order of kHz, the major constraints with WSN for natural signals lie in area and power consumption rather than speed requirement, meaning that RMPI and MWC are

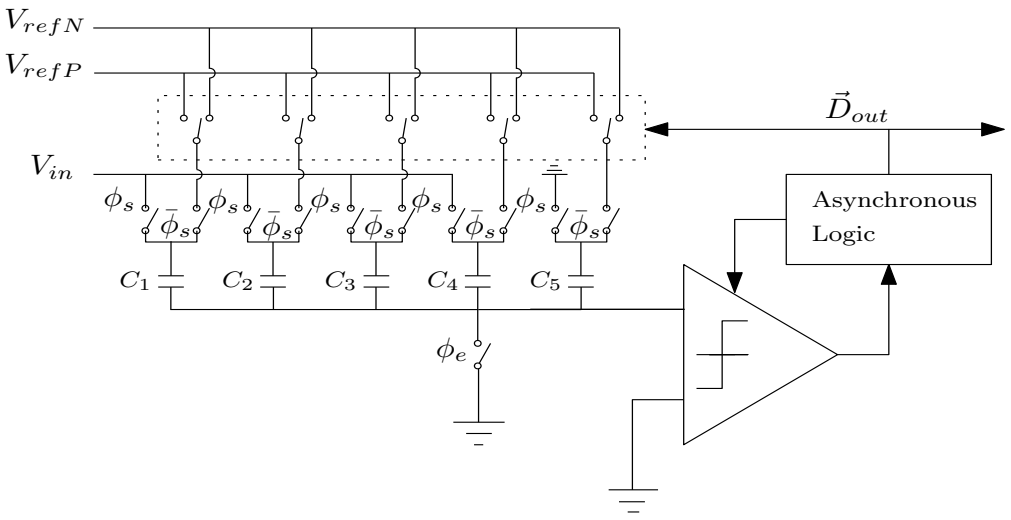


Figure 2.5: Non-uniform adc architecture.

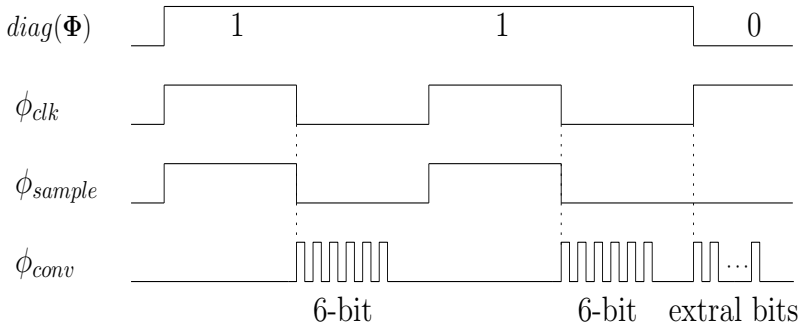
unnecessary. Plus that NUS may result in information loss of many natural signals, RD becomes the best choice for these applications. Different from conventional RD architectures that require analog mixers and active integrators before a low-rate ADC [16–19], we propose a fully-passive CS framework that directly embeds random demodulation into a conventional SAR ADC. The proposed CS SAR ADC operates in discrete time rather than continuous time. In real implementation, the switch capacitor circuit [20] in the SAR ADC operates with the pre-defined PRBS which allows to achieve high efficient sampling process.

Fig. 2.5 shows the architecture for a 12-bit CS SAR ADC. Although a single-ended version is shown here, the real implementation could be differential. There are two major differences between a CS SAR ADC and a conventional SAR ADC. One is that the input signal $\vec{s}$ is multiplied with a

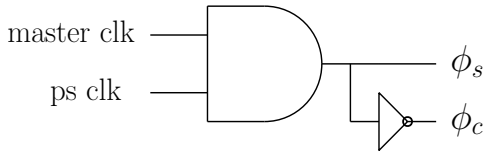
PRBS $\vec{p}$ to become a randomized sampling before being sampled. For a differential input signal, this sampling period is equivalent to the symbol status of the PRBS vector $\vec{p}$ which can be easily implemented by turning on and off the switch capacitor circuit. The other difference is that quantization does not happen after every-time sampling but only happens depending the number of following 0s after sampling taking place (1 in the PRBS vector). Before facing the next sampling period, the input signal is quantized in successive manner such as a conventional SAR ADCs and the quantization cycle is denoted as ϕ_5 in Fig. 2.5. ϕ_e is a bit earlier cycles of ϕ_1-ϕ_4 for bottom-plate sampling. Since the sampling power is usually negligible in a SAR ADC design, the quantization phase takes far less time compared to a conventional SAR ADC which quantizses every samples with the maximum quantization bits (in this case 12-bit) meaning that the proposed architecture can save the total power consumption in sampling and quantizing phases, and allows savings in memory space after conversion.

In Fig. 2.6, we plot important clock timing which explains the relation among random sequence clock ($diag(\mathbf{\Phi})$), master clock(ϕ_{clk}), sampling clock (ϕ_{sample}), and conversion clock (ϕ_{conv}) cycles which operate the SAR ADC architecture appearing in Fig. 2.3. Other system clocks are operated as the same as the conventional SAR ADC, but the conversion clock ϕ_{conv} is triggered with different operation scheme to produce extra quantization bits.

If sampling time instance has *1* in the diagonal element of the measurement matrix $\mathbf{\Phi}$, ϕ_{sample} triggers ϕ_{conv} to start conversion. Next, the conversion



(a) Clocking for sampling and conversion.



(b) Clock generator.

Figure 2.6: Sampling and conversion clock timings (a) and clock generator (b).

clock ϕ_c is triggered simultaneously to operate the comparator for the SAR process, and the DAC starts producing digital bits of the sampled signal. If sampling time instance has *0* in the measurement matrix, the sampling clock ϕ_{sample} stays low and prepares the ADC for the next conversion after producing conversion outputs to the DAC. The delay between the end of conversion bit and the next conversion clock ϕ_{conv} is to reset and prepare for the next conversion. There is the main difference between the conventional SAR ADC and the proposed architecture in clocking ϕ_{conv}. Although the the sampling clock ϕ_{sample} stays low, ϕ_{conv} is being triggered to produce extra bit(s) if there is following zero(s).

The new architecture requires minimum modification of the conventional SAR ADC and mostly compatible to the architecture. Thus, the pro-

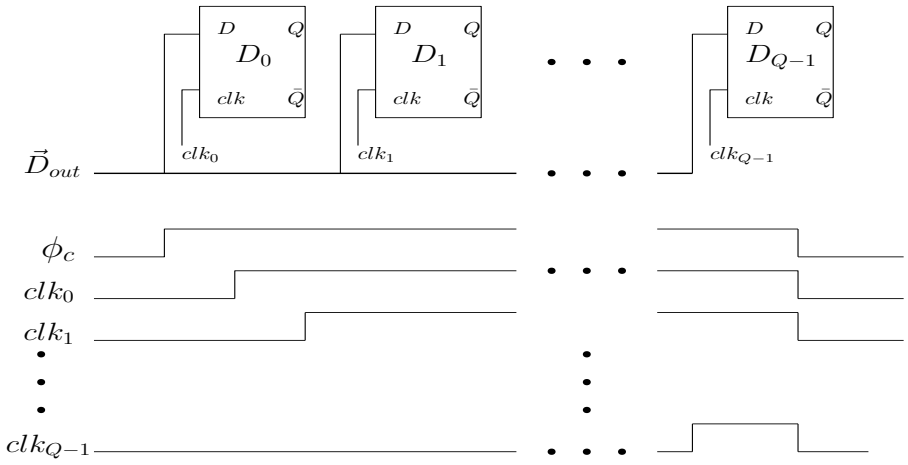


Figure 2.7: D flip-flop.

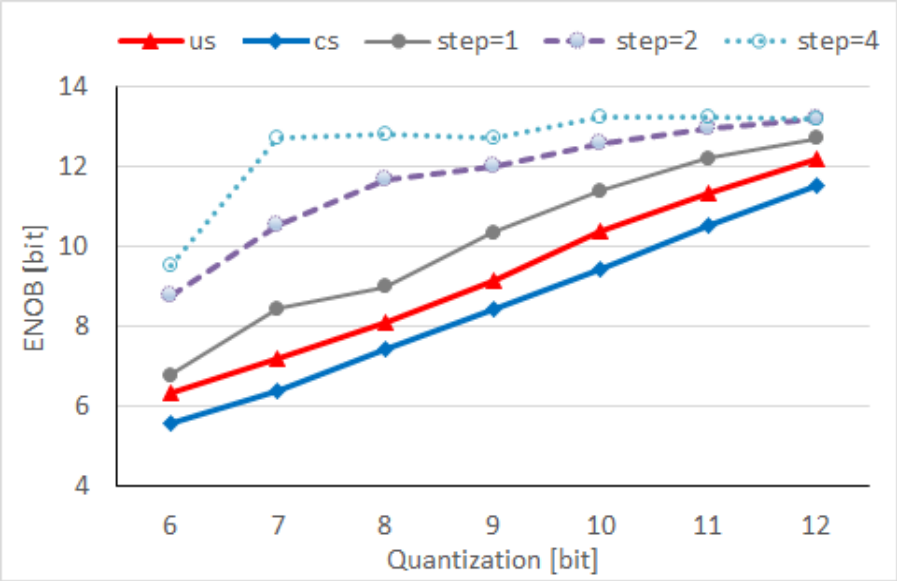
posed architecture is flexible to operate in a Nyquist-rate SAR mode for non-sparse signals.

2.4 Experiments

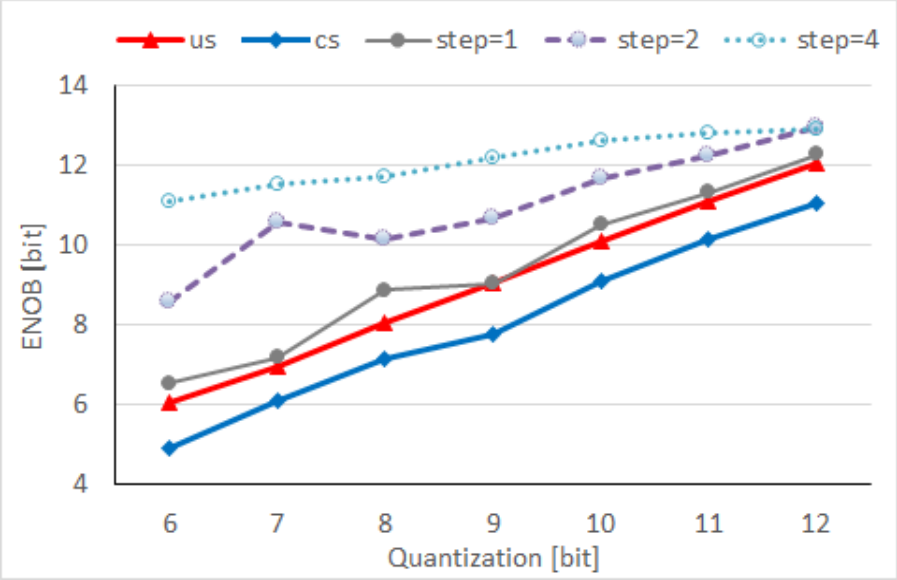
We compare the performance of the proposed sensing scheme to the uniform sampling (us) and traditional CS (cs) through MATLAB simulations. In the simulation, we explore the quantization scenarios with from 6 to 12-bit depth for the proposed quantization scheme. At each simulation case, 100 trials of simulation are performed and the results are averaged. Effective Number of Bits (ENOB) is investigated for comparison purpose and ENOB is defined as ENOB = (SQNR - 1.76) / 6.02 bit, where SQNR stands for signal-to-quantization noise ratio, the divisor 6.02 is for dB conversion, and the subtraction term of 1.76 is to compensate quantization error in an ideal ADC. Fig. 2.8 shows the comparison of ENOB (y-axis) vs. quantization level of SAR

ADC (x-axis) for input signals with $K \in \{3, 5, 10, 20\}$ sparseness in discrete Fourier transform domain. We compare ENOBs among uniform sampling (us), compressive sampling (cs), and the proposed quantization scheme with $step = \{1, 2, 4\}$. The x-axis indicates the quantization bit levels. For the result of us, it means ADC is uniformly quantized to this resolution. For cs, it performs random sampling with the fixed quantization levels. Lastly, the proposed scheme randomly samples the input with initial quantization bit from b_0 to b_r-bit which is described in Section 2.3.2.

As plotted in Fig. 2.8 (a) the proposed scheme outperforms us and cs schemes converting sparse input signals; (b) for inputs with low sparseness, the proposed scheme at least equivalent to us scheme; (c) for the least sparse signals in our simulation, us shows the best ENOB, but the proposed scheme works better than conventional cs-based sampling results. The performance of the proposed architecture is ruled by input signal sparseness with respect to the total number of measurements. The proposed system becomes more effective if the target input is sparser in the frequency domain. This is a expected result since the overall system is ruled by RIP condition in compressive sensing.

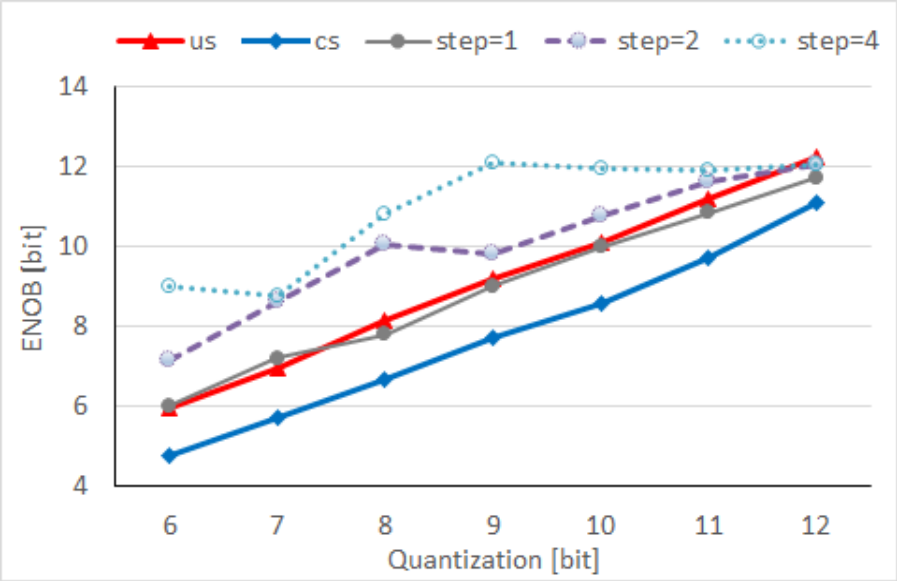


(a) $|x|_0 = 3$

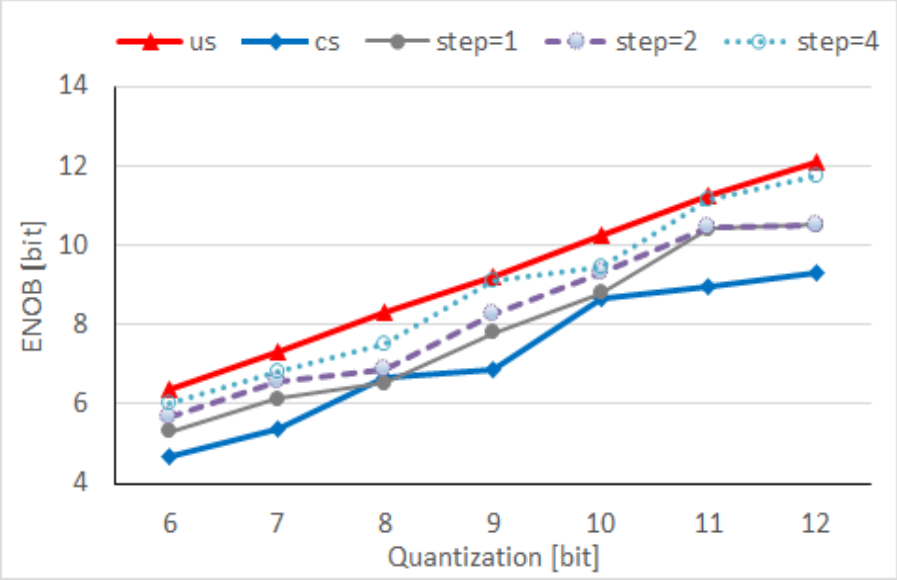


(b) $|x|_0 = 5$

Figure 2.8: Simulation results (high sparsity inputs).



(a) $|x|_0 = 10$



(b) $|x|_0 = 20$

Figure 2.9: Simulation results (low sparsity inputs).

2.5 Conclusion and discussion

In this chapter, a new sampling scheme has been presented that consists of a non-uniform quantization scheme with random sampling strategy. The proposed scheme is designed to increase the resolution of a SAR ADC making use of pre-defined PRBS which enables the acquisition of high-frequency signals with above 6-bit resolution, something that has proven challenging with conventional SAR ADC architecture. With the non-uniform quantization scheme, the average quantization noise is decreased. In addition, it provides higher quality signal recovery than the traditional CS-based sampling schemes.

This chapter has also discussed details regarding circuit level implementation in order to realize the scheme with SAR ADC architecture. The performance of CS-based sampling is mainly affected by the sparseness of signals, and this issue applies to the proposed scheme as well. In addition, the noise-folding effect that the CS strategy entails weakens the performance of CS-based sampling schemes. Thus, the proposed architecture may not be efficient for every type of signal, but it is ideal for band-limited sparse-signal acquisitions under moderate noise levels. For applications, gigahertz communication signals could be a potential candidate since they meet those requirements. In practice, there are multiple noise sources that can contribute to the total sum of noise levels, e.g. quantization and thermal noise. The proposed scheme reduces the total quantization noise in comparison with the conventional CS sample strategy, but the effect of other noise sources needs to be investigated in a subsequent study. Also, the future research should investigate the power

consumption of the proposed architecture, which is an issue that is not covered in this work. Nevertheless, the proposed non-uniform quantization strategy can be a possible method to overcome the sampling rate-and-precision limit that is a challenging problem in SAR ADC design, even with recent technological advancement.

Chapter 3

Multi-Channel Sparse-Signal Conversion

3.1 Introduction

Signal-processing applications such as sensor arrays, physiological signal monitoring, and brain machine interfaces (BMI), require digitization of multiple channels of analog signals. In BMI [21] and physiological signal acquisition [22], it is common to acquire up to 128 channels of simultaneous data [23, 24]. Also, in consumer electronics, multi-microphone technology is now the gold standard for speech enhancement [25]. In reference to the above mentioned examples, the question addressed in this chapter is whether or not it is necessary to linearly scale the analog hardware for each additional channel. We find that it is possible to use fewer analog-to-digital converters (ADCs) than channels by leveraging sparse representation of signals and blind source separation (BSS) techniques [26–28]. Compressive (compressed) sensing (CS) approaches have been and are being employed to try to reconstruct a signal at sub-Nyquist rates [29] with different levels of reconstruction accuracy. These approaches focus on recovering single channel [29, 30] or multi-band information [31] rather than multiple channel inputs as in the scenario we investigate.

Two straightforward approaches to performing multiple channel analog-

to-digital (A/D) conversion with a single ADC include time multiplexing and frequency multiplexing. In time multiplexing, all input channels are converted sequentially according to a multiplexing plan. However, when converting one channel, the information of other channels is not available. Therefore, the effective sampling rate per channel is given by the ADC sampling rate divided by the number of channels. This rate decreases as the number of channels increases, which is undesirable in energy-efficient sampling. In frequency multiplexing, the solution involves modulating the analog signals so that they occupy non-overlapping frequency bands and digitizing the sum of the modulated signal. The main drawback is that the required ADC sampling rate increases linearly with the number of channels leading to substantial power consumption.

The proposed solution is, in what follows, an alternative approach exploiting sparse-signal modeling of BSS with a known mixing matrix, which turns out an informed source separation (ISS) model [26], and sparse reconstruction methods, widely used in CS systems. In particular, this chapter considers the problem of using a single ADC or quantizer system to digitize multi-channel inputs that consist of an unknown number of sinusoids of unknown frequencies. For realizing the proposed system, we design switched-capacitor(SC)-based sampling and hold (S/H) circuits implementing the mixed signal block. Such systems perform the A/D conversion using discrete-time operations implemented in the analog domain.

In the proposed solution, the M-channel signals are sampled at the

Nyquist rate that is the same rate as a single-channel sampling case. However, the rate can be increased at a slightly higher rate if the input signals have lower sparseness levels than expected. The increased rate is determined by the maximum number of sinusoids in the input signals. The samples of the input signals are summed after multiplication by carefully selected pseudo-random binary sequences (PRBS) [32] of plus and minus ones (± 1) that can be implemented via polarity reversal of SC circuits. The single ADC or quantizer converts the mixture into digital sequences, and then the resulting output is separated into digitized sequences corresponding to the channel inputs at a DSP block. The overall architecture of the proposed ADC system for digitizing two input signals using a single quantizer is shown in Fig. 3.2. We can linearly extend the number of input channel by simply adding the same input circuit block if the input signals are guaranteed sufficient sparseness after the channel extension. Each signal is assumed to have a sparse representation in a known dictionary; that is, over any interval of time, each signal can be reconstructed using a number of dictionary entries that is lower than the number of degrees of freedom associated with that time interval.

3.2 Problem Formulation

3.2.1 Sparse-Signal Mixture Model

For simplicity of exposition, we assume here that we are dealing with a signal that consists of a random superposition of a random number of columns of the N-point discrete Fourier transform (DFT) matrix. We can represent

the m^{th} channel $N \times 1$ signal vector $\vec{s}_m$ in terms of N-point DFT matrix $\mathbf{F}$ that consists of $N \times 1$ column vectors $\vec{f}_n = \frac{1}{\sqrt{N}} exp\{-j2\pi k(n-1)/N\}$, where $n = 1, 2, \cdots, N$ that indicates n^{th} column, $k = 0, \pm 1, \cdots, \pm \lceil N/2 - 1 \rceil$, and a $N \times 1$ coefficient vector $\vec{\alpha}$ as,

$$\vec{s}_m = \mathbf{F}\vec{\alpha} = \sum_{n=1}^{N} \alpha_{m,n} \, \vec{f}_n, \tag{3.1}$$

where $m = 1, \cdots, M$ that indicates channels, and $\alpha_{m,n}$ is the n^{th} entry of a sparse coefficient vector $\vec{\alpha}_m$ corresponding to the dictionary atom $\vec{f}_n$. If the signal vector $\vec{s}_m$ is K_m-sparse, then its coefficient vector $\vec{\alpha}_m$ has K_m nonzero entries. Each channel input is now modulated with spreading sequence vector $\vec{p}_m$ associated with m^{th} input channel as,

$$\vec{x}_m = \vec{p}_m \, \vec{s}_m. \tag{3.2}$$

Subsequently, we obtain the mixture of the modulated signal vectors which has the same bandwidth of the input signal,

$$\vec{y} = \sum_{m=1}^{M} \vec{x}_m, \tag{3.3}$$

where $\vec{y}$ is a $N \times 1$ vector. The observation vector $\vec{y}$ can be written with respect to the equation (3.1) as,

$$\vec{y} = \sum_{m=1}^{M} \sum_{n=1}^{N} \alpha_{m,n} \, \vec{p}_m \, \vec{f}_n. \tag{3.4}$$

Now, we define a $N \times L$ union of dictionary $\mathbf{A}$, where $L = MN$ and $\mathbf{A} = [\mathbf{A}_1 \; \mathbf{A}_2 \; \cdots \; \mathbf{A}_M]$. The measurement matrix $\mathbf{A}$ consists of submatrices $\mathbf{A}_m$ obtained from modulating each column vector of the N-point DFT matrix $\mathbf{F}$

with spreading sequence vectors $\vec{p}_m$. In other words, the augmented measurement matrix $\mathbf{A}$ consists of the modulated DFT dictionaries $\mathbf{A}_m = \left[\vec{p}_m \ \vec{f}_n\right]$, where $n = 1, 2, \cdots, N$. With the augmented dictionary $\mathbf{A}$, we obtain the measurement vector as,

$$\vec{y} = \mathbf{A}\vec{\alpha}, \tag{3.5}$$

where $\vec{\alpha}^\top = \left[\vec{\alpha}_1^\top, \vec{\alpha}_2^\top, \cdots, \vec{\alpha}_M^\top\right]$. This forms an under-determined system, and we pictorially illustrate the system equation in Fig. 3.1. By accurately estimating the coefficient vector $\vec{\alpha}$, each input $\hat{s}_m$ can be recovered as,

$$\begin{bmatrix} \hat{s}_1 \\ \hat{s}_2 \\ \vdots \\ \hat{s}_M \end{bmatrix} = \begin{bmatrix} \mathbf{F} & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \mathbf{F} & \cdots & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \cdots & \mathbf{F} \end{bmatrix} \begin{bmatrix} \hat{\alpha}_1 \\ \hat{\alpha}_2 \\ \vdots \\ \hat{\alpha}_M \end{bmatrix}, \tag{3.6}$$

where $\hat{\alpha}_m$ is an $N \times 1$ vector. We pictorially illustrates the equation (3.5) in Fig. 3.1.

Now, we arrive at the question that is how to estimate a sparse solution of (3.5). In practice, a variety of convex [33, 34] or greedy algorithms [35, 36] have been suggested that yield a sparse coefficient vector $\vec{\alpha}$. We introduce three major classes of algorithms in the following subsection.

3.2.2 Signal Reconstruction

Let us discuss the problem of constructing the digitized sequences corresponding to all channel inputs using their sparse-signal structures and reconstruction algorithms that are widely used in the CS community. This can be done by identifying the sparse representation of the mixture in terms of

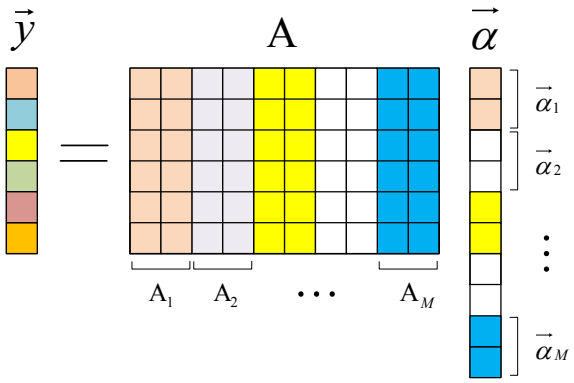


Figure 3.1: The mixture signal model ($\vec{y}$) with the augmented measurement matrix ($\mathbf{A}$) and the concatenated coefficient vector ($\vec{\alpha}$).

the union of the dictionaries corresponding to the signals in the mixture. In our discussion, we seek a sparse representation of the mixture in terms of the union of a modulated DFT matrix. The coefficients corresponding to entries drawn from the modulated DFT matrix will be used to reconstruct the digitized sequence corresponding to each channel. The theory extends naturally to the general case when we are dealing with an arbitrary number of sinusoids of arbitrary frequencies.

The ability to reconstruct the desired digitized sequences hinges on our ability to find the sparsest signal representation of the mixture. There are two major algorithms to find a sparse solution of under-determined system set-up [37], ℓ_1 linear/convex optimization approaches [38, 39], and greedy approaches [40–42].

Approach 1: The first family of methods that provides a sparse solution of an under-determined systems is the traditional ℓ_1 convex/linear optimization methods defined as,

$$\begin{aligned} \underset{\vec{\alpha}}{\text{minimize}} \quad & \|\vec{\alpha}\|_1 \\ \text{subject to} \quad & \vec{y} = \mathbf{A}\vec{\alpha}. \end{aligned} \tag{3.7}$$

There have been reported different recovery methods that produce the solution of the optimization problems. LASSO-styled ℓ_1 sparse recovery method [38, 39] is a widely used method in this category regularizing ℓ_1 optimization problems such as,

$$\underset{\vec{\alpha}}{\text{minimize}} \quad \frac{1}{2}\|\mathbf{A}\vec{\alpha} - \vec{y}\|_2^2 + \lambda \|\vec{\alpha}\|_1 , \tag{3.8}$$

where λ is a positive regularizing parameter. The methods are belong to this family can be implemented by linear programming techniques, and they have $O(N^3)$ complexity to recover signal vector with length N [4].

Approach 2: The second class of sparse representation methods is greedy methods. The orthogonal least square (OLS) [40], orthogonal matching pursuit (OMP) [43], and compressive sampling matching pursuit (CoSaMP) [42] belong to this category, and they have $O(NK^2)$ complexity in general where K is the number of signal components [36]. The OLS approach is similar to the OMP but uses a different directional update scheme. A simple modification of the OLS outperforms other methods. The modification consists of drawing at

each step simultaneously elements from each of the dictionaries in the union of spread dictionaries that provide a sparse representation of the mixture. That is, in our illustration, in each step we would select one column from the spread DFT matrix $\mathbf{A}_m$. In contrast, the traditional OLS method selects only one entry from the signal dictionary $\mathbf{F}$ at each step. The OLS steps are describe as following:

Algorithm 1 Multi-channel OLS procedure

1) Initialization
   $q = 0,\ r^0 = y,\ \hat{y}^0 = 0,$
   $\Omega_m^0 = \{1, 2, \cdots, K_m\}$, for all $m = 1, 2, \cdots, M$
   $\Gamma^0 = \oslash,\ W = \{d_{i_m}\}_{i_m \in \Omega_m^0}$
2) While stopping criteria are not met
   a) $q = q + 1$
   b) Pick atom with maximum correlation to residual
      $i_m^q = \arg\max_{j_m} |< w_{j_m}, r^{q-1} >|, j_m \in \Omega_m^{q-1}$
   c) Remove atom index from set and add to set Γ
      $\Gamma^q = \Gamma^{q-1} \otimes q^l$
      $\Gamma^q = \Gamma^{q-1} \cup i_m^q$
   d) Update residual and approximation
      $r^q = r^{q-1} - \sum_{i=1}^{M} < w_{i_m^q}, r^{q-1} > w_{i_m^q}$
      $\hat{y}^q = \hat{y}^{q-1} + \sum_{i=1}^{M} < w_{i_m^q}, r^{q-1} > w_{i_m^q}$
   e) Decorrelate remaining dictionary atoms from $w_{i_m^q}$
      such that for all $j_m \in \Omega^q$,
      $w_{j_m} = w_{j_m} - < w_{j_m}, w_{i_m^q} > w_{i_m^q}$
      $w_{j_m} = w_{j_m} / \|w_{j_m}\|_2$
   f) Check stopping criteria

Approach 3: It is also possible to use a reconstruction technique that combines advantages from ℓ_1 and ℓ_2 minimization methods. We promote better

reconstruction performance than each independent method. The combined $\ell_{1,2}$ method consists of two steps. First, a collection of frequency index to represent the m^{th} channel input $\vec{s}_m$, is estimated from a ℓ_1 solution such that $I_m = \{1 \leq i \leq N | \, |\alpha_{m,i}| > \epsilon\}$, where ϵ is a positive thresholding value slightly greater than zero, and $\alpha_{m,i}$ is the i^{th} entry of the coefficient vector $\vec{\alpha}_m$. Secondly, we compute a least square solution $\tilde{\alpha}$ using a new dictionary formed by column vectors that belongs to I_m from the modulated matrix A_m, $\underset{\tilde{\alpha}_m}{minimize} \left\| \vec{y} - \sum_{i \in I_m} \vec{f}_{m,i} \tilde{\alpha}_{m,i} \right\|_2$, where $\vec{f}_{m,i}$ is the i^{th} column vector of A_m. The recovery is performed as, $\vec{s}_m = \sum_{i \in I_m} \tilde{\alpha}_{m,i} \, \vec{f}_i$.

General Case: In the general case, the signal can be represented with an overcomplete dictionary with columns of the form $\vec{f}_n = \left[e^{-j\omega_n k}\right]$, where $\omega_n = n\Delta\omega$ and $\Delta\omega$ is chosen to provide the decreased frequency resolution.

These frequencies $\{\omega_n\}$, where $n = 1, 2, \cdots, N$, are used to generate the columns of the dictionary $\vec{f}_n = \left[e^{-j\omega_n k}\right]$. The augmented measurement matrix will then consist of the modulated dictionary elements, $A_m = \left[\vec{p}_m \; \vec{f}_n\right]$.

3.2.3 Incoherent Sampling and Signal Sparseness

Let us think about the sensing model of N measurements of MN-length signal of interest $\vec{x}$ such that

$$\vec{y} = \Phi \vec{x} \tag{3.9}$$

where the sensing matrix Φ has a dimension of $N \times (MN)$, and $M > 1$. In the noiseless case, the coherence-based recovery guarantee [44] can be obtained by the following theorem.

Theorem 3.2.1. *[45] Suppose the signal $\vec{x}$ is taken from the generic K-sparse model. If*

$$\sqrt{\mu^2 K \cdot c_0 \cdot \log MN} + \frac{K}{MN}||\Phi||_2^2 \leq C, \tag{3.10}$$

where a positive constant $c_0 \geq 1$, and $C > 0$, then $\vec{x}$ is the unique solution to ℓ_1 minimization programming with probability $1 - (MN)^{-c_0}$.

Abusing the MATLAB notation, with the measurement matrix Φ which has unit norm columns such that $||\Phi(:, i)||_2^2 = 1$, the coherence of matrix Φ is defined as

$$\mu(\Phi) = \max_{1 \geq i \neq j \geq (MN)} | < \Phi(:, i), \Phi(:, j) > |, \tag{3.11}$$

where $\Phi(:, i)$ denotes i-th column of the measurement matrix Φ. The coherence value is bounded by $[\mu_{min}, 1]$ and the lower bound μ_{min} is known as the Welch's bound [46] which is computed as $\mu_{min} = \sqrt{\frac{M-1}{MN-1}}$. By Hölder's inequality, the norm of sensing matrix Φ has lower bound

$$||\Phi||_2^2 = ||\Phi^H \Phi||_2^2 \geq \frac{\text{trace}(\Phi^H \Phi)}{N} = M. \tag{3.12}$$

In the noisy case, K-sparse signal $\vec{x}$ can be identified using the unconstrained LASSO with high probability provided that the nonzero coefficients have higher amplitudes than that of the noise signal [47]. In both theorems, it can be observed that smaller coherence $\mu(\Phi)$ of the sensing matrix supports

better recovery guarantees, and this is the crucial point designing the sensing matrix.

3.3 System Design

The proposed system consists of two blocks, a mixed signal block and a digital signal processing (DSP) block. The mixed signal block includes sample-and-hold (S/H) circuits, modulators, adders, and a single ADC or quantizer. The DSP block is to separate channel inputs $\hat{s}_1[n], \hat{s}_2[n], \cdots, \hat{s}_m[n]$ from the mixture $y[n]$ running a reconstruction algorithm, and generates different spreading sequences for channel modulation. In an actual system, S/H circuits, modulators, and adders are implemented using SC circuits. In the proposed architecture, we implement these operations in the mixed signal block, and we describe the details in Section 3.4.

3.3.1 Sampling Rate

We discuss the sampling rate here in the context of reconstructing signals that are quasi-stationary[1] over time intervals of length T. We also assume that each signal consists of a superposition of an unknown number of unknown sinusoids over short fixed intervals of T. The sampling rate f_s is selected such that the number of samples in any time interval T is larger than the sum of the

[1] A discrete-time signal $\{x[n]\}_{n=1}^{N}$ is quasi-stationary if $E\{x[n]\}$ is bounded for every N such that, $R_x(\tau) = \lim_{N\to\infty} \frac{1}{N} \sum_{n=1}^{N} E\{x[n]x[n+\tau]\}$, and the signal has spectral density, $\Phi_x(\omega) = \sum_{\tau=-\infty}^{\infty} R_x(\tau) e^{-j\omega\tau}$.

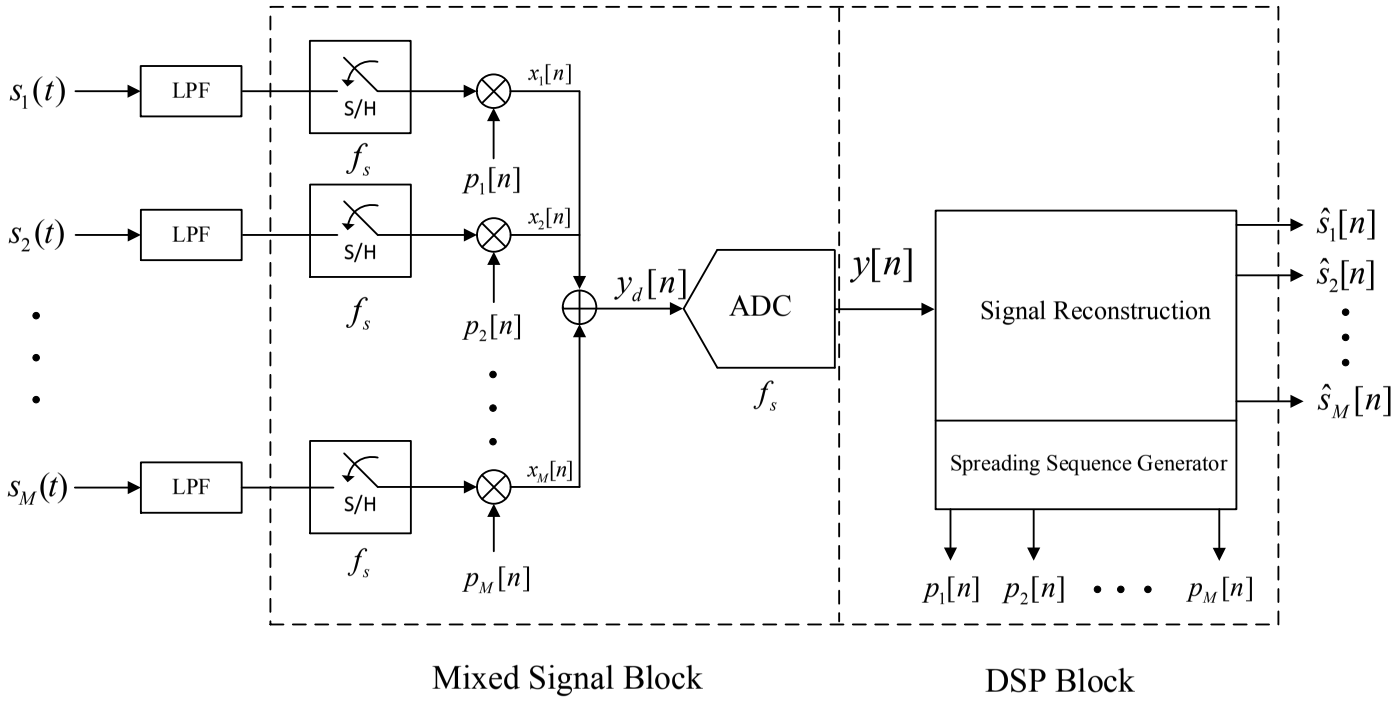


Figure 3.2: Proposed system architecture with M channels and a single ADC, and the system consists of a mixed signal block and a DSP block. $y_d[n]$ is the discrete-time mixture signal after summing all the modulated channel inputs, and $y[n]$ means the digital signal after quantizing the discrete-time signal.

total numbers of frequency components in the M channel inputs. For example, let us assume that at the Nyquist sampling rate, the time interval over which the signals are quasi-stationary consists of N samples. Furthermore, assume that each signal consists of a random superposition of a random number of columns of the N-point discrete Fourier transform (DFT) matrix. Then reconstruction from signals sampled at the Nyquist is possible only if the sum of the numbers of frequency components in the M channel inputs is less than $N/2$. In other words, for signals that are quasi-stationary over intervals of length T, the sampling rate f_s needs to provide in any time interval T a number of samples $N = Tf_s$ such that N is larger than the sum of the total numbers of dictionary atoms required to express each of the M channel inputs.

3.3.2 Modulation and Mixing

The main challenge in the proposed system is the separation of the samples of the signals after they have been modulated and summed. If the input signals are band-limited and sparse in a known domain, the channel inputs can be represented by a sparse representation method with a linear combination of dictionary atoms, column vectors of the dictionary, and coefficient vectors corresponding to each atom.

To address these challenges, we modulate every channel inputs by a properly designed sequences. We select to use sequences of ± 1 to perform the modulation. Such a modulation scheme can be simply implemented using polarity reversal. Furthermore, it avoids amplifying or attenuating the signal

samples. Finally, demodulation is very simple as it consists of multiplying the signal samples by the same sequence used in the modulation stage. Amongst all possible sequences of ± 1, we seek a sequence that will simplify the signal reconstruction problem. After modulation by such a sequence, each modulated dictionary atom must have a non-sparse representation in terms of the original dictionary.

3.3.3 Selection of Mixing Sequences

In practice, we need to select a pseudo-random sequence of ± 1. Several classes of PRBS with efficient correlation properties are reported in the communication studies such as maximum length, Gold [48], Kasami [49], and Hadamard [50] sequences. Auto- and cross-correlation properties of the sequences are important. Hadamard sequences are reported to offer a poor spectral estimation probability because they show multiple peaks in their cross-correlation function [31]. Kasami sequences are regarded as the optimal choice in communication, but the sequences also yield many peaks at the Welch's bound level. Contrary to Hadamard and Kasami sequences, maximum length and Gold sequences yield peaks with lower aggregate energy than other sequences, and both sequences show similar probability of successful reconstruction performance [31]. Gold sequences are proposed in 1967 [48], and constructed by EOR-ing two maximum length sequences. Due to this inherent property from generation, Gold sequences have better cross-correlation property than maximum length sequences. Thus, the Gold sequences is the optimal

Table 3.1: Types of pseudo-random sequences.

Types	Set of pairs	r	μ
Maximal	$2^r + 1$	even and odd	≥ 1
Gold	$2^r + 1$	odd	$\leq 1 + 2^{\frac{r+1}{2}}$
Gold	$2^r + 1$	even	$\leq 1 + 2^{\frac{r+2}{2}}$
Kasami (small)	$2^{(r/2)}$	even	$\leq 1 + 2^{\frac{r+2}{2}}$
Kasami (large)	$2^{(r/2)}(2^r + 1) - 1$	even and mod(r,4) = 2	$\leq 1 + 2^{\frac{r+2}{2}}$

*r is a positive integer and each method has $N = 2^r - 1$ sequence length.

choices to modulate each channel input with ± 1 sequence guaranteeing minimum coherence in Theorem 3.10. We compare the cross-correlation (μ) and other characteristics of these peudo-random sequences in Table 3.1.

3.3.4 Comparison with Conventional CS

In this subsection several differences between our sparse data converter and conventional CS approaches are addressed. The proposed system uses the same PRBS as conventional compressed sensing, but the proposed architecture uses the sequences with a different way. In CS approaches, the sequences are to compute random projections of the input signal. Thus, the input signal is multiplied in the analog domain by the ± 1 sequences, leading to bandwidth expansion. The multiplication is followed by integration to compute a projection. Following that, an integrator [29] is required before or after modulating input signals (see Fig. 3.3 (a)). Readers may refer recent studies exploiting CS techniques in [30]. In contrast, we do not compute projections and do not need integrators after modulation (see Fig. 3.3 (b)). The modulation in our system

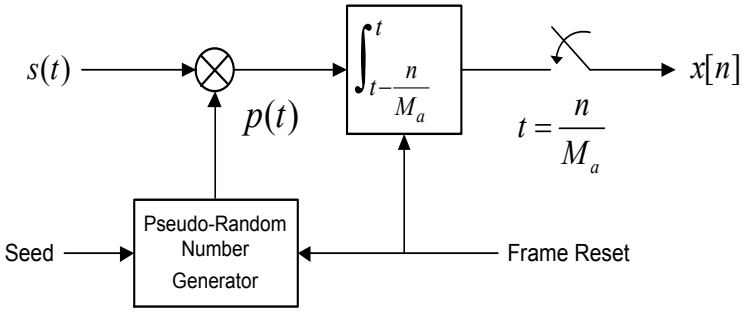
is a discrete-time operation, albeit implemented in the analog domain using SC circuits. Its purpose is to maximally decorrelate the dictionaries used to represent different input signals.

3.4 Circuit Level Realization

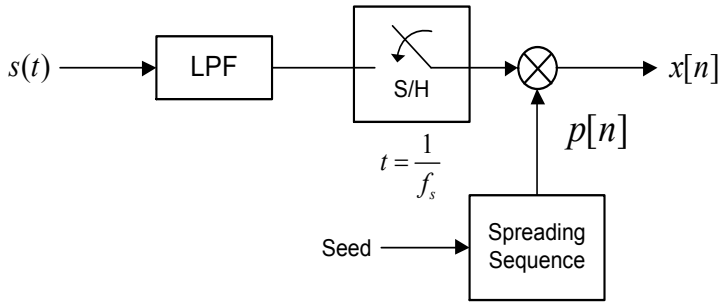
In this section, we will discuss the circuit level realization concentrating on the mixed signal block and the single-channel ADC for the proposed ADC system. For simplicity, we explain the proposed system with two channel inputs instead of M channels and a single ADC. The number of input channels in our proposed system is linearly scalable, and we can increase the number of channels by minimal modifications of the mixed signal block and reconstruction algorithms in the DSP block with the identical mixed signal block as in Fig. 3.2. However, the increased channel inputs are spread over the same bandwidth as the two-channel case. Thus, the input bandwidth needs to be tightened by LPFs depending on the sparseness of the input signals.

3.4.1 Selection of ADC

We do not require special design for the single-channel ADC (see Fig. 3.2). It can be implemented using various types of ADC structures, including flash, folding and interpolating, pipelined [5, 6], and successive approximation register (SAR). If the pipelined structure is adopted, which is suitable for high-speed (10MHz to 1GHz) and medium resolution (8 to 14 bits) applications, we can reduce the overall circuit power by merging the first-stage of the pipelined



(a) Random modulator (RD).



(b) Proposed sparse data converter.

Figure 3.3: Modulation and sampling of the conventional RD and the proposed system.

ADC with the mixed signal block of Fig. 3.4, following the design principles of [6, 51].

3.4.2 Switched-Capacitor-Based Modulation

The reason for using the SC circuit to implement the mixed signal block is its high linearity [52]. Assuming the OTA is ideal, the precision of the analog operation in equation (3.13) is set by capacitor ratios, which are insensitive to process, voltage, and temperature (PVT) variations. Switch nonidealities, including nonlinear resistance, clock feed-through, and charge injection, can be effectively addressed by existing circuit techniques, such as bottom-plate sampling [53, 54] and clock bootstrapping [55, 56]. In real implementation, the linearity of the SC circuit is likely to be limited by OTA nonidealities, such as nonlinear output resistance. To ensure adequate OTA linearity, we can use gain boosting techniques and calibration techniques [20, 57].

3.4.3 Mixed Signal Block

The mixed signal block of the proposed two-channel ADC shown in Fig. 3.4 can be efficiently implemented using SC circuits with high linearity. Fig. 3.4 shows one SC circuit example that implements altogether the functions of random modulation, S/H, and summation. The waveforms of the clocks that control the switches are shown at the bottom of Fig. 3.4.

$$\vec{y} = \left(\vec{p}_1 \otimes \vec{s}_1 + \vec{p}_2 \otimes \vec{s}_2\right)/2, \tag{3.13}$$

where $\otimes$ represents elementwise vector multiplication.

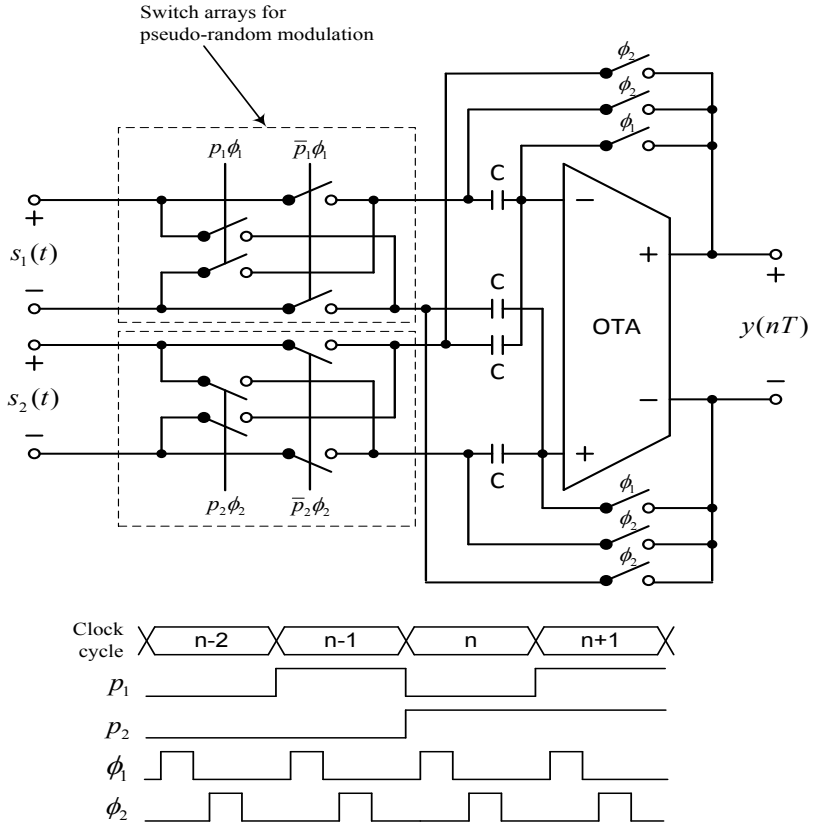
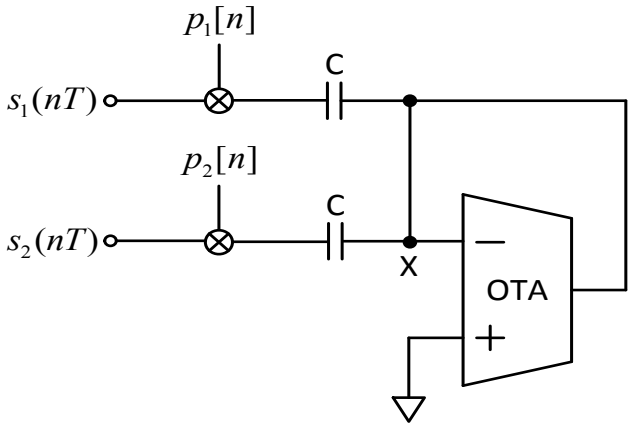
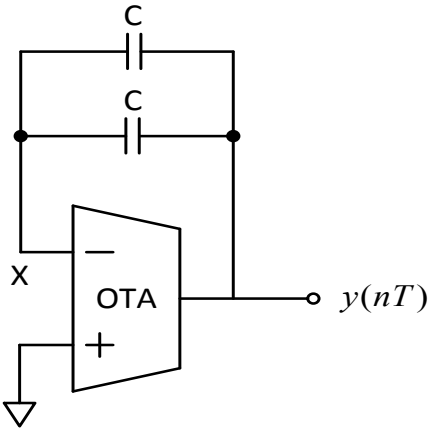


Figure 3.4: Optimized mixed-signal block based on SC circuit.



(a) The sampling phase when ϕ_1 is high.



(b) The summation phase when ϕ_2 is high.

Figure 3.5: Simplified single-ended block diagrams.

The mixed signal block has two operation phases, controlled by two non-overlapping clocks ϕ_1 and ϕ_2. When ϕ_1 is high, the SC circuit operates in the sampling phase, whose simplified single-ended block diagram is shown in Fig. 3.5(a). In this phase, the operational transconductance amplifier (OTA) is configured in unity feedback to ensure that node X is a virtual ground. The two input signals $\vec{s}_1$ and $\vec{s}_2$ are multiplied with $\vec{p}_1$ and $\vec{p}_2$ by the switch arrays (see Fig. 3.4), and the products are sampled on two capacitors. When ϕ_2 is high, the SC circuit operates in the summation phase, in which the capacitors are reconfigured to be placed across the OTA, as shown in Fig. 3.5(b). Assuming the SC circuit completely settles at the end of this phase, we can prove, based on charge conservation at node X, that: Although there is a divide-by-2 operation in the equation (3.13), which is different from the mixed signal block shown in Fig. 3.2, this gain error can be compensated by scaling the output of the single-channel ADC in the digital domain.

3.4.4 Digital Back-End

The major role of the DSP block is to separate and reconstruct each channel input accurately from the digitized mixture using convex optimization or greedy methods. The block also needs to produce PRBS to spread channel inputs over the available mixture bandwidth. The spreading sequences such as maximum length and Gold sequences can be iteratively generated using a set of shift registers [58], but we uses pre-computed sequence patterns. The selection of spreading sequences determines the pattern of ± 1, and then the

pattern can be pre-stored in memory devices inside the DSP block. The S/H circuits use the pattern to spread each input before summing them. Also, the stored sequence patterns are referred in the separation process as well because the separation is performed with the modulated dictionaries. In addition, the DSP block performs framing and windowing the digitized mixture signals for block-wise recovery of the input signals.

3.5 Simulation Results

In this section, we demonstrate simulation results of the proposed system corresponding to digitized sparse input signals. To find ℓ_1 and LASSO solutions, we write MATLAB codes based on disciplined convex programming with CVX [59]. Also, the reconstruction algorithms that recover the input signals in the DSP block are simulated via MATLAB programming as shown in Fig. 3.6. To evaluate input signal occupancy versus reconstruction fidelity, we first synthesize multi-tone signals that consist of K_m number of random integer frequency components. The frequency components and amplitudes of sinusoids are randomly selected within the available bandwidth. The mixture of each channel signal is sampled at 512Hz, and then we compute SRERs. Figs. 3.7 to 3.9 illustrates the results of MATLAB simulations. To show the multi-channel capability of the proposed architecture, we increase the number of channels from two to four channels. We found empirically greedy methods outperform ℓ_1 methods for input signals with moderate occupancy ($\leq 50\%$) in Figs. 3.7 to 3.9.

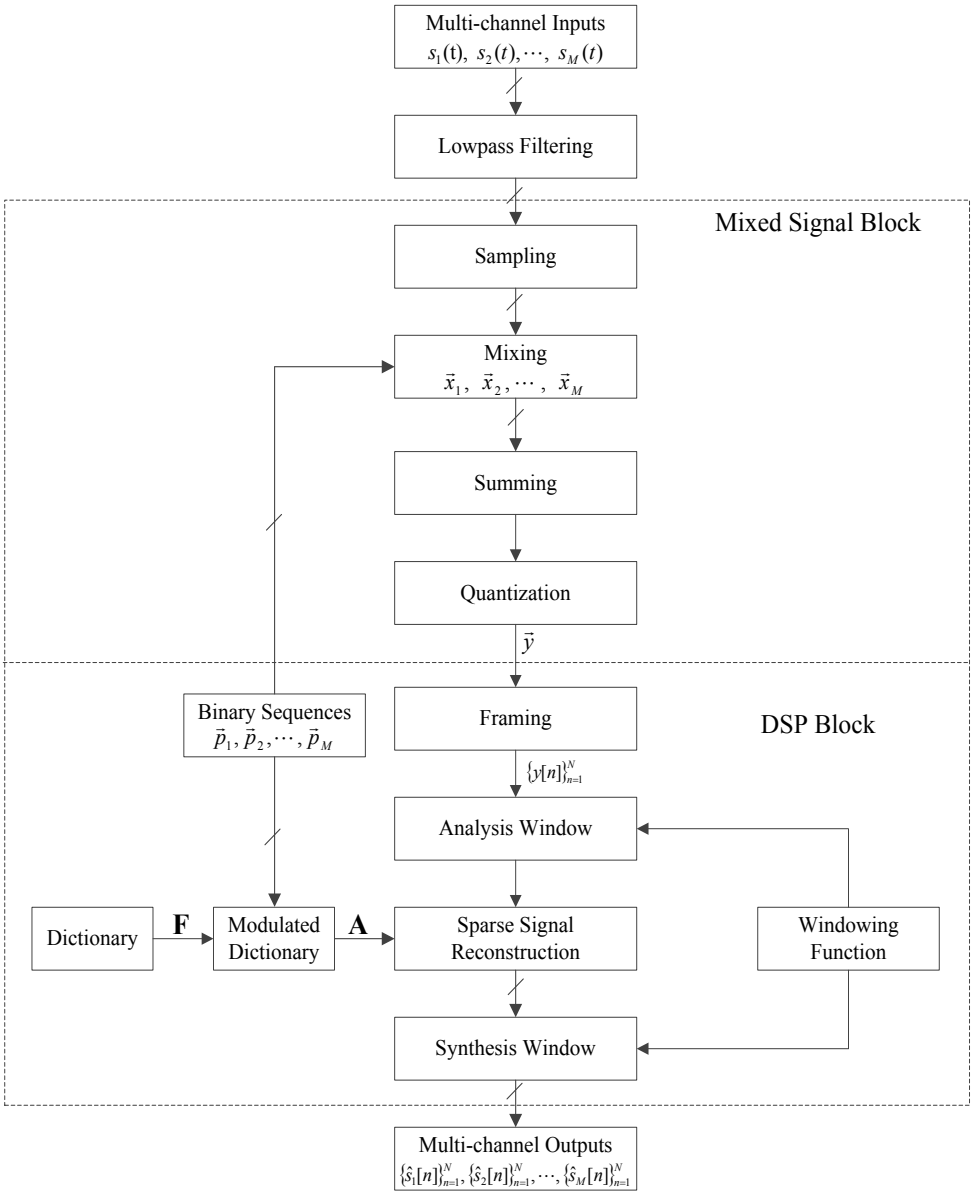


Figure 3.6: Simulation procedure with the proposed architecture.

3.5.1 Occupancy and SRER

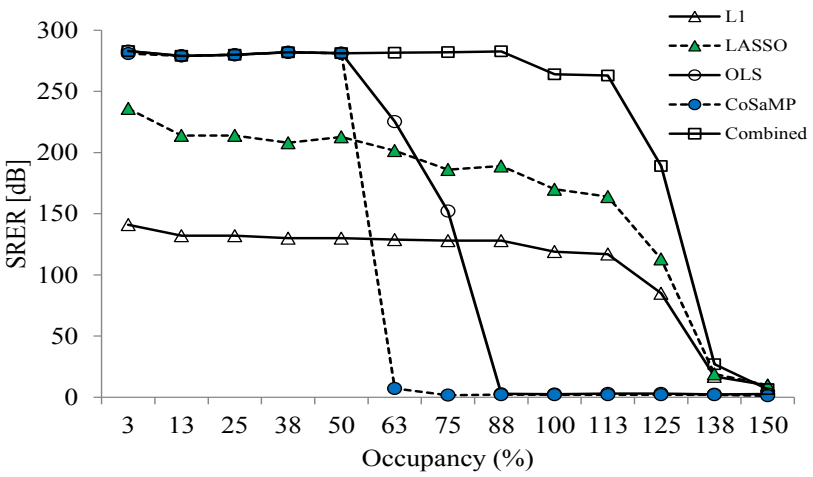
The sparse reconstruction algorithms introduced in Section 3.2.2 are tested for comparison. To evaluate the fidelity between the input and corresponding reconstructed signals, we define the reconstruction signal-to-reconstruction-error-ratio (SRER) as,

$$\mathrm{SRER}(\vec{s}, \hat{s}) = 20 \log_{10} \left(\frac{\|\vec{s}\|_2}{\|\vec{s} - \hat{s}\|_2} \right), \tag{3.14}$$

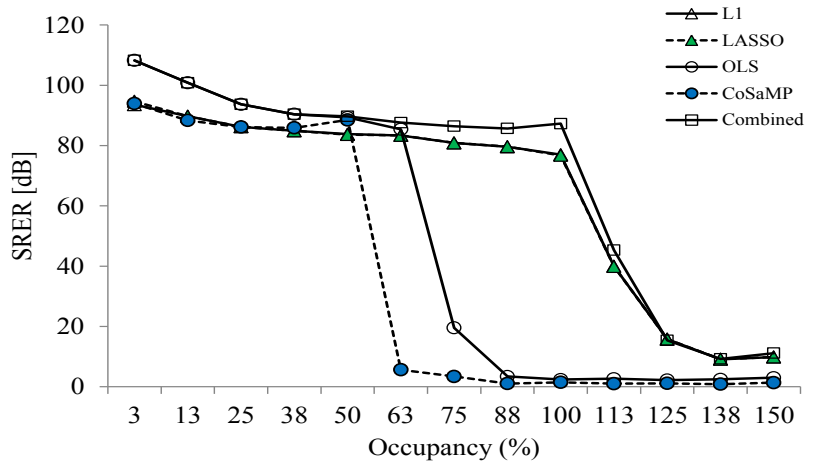
where $\vec{s}$ is the input signal, and $\hat{\mathbf{s}}$ is its recovery signal. To see the relationship between input signal sparsity versus the reconstruction performance, we need to define a metric for sparseness measure clearly. Because readers may be confused to see the sparseness of the input or mixture signals, we compute a percentage of the frequency components that embedded in all input signals. With this idea, we define the occupancy of frequency components within the mixture signal as,

$$\text{Occupancy } (\%) = \frac{\sum_{m=1}^{M} K_m}{B\,T} \times 100, \tag{3.15}$$

where K_m is the number of frequency components of the m^{th} channel input, B is the mixture bandwidth, and T is the sampling time interval. The simulation performed 100 times with synthesized inputs, and the input signal is of randomly selecting K_m frequency components. In Figs. 3.7 to 3.9, the horizontal axis indicates the occupancy of the synthesized input signals, and the vertical axis shows resulting SRERs.

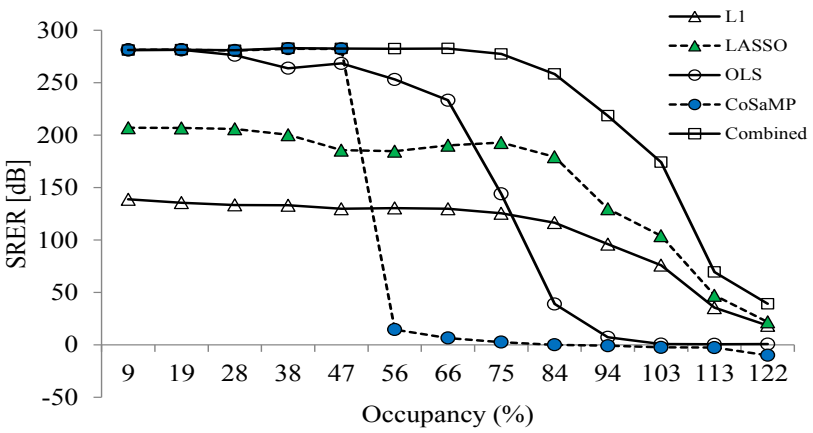


(a) Ideal ADC case without quantization noise.

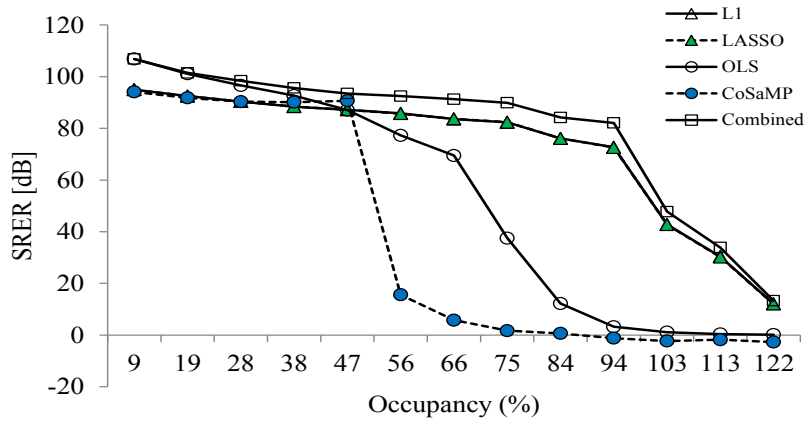


(b) Realistic ADC case with 16-bit quantization noise.

Figure 3.7: Simulation results of multiple-channel inputs with ideal and 16-bit ADCs: Two-channel inputs ($M = 2$).

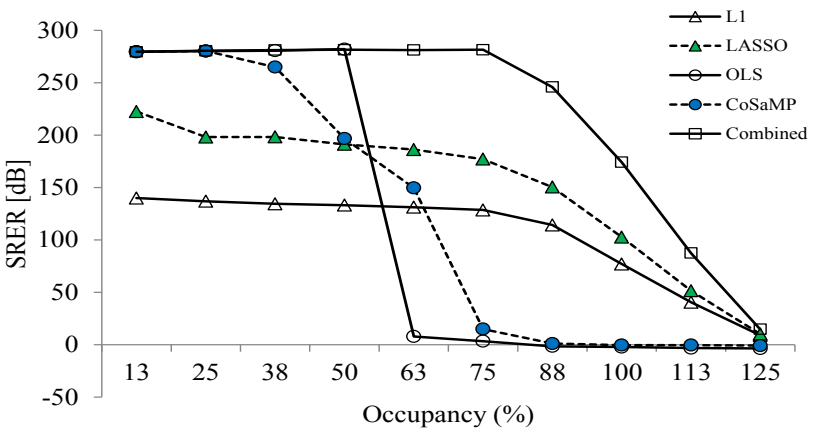


(a) Ideal ADC case without quantization noise.

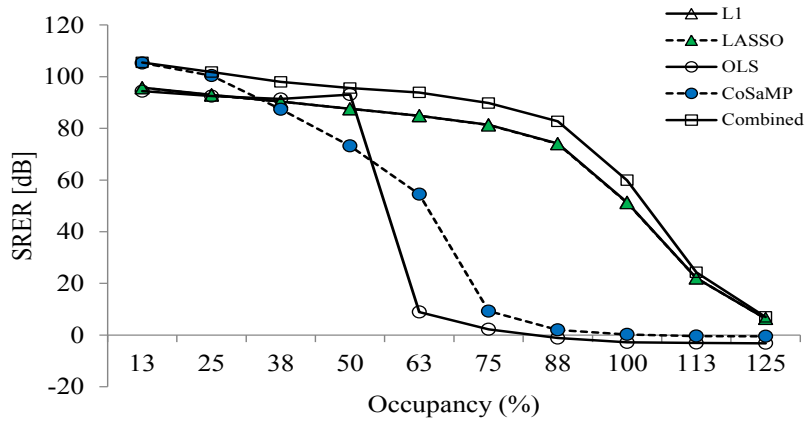


(b) Realistic ADC case with 16-bit quantization noise.

Figure 3.8: Simulation results of multiple-channel inputs with ideal and 16-bit ADCs: Three-channel inputs ($M = 3$).



(a) Ideal ADC case without quantization noise.



(b) Realistic ADC case with 16-bit quantization noise.

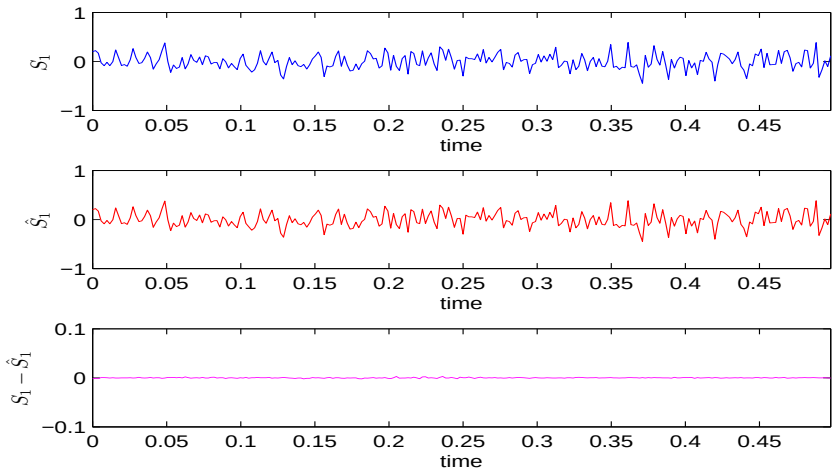
Figure 3.9: Simulation results of multiple-channel inputs with ideal and 16-bit ADCs: Four-channel inputs ($M = 4$)

Table 3.2: Windowing and recovery improvements

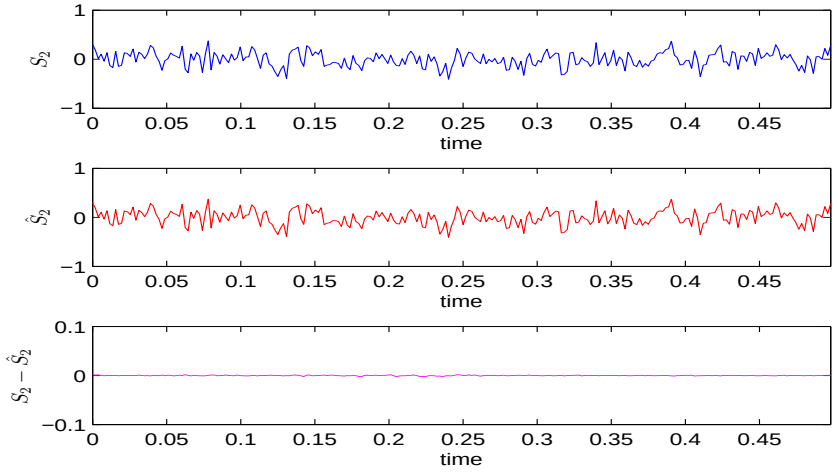
Category	**Type**	**Improvements**
Window Functions	Hanning, Hamming, Sine, Ogg-Vorbis	$\leq$ 5dB
Spreading Sequences	Maximum, Gold, Kasami, Hadamard	$\leq$ 5dB
Dictionary Selection	DFT, DCT, MDCT	$\geq$ 10dB
Recovery Methods	ℓ_1, LASSO, OLS, CoSaMP, Combined	$\geq$ 10dB

3.5.2 Continuous Conversion of Multi-Channel

In continuous conversion, we cannot ensure the quasi-stationary property of the input signal, thus framing and windowing are essential in recovering each input signal out of the digitized mixture. Because of the block-wise processing, we may lose some signal information, thus the recovery process is performed with 50% overlap in every frames. There are many choices to make in the continuous conversion, and we summarize the expected improvements by applying different selection for reconstruction process in Table 3.2. From the table, the reconstruction is more affected by the selection of dictionary to represent the mixture signals and recovery methods.

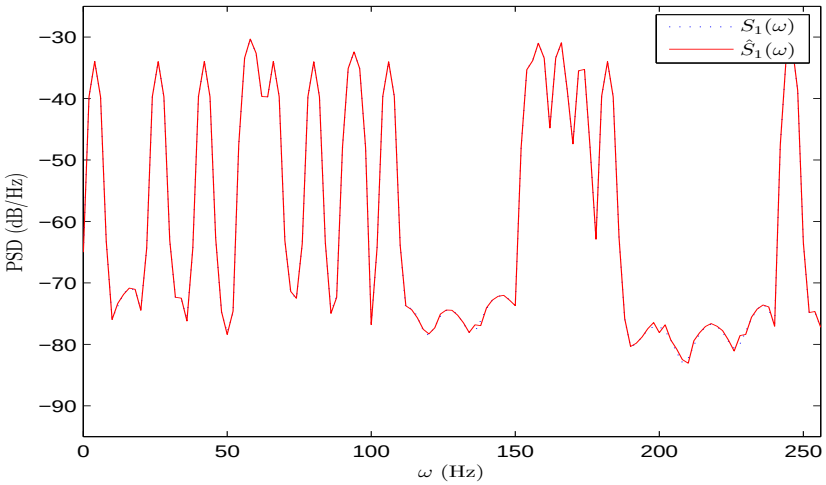


(a) Recovery error of 1st channel: SRER($\mathbf{s}_1$, $\hat{\mathbf{s}}_1$) = 46.7dB.

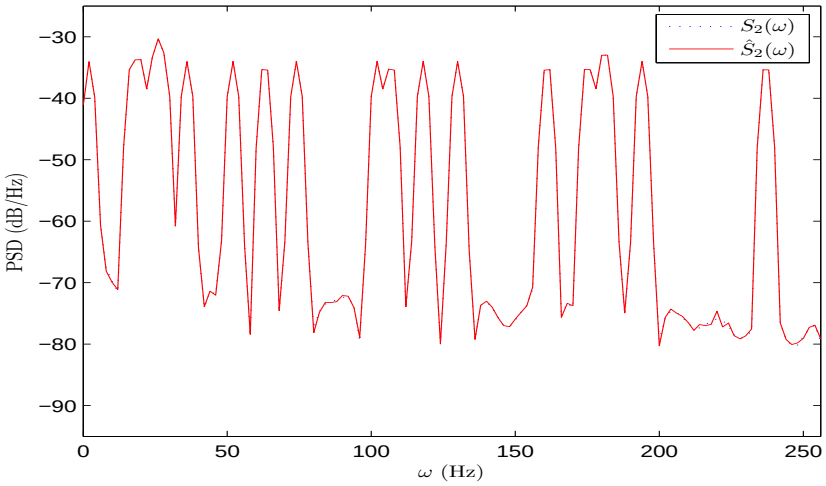


(b) Recovery error of 2nd channel: SRER($\mathbf{s}_2$, $\hat{\mathbf{s}}_2$) = 46.7dB.

Figure 3.10: Signal recovery of synthesized inputs ($s_1 \neq s_2$): (a) and (b) plot the first and second channel inputs. Input (upper), recovered (middle), and error ($\mathbf{s}$-$\hat{\mathbf{s}}$) (bottom) signals are shown respectively.



(a) Power spectrum of 1st channel: SRER($\mathbf{s}_1$, $\hat{\mathbf{s}}_1$) = 46.7dB.



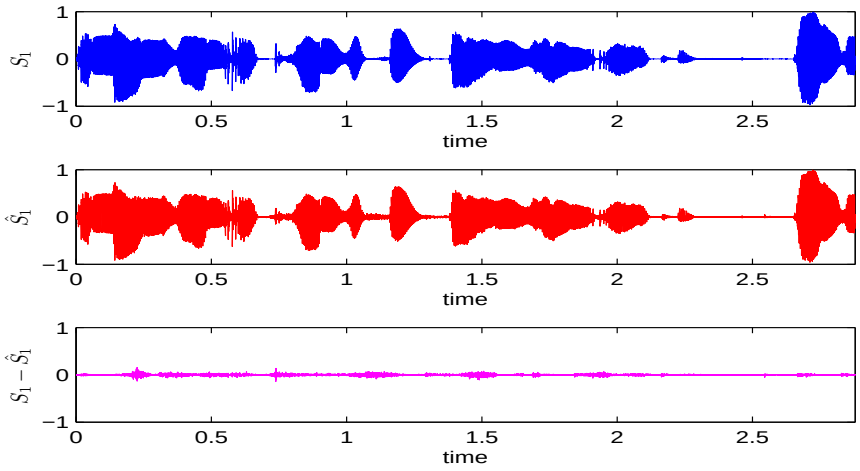
(b) Power spectrum of 2nd channel: SRER($\mathbf{s}_2$, $\hat{\mathbf{s}}_2$) = 46.7dB.

Figure 3.11: Signal recovery of synthesized inputs ($s_1 \neq s_2$): Spectral power density: (a) and (b) show the frequency power spectrum of input (dotted line) and recovered (solid line) signals.

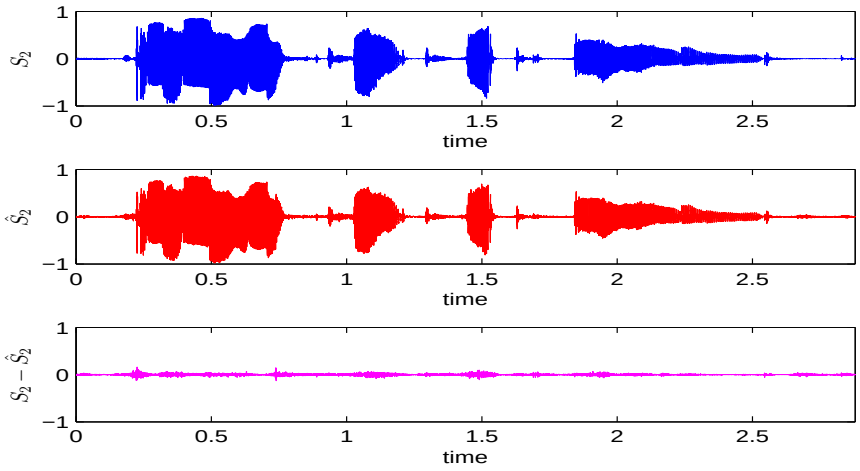
3.5.3 Simulation With Speech Signals

So far, we have shown that the proposed multi-channel scheme works well under the assumption that the inputs are sparse in certain domain. A natural question that arises is whether the proposed scheme should work for signals that are not or moderately sparse. One of such examples is speech signals. We test two sets of speech samples to see the reconstruction performance through our ADC architecture. Two three-second long speech samples are prepared for the simulations, and they are sampled at 8kHz through the proposed ADC architecture. Speech signals are known to be sparser in modified discrete cosine transform (MDCT) basis than the other basis. Thus, an MDCT dictionary is selected rather than a DFT dictionary for the sparse representation of the mixture signal. To find sparse coefficient vectors, we use SL0 solver [60, 61] as the same as the previous simulations. The simulations with speech signals show 23.3dB and 24.3dB SRERs for the first and second input channels respectively, and the results are shown in Figs. 3.12 and 3.13.

The proposed architecture works even for the scenario with an identical input on both channels, and we obtained 22.4dB SRERs on both channels when we use the same speech samples as inputs to the two channels. In the case of identical or correlated channel inputs, the total spectral occupancy of input signals is increased in every signal frames than uncorrelated cases. The increased occupancy results in slightly decreased SRERs after reconstructing each input signals as shown in Figs. 3.7 to 3.9.

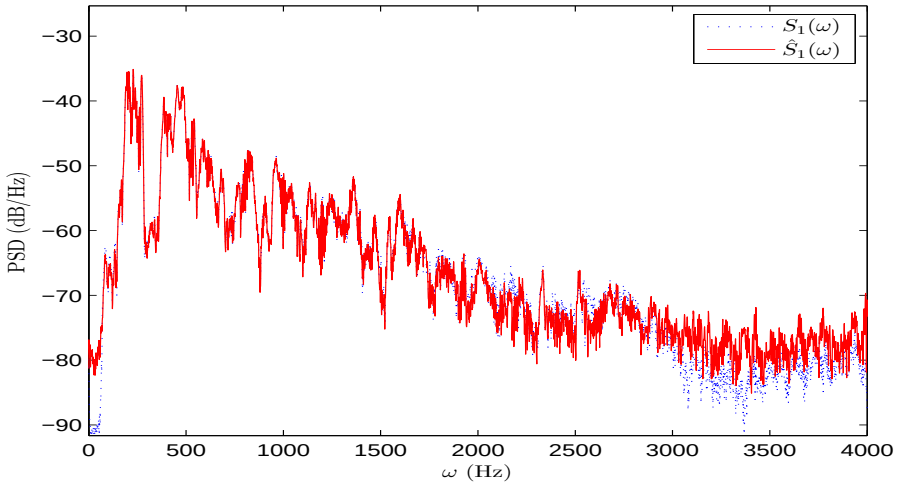


(a) (a)

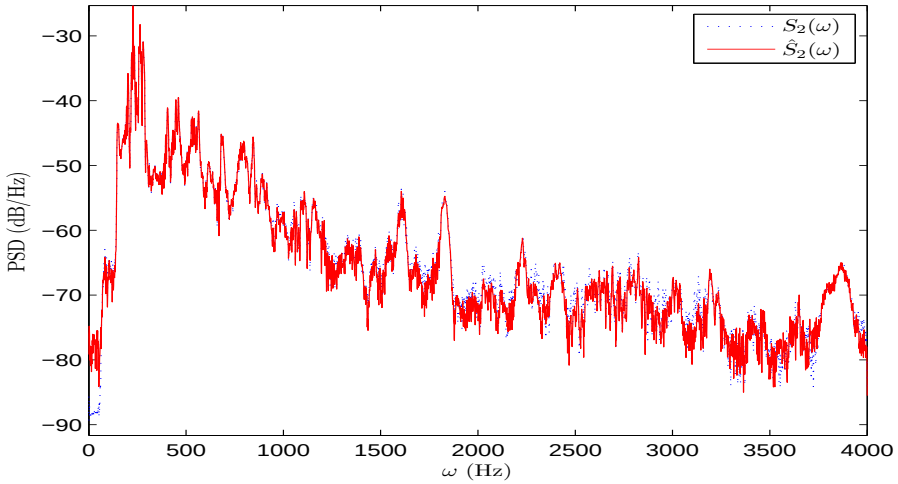


(b) (b)

Figure 3.12: Signal recovery of different speech inputs ($s_1 \neq s_2$): (a) and (b) plot the first and second channel inputs. Input (upper), recovered (middle), and error ($\mathbf{s}$-$\hat{\mathbf{s}}$) (bottom) signals are shown respectively. Recovery error of the first channel: SRER($\mathbf{s}_1$, $\hat{\mathbf{s}}_1$) = 23.3dB. Recovery error of the second channel: SRER($\mathbf{s}_2$, $\hat{\mathbf{s}}_2$) = 24.3dB.



(a)



(b)

Figure 3.13: Spectral power density: (a) and (b) show the frequency power spectrum of input (dotted line) and recovered (solid line) signals. Power spectrum of the first channel: SRER($\mathbf{s}_1$, $\hat{\mathbf{s}}_1$) = 23.3dB. Power spectrum of the second channel: SRER($\mathbf{s}_2$, $\hat{\mathbf{s}}_2$) = 24.3dB.

3.6 Circuit Implementation

The proposed multi-channel architecture is designed and fabricated in 130nm CMOS process. Similar to conventional SAR ADC, the design blocks consist of clock generator, mixer, DAC array, comparator, and asynchronous SAR logic blocks. By effectively integrating all the blocks into a single SAR ADC, we not only save power, signal bandwidth and area, but also the design tries to avoid timing skew, offset mismatch, and gain mismatch across channels. The trick to avoid timing skew is on the fact that all the channels are being sampled are controlled by one bottom-plate sampling switch. Thus, the design with one comparator is guaranteed to avoid offset mismatch. The gain mismatch comes from the capacitor mismatch, but this can be compensated with the capacitor calibration.

After prototyping the architecture, removing or calibrating offsets is a necessary to improve the ADC's accuracy as otherwise it is turned into large noise by the PRBS. It is worthwhile to note here how to calibrate the overall ADC offset. An easy calibration of the fabricated ADC is found by taking advantage of the inherit multiplication between the input $\vec{s}$ and the PRBS $\vec{p}$. To remove the offset value, the mean of the ADC result V_{os} is measured after applying a monotonous input $\vec{s}$ such as $V_{os} = mean(\vec{p} \otimes \vec{s} + v_{off})$, where v_{off} is the comparator offset voltage.

Different from the single-channel CS SAR ADC in Chapter 2 which requires non-uniform quantization cycles depending on the neighboring sampling cycles, the multi-channel CS SAR ADC requires exactly the same the

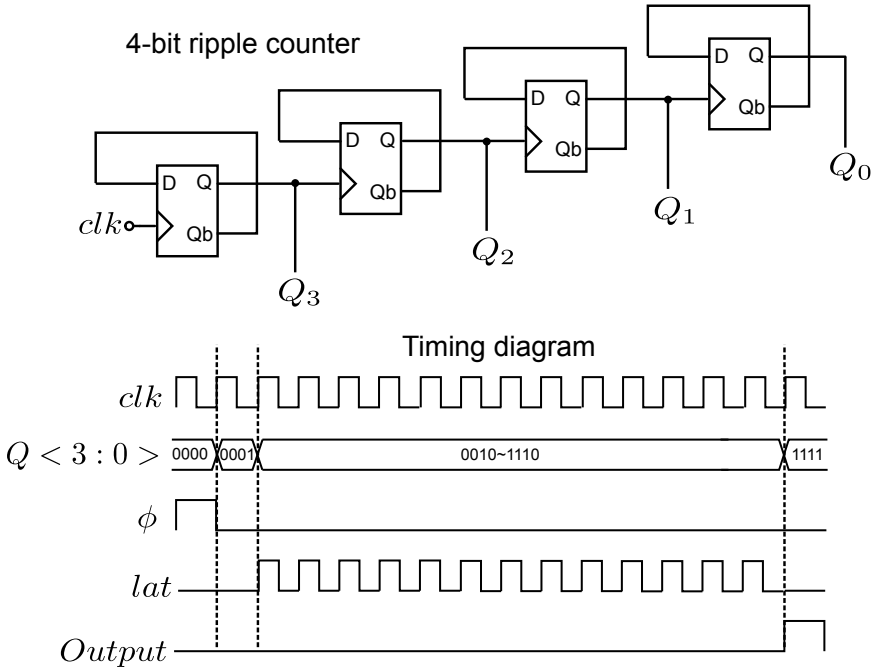


Figure 3.14: Proposed 12-bit four-channel CS SAR ADC timing diagram.

operation timing as a conventional SAR ADC. In the sampling phase, all the channels are sampled simultaneously . All the channels are averaged on-the-fly and conversion phases start after the sampling phase. Thus, the SAR logic can be easily implemented in a synchronous fashion.

Fig. 3.14 shows the timing diagram for the 12-bit four-channel CS SAR ADC operation. As can be seen, a 4-bit ripple counter is used to divide the master clock into 16 cycles. The 1^{st} cycle is used for the sampling phase ϕ_1. *lat* is a clock signal for the comparator. When it is high, the comparator starts to make a decision. When it is low, the comparator is reset. After sampling, the DAC array is redirected to an initial sequence {1,-1,-1,-1,-1,-1,-1} to be

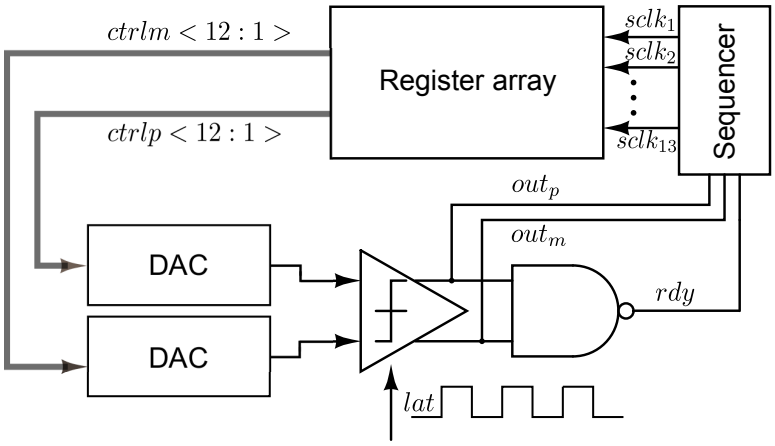


Figure 3.15: Synchronous SAR logic architecture.

ready for the first-bit comparison. The 2^{nd} cycle is used for the DAC settling to the initial sequence. The *lat* signal starts from the 3^{rd} cycle and ends at the 15^{th} cycle, producing 13 digital outputs, one of which is a redundant bit. The final cycle *Output* is used to store the digital outputs.

Fig. 3.15 shows the synchronous SAR logic architecture. Compared to the asynchronous SAR logic architecture, the major difference is that the comparator is clocked by a synchronous *lat* signal rather than self-clocked. More details about the ADC design is described in [62], which has been completed while Dr. Wenjuan Guo was a Ph.D student at The University of Texas at Austin.

3.7 Measurement Results

The proposed multi-channel ADC is designed in a 12-bit four-channel SAR architecture and the design is fabricated in a 0.13 μm CMOS process,

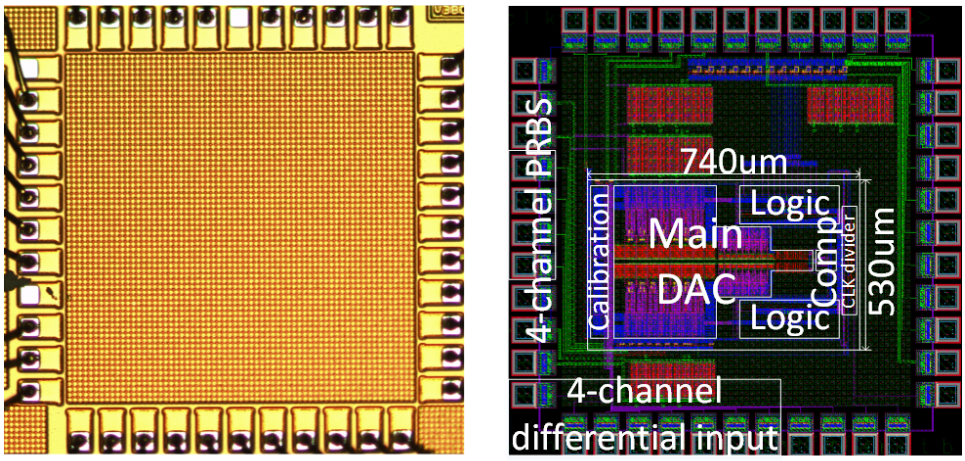


Figure 3.16: Chip die photo and layout.

occupying an area of 0.39 mm^2. The die photo and layout of final design is shown in Fig. 3.16. The chip is designed at a power supply of 0.8 V and a sampling frequency of 1 MS/s. The total DAC capacitance is 2.1 pF $\times$ 2 with a unit capacitor of 2 fF.

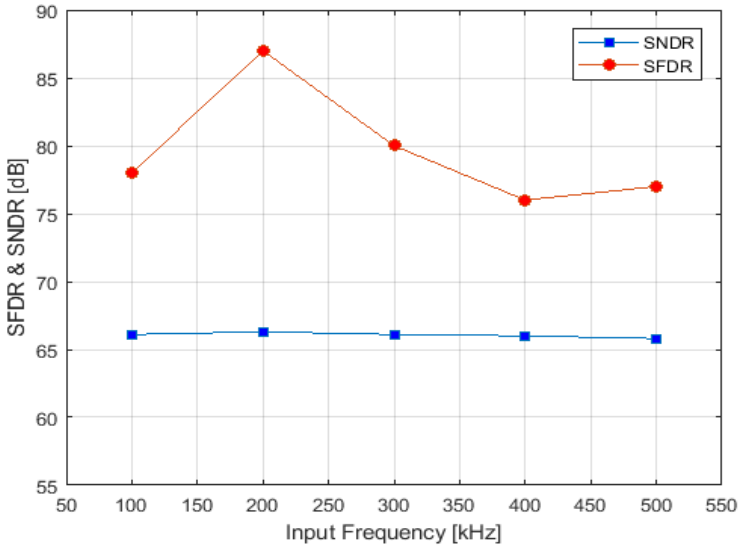
After fabrication, the prototype ADC is tested in two modes: 1) Single-Channel Model and 2) Multi-Channel Mode. In the Single-channel Mode, the PRBS is set to be always 1 and the chip performance is measured which gives a overview of the design completeness. In the Multi-Channel Mode, the PRBS is generated from an external FPGA and streamed into the chip via a four-channel level shifter. To demonstrate the four-channel sampling performance, discrete-tone signals and real-word speech signals are prepared and tested. In this section, the measured performance is presented, and the performance comparison between the four-channel prototype ADC and prior single-channel

CS works will be exhibited in the next section.

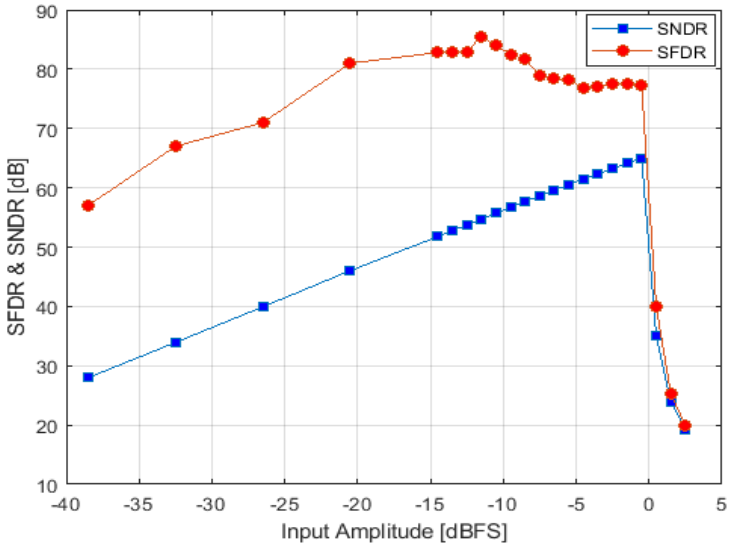
3.7.1 Single-Channel Mode Measurements

To verify the performance of the prototype SAR ADC, the chip is operating with all $\vec{p}_m$ to be 1 instead of modulating with PRBS. With this set-up, all the channels sense the same input signals, and thus the four-channel CS SAR ADC works exactly the same as a conventional SAR ADC. Fig. 3.17(a) shows that the measured spurious-free dynamic range(SFDR) and signal-to-noise-and-distortion ratio(SNDR) up to the Nyquist rate which are measured to be 76 dB and 66 dB respectively. Fig. 3.17(b) shows the SFDR and SNDR trend with various input amplitudes. To demonstrate the capability of the ADC to sample four-channel input signals simultaneously, Fig. 3.18 shows the measured output spectra when a 100.016 kHz, 200.016 kHz, 300.016 kHz, and 400.016 kHz -3 dBFS sinusoidal inputs are fed to each channel respectively. Since the ADC output is the averaged value of the four channels, the output spectra should contain four tones at these input signal frequencies, each of which is around -15 dBFS. The total power consumption is measured to be 34 μW with 0.8 V and 1 MS/s operation.

Fig. 3.19 illustrates the measured power breakdowns of the chip. It is worthwhile to note that the digital portion accounts for 74% which can be greatly reduced by process scaling. Combining all the metrics, the prototype ADC achieves a FoM of 20.4 fJ/conversion-step in the Nyquist-mode.



(a) SFDR & SNDR vs. input frequency.



(b) SFDR & SNDR vs. input amplitude.

Figure 3.17: Measured ADC performance without PRBS.

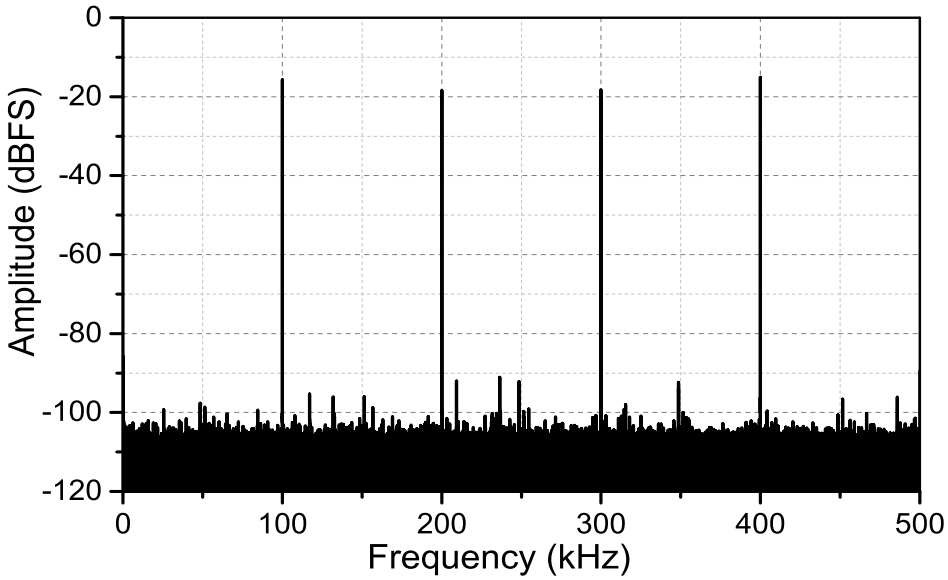


Figure 3.18: Measured output spectrum when inputting a 100.016 kHz, 200.016 kHz, 300.016 kHz, and 400.016 kHz -3 dBFS sinusoidal wave to each channel, respectively.

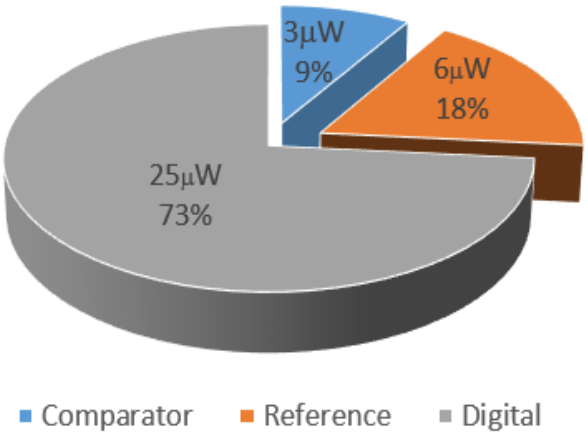


Figure 3.19: Power breakdown.

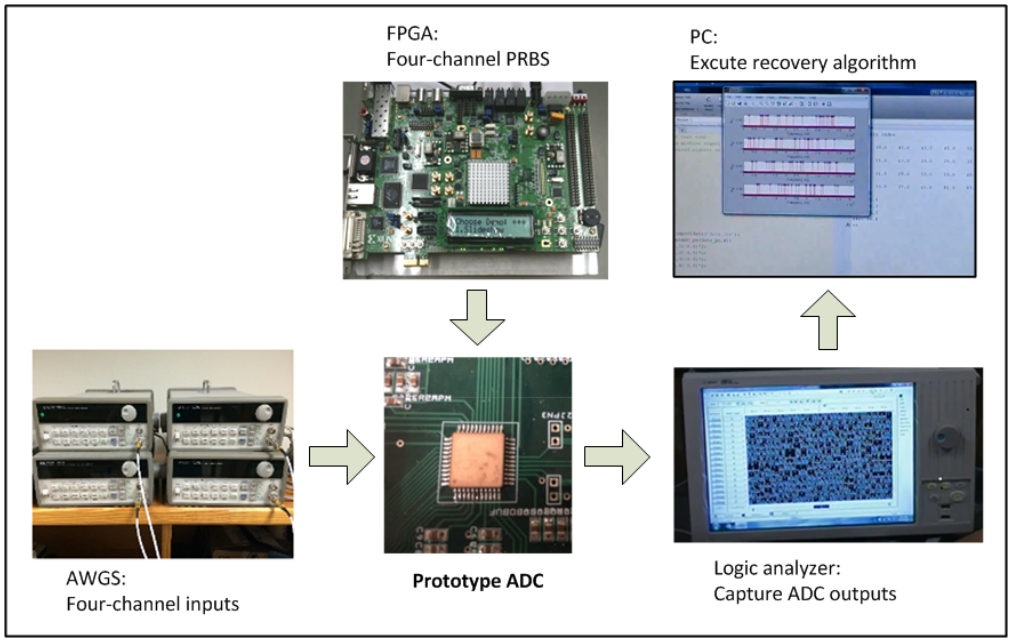


Figure 3.20: Test bench diagram.

3.7.2 Multi-Channel Mode Measurements

To verify the multi-channel sampling capability of the prototype ADC, four sets of PRBS are fed to the chip from the FPGA. Fig. 3.20 shows the block diagram of the test bench. four arbitrary waveform generators (AWG) are prepared for the four-channel inputs. The chip outputs are connected to a logic analyzer which transmits the channel outputs to a PC, and the four-channel signal recovery is performed in the PC. The all test procedures are captured in video recording which explains how experiment is performed, can be found in the Youtube link: http://youtu.be/AWraL5m-X9A.

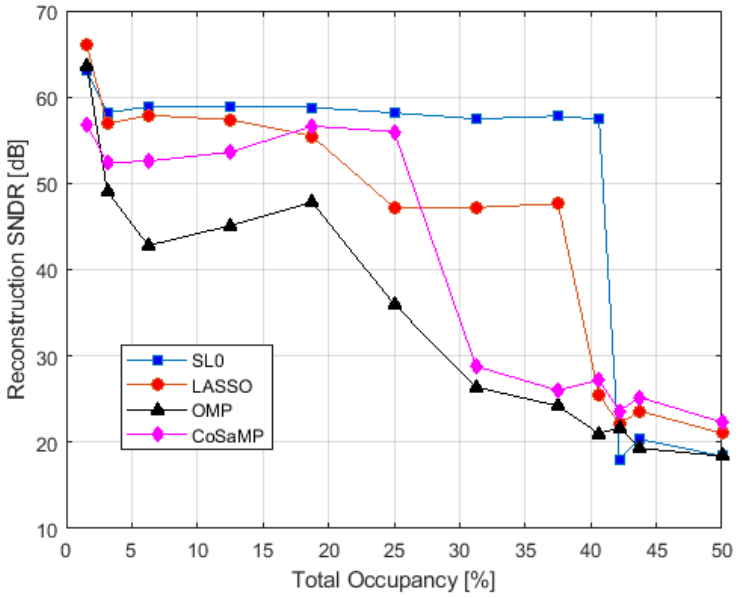
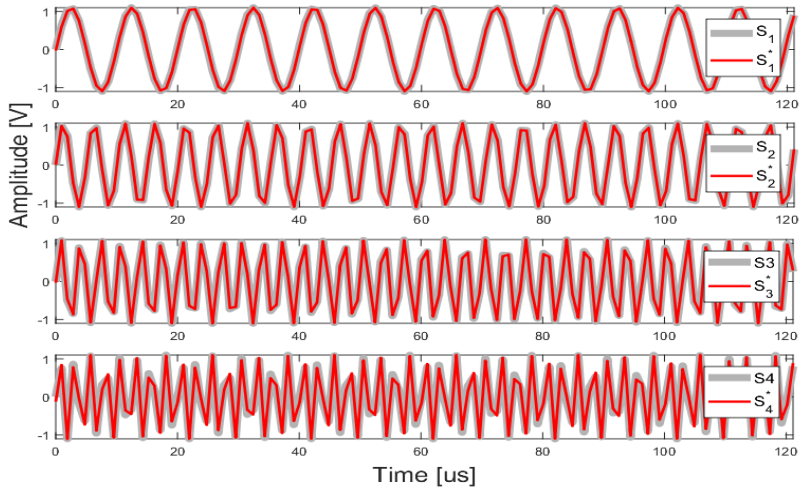


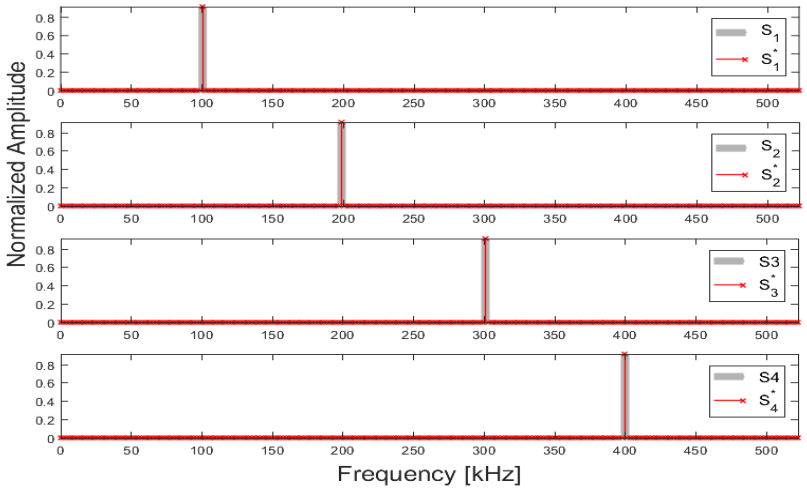
Figure 3.21: Measured post-reconstruction SNDR with different total channel occupancies and reconstruction algorithms when all channel signals are independent.

3.7.2.1 Discrete Tone Measurements

To test the maximum sparsity and occupancy of the prototype SAR ADC, multi-tone discrete signals are prepared and the discrete-tone signals consist of multiple sinusoidal waveforms at different frequencies. Since the CS SAR ADC has four channels, the total channel occupancy is defined as $\sum_{m=1}^{4} K_m/(N/2)$, where K_m indicates the number of frequencies the m^{th}-channel signal has, and N is the length of PRBS. Four sets of 512-length PRBSs are generated in the FPGA and input the mixed signal block. To simplify the testing, we let each channel possess the same number of frequencies. In scenario 1) when all-channel signals are independent, the frequency values of each channel signal are randomly generated. With different channel occupancies and reconstruction algorithms, we measure the four-channel average post-reconstruction SNDR. Two convex optimization methods (CVX and SL0) and two greedy algorithms (OMP and CoSaMP) are tested [8]. For greedy methods, K_{max} for each channel is set to be 100. As shown in Fig. 3.21, CVX and SL0 achieve the peak SNDR of 66 dB and the max occupancy of 41% (26 tones per channel), respectively. Fig. Figs. 3.22 and 3.23 shows the measured time-domain and frequency-domain results of the input signals s_m and reconstructed signals ${}^{*}s_m$ via the SL0 method in the single-tone case and 26-tone case, respectively.

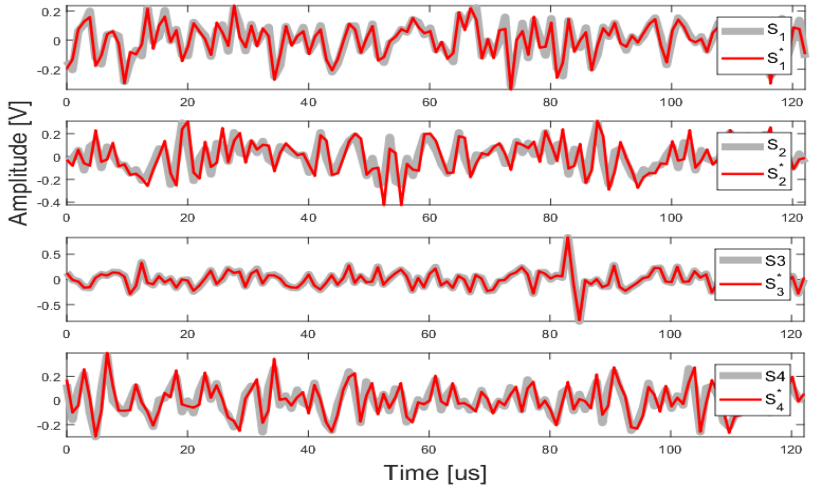


(a)

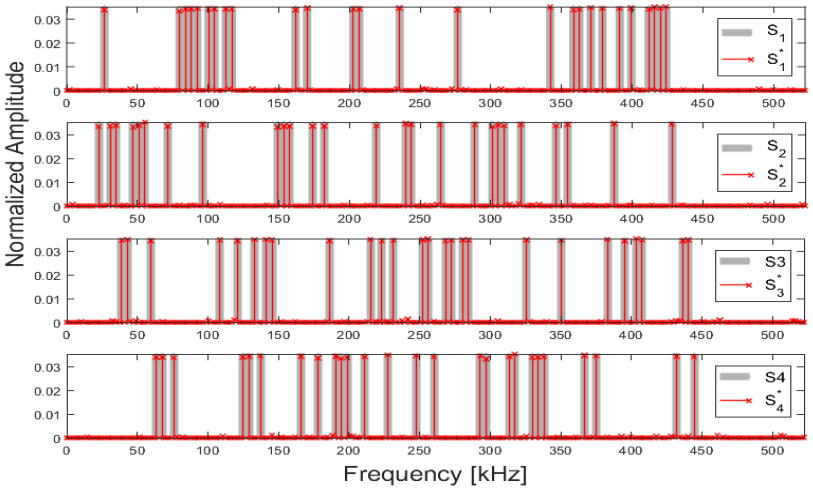


(b)

Figure 3.22: Measured time-domain (a) and frequency-domain (b) results of the input signals s_m (gray) and reconstructed signals s_m^* (red) via the SL0 method in the single-tone case.



(a)



(b)

Figure 3.23: Measured time-domain (a) and frequency-domain (b) results of the input signals s_m (gray) and reconstructed signals s_m^* (red) via the SL0 method in 26-tone case.

3.7.2.2 Measurement of Real Speech Signals

In addition to the discrete-tone tests, we also test the chip capability to convert real-world sparse signals. To investigate the scenario when all channel signals are independent, we also test four-channel 1 second-long speech signals from different sources. At a sampling rate of 16 kHz, the total length of 1-channel speech signal is 16000. To reduce the computation complexity, the ADC output is divided into multiple 512-length frames, each of which individually conducts the CS process. All the frames are 50% overlapped with each other and windowed to smooth the edges. Fig. 3.24 demonstrates their reconstruction results via the SL0 method. Except weak signals beyond 4 kHz buried in the noise floor, $\hat{s}_m$ match well with s_m. According to the equation (3.14), the SRERs for each channel are to be obtained as 14.5 dB, 12.1 dB, 14.3 dB and 14.1 dB, respectively.

3.8 Performance Comparison

There are several literatures that have reported actual measurements of their CS-based ADC designs. The comparison among works is presented in Table 3.3. Since the proposed ADC can simultaneously convert 4 channels, its power per channel is only 1/4 of the total power, leading to an effective FoM per channel of 5.1 fJ/conversion-step. This 4-time power saving is enabled by CS. Table 3.3 summarizes the chip performance. Since our work is the first to demonstrate chip measurement results for CS-based multi-channel ADCs, Table 3.3 makes a comparison with prior single-channel CS works. As can

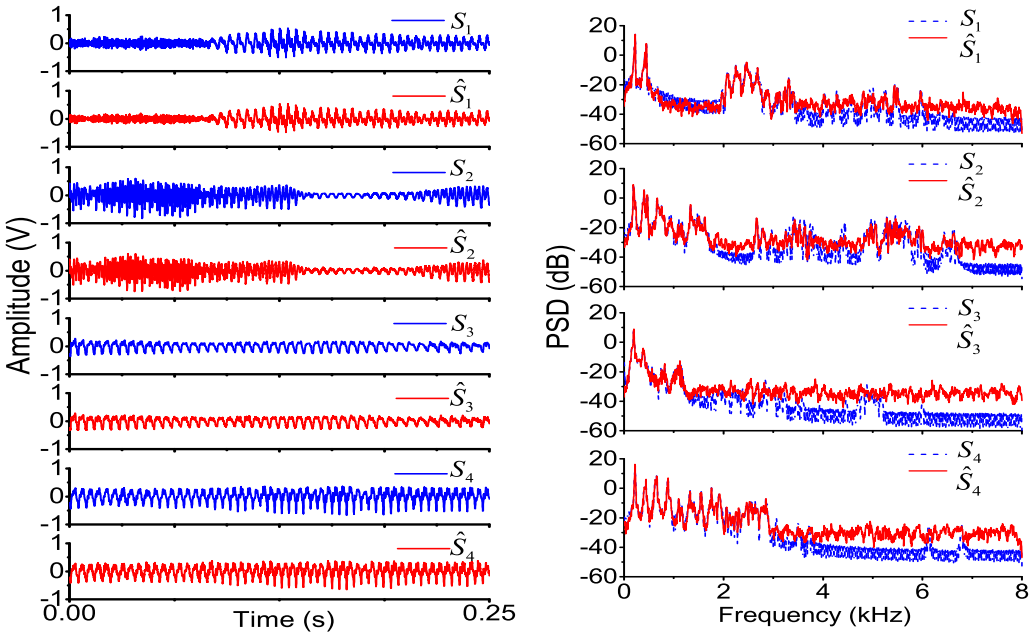


Figure 3.24: Measured time-domain (left) and frequency-domain (right) results of the four-channel 1s-long speech signals via the SL0 method. s_m (blue) are the input signals, and $\hat{s}_m$ (red) are the reconstructed signals.

Table 3.3: Comparison with state-of-the-art CS works

Design	Gangopadhyay et al. [63]	Trakimas et al. [64]	This work
CMOS technology [nm]	130	90	130
ADC performance			
Supply [V]	0.9	0.9	0.8
Sampling rate [MS/s]	0.002	5.5	1
Resolution [bit]	10	10	12
SNDR [dB]	40.6	57.6	66
ENOB [bit]	6.5	9.3	10.7
Post-reconstruction performance (Compression ratio (CR) = 4)			
Peak SNDR_{PR} [dB]	40.6	43	66
Peak ENOB_{PR} [bit]	6.5	6.9	10.7
Max occupancy	5%	4%	41%
Power [μW]	1.8	175	34
Area [mm^2]	6	0.15	0.39
FoM_{CS}[fJ/step]	9900	73.3	5.1
$FoM_{CS} = Power/2^{ENOB_{PR}}/f_s/CR$			

be seen, our work achieves at least 20 dB higher post-reconstruction SNDR ($SNDR_{PR}$) and 14-times better FoM. With the capability of converting multi-channel signals simultaneously, our work can also deal with a much higher bandwidth occupancy than other works [63] [64].

3.9 Conclusion

This chapter have presented a new form of ADC architecture to digitize multi-channel signals with a single ADC exploiting sparse-signal properties of the channel inputs. With the proposed scheme, each channel is sampled at the Nyquist rate of the ADC, and the architecture enables the recovery all channel inputs. This chapter has discussed the design of the system including the sampling rate selection, mixing sequences, and dictionary selection to recover each channel input from the mixture signal.

Future work should address several issues such as the possible maximum number of input channels, and the ratio of bandwidth expansion to enhance the sparsity of input signal mixture. Exploring an effective application is another research direction that can help make the proposed system applicable to commercial devices requiring multi-channel ADCs. Currently, we are investigating bio-signal (EEG, ECG, and EMG), and array-signal (infra red imaging, and capacitive touch screens) applications since they require multi-channel signal acquisition.

Chapter 4

Sequential Energy Detector

4.1 Introduction

In this chapter, we present a highly efficient detection scheme that can reliably detect binary events with a fraction of the energy consumption required for conventional energy detection. In detection tests, as the number of sensing points is increased, high power consumption or increased sensing latency are expected in processing. To overcome these limitations, a fast sensing and detection scheme is required. A fast sensing circuit can be designed with increased power consumption. In addition, the circuit increases hardware complexity. Thus, engineers need to consider a trade-off between sensing latency and power consumption to meet system requirements. In mobile devices such as smart phones and tablet PCs, a major portion of energy is consumed in user interfaces (LCD display and touch input processing) [65, 66]. For accurate detection and better user interface, energy-efficient sensing and detection schemes are necessary to manage multiple sensor inputs.

Compressed sensing (CS) based systems use fewer measurements than the standard sampling strategy [4, 67, 68]. However, the CS-based method requires a specially designed modulation circuit for measurement. Previous

studies show that multi-channel sparse signals can be effectively sampled by a single ADC [8, 67]. The main objectives of the studies are to recover exact signals by modulating the sparse input signals in the frequency domain using pseudo sequences. In both cases, the energy savings are achieved on the sensing side, but the savings are degraded because of the recovery methods that generally require complex or iterative computations.

Robust and reliable detection systems have been studied, focusing mostly on the probability ratio test [69]. The sequential energy detector [70] was proposed for an efficient detection of spectrum sensing in cognitive radio systems [71–74]. We consider the binary event detection problem as an extension of the work, and we derive the average sample numbers (ASNs) of the proposed sequential scheme. For comparison, the relative efficiency (RE) of the proposed method has been computed and it shows high efficiency in event detection problem under realistic signal-to-noise ratio (SNR) conditions.

4.2 Problem Formulation

For signals with low SNR, multiple measurements must be averaged for accurate detection. For example, in the case of capacitive touch screens, $20 \sim 100$ measurements are required to obtain $20 \sim 30$ dB SNRs to detect finger touches using today's analog circuit technology [75, 76]. Supposing that we monitor N measurements on each sensor nodes to decide the existence of signal of interest (binary event), the detection problem can be modeled as a binary hypothesis testing problem: Under the null hypothesis H_0, the noisy

measurement of a sensor signal without event input, and under the alternative hypothesis H_1, the noisy measurement of a sensor signal with event input. This hypothesis problem can be written as

$$\begin{aligned} H_0 :&\ x(t) = v(t), \\ H_1 :&\ x(t) = s(t) + v(t), \end{aligned} \tag{4.1}$$

where $s(t)$ denotes a unknown event signal, $v(t)$ is a noise process that is modeled as a discrete time zero-mean white Gaussian noise with covariance $E[v(t)v(s)] = E_v\delta_{k,l}$ with noise power density E_v and Kronecker delta function $\delta_{k,l}$. The event signal $s(t)$ could be either a deterministic or a random variable. For generalization, we assume that the event signal is a real random variable, and the sign of the signal is unknown. Under this formulation, it is well known that the energy detector is the optimal detection method [77–79]. The energy of $s(t)$ can be computed by $E_s = \frac{1}{T}\int_{t=0}^{T} s^2(t)dt$ [3]. During a sampling interval (0,T), the energy is approximated by

$$\int_{t=0}^{T} x^2(t)dt = \frac{1}{2B}\sum_{i=1}^{2TB} x_i, \tag{4.2}$$

where $x_i = x(i/2B)$. Over sampling time $(0, T)$, we obtain a measurement vector $\vec{x} = [x[1], x[2], \cdots, x[N]]$, $\vec{v} = [v[1], v[2], \cdots, v[N]]$, and $\vec{s} = [s[1], s[2], \cdots, s[N]]$. Thus, measurement interval T and bandwidth B have to be suitably chosen to produce an integer u. The energy of each signal can be detected both in time- or frequency-domain, and the choice depends on detection resources available. The test statistic can rewritten using the N sampled signal vector $\vec{x}$ as

$$T(\vec{x}; N) = \sum_{n=1}^{N} x^2[n]. \tag{4.3}$$

4.3 Proposed Sequential Event Detection

In this section, we introduce a sequential energy detector (SED) which is based on sequential probability of ratio test (SPRT) [70]. We extend the SED to find optimal number of samples to make SED more efficient for the detection problem. Assuming that the event signal can be modeled as a Gaussian process, impressive energy savings are possible using the concept of SED. We considered the case when sensor signal is unbiased or has to be unbiased after sampling to remove the bias wander which is troublesome in most detection problem. The unbiased sensor measurement can be modeled as

$$\begin{aligned} H_0 :\ & \underline{x}[n] \sim (0, E_v), \\ H_1 :\ & \underline{x}[n] \sim (0, E_s + E_v), \end{aligned} \tag{4.4}$$

and thus, the likelihood test $L(\vec{\underline{x}}; N)$ becomes

$$\frac{\frac{1}{(2\pi(E_s+E_v))^{N/2}} \exp\left(-\frac{1}{2(E_s+E_v)} \sum_{n=1}^{N} \underline{x}^2[n]\right)}{\frac{1}{(2\pi E_s)^{N/2}} \exp\left(-\frac{1}{2E_v} \sum_{n=1}^{N} \underline{x}^2[n]\right)}. \tag{4.5}$$

Since the test statistic $L(\vec{\underline{x}}; N)$ is continuous and monotonic, the log-likelihood ratio test can be defined $\ln\left(L(\vec{\underline{x}}; N)\right) \equiv \Lambda_N$:

$$\Lambda_N = \frac{N}{2} \ln\left(\frac{E_v}{E_s + E_v}\right) + \frac{E_s}{2E_v(E_s + E_v)} \sum_{n=1}^{N} \underline{x}^2[n]. \tag{4.6}$$

Thus, we decide H_1 if

$$T(\vec{\underline{x}}; N) = \sum_{n=1}^{N} \underline{x}^2[n] > \eta, \tag{4.7}$$

where η is the threshold for a fixed probability of false alarm. The sufficient statistic of likelihood ratio test is $T(\vec{\underline{x}}; N) = \sum_{n=1}^{N} \underline{x}[n]^2$, which is the sum

of squares of a Gaussian distributed random variable and called fixed sample size (FSS) energy detector. The sum of squared random variables can be approximated as a normal distribution if the number of samples is $N > 20$ in general. By the law of large number, the test statistic becomes

$$\begin{aligned} H_0 :\ & T(\underline{\vec{x}}; N) \sim \mathcal{N}(NE_v, 2NE_v^2), \\ H_1 :\ & T(\underline{\vec{x}}; N) \sim \mathcal{N}(N(E_v + E_v), 2N(E_s + E_v)^2). \end{aligned} \tag{4.8}$$

If $N < 20$, when the test can be terminated with a few samples, the test $T(\underline{\vec{x}}; N)$ obeys the chi-square distribution. Thus, the test obeys a chi-square distribution as follows:

$$\begin{aligned} H_0 :\ & \frac{T(\underline{\vec{x}}; N)}{E_v} \sim \chi^2_N, \text{ and} \\ H_1 :\ & \frac{T(\underline{\vec{x}}; N)}{E_v + E_s} \sim \chi^2_N. \end{aligned} \tag{4.9}$$

The false alarm and detection rates of chi-square random variables are defined as

$$\begin{aligned} P_F &= Q_{\chi^2_N}\left(\frac{\eta}{E_v}\right), \text{ and} \\ P_D &= Q_{\chi^2_N}\left(\frac{\eta}{E_v + E_s}\right). \end{aligned} \tag{4.10}$$

The probability distribution of $T(\underline{\vec{x}}; i) = \sum_{n=1}^{i} \underline{x}[n]^2 = y$ has chi-squared distribution with $y \sim \mathcal{N}(0, E_v)$. For i samples of $y[n]$, the log-likelihood ratio test Λ_i is

$$p_Y(\vec{y}; i) = \frac{1}{2E_v\Gamma(i/2)}\left(\frac{y}{2E_v}\right)^{i/2-1} \exp\left(-\frac{y}{2E_v}\right), \tag{4.11}$$

where $\Gamma(i)$ is the gamma function defined as $\Gamma(i) = \int_0^\infty x^{i-1}\exp(-x)dx$. The SPRT is performed as following. In sequential detection, instead of comparing

the test statistic to a single threshold, there are 3 regions defined via 2 thresholds (A and B). If the statistic is above the higher threshold (B) or below the lower threshold (A), we have sufficient confidence to decide the hypothesis, and if it is between the two thresholds, we need to collect more samples in a sequential manner:

$$\begin{aligned} &\text{- Decide } H_0 \text{ if } L(\vec{y}; i) \leq A \\ &\text{- Decide } H_1 \text{ if } L(\vec{y}; i) \geq B \\ &\text{- Else take next sample.} \end{aligned} \tag{4.12}$$

The thresholds are from the Wald approximations which are based on the Wald-Wolfowitz theorem [80]. The theorem forms the fundamental foundation of sequential detection which has the minimum expected sample size amongst all other likelihood-ratio-based tests for given P_D and P_F

$$\begin{aligned} A &= \frac{1 - P_D}{1 - P_F}, \text{ and} \\ B &= \frac{P_D}{P_F}. \end{aligned} \tag{4.13}$$

The test terminates if the test statistic reaches either the lower or upper threshold values which are defined in (4.13). Fig. 4.1 illustrates an example of the sequential detection, and the test is terminated after processing 19 samples.

In chi-square distribution, the likelihood ratio test $L(\vec{y}; i)$ is expressed as

$$\begin{aligned} &\frac{\frac{1}{2(E_s+E_v)\Gamma(i/2)} \left(\frac{y}{2(E_s+E_v)}\right)^{i/2-1} \exp\left(-\frac{y}{2(E_s+E_v)}\right)}{\frac{1}{2E_v\Gamma(i/2)} \left(\frac{y}{2E_v}\right)^{i/2-1} \exp\left(-\frac{y}{2E_v}\right)} \\ &= \left(\frac{1}{\lambda+1}\right)^{i/2} \exp\left(\frac{\lambda}{2E_v(\lambda+1)} \sum_{n=1}^{i} y[n]^2\right), \end{aligned} \tag{4.14}$$

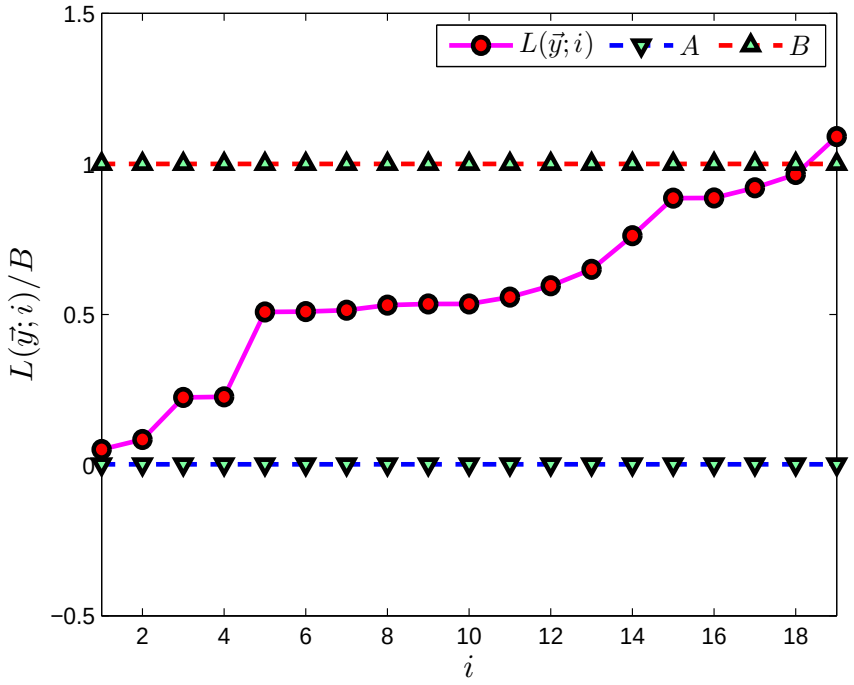


Figure 4.1: Sequential detection strategy. The test is terminated by sequential energy detection with 19 samples under the conditions of -5 dB SNR, $P_D = 0.95$, and $P_F = 0.05$.

where $\lambda = E_s/E_v$. The log-likelihood test $\Lambda_i = \ln\left(L(\vec{y};i)\right)$ can be shown as

$$\begin{aligned}\Lambda_i &= \frac{i}{2}\ln\left(\frac{1}{\lambda+1}\right) + \frac{\lambda}{2E_v(\lambda+1)}\sum_{n=1}^{i} y[n]^2 \\ &= \Lambda_{i-1} + \alpha + \beta y[i]^2,\end{aligned} \tag{4.15}$$

where $\alpha = \frac{1}{2}\ln\left(\frac{1}{\lambda+1}\right)$, and $\beta = \frac{\lambda}{2E_v(\lambda+1)}$. We normalize the expression by dividing both sides with β, then

$$\Lambda_i^{'} = \Lambda_{i-1}^{'} + \alpha^{'} + y[i]^2, \tag{4.16}$$

where $\Lambda_i^{'} = \Lambda_i/\beta$, $\alpha^{'} = \alpha/\beta$. The constant $\alpha^{'}$ can be pre-computed using prior

information. (4.16) shows the iterative relation as the number of samples i is increased. The main advantage of the iterative form is that the computation requires the same number of multiplications as that of the FSS-based detection. As the number of test samples i is increased, the iterative operation is performed by squaring a new sample followed by summing with a constant and the previous test. Thus, the operation requires slightly increased number of additions which are much cheaper than squaring a floating point value. Compare operations in each iteration are the main cost using the iterative operation. Whenever updating the test statistic based on the iterative form, the statistic is compared with the upper and lower threshold as following

$$\begin{aligned} &\text{- Decide } H_0 \text{ if } \Lambda_i^{'}(\vec{y}; i) \leq A^{'} \\ &\text{- Decide } H_1 \text{ if } \Lambda_i^{'}(\vec{y}; i) \geq B^{'} \\ &\text{- Else take next sample.} \end{aligned} \tag{4.17}$$

where $A^{'} = \ln A/\beta$, and $B^{'} = \ln B/\beta$. However, the cost is negligible if we can start comparing a test statistic which is computed with the ASNs, average number of samples to reach at a target detection accuracy, to terminate the iterative operation. Also, the efficiency of the SED-based method can be estimated from ASNs. To investigate the efficiency of the sequential energy detector, we derive the average sample number N_{SED} of the SED. The stopping time of sequential test is a random variable, thus the average number of tests which guarantees the target P_D and P_F is also random. Using Wald's equation

[80], the ASN is approximated as

$$\begin{aligned}\mathbb{E}[N_{SED}|H_0] &\approx \frac{P_F \ln A + (1-P_F)\ln B}{\mathbb{E}[\Lambda_{N_{SED}}|H_0]},\\ \mathbb{E}[N_{SED}|H_1] &\approx \frac{P_D \ln A + (1-P_D)\ln B}{\mathbb{E}[\Lambda_{N_{SED}}|H_1]}.\end{aligned} \tag{4.18}$$

The denominators of the right sides of (4.18) are computed by taking expectation of (4.14):

$$\mathbb{E}[\Lambda_{N_{SED}}|H_\theta] = N_{SED}\cdot\alpha + \beta\cdot\mathbb{E}\left[\sum_{n=1}^{N_{SED}} y[n]^2|H_\theta\right], \tag{4.19}$$

where hypothesis index $\theta = 0, 1$. Since $\mathbb{E}\left[\sum_{n=1}^{N_{SED}} y[n]^2|H_\theta\right]$ can be computed as

$$\begin{aligned}\mathbb{E}\left[\sum_{n=1}^{N_{SED}} y[n]^2|H_0\right] &= E_v\cdot\mathbb{E}\left[\chi^2_{N_{SED}}\right]\\ &= E_v\cdot N_{SED}\\ \mathbb{E}\left[\sum_{n=1}^{N_{SED}} y[n]^2|H_1\right] &= (E_s+E_v)\cdot\mathbb{E}\left[\chi^2_{N_{SED}}\right]\\ &= (E_s+E_v)\cdot N_{SED},\end{aligned} \tag{4.20}$$

the equation (4.18) can be written:

$$\begin{aligned}\mathbb{E}[\Lambda_{N_{SED}}|H_0] &= \frac{N_{SED}}{2}\left[\frac{\lambda}{E_v(\lambda+1)} - \ln(\lambda+1)\right],\\ \mathbb{E}[\Lambda_{N_{SED}}|H_1] &= \frac{N_{SED}}{2}\left[\lambda - \ln(\lambda+1)\right].\end{aligned} \tag{4.21}$$

With this result, the ASN is approximated as, The ASN is approximated as,

$$\begin{aligned}\mathbb{E}[N_{SED}|H_0] &\approx \left(\frac{2(P_F\ln A + (1-P_F)\ln B)}{\frac{\lambda}{E_v(\lambda+1)} - \ln(\lambda+1)}\right)^{1/2},\\ \mathbb{E}[N_{SED}|H_1] &\approx \left(\frac{2(P_D\ln A + (1-P_D)\ln B)}{\lambda - \ln(\lambda+1)}\right)^{1/2}.\end{aligned} \tag{4.22}$$

Thus, the N_{SED} is selected from two hypotheses:

$$N_{SED} = \max\{\mathbb{E}[N_{SED}|H_0],\ \mathbb{E}[N_{SED}|H_1])\}. \tag{4.23}$$

On the other hand, the number of samples of FSS which ensures to obtain target P_D and P_F is derived from (4.24) From the equations, the expected number of samples which is required to obtain the target detection accuracy is computed as

$$\begin{aligned} N_{FSS}^{'} &= 2\left[\frac{Q^{-1}(P_F)}{\lambda} - \left(1+\frac{1}{\lambda}\right)Q^{-1}(P_D)\right]^2, \text{ and} \\ N_{FSS} &= \lceil N_{FSS}^{'} \rceil. \end{aligned} \tag{4.24}$$

We compare N_{FSS} and N_{SED} in Fig. 4.2 (a), and they are function of SNR, P_D, P_F. Clearly, the SED requires much fewer samples to terminate a test. The efficiency of the SED is computed by comparing the expected numbers of N_{FSS} and N_{SE}. The relative efficiency (RE) of test is defined as

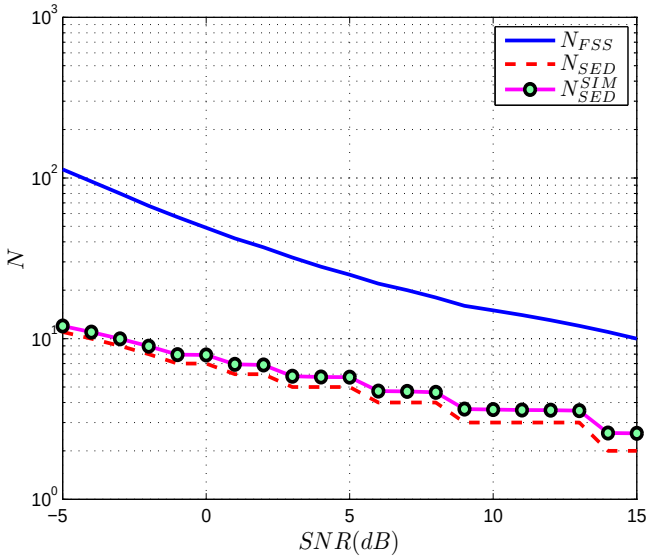
$$RE = \frac{N_{FSS}}{N_{SED}}. \tag{4.25}$$

Computing (4.25) in a closed form analytically is not trivial. Thus, we investigate the relative efficiencies through simulation in the following section.

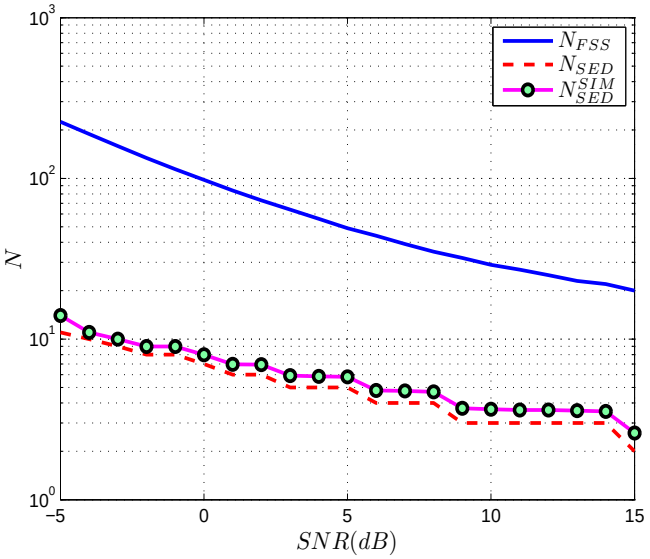
4.4 Sequential Test with ASN

We perform MATLAB simulation of the SED with pre-computed ASNs. In the simulation, two cases with different conditions are investigated; The target probabilities of detection and false alarm are set to $\{P_D = 0.95, P_F = 0.05\}$ and $\{P_D = 0.99, P_F = 0.01\}$ varying SNRs from -5dB to 15dB. The number

of samples to terminate each test is measured, and the results show that the proposed method require much fewer samples (N_{SED}) than those of the conventional fixed sample size test (N_{FSS}). In Fig. 4.2, we demonstrate the simulation results, and the FSS requires more samples to meet the stricter condition (a) than the relaxed condition (b). The simulation results show very small gaps between the measured N_{SED} and the computation by (4.23).



(a)



(b)

Figure 4.2: Comparison of the number of multiplications between FSS and SED. (a) $P_D = 0.95$, $P_F = 0.05$, (b) $P_D = 0.99$, $P_F = 0.01$.

As stated in the previous section, the relative efficiency defined in (4.25), cannot be computed in a straightforward way. Instead, the empirical RE is demonstrated in Fig. 4.3 based on the simulation results. The proposed detection scheme shows better performance under low SNR conditions than samples with high SNRS. Still, fewer samples are required to make a binary decision than the case using conventional energy detection approach.

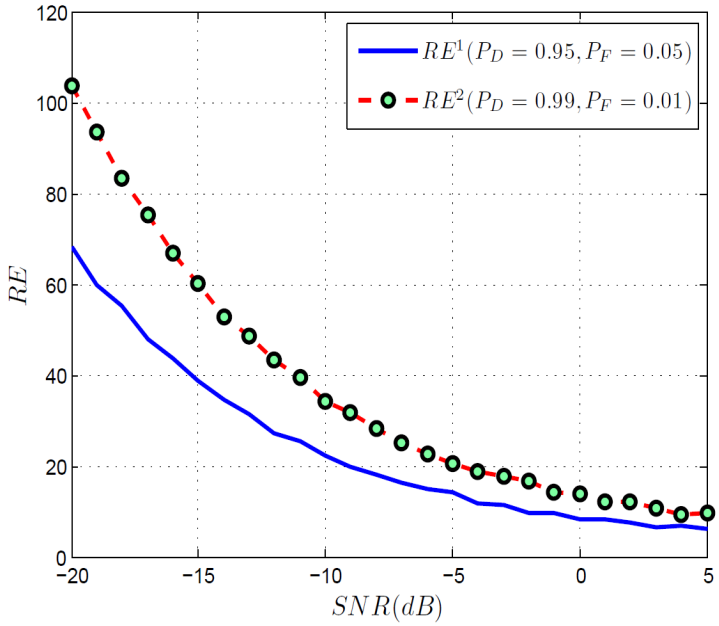


Figure 4.3: Relative efficiencies of $P_D = 0.95$ with $P_F = 0.05$ (RE^1: blue-solid line) and $P_D = 0.99$ with $P_F = 0.01$ (RE^2: circle-dotted line).

4.5 Conclusion

In this chapter, we have proposed a novel detection scheme that delivers impressive savings in the sensing time of binary event detection using

SED. These savings can translate into a significant boost to the operational battery life of today's mobile devices. The savings comes from the elaborated sequential-detection scheme and the expense of slightly decreased detection performance. As an application, this thesis has considered capacitive touch-screen displays [75], which is one of the biggest drains on the battery in mobile devices. The touch detection system of a capacitive touch-screen consumes 2.1mW at 120Hz sampling in normal operation [81] and iPhone 5 has a 5.4Wh battery [82]. Touch screens account for more than 10% of total power consumption excluding backlight in operation[66]. Considering weak SNR conditions, roughly 70% savings in touch detection will increase the operation time of mobile devices. The proposed method is relatively versatile for applications that require binary decision from multiple measurements other than touch input detection. In addition, the proposed scheme can be combined with the CS and sparse-signal sampling methods as a form of post-processing to detect binary events; it can also independently with general detector systems. In Fig. 4.4 the example is demonstrated. The proposed detection scheme is applied to voice activity detection after signal recovery, which is discussed in Chapter 3.

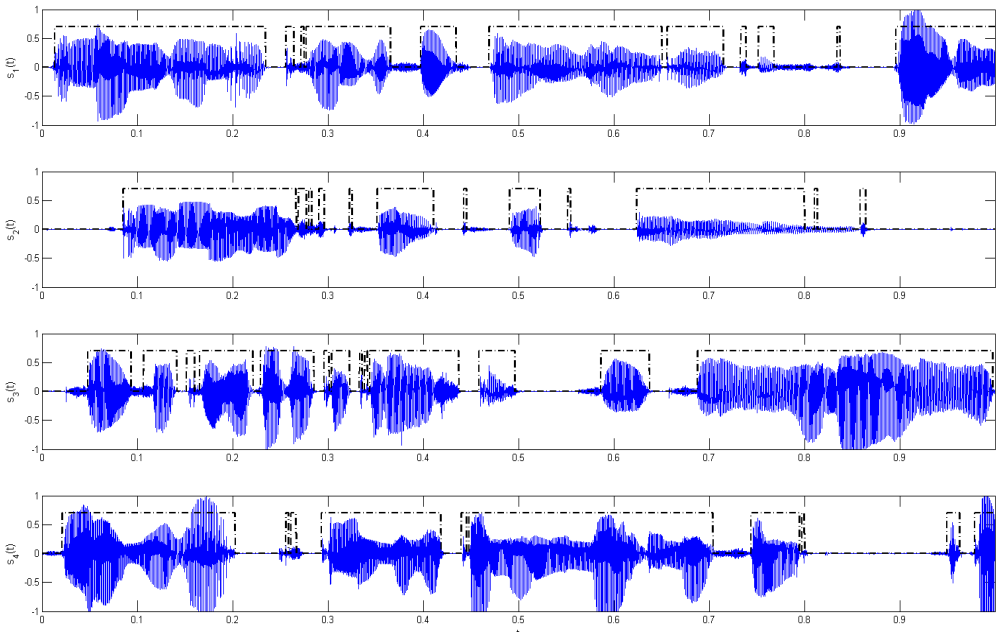


Figure 4.4: Voice activity detection of four-channel signal after recovery using the the proposed scheme ($P_D = 0.99$, $P_F = 0.01$). The blue plots show speech signal in each four channels and the black dotted-line indicate the regions where speech signal is detected.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

Through this dissertation, novel sampling and detection methods have been explored in an effort to overcome current system limitations defined by the Shannon-Nyquist sampling theorem and the binary hypothesis testing procedure. Although much progress has been made in scaling transistors for digital circuits, sampling high-bandwidth and multiple-channel signals is challenging problems in terms of energy consumption, bandwidth requirement, and design area in mobile systems. This thesis could be a pathway to overcome the limitations from the conventional approaches.

The first contribution of this dissertation is in the area of non-uniform quantization analog-to-digital converter (ADC) architecture which improves the resolution of the sampled data in medium- or high-bandwidth signal sampling. The non-uniform quantization random sampler makes use of the signal acquisition process in successive-approximation-register (SAR) ADC architecture. A modified random sampling procedure and signal recovery model have been presented in which better signal precision is achieved in comparison with the conventional compressive sensing approach. Circuit level realization is dis-

cussed to realize the new scheme incorporated with SAR ADC architecture.

The feasibility of using a single ADC system to digitize multi-channel inputs has been studied and the prototype ADC has been designed and fabricated. The analog front-end of the multi-channel ADC has been proposed; it effectively combines multiple channels using pseudo-random sequences and the successful channel recovery is performed in the back-end signal processing using the proposed recovery algorithms. For both mixing and recovery, various pseudo-random sequences have been compared. Ultimately, the maximum-length or Gold sequences have been shown to be the most suitable for the purpose due to their cross-correlation properties. In the proposed framework, the multi-channel sparse signals are sampled at the Nyquist rate, which is the same as a single channel. However, the recovered channels do not suffer bandwidth reduction in the input signals and this is the major advantage of the ADC architecture. The prototype implementation of the proposed architecture is realized in a 130nm CMOS process. The prototype ADC successfully demonstrates sampling up to four channels with high signal-to-reconstruction-error rates. To the best of our knowledge, this is the first work presenting a multi-channel data conversion using switch capacitor circuits to mix the input channels in the analog front-end; and in which the framework is implemented in real silicon for lab measurements. Since the proposed ADC can simultaneously convert four channels, its power per channel is only 1/4 of the total power, leading to an effective figure-of-merit (FoM) per channel of 5.1 fJ/conversion-step. Since our work is the first to demonstrate chip measure-

ment results for compressed sensing (CS)-based multi-channel ADCs, Table 3.3 makes a comparison with prior single-channel CS works. As can be seen, this work achieves at least 20 dB higher post-reconstruction SNDR ($SNDR_{PR}$) and 14-times better FoM. With the capability of converting multi-channel signals simultaneously, our work can also deal with a much higher bandwidth occupancy than other works [63] [64].

A highly efficient detection scheme has been derived that improves the current binary hypothesis testing scheme with reduced processing complexity. The proposed procedure requires fewer measurements to determine the existence of a signal of interest over the noise measurements. The proposed detection strategy consists of two steps; summing and sequential detection phases. By separating the detection steps, total sample numbers and in turn computations are highly reduced. The reduction can be translated into energy savings. The savings can help with extending operating time in energy-limited mobile systems. The proposed detection scheme also shows robust detection performance under low signal-to-noise conditions compared to the conventional detection scheme, which is based on fixed sample size.

The contributions mentioned above can shape future mobile and wearable systems to be more efficient by reducing power requirement, storage space, and data transmission during operation.

5.2 Future Work

1. **Non-uniform quantization random sampler:** The proposed scheme reduces the total quantization noise compared to the conventional CS sample strategy. The estimation of power consumption of the proposed architecture is not trivial and it is not covered in this thesis. The estimation will be subject to the design factors such as the number of quantizer and CMOS processes. Thus, the proposed work is focused on analog front-end architecture in the mixed-signal block which leads to high precision signal acquisition after signal recovery. The post-processing holds the key operating the non-uniform quantization scheme, which depends on the complexity of the recovery algorithm. A fast algorithm will enable the converter to produce real-time or high throughput signal acquisitions. Yet, the proposed reconstruction method is not cheap and is a little more complex compared to the conventional recovery algorithms in compressed sensing. Recovery complexity is a common issue in CS-based systems so could be a worthwhile topic to advance our research agenda.

2. **Multi-channel sparse-signal conversion:** Exploring an effective application is another area of research necessary for making the proposed system applicable to commercial devices that require multi-channel ADCs. Possible applications have been actively investigated; by far, bio-signal (EEG, ECG, and EMG) and array signal (infra-red imaging, and capacitive touch screens) applications have been promising candidates since they require multi-channel signal acquisition and show good sparseness

in a certain domain. The reconstruction algorithms proposed in this thesis can be improved by using the block sparseness property between the input and mixture signals which is not investigated in this thesis.

3. **Sequential energy detection:** The proposed detection procedure has been shown that substantial savings on test samples are achievable. Further savings can be expected if the proposed detection procedure could be combined with the proposed multi-channel sparse data converter detecting binary event occurrence. In this scenario, signals from other channels contribute as interference and are regarded as noise. These extra inter-channel noise contributions will be hostile to making a correct decision. However, the proposed scheme shows effective robustness against noisy measurements so as to compensate for the effects of unwanted signal interferences.

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Vita

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