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Heterogeneous Integration of Graphene and Si CMOS for Gas Sensing Applications

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Heterogeneous Integration of Graphene and Si CMOS for Gas Sensing Applications

by

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Dedicated to

My Parents, Zahra and Seyed Mohammad Ali

And

My Love, Mir Mohammad

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When my Ph.D. journey began, I never imagined that I would love the University of Texas at Austin (UT) and the city of Austin this much. Now that this journey is drawing to an end, it will be difficult to leave UT. I will miss the friendly atmosphere, never-ending conversations with friends laughing and complaining about our common problems, my endless efforts to learn more, moments of achievement and frustration, and even my sleepless nights doing research. Above all, it was this city where I started a wonderful life with the love of my life, Mir Mohammad, had lots of great moments, and enjoyed every second of our life together.

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Heterogeneous Integration of Graphene and Si CMOS for Gas Sensing Applications

Seyedeh Maryam Mortazavi Zanjani, Ph.D.

The University of Texas at Austin, 2014

Supervisor: Deji Akinwande

Detecting presence of gas molecules is of prominent importance for controlling chemical processes, safety systems, and industrial and medical applications. Despite enormous progress in this field over past few decades on developing and improving various types of gas sensors, sensors with higher sensitivity, selectivity, lower sensing limit, and lower cost that can perform at room temperature are highly sought-after. Discovery of graphene and its succeeding progress in nanotechnology has paved the way to design ultra-sensitive gas sensors that can detect individual gas molecules while operating at room temperature. Graphene is a promising candidate for gas sensing applications due to its unique transport properties, exceptionally high surface-to-volume ratio, and low electrical noise.

In this dissertation, a graphene gas sensor fully integrated with silicon CMOS platform is presented, and its performance for detecting NO_2 and NH_3 gas molecules is investigated. This integration helps benefit the high gas sensitivity of graphene at room temperature as well as the compact size, robustness, low cost, and advantages of standard industrial scale production of CMOS technology. Recent progress in large scale growth of CVD graphene paves the path toward commercialization of graphene-based CMOS sensors to provide highly sensitive low-cost sensors for industrial applications. To best of

our knowledge, this work is the first integration of mono-layer graphene and silicon CMOS. Also, this is the first implementation of graphene integrated gas sensor. Heterogeneous integration of monolayer graphene and silicon CMOS can introduce a platform to exploit the unique electronic properties of monolayer graphene for gas sensing applications and also take a step further toward commercialization of ultrasensitive monolithic graphene-based gas sensors.

Furthermore, we were able to enhance sensitivity of CVD graphene to NH_3 by almost an order of magnitude. We experimentally showed that sensitivity of graphene to NH_3 can be enhanced by 7 folds compared to as-fabricated graphene by introducing NO_2 molecules as dopants. We observed this enhancement for graphene sensors microfabricated on SiO_2/Si substrate, as well as our integrated graphene-CMOS sensors. This finding not only increases current understanding on adsorption mechanisms of molecules to graphene, but also takes another step toward commercialization of graphene sensors.

Table of Contents

List of Tables

List of Figures

Chapter 1 : Introduction

1.1. MOTIVATION

Detecting presence of gas molecules within an environment is of prominent importance for controlling chemical processes and safety systems, among others [1]. NO_2, which is a major air and water pollutant and a source of acid rain [2, 3], is a byproduct of most combustion processes in electricity, transportation, and industry sectors [4, 5]. It is critical to detect traces of NO_2 molecules in these processes for controlling NO_2 emission. Similarly, detection of NH_3 is required in agricultural, industrial, and medical environments [6]. Both NO_2 and NH_3 gases are very toxic by inhalation and can impair the human respiration systems and lung tissues [7, 8]. A long-term exposure to NO_2 at concentrations above 40–100 μg/m3 (1ppm) may decrease lung function and increase adverse effects on respiratory system [9]. Current commercial NO_2 and NH_3 sensors include electrochemical sensors and metal-oxide sensors [10-13]. Electrochemical sensors and commercial metal-oxide sensors are bulky and power hungry [7]. Metal-oxide sensors are smaller compared to electrochemical sensors but the downside of metal-oxide sensors is their elevated operating temperatures (200˚C to 600˚C) to achieve relatively high sensitivity [1, 2, 7].

Nanostructures are believed to hold a great potential toward enhancing performance of gas sensors and achieving highly sensitive miniature low-cost low-power sensors that can perform at room temperature. High sensitivity and fast response of nanostructured gas sensors have already been reported for nanostructured metal-oxide sensors [14-16], nanowire devices [17, 18], and carbon nanotube (CNT) [19, 20]. This

enhancement is mainly due to increased surface to volume ratio of nanostructures that makes their electronic properties extremely sensitive to adsorbed molecules. However, some of metal-oxide and nanowire sensors operate at relatively high temperatures while others are relatively expensive [21-24]. Furthermore, the resistance of metal oxides are very high (typically in kΩ –MΩ range), inhibiting its integration with low power devices [25-27].

Discovery of graphene and its succeeding progress in nanotechnology has paved the way to design ultra-sensitive gas sensors that can detect individual gas molecules [27, 28]. Graphene is a one-atom-thick sheet of sp^2 bonded carbon atoms arranged in honey-comb structure [28]. Among nanomaterials, graphene is a promising candidate for gas sensing applications due to its unique transport properties, exceptionally high surface-to-volume ratio, and low electrical noise [27]. It can provide higher sensitivity to adsorbed gas molecules compared to CNT due to its two-dimensional structure as opposed to one-dimensional structure of CNT. Mechanically exfoliated graphene has been used to detect individual gas molecules since its discovery [27, 29, 30]. Recently, chemical vapor-deposited (CVD) graphene has received growing attention because of its potential for large scale applications [25, 31-33]. Graphene gas sensors have gained attention in industry as well. Honda Motor Company has filed a patent for a graphene-based gas sensor, which describes a sensor for atmospheric gases, such as NO, NO_2 and NH_3, based on graphene and carbon nanotubes [34].

Multi-layer graphene has been recently integrated with silicon-based complementary metal-oxide semiconductor (CMOS) as interconnect [35-38]. Also, a CMOS sensor interface that uses CNT as gas sensing medium has been reported in literature [39]. In that report, an off-chip carbon nanotube sensor array was fabricated on

a separate substrate and the CMOS sensor interface was designed and implemented to detect the presence of NO_2.

In this dissertation, a fully integrated CMOS and graphene gas sensor is presented. This integration helps benefit the high sensitivity of graphene as well as the small size, high performance, low cost, and easy mass-production advantages of CMOS technology together. Recent progress in large scale growth of CVD graphene [32] paves the path toward commercialization of graphene-based CMOS sensors and provide highly sensitive low-cost sensors for industrial applications. To best of our knowledge, this work is the first integration of mono-layer graphene and silicon CMOS. Also, this is the first implementation of graphene integrated gas sensor. Integration of monolayer graphene and silicon CMOS can introduce a platform to exploit the unique electronic properties of monolayer graphene for sensing applications and also take a step further toward commercialization of ultrasensitive heterogeneous graphene-based gas sensors.

Furthermore, we were able to enhance sensitivity of graphene gas sensor to NH_3 by almost an order of magnitude. This improvement was achieved by doping graphene with NO_2 gas. CVD graphene shows high sensitivity to NO_2 but the sensitivity of CVD graphene to NH_3 is relatively low [25, 33, 40]. There are a number of theoretical and experimental reports that show introducing defects can increase the sensitivity of graphene to NH_3 [41-43]. Graphene sensitivity can also be improved by introducing dopants such as B, N, Al, S based on some theoretical investigations [43-50]. However, an experimental study on gas sensing characteristics of p-doped graphene is still lacking. In this dissertation, we experimentally show that sensitivity of graphene to NH_3 can be enhanced by 7 folds compared to as-fabricated graphene by introducing NO_2 molecules as dopants.

1.2. OUTLINE

This dissertation is organized as follows. Chapter 2 reviews the prior studies on graphene for gas sensing applications. Also, the previous works on multi-layer graphene interconnects integrated with silicon CMOS are reviewed in this chapter. Our proposed gas sensor which is based on integration of mono-layer graphene and silicon CMOS is introduced, and a technique to enhance the sensitivity of graphene sensor to NH_3 gas is proposed.

Chapter 3 describes the design and analysis of the readout platform for our CMOS-graphene gas sensor. The silicon CMOS platform is designed and implemented in system 0.18μm TSMC CMOS technology.

Chapter 4 provides the details of the post-CMOS process assembly and describes the challenges of integrating graphene with silicon CMOS platform and methods to address these challenges.

Chapter 5 includes measurement results for graphene/CMOS integrated gas sensors as exposed to NO_2 and NH_3 gases. This chapter also describes the measurement setup designed and implemented for characterization of graphene gas sensors. A graphene sensor on SiO_2/Si substrate was designed and fabricated to certify the functionality of our measurement system. Also, the graphene/SiO_2/Si device was employed to reproduce literature results for graphene gas sensors, and provide a reference for assessing performance of graphene/CMOS sensors and effectiveness of our proposed method to enhance graphene sensitivity to NH_3.

Our measurement results revealed that as-fabricated graphene is not very sensitive to NH_3, which is consistent with previous reports [25, 33, 40]. Chapter 6

discusses our proposed technique to enhance sensitivity of graphene to NH_3 and provides measurement results and stability measurement of the method.

Chapter 7 summarizes our accomplishments and highlights the important results of our work along with some suggestions for the future research in this area.

Chapter 2 : Graphene Gas Sensors and Prior Works

2.1. INTRODUCTION

In this chapter, we explain the prior researches performed in the area of graphene NO_2 and NH_3 sensors. This is followed by the discussion on the previous studies on integration of multi-layer graphene and silicon CMOS for interconnect applications. Subsequent to explaining those studies, a novel class of graphene gas sensors is proposed. Moreover, the sensitivity of graphene to NH_3 is presented and compared to show the current gap and need in enhancing the sensitivity of graphene sensors to NH_3 gas.

2.2. COMMERCIAL NO_2 AND NH_3 SENSORS

Current commercial NO_2 and NH_3 gas sensors include electrochemical sensors and metal-oxide sensors [10-13].

2.2.1. Electrochemical Sensors

As shown in Figure 2.1, electrochemical sensors contain two electrode, working electrode and counter electrode, in contact with an electrolyte. The working electrode is in contact with both electrolyte and the ambient air to be monitored via a porous hydrophobic membrane. The electrodes/electrolyte is usually placed in a plastic housing with gas entry and electrical contacts. The gas diffused into the sensor to working electrode through the porous membrane. In the working electrode the gas is either oxidized or reduced, causing a change in the electrode potential. This electrochemical reaction causes a potential difference between working electrode and counter electrode.

The current flow due to the potential difference determines the concentration of the gas [13]. One of disadvantages of electrochemical sensors is their limited life-time; the electrolyte is used up in the reaction requiring a renewal of the electrochemical cell.

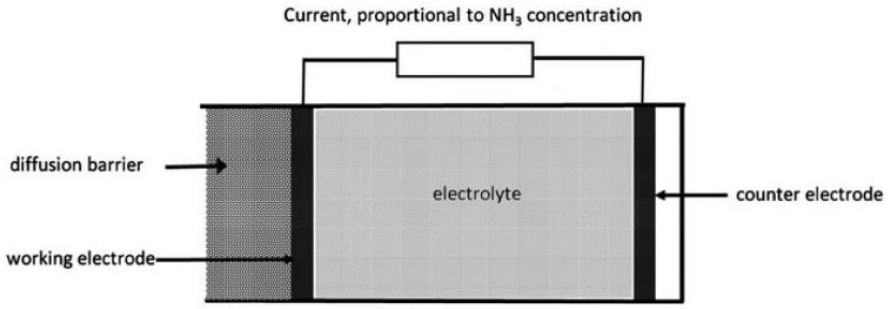


Figure 2.1: Electrochemical sensors (Figure courtesy of [13]).

2.2.2. Metal-Oxide Sensors

Metal-oxide sensors operate as following. Several kinds of oxygen adsorbates are always covering the surface of semiconductor metal-oxides in air [51]. As illustrated in Figure 2.2, these oxygen adsorbates create a depletion region on the surface of metal-oxide grains. The depth of the depletion region is a function of the oxygen adsorbates on the surface and intrinsic electron concentration in the bulk. Upon exposure of metal-oxide sensor to inflammable gases at elevated temperatures (300-500°C), the oxygen adsorbates are consumed by the reaction. Decrease in the oxygen adsorbates decreases the depletion region on the surface of metal-oxide grains resulting in a change in resistance of metal-oxide. Consequently, the resistance of metal-oxide sensor is an indicator of the amount of gas in the environment. The disadvantage of this sensor is its elevated operating temperature.

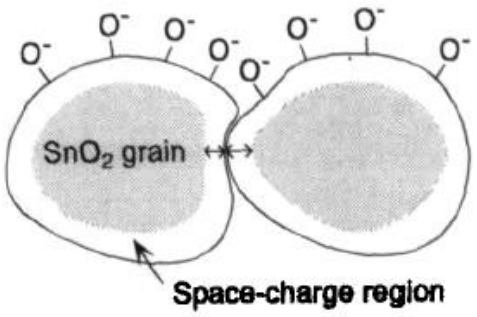


Figure 2.2: Semiconductor metal-oxide sensors (Figure courtesy of [2]).

2.3. GRAPHENE GAS SENSING PROPERTIES

Chemical and biological sensing have gained a lot of attention in recent years [23, 27, 52]. Among nanomaterials, graphene is a promising candidate for gas sensing applications due to its unique transport properties, high surface-to-volume ratio, and low electrical noise [27]. Graphene can be realized by peeling off a single layer of carbon from a graphite stack [53] or CVD method on Cu and Ni substrates [54-56]. Several graphene gas sensors capable of detecting individual gas molecules of NO_2 and NH_3 have been reported in literature [25, 27, 29, 40, 57].

2.3.1. Graphene as Resistor

As a gas molecule adsorbs to graphene, the location of adsorption experiences a local change in electrical resistance [27]. Conductivity of graphene, σ, is determined by the relative contributions of the following scattering sources [58]:

$$\sigma^{-1} = \sigma_{ci}^{-1} + \sigma_{sr}^{-1} + \sigma_{mg}^{-1} + \sigma_{LA}^{-1} + \sigma_{PO}^{-1} + \sigma_{corr}^{-1} \quad (2.1)$$

where the subscripts indicate the contributions due to charged impurities (ci), short-range scatterers (sr), midgap states (mg), longitudinal acoustic phonons (LA), polar optical phonons (PO) and surface corrugations (corr). Both Theories and experiments indicate that the dominant carrier scattering mechanism in 2D graphene monolayers is Coulomb scattering by random charged impurities located near the interface between the graphene layer and the substrate [59]. Moreover, [60, 61] showed that mobility was drastically improved by reducing carrier scattering in suspended graphene through current annealing which confirms the role of charged impurity scattering.

As shown in (2.2), charged impurity scattering in graphene produces a conductivity that is linearly dependent on charge density while inversely proportional to impurity density [59, 62-66]. Equation (2.2) can be rewritten as equation (2.3).

$$\sigma_{ci}(n) = C_{ci} e \left| \frac{n}{n_{imp}} \right| + \sigma_{res} \tag{2.2}$$

$$\sigma_{ci}(n) = ne\mu_{\mathrm{ci}} + \sigma_{res} \tag{2.3}$$

where C_{ci} is a constant, e is the electronic charge, n is the charge density of graphene, n_{imp} is charged impurity density, μ_{ci} is the carrier mobility of graphene, and σ_{res} is residual conductivity at n=0.

The conductivity of a sheet of graphene changes upon exposure to various gases including NO_2 and NH_3. There are two theories which explain the change in resistance. The first theory is that the adsorbed molecules change the local carrier concentration in graphene one by one electron, which leads to step-like changes in resistance [27]. The second theory is that graphene carrier mobility increases as NO_2 gas molecules gets absorbed on graphene's surface, acting as compensator that neutralizes the random

charged impurity centers in the substrate [30]. Regardless of physical theories behind this phenomenon, all previous experimental and theoretical studies indicate that resistivity (conductivity) of graphene decreases (increases) upon exposure to NO_2 while it increases (decreases) upon exposure to NH_3 [27, 29]. Furthermore, NO_2 acts as acceptor in interaction with graphene, while NH_3 as donor. Additionally, NH_3 has a closed-shell structure and will therefore be nonmagnetic, while NO_2 is short of one electron and is paramagnetic [57].

2.3.2. Graphene as Field Effect Transistor

I-V curve of a graphene field effect transistors is shown in Figure 2.3. The voltage at which current is minimum is called V_{dirac}. V_{dirac} moves to right upon exposure to NO_2 and moves to left upon exposure to NH_3.

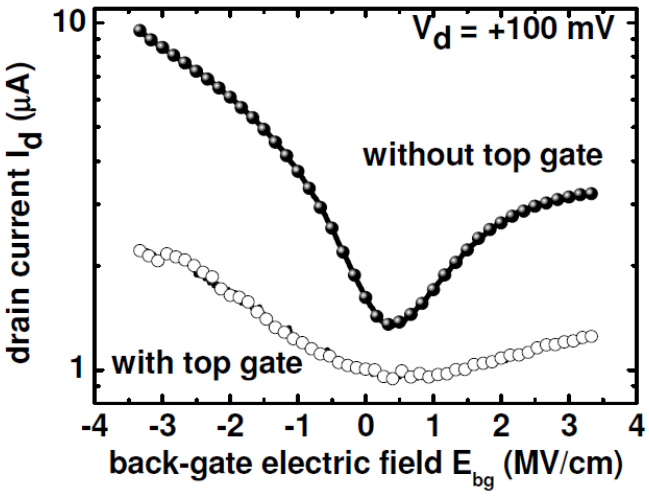


Figure 2.3: I-V curve of a graphene field effect transistor (Figure courtesy of [67]).

2.4. PRIOR STUDIES ON INTEGRATION OF MULTI-LAYER GRAPHENE AND CMOS

In 2008, Close, et al. successfully integrated carbon nanotube (CNT) and CMOS where CNT was used as an interconnect [68] (Figure 2.4).

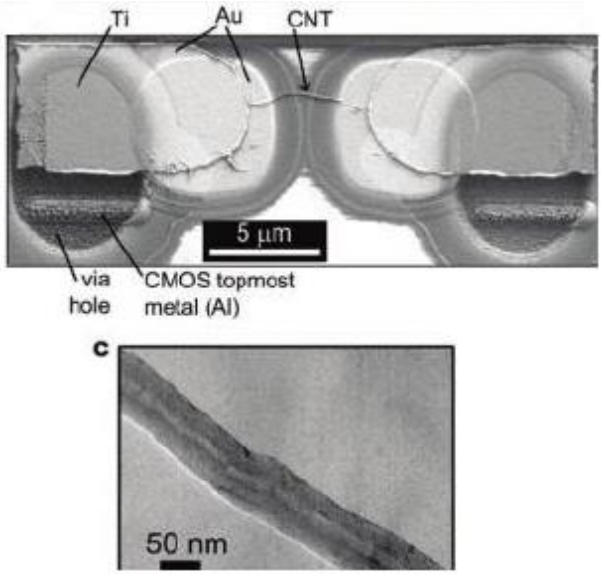


Figure 2.4: CNT interconnect (Figure courtesy of [68]).

Later on, multi-layer graphene has been integrated with silicon CMOS as an interconnect [35-38]. The thickness of graphene in [36] is 15-20nm (about 45-60 layers); consequently, it is easily visible on top of the CMOS chip (Figure 2.5). Moreover, four-layer graphene flakes integrated with CMOS as an interconnect are visible as shown in Figure 2.6 [38].

A CMOS sensor interface that uses CNT as gas sensing medium has been reported in literature [39]. In that report, an off-chip carbon nanotube sensor array was fabricated on a separate substrate and the CMOS sensor interface was designed and

implemented to detect the presence of NO_2 (Figure 2.7). The minimum NO_2 detection level in [39] was 50 part per million (ppm).

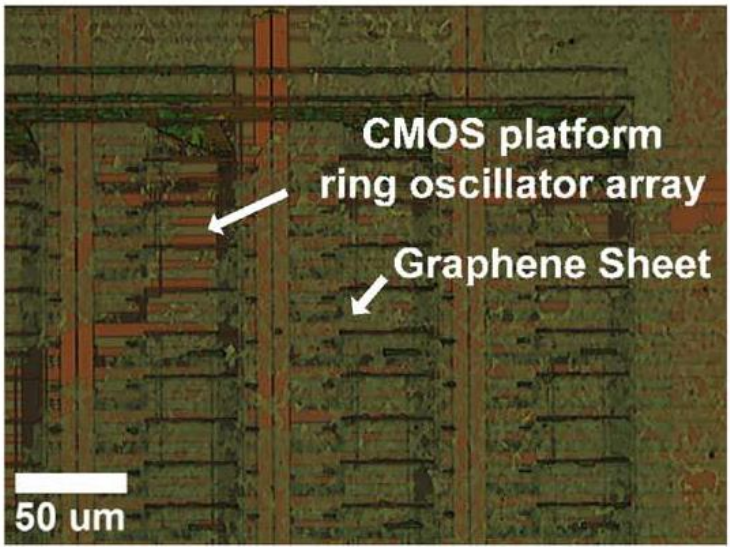


Figure 2.5: Multi-layer graphene interconnect integrated with silicon CMOS (Figure courtesy of [36]).

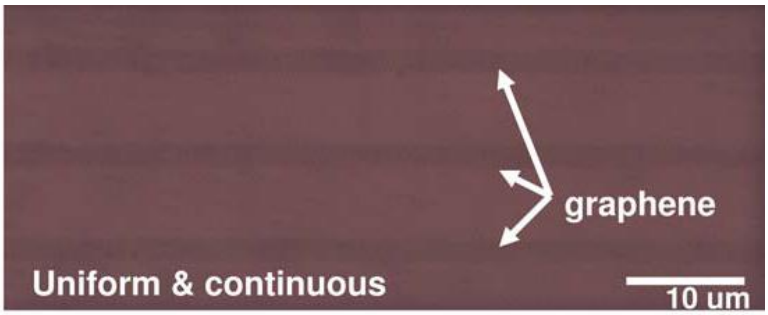


Figure 2.6: Multi-layer graphene interconnect integrated with silicon CMOS in the FPGA (Figure courtesy of [38]).

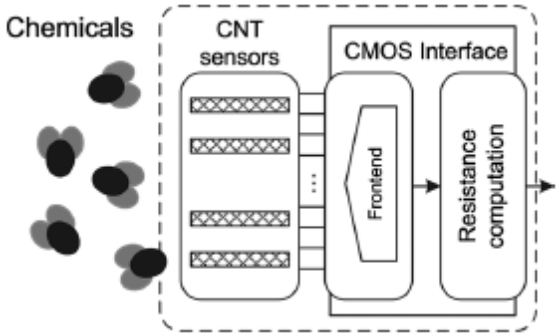


Figure 2.7: CMOS interface and CNT as the sensing medium (Figure courtesy of [39]).

2.5. THE PROPOSED GRAPHENE SENSOR

Today, there is an ever-growing demand in sensing exact concentration of environmental gasses including NO_2 and NH_3. Graphene is a promising candidate for gas sensing applications. In this dissertation, we employed graphene as a sensing medium to detect traces of NO_2 and NH_3.

2.5.1. Graphene Integrated Gas Sensors

Large scale synthesis of high quality graphene films paves the path toward industrializing graphene gas sensors. Graphene is a two dimensional (2D) material with potential capability of integration with Si CMOS. The graphene integrated gas sensor benefits the advantages of graphene and Si CMOS technology. In this dissertation, a fully integrated CMOS and graphene gas sensor is presented. This integration helps benefit the high sensitivity of graphene as well as the small size, high performance, low cost, and easy mass-production advantages of CMOS technology together. Recent progress in large scale growth of CVD graphene [32] paves the path toward commercialization of

graphene-based CMOS sensors and provide highly sensitive low-cost sensors for industrial applications. To best of our knowledge, this work is the first integration of mono-layer graphene and silicon CMOS. Also, this is the first implementation of graphene integrated gas sensor. Integration of monolayer graphene and silicon CMOS can introduce a platform to exploit the unique electronic properties of monolayer graphene for sensing applications and also take a step further toward commercialization of ultrasensitive heterogeneous graphene-based gas sensors.

The Block diagram of the proposed graphene integrated gas sensor is shown in Figure 2.8. The gas molecules

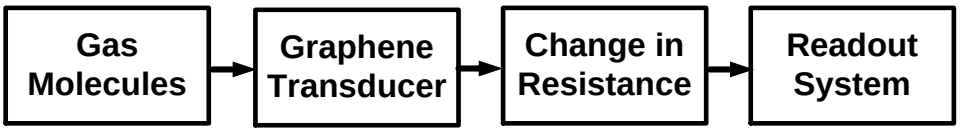


Figure 2.8: Block diagram of the proposed graphene integrated gas sensor.

The resistivity (conductivity) of a sheet of graphene changes upon exposure to various gases including NO_2 and NH_3. However, the response of graphene toward different gases is not similar. Resistivity (conductivity) of graphene decreases (increases) upon exposure to NO_2 while it increases (decreases) upon exposure to NH_3 [27]. The change in resistance of the graphene is detected by the readout circuit in the form of the output frequency. The readout circuit detects the changes of graphene resistance and sends out a signal whose frequency is an indicator of the gas concentration. The architecture of the CMOS readout system is suitable for simple remote sensing where the buffer can drive an antenna and broadcast the oscillating frequency for wireless remote

sensing. The readout circuit of the graphene integrated gas sensor was designed and implemented in CMOS 0.18μm technology to study the feasibility of graphene and CMOS integration for gas sensing applications.

2.5.2. Sensitivity Enhancement of Graphene Gas Sensors

In this study, we were able to enhance sensitivity of graphene gas sensor to NH_3 by almost an order of magnitude. This improvement was achieved by doping graphene with NO_2 gas. CVD graphene shows high sensitivity to NO_2 but the sensitivity of CVD graphene to NH_3 is relatively low [25, 33, 40].

Previous studies show that introducing defects or dopants can increase the sensitivity of graphene to NH_3 [41-49]. Results of the previous experimental studies of defected or doped graphene and their sensitivity to NH_3 have been compared in Table 2.1.

Reference	Graphene Type	Post Process	Min. Detection Level	Sensitivity
[25]	CVD growth	—	65ppm	2.2% @ 65ppm
[47]	CVD growth	Graphene surface decorated with Pt	15ppm	9.5% @ 58ppm
[48]	CVD growth	Graphene surface decorated with AuNPs	15ppm	8% @ 58ppm
[41]	Mechanical exfoliation	Introduced defect using Ar plasma	10ppm	20% @ 20ppm
This study CVD graphene	CVD growth	—	2ppm	2.7% @ 55ppm
This study NO_2-doped graphene	CVD growth	NO_2-doped	2ppm	20.2% @ 55ppm

Table 2.1: Comparison of previous experimental studies of defected and doped graphene on sensitivity to NH_3

Theoretical and experimental studies of defected graphene in gas sensing applications have been presented in literature [41-43]. Theoretical studies of doped graphene also show positive results increasing sensitivity of graphene to NH_3 [43-46, 50]. However, an experimental study on gas sensing characteristics of p-doped graphene is still lacking. In this dissertation, we experimentally show that sensitivity of graphene to NH_3 can be enhanced by 7 folds compared to as-fabricated graphene by introducing NO_2 molecules as dopants.

2.6. SUMMARY

In this section, the theory behind the current commercial sensors, the properties of graphene sensors, the previous successful integration of multi-layer graphene and si CMOS as interconnect were explained. Moreover, our proposal for implementation of integrated graphene/CMOS gas sensor and its sensitivity enhancement to NH_3 were presented.

Chapter 3 : CMOS Readout System for Graphene Gas Sensor

3.1. INTRODUCTION

This chapter presents the design of readout circuit for gas sensing platform. The readout circuit was designed and implemented in CMOS 0.18μm technology to study the feasibility of graphene and CMOS integration for gas sensing applications. First, the architecture of the readout system is explained. Then, a comprehensive analysis of the chosen circuit is demonstrated. To end, the transfer function and sensor transient output is illustrated.

3.2. ARCHITECTURE OF READOUT SYSTEM

The architecture of the CMOS readout circuit of the gas sensor is illustrated in Figure 3.1. To study the feasibility of integrated graphene/CMOS gas sensor, a ring oscillator is implemented as the core sensing block. As depicted in Figure 3.1, one interconnect wire in the oscillator loop was intentionally missing, and was to be implemented with graphene on the chip surface during the post-CMOS processing. Sensing measurements were carried out by changing the output frequency of the ring oscillator, f_s, based on the value of the transducer which is the change in graphene resistance. This topology is promising for NO_2/NH_3 gas sensing because of three advantages. First, this configuration provides selectivity for the sensor as exposed to NH_3 or NO_2, since exposure to NH_3 gas decreases while NO_2 gas increases the oscillation frequency. The second is that the sensor output is a data of frequency format as opposed to amplitude; consequently, it is less susceptible to amplitude-affecting non idealities of the measurement path. Last but not least, the architecture of the CMOS readout system is

suitable for simple remote sensing where the buffer can drive an antenna and broadcast the oscillating frequency for wireless remote sensing.

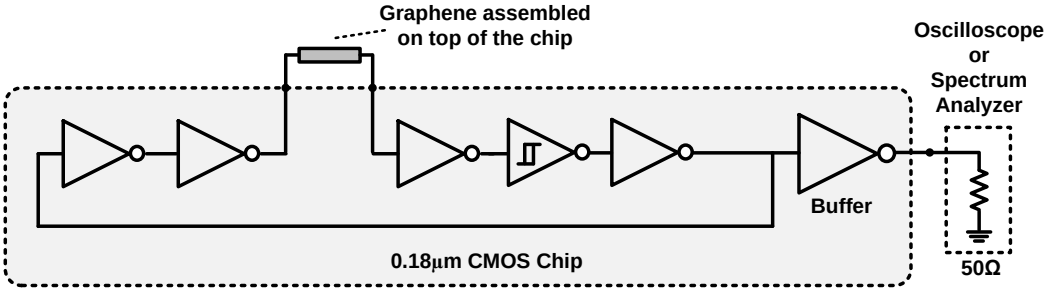


Figure 3.1: Circuit-level diagram of graphene integrated gas sensor.

The on-chip section of the sensor is shown inside the gray box. The graphene transducer is assembled on top of the CMOS chip in subsequent post-CMOS processing steps.

3.3. TRANSDUCER

In this work, graphene is used as the transducer of the environmental gas sensor. The resistivity (conductivity) of a sheet of graphene changes upon exposure to various gases including NO_2 and NH_3. However, the response of graphene toward different gases is not similar. Resistivity (conductivity) of graphene decreases (increases) upon exposure to NO_2 while it increases (decreases) upon exposure to NH_3 [27]. The change in resistance of the graphene is detected by the readout circuit in the form of the output frequency. Figure 3.2 shows the transducer section of the graphene integrated gas sensor.

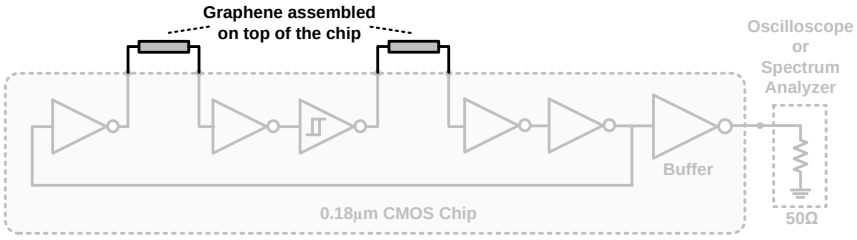


Figure 3.2: Transducer of graphene integrated gas sensor.

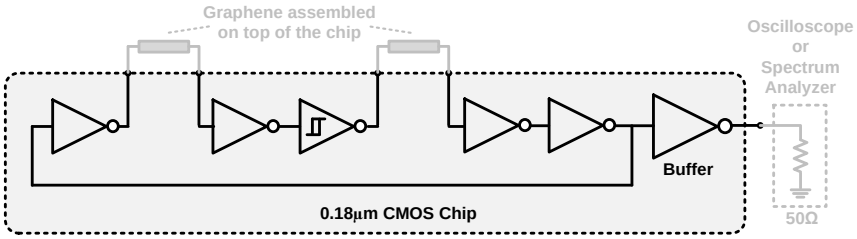


Figure 3.3: Readout circuit of graphene integrated gas sensor.

3.4. GRAPHENE INTEGRATED RING OSCILLATOR ANALYSIS

The readout circuit of the graphene integrated gas sensor is designed and fabricated in TSMC 0.18μm CMOS technology. Figure 3.3 demonstrates the readout circuit in the gray box. The readout circuit detects the changes of graphene resistance and sends out a signal whose frequency is an indicator of the gas concentration. The readout circuit is a five stage ring oscillator implemented in CMOS technology with one or two missing interconnects. During post-CMOS processing, the missing interconnects are assembled by sheets of graphene on top of the CMOS chip.

3.4.1. Output Frequency of N-Stage Ring Oscillator

An *N*-stage CMOS ring oscillator is illustrated in Figure 3.4. Odd number of inverters is requires in order to have oscillation in a ring oscillator.

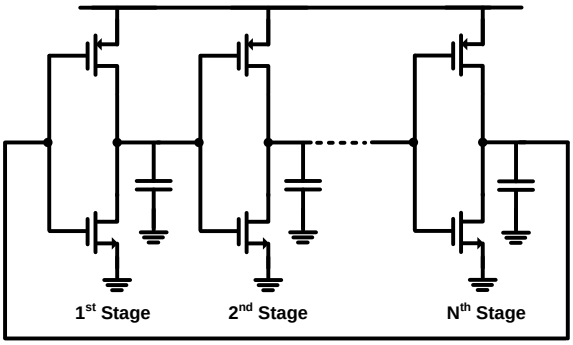


Figure 3.4: *N*-stage CMOS ring oscillator.

The output frequency of an *N*-stage CMOS ring oscillator is illustrated in equation (3.1).

$$f_s = \frac{1}{2Nt_D} \tag{3.1}$$

where f_S is the output frequency, t_D is the delay of each inverter, and N is number of inverters.

$$t_D = R_{ON}(C_g + C_d) \tag{3.2}$$

where R_{ON} is the output resistance of each inverter, C_g is the total capacitance of the gate of each inverter and C_d is the total capacitance of the drain of each inverter. It is assumed that all NMOS and CMOS transistors have equal C_g, C_d, and R_{ON} values. Hence, output frequency of an *N*-stage CMOS ring oscillator is illustrated in equation (3.3).

$$f_s = \frac{1}{2\{NR_{ON}(C_g+C_d)\}} \tag{3.3}$$

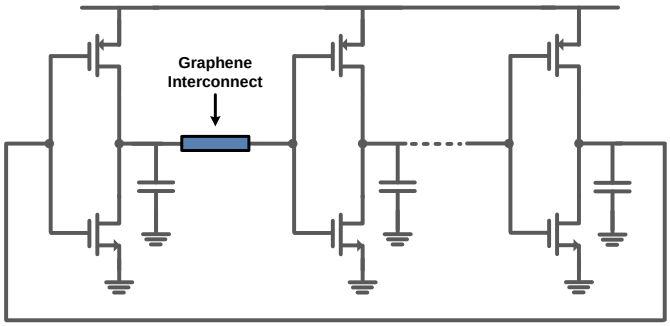


Figure 3.5: *N*-stage graphene integrated ring oscillator.

3.4.2. Optimum Number of Inverters in a Ring Oscillator

Figure 3.5 shows an *N*-stage graphene integrated ring oscillator. As illustrated in equation (3.4), the frequency of the graphene integrated ring oscillator is a function of graphene resistance and number of inverters. Equation (3.5) shows the sensitivity of output frequency with respect to change in graphene resistance.

$$f_s = \frac{1}{2\{NR_{ON}(C_g+C_d)+(R_{GR}+\Delta R_{GR})C_g\}} \tag{3.4}$$

$$S_{R_{Gr}}^{f_s} = \frac{\frac{\partial f_s}{f_{s,Nominal}}}{\frac{\partial R_{GR}}{R_{GR,Nominal}}} = \frac{-2C_gR_{GR}}{2\{NR_{ON}(C_g+C_d)+R_{GR}C_g\}} \tag{3.5}$$

where R_{GR} is the resistance of the graphene and ΔR_{GR} is the change in graphene resistance due to gas exposure. It is worth to mention that $S_{R_{Gr}}^{f_s}$ is different from actual sensitivity, which is shown in equation (3.6).

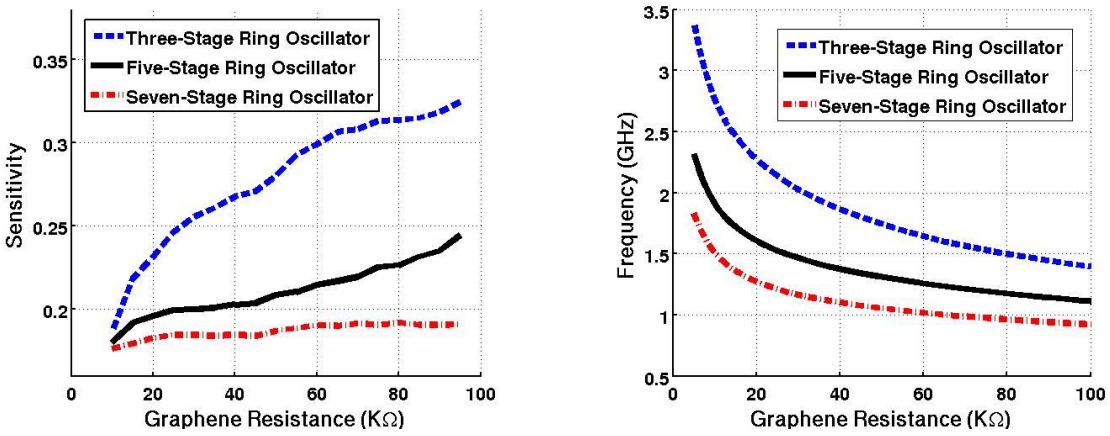
$$S_{gc}^{f_s} = \frac{\frac{\partial f_s}{f_{s,Nominal}}}{\frac{\partial R_{GR}}{R_{GR,Nominal}}} \times \frac{\frac{\partial R_{GR}}{R_{GR,Nominal}}}{gc} \tag{3.6}$$

where *gc* indicates gas concentration.

Sensitivity of the sensor, $S_{R_{Gr}}^{f}$, increases by increase in graphene resistance or by decrease in the number of inverters. The initial value of graphene resistance depends on growth condition, transfer method, and all post-CMOS processing steps. Consequently, we cannot predict the initial value of graphene resistance. Figure 3.6(a) shows the sensitivity of three-stage, five-stage, and seven-stage graphene integrated ring oscillator with respect to graphene resistance. Figure 3.6(b) demonstrates the output frequency of the ring oscillators with respect to graphene resistance. As predicted in equation (3.5) and shown in Figure 3.6(a), sensitivity of three-stage and seven-stage ring oscillators are the highest and the lowest respectively. Overall, the sensitivity decreases for higher order ring oscillators. The three-stage ring oscillator has a high output frequency for this technology and is more susceptible to phase noise [69, 70]. The phase noise of an *N*-stage ring oscillator is illustrated in equation (3.7) [69]. The detail of deriving this equation is demonstrated in appendix A.

$$\mathcal{L}(\Delta f) \simeq \frac{1}{6}\left(\frac{1}{NV_{swing}}\right)^2 \left(\frac{kT}{V_{char}}\right)\left(\frac{\mu_{eff}W_{eff}C_{ox}\Delta V^2}{\eta^3 LC_{node}^2}\right)\left(\frac{1}{\Delta f}\right)^2 \tag{3.7}$$

where N is the number of inverters, k is the Boltzmann constant, T is the absolute temperature, V_{char} is the characteristic voltage of the device, ΔV is gate overdrive voltage in the middle of transition, μ_{eff} is the mobility, W_{eff} and L are the effective channel width and length of the transistor, and C_{ox} is the gate-oxide capacitance per unit area, η is the proportionality constant, C_{node} is the effective capacitance on output node, V_{swing} is the voltage swing across the capacitor C_{node}.



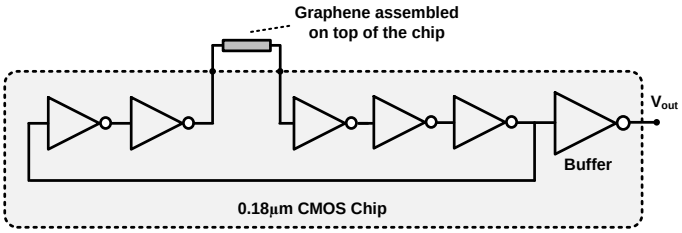
(a) (b)

Figure 3.6: (a) Sensitivity of graphene integrated ring oscillators with different orders, (b) Output frequency of graphene integrated ring oscillator with different orders.

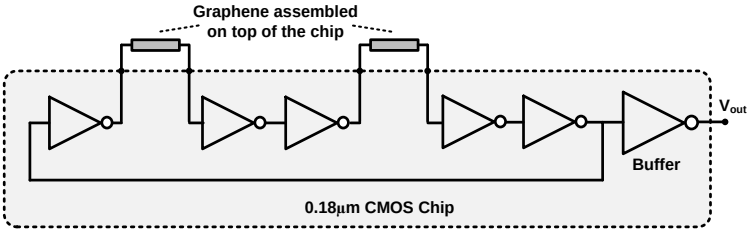
As shown in equation (3.7), the phase noise of ring oscillators increases by decrease in internal node swing voltage or order of the ring oscillator. The five-stage ring oscillator is less susceptible to noise than a three-stage one and has a relatively good sensitivity. Consequently, we decided to have five-stage ring oscillators as a readout platform for our gas sensor.

3.4.3. Optimum Number of Graphene Interconnects in a Ring Oscillator

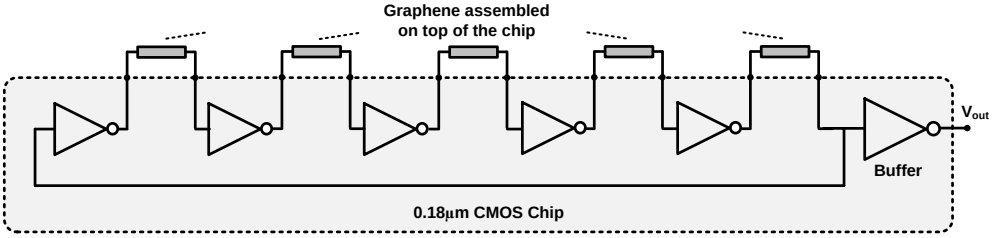
Another method to increase the sensitivity is to have a readout circuit with the graphene transducer incorporated in a distributed pattern. Figure 3.7 demonstrates readout circuit with fully lumped, partially lumped, and fully distributed graphene transducers.



(a)



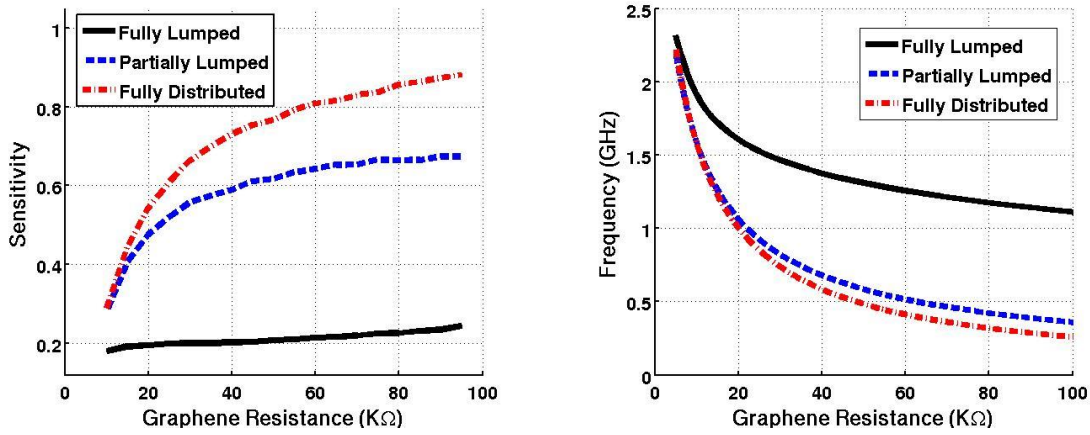
(b)



(c)

Figure 3.7: Readout circuit with (a) fully lumped graphene transducer, (b) Partially lumped graphene transducer, (c) Fully distributed graphene transducer.

Figure 3.8 compares the sensitivity of a five-stage ring oscillator with fully lumped, partially lumped, and fully distributed graphene transducer as graphene resistance increases. The total value of graphene resistance in all three structures is equal.



(a) (b)

Figure 3.8: (a) Sensitivity of a five-stage ring oscillator with fully lumped, partially lumped, and fully distributed transducer, (b) Output frequency of a five-stage ring oscillator with fully lumped, partially lumped, and fully distributed transducer.

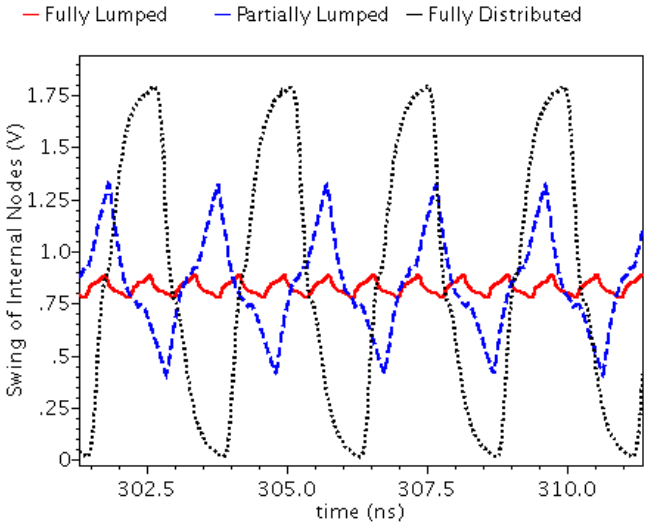


Figure 3.9: Swing of internal nodes of five-stage ring oscillators with fully lumped, partially lumped, and fully distributed transducer.

The sensor with fully lumped transducer shows lower sensitivity to graphene resistance change. The main reason is that the voltage swing of internal nodes in lumped structure is less than the voltage swing of internal nodes in fully distributed structure. Internal node voltage swings of fully lumped, partially lumped, and fully distributed structures are shown in Figure 3.9. Based on equation (3.7), phase noise of the ring oscillator increases as the swing of internal nodes decreases. Consequently, the fully lumped structure is more susceptible to noise and less sensitive to resistance change.

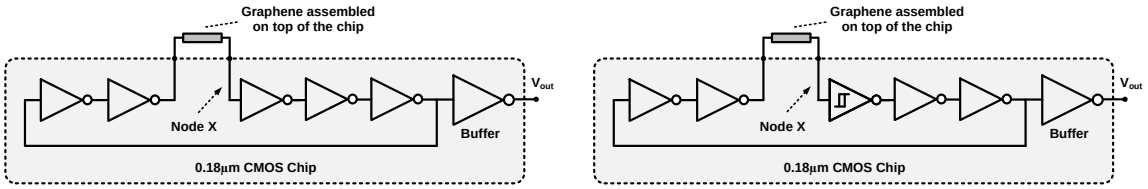
For post-CMOS processing steps, the fabrication yield of the sensor with fully distributed transducer is lower than its fully lumped counterpart. The main reason is that five graphene interconnects should be successfully integrated with the CMOS platform as opposed to one or two. Table 3.1 compares the sensitivity and post-CMOS processing yield of different topologies. In this study, we chose readout circuits with fully lumped and partially lumped transducers to benefit the higher yield of the former and moderate sensitivity of the latter.

	Sensitivity	Yield of Post-CMOS Processing
Fully Lumped	Low	High
Partially Lumped	Moderate	Moderate
Fully Distributed	High	Low

Table 3.1: Sensitivity and post-CMOS process yield of different topologies.

3.4.4. Sensitivity Analysis of Schmitt-Trigger Ring Oscillator

Another method to further increase the sensitivity of the readout circuit is to use Schmitt-trigger inverters as opposed to basic inverters. Figure 3.11 compares the sensitivity of two five-stage ring oscillators shown in Figure 3.10.



(a) (b)

Figure 3.10: (a) Five-stage ring oscillator with basic inverters, (b) Five-stage ring oscillator with basic and Schmitt-trigger inverters.

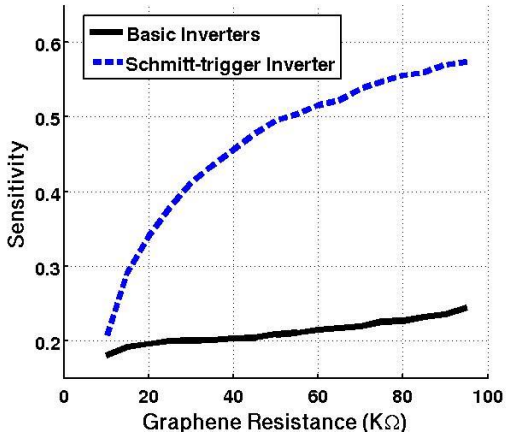


Figure 3.11: Sensitivity of a five-stage ring oscillator with basic and Schmitt-trigger inverters.

In Schmitt-trigger inverters, the swing of the internal nodes increases. Consequently, phase noise of fs is reduced and sensitivity is increased. Figure 3.12 shows the swing of the internal nodes of the two mentioned ring oscillators. Adding more

Schmitt-trigger inverters, will not necessarily increase the sensitivity. That's mainly because even one Schmitt-trigger inverter is enough to increase the swing of the internal node and more Schmitt-trigger inverters will not further increase the voltage swing.

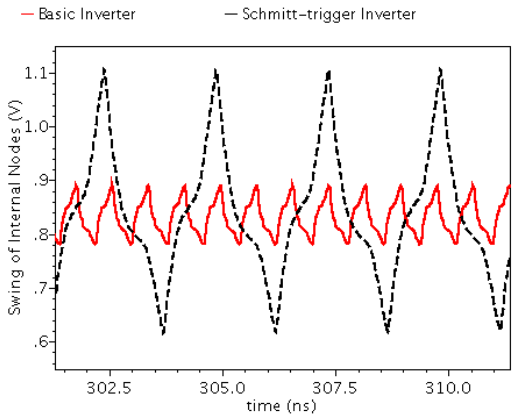
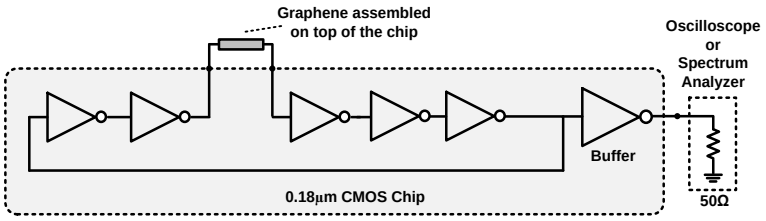


Figure 3.12: Swing of node X of the five-stage ring oscillator with basic and Schmitt-trigger inverters.

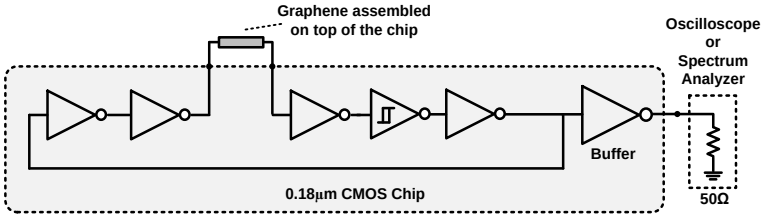
3.5. READOUT CIRCUIT

Based on the discussions in previous section, four readout circuits for graphene integrated gas sensor were proposed. The readout circuits were chosen such that the combination of yield of post-CMOS processing and sensitivity to gas concentration is relatively high. As shown in Figure 3.13, all four readout circuits are five-stage ring oscillators with arrangements of one/two graphene interconnects and basic/Schmitt-trigger inverters. In this report, the readout circuits will be referred to based on the following naming convention: the circuit with one missing interconnect is called RO1 (Figure 3.13 (a)), the circuit with one missing interconnect and one Schmitt-trigger inverter is called RO1S (Figure 3.13 (b)), the circuit with two missing interconnects is

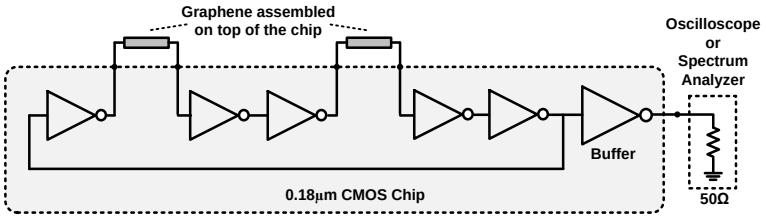
called RO2 ((Figure 3.13 (c))), and the circuit with two missing interconnects and one Schmitt-trigger inverter is called RO2S (Figure 3.13 (d)).



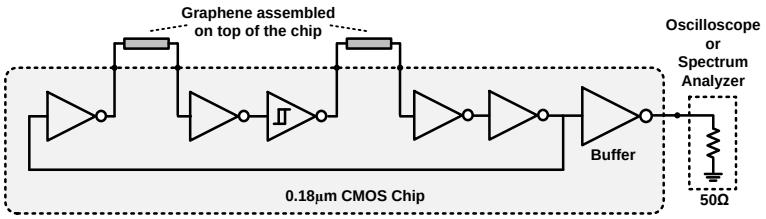
(a)



(b)



(c)



(d)

Figure 3.13: Readout circuit with (a) fully lumped graphene transducer, (b) fully lumped graphene and Schmitt-trigger inverter, (c) partially lumped graphene transducer, (d) partially lumped graphene and Schmitt-trigger inverter.

3.5.1. Basic Inverter Design

The implementation of basic inverter is demonstrated in Figure 3.14.

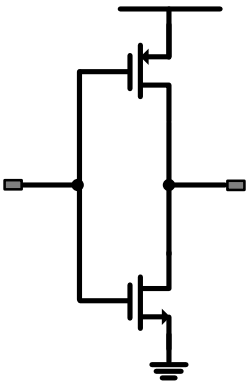


Figure 3.14: Basic inverter.

3.5.2. Schmitt-Trigger Inverter Design

Figure 3.15 shows the implementation of Schmitt-trigger inverter with a 940 mV hysteresis window. The circuit shown in Figure 3.15 has a well-known design [71].

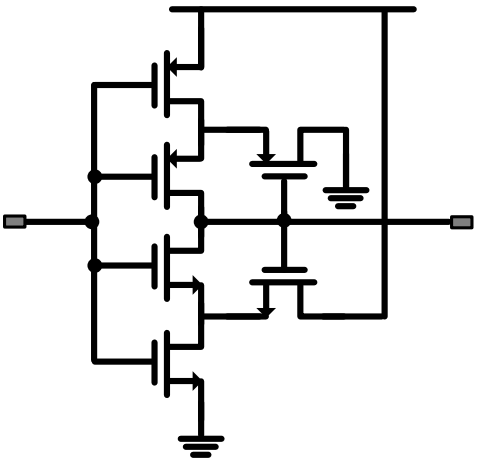


Figure 3.15: Schmitt-trigger inverter.

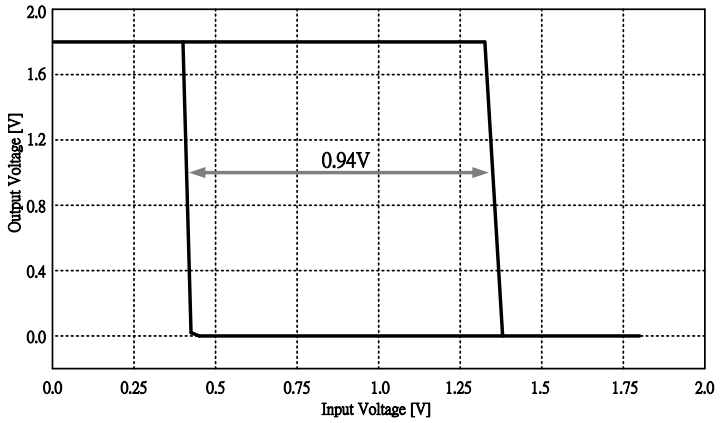


Figure 3.16: Input-output characteristic of Schmitt-trigger inverter.

The input-output characteristic of the Schmitt-trigger inverter with supply voltage of 1.8V is shown in Figure 3.16.

3.5.3. Buffer

The ring oscillator is followed by a buffer to be able to handle the load. The load is the 50Ω resistance of the oscilloscope or spectrum analyzer. The buffer consists of three inverter stages whereas the size of the third inverter is larger than second, and the size of the second inverter is larger than the first one.

3.5.4. Sensor Transfer Function and Transient Output

Figure 3.17 shows the transient output of the four readout circuits assuming 30KΩ resistance for all the graphene interconnects.

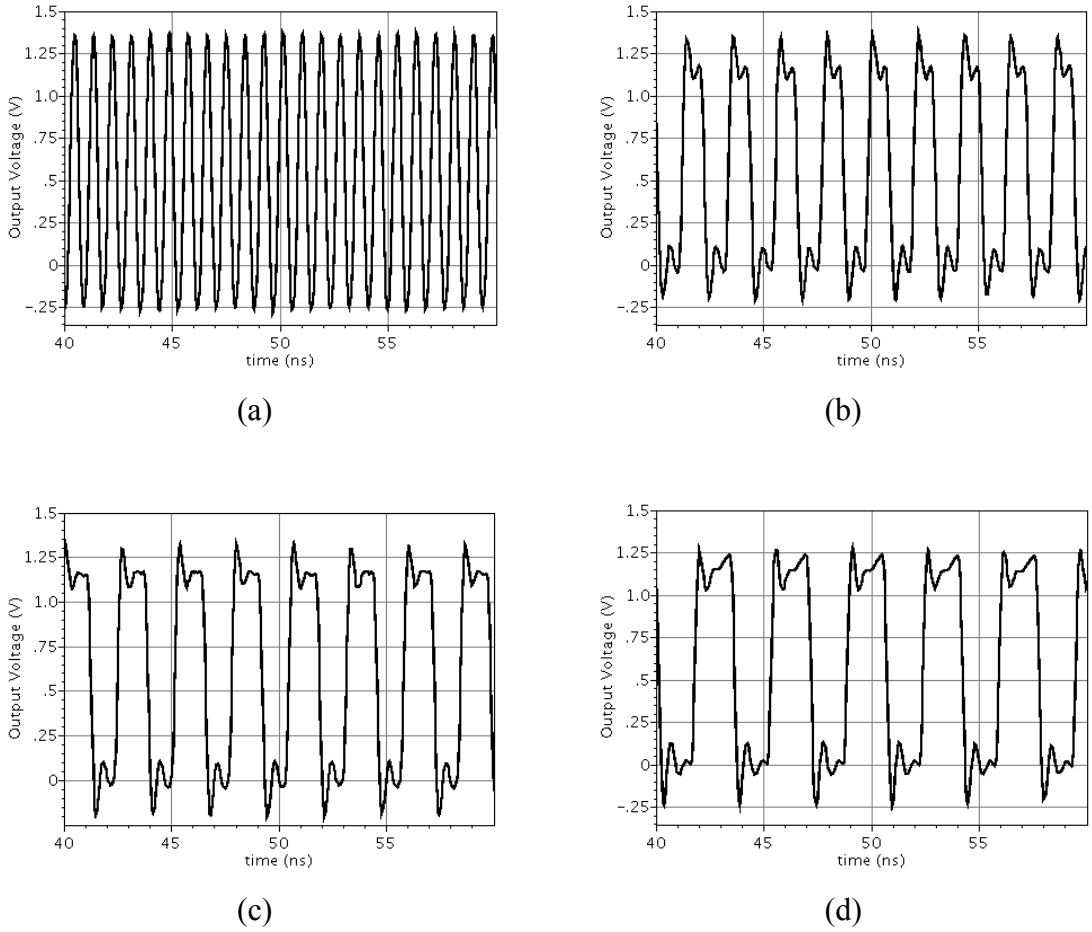
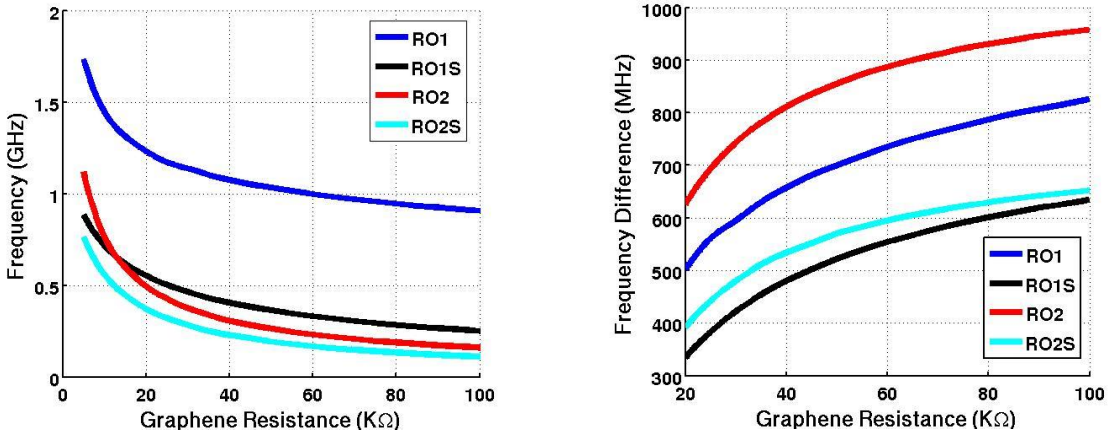
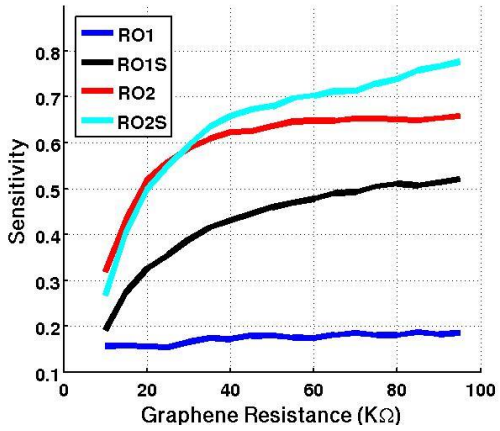


Figure 3.17: Sensor transient output for (a) RO1 at R=30KΩ, (b) RO1S at R=30KΩ, (c) RO2 at R=30KΩ, (d) RO2S at R=30KΩ.

Figure 3.18 illustrates the output frequency, sensor transfer function, and sensitivity vs. graphene resistance for four readout circuits.



(a) (b)



(c)

Figure 3.18: (a) Output frequency of sensor, (b) Sensor transfer function, (c) Sensitivity of sensor.

3.6. SUMMARY

The design of the readout circuit of graphene integrated gas sensor was discussed in this chapter. The readout circuit was implemented in TSMC 0.18μm CMOS

technology. The transducer of the sensor is graphene interconnects which will be assembled on top of the CMOS chip through post-CMOS processing steps. The post-CMOS assembly process is covered in next chapter.

Chapter 4 : Integration of Graphene Sensor with Silicon CMOS

4.1. INTRODUCTION

In order to complete the design, implementation, and fabrication of graphene integrated gas sensors, graphene interconnects were assembled on top of the CMOS platform. This chapter presents post-CMOS processing steps to integrate graphene interconnects with underlying CMOS readout circuit. The challenges faced in the fabrication and integration of the sensor is explained here. Also, the layout techniques and fabrication methods to overcome the obstacles are described in this chapter.

4.2. KEY DESIGN RULES OF TSMC 0.18 μM CMOS TECHNOLOGY

Our platform CMOS circuit was implemented using a 0.18μm CMOS technology from TSMC. Table 4.1 summarizes the key design rules for the TSMC 0.18μm CMOS technology. Six aluminum metallization layers are available as shown in Figure 4.1. The manufactured chips are passivated by a double layer of silicon oxide and silicon nitride.

M1 Thickness / Width	0.53 / 0.23 μm
M2 Thickness / Width	0.53 / 0.28 μm
M3 Thickness / Width	0.53 / 0.28 μm
M4 Thickness / Width	0.53 / 0.28 μm
M5 Thickness / Width	0.53 / 0.28 μm
M6 Thickness / Width	1.20 / 0.44 μm
Passivation Layer Thickness	1.75 μm

Table 4.1: Key design rules of TSMC 0.18μm CMOS technology

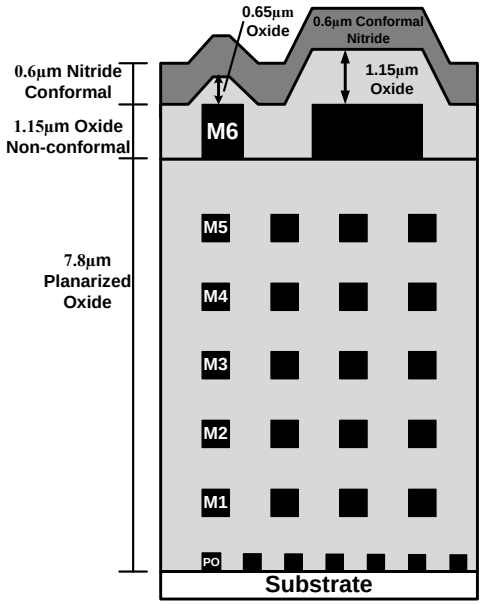


Figure 4.1: Cross section of a 0.18μm CMOS TSMC chip showing the six levels of aluminum metallization M1, M2, M3, M4, M5, and M6 and the backend dielectric stack. PO refers to polysilicon transistor gate.

The procedure to build a graphene integrated gas sensor in as follows. First, we designed a purely-CMOS readout circuit with select interconnects intentionally missing from the layout, and had it manufactured by a CMOS foundry (TSMC). Then, we post-processed the CMOS chip at cleanroom to implement the missing parts with graphene interconnects right on the chip surface at the required locations and connected the graphene interconnects to the readout circuit. Figure 4.2 shows the cross section of CMOS chip after integration of graphene and CMOS. The graphene interconnect acts as transducer and converts the gas concentration to a change in resistance of graphene. A change in graphene's resistance will cause a change in frequency of the output signal which determines the concentration of the gas.

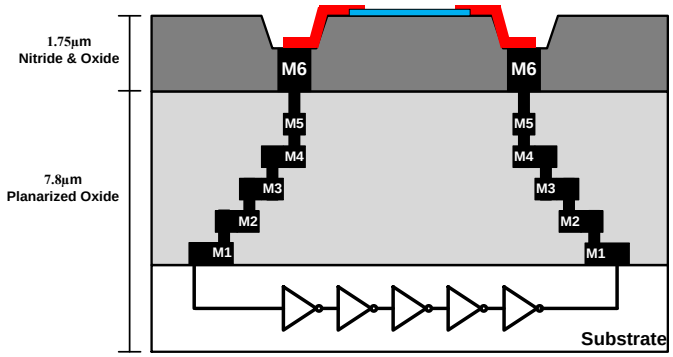


Figure 4.2: Graphene interconnect as transducer assembled on top of the readout circuit.

4.3. Layout Challenges of Graphene and CMOS Integration

The layout of the designed CMOS platform including all four readout circuits is illustrated in Figure 4.3.

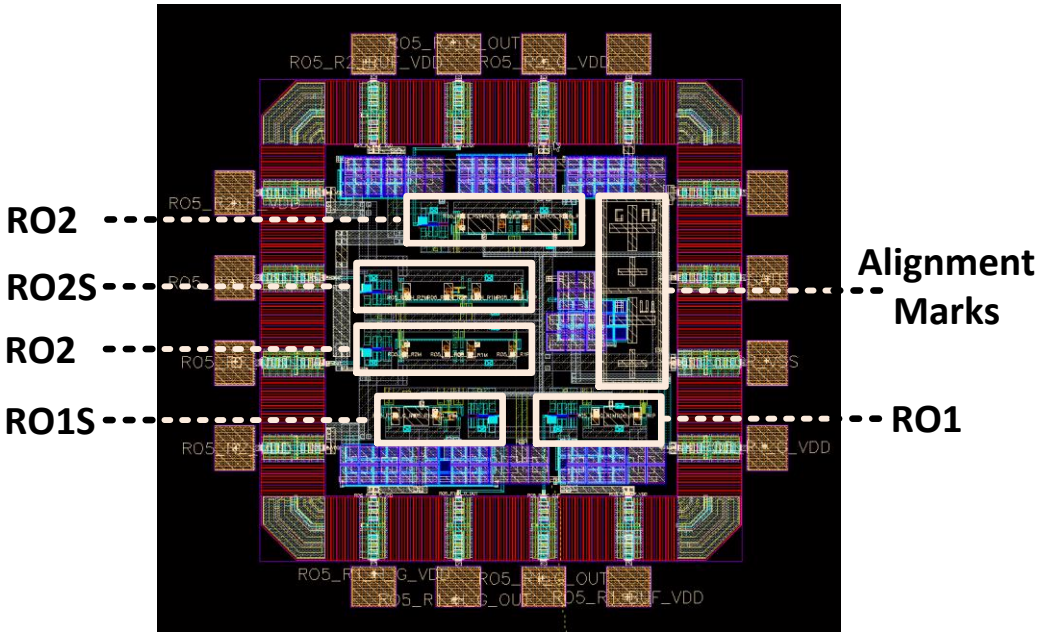


Figure 4.3: Layout of the CMOS platform.

Although post-CMOS processing of this sensor is challenging, some layout techniques can be used to overcome the obstacles. The techniques used to increase the yield of post-CMOS processing are explained in this section.

4.3.1. Alignment Marks

The post-CMOS processing includes two steps of lithography. Alignments marks are required to perform any lithography step, either photo lithography or electron-beam lithography (EBL). There are two methods to design the alignment marks on the CMOS chip: One is to pattern and deposit metal to form the alignment marks as part of the post-CMOS assembly process. Then, use those alignment marks during the rest of the post-CMOS processing steps. The other technique is to design the alignment marks on the CMOS chip and have it manufactured by a CMOS foundry. The latter technique is used in this design. As shown in Figure 4.1, the passivation layer, covering sixth metal layer (M6), is composed of double layers of silicon oxide and silicon nitride. Both silicon oxide and silicon nitride are almost transparent; consequently, any pattern that is formed in topmost metal layer (M6) is visible under microscope. As shown in Figure 4.4, one set of alignment marks for post-CMOS lithography exposure were patterned in the sixth metal layer.

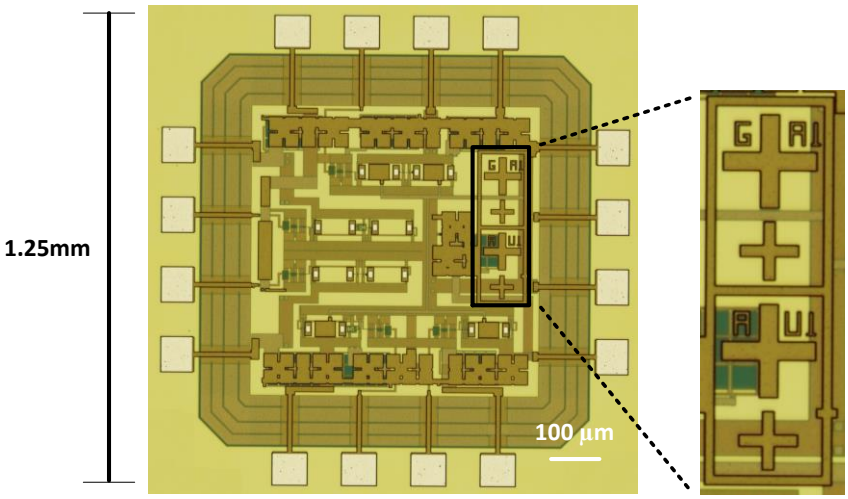


Figure 4.4: A micrograph of alignment marks.

4.3.2. Non-Planar Surface

The other serious issue during post-CMOS processing is the non-planar surface of the top part of the die, as shown in Figure 4.5. Maximum height difference at chip surface is as high as 1.8 µm.

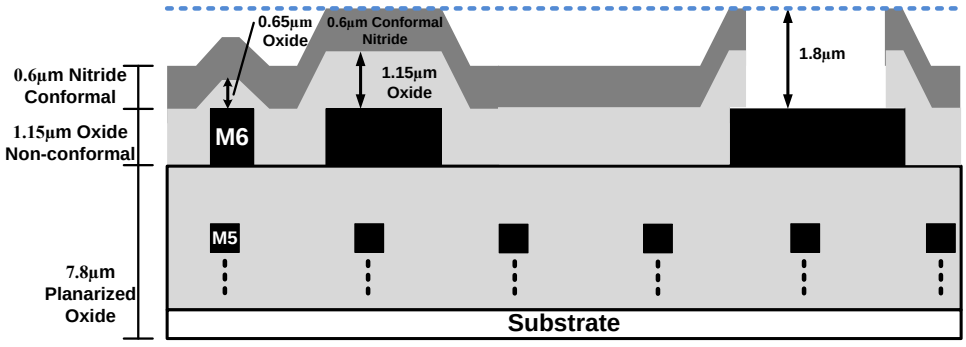


Figure 4.5: Height profile of etched passivation layer

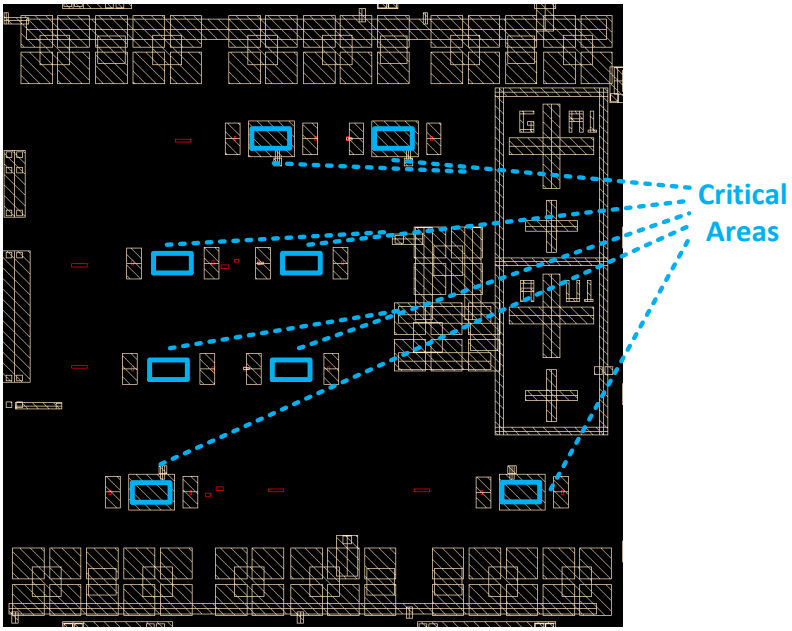


Figure 4.6: M6 layer of the layout of the CMOS platform.

The thickness of PR and PMMA is not uniform across the chip due to surface topography; consequently, the quality of lithography and lift off was tremendously degraded. The surface topography also affected graphene transfer. The yield of graphene transfer on CMOS chip was decreased compared to SiO_2 substrate.

The best method to improve the topography of the surface is to avoid using M6 layer across the entire surface or at least at critical locations of the surface. Figure 4.6 illustrates the layout of M6 across the chip surface. In this design M6 is only used for alignment marks and establishment of connection between graphene and underlying CMOS chip.

In order to establish connection between graphene and the underlying CMOS circuit, two pieces of M6 is required as shown in Figure 4.7 (a). As explained in section

4.4.2, there is a thick layer of PMMA (poly methyl methacrylate) on top of graphene right after transfer of graphene to the CMOS chip. The next step after graphene transfer is to resolve that PMMA layer by acetone. The purpose of graphene transfer is to put graphene in the area between M6 openings. However, the height difference of about 1.2µm causes the graphene to peel off or tear right after dissolving the PMMA in acetone. To improve the graphene transfer yield, a piece of M6 is designed in layout to make that part of the surface locally planar. Figure 4.7 (b) illustrates the explained concept. In chapter 6, the yield of graphene transfer for both gated and non-gated interconnects are compared.

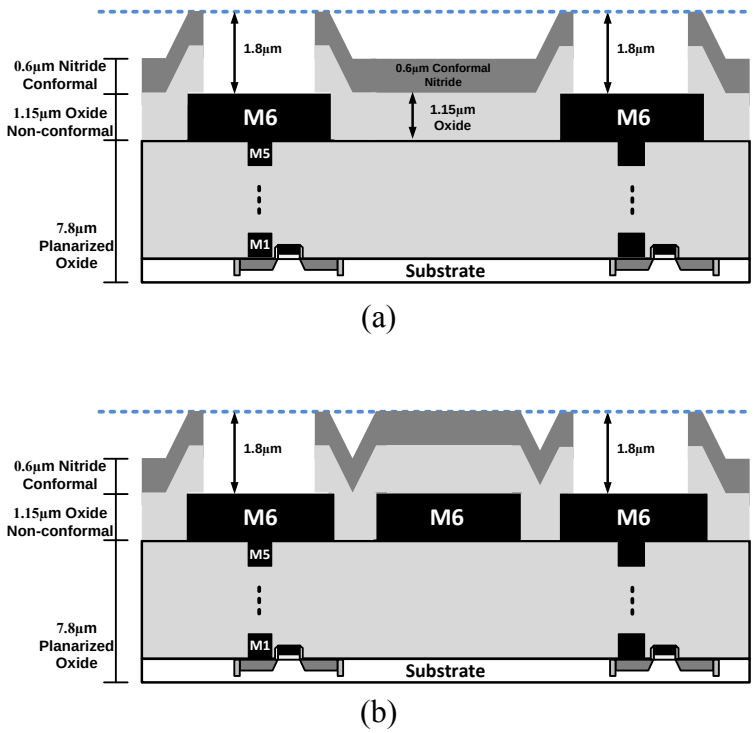


Figure 4.7: Chip cross section of (a) Non-gated graphene interconnect, (b) Gated graphene interconnect.

4.3.3. Passivation Opening for Graphene Integration

As illustrated in Figure 4.2, via holes were etched through the CMOS passivation layer to reveal M6 aluminum layer. Next, a combination of titanium and gold was deposited on via holes and nearby areas to establish electrical connections between graphene and the underlying CMOS transistors. There are two methods to etch via holes through the passivation layer. The first one is to carry out a combination of dry and wet etch as part of the post-CMOS processing steps. The second is to design an etching pattern for passivation layer in the layout of the CMOS and have it manufactured by a CMOS foundry. The challenges of the first technique are explained later in this chapter. The second technique is easier but extra consideration is required. The sidewall angle of the etched via is an important factor in the success of establishing electrical connection between graphene interconnect and CMOS readout circuit. As shown in Figure 4.8, a connection will be established if the sidewall angle is less than 90 degrees. On the other hand, no connection will be established for sidewall angles of more than 90 degrees.

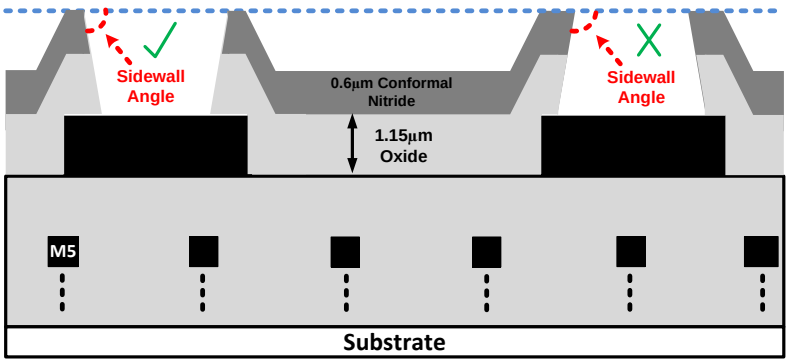
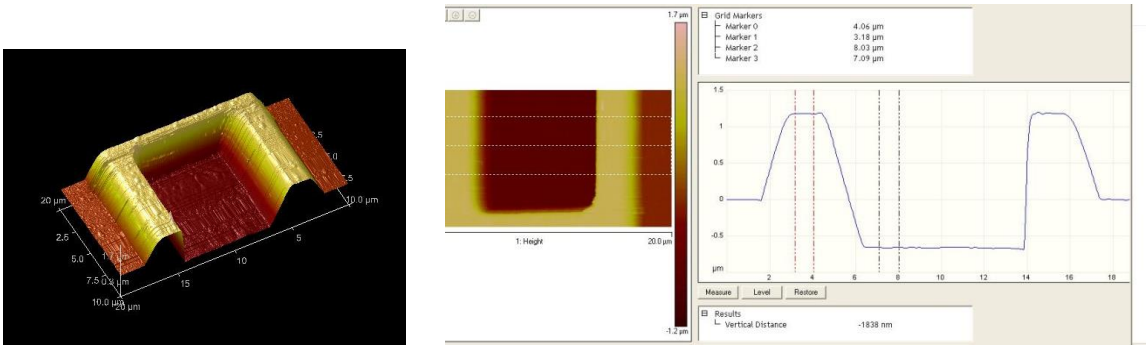


Figure 4.8: The sidewall angle of etched via hole. The left side shows the desired sidewall angle.

The topography of the chip surface with via opening through CMOS fabrication foundry (TSMC) was measured by Atomic Force Microscope (AFM) and shown in Figure 4.9. The sidewall angle is less than 90 degrees and good enough for establishing connection between graphene and CMOS circuit.



(a) (b)

Figure 4.9: AFM monograph for height profile of the via hole in passivation layer etched by TSMC

4.4. POST-CMOS PROCESSING

As explained previously in this report, the goal of post-CMOS processing is to grow graphene, transfer the graphene to the top of the CMOS chip, and connect the transferred graphene to the readout circuitry through the via hole in passivation layer and the top-most metal layer, M6. All the post-CMOS processing steps are carried out at Microelectronics Research Center at The University of Texas at Austin.

4.4.1. Graphene Growth

Graphene is either exfoliated from graphite or grown by CVD [28, 72]. In this work, graphene samples were synthesized by CVD on copper film [73]. 500nm

evaporated Cu on SiO_2/Si was used as a starting material. Then, Cu film was annealed at 1000C for 5min. The last step was growth of graphene under Methane flow at the same temperature. All growth steps were performed inside the black magic chamber that is shown in Figure 4.10.

Figure 4.10: Black magic system by Aixtron for growing graphene by chemical vapor deposition.

4.4.2. Graphene Transfer

The CVD graphene was transferred to a Si/SiO_2 substrate via a conventional PMMA-supported wet-transfer process using ammonia persulfate copper etchant [32, 74]. The transfer steps are shown in Figure 4.11.

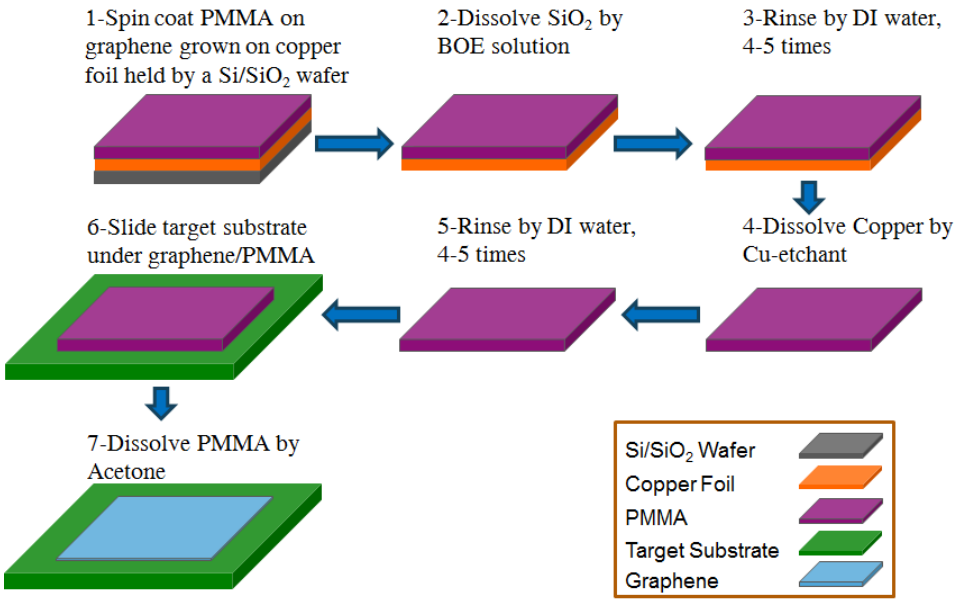


Figure 4.11: Graphene transfer steps.

4.4.3. Optical Lithography or Electron Beam Lithography

Lithography is challenging on such small pieces, because of the accumulation of resist at the chip corners during spin coating. We typically observed that by centering the sample on the spin coating chuck, photo-resist (PR) and PMMA (poly methyl methacrylate) grossly accumulated within 500μm and 200μm of the four chip corners respectively. We also noticed that corner accumulation can be replaced by edge accumulation if we put the sample not at the center of the spin coating chuck. Any patterning near one chip edge was impossible because of this edge accumulation, known as the edge bead. It also degraded the achievable resolution and overlay accuracy either

using optical lithography or electron beam lithography. Optical lithography did not yield acceptable resolution because the mask could not get into full contact with the chip surface. With electron beam lithography, finding of alignment marks was challenging due to charge accumulation on the surface. Typical achievable resolution was around 3μm and 1μm using the KarlSuss MA6 mask aligner and Carl Zeiss ebeam lithography tool respectively. Their respective overlay accuracy was around 2μm and 0.5μm.

The thickness of PR and PMMA was not uniform across the chip due to surface topography; however, smoother surface could be obtained using PMMA. The non-uniform resist reduces the quality of lift off process. The thickness of resist should be at least 2μm to have a good lift off on a surface of 1.8μm topography. However, thick resist causes a thick accumulation on edges of the die, which severely degrades the quality of the lithography. We generally observed that the yield of lift-off for electron beam lithography is higher than the one for optical lithography.

To achieve a higher resolution and overlay accuracy as well as a more successful lift-off step, we chose electron beam lithography.

4.4.4. Other Fabrication Steps

Upon delivery by TSMC, the 2.5 mm x 2.5 mm CMOS chip was bonded (using epoxy) to a carrier 1-in x 1-in silicon substrate. This significantly facilitated handling the chip in the clean room, as well as protecting the CMOS chip from electrostatic discharge since the chip was never directly touched thereafter.

Figure 4.12 illustrates the post-CMOS processing flow to implement the graphene interconnects on the CMOS platform. First, CVD graphene was growth in the black magic and transferred to the CMOS chip (step 2). Then, the graphene interconnect on the

CMOS chip were patterned using electron beam lithography (EBL) and selectively etched using a low-power oxygen plasma reactive-ion-etch (RIE) (step 3). Next, electron beam lithography followed by e-beam evaporation was used to pattern Ti/Au (5nm/45nm) contacts that establish the electrical connection between graphene interconnects and CMOS transistors (step 4). The graphene interconnects have a width of 5 μm and length of 15 μm. To improve the quality of lift off and decrease the chance of tearing or folding the graphene, the PMMA was not removed after step 3 and PMMA for the succeeding step (step 4) was spin coated on top of the existing PMMA.

The layout techniques developed in this study greatly improved the yield and simplified the post-CMOS processing. Table 4.2 compares the complexity of post-CMOS processing flow in this study as well as the previous reports.

It is worth mentioning that mono-layer graphene is invisible on top of the CMOS chip and other techniques such as Raman spectroscopy or scanning electron microscopy (SEM) were employed to verify the existence of graphene in predefined locations.

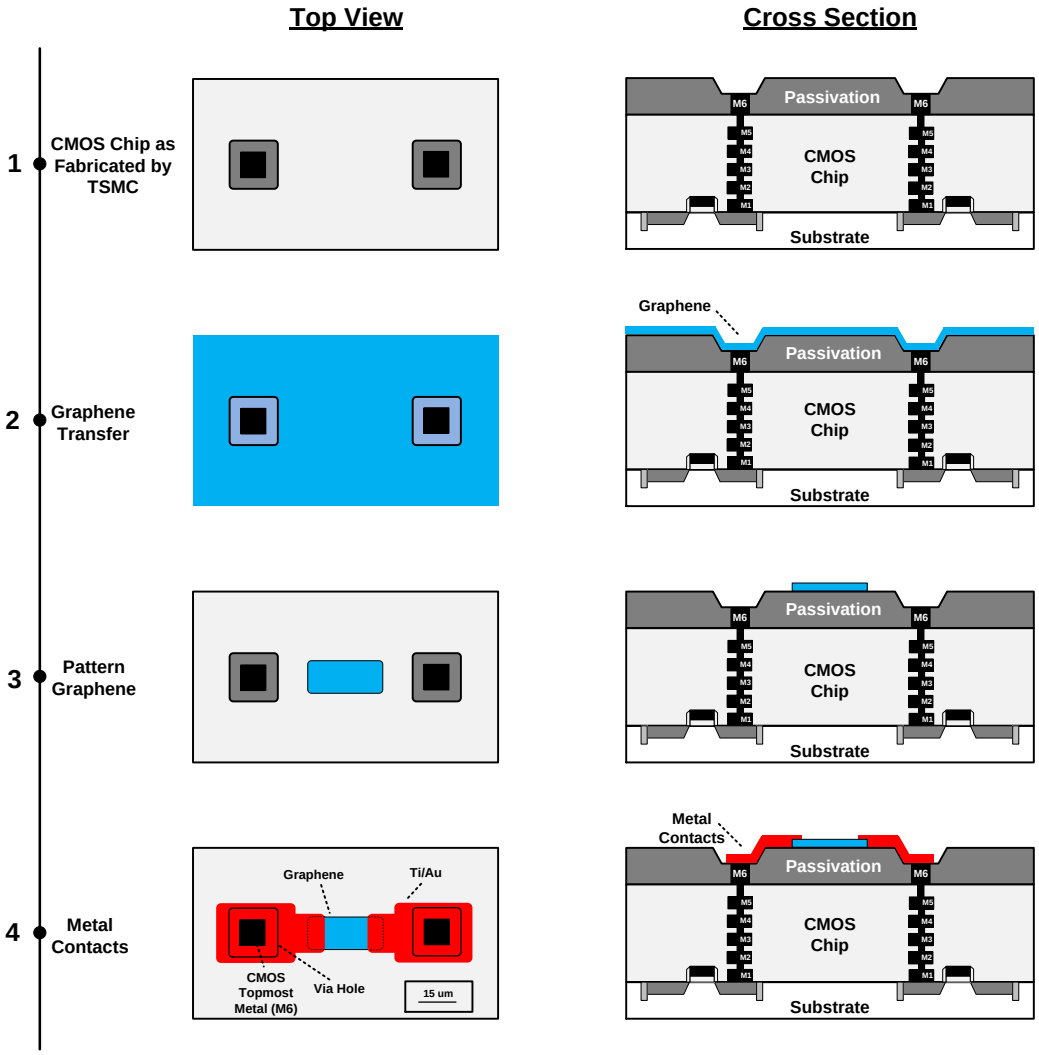
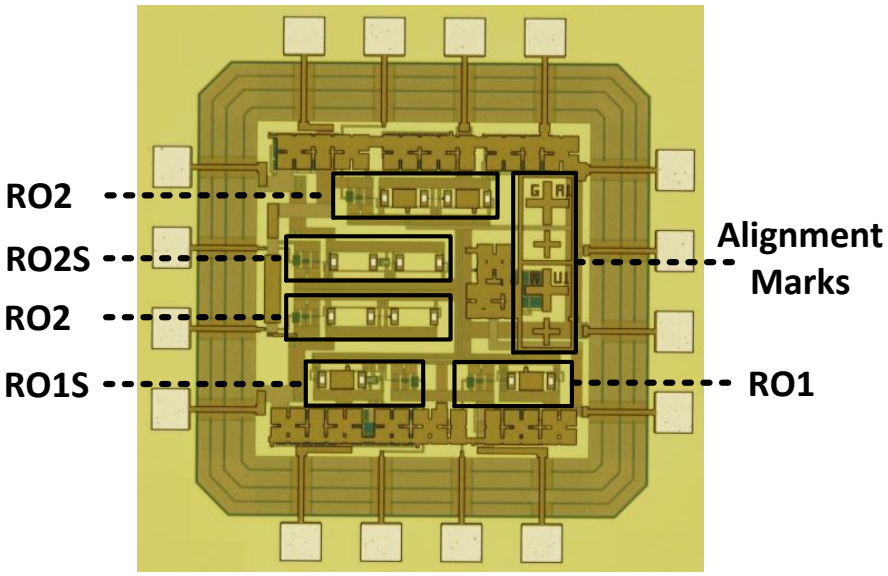


Figure 4.12: Post-CMOS processing steps.

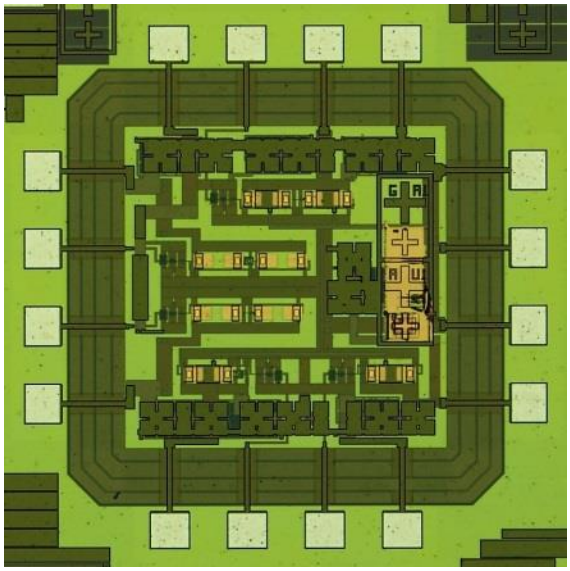
Reference	Post-CMOS Processing Steps
[36]	▪ Transfer and Pattern of Graphene ▪ Deposit Cr/Au Contacts ▪ Etch Via holes through passivation layer ▪ Deposit Ti contact to establish connection
[37]	▪ Transfer and Pattern of Graphene ▪ Deposit Ti/Pt Contacts ▪ Etch passivation layer ▪ Deposit via plug
[38]	▪ Etch passivation layer ▪ Deposit via plug ▪ Transfer and Pattern of Graphene ▪ Deposit Contacts
This Study	▪ Transfer and Pattern of Graphene ▪ Deposit Ti/Au Contacts

Table 4.2: Comparison of post-CMOS processing steps

Figure 4.13 shows the optical micrograph of CMOS chip before and after post-CMOS assembly process. A close-up optical and a scanning electron microscopy (SEM) micrograph of a sensor with one graphene interconnect are shown in Figure 4.14.

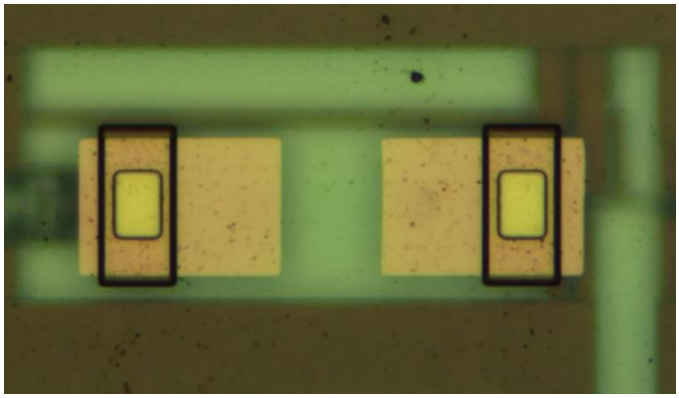


(a)

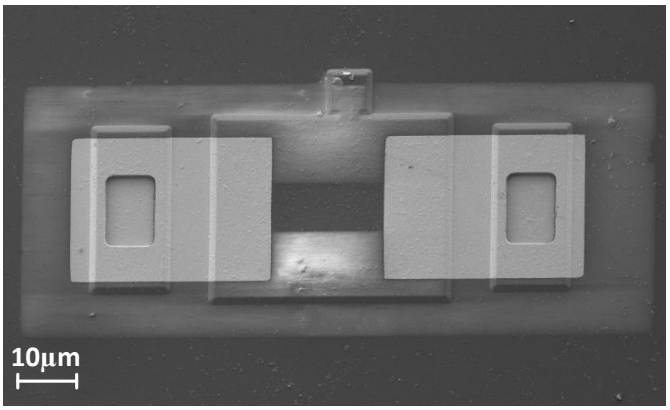


(b)

Figure 4.13: CMOS chip micrograph (a) As fabricated by TSMC, (b) After post-CMOS processing.



(a)



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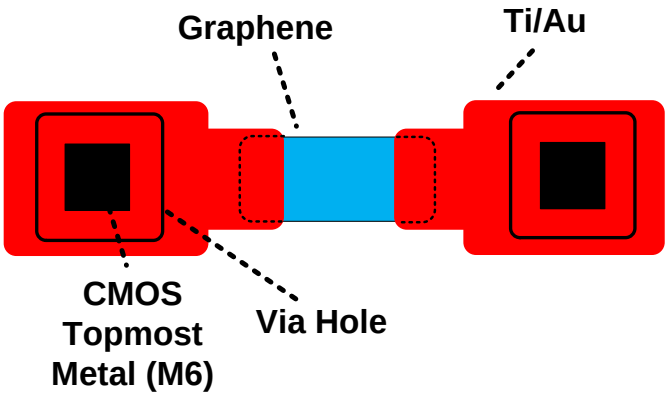


(c)

Figure 4.14: Close-up views of a fabricated graphene integrated sensor (a) microscope image, (b) SEM image, (c) corresponding diagram.

Graphene is not visible on CMOS chip under optical microscope. However, graphene can be seen under SEM due to accumulation of charge on adjacent non-conductive areas. As shown in Figure 4.14(b), there is charge accumulation on areas of passivation layer, which is made of a combination of silicon oxide and silicon nitride, where graphene has etched away. In comparison, there is no charge accumulation on areas of passivation layer covered with conductive graphene. This phenomenon produces a contrast and allows us to visually inspect the graphene channels under SEM and find channels with no tears or cracks. Figure 4.15 shows SEM micrograph of a torn graphene channel. The Raman signature of graphene on those areas with no charge accumulation confirms that these areas are covered with graphene.

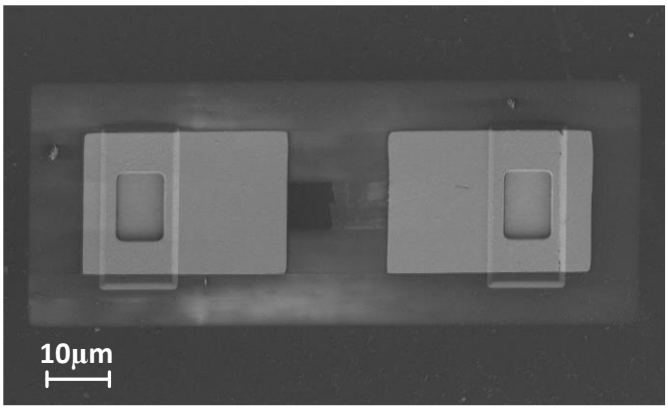


Figure 4.15: Close-up view SEM image.

4.5. INTEGRATION REQUIREMENTS: FIRST AND SECOND IMPLEMENTATIONS

The improvements in circuit, layout, and fabrication techniques employed in this study were achieved after an unsuccessful implementation of graphene integrated gas

sensor. Table 4.3 demonstrates the improvements in circuit design, layout design, and fabrication techniques.

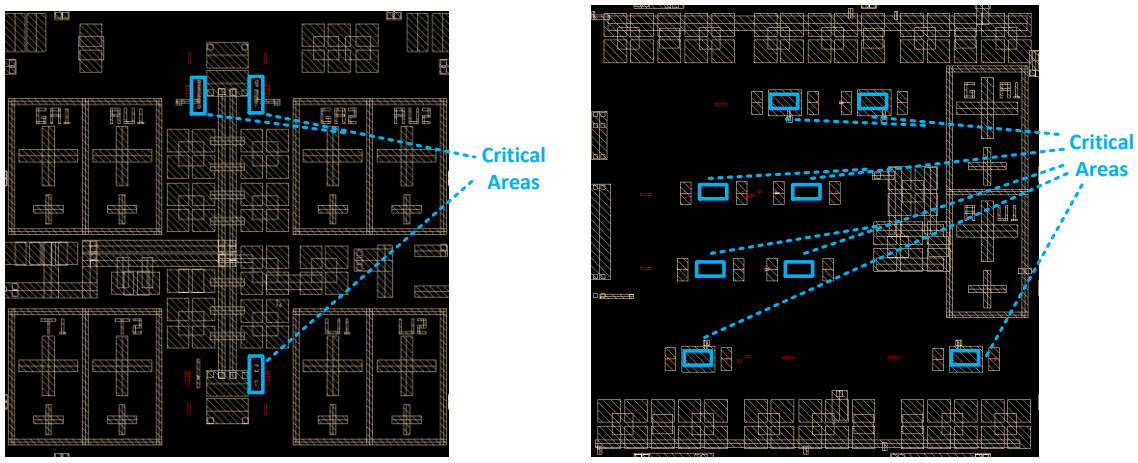
	First Implementation	Second Implementation
Circuit Improvements	▪ Basic inverters ▪ Fully lumped transducer	▪ Basic & Schmitt-trigger inverters ▪ Fully & partially lumped transducers
Layout Improvements	▪ More design in M6 layer ▪ Etch via holes manually ▪ Non-gated graphene interconnects	▪ Less design in M6 layer ▪ Etch via hole through TSMC ▪ Gate graphene interconnects
Post-CMOS Processing Improvements	▪ Optical lithography	▪ Electron beam lithography

Table 4.3: Comparison of first and second implementation.

Circuit improvements include adding partially lumped transducer and readout circuit. Moreover, replacing one of the basic inverters with Schmitt-trigger inverter further increased the sensitivity.

In first implementation, optical lithography and dry/wet etch were carried out to pattern and etch via holes through passivation layer. The thickness of PR is not uniform across the chip due to surface topography whereas etch rate is equal everywhere on the surface. Consequently, controlling the etch process to obtain the desired pattern became challenging and over-etching of areas with thinner PR occurred. In the second implementation, fabrication yield was considerably improved by having the CMOS foundry etch via holes through passivation layer to expose M6.

With proper arrangement of top-most metal layer, M6, we could obtain smoother surface, higher yield of graphene transfer, more uniform PMMA thickness, and easier lift-off. Figure 4.16 illustrates the layout of M6 layer for both implementations.



(a) (b)

Figure 4.16: M6 layer of (a) First implementation, (b) Second implementation.

In the first implementation, M6 was used for all supply routings, alignment marks, connection to CMOS circuit, and bypass capacitors; consequently, there were so many metals on M6 layer. In the second implementation, M6 was only used for alignment marks and connection to CMOS circuit. This change made the surface more planar and helped increasing the yield of post-CMOS process.

4.6. SUMMARY

In this chapter, the implementation and post-CMOS assembly process of graphene integrated gas sensor were explained. Moreover, the challenges of such integration and

the layout and fabrication techniques to facilitate the integration were discussed. Next chapter presents the measurement setup to investigate the sensor response of our integrated gas sensor. Measurement setup incudes designing the sensor chamber as well as the peripheral required to control the gas concentration and the pressure inside the chamber.

Chapter 5 : Measurement of Graphene Integrated Gas Sensor

5.1. INTRODUCTION

In the previous chapters design, implementation, and post-CMOS processing of the graphene integrated gas sensor were demonstrated. We presented a novel platform for the development and deployment of gas sensors in integrated systems. For this purpose, graphene was integrated on top of the CMOS chip. Our platform CMOS circuit was implemented using a 0.18μm CMOS technology from TSMC.

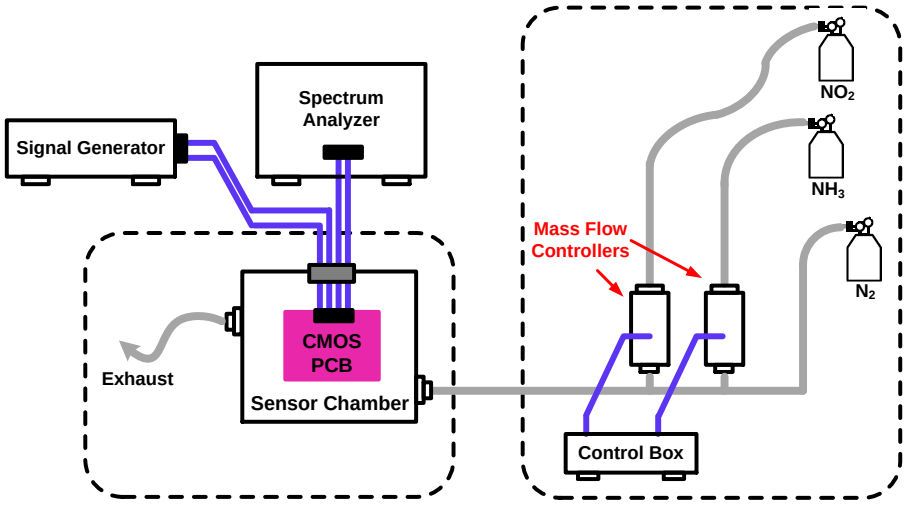
This chapter presents the measurement setup used to characterize the graphene integrated gas sensor. The measurements of the gas sensor were carried out in a specific chamber under particular pressure and temperature conditions.

A graphene device on Si/SiO_2 substrate, named test device, was designed, fabricated, and measured in our sensor chamber for two purposes. First, the test device was used to certify the functionality of our sensor chamber. Second, the test device was employed to reproduce the sensor responses and gas sensitivities reported in literature as a baseline for the measurements of our graphene integrated gas sensor.

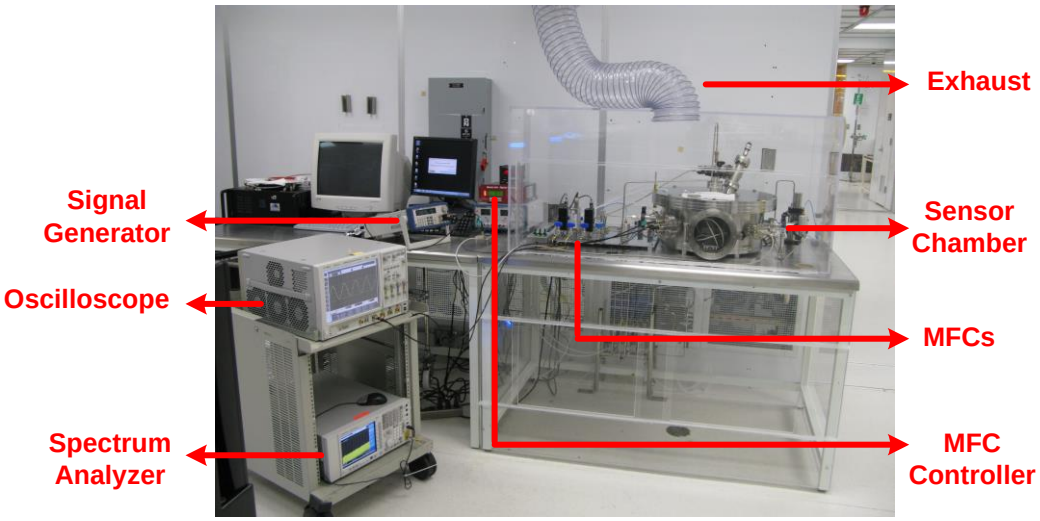
This chapter also presents the measurement results of graphene integrated gas sensors. The measurements fall into two major classifications. The purpose of first group of measurements is to demonstrate that the designed and post-CMOS processed device is functional while the second sets of measurement validate the specifications of the sensor. Measurements of the first category include Raman spectroscopy, probing of the graphene interconnects, and proving the functionality of CMOS ring oscillators and post-CMOS processing recipes. Sensitivity response measurements are carried out inside the sensor chamber as the second set.

5.2. MEASUREMENT SETUP

Figure 5.1 demonstrates the measurement setup that is developed to measure the sensor response. The probe pads of the graphene device were wire bonded to the leads of a chip carrier using west-bond 7476D. The chip carrier was placed in an electrical socket on a printed circuit board (PCB), making it possible to electrically address the graphene device. Figure 5.2 shows the PCB board designed for our sensor measurement. The PCB board was placed inside a sensor chamber with electrical feed-through to perform the measurement. The functionality of the sensor is measured by exposing the graphene sensor to various concentrations of nitrogen dioxide (NO_2) and ammonia (NH_3). Gas concentration was controlled using mass flow controllers (MFCs) ahead of a mixing manifold, with N_2 as a diluting gas. Two MFCs were used each with a separate control switch: one for NH_3 and one for NO_2. Each of the NH_3 and NO_2 gases were 100 parts-per-million (ppm), in dry air, at their source. Using MFCs with nitrogen as the diluting gas permits a range of concentrations for each test gas from 2 to 100 ppm. All tests were carried out at atmospheric pressure and room temperature. As shown in the diagram, signal generator provides the supply for the CMOS chip and the output is measured using a spectrum analyzer or oscilloscope.



(a)



(b)

Figure 5.1: (a) Diagram of sensor chamber, (b) Sensor measurement setup

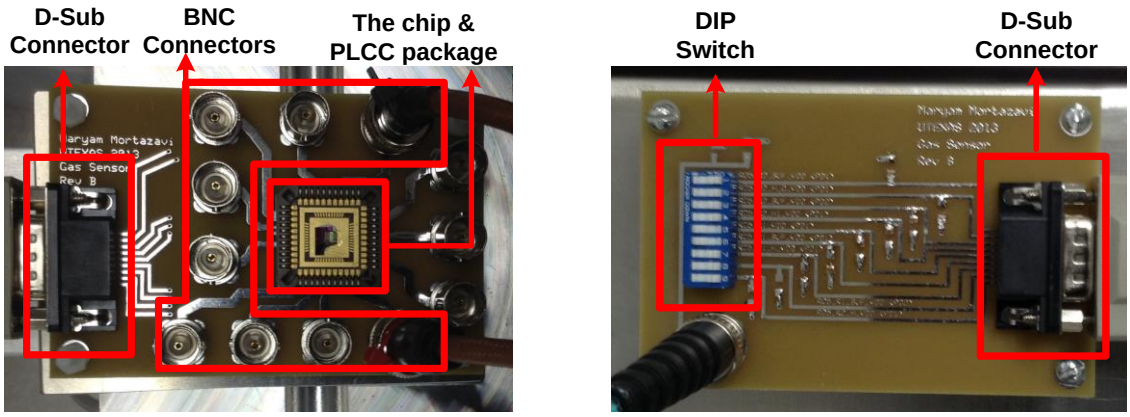


Figure 5.2: Printed circuit board (PCB) used for measurement.

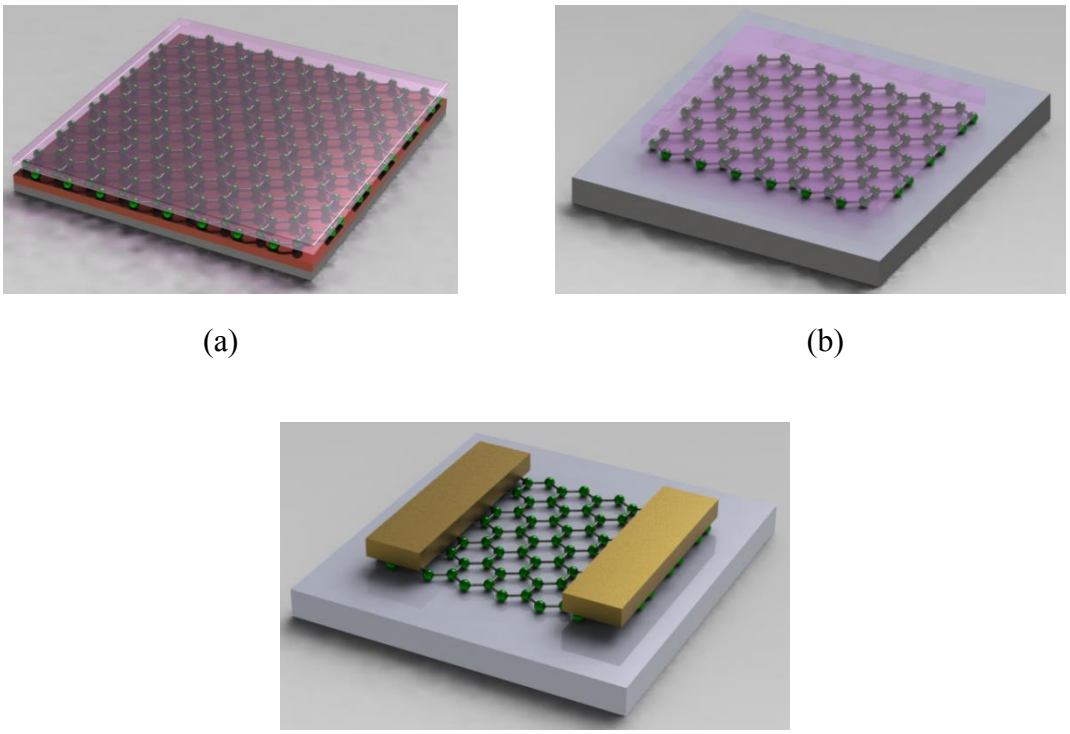
5.3. Graphene Gas Sensor on Silicon Oxide Substrate

Four-probe graphene devices on Si/SiO_2 substrate were used to investigate the sensitivity of graphene as exposed to NH_3 and NO_2.

5.3.1. Fabrication

Graphene samples were synthesized by chemical vapor deposition (CVD) on copper film [73]. The CVD graphene was transferred to a Si/SiO_2 substrate via a conventional PMMA-supported wet-transfer process using ammonia persulfate copper etchant [32, 74]. A 300-nm thick thermally grown silicon dioxide on silicon is chosen as the substrate to facilitate the visibility of graphene on top of the substrate. The graphene channel on Si/SiO_2 substrate is patterned using electron beam lithography (EBL) and etched using a low-power oxygen plasma reactive-ion-etch (RIE). Next, electron beam lithography followed by e-beam evaporation was used to pattern four Cr/Au (5nm/45nm) contacts across the graphene channel. The device has a channel width of 10 μm and

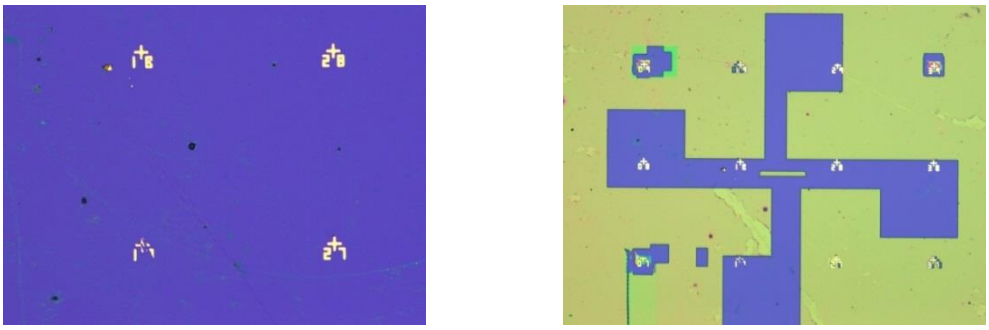
channel length of 25 μm. The fabrication process steps are shown in Figure 5.3. Optical microscope images of a fabricated sample after each processing step are shown in Figure 5.4.



(a) (b)

(c)

Figure 5.3: Illustration of the fabrication steps of graphene NH_3 gas sensor (Figure courtesy of Milo Holt).



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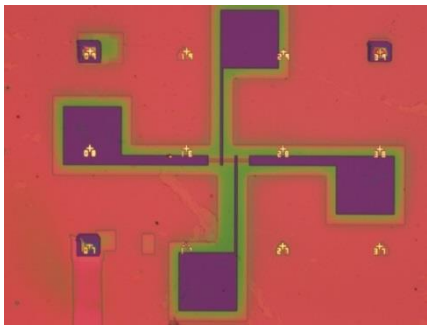

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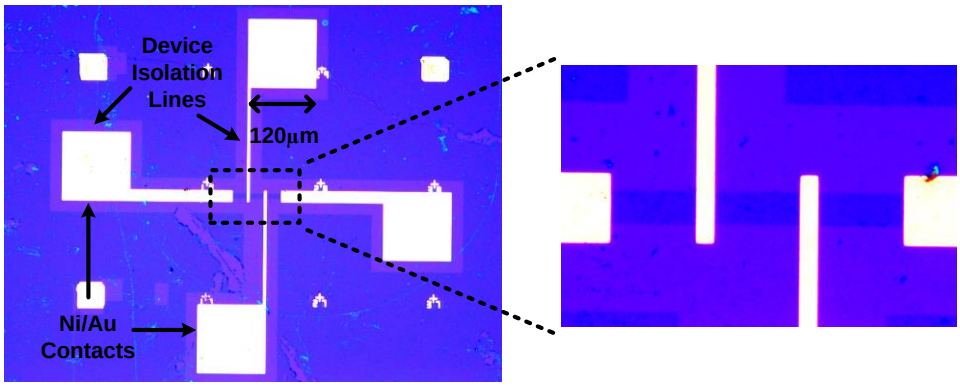


(d)

Figure 5.4: Optical microscope images of graphene gas sensor, (a) After graphene transfer, (b) After graphene etch, (c) After ebeam lithography to deposit metal, (d) After lift-off.

Raman spectroscopy was employed using Nd:YAG laser (532 nm wavelength) under ambient conditions in order to study the effect of doping on 2D to G ratio of graphene. Pristine graphene has Raman signatures at 1580 cm^{-1}, G peak, and 2690 cm^{-1}, 2D peak [75]. The 2D peak is single and symmetric for mono-layer graphene, but it becomes more asymmetric as the thickness of graphene increases [76]. Consequently, the 2D peak is a significant indicator of mono-layer graphene. The Raman spectroscopy results of our devices indicate that the graphene is mono-layer in all of our devices. Raman spectroscopy employed on the graphene sensor is demonstrated in Figure 5.5.

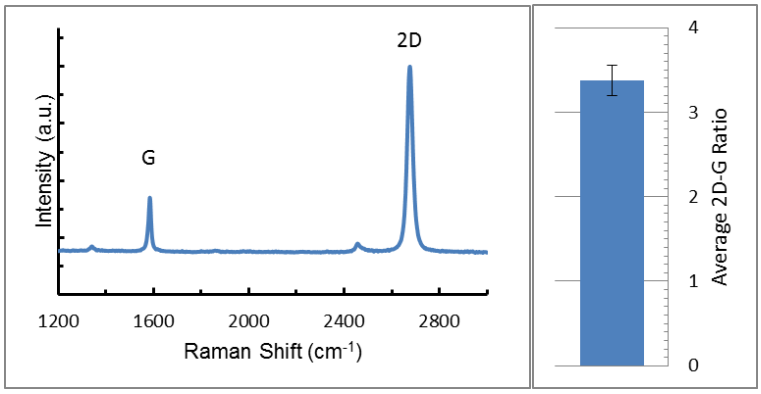
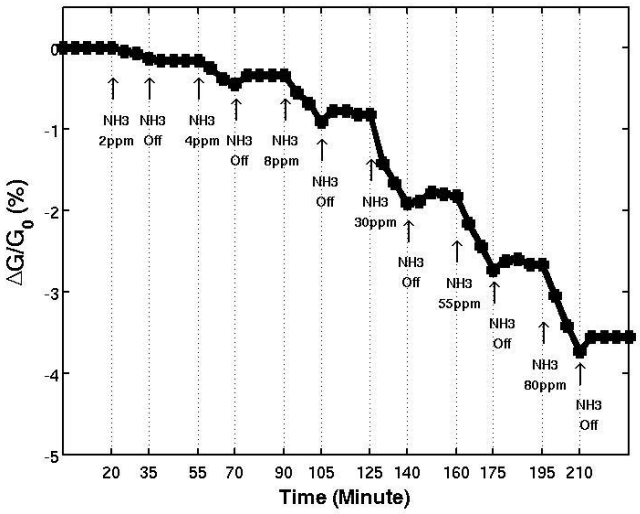


Figure 5.5: Raman spectroscopy result of graphene device on Si/SiO_2 substrate.

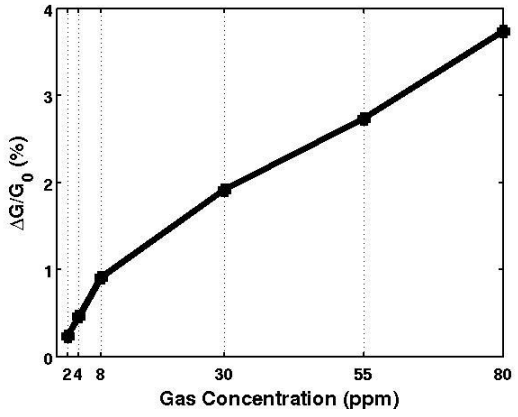
5.3.2. Measurement of Graphene Sensor on Si/SiO_2 Substrate

The gas molecules were detected by measuring the changes in electrical resistance of graphene as exposed to gas. Figure 5.6 and Table 5.1 show the sensor response of CVD graphene as exposed to various concentrations of NH_3. In this work, graphene was exposed to a range of NH_3, from 2 ppm to 80 ppm. The change of conductance

normalized by the initial conductance, defined as the sensitivity, was recorded in real-time using a Labview data acquisition system. The four-terminal graphene devices were characterized using HP-4156A semiconductor parameter analyzer. All tests were carried out at atmospheric pressure and room temperature.



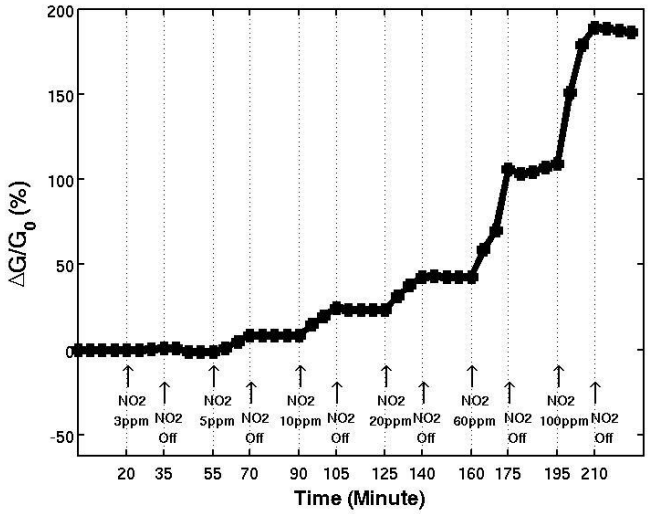
(a)



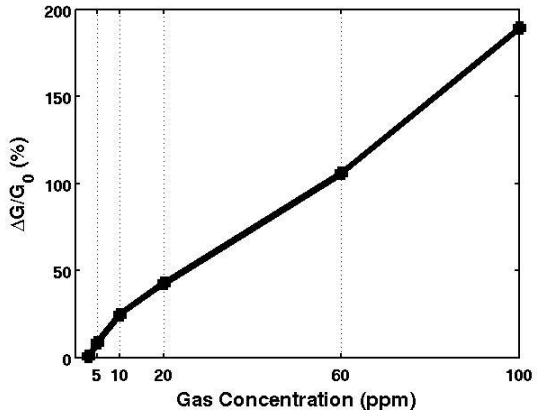
(b)

Figure 5.6: (a) Sensor response of CVD graphene to NH_3, (b) Sensitivity versus concentration.

Figure 5.7 and Table 5.2 show the sensitivity of CVD graphene as exposed to various concentrations of NO_2, from 3 ppm to 100 ppm.



(a)



(b)

Figure 5.7: (a) Sensor response of CVD graphene to NO_2, (b) Sensitivity versus concentration.

CVD Graphene Sensitivity (%)	2 ppm	4 ppm	8 ppm	30 ppm	55 ppm	80 ppm
NH_3	0.24	0.46	0.91	1.91	2.73	3.74

Table 5.1: Graphene sensor response to various concentrations of NH_3.

CVD Graphene Sensitivity (%)	3 ppm	5 ppm	10 ppm	20 ppm	60 ppm	100 ppm
NO_2	0.80	8.67	24.74	42.76	105.82	189.17

Table 5.2: Graphene sensor response to various concentrations of NO_2.

As demonstrated in the measurements and proved in literature (ref), conductance of graphene decreases as exposed to NH_3 and increases as exposed to NO_2. Also, graphene is very sensitive as exposed to NO_2 while it is just slightly sensitive to NH_3. In next section, measurement results of the graphene integrated gas sensor are presented.

5.4. GRAPHENE INTEGRATED GAS SENSOR

The measurement setup used to characterize the graphene integrated gas sensor was presented previously in this chapter. Also, a graphene device on Si/SiO_2 substrate, named test device, was designed, fabricated, and measured in our sensor chamber. This section presents the measurement results of graphene integrated gas sensors.

5.4.1. Yield of Post-CMOS Processing

The first step after completion of post-CMOS processing is to figure out the yield of the post-CMOS assembly process. A successful assembly process includes the presence of continuous layer of graphene in predefined locations that establishes connection with the underlying CMOS readout circuit. The yield of the full process flow is mainly determined by yield of the graphene transfer process and lift off. We observed that the yield of graphene transfer on CMOS chip is lower than the yield of graphene transfer on SiO_2 substrate. The main reason is that a continuous layer of graphene is required to be present at predefined locations of the CMOS chip. However, the selection of continuous area of graphene is allowed in the case of graphene devices on Si/SiO_2 substrate. The other reason is the rough and non-planar surface of CMOS chip which creates tears in graphene after dissolving of PMMA in the last step of graphene transfer (Figure 4.11). Figure 4.1 illustrates the non-planar surface of CMOS chip surface. As shown in Figure 5.8, the measured topography of the metal pad of the CMOS chip shows a 50nm roughness.

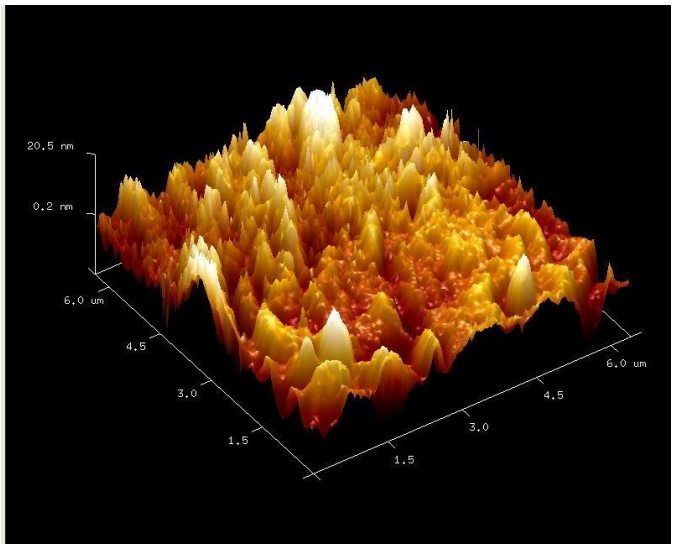


Figure 5.8: AFM monograph for height profile of CMOS die surface in the planar part.

Mono-layer graphene is invisible on top of the CMOS chip and other techniques such as characterizing the resistance of graphene interconnect or Raman spectroscopy were employed to verify the existence of graphene in predefined locations.

5.4.1.1. Characterizing Resistance of Graphene

As shown in Figure 4.7, a gate at top most metal layer is designed under the location of graphene to improve the topography of the surface and yield of graphene transfer. Table 5.3 compares graphene transfer yield of gated and non-gated graphene interconnects on CMOS chip, as well as graphene channel on Si/SiO_2 substrate.

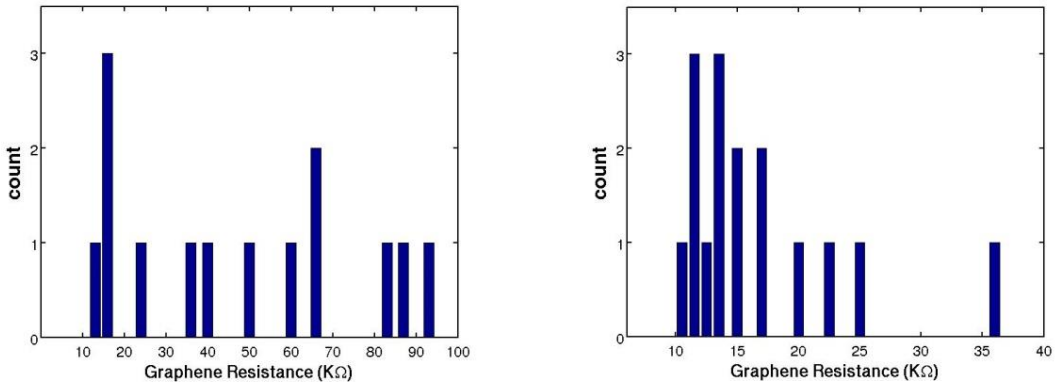
The resistance of each graphene interconnect was measured by probing the pads across that interconnect and characterized using B1500 semiconductor device parameter analyzer. Figure 5.9 illustrates the resistance of gated and non-gated graphene on CMOS

chip, along with graphene on Si/SiO_2 substrate. It is obvious that the yield and graphene resistance on Si/SiO_2 substrate is better than CMOS.

	Graphene on Si/SiO_2 Substrate	Gated Graphene on CMOS Chip	Non-gated Graphene on CMOS Chip
Yield	75%	52%	33%

Table 5.3: Yield of graphene transfer and lift off

Measuring the resistance of graphene by probing only proves continuity of graphene across the interconnect line; however, electrical connection of graphene to the underlying CMOS transistors is validated by measuring the oscillation frequency of the graphene integrated sensor (section 5.4.3).



(a) (b)

Figure 5.9: Resistance of graphene on (a) CMOS chip, (b) SiO_2 substrate.

5.4.1.2. Raman Spectroscopy

Raman spectroscopy was employed using Nd:YAG laser (532 nm wavelength) under ambient conditions. The Raman spectroscopy results of our devices indicate that the graphene is mono-layer in all of graphene interconnects. Figure 5.11 illustrates the Raman spectroscopy of graphene on CMOS chip. A line Raman spectroscopy was employed on a graphene interconnect along the line shown in Figure 5.10. Raman spectroscopy of three points (Figure 5.10) were shown in Figure 5.11(a) which indicates existence of graphene in area of interest. To prove the continuity of graphene interconnect, 2D values are illustrated in Figure 5.11(b).

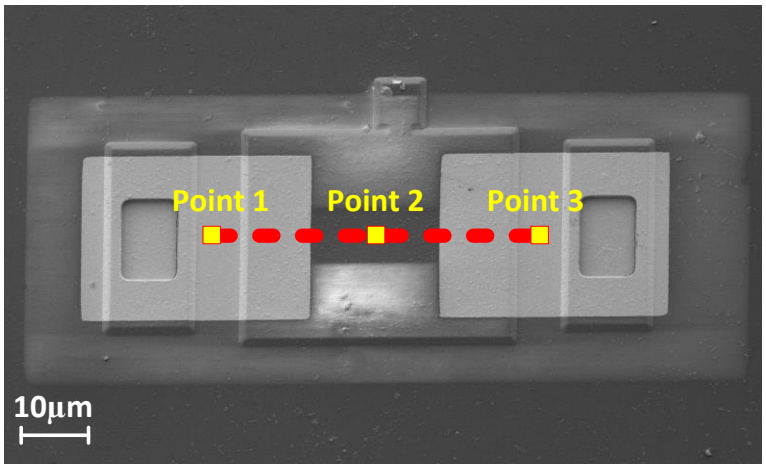
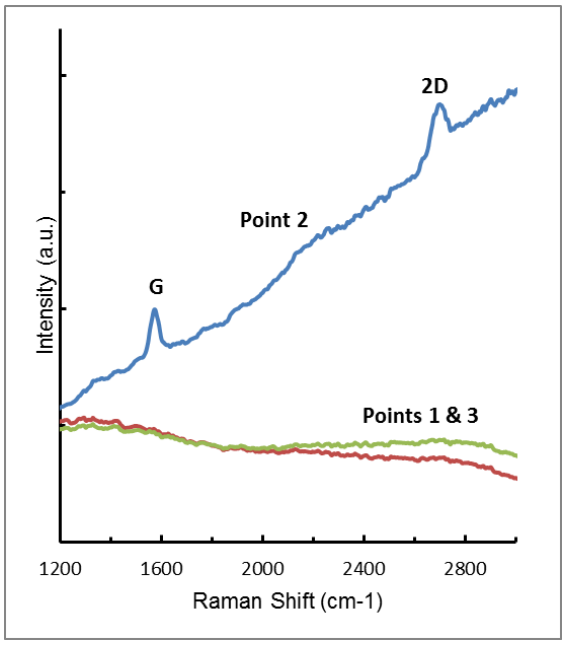
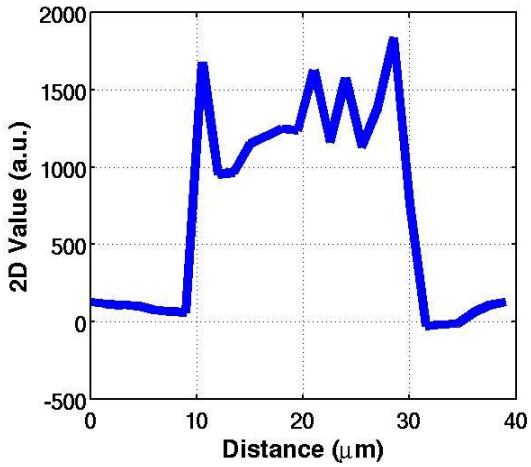


Figure 5.10: SEM image of the area to show the line along which Raman spectroscopy is employed.



(a)



(b)

Figure 5.11: (a) Raman spectroscopy results for three points along the line, (b) Profile of area under 2D peak of graphene along the line.

5.4.2. Measurement of CMOS-Only and Nickle-CMOS Test Structures

So far, we proved the continuity of graphene interconnects on the CMOS chip. However, two more steps are required to ascertain the functionality of the integration. First, a CMOS-only readout circuit was designed and used to verify the functionality of CMOS readout circuit. The readout circuit of CMOS-only and graphene integrated CMOS sensor are exactly the same. The only difference is that the missing graphene interconnect is replaced by M6 in CMOS-only readout circuit. Second, the integration fabrication recipe was verified by replacing graphene interconnect with Nickle. In the second tapeout TSMC foundry performed via hole etching through passivation layer. It was critical to ensure that electrical connections could be established properly through these via holes.

During these measurements, the CMOS chip which is a 16-pin die fabricated in standard 0.18μm CMOS technology is placed in a 44 pin PLCC chip carrier. The chip carrier was placed in an electrical socket on a printed circuit board (PCB) shown in Figure 5.2. Figure 5.12 shows the test setup used for characterizing CMOS-only and Nickle-CMOS readout circuits. The signal generator provides the supply voltage for the CMOS chip and the oscilloscope measures the frequency of output signal. Figure 5.13(a) shows the micrograph of the CMOS chip after completion of the post-CMOS process to integrate Nickle with CMOS. Figure 5.13(b) illustrates the output frequency versus supply voltage for Nickle-CMOS readout circuits for RO1, RO1S, RO2, and RO2S sensor structures. The increase of output frequency with increasing supply voltage demonstrates that CMOS circuit of all four sensor structures are functional and integration recipe can establish electrical connection between Ni interconnects and underlying CMOS circuit.

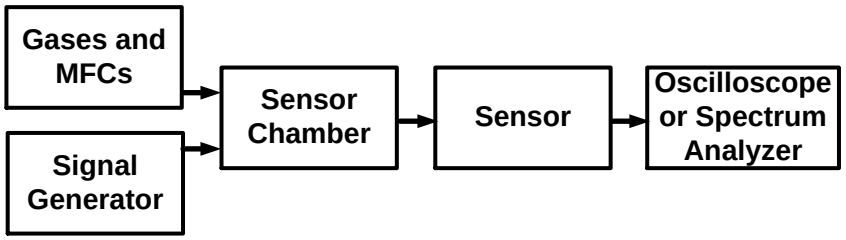
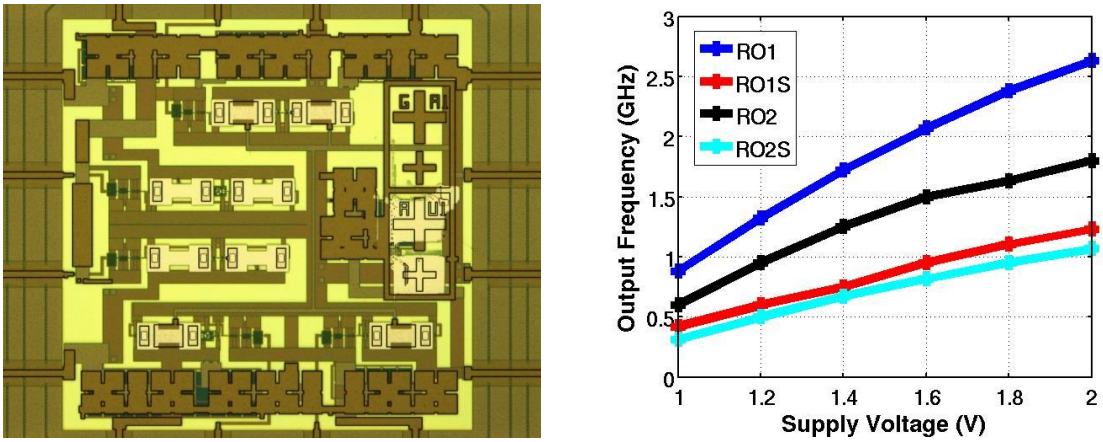


Figure 5.12: Test setup for characterizing CMOS test structure



(a) (b)

Figure 5.13: (a) CMOS micrograph after Ni/CMOS integration, (b) Measured oscillation frequency of the test structures.

5.4.3. Measurement of Graphene Integrated Gas Sensor

The probe pads of the graphene integrated gas sensor were wire bonded to the leads of a chip carrier using west-bond 7476D. The PLCC chip carrier was placed in an electrical socket on a PCB (Figure 5.2), making it possible to electrically address the graphene device. The PCB board was placed inside a sensor chamber with electrical feed-through to perform the measurement. Figure 5.1 shows the test setup used for characterizing graphene integrated gas sensor.

Figure 5.14 shows the graphene integrated gas sensor transfer response as exposed to various concentrations of NO_2, 3ppm to 100ppm for different supply voltages. As illustrated in Figure 5.14, the frequency change goes as high as 250MHz. For RO1S and RO2S, the frequency change increases as supply voltage increases. In the case of RO1 and RO2 the trend is different. All measured transfer functions are consistent with the simulation results.

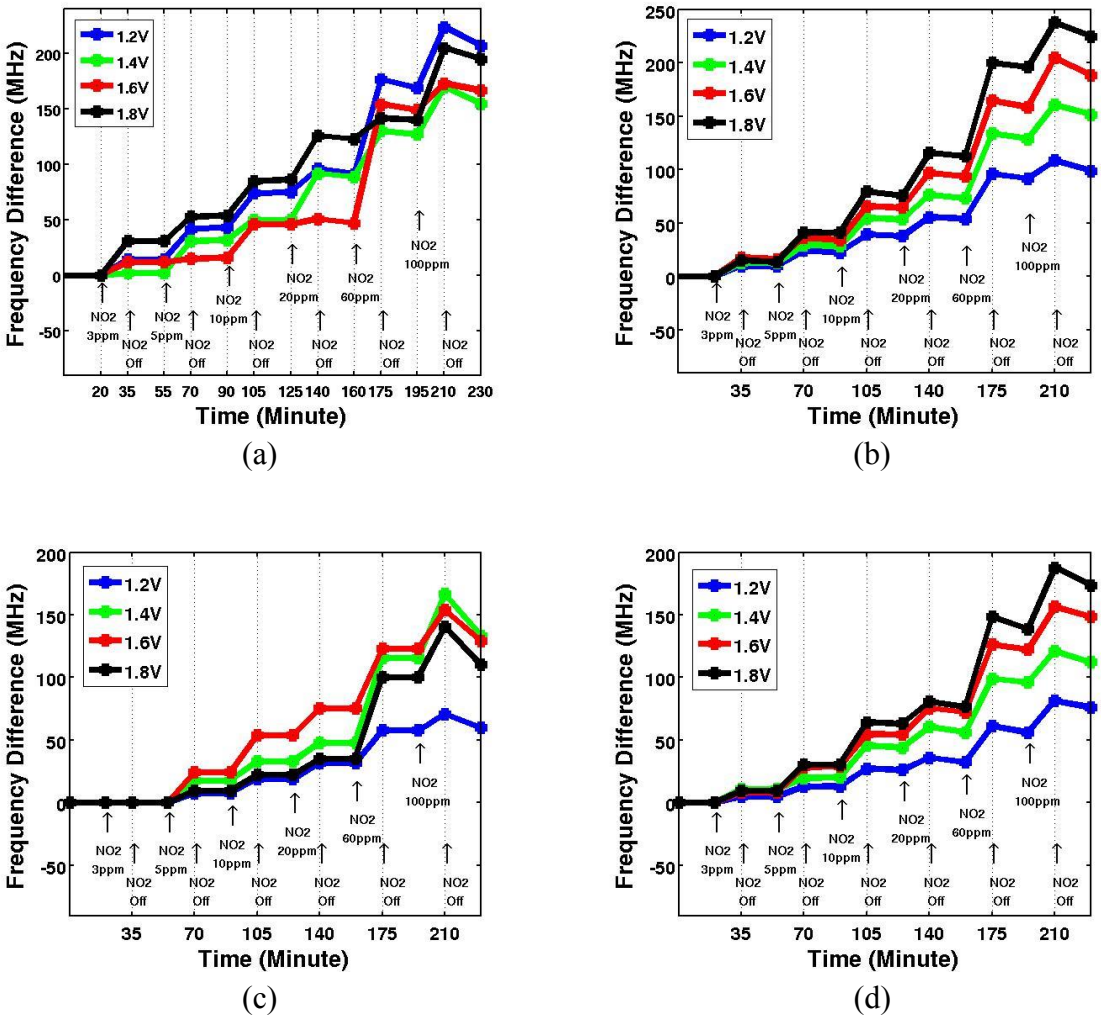
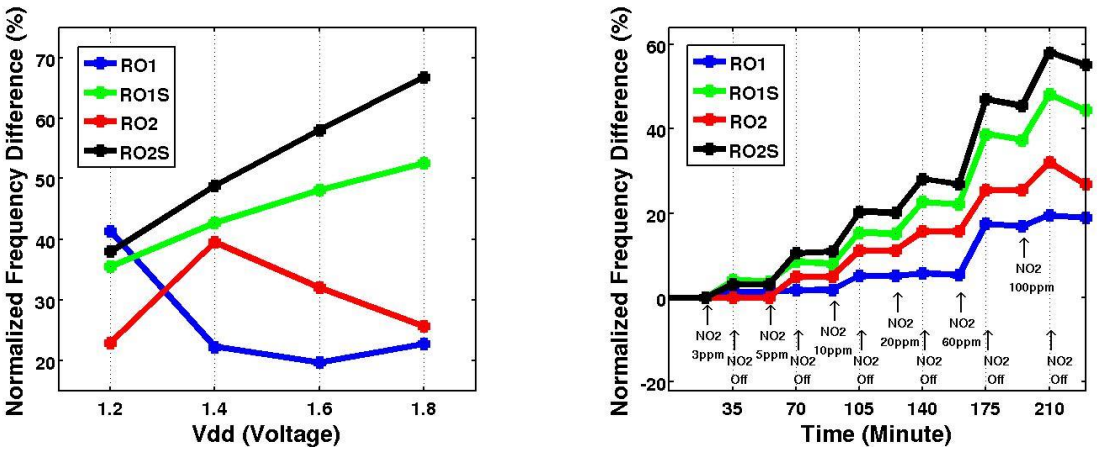


Figure 5.14: Sensor transfer function of (a) RO1, (b) RO1S, (c) RO2, (d) RO2S

Figure 5.15(a) illustrates the sensor response of RO1, RO1S, RO2, and RO2S structures versus supply voltage for 100ppm of NO_2. Figure 5.15(b) shows the sensor response of the sensors versus time.



(a) (b)

Figure 5.15: Sensor response of RO1, RO1S, RO2, and RO2S (a) versus supply voltage, (b) versus time.

RO2S shows the highest sensitivity whereas RO1 shows the lowest sensitivity. Simulation results demonstrated that sensitivity of RO2 is higher than RO1S. However, measurement results showed otherwise. The main reason was that initial resistance of graphene in RO1S sensor was higher than the initial resistance of graphene in RO2 structure. The total value of graphene interconnect resistance consists of resistance of graphene and contact resistance between graphene and deposited metal. Graphene resistance changes upon exposure to NO_2 or NH_3; however, contact resistance is constant. Therefore, the sensitivity of total resistance to gas exposure is increased with larger ratio of graphene resistance to contact resistance. We maximized the area between graphene and deposited metal to minimize the contact resistance. Since contact resistance cannot

be minimized further, the sensitivity is improved by using longer graphene channels. The ratio of channel length to width of graphene interconnect in RO2 structure was 2 compared to 3 for the similar ratio for RO1S structure, which explains the higher sensitivity of RO1S structure compared to RO2. By using the measured values of graphene resistance in the simulations, we consistently found higher sensitivity of RO1S sensor compared to RO2 sensor.

Output voltage of RO1, RO1S, RO2, and RO2S structures before and after exposure to 100ppm of NO_2 is illustrated in Figure 5.16.

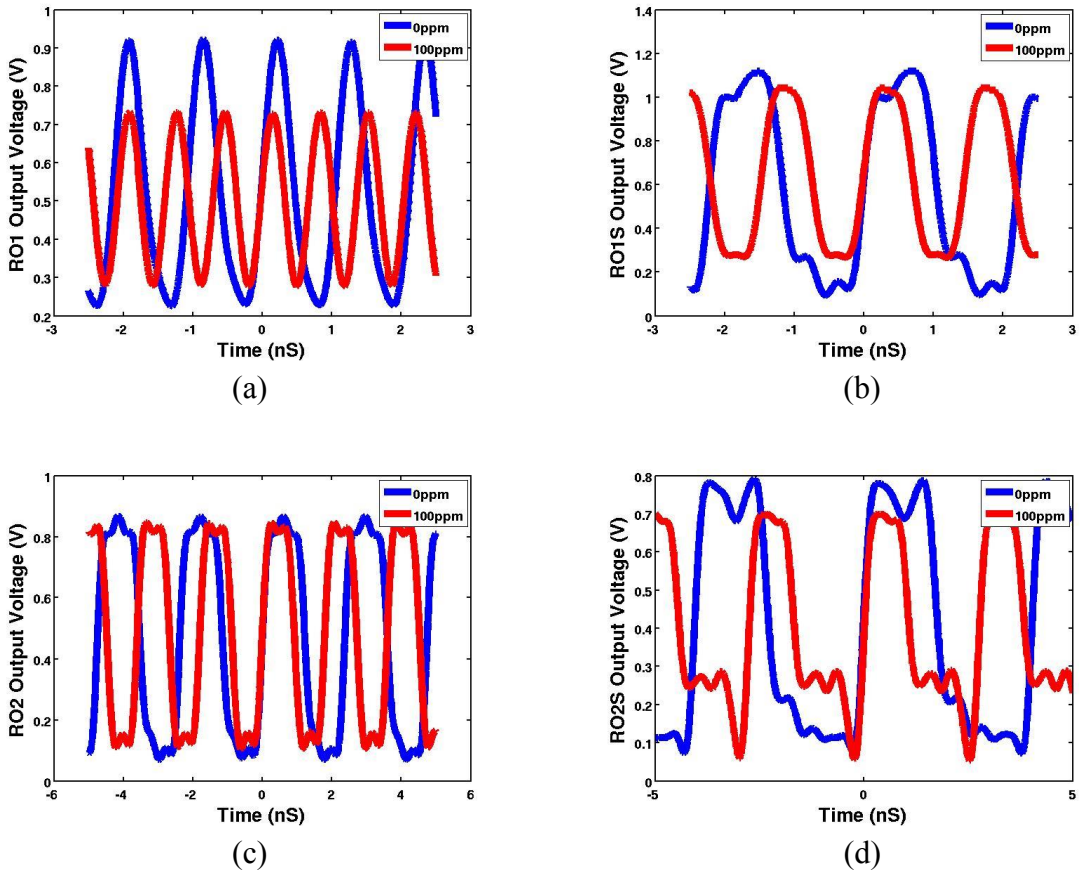


Figure 5.16: Output voltage before and after exposure to 100ppm (a) RO1, (b) RO1S, (c) RO2, (d) RO2S.

The spectrum for the phase noise of RO1S structure is demonstrated in Figure 5.17. As shown in the spectrum of the phase noise, the minimum detection level is 6MHz. All the four structures are capable of detecting 3ppm of NO_2 which changes the output frequency more than 6MHz.

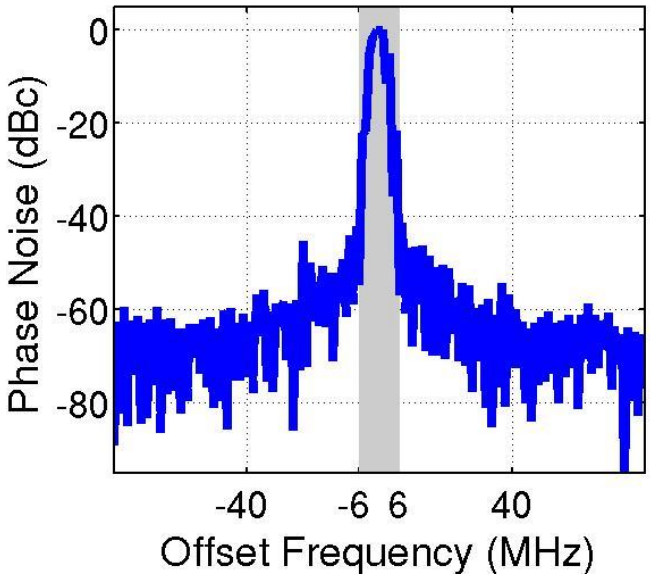


Figure 5.17: Output voltage before and after exposure to 100ppm (a) RO1, (b) RO1S, (c) RO2, (d) RO2S.

5.5. SUMMARY

In this chapter, the measurement setup to characterize the sensor response of the graphene integrated gas sensor was developed. Moreover, a four-terminal graphene device was designed, fabricated, and measured in the sensor chamber to certify the functionality of our measurement setup. The graphene device was also used to reproduce

the sensor response of graphene reported in literature to form a baseline for our graphene integrated gas sensor measurements.

The measurement results of graphene integrated gas sensor were presented in this chapter. The results show that sensing properties of graphene integrated with CMOS is promising. In general, this sensor benefits the advantages of graphene high sensitivity and CMOS technology together. The minimum NO_2 detection level of this sensor is 3ppm.

We observed that the sensitivity of graphene to NH_3 is relatively low. We investigated some methods to increase the sensitivity of graphene to NH_3 and proposed a method to do so. The method to enhance the sensitivity of graphene to NH_3 is presented in next chapter.

Chapter 6 : Sensitivity Enhancement of Graphene Gas Sensor

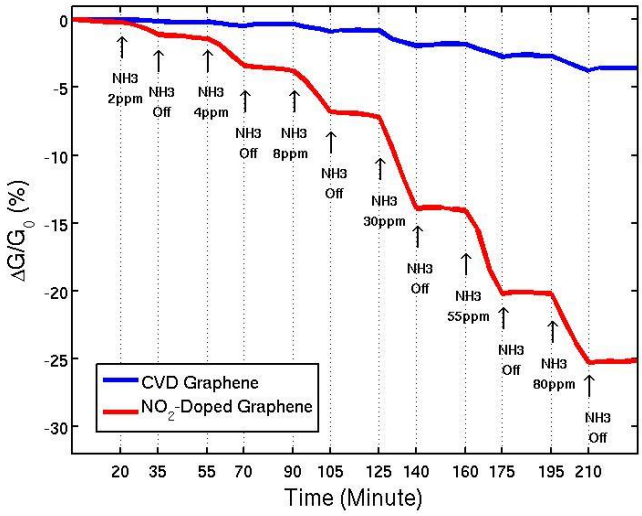
6.1. INTRODUCTION

The sensor responses of CVD graphene to NO_2 and NH_3 were illustrated in the previous chapter. Also, the sensitivity of the graphene integrated gas sensor to NO_2 was investigated. As demonstrated in our measurement and verified by literature, CVD graphene shows high sensitivity to NO_2 but the sensitivity of CVD graphene to NH_3 is relatively low [25, 33, 40]. In this chapter, a method to enhance the sensitivity of graphene to NH_3 is proposed.

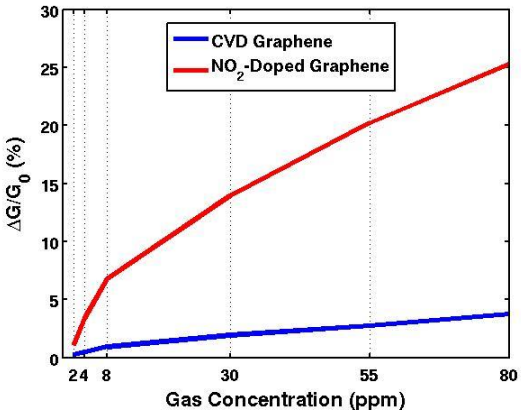
6.2. PROPOSED METHOD TO ENHANCE THE SENSITIVITY OF GRAPHENE

Four-probe graphene devices on Si/SiO_2 substrate were used to investigate the sensitivity of graphene as exposed to NH_3 and NO_2. The fabrication steps of the four-probe graphene devices are described in section 5.3. Details of measurement setup are covered in section 5.2.

Figure 6.1(a) (blue curve) shows the sensor response of CVD graphene as exposed to various concentrations of NH_3. In this measurement, graphene was exposed to a range of NH_3, from 2 ppm to 80 ppm. The sensitivity of graphene to NH_3 was recorded in real-time using a Labview data acquisition system. The graphene was then doped by NO_2, and sensor response was measured under the same conditions. Response of NO_2-doped graphene to various concentrations of NH_3 is depicted by the red curve in Figure 6.1(a). Figure 6.1(b) demonstrates the sensitivity of CVD and doped graphene with respect to NH_3 gas concentration.



(a)



(b)

Figure 6.1: (a) Sensor response of CVD graphene to NH_3. (b) Sensitivity versus concentration.

Table 6.1 compares the sensitivity of CVD and NO_2-doped graphene to different concentrations of NH_3. As shown in Figure 6.1, the sensitivity of CVD graphene is 3.7% for 80 ppm flow rate of NH_3 at room temperature and atmospheric pressure, comparable

to others' research [25, 31, 40]. The sensitivity of NO_2-doped graphene to 80 ppm of NH_3 is 25.3%, seven times (7x) greater than the sensitivity of CVD graphene to NH_3 alone. At lower concentrations of NH_3, the sensitivity is even greater: 8.5x at 4ppm and 11x at 2ppm. In general, it is observed that doping graphene by NO_2 significantly increases the sensitivity of graphene to NH_3. A saturation effect is observed as concentration of NH_3 gas increases for both CVD graphene and NO_2-doped graphene.

NH_3 Concentration	2 ppm	4 ppm	8 ppm	30 ppm	55 ppm	80 ppm
CVD Graphene Sensitivity (%)	0.1	0.4	0.9	1.9	2.7	3.7
NO_2-Doped Graphene Sensitivity (%)	1.1	3.4	6.8	13.9	20.2	25.3

Table 6.1: Sensitivity of CVD graphene and NO_2-doped graphene to NH_3.

6.3. INVESTIGATING CHARGE TRANSFER DOPING OF GRAPHENE

To investigate the charge-transfer doping of graphene, we fabricated three-terminal back-gated graphene field effect transistors (GFET). The fabrications process steps of the graphene field effect transistor are identical to the fabrication process steps of the four-probe graphene device. The only difference between the two devices is the resulting pattern of graphene and probe contacts. The block diagram of the three-terminal back-gated GFET is shown in Figure 6.2.

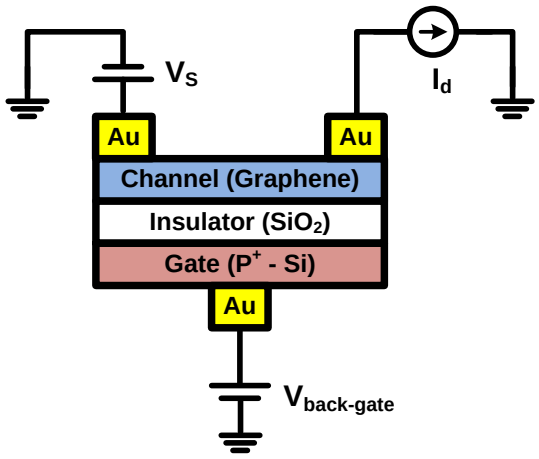
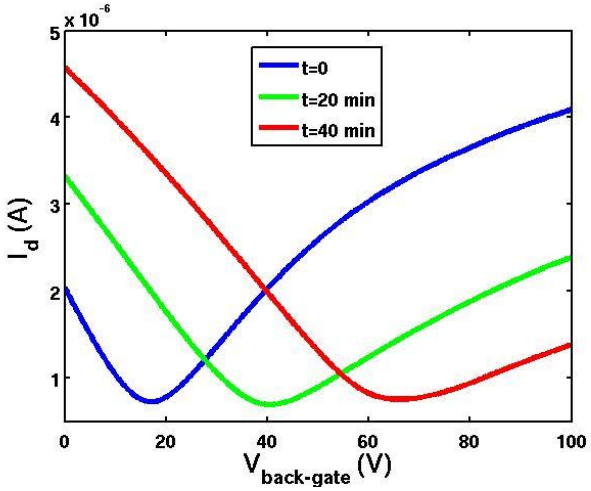


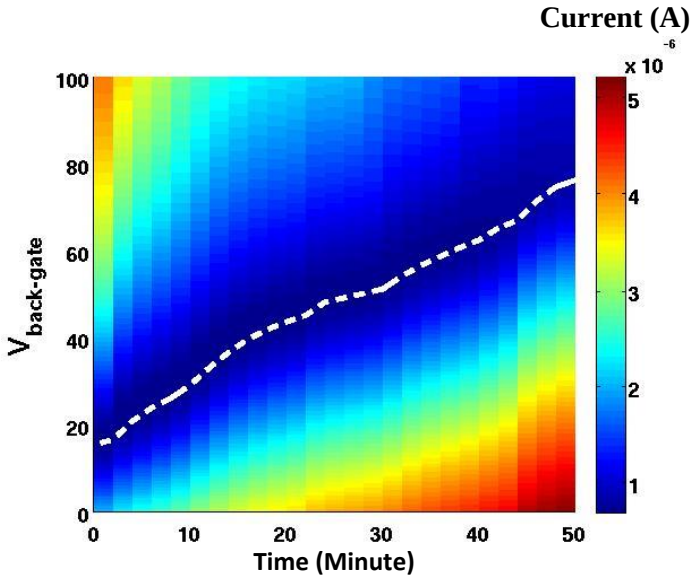
Figure 6.2: Block diagram of the three-terminal back-gated GFET.

HP-4156A semiconductor parameter analyzer was used to characterize the I-V curve of the transistor as shown by the blue curve in Figure 6.3(a). The I-V curve is measured by applying 0 to 100V at the back gate of the device, which is the back of the silicon substrate. V_{dirac} is 18V, meaning that the graphene is slightly p-type. The GFET is then doped with NO_2 and its I-V curve is measured during doping. To dope the graphene, the CVD graphene is exposed to 100 ppm of NO_2 gas at 500 Torr and room temperature for 50 minutes. By doping the graphene with NO_2, the graphene becomes further p-doped and V_{dirac} moves to the right (increases). Figure 6.3(a) also shows the I-V curve of the GFET after doping for 10 minutes (green curve) and 20 minutes (red curve). Figure 6.3(b) shows a 3D contour of current with respect to voltage over time. 'x' and 'y' axis show time and back-gate voltage, respectively, while the height of the contour shows current. The dashed line in the contour indicates how V_{dirac} changes over the course of time. As is shown in Figure 6.3(b), V_{dirac} increases as graphene becomes more doped. As dopoing continues, V_{dirac} becomes greater than 100V, beyond the limit of our

measurement setup. A simple extrapolation suggests that V_{dirac} was roughly 165V at the end of the doping process.



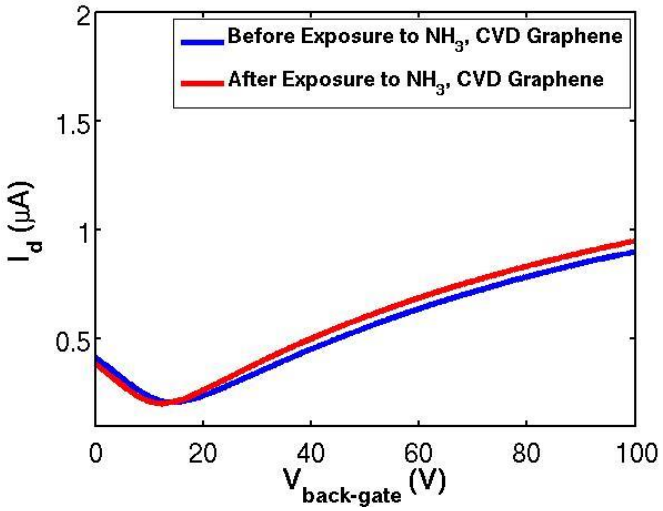
(a)



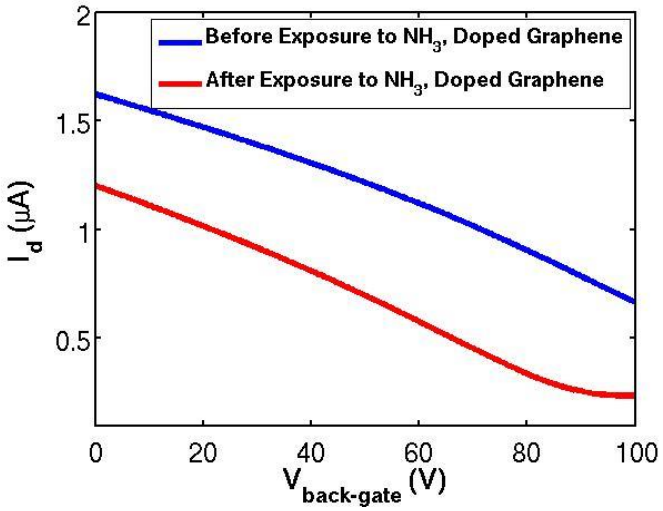
(b)

Figure 6.3: (a) I-V curve of GFET at different times during doping. (b) Contour plot of I-V curve during doping by NO_2, V_{dirac} is indicated by dashed line.

Figure 6.4(a) shows the I-V curve of CVD graphene before and after exposure to 100ppm of NH_3.



(a)



(b)

Figure 6.4: Comparison of I-V curve before/after exposure to NH_3 for (a) CVD graphene and (b) NO_2-doped graphene

Before exposure to NH_3, V_{dirac} of this sample was 15V, with a slight shift to 12.25V after exposure. The change in the I-V curve of CVD graphene before and after exposure to 100ppm of NH_3 is hardly noticeable. Figure 6.4(b) on the other hand, depicts the I-V curve of NO_2-doped graphene before and after exposure to 100ppm NH_3. V_{dirac} of the GFET is above 100V mainly because NO_2-doping shifts V_{dirac} to high voltages. The change in I-V curves before and after exposure is easily observable. Simple extrapolation of the I-V curve shows that V_{dirac} of NO_2-doped graphene was 144V before and 100V after exposure to 100ppm of NH_3.

6.4. Correlation between Doping Level and Sensitivity

To study the correlation between doping level and percentage increase in sensitivity, the GFETs were doped with different levels and the sensor response to NH_3 was measured. First, the GFET was doped until V_{dirac} reached 70V. Then, the GFET was doped further until V_{dirac} reached 165V. Figure 6.5 illustrates the sensor responses of the GFET for both cases. We observed that the increase in sensitivity improves as doping level increases.

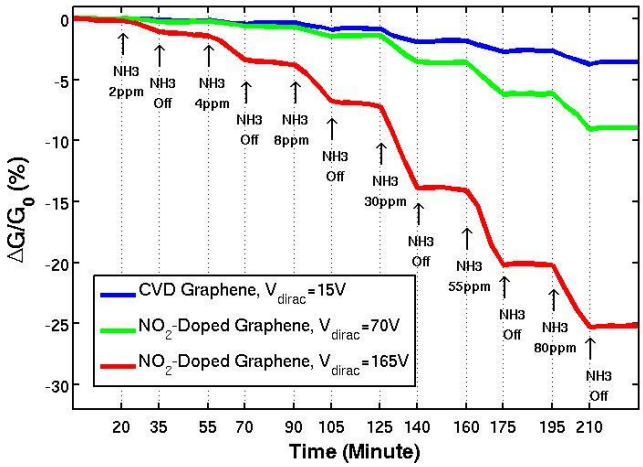


Figure 6.5: Sensitivity versus time for different doping levels.

6.5. RAMAN SPECTROSCOPY

Raman spectroscopy was employed using Nd:YAG laser (532 nm wavelength) under ambient conditions in order to study the effect of doping on 2D to G ratio of graphene. The Raman spectroscopy results of our devices indicate that the graphene is mono-layer in all of our devices. Crowther, et. al. performed an experimental study on charge-transfer doping of graphene by NO_2. They experimentally showed the 2D to G ratio of graphene decreases as the doping level of NO_2 on graphene increases [77]. The same result was observed for electrostatically doped graphene in gated devices [78-80] as well as chemically charge-transfer-doped graphene devices [81-84]. Our observation also shows the same result. Figure 6.6 illustrates the Raman spectroscopy of CVD graphene and NO_2-doped graphene. The 2D to G ratio of CVD graphene decreased from 3.425 to 1.815 after doping, which is 47% of the initial ratio.

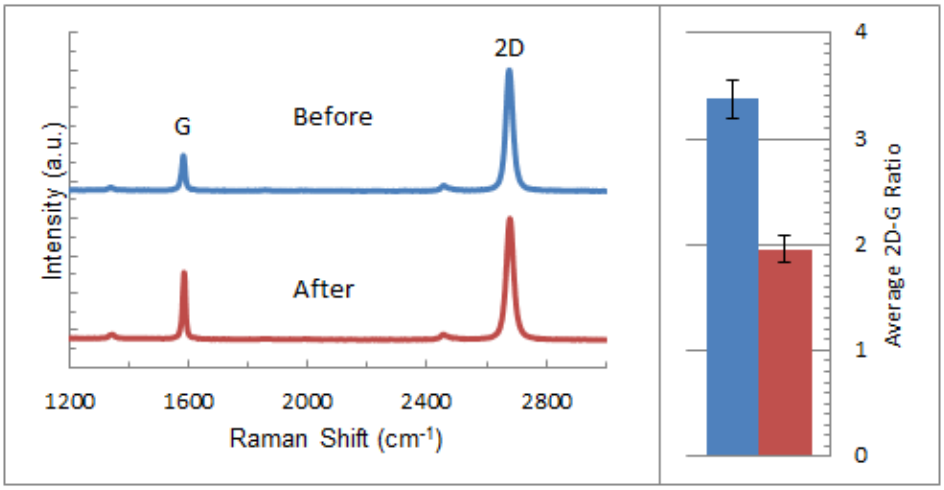


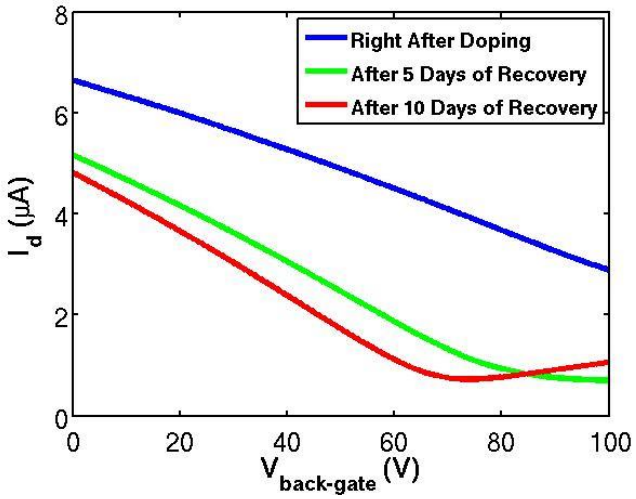
Figure 6.6: Raman spectroscopy results before and after doping.

6.6. STABILITY OF DOPING

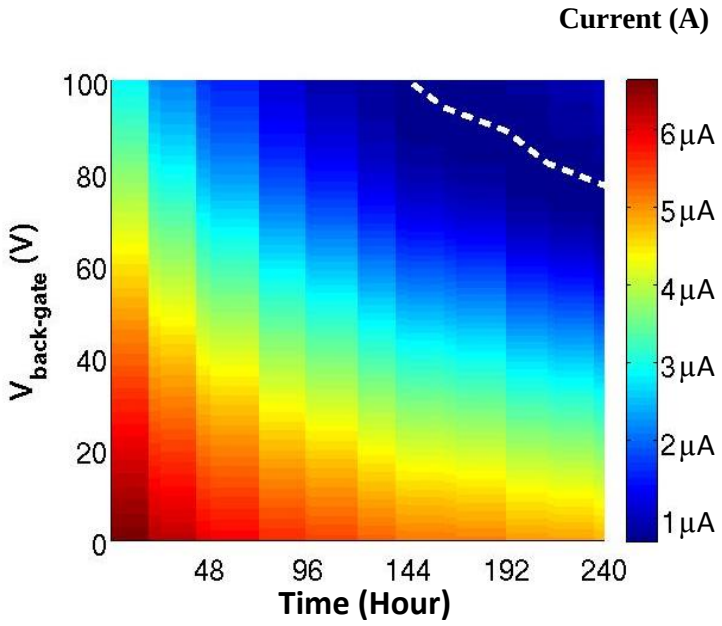
Stability of NO_2-doped graphene is another important concern addressed in this study. The graphene field effect transistor was exposed to 100 ppm of NO_2 for 50 minutes at 500 Torr, and the I-V curve of the NO_2-doped GFET was characterized immediately after doping. To characterize the I-V curve, voltage of 0 to 100V was applied at the back gate of the transistor and current of the transistor was measured. Then, the graphene transistor was kept in the same chamber for 10 days and I-V characterization was performed on the same sample once a day. The result is shown in the 3D contour of Figure 6.7. 'x' and 'y' axis show time and back-gate voltage, respectively, and the height of the contour shows current. We observed that V_{dirac} decreased as time increased. As shown in Figure 6.7, V_{dirac} decreased from 152V to 74V in 10 days, meaning that NO_2-doped graphene is not completely stable.

6.7. DISCUSSION ON DOPING

In general, we observed that doping graphene with NO_2 increases the sensitivity of graphene to NH_3. It is essential to understand the adsorption mechanism of NO_2 and NH_3 on graphene to analyze the increase in sensitivity. Adsorption is generally categorized as either physisorption or chemisorption, depending on the amount of energy transferred between adsorbate and surface, with physisorption being the less energetic of the two [57]. Theoretical predictions of NO_2 on pristine graphene indicate physisorption, while adsorption of NO_2 on defective or disordered graphene is chemisorption [43, 57, 85]. Moreover, chemisorption of NO_2 on defective graphene is more energetically favorable than physisorption of NO_2 on pristine graphene [43]. Consequently, we expect higher sensitivity to NO_2 for defective graphene.



(a)



(b)

Figure 6.7: (a) I-V curve of GFET at different times during recovery. (b) Contour plot of I-V curve during recovery in 10 days.

We argue that any CVD graphene synthesized on copper, to date, contains grain boundaries that provide reaction sites for adsorbents. Dimensions of grain boundaries are of the order of 0.5μm while the graphene device used in recent devices is in the order of a couple of micrometers. Consequently, graphene synthesized by CVD cannot be pristine graphene and is considered semi-defective (disordered). The abovementioned defect is completely different from structural defects generated by methods such as Ar plasma [41].

We assume that the adsorption mechanism of CVD graphene is chemisorption, which explains the high adsorption rate of NO_2 measured on the graphene samples as well as the tremendous change in V_{dirac} after exposing graphene to NO_2.

Regardless of the adsorption mechanism, previous studies show that adsorption of NO_2 on graphene makes the graphene device p-type [27, 33, 40, 86-88]. Our measurements confirmed the same; exposure to NO_2 shifted the V_{dirac} to the right, meaning that NO_2-doped graphene is a p-type graphene.

Several research groups performed theoretical studies to explore the adsorption energy of different molecules on graphene [43-46]. According to Zhang, et. al. the adsorption energy is defined as following [43]:

$$E_{ad} = E_{(moleule+graphene)} - E_{(graphene)} - E_{(moleule)} \quad (6.1)$$

where $E_{(molecule+graphene)}$, $E_{(graphene)}$, and $E_{(molecule)}$ are the energies of the molecule on the graphene device, graphene, and the molecule, respectively. The mentioned studies indicate that the sensitivity of graphene to a molecule improves as the adsorption energy of a reaction increases. Those studies also show that adsorption energy of graphene to NH_3 increases if graphene is doped by Boron or Aluminum, both of which are p-type

doping of graphene [43, 44]. Reference [43] shows that adsorption energy of NH_3 on B-doped graphene is five times more than adsorption energy of NH_3 on CVD graphene, whereas [44] shows that adsorption energy of NH_3 on B-doped and Al-doped graphene is 50 and 300 times more than that of CVD graphene respectively. As explained earlier, NO_2 also dopes the graphene to a p-type graphene device, very similar to Boron and Aluminum. While there is no theoretical study with direct calculation of adsorption energy of NH_3 on NO_2-doped graphene, our results are supported by existing theoretical work.

6.8. NO_2-DOPED GRAPHENE INTEGRATED GAS SENSOR: EXPOSURE TO NH_3

The proposed method to increase the sensitivity of graphene to NH_3 was applied to graphene integrated gas sensors. First, the graphene integrated gas sensor was doped by NO_2. To dope the graphene, the graphene integrated gas sensors were exposed to 100 ppm of NO_2 gas at 500 Torr and room temperature for 50 minutes. Then, the sensor response was measured. Details of measurement setup are covered in section 5.2. Figure 6.8(a) and Figure 6.8(b) illustrate the sensitivity of RO1S and RO2S readout circuits with NO_2-doped graphene transducers. As we were expecting, the frequency of oscillation decreased upon exposure to NH_3. As shown in Figure 6.1, the conductance (resistance) of graphene decreases (increases) when graphene is exposed to NH_3. Consequently, the output frequency decreases.

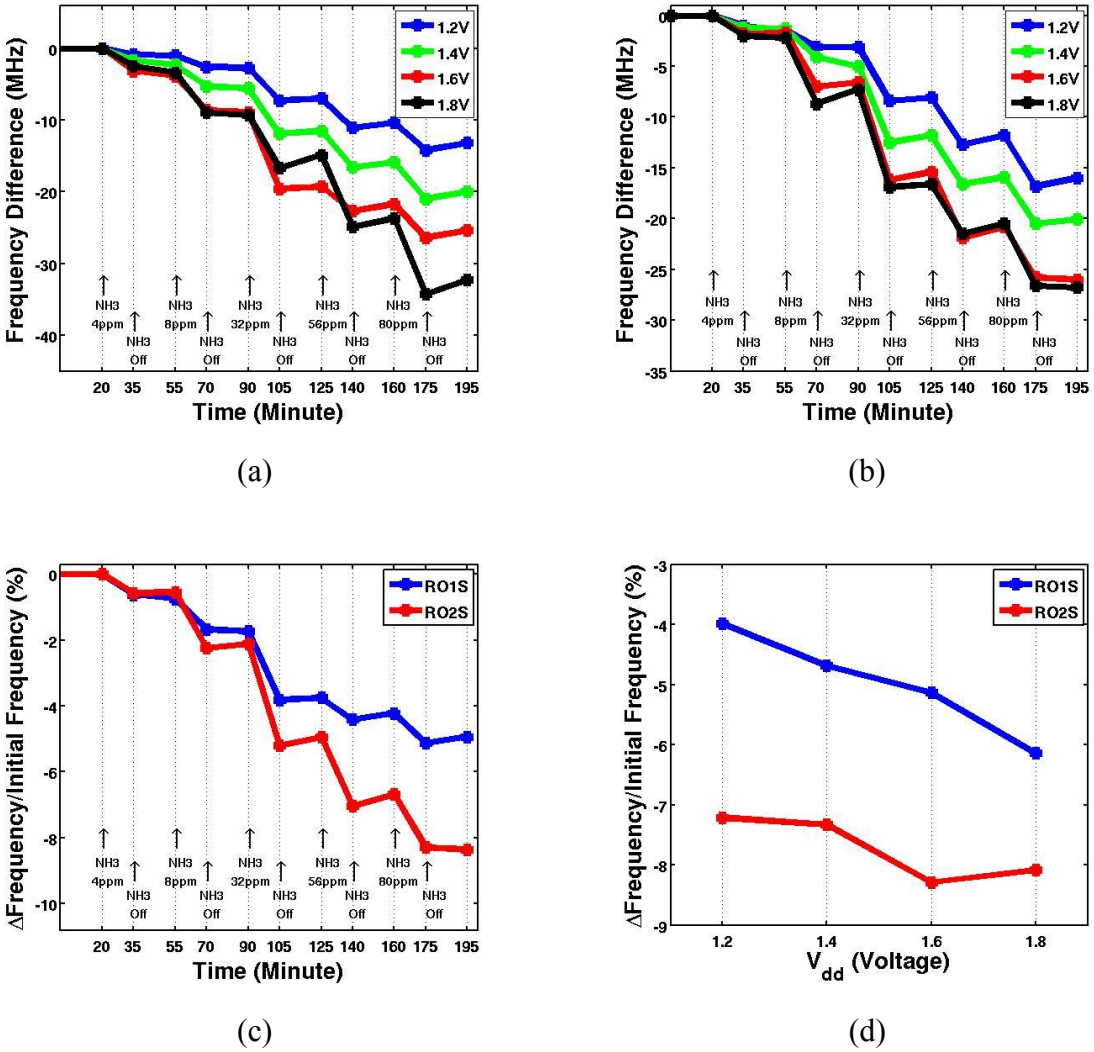


Figure 6.8: (a) Sensor transfer function of RO1S, (b) Sensor transfer function of RO2S, (c) Sensor response of RO1S and RO2S versus time, (d) Sensor response of RO1S and RO2S versus supply voltage

The measurement results show that the sensitivity of RO2S is higher than sensitivity of RO1S. Also, sensitivity increased as power supply increased. These results are confirmed by simulation results.

6.9. SUMMARY

In summary, we have demonstrated a novel method to increase the sensitivity of CVD graphene to NH_3. To improve the sensor response of CVD graphene to NH_3, CVD graphene was exposed to 100 ppm of NO_2 gas under 500 Torr at room temperature for 50 minutes. The measurement results show a 7x increase in sensitivity after doping. Measurements also demonstrated that an increase in sensitivity is directly correlated with doping level; sensitivity increases proportionally with doping. To study the doping process, I-V curves of three-terminal back-gated GFETs were characterized during the doping process. I-V characterization results show that graphene becomes increasingly p-type after doping, with V_{dirac} increasing beyond 100V, the limit of our measurement setup. Simple extrapolation of the I-V curve results in V_{dirac} of 165V. Raman spectroscopy employed on the doped sample revealed a decrease in the 2D – G ratio after doping. Lastly, the stability of NO_2 doping was studied by monitoring the desorption rate of NO_2-doped graphene. The I-V curve of NO_2-doped graphene was characterized directly after doping as well as once a day for a ten day period thereafter. While measurement results indicate that this doping method is not completely stable, this study nevertheless presents a new path to develop p-doped graphene, and promotes future research into different methods for stabilizing NO_2-doped graphene.

We also applied the sensitivity enhancement technique to graphene integrated gas sensors and measured the sensor response after NO_2-doping the graphene transducers. Although the sensitivity of graphene to NH_3 is low, this sensor shows about 30MHz of

change in output frequency. Since the output frequency is less susceptible to amplitude-affecting non idealities of the measurement path, 30MHz will be easily captured which is one of the advantages of this sensor. Moreover, the sensor selectively detects NO_2 and NH_3. Figure 6.8 shows that the output frequency decreases as sensor is exposed to NH_3 whereas Figure 6.8 illustrates that output frequency increases as sensor is exposed to NO_2. Consequently, this configuration provides selectivity for the sensor as exposed to NH_3 or NO_2.

Chapter 7 : Summary and Future Work

7.1. SUMMARY

In this dissertation, we have demonstrated heterogeneous integration of monolayer graphene and silicon CMOS for gas sensing applications. This proof-of-concept prototype chip validates the feasibility of this integration and allows us to investigate the sensitivity of graphene/CMOS sensors to NO_2 and NH_3 gases. Graphene interconnects were assembled on top of the CMOS platform where they are ordered in series with other resistances of the ring oscillator. As gas molecules are adsorbed to the graphene surface, graphene is doped and its resistance changes. The presence of gas molecules is detected by reading frequency of the ring oscillator which varies by resistance of graphene. In this report, we also addressed challenges of assembling graphene on CMOS. In our first, we etched through the passivation layer, similar to previous CMOS integration reports, to connect graphene to CMOS platform. In our second tapeout, we optimized CMOS circuit design, CMOS layout, and fabrication techniques to achieve improved gas sensitivity and graphene/CMOS assembly yield.

We conducted measurements to investigate performance of graphene/CMOS gas sensors. To perform measurements, we assembled an environmentally controlled chamber with NH_3 and NO_2 gases and electrical feedthroughs. We also fabricated graphene/SiO_2/Si devices to reproduce reported sensitivities in literature as well as produce a baseline for assessing performance of graphene/CMOS gas sensors.

Another achievement of this dissertation is the development of a novel technique to enhance the sensitivity of CVD graphene to NH_3. CVD graphene was p-doped by exposing to 100 ppm of NO_2 gas under 500 Torr at room temperature for 50 minutes. The

measurement results show a 7 folds increase in sensitivity after doping. Measurements also demonstrated that an increase in sensitivity is directly correlated with doping level; sensitivity increases proportionally with doping. Furthermore, in depth investigation of stability and charge transfer properties of the doping technique is presented. While measurement results indicate that this doping method is not completely stable, this study nevertheless presents a new path to develop p-doped graphene, and promotes future research into different methods for stabilizing NO_2-doped graphene. Furthermore, we applied this technique to enhance sensitivity of graphene/CMOS sensors and obtained remarkable improvement in NH_3 sensitivity, taking another step toward viable graphene/CMOS sensors for industrial applications. The minimum detection level of the graphene integrated gas sensor is 3ppm for NO_2 and 8ppm for NH_3.

7.2. FUTURE WORK

The research presented in this dissertation paves the path toward progress in sensors based on 2D materials providing high sensitivity, low cost, and fast response. The future work spans the material, device, and circuit level ideas.

Selective detection of gases in an environment where more than one gas is present has not been covered in this research. The presented graphene integrated gas sensor is capable of selectively detecting NO_2 and NH_3 gases if only one of those gases is present in the environment. Current platform can be used with functionalized graphene, graphene decorated with nanoparticles, or other 2D materials to obtain selective detection. Also, electrical properties of graphene could be used to selectively detect NO_2 or NH_3 gases. For instance, Balandin demonstrated that selective detection of tetrohydrofuran, methanol, acetonitrile, or chloroform gases is possible by using low frequency noise of

graphene whereas electrical resistivity could quantitatively measure the concentration of these gases [89].

Graphene sensor can be recovered to its initial undoped state with annealing at 150°C [27]. This annealing temperature can be easily achieved by sending a large current through graphene channel [60, 61, 90]. The same technique could be used to desorb gas molecules form the surface of graphene after each gas exposure and reset the graphene to its original electrical condition. Adding such feature to the graphene integrated gas sensor will allow quick recovery which is essential for practical applications.

The demonstrated graphene/CMOS integration technique could potentially be used for integrating any other 2D material on top of a CMOS platform. Other 2D materials such as MoS_2 (molybdenum disulfide) [91, 92] can be explored in the search for even more sensitive practical gas sensors. Moreover, the integration technique could be used in other applications such as integrated graphene antenna, graphene/CMOS transceiver, and graphene/CMOS frequency doubler.

Although we demonstrated that the sensitivity of NO_2-doped CVD graphene to NH_3 is superior compared to as-fabricated CVD graphene by almost an order of magnitude, the mechanism of this improvement remains elusive. It is not clear whether NH_3 molecules are adsorbed to nearby NO_2 molecules or to the graphene surface. Theoretical simulations are necessary to find the adsorption sites for NH_3 molecules with lowest adsorption energy on NO_2-doped graphene. The results of this investigation can lead us toward dopants that allow us to design more sensitive graphene sensors.

The extremely high surface to volume ratio of graphene supported on a substrate can be further increased if graphene is suspended such that both surfaces are equally exposed to gas molecules. Compared to supported graphene, sensitivity could be doubled

in suspended structure. In the absence of trapped charges and impurities of the substrate, adsorption mechanism might be totally different. Similarly, the effect of dopants on sensitivity and the interaction between dopants and adsorbed gas molecules could be drastically influenced. These investigations not only address some fundamental questions on adsorption mechanisms, but also can provide clues to develop ultra-sensitive gas sensors for practical applications and research goals.

Appendix A : Phase Noise in Ring Oscillators

In this section, the phase noise of ring oscillators is explained [69]. As an example, consider a five-stage inverter chain ring oscillator shown in Figure A1.

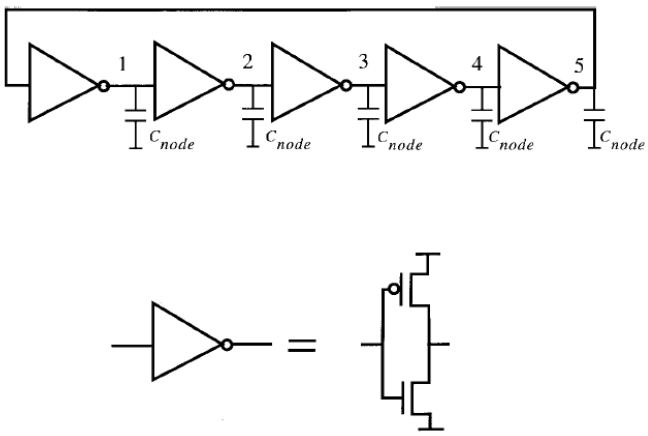


Figure A1: Five-stage inverter chain ring oscillator.

The output of this ring oscillator can be written as

$$V_{out} = A(t).f[\omega_0 t + \emptyset(t)] \tag{A.1}$$

where the function f is periodic with frequency f_0 ($\omega_0=2\pi f_0$) and $A(t)$ and $\emptyset(t)$ model fluctuations in amplitude and phase due to any internal or external noise source.

The phase noise of a single-ended CMOS ring oscillator is given by equation (A.2) [69]:

$$\mathcal{L}(\Delta f) \simeq \frac{8}{3\eta}\frac{kT}{P}\left(\frac{V_{DD}}{V_{char}}\right)\left(\frac{f_s}{\Delta f}\right)^2 \tag{A.2}$$

where η is the proportionality constant, k is the Boltzmann constant, T is the absolute temperature, P is the total power dissipation, V_{DD} is the supply voltage, V_{char} is the characteristic voltage of the device, and f_s is the output frequency of ring oscillator. η, P, f_s, and V_{char} are defined in equations (A.3) to (A.6)

$$\eta = t_D f'_{max} \tag{A.3}$$

$$P = 2\eta N V_{DD} q_{max} f_s \tag{A.4}$$

$$V_{char} = \Delta V / \gamma \tag{A.5}$$

$$f_s = \frac{1}{2Nt_D} \simeq \frac{\mu_{eff} W_{eff} C_{ox} \Delta V^2}{8\eta N L q_{max}} \tag{A.6}$$

where t_D is delay of each inverter, f'_{max} is the maximum slope of the waveform f in equation (A.1), N is the number of inverters, q_{max} is the maximum charge (in coulombs) on node 5, ΔV is gate overdrive voltage in the middle of transition, γ is the thermal noise parameter of MOS and MOS transistors, μ_{eff} is the mobility, W_{eff} and L are the effective channel width and length of the transistor, and C_{ox} is the gate-oxide capacitance per unit area. q_{max} and ΔV are defined as:

$$q_{max} = V_{swing} \times C_{node} \tag{A.7}$$

$$\Delta V = (V_{DD}/2) - V_T \tag{A.8}$$

where V_T is the threshold voltage of NMOS and PMOS transistors, C_{node} is the effective capacitance on node 5, V_{swing} is the voltage swing across the capacitor C_{node}.

By combing equations (A.2), (A.4), and (A.6) we get:

$$\mathcal{L}(\Delta f) \simeq \frac{1}{6}\left(\frac{1}{NV_{swing}}\right)^2 \left(\frac{kT}{V_{char}}\right)\left(\frac{\mu_{eff}W_{eff}C_{ox}\Delta V^2}{\eta^3 LC_{node}^2}\right)\left(\frac{1}{\Delta f}\right)^2 \tag{A.9}$$

Appendix B : Post-CMOS Processing Flow

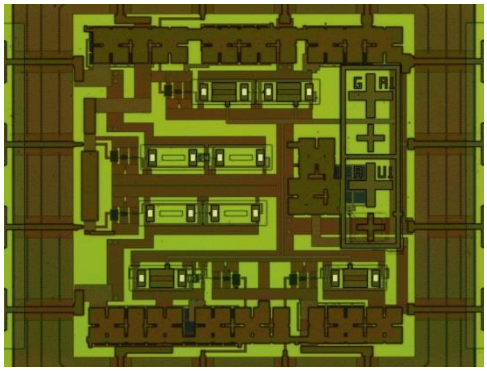
The details of post-CMOS process flow developed to integrate graphene and CMOS are described in this appendix.

Step	Details
1	Glue CMOS chip to the Si substrate (2cm x 3cm) for handling by placing a tiny droplet of epoxy close to one edge of the substrate
2	Clean CMOS chip glued on the Si substrate - Acetone rinse for 10min - IPA rinse for 2min - Blow dry with N_2 gun
3	Transfer CVD graphene to the top of CMOS chip (details explained in Table B2)
4	Spin-coat PMMA 996K 7% in chlorobenzene on the CMOS/Si substrate two times: - Step-1. Spin-rate : 0 rpm, Ramp-rate : 0 rpm/sec, Time : 5 sec - Step-2. Spin-rate : 6000 rpm, Ramp-rate : 2000 rpm/sec, Time : 60 sec - Bake on hotplate, 190°C, 4 minutes under beaker - Step-3. Spin-rate : 0 rpm, Ramp-rate : 0 rpm/sec, Time : 5 sec - Step-4. Spin-rate : 6000 rpm, Ramp-rate : 2000 rpm/sec, Time : 60 sec - Bake on hotplate, 190°C, 4 minutes under beaker
5*	Equipment : Carl Zeiss ebeam lithography tool - Electron beam lithography to pattern graphene - Develop by MIBK:IPA 1:3

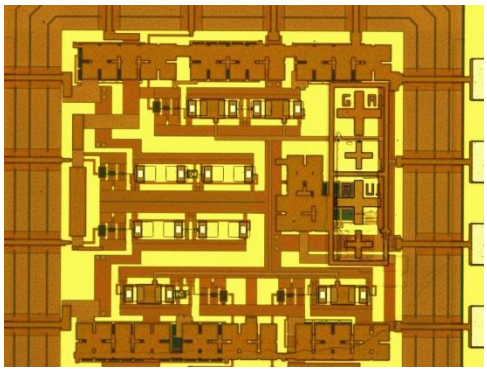
6	Equipment : Plasmatherm 790 To etch graphene (details explained in Table B2)
7	Spin-coat PMMA 996K 7% in chlorobenzene on the CMOS/Si substrate two times: - Step-1. Spin-rate : 0 rpm, Ramp-rate : 0 rpm/sec, Time : 5 sec - Step-2. Spin-rate : 6000 rpm, Ramp-rate : 2000 rpm/sec, Time : 60 sec - Bake on hotplate, 190°C, 4 minutes under beaker - Step-3. Spin-rate : 0 rpm, Ramp-rate : 0 rpm/sec, Time : 5 sec - Step-4. Spin-rate : 6000 rpm, Ramp-rate : 2000 rpm/sec, Time : 60 sec - Bake on hotplate, 190°C, 4 minutes under beaker
8*	Equipment : Carl Zeiss ebeam lithography tool - Electron beam lithography to deposit metal contacts - Develop by MIBK:IPA 1:3
9	Equipment : CHA1 Ti/Au (5nm/45nm) deposition using e-beam evaporation
10*	Liftoff of deposited metal films - Leave samples in Acetone overnight - Transfer the sample to the IPA beaker and wait for 1 min

Table B1: Post-CMOS process flow developed to integrate graphene and CMOS

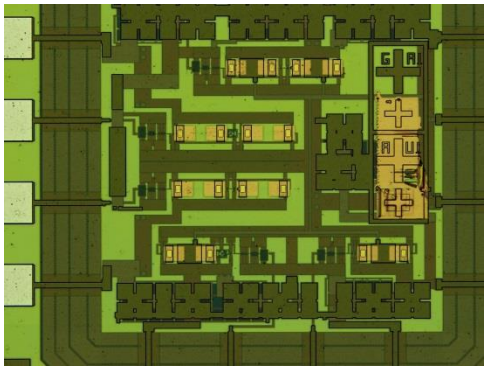
* Chip micrograph after this step is demonstrated in Figure B1



(a)



(b)



(c)

Figure B1: Chip micrograph (a) After step 5, (b) After step 8, (c) After step 10.

Step	Details
1	Chemical Vapor Deposition of Graphene using Cu foils
2	Attach Graphene/Cu foil samples on silicon carrier wafers
3	Spin-coat PMMA A4 on Graphene/Cu foil samples - Step-1. Spin-rate : 500 rpm, Ramp-rate : 1000 rpm/sec, Time : 5 sec - Step-2. Spin-rate : 4000 rpm, Ramp-rate : 2000 rpm/sec, Time : 40 sec - Step-3. Spin-rate : 0 rpm, Ramp-rate : 2000 rpm/sec, Time : 1 sec
4	Detach the spin-coated samples from silicon carrier wafers
5	Leave the samples in a desiccator overnight to remove residual solvents
6	Back-side graphene etching - Load the spin-coated samples upside-down in an RIE system - Oxygen plasma RIE for 1min to remove back-side graphene films (see Appendix A.3 for the details)
7	Cu wet-etch - Prepare clean, triple-rinsed beakers - Pour ammonia persulfate (APS-100) in each beaker - Float the sample in the beaker to etch supporting Cu - Wait for 2 hours to complete etching Cu foils
8	Rinse samples with deionized (DI) water - Prepare three triple-rinsed beakers - Transfer one sample to the first beaker and wait for 30 min. - Transfer the sample to the second beaker and wait for 5 min. - Transfer the sample to the last beaker and wait for 5 min.

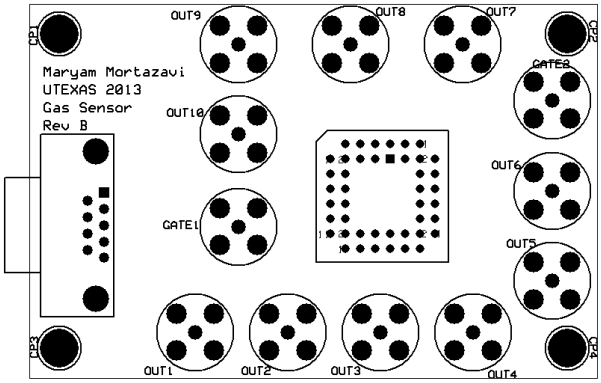
Table B2: Wet Transfer Process of Graphene Films (Courtesy of Jongho Lee)

Step	Details
1	Equipment : Plasmatherm 790 Place samples on a silicon carrier wafer Load samples with a carrier wafer at the center of the chamber
2	Pump (pressure : 100 mTorr, hold time : 10 sec)
3	Evacuation (pressure : 10 mTorr, hold time : 1 min)
4	Purge (pressure : 200 mTorr, hold time : 30 sec)
5	Evacuation (pressure : 10 mTorr, hold time : 30 sec)
6	Process step 1 O2 flow rate : 10 sccm, pressure : 200 mTorr no RF power applied, hold time : 1 min (fixed)
7	Process step 2 O2 flow rate : 10 sccm, pressure : 200 mTorr RF power : 50 W, hold time : 40 sec
8	Evacuation (pressure : 10 mTorr, hold time : 30 sec)
9	Purge (pressure : 200 mTorr, hold time : 30 sec)
10	Evacuation (pressure : 10 mTorr, hold time : 30 sec)

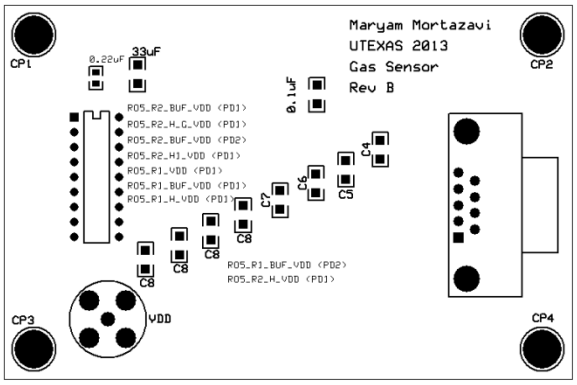
Table B3: Oxygen Plasma Reactive Ion Etch of Graphene Films (Courtesy of Jongho Lee)

Appendix C : Details on Layout of PCB Board

The following figures show the layout of the printed circuit boards (PCBs) designed for the measurement. Figure C1 (a) shows the layout of the PCB board used inside the chamber. During the measurement, the chip inside the chamber is not accessible and the PCB demonstrated in Figure C1 (b) was used to access and control each of the ring oscillators separately through the D-connector.



(a)



(b)

Figure C1: Layout of PCB boards (a) In the sensor chamber, (b) Out of the chamber.

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