THE HAWAII MUON BEAMLINE

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ACKNOWLEDGMENTS

At the time of this writing, the second generation Hawaii Muon Beamline has been an ongoing project at the IDlab for almost a year. It has required many disciplines in order to become realizable, including mechanical and electrical engineering for the electronics and structure, as well as Physics for the underlying theory of operation. I would like to thank all of those who have spent their time and dedication on the help with this particle detector, without you, we wouldn't have been able to complete this endeavor as efficiently as we did.

First of all, I would like to thank my advisor Prof. Gary Varner for his help and dedication for this project as well as giving me the opportunity to embark this journey. Khanh Le for the hard work and dedication for the design and implementation of the mechanical, electrical and programing portions of the scintillator planes. Roy Tom for being extremely helpful with the mechanical build of HMB, as well as mechanical student helpers ZJ Lin and Marrissa Kuwabara. Nathan Park and Cameron Asaoka for the help with many miscellaneous tasks related to HMB. Finally I would like to thank everyone else in IDLab for your support and help throughout the years, including Matt Andrew, Julien Cercillieux, Bronson Edralin, Peter Orel, Andrej Seljak, Chris Ketter, and Harley Cumming. I feel very proud to have worked with all of you and will never forget the experience.

ABSTRACT

High Energy Physics (HEP) instrumentation development programs often require extensive tests of experimental equipment such as silicon pixel detectors, single photon sensitive detectors for Cherenkov radiation, particle time of flight systems, etc. These tests are usually conducted at accelerator research facilities where available beam-time is not only limited, but also expensive. The Hawaii Muon Beamline (HMB) will use cosmic-ray generated muons to enable performance evaluations of such devices under test. HMB is a beam telescope constructed out of four position sensitive tracking detectors and a calorimeter system for measurement redundancy. Position tracking detectors are built using an array of geiger-mode avalanche photodiodes, also known as Multi-pixel Photon Counter (MPPCs), coupled to square Polyvinyl Toluene (PVT) scintillator blocks. The MPPCs are positioned orthogonally along the block edges. Charged particles traveling through a scintillation block emit detectable amounts of light. The analog output pulses from the MPPCs trigger the TARGETX waveform digitizing ASIC which samples at 1 Giga Sample per second (GSPS). From the pulse amplitudes, being proportional to the amount of light, the charged particle penetration position can be estimated in a 2D plane. To construct the HMB, each pair of tracking detectors need to be placed vertically, one on top of the other, providing the entrance and exit position of the beam. In between both pairs, space is made available for a device under test. In addition, a separate calorimeter system composed of four rectangular blocks of Sodium Iodide (NaI) crystals coupled to photomultiplier tubes (PMT) is placed below and off-axis of the lower pair tracking system. This calorimeter system is used to measure the deposited energy of the particle exiting the system and to veto shower events. HMB enables to handle sub-nanosecond timing of signals, and its digital processing core is implemented on an FPGA, which instructs a PC to read out from each detector subsystem via Gigabit Ethernet. The collected data allow post-processing algorithms to determine the precise trajectory of the passing particle, hence enables the use of this information to categorize the device under test. This document focuses on the construction of HMB. It describes in detail its electronic readout system and presents some initial results.

CONTENTS

CHAPTER 1
INTRODUCTION

The Instrumentation Development Laboratory (IDLab) at the University of Hawaii has been producing a number of detector systems used at accelerator facilities (Belle II), underground detectors (Borehole Muon Detector), and in Antarctica (ANITA). Before deployment, these devices require testing and validation, which is usually done at other accelerator centers (SLAC, KEK, etc.), requiring extra time and significant funds. This is done by obtaining the trajectory of an incident particle by using reference detectors in the beam-line of an accelerator research facility and comparing the trajectory of the particle beam of a separate device under test (DUT). By having a reference beamline detector system in-house, said tests may be done and deployment of a detector system could be smoother, thus lowering development time and costs. It is presented in this document, a method of development of a prototype detector, which will meet the needs of obtaining a reference beamline in which a DUT may be tested.

1.1 Problem Definition

An Imaging Time-of-Propagation (iTOP) detector prototype was built by the IDLab in March 2010. It measured cosmic muons and tracked their position as they passed through four superlayers of 32 cylindrical drift tubes. As cosmic muon passes through the system, Cherenkov photons are internally reflected and collected with a Hamamatsu H8500 Multianode PhotoMultiplier Tube. A custom Application Specific Integrated Circuit (ASIC) then records these events [1]. Although the iTOP prototype detector has been built and tested to work well, there is a need to use similar technology allowing a DUT to undergo positioning tests. For this research, a second generation detector, The Hawaii Muon Beamline (HMB) has been designed and built from ground up.

Hypothesis *The next generation Hawaii Muon Beamline, is an improved cosmic-ray observatory reference system, which will allow significant detector and electronics testing of devices produced before being deployed to a permanent area of establishment.*

1.1.1 Research Objectives

- To design, fabricate, and test individual components required for a fully functional HMB system after integration.
- To integrate components using a common clock distribution system allowing synchronization of data acquisition for a cosmic-ray muon detector where precision timing is needed.

1.1.2 Background

The HMB is a muon detector which detects muons that are created by cosmic ray particles as they enter the Earth's atmosphere. On average, about 10,000 muons reach every square meter of the earth's surface per minute due to their mean lifetime of 2.2 μs [2]. In order to detect theses muons, clear plastic scintillator blocks are used. A scintillator block is a type of material which exhibits scintillation when ionized by a particle such as a muon, which during the process absorbs some of the particle's energy and re-emits in the form of light [2]. A Silicon PhotoMultiplier Diode (SiPM) or a Photo Multiplier Tube (PMT) then detects the light which was created due to scintillation and outputs an analog pulse which could be read by a scope or a custom ASIC analog-to-digital (ADC) chip.

1.1.3 Approach

A clear and concise approach for the design and implementation of the HMB is shown with the following bullet list:

- Build a polyvinyl toluene (PVT) scintillator system for detecting positioning of an incident muon.
  - Construct four layers of square polyvinyl toluene detectors in the same X and Y axis. The distance in the Z axis is then taken in to consideration when reconstructing the angle of an incident muon.
  - Each of these four layers utilizes Multi-pixel Photon Counter (MPPC) SiPM devices in order to detect photons produced by the interaction of the transitioning muons [3]. The signal subsequently output by these MPPCs is an analog signal, which will be triggered upon and recorded by the TARGETX ASIC [4] [5].
- Build an off axis NaI detector system for detecting ionization loss of an incident muon.
  - An off-axis NaI detector system will be placed below the PVT scintillating planes. The analog output signal will be monitored by a dynamic range amplifier board, then digitized by the TARGETX chip [4] [5].
- Implement a clock distribution and trigger system.
  - A separate board was required which will allow a synchronized clocking system in which each subsequent trigger from a passing muon may be referenced to each other.

CHAPTER 2
OVERVIEW AND HMB STRUCTURE

This chapter describes each of the components required to build the HMB which is decomposed into three major categories: muon detection methods, readout electronics, and the mechanical subsystem. The detector systems utilizes the method of scintillation in order to emit light produced by a passing muon. The readout electronics then digitizes analog pulses produced by SiPM devices or PMTs. The data is then collected by a PC using readout electronics where offline analysis software is utilized to reconstruct the path trajectory of the incident muon. Due to the method of detection, introduction of any unnecessary light will skew data taken, thus the detector subsystem must be in a completely dark environment.

The mechanical subsystem includes the design and implementation of dark chamber while still allowing easy access to components inside.

The block diagrams in Figure 2.1 and Figure 2.2 shows the author's contribution in HMB. Blue blocks indicate the portions of the HMB components that were designed by the author, where red blocks is a colleague's contribution. Coordination and teamwork played a large part in the design and implementation for the entire project.

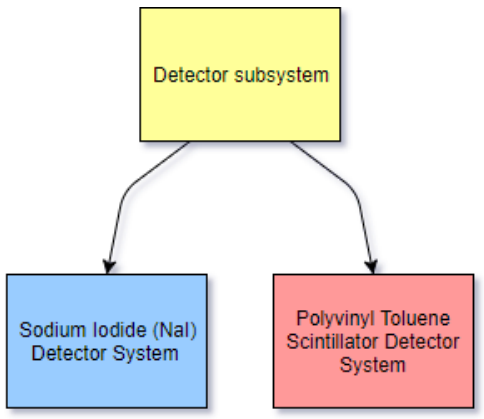

Figure 2.1: The two types of detector subsystems, blue shows the author contribution with the Sodium Iodide (NaI) detector system, and red shows a colleague's contribution with the Polyvinyl Toluene system.

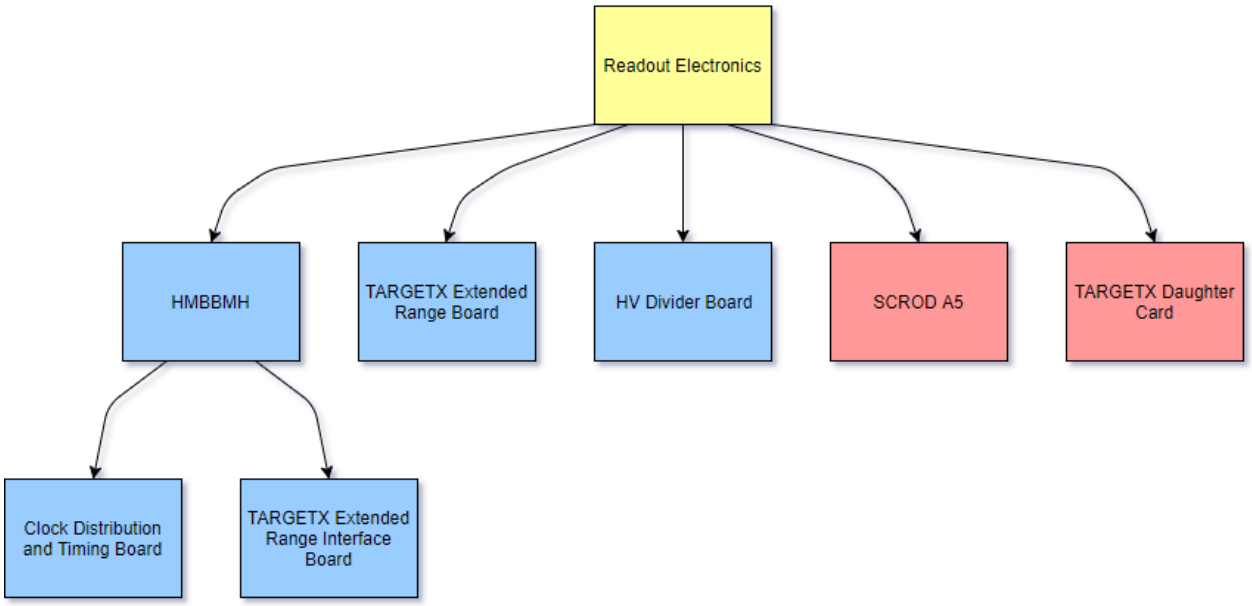

Figure 2.2: There are five different types of readout electronics. Blue blocks shows the author's contribution which include HMBBMH, TARGETX Extended Range Board, and HV Divider Board. Red blocks show a colleague's contribution which include SCROD A5, and the TARGETX Daughter Card.

Figure 2.3 shows an overview of a muon traveling through the detector subsystems. In order for an event to be valid, it first enters the top Polyvinyl Tolueue (PVT) plane then it must exit the bottom PVT plane. Once the entire HMB system is calibrated, data from a DUT can be compared to the data obtained by the PVT planes and calorimeter systems. As a muon travels through the top PVT plane, a trigger is sent to the CDT board which prepares each detector system for a readout once a valid event is registered. During readout, each detector system, including the DUT will send all data to a PC where offline post-processing occurs.

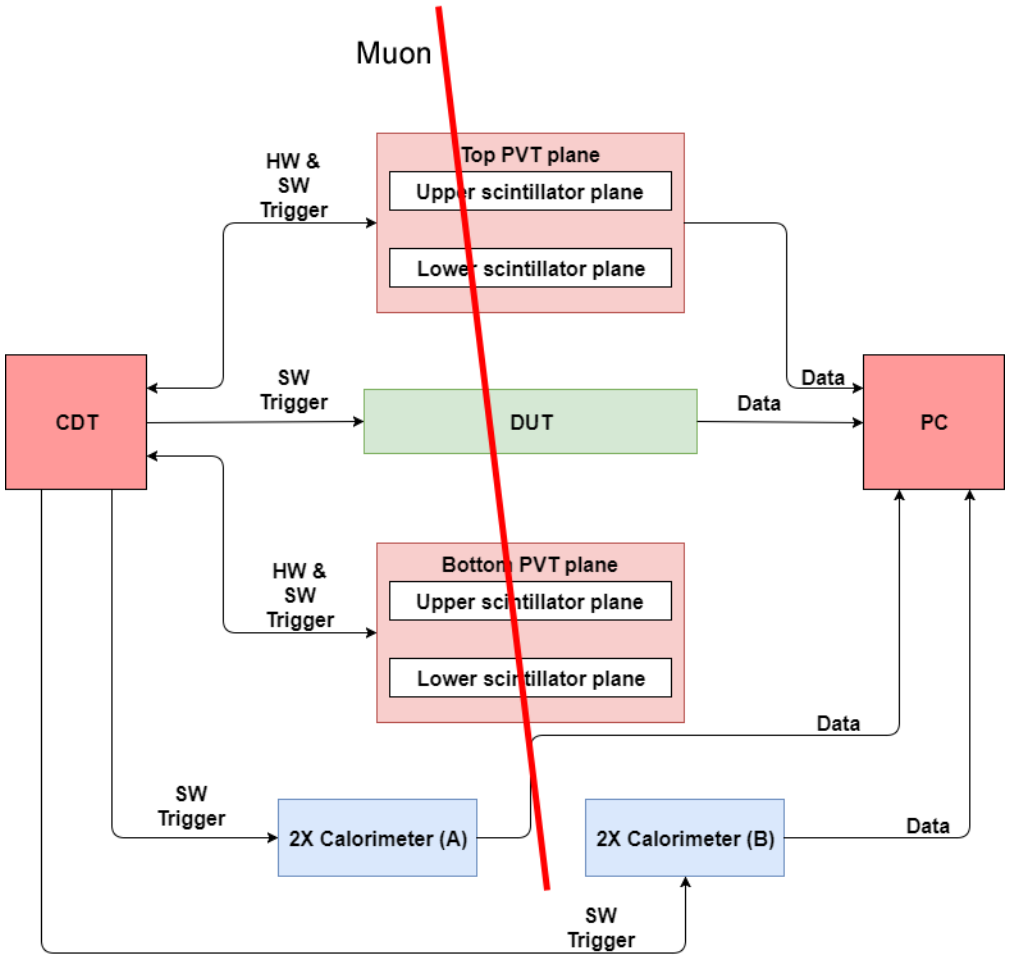

Figure 2.3: Overview of HMB system showing muon traveling through detectors..

The following subsections describe how the PVT detector planes and NaI detector systems work in order to capture the required data to show muon trajectory through the HMB system.

2.1 Muon Detection Methods

In HMB, Once photons are emitted within a scintillator block due to interactions with passing muons, either silicon photodiodes or photo multiplier tubes are used to sense these photons. The following subsections describe the two types of materials used for detection within HMB.

2.1.1 Polyvinyl Tolueue Scintillator

Polyvinyl Tolueue (PVT) Scintillating detector planes are primarily used for capturing the positioning of a particle as it travels through HMB. There are a total of 4 PVT scintillator planes which

are aligned in the X and Y axis. Each plane can track an estimated position of an incident particle. In order to do so, the PVT material has been cut into blocks with a square area of 30cm x 30cm and a thickness of 1cm. The top and bottom layers are engraved with grooves to accommodate 2mm thick wavelength shifting fiber [6]. There are 15 grooves with a pitch of 400mils on top of the block, and 15 grooves with the same pitch on the bottom. These grooves are machined out orthogonal to each other. The fiber is then inserted in these groves which are fixed with optical cement. Figure 2.4 shows a single machine grooved PVT blocked with wavelength shifting fibers installed.

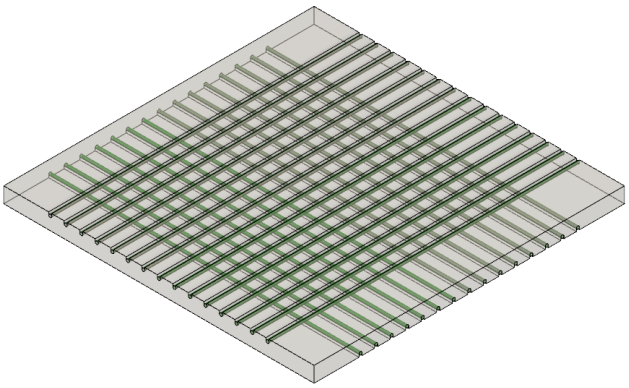

Figure 2.4: Machined grooved PVT scintillator plane with wavelength shifting fibers installed.

As charged particles are incident through each PVT block, photons are emitted in the blue light spectrum, they are then coupled to the wavelength shifting fiber. This type of fiber was chosen since its output light, which is shifted to the green light spectrum, are detected by the Hamamatsu S13360-1325CS MPPC with the highest absorption efficiency [3]. The SiPM devices are coupled to one end of the wavelength shifting fiber using optical cookies. On the other end of the wavelength shifting fiber, reflective tape has been installed. As a muon travels through the scintillator block, the wavelength shifting fibers in proximity to where the muon was incident will couple more light than ones further away. Different light intensities detected from each of the wavelength shifting fibers by the SiPM devices could then be used to pinpoint the exact location of where the particle has interacted within the PVT plane. In the most ideal situation, a muon will travel through each of the 4 planes in which it's trajectory within the HMB structure could be reconstructed. A muon incident with a PVT plane may experience ionization loss due to inelastic collisions with atomic electrons of the material [7]. The energy transferred during these collisions can accelerate these electrons thus producing secondary showers which is detectable with an off axis detector system beneath the 4 PVT scintillating planes. Figure 2.5 shows a plot of muon ionization losses for different materials [7]. For a muon with 1GeV of energy, we can expect about 1MeV of energy loss throughout each PVT plane on average.

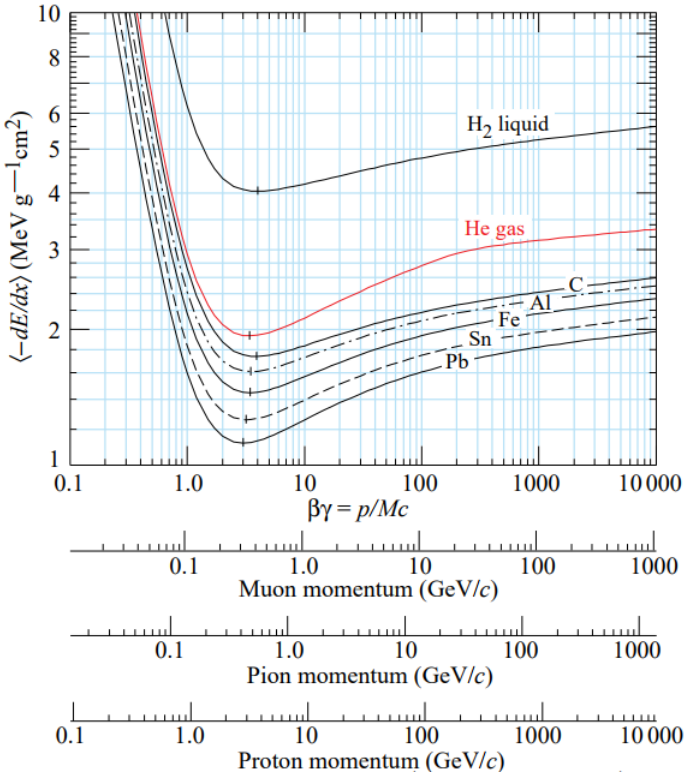

Figure 2.5: Ionization loss plot of a muon incident with various materials.

2.1.2 NaI Scintilators

Sodium Iodide (NaI) scintillation detectors are used to detect deflecting electrons due to potential ionization loss of the incident muon within a PVT scintillator block. The NaI detectors in which was used in HMB have rectangular cross sections with the dimensions of 15.75 x 2.25 x 4.33 inches (see Figure 2.6). A rectangular cross-section NaI detector provides a larger acceptance area in contrast to a circular version.

Figure 2.6: Square cross-section NaI scintillation detectors.

When muons collide with electrons within a PVT plane, the resulting energy transfer will

accelerate the electrons which could cause many collision per path length. We can detect any deflecting electron by providing a secondary NaI detector plane which is placed around the base of the structural support of the PVT planes. Figure 2.7 shows the PVT detector tower with the NaI scintillator detectors surrounding the base.

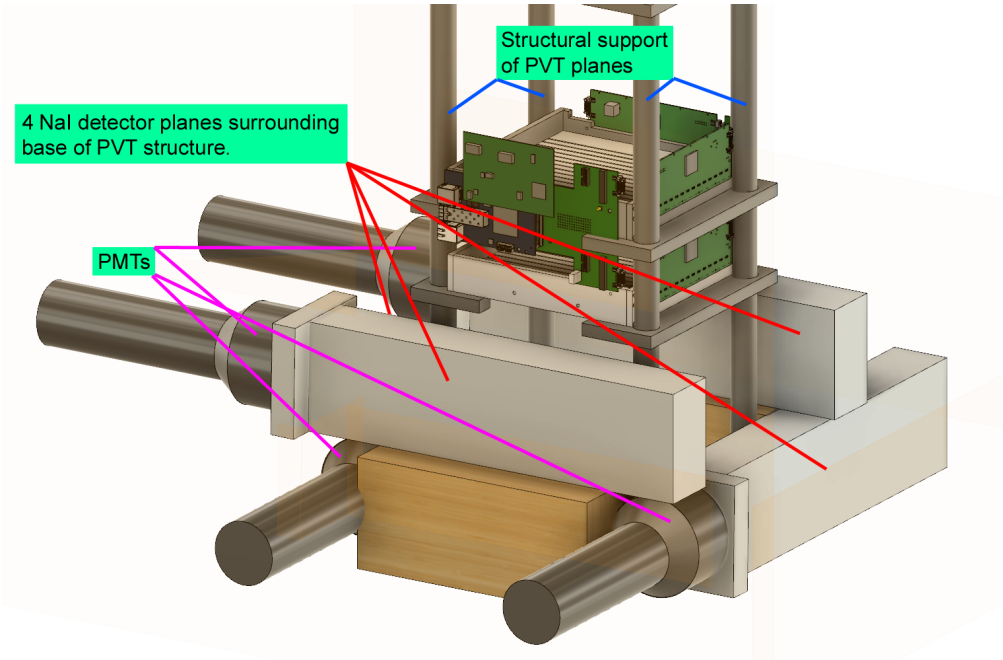

Figure 2.7: PVT detector tower showing rectangular NaI detectors.

As these deflected electrons interact with the NaI scintillator, photons are emitted and detected by a PMT which is fixed at the end of each NaI detector. As the photons reach the PMT, they interact with a layer of photocathode material which emit electrons. These electrons are then ejected into a sequence of numerous dynode stages where each stage is roughly 100V higher in potential than the last. These dynode stages allow electrons to be proportionally multiplied where the last stage, the anode, creates a current pulse which is detected.

2.2 Readout Electronics

2.2.1 TARGETX ASIC Overview Description

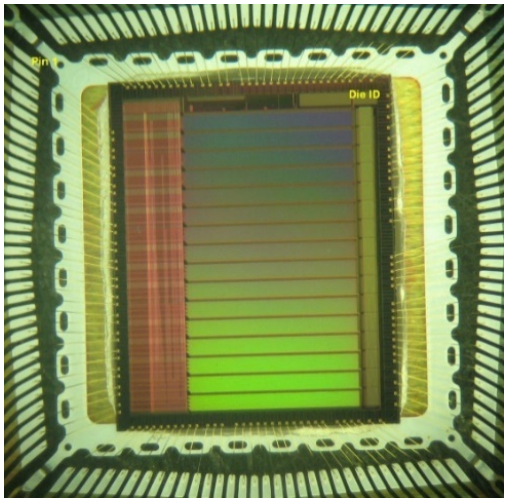

Figure 2.8: Die of TARGETX Waveform Digitizing ASIC.

The TARGETX is a waveform digitizing ASIC (Figure 2.8) which is capable of digitizing analog signals at a rate of 1 Giga-Samples Per Second (GSPS) [4] [5]. It was designed by Prof. Gary Varner and was fabricated in the TSMC 250nm CMOS process. There are 16 analog input channels where a digital readout of the data is done serially for each channel simultaneously. Each channel contains a storage array of 512 sets of 32 memory storage cells allowing a total viewable window of 16.3 μs. A signal over threshold circuit available within the chip allows a self-triggering system which is an important feature for particle detection. The TARGETX is used to sample the analog pulses which the silicon photodiodes and PMTs produce from light emitted due to scintillation. Many previous experiments which utilizes PMTs and other photo detectors often used oscilloscopes to record and collect data. The TARGETX, dubbed "oscilloscope on a chip," is a much more efficient way for any modern particle physics experiments to record many channels of data simultaneously while saving space and power. Some examples of other experiments which utilize the TARGET family ASICs to obtain data are the Cherenkov Telescope Array [8] [9] [10] and the Borehole Muon Detector (BMD) [11]. Due to strict timing requirements, the control of the TARGETX is done with an FPGA. The FPGA is then responsible for routing this data to a PC via Ethernet protocol.

2.2.2 TARGETX Daughter Cards (Khanh Le)

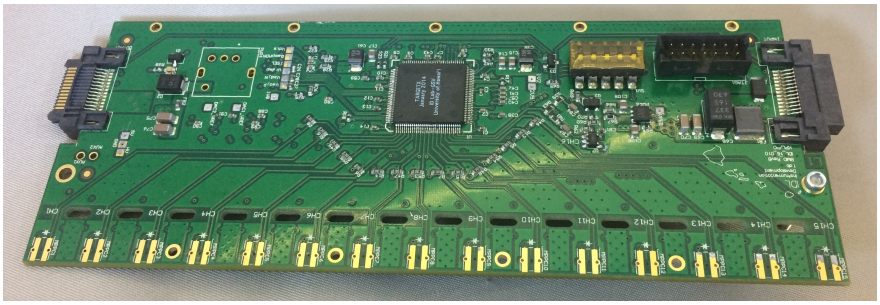

Figure 2.9: Top view of TARGETX daugthercard.

The TARGETX BMD Daughtercards shown in figure 2.9 were designed and built for the BMD project, but the design has been recycled for the Hawaii Muon Beamline. These daughtercards are equipped with 15 SiPM multi-pixel photon counters (MPPCs), at a pitch of 400mils, which utilizes multiple Avalanche Photodiodes in a single package (shown in figure 2.10).

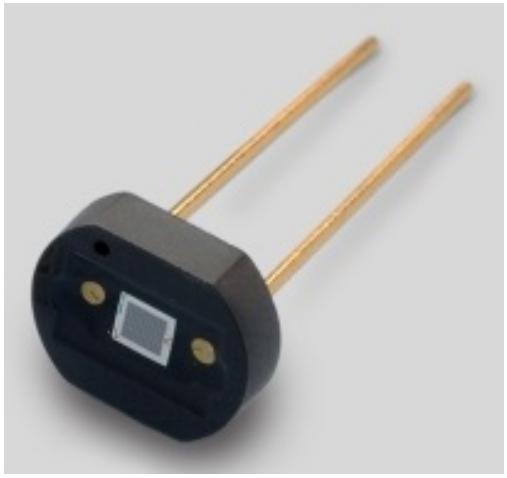

Figure 2.10: Hamamatsu S13360-1325CS. [3]

Each MPPC has a photosensitive area of 3mm x 3mm providing a pixel pitch of 50 μm offering a total of 3600 pixels [3]. It can detect single photons where the pulse of each photon is superimposed to the previous in discrete steps. Due to the discrete superimposed nature of the MPPC, it is ideal for detecting the intensity of light emitted from a device such as a scintillator. The signal produced by the MPPC is in turn monitored by an on-board TARGETX, and the TARGETX is controlled by a Xilinx SPARTAN 6 FPGA. Other components on-board the TARGETX Daughtercards include a DC-DC HV converter used for the biasing of the MPPCs, SRAM for the storage of pedestal voltages of the TARGETX, as well on power circuitry, and a temperature sensor.

HV Base for PMT

The PMT attached to the NaI crystal detects photons using 10 dynode stages which can provide gain of a primary electron as much as 100 millions times (160dB). In such a way, it is possible to detect individual photons when the incident flux of light is low where normally they were rendered undetectable. Each dynode stage is approximately 100V greater than the previous stage, with the anode being the last providing an AC coupled signal which will be read out to the TARGETX. In order to provide the voltages needed for the different dynode stages, as well as read out from an anode, an HV Base was designed and fabricated, see figure 2.11.

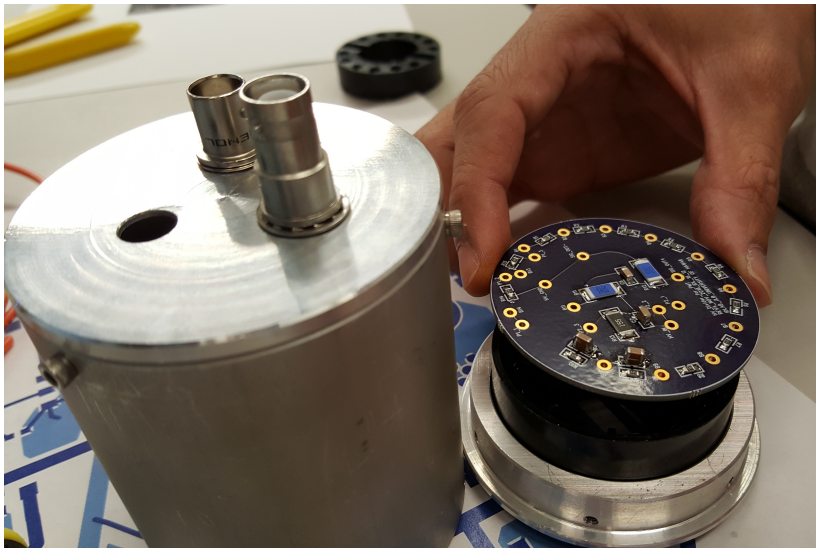

Figure 2.11: HV base enclosure (left) Internal HV divider board assembly (right).

The HV Base uses a circular PCB board design which contains the voltage divider circuit used in the dynode stages of the PMT. It attaches to the pin end of the PMT and provides HV to the dynode stages and a signal out connector. A voltage input of up to 1500V is provided to the HV Base through an SHV connector. As a signal is produced by the PMT, it is outputted through the BNC connector of the HV Base.

2.2.3 TARGETX Extended Range Board

Due to the broad range of energies, the PMT will output a wide range of pulses with amplitudes from the millivolt range all the way up to 10s of volts. Although the TARGETX can digitize analog pulses, it is only a 2.5V device, where pulses with magnitudes greater than 2.5V can potentially damage the ASIC. In order to read out these PMT pulses of various amplitude, an amplifier board providing various gain stages for lower signals, and attenuation stages for larger signals was needed for HMB. The TARGETX Extended Range Board utilizes a total of 2 attenuation stages as well

as 6 gain stages. The attenuation stages provides an attenuated signal of 10^{-2} and 10^{-1} of the original signal. The gain stages provides amplified signals of 10^{0} to 10^{5}. A signal pulse is injected into the TARGETX Extended Range board from the HV Base by a BNC cable. The signal is then fed to all the attenuation and gain stages simultaneously. The circuit is designed in such a way that the output of each attenuated or amplified signal is clipped at a voltage which is safe for the TARGETX.

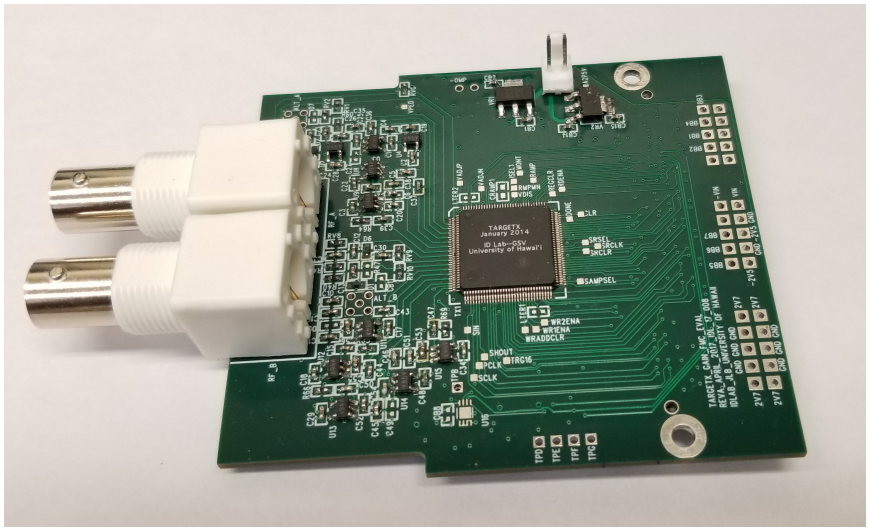

Figure 2.12: View of TARGETX Extended Range Board.

Figure 2.13 shows the circuit for the 10^{-1} attenuation stage. The voltage divider at the beginning determines the attenuation amount where the diode will clamp any voltages that will be unsafe for the TARGETX. Because the pulses from the PMT are negative going, a 1Megaohm pull-up resister raises the DC input allowing full range of readout to the TARGETX linear range. The 10^{-2} gain stage is similar except the divider resistors are configured differently.

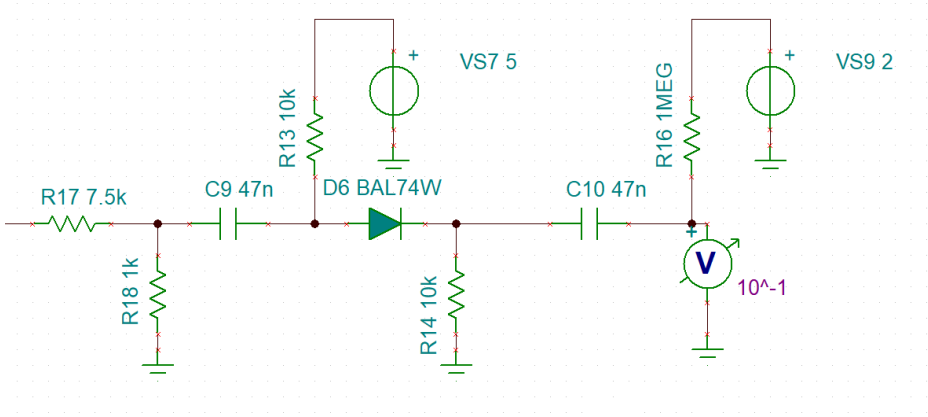

Figure 2.13: 10^{-1} attenuation stage on TARGETX Extended Range Board.

Figure 2.14 shows the circuit for the 10^{1} gain stage. A non-inverting amplifier configuration allows a gain of approximately 20dB. Each gain stage thereafter is then copied and cascaded.

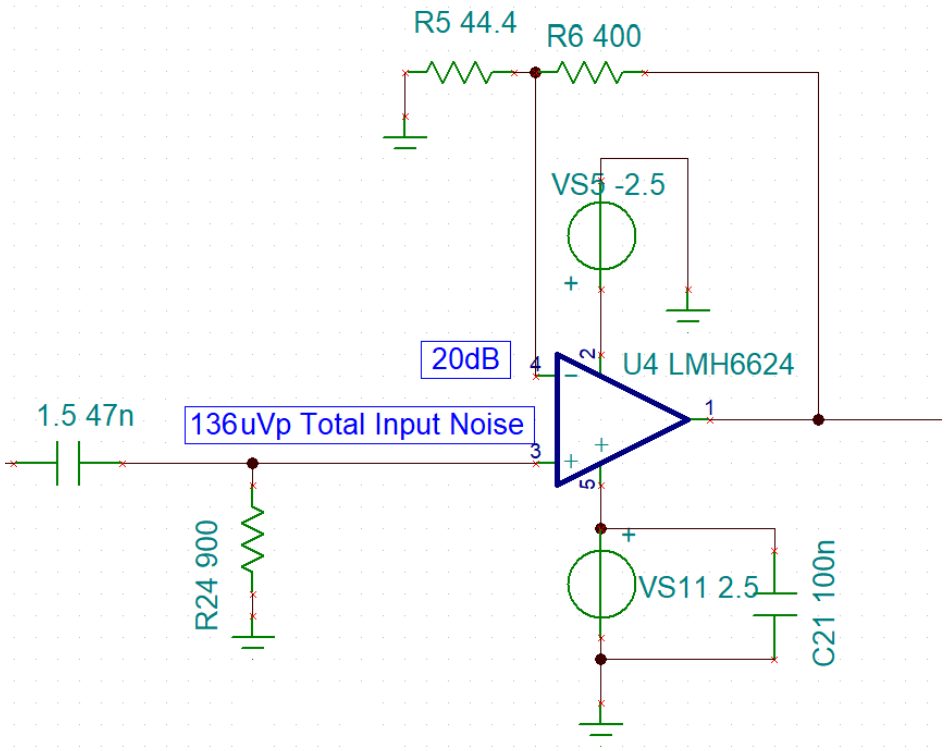

Figure 2.14: 10^{1} gain stage on TARGETX Extended Range Board.

After the TARGETX digitizes each variant of the input signal, it is sent to the PC for post analysis where the largest unclipped signal is used.

2.2.4 MicroZed Board

The MicroZed board (Figure 2.15) is a low cost development board which contains a Zynq 7010 SoC. It was chosen to be used as the control and readout of the TARGETX Extended Range board, as well as control for the Clock Distribution and Triggering (CDT) board. The Zynq 7010 SoC features an Programmable Logic (PL) equivalent Artix-7 containing 28k logic cells and a total of 2.1Mb of addressable block memory. A dual-core ARM Cortex-A9 microprocessor core with clock speeds up to 667MHz resides as the Processing System (PS) side of the Zynq 7010. In order to fully utilize the MicroZed, HMB will need a carrier board which will connect to the bottom connectors of the MicroZed, this will allow access to a total of 100 PL pins which may control a TARGETX chip. An on board Ethernet jack provides communication to a PC for data logging. The MicroZed board will be used with the TARGETX Extended Range board which it will interface through the HMBBMH motherboard.

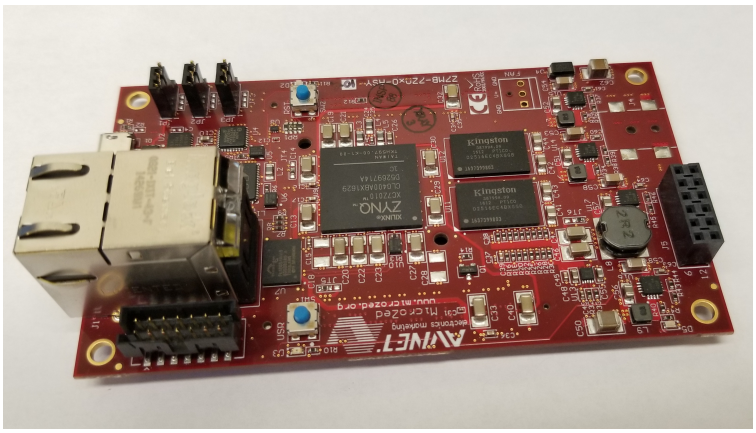

Figure 2.15: View of Microzed board

2.2.5 SCROD A5

The SCROD A5 (Figure 2.16) is a development board which was designed and have been used on multiple projects in the IDLAB. It uses a Xilinx Spartan 6 XC6SLX150T FPGA which contains 147,443 logic cells and a total of 4,824 Kb of addressable block memory. There are a total of 4 120 pin connectors which provide voltage/ground nets, and access to I/O pins of the FPGA for a connected device such as the TARGETX BMD Daughtercard.

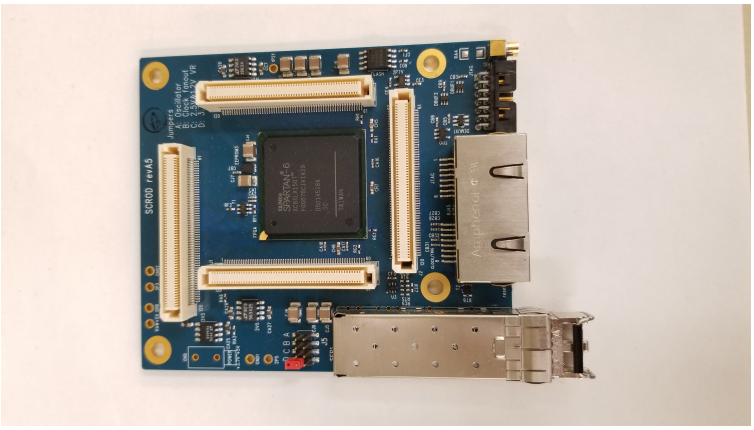

Figure 2.16: View of SCROD board

2.2.6 HMBBMH Board

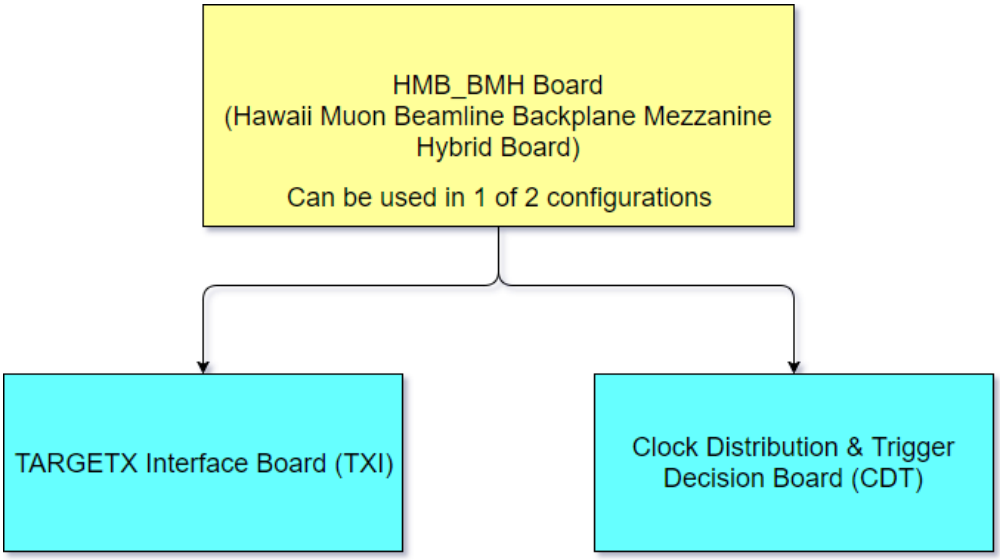

Figure 2.17: HMBBMH board configurations.

The Hawaii Muon Beamline Backplane Mezzanine Hybrid (HMBBMH) motherboard was designed specifically for HMB. The HMBBMH board is a single board that functions as two separate types of board. As in Figure 2.17, the first function of the HMBBMH board is an interface motherboard for the TARGETX Extended Range boards. Although the TARGETX Extended Range Boards provides an ASIC on-board, it does not contain an FPGA which is needed for control and transfer of data to PC. The HMBBMH board includes a LPC FMC connector which the TARGETX Extended Range board can connect to, as well as connectors for a controlling FPGA board. The second function of the HMBBMH motherboard allows it to act as a clock distribution and

triggering board. It is necessary that the readout electronics for all detectors within HMB operate at the same frequencies with minimal phase shift. A PC external to HMB will make the final decision on whether events registered from each detector is valid. Each event needs to happen at nanoseconds apart from each other otherwise the events are most likely not related. Power may be provided through the on-board Molex connector or via VME connectors. If using VME connectors, as in HMB, variant of the boards will be seated vertically on a VME connector board. There are on-board regulators which provides power to various components on board, as well as to the connected FPGA and TARGETX Boards. The HMBBMH board was also designed so that multiple variants of the board can be in the same JTAG chain, this allows the FPGA on each board to be configured using one single TCL script without having the need to disconnect and reconnect Digilent JTAG programmers after programming each individual FPGA. The following will go more in-depth to the two separate functions of the HMBBMH Motherboard.

TARGETX Extended Range Interface Board (TXI)

Figure 2.18 shows a diagram of the features of the HMBBMH TARGETX Interface board included to be used as a TXI Board. The blocks shaded with blue represents components that are installed on the board, and blocks shaded in red represent components that are not installed. For this version of HMB, the connectors for the MicroZed board has been populated so that the Zynq 7000 may be used to control the TARGETX. All connections from the MicroZed board has been routed directly to the TARGETX Extended Range Board. An RJ45 triggering connector provides a remote clock which is relative to the clock of the whole HMB system as well as trigger bits from the CDT board. The remote clock from the Ethernet port is then inserted into a 1:2 fanout chip where copies of the clock are used for the TARGETX digitization firmware on the ZYNQ, the other copy is not used in this configuration since the on-board SFP connector will not be used.

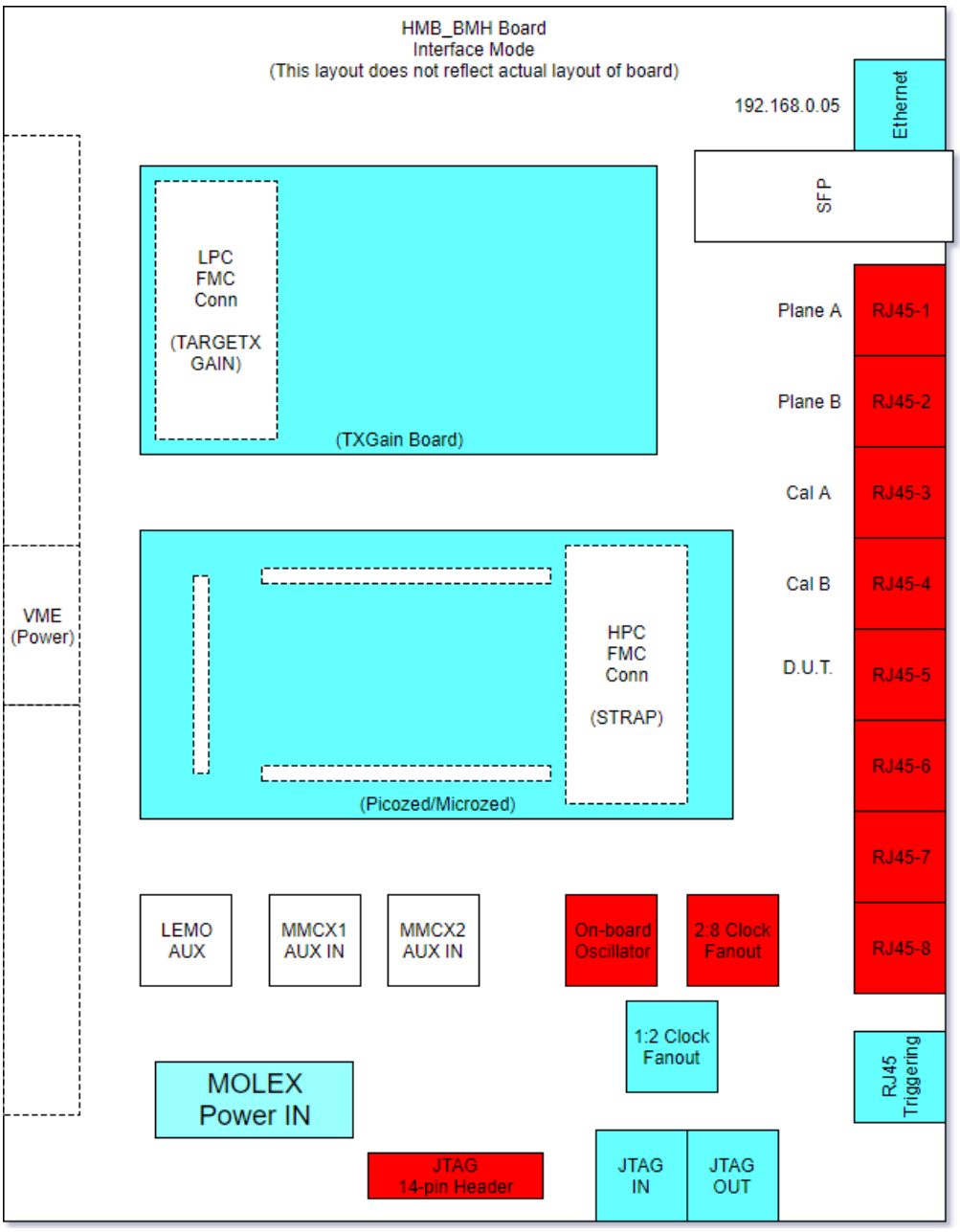

Figure 2.18: TARGETX Extended Range Interface board configuration.

A final version of the TARGETX interface board showing required components installed can be viewed in Figure 2.19.

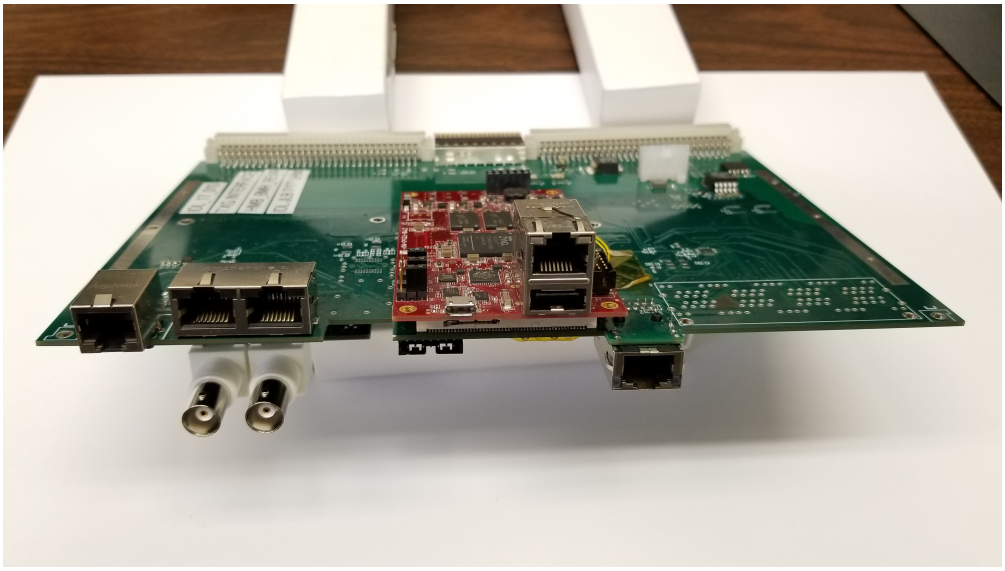

Figure 2.19: Fully populated HMBBMH board configured as TARGETX interface board.

Clock Distribution and Triggering Board (CDT)

Figure 2.20 shows a diagram of the features of the HMBBMH motherboard included to be used as a CDT Board. Primarily, this variant of the HMBBMH motherboard is used as a clock distribution board. An RJ45 housing provides 8 connectors, 7 of which are used to output a remote clock, and triggers to and from the detector subsystems. The connectors for the MicroZed is populated in order to used the Zynq SoC for decision logic which then determines when an external PC obtains data from the detector planes. A JTAG header pin allows for a Digilent programmer to be installed to this board specifically where each subsequent HMBBMH board can be connected via an Ethernet cable using the JTAG out/in jacks were a JTAG chain could be initiated, allowing for a simple method of programming all Zynq FPGAs at a single time. Further details on how the decision logic works is explained in the next chapter.

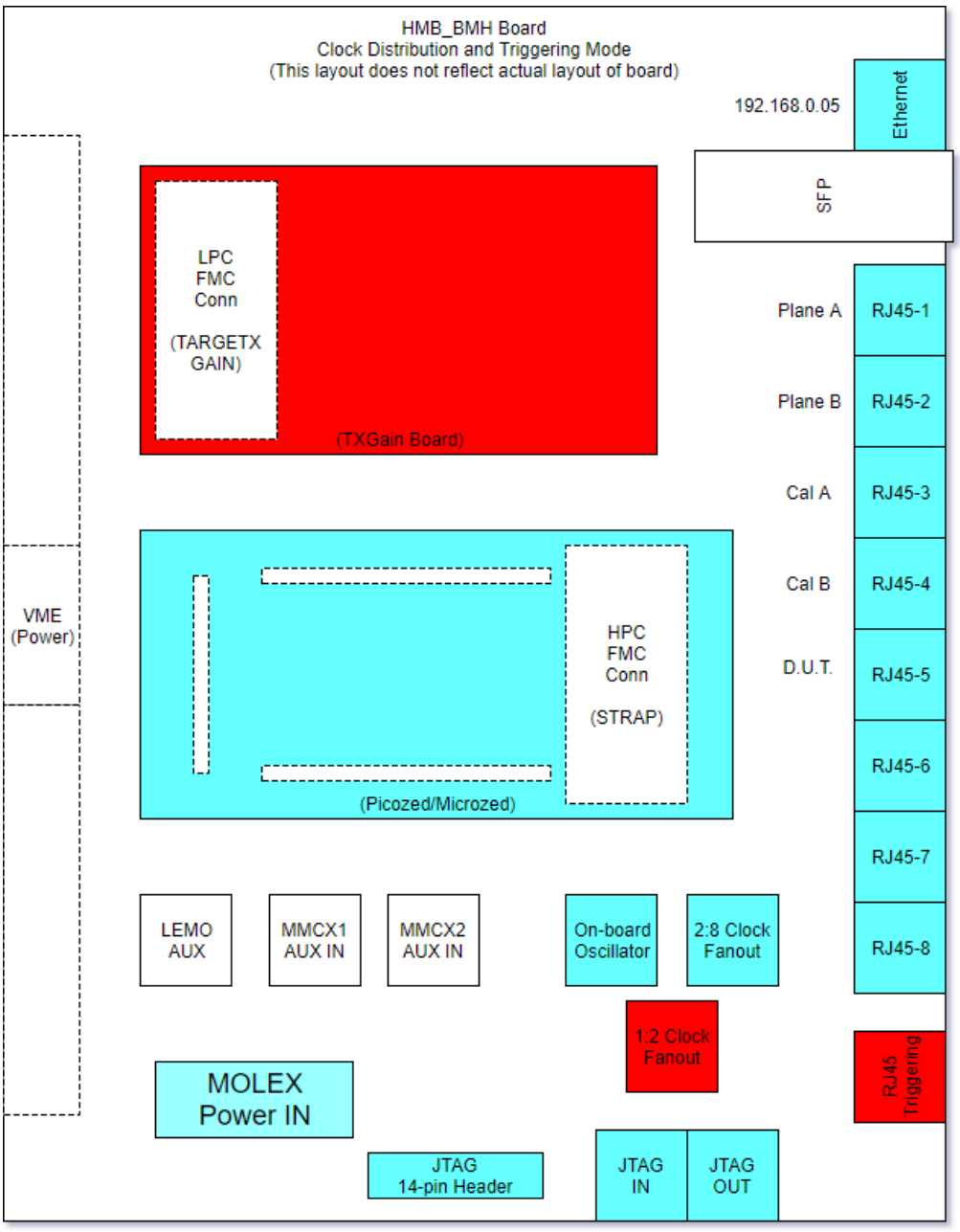

Figure 2.20: HMBBMH Clock Distribution and Triggering board configuration.

A final version of the CDT board showing required components installed can be viewed in Figure 2.21.

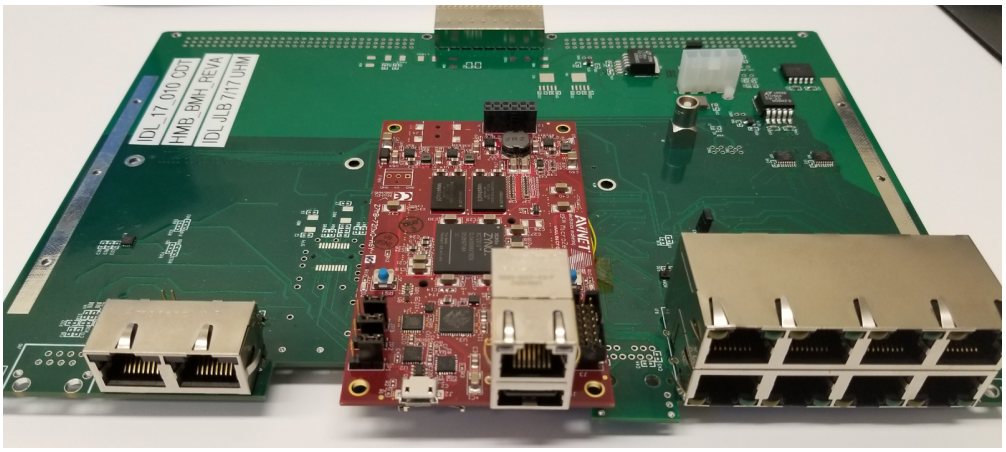

Figure 2.21: Fully populated HMBBMH board configured as CDT board.

2.2.7 External PC

An external PC which will sit next to the HMB structure will communicate with the components within the interior of HMB. The CDT board will instruct the PC when an event of interest has occurred, immediately after, the PC will query the data from the readout electronics of each detector subsystem which will be distinguishable by distinct IP addresses. Once the data is obtained, the PC will display real-time data of the event.

2.3 HMB Enclosure

This first version of Hawaii Muon Beamline uses two different types of detector systems. The NaI detectors include a light shielded casing straight from the manufacturer, but the PVT scintillator planes are exposed. Due to this, the HMB enclosure needs to be completely shielded from any external light source. The design that was chosen for the HMB enclosure gives a completely light tight interior while still allowing I/O and power throughput. The next sections describe the mechanical components used to build the HMB enclosure, miscellaneous components used, as well as power distribution for the entire system.

2.3.1 Mechanical Subsystem

Construction of the HMB enclosure took many factors in to consideration. The first was that the interior needed to be dark. The HMB enclosure also needed to be modular which will allow different configurations need for various DUT device testing. Finally, the structure needed to have easy access to the interior as well as provide throughput connectors for I/O data and power. A frame using aluminum t-slot extrusion provides a skeletal structure for the walls which was made

from plywood. The walls sit on an optical bench which takes up 48 1/4 x 46 1/4 inches of space. The exterior is 48 inches high which allows the detector tower to fit within the light tight HMB enclosure. The bottom of the HMB enclosure is bare which was done to give interior components a flat surface provided by an optics bench, allowing easily customizable setups for any future experiments.

Figure 2.22 shows the interior detector tower. The inside wall has been painted matte black which absorbs any light which may leak in. T-slots were used to build the 4 corners of the detector tower where the shelving of the PVT scintillator planes, made out of acrylic, provide structural stability. Space for a center shelf allows future DUT devices to be installed. In order to gain access of the components inside, the front side of the structure is completely removable. A semi-thick layer of neoprene lines the inner seams of the front wall which blocks any outside light which may seep in through cracks.

Figure 2.22: Preliminary photo of the interior of the HMB enclosure shown.

2.3.2 Miscellaneous HMB Components

An I/O panel on the side wall of the HMB structure provides input and output data to an external PC. Table 2.1 shows the various connectors which are installed on the I/O panel. In total there are 6 USB throughput connectors, 4 Ethernet couplers, and one AC adapter connector. The 8 USB connectors are primarily used for connecting JTAG programmers to the HMBBMH and SCROD boards during testing, once firmware is closer to finalization, the firmware will be flashed to the board and the USB connectors may not be necessary any longer. A power strip powered by the AC adapter connector will provide AC power to any miscellaneous part that may be inside the HMB structure. So far, an Ethernet switch is the only component which will need to be plugged to the power strip. Figure 2.23 shows the I/O panel before installation.

Table 2.1: Throughput connectors on the HMB I/O panel.

8x USB throughput ports
4x Ethernet throughput ports
1x SMA throughput ports
AC Adapter for internal AC power strip

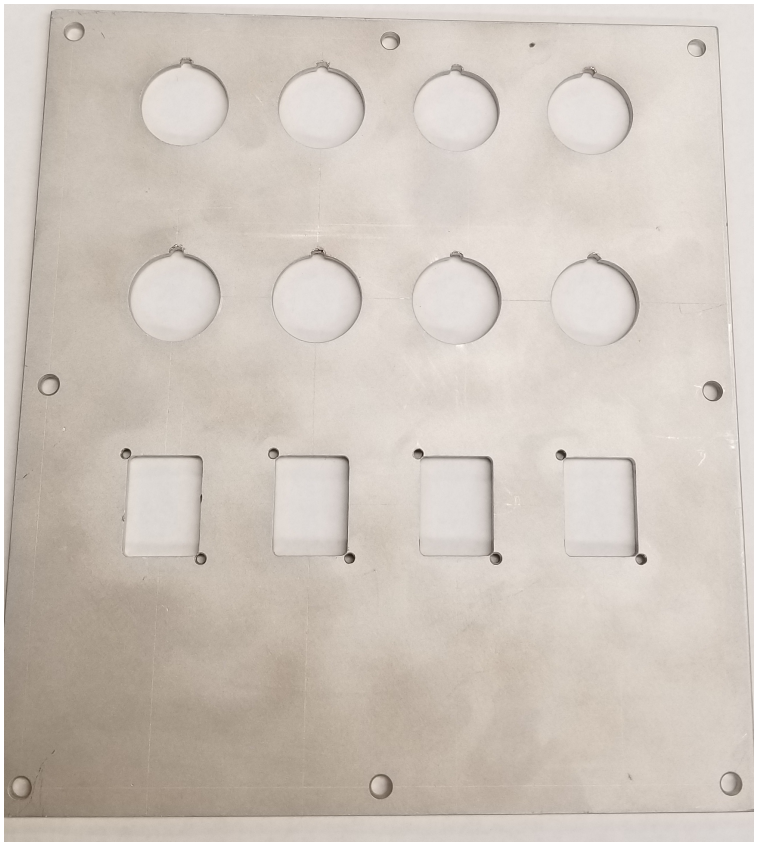

Figure 2.23: View of I/O panel before installation. Holes for AC plug and SMA cable are not shown

CHAPTER 3
IMPLEMENTATION

In this chapter, the HMB components are assembled to create detector subsystems as well as the main clock distribution and triggering system. It describes the integration of the HMB components and its implementation in hardware.

3.1 Experimental Setup

There are two types of detection systems as mentioned in Chapter 2, PVT scintillator planes, and the Calorimeter system. Both the top and bottom PVT plane consists of two scintillating planes. Between both pairs of the PVT plane is a shelf where a DUT will be placed. As a particle traverses through HMB, any muon which passes through all PVT planes could be used to reconstruct its trajectory path. Any DUT on the middle shelf should show the same trajectory path as the reference beamline provided by HMB. The following subsections will show each of these detector subsystems as a whole and how everything is integrated.

3.1.1 Clock Distribution and Triggering

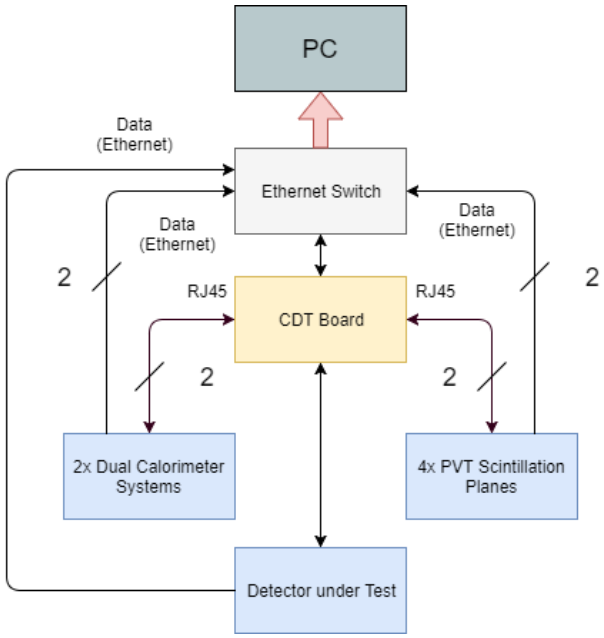

Figure 3.1: Block diagram of readout system. The CDT board obtains local triggers from all detector subsystems, then instructs a PC to collect data during events of interest.

The CDT board in the HMB controls the entire system, it is responsible for letting the PC know when to obtain data from all detector subsystems after determining when an event of interest has occurred. A central Ethernet switch connects the CDT, all detector subsystems, as well as the PC together. Figure 3.1 shows a block diagram of the CDT board (yellow) connected to the detector subsystems and an Ethernet switch. An RJ45 trigger cable specifically provides a synchronized remote clock, and provides local triggers from the detector subsystems to the CDT board. If in the situation of Figure 3.2, when a muon is incident through each PVT plan subsequently, a local trigger from each PVT scintillating plane will signal the SCROD to collect data from the two planes in which it is connected. If data from both planes is shown to have originated from the same muon, a second level trigger is sent from the SCROD to the CDT. The CDT then determines if the lower two PVT scintillating planes signals the CDT to indicate that same muon has passed its system. If it has been too long for the second trigger from the second plane to signal the CDT, the CDT then marks the first set of data from the first PVT plane as non-usable. If in the case that a muon travels through all 4 PVT scintillating planes, the CDT sends a global trigger to the PC, indicating for it to connect data from the two SCRODs, collecting data from all four PVT scintillating planes. The PC also collects data from the NaI detector subsystems which may give additional information of the incident muon. The PC is able to collect data from each of the detector subsystems sequentially since each detector subsystems have it's own IP address.

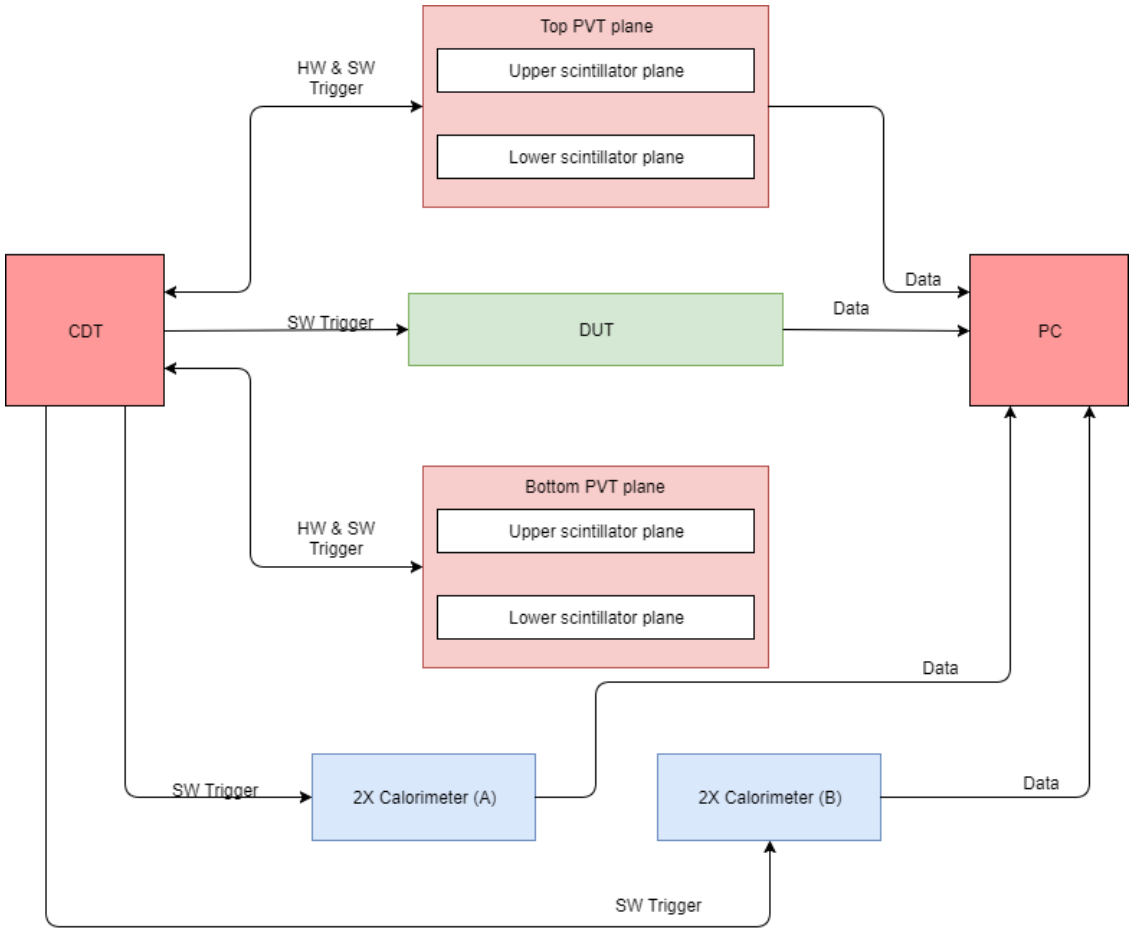

Figure 3.2: Shown is the HMB detectors integrated together. Above are the top 2 PVT scintillation planes, the DUT shelf, and the bottom 2 PVT scintillation planes. The base is surrounded by four NaI detector systems.

3.1.2 Detector Subsystems

Scintillating Detector Planes

In HMB, two PVT scintillating planes will be stacked together and share the same SCROD. Each of the PVT scintillating planes will have two TARGETX daughtercards, one for the X-plane, and another for the Y-plane. The SCROD acts as a main data collector and will obtain data from each daughtercard and send it up to a PC given any events of interest.

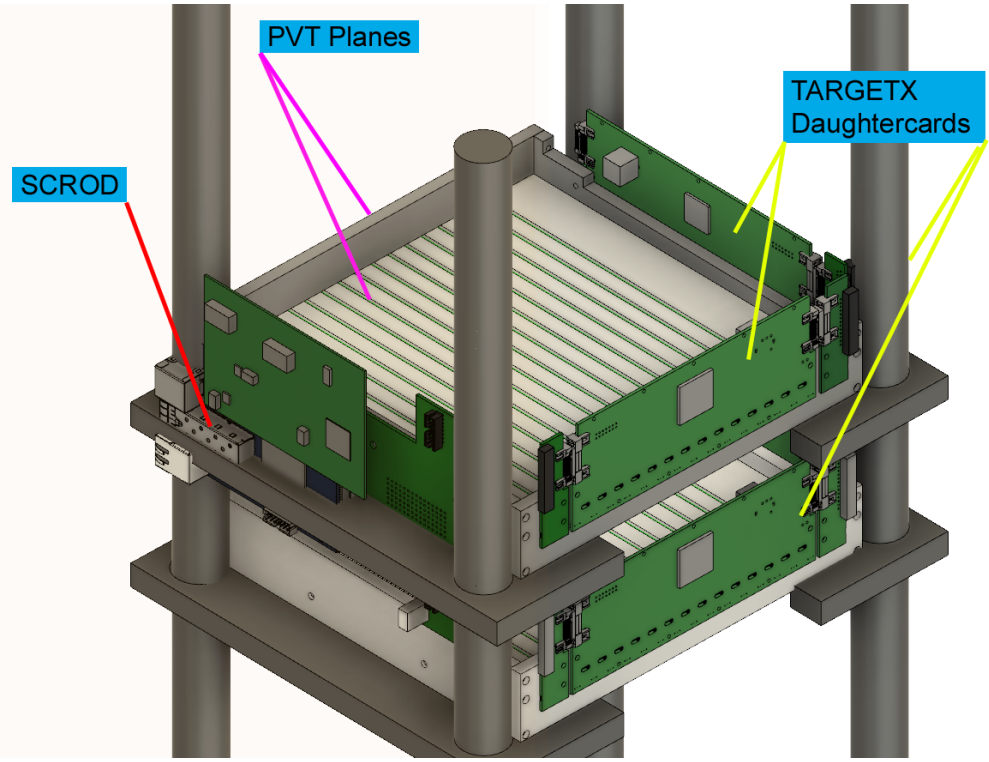

Figure 3.3: Polyvinyl toluene detector blocks w/readout electronics.

Figure 3.4 shows an overall block diagram of the readout system for two stacked PVT detector planes. When a large enough pulse from any MPPC triggers the TARGETX, the TARGETX will obtain digitized waveforms from each of the 15 MPPCs in parallel. The data will then be stored in BRAM on the SPARTAN 6 for each of the daughtercards. The SPARTAN 6 will then packetize the data and send it to the SCROD where it is then on standby to send to the PC if requested by the CDT.

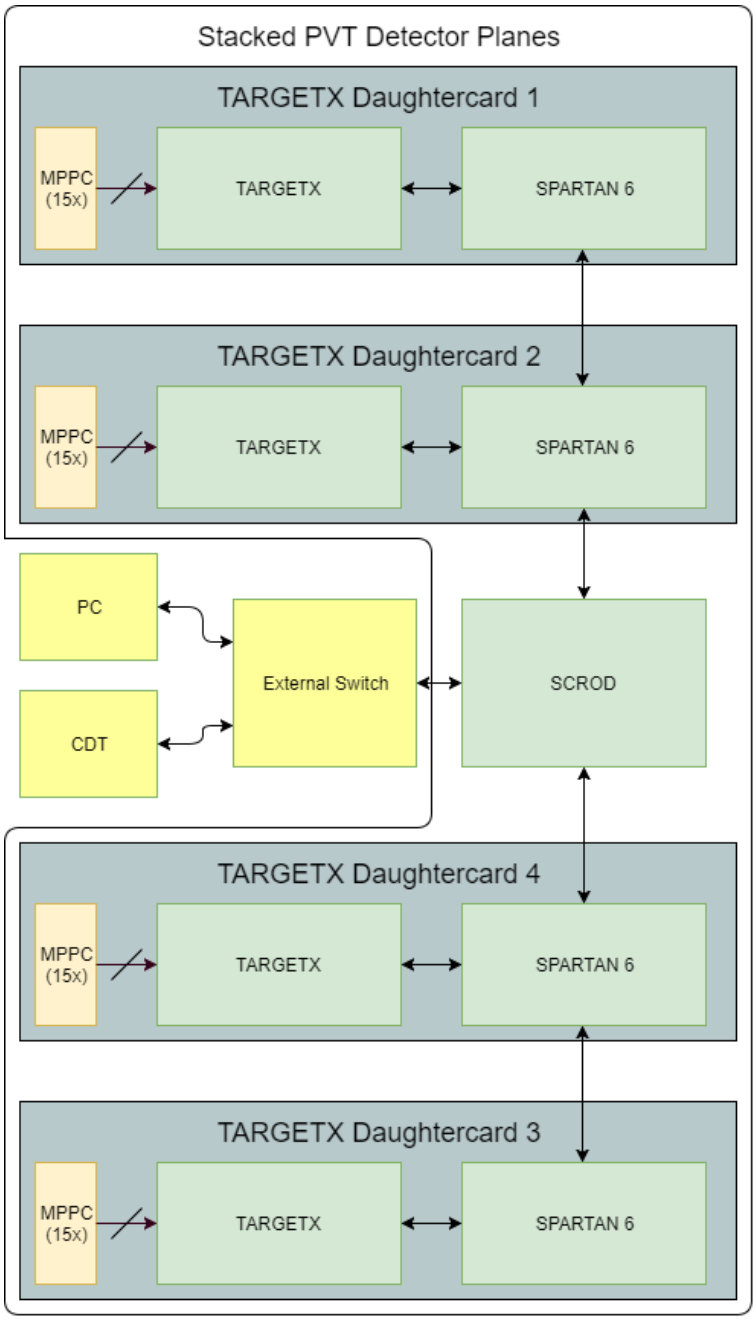

Figure 3.4: Block diagram showing two stacked detector planes sharing the same SCROD.

Calorimeters

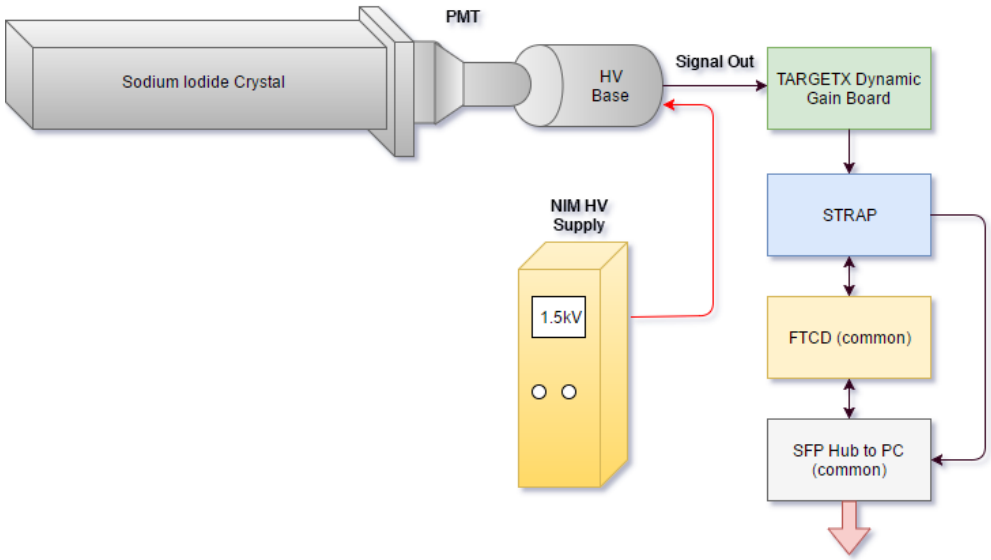

Figure 3.5: Block diagram showing readout of a single calorimeter.

The calorimeter system in Figure 3.5 will monitor particles as they interact with the NaI crystal. The HV Base provides external HV to the PMT as well as provide a signal out to the TARGETX Extended Range board via BNC connector. The TARGETX Extended Range board of provides the eight gain stages from 10^{-2} to 10^{5}. By reading out multiple gain stages in parallel, the user may perform post-processing in determining which channel to select in processing the data which gives the most data points without the occurrence of clipping. Once an event does happen, the STRAP board will send this information to the CDT control board, then from there, it is decided whether or not the data should be sent to the PC.

3.1.3 Firmware Implementation

Although the firmware used to control the TARGETX has been written in the past, effort was required in order to port over the TARGETX firmware to the Zynq 7010, for the TARGETX Gain board, as well as the SPARTAN 6, for the TARGETX daughtercards. The following itemized list shows all the devices in which custom firmware was required.

- TARGETX Extended Range Board – ZYNQ 7010
- CDT Board - ZYNQ 7010
- SCROD - SPARTAN 6
- TARGETX Daughtercard - SPARTAN 6

Figure 3.6 shows a Vivado block diagram of the processing side (PS) of the ZYNQ 7010. The two IP blocks of interest are the HMB_TX_Ethernet_Regs_0 and GPR_Registers_0. The ARM Cortex A9 block contains all the necessary IP within the PL in order to interface with the microcontroller, and the TARGETX REadout Firmware block contains the firmware which is needed in order to interface with the TARGETX. The GPR_Registers_0 custom IP block contains 24 32-bit registers which are required for the TARGETX firmware. Each register specifically controls a parameter of the TARGETX readout state machine which allows configuration and operation of the TARGETX. Figure 3.1 shows a legend of each register, what each functions as, and how many bits each consists of. The miscellaneous registers are primarily used for debugging purposes, while the rest of the internal_ registers are needed in order to configure the TARGETX so that it may be interfaced to. HMB_TX_Ethernet_Regs_0 IP block has been implemented in the programmable logic (PL) side of the Zynq which acts as a buffer for waveform data obtained from the TARGETX. These blocks are critical for the communication between each of the devices used for this application.

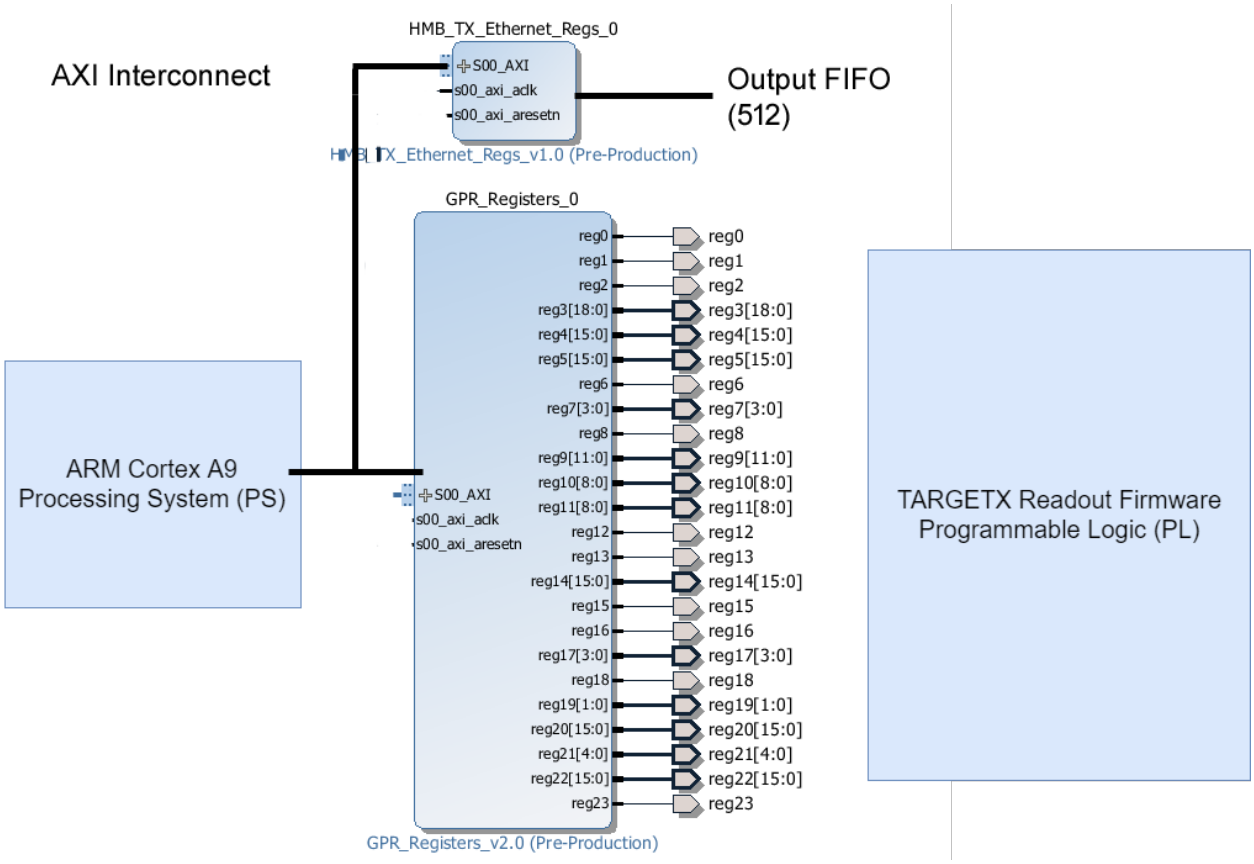

Figure 3.6: Block diagram in Vivado shows the processing system implementation interconnects in the programmable logic side. Software loads values into GPR_Registers_0 which controls the TARGETX readout state machine. Data produced from the TARGETX is then sent through an AXI FIFO, HMB_TX_Ethernet_Reg_0 back to the PS where code resides which sends data to a PC via Gigabit Ethernet.

Table 3.1: Zynq General Purpose Registers

Register	Function	bits
reg0	Miscellaneous	1-bit
reg1	Miscellaneous	1-bit
reg2	Miscellaneous	1-bit
reg3	Miscellaneous	1-bit
reg4	internal_tx_dac_load_period	16-bits
reg5	internal_tx_dac_latch_period	16-bits
reg6	internal_SOFTWARE_TRIGGER	1-bit
reg7	internal_CMDREG_trig_mode	4-bits
reg8	internal_READCTRL_asic_enable	1-bit
reg9	internal_READCTRL_trig_delay	12-bits
reg10	internal_READCTRL_dig_offset	9-bits
reg11	internal_READCTRL_win_num_to_read	9-bits
reg12	internal_READCTRL_readout_reset	1-bit
reg13	internal_READCTRL_RESET_EVENT_NUM	1-bit
reg14	internal_READCTRL_use_fixed_dig_start_win	16-bits
reg15	internal_CMDREG_SROUT_TPG	1-bit
reg16	internal_PEDMAN_calc_peds_en	1-bit
reg17	internal_CMDREG_PedCalcNAVG	4-bits
reg18	internal_RESET_SAMPLING_LOGIC	1-bit
reg19	internal_CMDREG_SAMPLIG_LOGIC_RESET_PARAMS	2-bits
reg20	internal_CMDREG_READCTRL_ramp_length	16-bits
reg21	internal_dac_addr	5-bits
reg22	internal_dac_value	16-bits

3.1.4 Power Distribution

There are numerous power rails needed for the HMB system: 24V, 6V, -6V, and ground. These are all provided by An Excelsys power supply which is installed on an exterior shelf of the HMB structure which provides up to 4 different voltages. Various power modules may be installed in up to four slots of the power supply which is able to output a maximum of 600W. Table 3.2 shows the power modules used for the HMB along with their set voltage and maximum output power.

Table 3.2: Xcelsys Power Mods used in the HMB

Model	Set Voltage	Maximum output
XG7	12V	120W
XG3	6V	240W
XG2	-6V	200W

The Excelsys power supply sits on an outside shelf where each rail is fed through to an interior bus. A custom HV power supply, also on the exterior shelf of the HMB structure, provides HV to PMTs within the HMB structure. The HV is distributed by an array of SHV connectors which are in a parallel configuration and bypassed with a high voltage 0.01μF capacitor. Most of the components within the HMB structure require 6V to be powered, with the exception of the negative supply on-board the TARGETX Extended Range board, where -6V is needed, and the HV power supply which also needs 24V. Table 3.3 shows each component and breaks down the voltages needs. The power consumption in the table shows the maximum power each device may draw. It is shown that the components in the HMB will only draw 129.9W of power, this is well within the maximum the Excelsys is able to handle.

Figure 3.7 shows a block diagram of the Excelsys power supply and how power is distributed throughout the system. The red blocks are exterior to the system, where the blue blocks are interior. A power budget shows that the Excelsys power supply is more than capable of providing the power needed to the electronics.

Table 3.3: Maximum power draw from each component. TXDC is TARGETX daughter card

Device	Volts	Current	Power	QTY	Total
HV Power Supply	24V	2.7A	64.8W	1	64.8W
	6V	0.3A	1.8W	1	1.8W
	-6V	0.1A	0.6W	1	0.6W
HMBBMH	6V	0.4167A	2.5W	3	7.5W
MicroZed	6V	0.8A	4.8W	3	14.4W
TXGain	6V	0.8A	4.8W	2	9.6W
	-6V	0.1A	0.6W	2	1.2W
SCROD/TXDC	6V	2.5A	15W	2	30W
Total			94.9W		129.9W

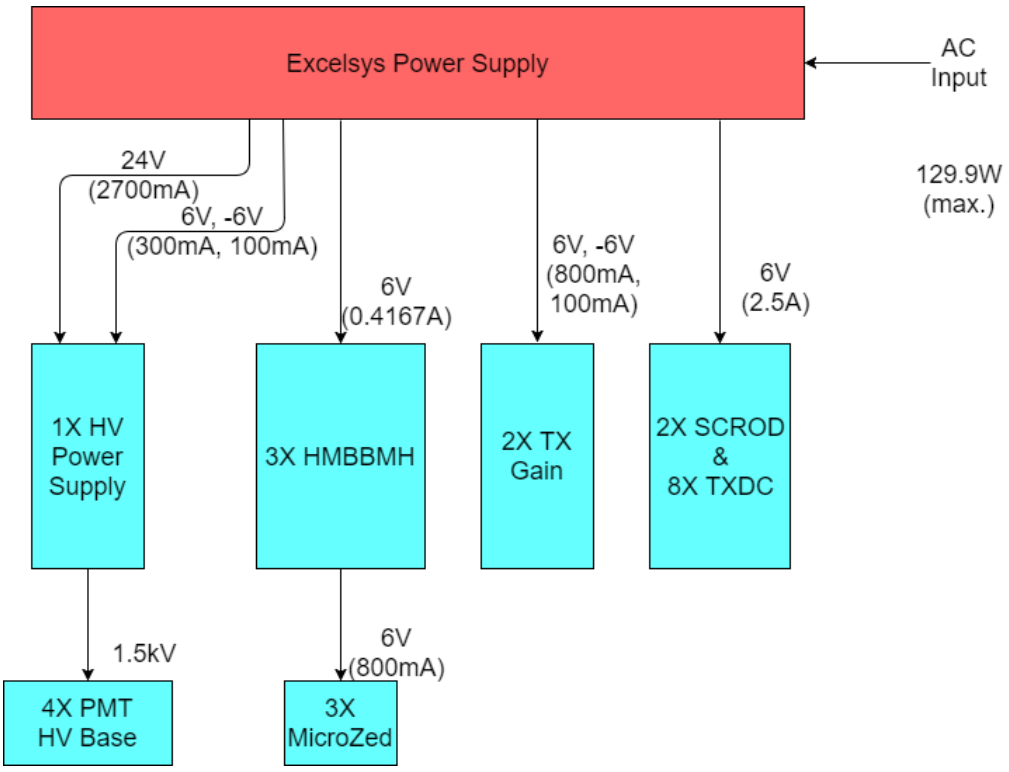

Figure 3.7: Power distribution of HMB components.

CHAPTER 4
RESULTS

4.1 HMB Commission Results

4.1.1 TARGETX Readout using MicroZed Board

Once a readout of the TARGETX was implemented on the MicroZed board, a first dataset was obtained in order to determine pedestals of each channel. For this test case, no signals were injected into the RF inputs of the TARGETX, rather each input was biased at a DC voltage of 2.2V where four windows of each channel was simultaneously read out. This was done for all 512 windows, taking a four channel readout 128 times. This needed to be done primarily because at the end of each 32 sample window, there is a sample ADC count with a value which deviates from the rest, these are always outliers. By taking 100 iterations of each window, the standard deviation of each sample value is approximately 3-4 ADC counts, the same goes for the outliers. Taking multiple iterations of each of the 512 windows, we could determine the mean value of each sample which could be subtracted from proceeding readings where the only components of the waveform is the injected signal along with its baseline. Therefore data taken on any window could be pedestal subtracted, thus getting rid of consistent outliers and noise, allowing a much cleaner waveform.

Figure 4.1 shows a histogram of raw, non-pedestal subtracted data taken from windows 8 - 23. It shows that the baseline has a mean value of approximately -2162mV or ADC counts (assuming 1 ADC count is approximately 1mV). A second peak at approximately -2265 ADC counts shows the mean value for the outliers. After applying pedestal subtraction to the sample values, we obtain the graph shown in Figure 4.2. This pedestal subtracted data shows the baseline of each channel close to zero, and without any outlier peaks.

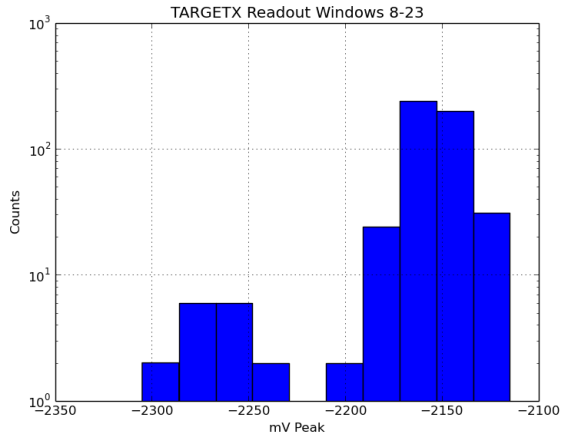

Figure 4.1: First TARGETX data readout using ZYNQ. Histogram shows non pedestal subtracted data from readout window 8 to 23.

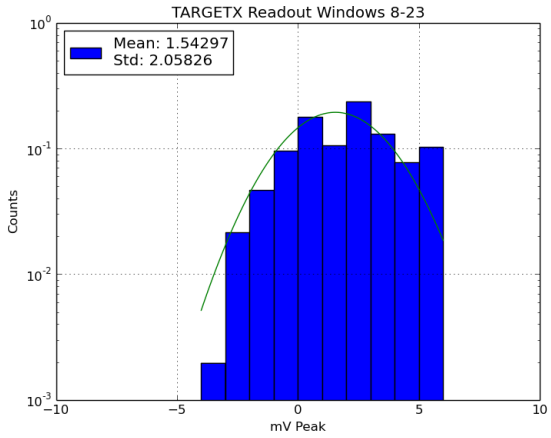

Figure 4.2: Histogram shows gaussian forming near baseline of zero for pedestal subtracted data.

Figure 4.3 shows a pedestal subtracted waveform from a four window readout from channel 10 (unity gain stage) of the TARGETX readout of the TARGETX Gain Board. Figure 4.4 shows a pedestal subtracted 64MHz sinewave readout from the same channel.

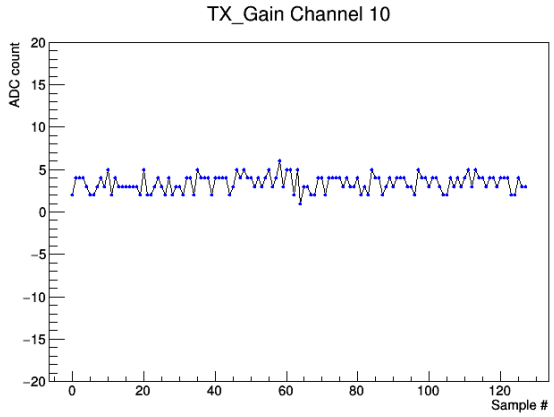

Figure 4.3: TARGETX readout of pedestal subtracted noise.

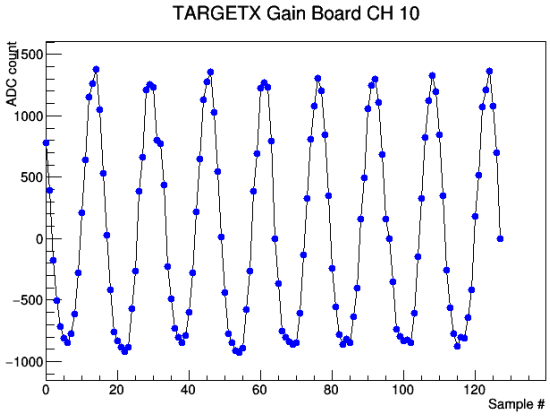

Figure 4.4: TARGETX readout of 64MHz pedestal subtracted sine wave.

The TARGETX is capable of issuing a self-trigger by the use of an internal comparator circuit. By setting an internal TARGETX DAC value, an RF input could be compared which will issue a trigger if the set value is either greater or lesser than an input pulse. By using the internal TARGETX trigger, the TARGETX Gain board could self-trigger according to threshold values set by software. Figure 4.5 shows a pulse which was triggered by the TARGETX.

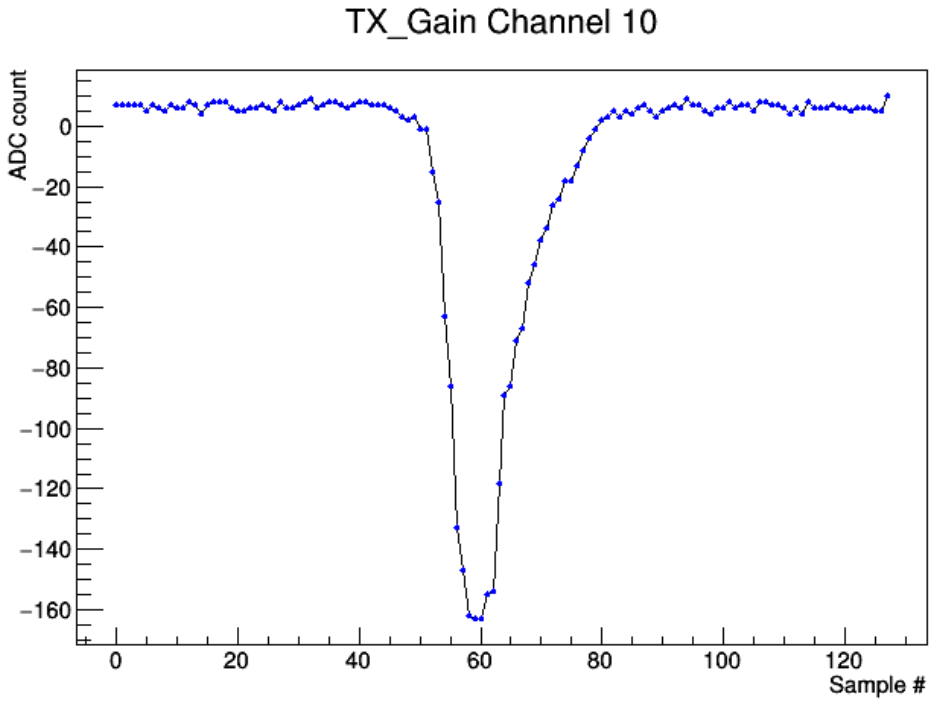

Figure 4.5: Pulse Triggered by TARGETX in unity gain stage.

4.1.2 TARGETX Gain Board Readout

The scope of this subsection is to document the outputs of each gain stages to determine how close actual gains are from the theoretical. Before proceeding to test results, Figure 4.6 shows results from simulation of the TARGETX Extended Range Board for the individual gain stages with an inverted 1mV pulse injected. The purple line shows the is 10^1 stage where we have an output pulse amplitude of 10mV, the red line is 10^2 with an output pulse amplitude of 100mV, and the blue line is 10^3 with an output pulse amplitude of 1000mV. The green lines which are the 10^4 and 10^5 stages are too large to input to the TARGETX, therefore the clamping stages protects the inputs. In this case all gain situations are ideal, the feedback passive components contain values with zero tolerances and there is no noise injected into the system.

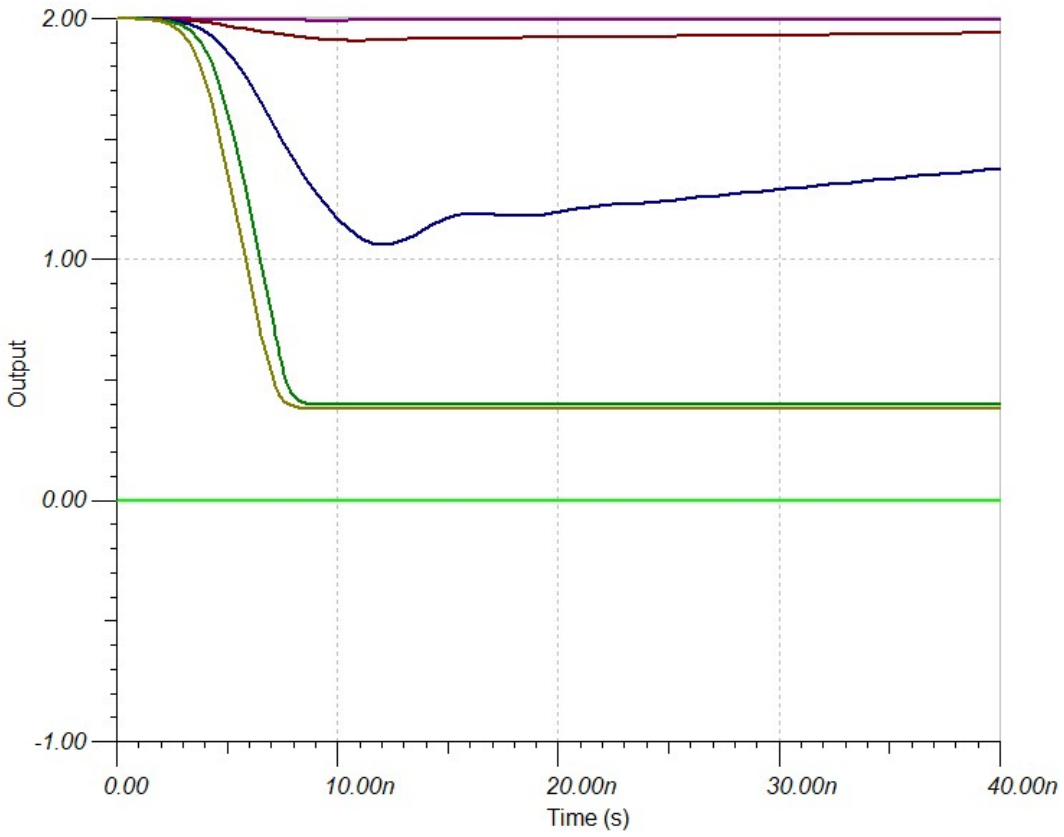

Figure 4.6: Simulation of gain stages with a 1mV inverted pulse inserted.

After assembly of the TARGETX Gain Board, each gain stage was tested by inputting a pulse similar to that of the PMT output from the calorimeter system. The mean output peak through each stage was then determined by the use of a peak finding algorithm where numerous values were then binned in order to plot a histogram. The data obtained from this test was from a scope probe, which introduced some noise. Because of the noise, the data was filtered through a butterworth filter in software before the peak finding algorithm was used.

In Figure 4.7 a histogram shows the mean of a 1Vp pulse at unity gain input of the TARGETX Gain board. Figure 4.8 shows a 10mVp pulse at a gain of 10^1. Although a mean peak of 100mV is expected, the feedback circuit on the non-inverting amplifier configuration are not tuned. For this stage, as well as the other stages on this board, further calibration will need to be done in order to obtain mean peaks at which is expected. Figure 4.9 shows a histogram of a 1mVp input pulse at a gain of 10^2 where the mean value is 94mV. Finally, Figure 4.10 shows a histogram of the same 1mVp but at a gain stage of 10^3. In this case, we obtain a mean value very close to 1Vp.

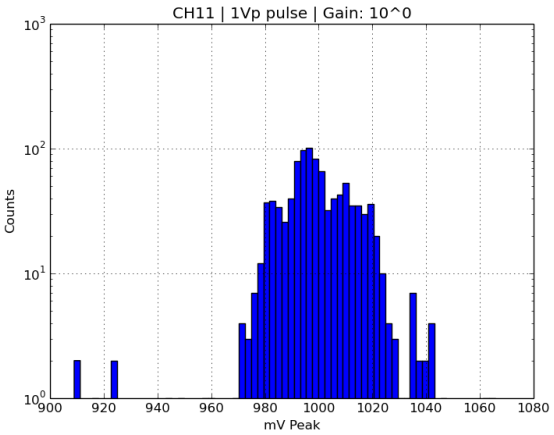

Figure 4.7: Histogram of 1Vp pulse at unity gain.

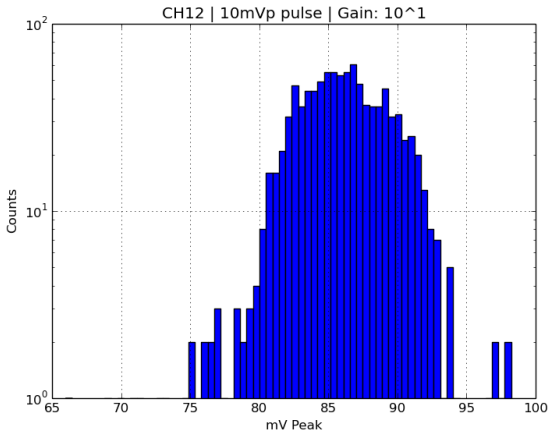

Figure 4.8: Histogram of 10mVp pulse at gain of 10.

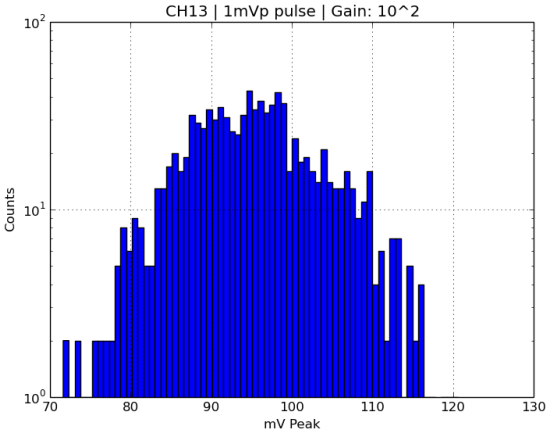

Figure 4.9: Histogram of 1mVp pulse at gain of 10^2.

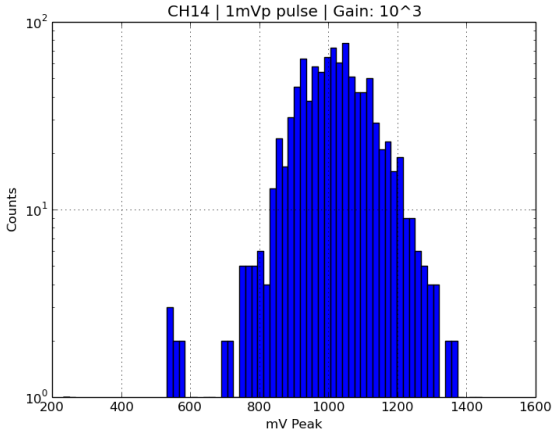

Figure 4.10: Histogram of 1mVp pulse at gain of 10^3.

After the test runs required for obtaining the above plots, it was concluded that the gain stages of 10^4 and 10^5 amplified too much noise which was inherent to the system to be of any use. In order to remedy this situation for possible future use of these gain stages, it is necessary to reduce the noise generated by the 5V regulator which is used to clamp the injected signal to the TARGETX.

4.1.3 HMB Enclosure Dark Tests

The following two plots shows histograms from dark tests within the HMB enclosure. A PMT system separate from the calorimeters was used for this test. The idea behind this test was to use PMTs in order to compare how dark the interior of the HMB enclosure is with both the outside

light off, and on. Ideally, by taking a histogram of dark current pulses of the PMT within the structure, in both situations, these plots should look the same. By looking at Figure 4.11 we see how the plot should look when there is no light entering the structure, this is with lab light, outside of the structure, off. Figure 4.12 shows a histogram with the outside light off. We see that the dark current height not distributed more evenly as it was with the outside light off. This change in data signifies that there is a slight light leak within the HMB structure which could be fixed by covering any known cracks.

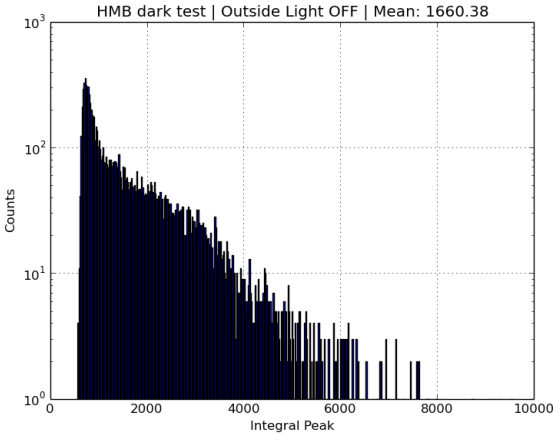

Figure 4.11: Histogram of peak height from dark currents of HMB dark test with outside light off.

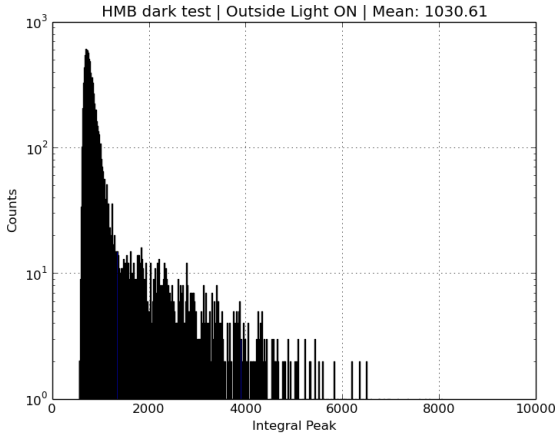

Figure 4.12: Histogram of peak height from dark currents of HMB dark test with outside light on.

CHAPTER 5
FUTURE WORK

Based off of the results, the next step to take with HMB would to calibrate the TARGETX Gain board. The mean values of the gain stages were close to the expected, but it may be ideal to tune the feedback circuit of the gain stages, as well as the voltage dividers in the attenuations stages. Also, in order to utilize the 10^4 and 10^5 gain stages, it will be necessary to replace the 5V voltage regulator with one that have less noise. Another area of improvement would be with the firmware.

Once tweaks are made, a final integration of all the components of the HMB system will allow reconstruction of a muon and the ability to compare the detected beam-line with a DUT. After the final integration of HMB, a third detector system will be built which will allow momentum measurement of a muon. A momentum spectrometer will be built and placed below the HMB system (shown in Figure 5.1). It consists of two sets of Dual-sided Silicon Strip detectors (DSSD) above and below a 0.5 T permanent magnet. The magnet curves the trajectory of a passing particle, and the DSSDs tracks the new trajectory. The radius of the curved path is related to the momentum of the particle. When a particle passes through one of the strips on the DSSD a voltage is induced on the strip. The trajectory of the particle is determined by locating voltage pulses on the DSSDs. The Viking Architecture One (VA1) chip is used to amplify and readout the voltage pulses from the detectors. Each detector has two VA cards consisting of five daisy-chained VA1 chips. The DSSD Data Acquisition (DAQ) system interfaces the VA1 chips to the PC. It also supplies power and amplifier control biases to the VA1.

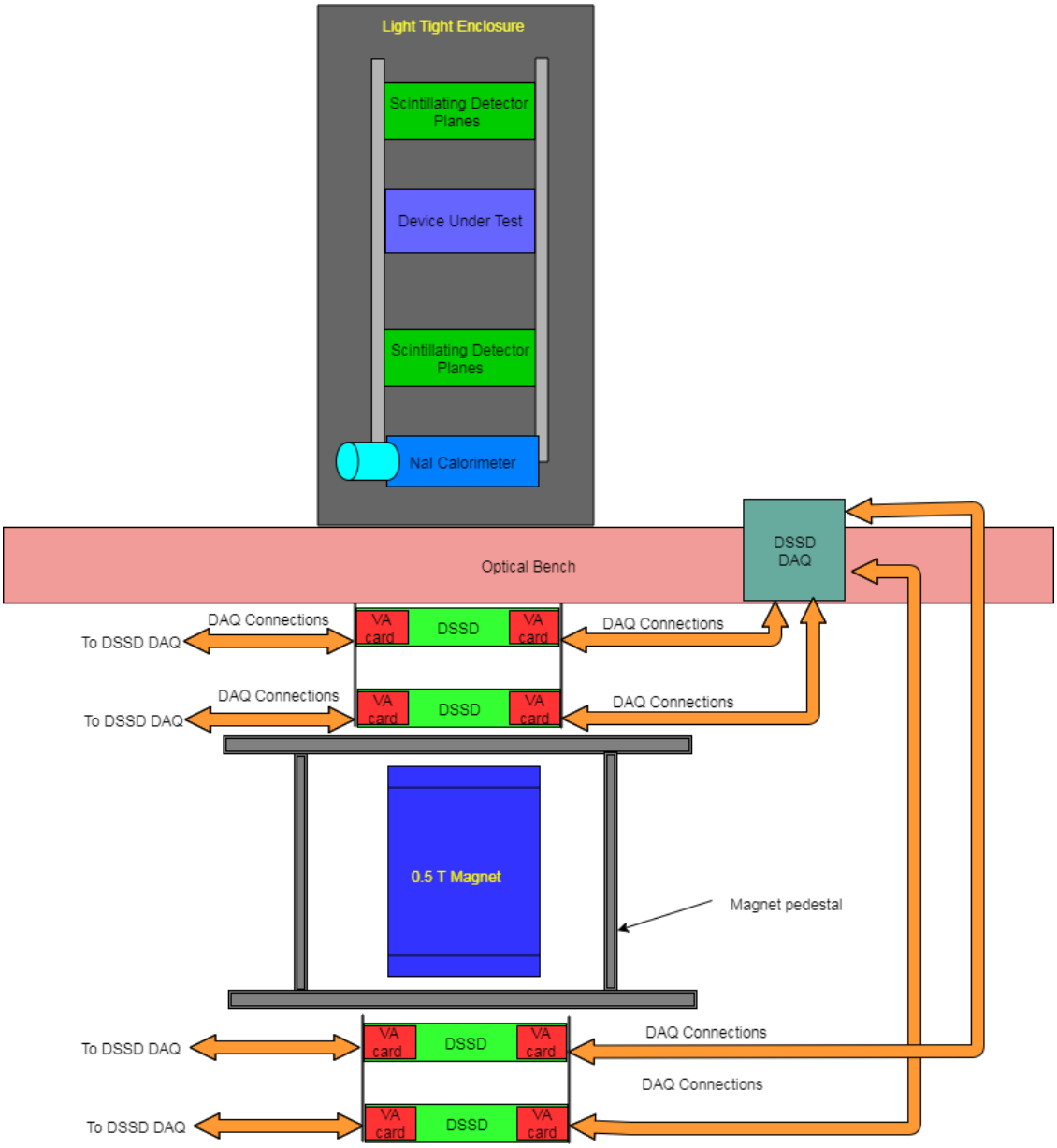

Figure 5.1: Future addition of a momentum spectrometer system shows dual-sided silicon strip detectors above and below a 0.5T magnet.

CHAPTER 6
CONCLUSION

The HMB went from concept, to design, to actual components in which are needed for a fully realized system. A TARGETX Extended Range board was built which offers a total of 8 gain stages from 10^{-2} to 10^{5}. An HMBBMH board which could be used as an interface to the TARGETX Extended Range board as well as a CDT board which distributes a common clock and handles decision logic. Working firmware which is able to readout the TARGETX chip from the TARGETX Extended Range board. And finally, the rest of the system which will allow final integration of all the components, including the PVT scintillation detector planes which will be responsible for reconstruction of a muon incident within HMB.

In conclusion, the components realized in this Thesis will provide HMB the tools in which it needs in order to fully realize a muon detector which will allow in-house detector testing. Integration of the final components, as mentioned in the future research section, will continue as a full muon reconstruction is not far off.

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