# Micro-fabrication and Characterization of Highly Doped Silicon-Germanium Based Thermoelectric Generators


Francesco Mirando

School of Engineering
University of Glasgow

Submitted in fulfilment of the requirements
for the degree of Doctor of Philosophy (Ph.D.)

December 2017

# Abstract

Over the last decades of research on sustainable energy, thermoelectric generation has been identified as a potential energy harvesting solution for a wide range of applications. Nowadays, the commercial thermoelectric technology is almost entirely based on tellurium alloys, it mainly addresses room temperature applications and it is not compatible with MEMS and CMOS processing.

In this work, silicon-germanium based micro-devices have been designed, developed and characterized with the aim of addressing the heat recovery needs of the automotive industry. The micro-scale of the fabricated devices, together with the full compatibility with silicon micro-processing, also profiles an interesting potential for application in the autonomous sensor field. Most importantly, the configuration and the fabrication processes of such silicon-based generators constitute a platform to transfer the results of decades of promising material investigations and engineering into practical micro-scaled thermoelectric generators.

The room temperature characterization of the manufactured micro-generators revealed power factors up to $13.9\times10^{-3}$ µW/(cm$^2$K$^2$) and maximum output power density up to 24.7 µW/cm$^2$. In such temperature range, the micro-devices manufactured in this work are still not as performing as the state-of-the-art bismuth-telluride based technology. However, at around 300 °C, the developed micro-modules are predicted to produce a maximum power output of 1.2-1.5 mW under 10 °C temperature gradient, which corresponds to 35-45% of the room temperature performance of the only commercial bismuth telluride based micro-devices.

The results show that silicon-germanium micro-modules could potentially compete with the state-of-the-art commercial micro-devices, being better performing at higher temperature, but also offering the advantage of being a sustainable MEMS and CMOS compatible option for autonomous sensors integration.

# Acknowledgments

First and foremost, I would like to thank my supervisors: Prof. Douglas Paul and Prof. Andy Knox. Thanks for giving me the opportunity to collaborate to the present ETP project, making this PhD possible. Thanks for your continuous support during these four years, you really helped me becoming a more mature scientist.
Dr. Lourdes Ferre Llin, I will never be able to thank you enough for all the support you offered me during these years. Thanks for your genuine patience and giudance, and thanks for the long thermoelectric chats.
Despite I worked with Dr. Antonio Samarelli only for a short time of my PhD, I still had the opportunity to glean precious suggestions from his jumbo nanofabrication knowledge. Thanks for all your technical hints, for being a sincere friend and for stimulating my reaserch interests.
Thanks to Dr. Andrea Montecucco, Dr. Jonathan Siviter, Dr. Paul Mullen, Matt Garland and Marcos Compadre, your guidance in device characterization is invaluable and the moments we shared at the thermolectric conferences are memorable.
Dr. Kevin Gallacher and Dr. Ross Millar, thanks so much for introducing me to micro-Raman spectroscopy and for your precious suggestions and encouragement.
A big thanks to my friends and office mates, I could spend pages thanking you all for the most various reasons, but I am sure that you know who you are and what we shared. Cheers guys.
Thanks to my family for the continuous support in every moment of my life.

# Preface

The work presented in this Thesis has culminated in the following journal publications and conference proceedings:

1. **Mirando, F.**, Ferre Llin, L. and Paul, D.J., "Microfabrication and Characterization of Highly Doped Silicon-Germanium Based Micro Thermoelectric Modules", *The 10th International Conference on Silicon Epitaxy and Heterostructures (ICSI-10)*, Warwick (UK), 14-19 May 2017.

2. Ferre Llin, L., **Mirando, F.**, Samarelli, A., Odia, A., Cecchi, S., Etzelstorfer, T., Muller Gubler, E., Charastina, D., Isella, G., Stangl, J., Weaver, J.M.R., Dobson, P.S. and Paul, D.J., "The Use of Silicon-Germanium Superlattices for Thermoelectric Devices and Microfabricated Generators", *ECS Transactions*, 2016, 75, (8), p.469-478.

3. **Mirando, F.**, Ferre Llin, L. and Paul, D.J., "Highly Doped Silicon-Germanium Microfabricated Thermoelectric Modules for 500 °C Operation", *Energy Technology Partnership Annual Conference*, Aberdeen (UK), 3 November 2016.

4. **Mirando, F.**, Ferre Llin, L. and Paul, D.J., "Design and Microfabrication of Highly Doped Silicon-Germanium Thermoelectric Modules for 500 °C Operation", *14th European Conference on Thermoelectricity (ECT2016)*, Lisbon (Portugal), 20-23 September 2016.

5. **Mirando, F.**, Ferre Llin, L. and Paul, D.J., "Highly Doped Silicon-Germanium Thermoelectric Module: Design and Fabrication", *ICT - Energy Science Conference 2016*, Aalborg (Denmark), 16-19 August 2016.

6. **Mirando, F.**, Samarelli, A., Nandhakumar, I., Naylor, A.J., Burton, M. and Paul, D.J., "Thermoelectric Characterisation of Electrochemically Deposited Bismuth Telluride Materials by Microfabricated Resistive Thermometry", *ICT-Energy Letters*, 2016, 11, p.15-16.

7. **Mirando, F.**, Ferre Llin, L. and Paul, D.J., "Microfabrication of Thermoelectric Devices", *Energy Technology Partnership Annual Conference*, Glasgow (UK), 22 October 2015.

8. **Mirando, F.**, Samarelli, A., Nandhakumar, I., Naylor, A.J., Burton, M. and Paul, D.J., "Thermoelectric Characterisation of Electrochemically Deposited Bismuth Telluride Materials by Microfabricated Resistive Thermometry", *ICT - Energy International Doctoral Symposium*, Bristol (UK), 16 September 2015.

9. **Mirando, F.**, Samarelli, A., Nandhakumar, I., Naylor, A.J., Burton, M., Khouharenko, E., White, N.W. and Paul, D.J., "Thermoelectric Characterisation of Electrochemically Deposited Bismuth Telluride Materials", *12th European Conference on Thermoelectricity (ECT2014)*, Madrid (Spain), 23-28 September 2014.

# Contents

# List of Figures

# List of Tables

# Abbreviations and Symbols

## Acronyms

| | |
|---|---|
| TEG | ThermoElectric Generator |
| IoT | Internet of Things |
| CMOS | Complementary Metal-Oxide-Semiconductor |
| MEMS | Micro-Electro-Mechanical Systems |
| ETP | Energy Technology Partnership |
| JWNC | James Watt Nanofabrication Centre |
| $\mu$TEG | Micro-scaled ThermoElectric Generator |
| CVD | Chemical Vapor Deposition |
| MOCVD | Metal-Organic Chemical Vapor Deposition |
| PVD | Physical Vapor Deposition |
| RTG | Radioisotope Thermoelectric Generator |
| BiCMOS | Bipolar Complementary Metal-Oxide-Semiconductor |
| SIMS | Secondary Ion Mass Spectrometry |
| SRP | Spreading Resistance Profiling |
| SOI | Silicon On Insulator |
| TLM | Transfer Length Method |
| CTLM | Circular Transfer Length Method |
| SThM | Scanning Thermal Microscopy |
| TDTR | Time Domain ThermoReflectance |
| CCD | Charged Coupled Device |
| FEM | Finite Element Method |
| SEM | Scanning Electron Microscope |
| PECVD | Plasma-Enhanced Chemical Vapor Deposition |
| RF | Radio Frequency |
| RIE | Reactive Ion Etching |

| | |
|---|---|
| ICP | Inductively Coupled Plasma |
| PECVD | Plasma-Enhanced Chemical Vapor Deposition |
| EDX | Energy Dispersive X-Ray |

# Symbols

| | |
|---|---|
| $\alpha$ | Seebeck coefficient |
| $\Pi$ | Peltier coefficient |
| $\beta$ | Thomson coefficient |
| $\eta$ | Efficiency |
| $ZT$ | Figure of merit of thermoelectrics |
| $Bi_2Te_3$ | Bismuth Telluride |
| $Sb_2Te_3$ | Antimony Telluride |
| $PbTe$ | Lead Telluride |
| $GeTe$ | Germanium Telluride |
| $SnTe$ | Tin Telluride |
| $SiGe$ | Silicon Germanium |
| $GaAs$ | Gallium Arsenide |
| $Si_3N_4$ | Silicon Nitride |
| $SiO_2$ | Silicon Dioxide |
| $CO_2$ | Carbon Dioxide |

# Chapter 1

# Introduction

## 1.1 Motivation

In recent decades, the world's increasing demand for energy, in conjunction with the alarming impact that the combustion of fossil fuels has on global climate change, has raised a social and political debate about the sustainability of energetic systems.
In this respect, the European Union developed the Europe 2020 strategy aiming at overcoming structural weaknesses in the continental economy by subsidizing smart (based on knowledge and innovation), sustainable (more resource efficient) and inclusive (promoting economic, social and territorial cohesion) growth. The provision aims at reducing greenhouse gas emissions by at least 20% compared to 1990 levels (Figure 1.1), increasing energy consumption from renewable energy sources by 20% and increasing energy efficiency by 20%. The transition towards a resource efficient and low-carbon economy would enhance competitiveness and promote energy security by decoupling economic growth from resource and energy use.
The landmark definition of sustainable energy was provided in 1987 by the United Nations Brundtland Commission in the "Our Common Future" report [1]. In such agenda, the World Commission on Environment and Development formulated criteria that an energy source is required to meet to be considered sustainable:

1. The energy source is not significantly depleted by continuous use;
2. The energy generation does not cause significant pollution or hazards to humans, ecology or climate systems;
3. The energy generation does not cause significant perpetuation of social injustice.

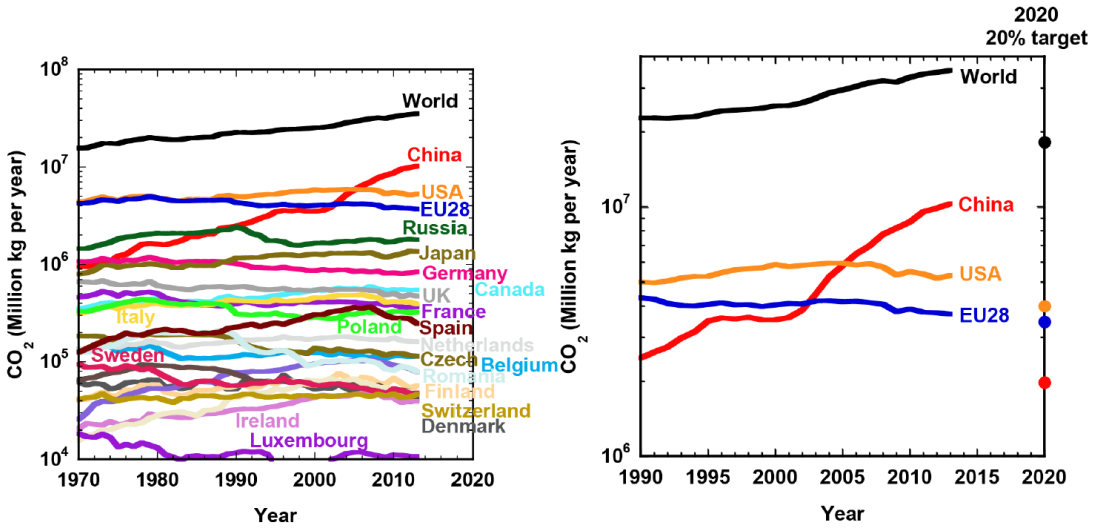



Figure 1.1: Carbon dioxide ($CO_2$) emission per year for the European countries and the major world economies [2].

Renewable energy generation represents a sustainable way to effectively reduce carbon emissions; however, most of these energy technologies present high capital cost and have long payback periods. Moreover, many renewable sources cannot guarantee constant supply of energy and require to be combined with storage and/or alternative power supply mechanisms. The storage of large amounts of energy is really problematic, with only pump-hydro storage being able to address the task in a sustainable manner. At a smaller scale, batteries and super-capacitors instead represent a valuable storage option. Thereby, while a fundamental part of research focuses on renewable energy power generation, a parallel approach consists of integrated systems capable of harvesting wasted energy.

As an example, the U.S. Department of Energy reported that only about 14% to 30% of the fuel energy is used to move a vehicle down the road; while the rest of it is lost to engine and driveline inefficiencies (68% - 72%) and used to power accessories [3], Figure 1.2. Most of the multinational companies in the automotive sector already demonstrated interest in improving vehicle efficiency, also motivated by the more stringent international regulations on $CO_2$ emissions. Energy harvesting solutions, in particular those based on heat pipes and ThermoElectric Generators (TEGs), are currently attracting a vast interest due to their potential of improving vehicle efficiency by recovering wasted heat and consequently reducing the load on the shaft-driven alternator. Both thermoelectrics and heat pipes are solid state, silent, scalable and durable technologies, which are thereby suitable for automotive applica-

tions. As a matter of fact, General Motors recently reported up to 5% fuel economy improvements in vehicles thanks to the assistance of thermoelectric units [4]. Moreover, Freedom Car, a research initiative funded by the US Government, is aiming at an impressive fuel economy improvement of 10% [5]. Thermoelectric systems could indeed be integrated in vehicles to power the various electrical accessories. The air conditioning unit can be taken as an example. An air conditioning unit generally consumes around 3 l of fuel every 100 km. In the assumption that a vehicle covers 10 000 km every year, the air conditioner itself would consume about 300 l of fuel, which corresponds to 500-700 kg of $CO_2$ emissions. Such fuel consumption and carbon dioxide emission could be avoided by implementing thermoelectric based energy recovery systems to power the air conditioning unit as well as headlamps, parking lights, wipers and other vehicle electrical equipment. These units are conventionally powered by batteries charged by the shaft-driven alternator. Replacing the current vehicle alternator technology is a challenging task as a shaft-driven alternator has the ability to provide high power whenever the vehicle is moving, while thermoelelctric systems require a warm-up time before being able to produce electricity. Attempts to develop TEGs systems mounted on the exhaust stream of a vehicle have already been undertaken [6–10] and will be reviewed in the following Chapter.

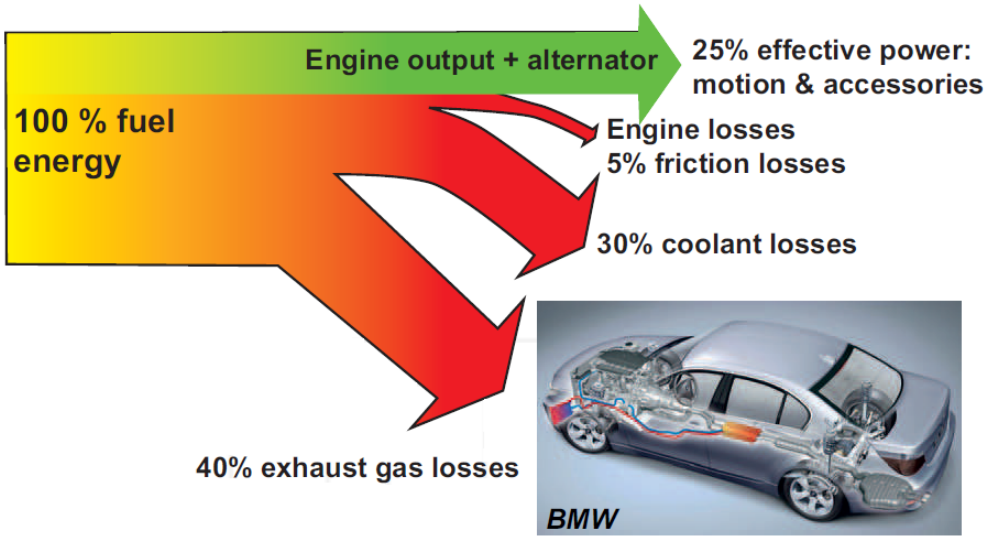



Figure 1.2: Schematic diagram of the distribution of the energy generated from the vehicle fuel combustion [11].

The exhaust line of any vehicle consists of a series of emission control and sound attenuation components (i.e. catalytic converter, particulate filter, silencers or mufflers). The temperature of exhaust gas gradually decreases moving away from the engine manifold. The latter can reach temperatures up to 1000 °C. At the catalytic converter, the exhaust gases have temperature in the range of 300 - 500 °C. At the exhaust muffler the temperature further drops to around 150-300 °C. Hence, different TEG systems can be designed for different operating conditions and installed on each element of the exhaust stream. However, there are a number of challenges to the integration of TEGs in vehicles. The thermoelectric efficiency of TEGs is dependent on temperature and it peaks at nearly the melting point of the thermoelectric material in use. The continuous operation at around melting point leads to degradation of the thermoelectric material defeating the purpose of the installation. Moreover, TEG materials are hard and brittle; thus, vibrations and thermal loading may cause cracks which decrease the electrical properties and ultimately the efficiency of the TEGs. Finally, another major challenge is represented by the implementation of an efficient cooling of the cold side of the TEGs. The cooling unit for the TEGs systems could be merged with existing engine cooling unit, but it would introduce additional cost and make the system more complex.

Like automotive, every other system (semiconductor devices, computing systems, data-centers, industrial foundries, photovoltaic power plants, human bodies, etc.) have available waste heat that could be converted to electricity through the application of TEGs. In particular, in the age of the Internet of Things (IoT), these scalable solid-state energy converters could represent a sustainable miniature power supply for wearable electronics, bio-integrated systems, cybernetics and others.

Indeed, ambient intelligence devices, various sensor networks for safety and environmental monitoring, and implantable medical sensors all require powering systems. Wiring can often be expensive and inconvenient, batteries need regular replacement and RF-powering is limited by operating distance. The typical power consumption of different electronic devices and systems is schematically reported, and compared to the power that can be sustainably generated, in Figure 1.3. The modern CMOS-based sensors can operate at low power levels, ranging from 1 µW to 10 µW at frequencies of around 100 kHz. Radio transmitters generally require about 1 mW, but burst transmission can further reduce minimum average power required. An energy harvester, capable of delivering a few µW into a battery or a capacitor, would immediately gain access to a number of applications and most importantly it would boost the development of even lower power devices, opening the way to the autonomous nanoscale

systems for implants and in vivo health monitoring, environmental warning and hazard detection.

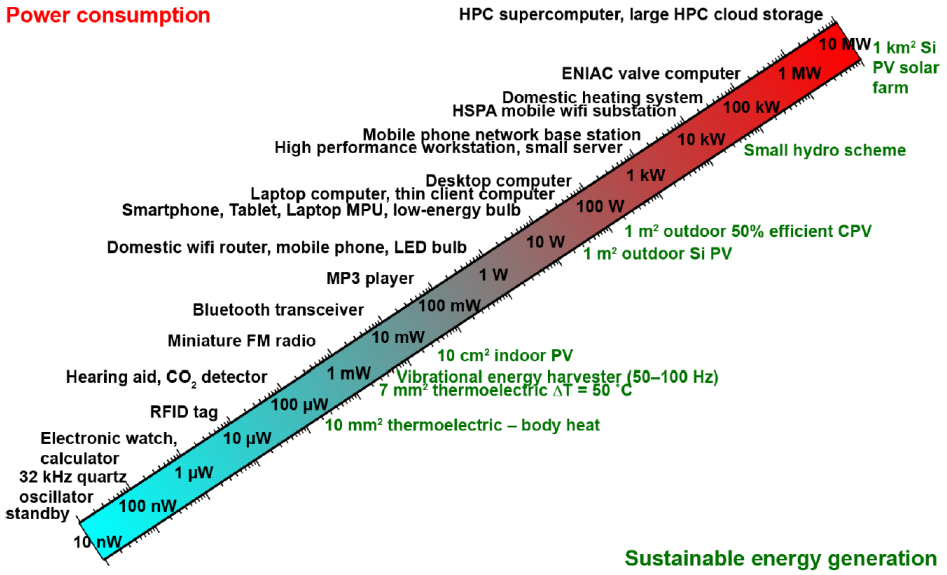



Figure 1.3: Typical power consumption of different electronic devices and systems versus the power that can be sustainably generated [11].

Due to their finite lifetime, disposable batteries are not a feasible solution in the computing dream of "wireless autonomous sensors everywhere". Rechargeable batteries could instead fit in an hybrid energy source which combines harvesting and storage. The convenience of hybrid devices is also highlighted by the comparison between the energy density per unit weight or volume of state-of-the-art batteries and energy harvesters, with the first being an order of magnitude better. The device size also needs to be reduced in order for the hybrid energy elements to match the footprint/volume of the powered sensor.
Ultimately, an ambitious target scenario for hybrid energy harvesting systems is represented by the roadmap for microbattery energy storage, Figure 1.4. Over the next 10-15 years, the energy supply components, harvesting and storage, are expected to be integrated on chip occupying a $1\,mm^2$ footprint, an area which is no larger than the one of the powered electronics.

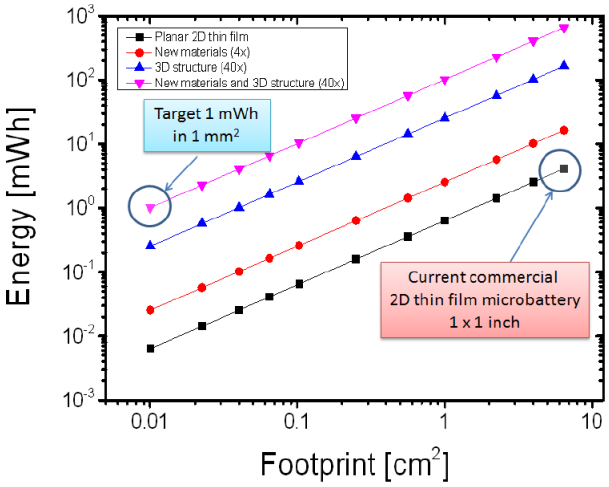



Figure 1.4: A roadmap for microbattery energy storage targeting the ability of delivering 1 mW h of energy with a 1 $mm^2$ footprint [11].

Among energy harvesting technologies, thermoelectrics constitute an attractive option as scalable, mechanically robust, without moving parts or need of maintenance, and operational over a wide range of temperatures.
The only commercial micro-scaled thermoelectric modules are currently based on tellurium alloys and mainly address room temperature applications with an 18% Carnot efficiency and a maximum output power density per degree of 1.12 $mW/cm^2K$ [12]. Moreover, the state-of-the-art bulk thermoelectric devices often adopt rare (i.e. tellurium is the 9th rarest element on earth) and toxic (i.e. tellurium, bismuth, lead, antimony) materials, hence the interest in more sustainable materials with comparable, if not improved, efficiency is growing in order to fill the technology gap.
Many fields of technological research such as electronics, photonics and more recently energy harvesting already focused particular attention on silicon, germanium and silicon-germanium alloys due to improvements in growth and fabrication capabilities. High quality epitaxial materials and well-established cost-effective low-dimensional fabrication are the technological strengths that, together with sustainability and complete integrability with Complementary-Metal-Oxide-Semiconductor (CMOS) and Micro-Electro-Mechanical Systems (MEMS), have captured the attention of the energy harvesting field.
Silicon-germanium alloys indeed show the best thermoelelctric efficiency at very high temperature (above 900 K) and have been successfully utilized in bulk radioisotope TEGs for space applications since the 1980s [13, 14]. However, these materials have reduced performances at lower temperatures and hence they need to be engineered

in order to be cost effective and compete in the market of integrated cooling and energy harvesting modules for electronic devices, automotive applications, solar cells and autonomous systems.

## 1.2 Aim of the Thesis

This Ph.D. was funded by the Energy Technology Partnership (ETP) with the aim of developing micro-fabricated devices for energy harvesting applications.
ETP is an alliance of Scottish Universities engaged in world class research across the different energy sectors: oil and gas, power generation, renewables and energy harvesting [15]. Over the years, ETP established strong industrial connections throughout the UK with the vision of commercially delivering new technologies. The research supported by ETP indeed covers all the aspects of R&D, from preliminary feasibility studies to commercial deployment through testing and development.
The partners involved in this project are European Thermodynamics Limited and the University of Glasgow. The collaborators mainly aimed at developing micro-devices designed to address the heat recovery needs of the automotive industry. In particular, the micro-devices targeted the operating conditions characteristic of a TEG system installed on the catalitic converter of the vehicle. In such region, the temperature of the exhaust gas is in the range of 300 - 500 °C. Moreover, the design of the micro-modules had to guarantee mechanical robustness to the vibrations, induced by both road surface and engine excitation, of the exhaust line. The automotive sector could indeed constitute the application driver to increase the manufacture volume and widespread use of thermoelectric devices. However, the micro-scale of the fabricated devices also profiles the potential for autonomous sensor applications.
Over the last decade, the focus of the thermoelectric field has been mostly directed towards the investigation of novel materials with exceptionally promising figures of merit. Despite such claims, almost none of these materials have been employed in the development of micro-scaled TEGs. Transforming lab records of preliminary measurements into reliable thermoelectric generator modules is indeed very challenging.
This project utilizes silicon-germanium wafers, the advantages of which have already been mentioned, to close the gap between research lab values and modules. The main aim is to develop a reliable and repeatable process for the fabrication of micro thermoelectric generators, with the expectation to transfer it to industrial manufacturing.
The ultimate vision of the project would be to build experience and knowledge to

support the mass production of micro-scaled thermoelectric devices.
The project started with the review of thermoelectric materials that could be suitable for the desired automotive application and for micro-processing. Silicon-germanium in wafer format was chosen for this work and the material was bought commercially from IQE Silicon Compounds [16]. The thermoelectric characterization of the p- and n-type materials was performed and low resistivity Ohmic contacts, which are stable over the temperature range of interest, were developed. Subsequently, with the values extracted from characterization, the micro-device was modeled in order to identify the geometry that would maximize the electrical performance under specific operating conditions. A flip-chip assembly based fabrication process was then developed for the reliable realization of micro-TEGs. This phase of the project was possible thanks to technologies available in the James Watt Nanofabrication Centre (JWNC), the support of its technical staff and the knowledge exchange among the users of the centre. Finally, the testing of the fabricated micro-devices was performed using a fully automated thermo-mechanical test rig with the technical support of Thermoelectric Conversion Systems Limited [17].
The work carried out throughout the project tackles the necessary steps to achieve the specific and ambitious aims of this Ph.D.:

- Developement of thermally stable electrical Ohmic contacts with low specific contact resistivity to the silicon-germanium highly doped material to minimise resistive losses and Joule heating effects in the micro-module.
- Design of a micro-scaled thermoelelctric generator which is able to address the heat recovery needs (mechanical robustness and thermal stability at 300-500 °C) characterizing the automotive application.
- Development of a contact metallization which is flip-chip assembly compatible and thermally stable over the expected operating temperature range (300-500 °C).
- Development of a complete, repeatable and reliable fabrication process for micro-scaled TEGs which is compatible with current industrial manufacturing capabilities.
- Complete thermoelectric testing of the micro-fabricated modules to understand performance and reliability of the developed technology.

## 1.3 Thesis Outline

This section outlines the organization of the Thesis by introducing the content of each chapter.

Chapter 2 introduces thermoelectricity and offers an overview of the most successfully used materials for the fabrication of thermoelectric modules. The performance and application of the most relevant devices in literature are also reported.
Chapter 3 briefly presents the silicon-germanium alloys used in this work. Crystal structure, strain related phenomena and thermoelectric properties of the material are indeed introduced and the epitaxial growth mechanism is delineated.
Chapter 4 provides a description of the methods employed to characterize the silicon-germanium alloys together with the respective acquired measurements.
Chapter 5 presents the modeling undertaken to design the silicon-based micro TEG. The device layout consequently adopted for fabrication is also explained.
Chapter 6 describes the micro-fabrication tools and techniques employed to realize the thermoelectric devices developed in this work.
Chapter 7 presents the characterization of the micro-fabricated modules. Electrical testing and thermoelelctric characterization are performed on several micro-devices and the analyzed data are presented and commented.
Chapter 8 summarizes the results achieved within this Ph.D. work and offers suggestions for future work and further optimization of the devices.

# Chapter 2

# Thermoelectricity: Principles and State of the Art

## 2.1 Thermoelectric Effects

Thermoelectric phenomena involve the direct conversion between thermal and electrical energy [18]. The Seebeck, Peltier and Thomson effects are the common way to exploit thermoelectricity.

The generation of electrical energy from thermal energy was originally discovered in 1822 by T.J. Seebeck. The German physicist demonstrated for the first time that a temperature gradient across two points in a conductor, or semiconductor, material produces a voltage difference across them. The Seebeck coefficient, $\alpha$, is thereby defined as the ratio between the voltage sensed, $\partial V$, and the existent gradient of temperature, $\partial T$:

$$\alpha = -\frac{\partial V}{\partial T} \tag{2.1}$$

A decade later, in 1834, J. Peltier demonstrated the use of an electric current to pump heat. Indeed, a change in temperature of either junction of a thermocouple is observed when an electric current is driven through a it. The Peltier coefficient, $\Pi$, is defined as the ratio of the heat flux, $Q$, and current, $I$:

$$\Pi = \frac{Q}{I} \tag{2.2}$$

However, it was not until 1850s that W. Thomson, better known as Lord Kelvin, realized that the gradient of the heat flux across a thermocouple is proportional to both the electric current and the temperature gradient:

$$\frac{\partial Q}{\partial x} = \beta I \frac{\partial T}{\partial x} \tag{2.3}$$

where $\beta$ is the Thomson coefficient.
Furthermore, Lord Kelvin related the physics of the Seebeck and Peltier effects and, in the so named Kelvin relationships, he described the correlation between the two effects:

$$\Pi = \alpha T \tag{2.4}$$

and

$$\beta = T\frac{\partial \alpha}{\partial T} \tag{2.5}$$

## 2.2 Thermoelectric Power Generation and Efficiency

Thermodynamic efficiency for both thermoelectric generators and coolers was first demonstrated by E. Altenkirch in 1911 [19, 20]. For a thermoelectric generator, the thermodynamic efficiency is defined as the ratio of the power supplied to the load and the heat absorbed at the hot junction.
Figure 2.1 presents the equivalent electrical circuit of a thermoelectric generator, for clarity represented by a single p-n junction, connected in series with a resistive load.

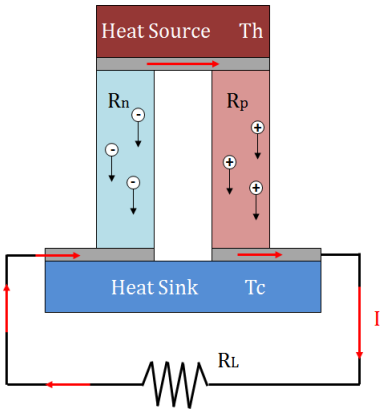



Figure 2.1: Schematic diagram of a single leg-pair thermoelectric module connected to a purely resistive load.

The power supplied to the load corresponds to the Joule heating of the resistor itself. From Ohm's law for the circuit, the current results:

$$I = \frac{(\alpha_p - \alpha_n)(T_h - T_c)}{R_L + R_p + R_n} \tag{2.6}$$

where $T_h$ and $T_c$ are respectively the temperatures of the hot and the cold heat sinks, $R_p$ and $R_n$ are the resistances of the p- and n-type semiconductor materials, $\alpha_p$ and $\alpha_n$ are the respective Seebeck coefficients and $R_L$ is the load resistance. According to Joule's law, the power delivered to the resistor results:

$$P_L = I^2 R_L = \left( \frac{(\alpha_p - \alpha_n)(T_h - T_c)}{R_L + R_p + R_n} \right)^2 R_L \tag{2.7}$$

On the other hand, from the superposition of one-dimensional Fourier heat transport, Peltier effect and Joule heating, the heat absorbed from the hot source corresponds to:

$$P_S = (\alpha_p - \alpha_n) I T_h + \frac{(\kappa_p + \kappa_n) A (T_h - T_c)}{L} - \frac{1}{2} I^2 (R_n + R_p) \tag{2.8}$$

where $\kappa_p$ and $\kappa_n$ are the respective thermal conductivity of the two semiconductor legs, while $L$ and $A$ are the length and the cross-sectional area of the thermoelectric legs. Combining equation 2.7 and equation 2.8, the efficiency of the system can be calculated:

$$\eta = \frac{P_L}{P_S} = \frac{\left( \frac{(\alpha_p - \alpha_n)(T_h - T_c)}{R_L + R_p + R_n} \right)^2 R_L}{(\alpha_p - \alpha_n) I T_h + \frac{(\kappa_p + \kappa_n) A (T_h - T_c)}{L} - \frac{1}{2} I^2 (R_n + R_p)} \tag{2.9}$$

The maximum efficiency can be derived by solving equation 2.9 for $\frac{d\eta}{d\left(\frac{R_L}{R_L + R_p + R_n}\right)} = 0$; resulting:

$$\eta_{max} = \left( 1 - \frac{T_c}{T_h} \right) \frac{\sqrt{1 + ZT} - 1}{\sqrt{1 + ZT} + \frac{T_c}{T_h}} \tag{2.10}$$

where $T = \frac{1}{2}(T_h + T_c)$ and $ZT$ is the figure of merit of thermoelectrics. The latter can be expressed as:

$$ZT = \frac{\alpha^2 \sigma}{\kappa} T \qquad \text{for single material} \tag{2.11}$$

$$ZT = \frac{(\alpha_p - \alpha_n)^2}{\left( \sqrt{\frac{\kappa_p}{\sigma_p}} + \sqrt{\frac{\kappa_n}{\sigma_n}} \right)^2} T \qquad \text{for the thermocouple} \tag{2.12}$$

The first part of equation 2.10, $\left(1 - \frac{T_c}{T_h}\right)$, corresponds to the Carnot efficiency; while the second part accounts for the losses and irreversible processes, which reduce as the dimensionless figure of merit, $ZT$, increases in value.

Figure 2.2 illustrates the comparison between the Carnot efficiency and the maximum thermoelectric efficiency calculated for different values of $ZT$ as function of $T_h$. It clearly appears that, at large power scales, thermoelectrics are less efficient

than Rankine or Stirling cycle engines. At smaller scale, below about 100 W, turbulence and viscous effects in fluids become dominant and the efficiency of Rankine and Stirling cycles decreases dramatically, making thermoelectrics a valuable option [21]. TEGs indeed do not have moving mechanical parts and are therefore significantly more reliable and maintenance free.

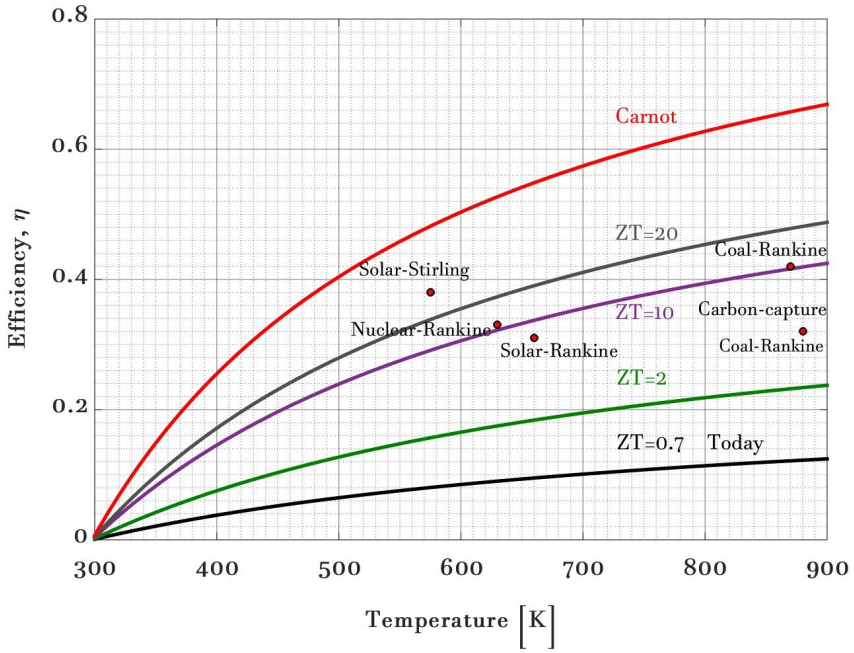



Figure 2.2: The thermodynamic efficiency of thermoelectrics calculated for different values of ZT, assuming a cold side temperature of 298 K (25 °C), compared to Carnot efficiency and Rankine and Stirling thermodynamic cycles.

A real TEG is composed of several thermoelectric couples electrically connected in series and thermally in parallel, as shown in Figure 2.3.
From an application point of view, it is obviously more interesting to evaluate what the maximum power output of a device could be under certain operational conditions, rather than knowing its efficiency.
Thereby, D.M. Rowe and G. Min [22] developed a formulation for the power output of a thermoelectric device operated in matched load conditions. Their work assumed a TEG having $N$ legs, each of which is of length $L$ and cross-sectional area $A$, where p- and n-type semiconductors have, for sake of clarity, identical Seebeck coefficients $\alpha$, electrical conductivity $\sigma$ and thermal conductivity $\kappa$. Including the effect of the metal-semiconductor contacts, having length $l_c$, specific contact resistivity $\rho_c$ and thermal conductivity $\kappa_c$; it was derived that:

$$V = \frac{\alpha N(T_h - T_c)}{1 + 2\frac{\kappa l_c}{\kappa_c L}} \tag{2.13}$$

$$I = \frac{\alpha\sigma A(T_h - T_c)}{2(2\rho_c + L/\sigma)(1 + 2\frac{\kappa l_c}{\kappa_c L})} \tag{2.14}$$

$$P = IV = \frac{\alpha^2\sigma AN(T_h - T_c)^2}{2(2\rho_c + L/\sigma)(1 + 2\frac{\kappa l_c}{\kappa_c L})^2} \tag{2.15}$$

The power output, Equation 2.15, highlights a number of issues. First of all, it can be observed that the power is dominated by $\alpha^2\sigma$, which is defined as the power factor of thermoelectrics. Moreover, the power output is proportional to the area and number of the legs of the module and also to the square of the temperature gradient.

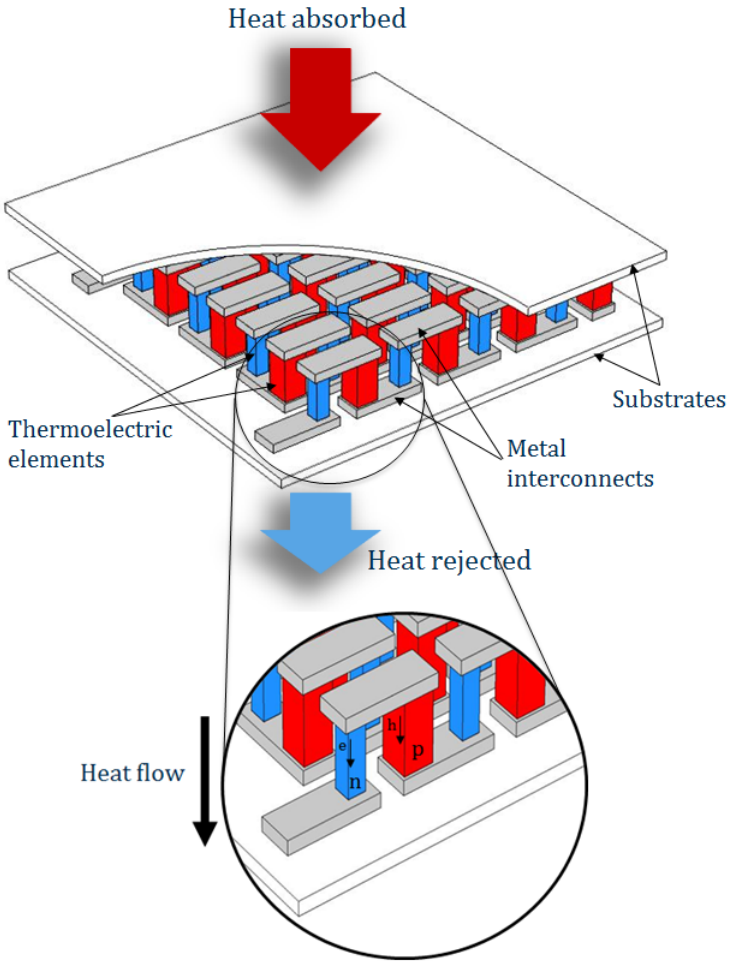



Figure 2.3: Schematic diagram of a thermoelectric module with p- and n-type legs bonded electrically in series and thermally in parallel.

Finally, whilst shortening the leg length would to the first order increase the power output, Equation 2.15 demonstrates that the contact resistance of each leg would start playing a larger part in reducing the output power. The latter consideration is of extreme importance for micro-fabricated modules, as having a low specific contact resistance is crucial to achieve a significant power output.

## 2.3 Thermoelectric Properties in 3D Semiconductors

As described in the figure of merit of thermoelelctric, Equation 2.11, the ideal thermoelectric material should simultaneously behave as an electrical conductor and a thermal insulator while also having a large Seebeck coefficient.
For metals and degenerate semiconductors, the Seebeck coefficient can be defined as a function of carrier concentration, $n$, and the effective mass of the carrier, $m^*$, [23]:

$$\alpha = \frac{8h^2k_b^2}{3eh^2}Tm^*\left(\frac{\pi}{3n}\right)^{\frac{2}{3}} \tag{2.16}$$

where $k_b$ is the Boltzmann constant, $h$ is the Planck constant and $e$ is the elementary charge.
In addition, the electrical conductivity can also be expressed as function of carrier concentration and mobility, $\mu$, [23]:

$$\sigma = ne\mu \tag{2.17}$$

From Equations 2.16 and 2.17, it clearly appears that a reduction in the carrier concentration would result in a larger Seebeck coefficient, but, at the same time, in a lower value of electrical conductivity. Similarly, the effective mass is proportional to the Seebeck coefficient. However, since heavier carriers move at slower velocity, revealing therefore reduced mobility, the effective mass of the carrier is also inversely proportional to the electrical conductivity.
On the other hand, the thermal conductivity is defined as the property of a material to conduct heat and, for semiconductors and metals, it can be expressed as the sum of the electronic contribution, $\kappa_e$, and the lattice contribution from phonons, $\kappa_{ph}$:

$$\kappa = \kappa_e + \kappa_{ph} \tag{2.18}$$

For non-degenerate semiconductors, the lattice contribution to the thermal conductivity dominates the electronic one: $\kappa_e << \kappa_{ph}$; the opposite happens for degenerate

semiconductors and metals: $\kappa_e >> \kappa_{ph}$.
The lattice contribution to the thermal conductivity is related to phonons; the modes of vibration of interacting particles in an elastic crystal lattice. Phonons are quasi-particles, which describe the excitation of the lattice and can be of two different modes. The acoustic modes are characterized by in phase neighbours oscillation, either in transverse or longitudinal direction, whilst the optical mode presents neighbours oscillating in anti-phase, Figure 2.4.

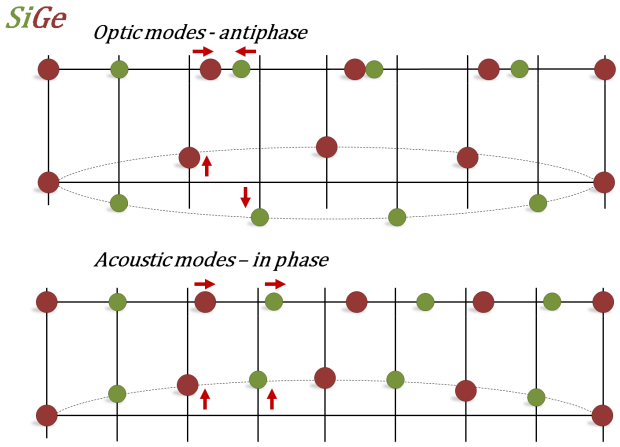



Figure 2.4: Schematic of optic and acoustic phonons modes of vibration in the longitudinal and transverse directions.

The phenomenological model to calculate the phonon contribution to the thermal conductivity was first published by J. Callaway [24]. By this approach, the lattice thermal conductivity results:

$$\kappa_{ph} = \frac{k_b}{2\pi^2}\left(\frac{2\pi k_b}{h}\right)^3 \int_0^{\frac{\theta_D}{T}} \frac{\tau_c(x)x^4e^x}{\nu(x)(e^x-1)^2}dx \tag{2.19}$$

where $\theta_D$ is the Debye temperature, $x = \frac{h\omega}{2\pi k_b T}$, $\omega$ is phonon angular frequency, $\tau_c$ is the combined phonon scattering time and $\nu$ is the phonon velocity.
The electrical contribution to the thermal conductivity has been derived from the Boltzmann transport equation by B. Nag [25]. For a total electron momentum relaxation time of $\tau$ for electrons of energy $E$, the electronic contribution to the thermal conductivity results:

$$\kappa_e = \frac{\sigma}{e^2T}\left[\frac{\langle\tau\rangle\langle E^2\tau\rangle - \langle E\tau\rangle^2}{\langle\tau^3\rangle}\right] \tag{2.20}$$

The clear and undesired result from Equation 2.20 is that $\kappa_e$ is proportional to the electrical conductivity. Moreover, in metals and degenerated semiconductors, the

electrical and thermal properties are coupled through the Wiedemann-Franz law [26]:

$$\frac{\kappa}{\sigma} = LT \tag{2.21}$$

where L is the Lorentz number and is equal to: $L = \frac{\pi^2}{3}\left(\frac{k_b}{e}\right)^2 = 2.44 \times 10^{-8} \mathrm{W\,\Omega\,K^{-2}}$. As a conclusion, the doping density constitutes the only parameter to vary in order to optimise the figure of merit in bulk thermoelectrics. However, improving one thermoelectric property by choosing better doping density does not necessarily result in higher values of ZT or power factor, $\sigma\alpha^2$. While ZT quantifies the ability of a given material to efficiently convert heat into electricity; the thermoelectric power factor describes the ability of a given material to produce electrical power in a space-constrained application. Figure 2.5 schematically shows the conflicting nature of thermoelectric properties in the case of bulk bismuth telluride, $Bi_2Te_3$, as a function of doping density.

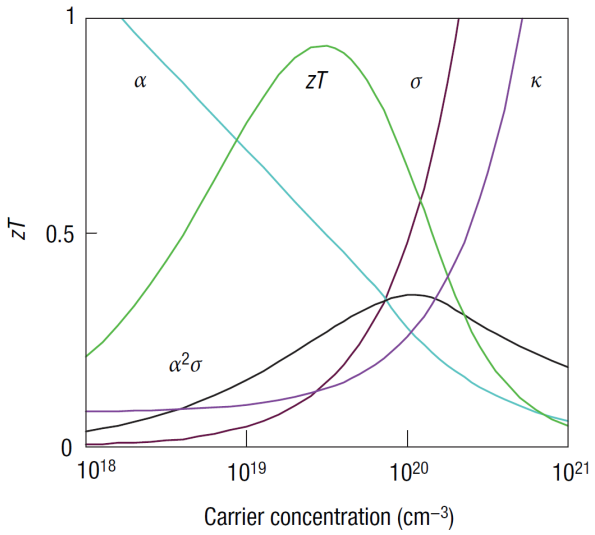



Figure 2.5: Thermoelectric properties and figures of merit for bulk bismuth telluride materials [23].

Thermoelectrics therefore require a rather unusual material: a 'phonon-glass electron-crystal' [23,27]. The phonon-glass requirements arises from the need to scatter phonons which have wide spectrum of wavelengths and mean free paths (ranging from 10 nm to 10 µm) [28,29]. Moreover, the ability to scatter phonons at a variety of length scales does not have to compromise the electron transport properties; thereby the electron-crystal requirement.

Traditionally, the field of thermoelectrics makes use of alloying between isoelectronic

elements in order to preserve the crystalline electronic structure of the material while determining a large mass contrast that disrupts the phonon path. Recent theoretical and experimental studies successfully demonstrated other methods to achieve 'phonon-glass electron-crystal' materials spreading a renewed excitement in the field.

## 2.4 State-of-the-Art Materials for Bulk TEGs

Decades of research and development on thermoelectric materials can be schematically summarized in Figure 2.6, where the thermoelectric performance of the established state-of-the-art p- and n-type materials are presented as a function of temperature.

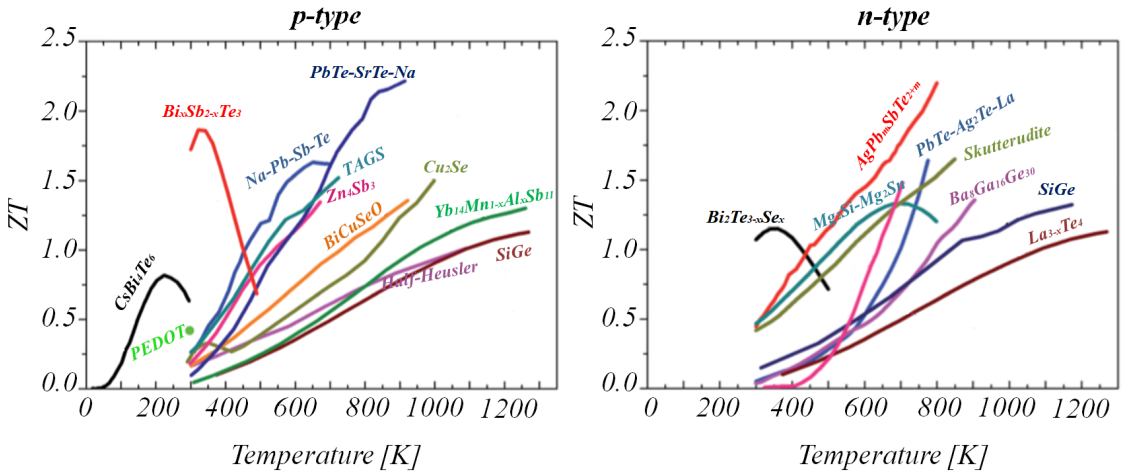



Figure 2.6: Summary of the figure of merit, $ZT$, for some of the best p- and n-type bulk thermoelectric materials reported in literature.

For near room temperature applications, tellurium alloys are the better performing and the most widely used materials for both p- (antimony telluride, $Sb_2Te_3$) and n-type (bismuth telluride, $Bi_2Te_3$). Bismuth telluride has been showing its promising thermoelectric behavior since the first investigations conducted in the 1950s [30–33]. Further thermoelectric improvements due to fine tuning of carrier concentration and alloying with antimony (Sb) and selenium (Se), respectively for p- and n-type, were demonstrated in studies on both single and polycrystalline $Bi_2Te_3$ [34–36]. This class of materials typically achieve peak figure of merit values in the range of 0.9 - 1.1. However, tellurium is the $9^{th}$ rarest element on earth, it is toxic and volatile at high temperatures [23]; therefore, its use is not sustainable for large scale production. Chalcogenides (sulfides, selenides and especially tellurides), which have chemical

compounds consisting of at least one chalcogen ion and at least one more electropositive element, are typically used for mid-temperature power generation (500-900 K). In particular, group-IV tellurides, such as lead telluride ($PbTe$) germanium telluride ($GeTe$) and tin telluride ($SnTe$), present peak $ZT$ values of around 0.8 [30, 32, 37, 38]. Higher performance, $ZT > 1.2$, has been reported for the p-type alloy $(GeTe)_{0.86}(AgSbTe_2)_{0.15}$, commonly referred as TAGS [39].

Silicon-germanium alloys are the most successful high-temperature (>900 K) materials for thermoelectric generators for both n- and p-type legs. Although the peak $ZT$ of these materials being fairly low, particularly for p-type, it is also very broad [40, 41]. Thereby, silicon-germanium reveals superior thermoelectric behavior over a wider range of temperatures if compared to the other state-of-the-art materials.

During the last decade, theoretical studies and improved fabrication technologies motivated researches all over the world to design and test novel high ZT materials. Sketterudites, half-Heusler compounds and silicon-based materials are the most likely to be the first to close the gap between the laboratory and industrial applications. All these three classes of thermoelectric materials constitute a sustainable technology, since neither rare (i.e. tellurium) nor toxic (i.e. lead) elements are used. Furthermore, these materials present a similar performance and thermo-mechanical properties for both p- and n-type materials, which substantially facilitates preliminary fabrication and the testing of complete modules.

Skutterudite, a cobalt arsenide mineral with variable amounts of nickel and iron, is commercially available in large quantities. Bulk TEGs from skutterudite powders show their best thermoelectric performance in the 700-900K range, already achiveing about 7-8% thermoelectric conversion efficiency [42–44], being thereby close to the requirements of commercialization.

Half-Heusler compounds, intermetallic alloys with a general formula $MNiSn$, where M is a group IV transition metal ($M = Zr, Hf, Ti$), recently attracted the attention of the thermoelectric field due to their high negative Seebeck coefficient [45–47]. The first bulk TEGs based on industrially sintered half-Heusler compounds (p- and n-type doped $(Zr_{0.4}Hf_{0.6})Ni(Sn_{0.98}Sb_{0.02})$) already have shown a peak ZT of 0.44 at 800 K [48]. Despite being environmentally friendly, low cost, chemically and mechanically resistant at high temperature, half-Heusler compounds still need to achieve long-term stability before reaching device production.

Oxide thermoelectric modules have also attracted interest due to the low cost of materials and processing, revealing instability of interface contacts at high temperature and relatively low ZT values [49]. A considerable number of oxide-based modules has

indeed been fabricated and tested [49–56] achieving output power densities as high as $300\,\mathrm{mW/cm^2}$ for a single pair of $16\,\mathrm{mm^2}$ legs operating at 1000 K and under a 500 K temperature gradient [52].

P-type higher manganese silicides and n-type magnesium silicides have already demonstrated moderate thermoelectric figures of merit in the medium-high temperature regime. Thermal stability, low costs and the relative abundance of the materials are tangible attractions for large scale applications. On the other hand, the synthetic approaches for high density optimized material are known to be challenging [57]. Magnesium silicide in optimized composition ($Mg_2Si_{0.55-x}Sn_{0.4}Ge_{0.05}Bi_x$ for $x = 0.02$) revealed peak values of ZT as high as 1.4 at around 800 K [58]; while higher manganese silicides demonstrated optimum ZT values, 0.6, at around 700 K [59]. The first thermoelectric silicide modules reported efficiencies between 3.7% and 5.3% at 1000 K [60, 61], but still exhibited temperature dependent degradation of the leg materials and contacts [61, 62].

## 2.5 Micro-Scaled TEGs

A renewed excitement in the thermoelectric field began in the mid 1990s thanks to theoretical studies which predicted micro- and nano-structured materials to have better thermoelectric efficiency compared to their bulk counterparts [63–66]. The electronic density of states of low dimensional systems [67] would lead to improved electronic transport properties, thereby to improvements of the thermoelectric figure of merit, Figure 2.7. Quantum-well [66, 68] and quantum-dot superlattice structures [69, 70], as well as single nanowires [71, 72] and porous nanomeshes [73], have been investigated and proved to be effective in improving thermoelectric performance. However, integrating low dimensional components into macroscopic energy harvesting systems constitutes a substantial challenge. Micro manufacturing the components composing the thermoelectric converters constitutes the most pragmatic approach to the task.

Micro-TEGs ($\mu$TEGs) differentiate from state-of-the-art macro ones by the size of the thermoelectric components, which results in an overall reduction of the size of the devices, Figure 2.8. $\mu$TEG module dimensions are not in the sub-millimeter scale due to the necessity of maintaining a temperature gradient across the device through the connection of an heat exchanger at the cold side and a heat collector at the hot side.

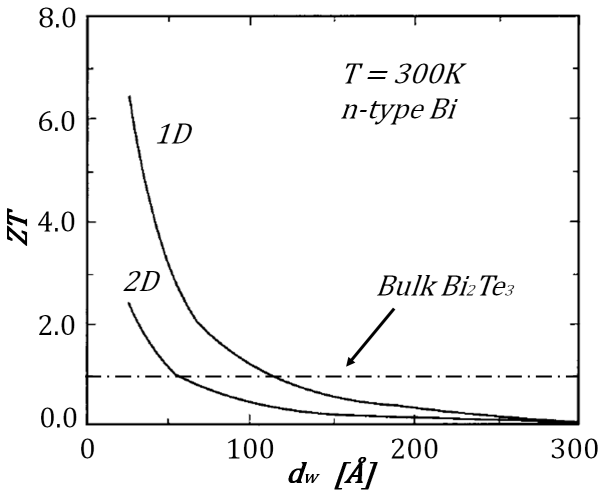



Figure 2.7: ZT dependence on quantum well (2D) and quantum wire (1D) widths, $d_w$, calculated by Hicks and Dresselhaus [63,65] in the case of n-type bismuth at room temperature. The results are compared to the literature ZT value for bulk $Bi_2Te_3$.

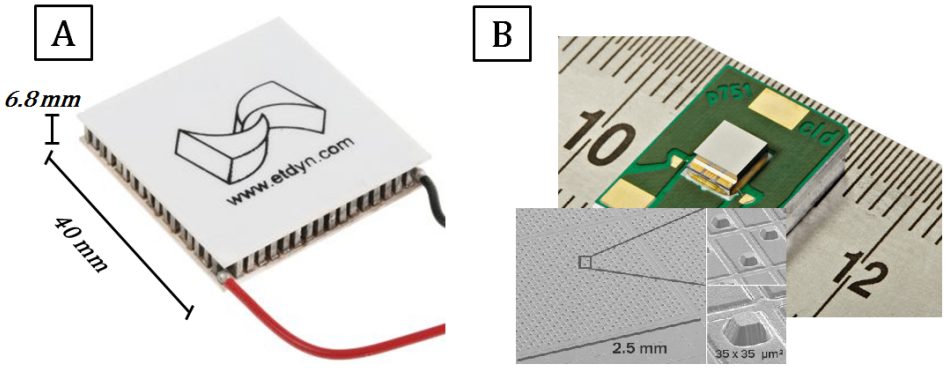



Figure 2.8: Examples of macro (A) [74] and micro (B) [75] scaled commercial thermoelectric modules.

Depending on the direction of the heat flow and the layout of the thermocouples, the $\mu$TEGs in literature can be classified in the three main categories, as illustrated in Figure 2.9: $\mu$TEGs having vertical heat flow and vertically fabricated thermocouples, devices characterized by vertical heat flow and laterally fabricated thermocouples and generators presenting lateral heat flow and laterally fabricated thermocouples. All macro TEGs, as well as several $\mu$TEG designs, utilize the cross-plane heat flow with vertically fabricated thermocouples configuration, with pillar-shaped thermoelectric legs sandwiched between thermally conductive substrates. The vertical heat flow design offers the advantage of improved thermal contact to the heat exchangers,

whilst being strongly limited by the reduced deposition thicknesses available from thin-film growth mechanisms. On the other hand, laterally fabricated thermocouples allow sufficient thermocouple lengths; however, more complex processing procedures (isotropically dry-etched [76] or micromachined [77] microcavities, assembly of planar layers [78]) become necessary to overcome the parasitic heat flow through the substrate.

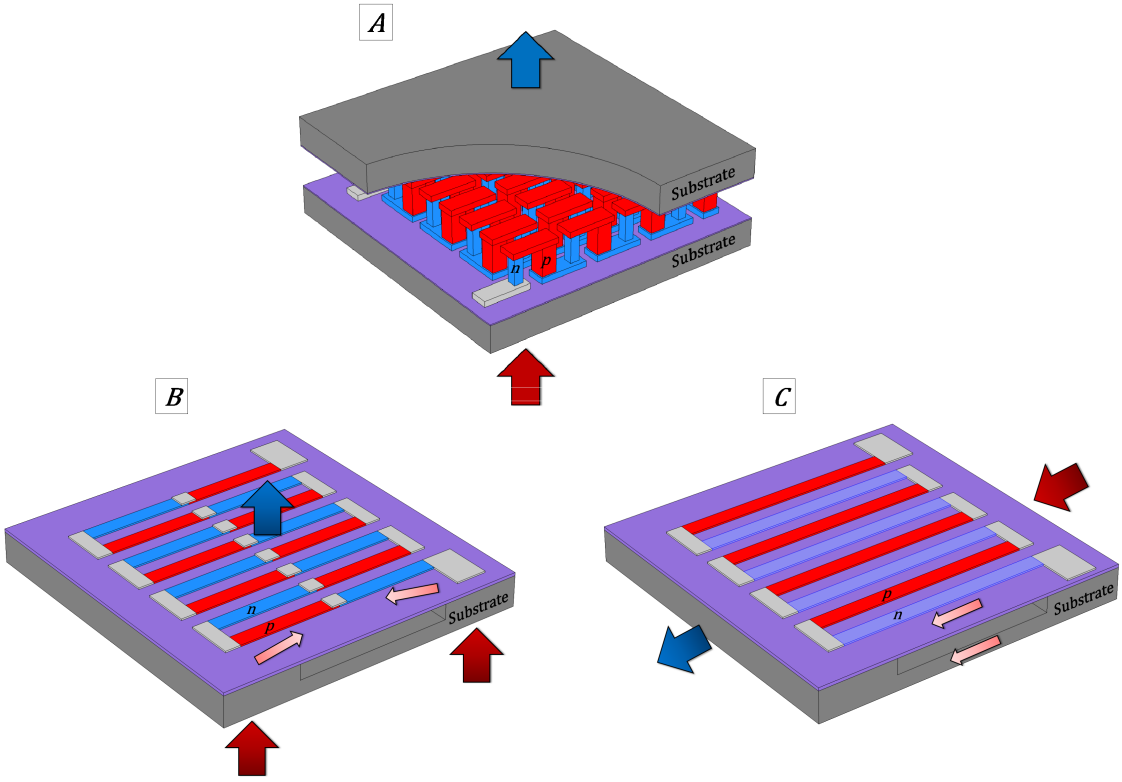



Figure 2.9: Illustrative schematic of the three main $\mu$TEG configurations: cross-plane heat flow and vertically fabricated thermocouples (A), cross-plane heat flow and laterally fabricated thermocouples (B) and in-plane heat flow and laterally fabricated thermocouples (C).

The fabrication of $\mu$TEGs is almost entirely based on bismuth telluride compounds with only minor attempts to produce in-plane silicon-based devices. A complete overview, collecting information on designs and performance of both commercially and academically realized $\mu$TEGs, is reported in Table 2.1. Early efforts in TEG miniaturization go back to 1989, when Rowe et al. fabricated the first $\mu$TEG realized using a silicon-on-sapphire substrate [79]. The first commercially developed $\mu$TEG appeared almost a decade later. In 1997, the German company Dunnschicht Ther-

mogenerator Systemen released a device based on sputtered thin films of bismuth telluride material on foils [80, 81]. Miniaturized bulk thermoelectrics were already applied to power wristwatches made by Bulova in 1982 and, at a later time, by Seiko [82, 83] in 1998. Commercially available $\mu$TEGs are entirely based on bismuth and tellurium alloys; thereby, as seen in Section 2.4, they only address near room-temperature applications. In recent years, the German company Micropelt established a scalable production of devices based on bismuth telluride materials grown by Chemical Vapor Depositon (CVD). P- and n-type wafers are processed separately, then cleaved and soldered at a later stage [12, 84]. Since 2013, Laird Technologies also started the production of $\mu$TEGs based on bismuth thelluride and antimony telluride superlattice structures grown by Metal-Organic Chemical Vapour Deposition (MOCVD) [70].

Thermogen Technologies Inc. just recently entered the market of micro-scaled thermoelectric generators with an innovative technology based on bismuth telluride materials deposited on flexible thin foils [85].

It must be noted that bismuth telluride, in both single crystals and polycrystalline forms, is characterized by a strong anisotropy in transport properties. Despite costs and complexity of the equipement, CVD has the advantage of allowing the growth of semiconductor materials with high control over the crystal orientation, thereby guaranteeing transport properties in specific directions. University researchers have investigated alternative growth techniques, such as sputtering, Physical Vapor Deposition (PVD), thermal co-evaporation and electrochemical depostion, which however offer limited control over material composition and crystal orientation. Electrochemical deposition was revealed to be the only suitable technique, among the above mentioned, to grow bismuth telluride materials with high a ZT in the direction perpendicular to the substrate [86].

At Jet Propulsion Laboratories, a MEMS-like microfabrication process for thermoelectric devices based on electrodeposited bismuth telluride was firt reported in 2002 [87]. A flexible $\mu$TEG, based on bismuth telluride materials electrochemically deposited applying a novel control method, was demonstrated at ETH Zurich by W. Glatz [88, 89].

In order to decrease TEG material and production costs, the well-established silicon technology in combination with MEMS micromachining techniques can also be taken into consideration. A $\mu$TEG based on micromachined poly-silicon-germanium was specifically designed for human body heat harvesting in [90]. The device, despite a very high internal resistance (30 M$\Omega$), reported an open-circuit output voltage of

12.5 V/cmK and a power factor of 0.026 µW/cm$^2$K$^2$ at matched external load.
An in-plane configuration micro device, with thousands of 6 µm tall silicon-germanium-aluminum freestanding thermocouples, was demonstrated to achieve an output power of 0.4 µW and an open circuit voltage of 1.49 V across a 3.5 K temperature gradient [91].
More in-plane micromachined TEGs, consisting of 1000 junctions of polycrystalline doped silicon and aluminum on across a 10 µm silicon membrane, were proved to provide an output power of 1.5 µW at 10 K temperature gradient [92].
Devices with thermocouples made of aluminum and n-doped poly-crystalline silicon, as well as electrodeposited bismuth telluride materials were fabricated and compared by Huesgen at al. [93].
Finally, $\mu$TEGs consisting of 400 poly-silicon legs were designed using the standard Bipolar CMOS (BiCMOS) process. Micromachined cavities underneath a 1.6 µm thick oxide layer demonstrated an improvement in the thermal efficiency of the device, resulting in open circuit voltages up to 200 mV K$^{-1}$ [77, 94]. With similar BiCMOS micro-processing, a silicon-germanium quantum-well based thermoelectric micro generator has been developed [76].

| Citation | | Material | | | Device Design | | | | Device Performance | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Author (et al.)** | **Year** | **Substrate** | **P-type** | **N-type** | **In/cross-plane heat flow Lateral/vertical thermocouples** | **Number of legs** | **Leg length [µm]** | **Leg cross-section [µm × µm]** | **Device area [mm$^2$]** | **Internal resistance [Ω]** | **$\Delta T$ across device [K]** | **Device $V_{oc}$ at $\Delta T$ [V]** | **Device $P_{out}$ at $\Delta T$ [µW]** | **Power Factor [µW/(cm$^2$K$^2$)]** |
| Rowe [79] | 1989 | sapphire | p-Si | n-Si | in/lat | 10 | 4500 | 100×0.4 | 9 | 69k | 10 | 0.024 | 0.002 | $2\times10^{-4}$ |
| Kim [95] | 1996 | glass | p-$Bi_{0.5}Sb_{1.5}Te_3$ | n-$Bi_2Te_{2.4}Se_{0.6}$ | in/lat | 300 | 20000 | 670×4 | 120 | 89k | 40 | 4 | 45 | 0.023 |
| Stordeur [80, 81] | 1997 | polyimide | p-$Bi_{0.5}Sb_{1.5}Te_3$ | n-$Bi_2Te_{2.7}Se_{0.3}$ | in/vert | 2250 | 1000 | 50×2.5 | 63.7 | 1M | 5 | 2.1 | 1.1 | 0.069 |
| Kishi [82, 83] | 1999 | Si | p-BiSbTe | n-BiTe | cross/vert | 520 | 600 | 80×80 | 1k | 40 | 1 | 0.3 | 22.5 | 56.25 |
| Glosch [92] | 1999 | Si | Al | n-poly Si | in/lat | 1000 | 500 | 7×1.2 | 16.5 | 900k | 10 | 2.4 | 1.5 | 0.091 |
| Venkatasubramanian [70] | 2001 | Si | $Bi_2Te_3$-type superlattice | | cross/vert | - | - | - | 10.23 | 11.3 | 10 | 0.26 | 1500 | 147 |
| Lim [87, 96] | 2002 | glass, Si | p-$Bi_{2-x}Sb_xTe_3$ | n-BiTe | cross | 63 | 20 | radius: 30 | 2.89 | 4 | 1.25 | 0.004 | 1 | 22.1 |
| Strasser [94] | 2002 | Si | p-poly Si | n-poly Si | in/lat | 59400 | 7 | 3.4×0.4 | 6 | 12M | 5 | 0.73 | 0.01 | 0.007 |
| Strasser [77] | 2003 | Si | p-poly Si | n-poly Si | in/lat | 15872 | 18.5 | 6×0.4 | 7 | 2.1M | 5 | 0.93 | 0.103 | 0.059 |
| Bottner [84] | 2004 | Si | p-$(Bi,Sb)_2Te_3$ | n-$Bi_2Te_3$ | cross | 12 | 20 | 100×30 | 1.12 | 7 | 5 | 0.0043 | 0.067 | 2.4 |
| Hasebe [78] | 2004 | polyimide | Cu | Ni | cross/lat | 380 | 2200 | 300×0.15 | 2700 | 6k | 1 | 0.006 | $1.6\times10^{-3}$ | $5.7\times10^{-5}$ |
| Harman [97] | 2006 | none | PbSeTe/PbTe *QDSL**, Cu | | cross/vert | 1 | 95 | $2000^2$ | 4 | 0.01 | 220 | 0.05 | $89\times10^3$ | 46 |
| Huesgen [93] | 2008 | Si | poly-Si | Al | in/lat | 125 | 120 | p:40×0.7<br>n:5×0.25 | 1.7 | 84k | 5 | 0.048 | 0.007 | 0.016 |
| Glatz [88, 89] | 2009 | polyimide | p-$Bi_{2+x}Te_{3-x}$ | n-$Bi_{2+x}Te_{3-x}$ | cross/vert | 90 | 126 | radius:105 | 52 | 7.11 | 51.2 | 0.106 | 393 | 0.288 |
| Wang [90] | 2009 | Si | poly-Si | poly-Ge | cross/lat | 4700 | - | 3×3 | 16 | 20M | 0.15 | 0.15 | $0.3\times10^{-3}$ | 0.026 |
| Leonov [98] | 2009 | Si | p-poly Si | n-poly Si | in/vert | 2300 | 100 | 19×- | 225 | 3.8M | 9 | 2 | 1 | 0.0055 |
| Xie [99] | 2010 | Si | p-poly Si | n-poly Si | cross/lat | 125144 | 16 | 5×0.7 | 100 | 52.8M | 5 | 16.7 | 1.3 | 0.052 |
| Kao [100] | 2010 | Si | p-poly Si | n-poly Si | in/lat | 24 | 640 | 5×0.3 | 0.72 | 2.45k | 1 | 67µ | $0.5\times10^{-6}$ | $6.4\times10^{-5}$ |
| Su [101] | 2010 | Si | poly-Si | poly-Ge | in/lat | 1766 | - | 10×0.7 | 2.5 | 6M | 29 | 3.2 | 0.45 | 0.021 |
| Yang [76] | 2011 | Si | poly-Si | poly-Ge | in/lat | 2250 | 60 | 4×0.3 | 2.25 | 2.3M | 20 | 4.52 | 2.26 | 0.251 |
| Micropelt [12, 75] | 2013 | Si | $(Bi,Sb)_2(Te,Se)_3$ | | cross/vert | 580 | 36 | 35×35 | 2.89 | 300 | 5 | 0.55 | 252 | 71 |

*QDSL**: Quantum Dots SuperLattice

Table 2.1: Comprehensive overview of the materials used in fabricated µTEGs and their design and performance.

## 2.6 Applications

The first application of thermoelectrics dates back to the 1960s when radioisotope thermoelectric generators (RTGs) were installed on satellites for space missions. In both NASA Voyager space missions, the radioactive decay of plutonium 238 was used to heat, up to 1000 °C, the heat sink of the silicon-germanium RTGs, whilst the outside of the spacecraft was adopted, via heat exchangers, as a cold sink. The silicon-germanium RTGs weight about 40 kg and produced 470 W at 40 V with an efficiency as high as 6.6% at launch. After more than 30 years, and over a light year away from Earth, Voyager's RTGs still serve the purpose, despite a 25% decrease in performance (now generating less than 350 W), well demonstrating the robustness of the technology. Current lack of plutonium 238 sources, as all the military nuclear reactors have been shut down, motivated a number of space research programmes to investigate different available radio isotopes [102].

At present, thermoelectric devices find their major application as Peltier coolers in the thermal management of semiconductor electro-optic components (i.e. diodes, lasers, power amplifier, IR detectors). As an example, a semiconductor laser could produce in excess of 10 W of dissipated heat over an area of few $mm^2$. The resulting local overheating would greatly affect the performance of the device and a cooling solution is thereby needed.

The major application of thermoelectrics as power generators is in the information and communication technology. High-performance computing systems and data centers require energy harvesting solutions to improve their system efficiency, while smart autonomous sensor systems need an electrical power source. The long term operation without need of maintenance allows thermoelectrics to be a cost effective solution in such environments. In particular, most wireless sensors systems now only require a few mW of power depending on the communication distance; thereby, a 1 $cm^2$ TEG, operating across a 50 K temperature gradient, would be enough to provide sufficient power.

Wearable electronics and autonomous medical implant systems are other applications of enormous interest. Live health-monitoring devices constitute a vast improvement in preventive health-care, possibly decreasing the cost of curative medicine. Such components can be of very small size and their integration in garments would make them non-invasive. The integration of health-monitoring devices is complicated by the necessity of batteries. However, the sensors often require to be in contact with the body and thermoelectric scavenging could harvest enough heat from the human body

to power medical devices. Despite the metabolic chemical reactions of the human body continuously produce heat, the temperature gradients available between body and air (1 °C $\Delta T$ at air ambient temperature of 4.7 °C and 8.5 °C $\Delta T$ at ambient temperature of 15 °C [103]) are limited, thereby a lot of research effort has to be directed towards efficient thermal management. Electrocardiography systems, powered by TEGs and integrated into clothing, have already been demonstrated and even tested by Imec [98]. Electroencephalography, electromyography and pulse oximeters are other extremely ambitious potential applications. Ultimately, such application scenarios could be addressed with autonomous in-vivo implants.

The automotive industry has the potential to establish thermoelectrics on the market, leading to the widespread use of the technology. In relation to environmental issues, the application of thermoelectrics to vehicles is of great interest. The current internal combustion engines have an average efficiency of 20% - 45% depending on engine type and driving conditions; with the remaining 55% - 80% of the fuel energy being converted into heat and dissipated through coolant and exhaust gases. The waste exhaust heat energy could be directly converted into electrical power, increasing the efficiency of the system and decreasing fuel consumption. Ultimately, the thermoelectric generator could be used to charge the car battery, replacing the current shaft-driven alternator. Some of the major automotive companies (like General Motors [6], BMW [9], Ford [10], Renault [7] and Honda [8]) already developed TEGs systems for exhaust heat recovery. The typical concept design presents the thermoelectric generators directly mounted on the exhaust pipe surface and cooled using the engine coolant. The first attempt to develop a thermoelectric heat recovery system for automotive applications was carried out on a 1999 GMC pickup truck [6]. The thermoelectric unit was made of 16 20 mm x 20 mm $Bi_2Te_3$ TEGs and it was able to achieve a 2% increase in fuel efficiency by producing an electrical power of 255 W at 80 °C coolant temperature with the vehicle moving at 110 km h$^{-1}$. The system developed by BMW [9] was instead based on segmented TEGs, composed of skutterudites, TAGS, PbTe and BiTe materials, installed on the exhaust shell of the catalytic converter and cooled via tube heat exchanger. The assesment of the system was performed on a BMW X6 vehicle with a recorded electrical power generation of 100 W at a vehicle speed of 60 km h$^{-1}$ and 600 W at 125 km h$^{-1}$. The corresponding increase in fuel efficiency ranged from 0.7% at 60 km h$^{-1}$ to 1.25% at 125 km h$^{-1}$. An analogous study was performed by Ford [10] on a Ford Fusion 3.0 l V-6 engine cruising at 100 km h$^{-1}$. The system was reported to achieve a peak electrical power of 500 W. The developed design adopted a finned tube heat exchanger lined with the segmented

TEGs, based on Half-Heusler and BiTe materials. The exhaust gas was flowing in the centre of the exchanger tube, while the outside surfaces were liquid cooled. In order to realize such architecture, 4.6 kg of thermoelectric material were used. The French automotive company Renault also designed a TEGs system targeting the heat recovery scenario of the exhaust line of a diesel truck engine [7]. The architecture adopted a combination of skutterudites, $Mn_2Si/Zn_4Sb_3$, and $Bi_2Te_3$ TEGs. The first were mounted along the exhaust line, where the temperature of the gases is in the range of 250-350 °C, while the second set of TEGs was designed to recover waste heat from the coolant (50-100 °C). The total power generation of such system was reported to reach 1 kW. Honda developed a simple TEGs system architecture using a rectangular box with TEGs placed on the surfaces and liquid cooling system on the cold side of the devices. The 32 30 mm x 30 mm TEGs produced a maximum of 500 W leading to a fuel consumption reduction of about 3%. All the investigations have demonstrated improvements in the overall fuel consumption efficiency; however, more feasibility tests are required before the integration of TEG systems in commercial vehicles.

Another developing industrial application is thermal-photovoltaic. The current efficiency of concentrator photovoltaic systems reaches values up to 45 %, achieved when the sunlight is concentrated up to a thousand times. Such light concentration results in the photovoltaic cells reaching very high temperatures, resulting in large thermal cycling which ultimately leads to failures and reduced lifetime of the system. The integration of thermoelectrics in photovoltaic power plants would then not only increase the electricity generated by the overall system, but would also help the cooling of the solar panels, reducing their thermal cycling and thereby increasing their lifetime. Improved Carnot efficiency and longer lifetimes lead to reduced costs and thermo-photovoltaic are now becoming a reality.

At the moment, despite being studied since the 1970s, thermoelectrics still require a 'launch application' that could increase the production volume. Automotive applications could play the role, even if more driven by legislation and sustainability policies that by the market. In addition, the autonomous sensor market would also help widespread the use of thermoelectrics. Nevertheless, the real limitation to the field is the need to find efficient and sustainable thermoelectric materials.

## 2.7 Chapter Conclusions

The present Chapter introduced the basics of thermoelectricity and offered an overview of the most successfully used materials. The main attempts of integrating TEGs systems on vehicles were reported. Moreover, a complete review of micro-processed thermoelectric devices was presented with particular attention on design, Figure 2.9 and performance, Table 2.1, of the micro-modules.

From the review of thermoelectric materials, silicon-germanium alloys, both n- and p-type, showed to be the most successful high-temperature (>900 K) materials. Although the thermoelectric peak of these materials is fairly low, it is also very broad [40, 41]. Therefore, silicon-germanium displays superior thermoelectric behavior over a wider range of temperatures if compared to the other state-of-the-art materials. Such ability to perform over a broad range of temperatures is highly desired for TEGs application on vehicles. The exhaust line of any vehicle consists of a series of emission control and sound attenuation components having gradually decreasing temperatures when moving away from the engine manifold. At the manifold temperatures reach up to 1000 °C, at the catalytic converter the exhaust gases are in the range of 300 - 500 °C, while just before the exhaust muffler the temperature further drops to around 150-300 °C. Hence, silicon-germanium based TEGs can be optimized for the different operating conditions and installed on each element of the exhaust stream. Moreover, the micro-scale of the thermoelectric devices would allow the application in an heterogeneous system, in combination with bulk modules, and, despite the required complexity of the cooling system, on the finned area of heat exchangers and cooling radiators.

The vibrations and the thermal loading characteristic of vehicles may cause cracks in the thermoelectric materials decreasing the electrical properties and ultimately the efficiency of the TEGs system. Thereby, the most suitable design among the ones in literature was identified to be the cross-plane heat flow with vertically fabricated thermocouples. Such configuration would avoid the necessity of fragile suspended structures and etched micro-cavities.

The thermoelectric and main crystallographic properties of bulk silicon-germanium alloys will be presented and analyzed as a function of temperature, germanium concentration and doping level in the next Chapter. The design details of the micro-modules will be presented in Chapter 5.

# Chapter 3

# Material Introduction

As has emerged from the review in Section 2.5, bismuth telluride and silicon based materials are the most successfully used in the fabrication of micro-scaled thermoelectric modules. Due to their excellent thermoelectric properties, tellurium-based materials have already been the object of detailed studies and they now constitute the state-of-the-art for $\mu$TEGs. However, the rarity of tellurium, combined with the high deposition and processing costs, is motivating the field to investigate cheaper and more sustainable options. On the other hand, despite being investigated since the 1980s, silicon-based thermoelectrics have only been used to prove the scalability of the technology. Thereby, there are still many areas of improvement for further development of micro devices.
Silicon-germanium has promising thermoelectric properties over a broad temperature range [23]. Furthermore, performance optimization for a specific operating temperature can be achieved by tuning doping level and germanium concentration in the alloy. In addition, silicon-germanium relies on a robust and competitive epitaxial technology and it can be fully integrated on silicon platforms.
The chapter briefly introduces the material used in this PhD project. Crystal structure and strain related phenomena in silicon-germanium alloys are described. A review of the thermoelectric properties of bulk silicon-germanium alloys is also reported. Finally, the epitaxial growth mechanism is delineated.

## 3.1 Silicon-Germanium

Both silicon and germanium are group IV elements in the periodic table and both present a diamond cubic crystal structure, see Figure 3.1. The diamond lattice is defined by a pair of intersecting face-centered cubic Bravais lattices which are displaced,

along the diagonal, by one quarter of the diagonal length.

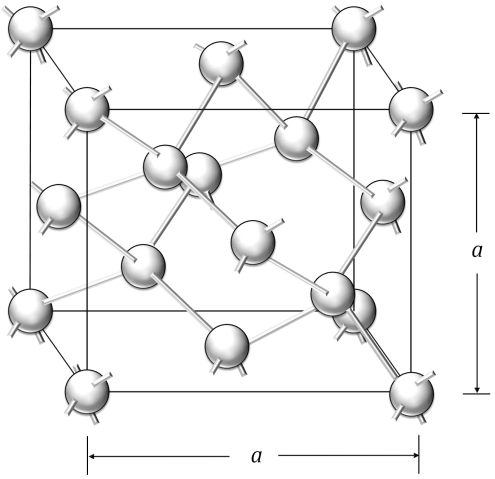



Figure 3.1: Diamond cubic crystal structure. The atoms are tetrahedrally bonded, with covalent bonds, to the four nearest neighbours.

Silicon-germanium is a substitutional alloy, meaning that, in a diamond cube crystal structure with no vacancies or interstitial defects, every germanium atom occupies the position of a silicon atom without any self-ordering. The lack of atomic ordering determines the impossibility to achieve control over the atomic layer composition of the silicon-germanium epitaxy.
At 300 K, the crystal lattice parameters for pure silicon and germanium are respectively $a_{Si}$=5.431 Å and $a_{Ge}$=5.658 Å, thereby differing by about 4%. The lattice parameter for the silicon-germanium alloy of $x$ germanium concentration can be calculated by linear interpolation between the lattice parameters of silicon and germanium, as described by Vegard's law:

$$a_{Si_{1-x}Ge_x} = (1 - x)\, a_{Si} + x\, a_{Ge} \tag{3.1}$$

Through experimental measurments [104], Vegard's law has been proven to overestimate the values of silicon-germanium lattice parameter. The accepted lattice parameters can be indeed calculated according to [104] as a function of Ge content:

$$a_{Si_{1-x}Ge_x} = a_{Si} + 0.1992\, x + 0.02733\, x^2 \tag{3.2}$$

### 3.1.1 Strain Related Phenomena

The lattice mismatch between silicon and germanium constitutes a challenge for epitaxial deposition, but, at the same time, it offers the opportunity to engineer strain

in the deposited films. The lattice mismatch, $f$, characterizing a silicon-germanium film deposited on a silicon substrate is calculated as:

$$f = \frac{a_{Si_{(1-x)}Ge_x} - a_{Si}}{a_{Si_{(1-x)}Ge_x}} \tag{3.3}$$

In the deposited layer, the in-plane strain, $\epsilon_{||}$, is defined as the lattice deformation with reference to the relaxed lattice, $a_{rel}$:

$$\epsilon_{||} = \frac{a_{||} - a_{rel}}{a_{rel}} \tag{3.4}$$

In mismatched single crystalline materials, the release of the elastic energy can lead to different phenomena: elastic accommodation (pseudomorphic growth, island nucleation), plastic accommodation (nucleation of misfit dislocations at the interface), wafer bending, surface roughening and cracks. Obviously, all of the above phenomena have relevant consequences on the morphology as well as on the electronic and optical properties of the materials.
When layers of material with lattice parameter larger than the one of the substrate (i.e. $Si_{1-x}Ge_x$ on $Si$) are grown coherently with the substrate, the in-plane lattice parameter of the deposited material will then adapt to match the one of the substrate. Consequently, the compression in the interface plane generates an expansion of the out-of-plane lattice parameter, see Figure 3.2. The presence of in-plane strain in the top layers also determines curvature of the whole wafer.

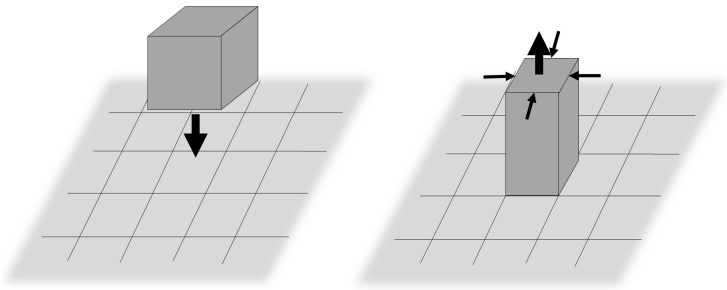


Figure 3.2: Schematic of coherent, otherwise known as pseudomorphic, growth of a material with a lattice parameter larger than the one of the substrate.

In the case of highly mismatched materials, the strain resulting from coherent growth would induce nucleation of islands. The latter is a plastic accommodation mechanism, known in silicon-germanium as the Stranski-Krastanow mechanism, in which the layer growth moves from 2D to 3D, see Figure 3.3.

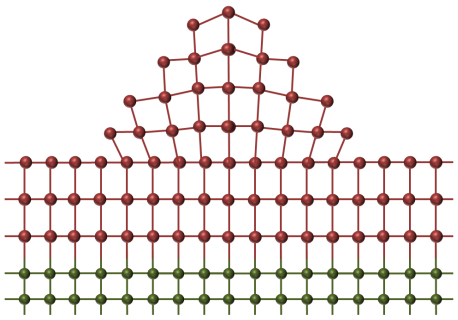


Figure 3.3: Schematic of lattice deformation in the case of strain-induced nucleation of islands. The green and red lattices represent the substrate and the deposited materials respectively.

On the other hand, in the case of moderate lattice mismatch between substrate and deposited material, the coherent growth would continue layer by layer with more energy being accumulated in the film. Once the critical thickness of deposited film, corresponding to a specific energy, is reached, it becomes energetically convenient to release the strain by forming misfit dislocation at the interface between materials, see Figure 3.4. A dislocation is a linear defect along which, the interatomic bonds are characterized by a different distribution if compared to the case of a perfect crystal.

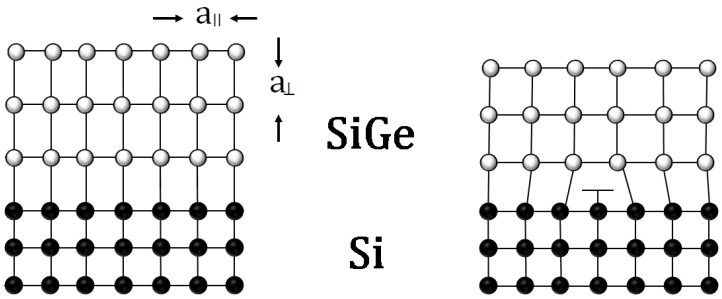



Figure 3.4: Schematic of a few monolayers of SiGe grown on Si substrate in case of coherent elastic relaxation (left) and plastic relaxation with the introduction of a misfit dislocation (right).

In the growth of high quality silicon-germanium films, the role of a relaxed SiGe buffer layer, acting as virtual substrate for the growth of the active material, is now essential in order to accommodate part of the lattice mismatch.
Finally, thermally induced strain represents another issue in epitaxial growth. In fact, the control of the atomic surface diffusivity requires the growth temperature to be higher than room temperature. Thereby, the post-growth cooling of materials with different thermal expansion coefficients would result in tensile thermal strain in the

deposited layers. In the case of Si and Ge, the thermal expansion coefficients at 300 K are $2.6\times10^{-6}K^{-1}$ and $5.7\times10^{-6}K^{-1}$ respectively. Specific cooling procedures can be employed to control the induced thermal strain.

## 3.2 SiGe Thermoelectric Properties: A Literature Review Analysis

The potential of silicon-germanium for thermoelectric applications was first demonstrated in 1958 [105]. In 1964, a complete thermal and electrical characterization of heavily doped silicon-germanium alloys [106] provided the landmark for successive material optimization. Although the work was initially commissioned by the U.S. Navy, it later became the reference point for NASA to develop RTGs for high temperature operation (from 600 °C to 1000 °C). Since then, silicon-germanium has become the established material for high temperature thermoelectric power generation.

In this work, the interest is instead pointed towards the optimum composition and doping level of p- and n-type silicon-germanium alloys for mid temperature (300 °C to 500 °C) operation, which characterizes most of the industrial environments. The data collected in [106, 107] on bulk silicon-like alloys prepared by zone leveling technique and hot pressing has been considered for analysis. In both studies, boron and phosphorous were used as p- and n-type dopants respectively.

### 3.2.1 Electrical Conductivity

In silicon-germanium alloys, the electrical conductivity, defined by Equation 2.17, is revealed to be proportional to doping level, while not significantly affected by the germanium concentration. The measurements collected in [106,107] have been plotted and reported in Figure 3.5 and Figure 3.6 for p- and n-type respectively. At around room temperature, the electrical conductivity of the heavily doped silicon-like alloys is in the range of $10^5\,S\,m^{-1}$ for both p- and n-type.

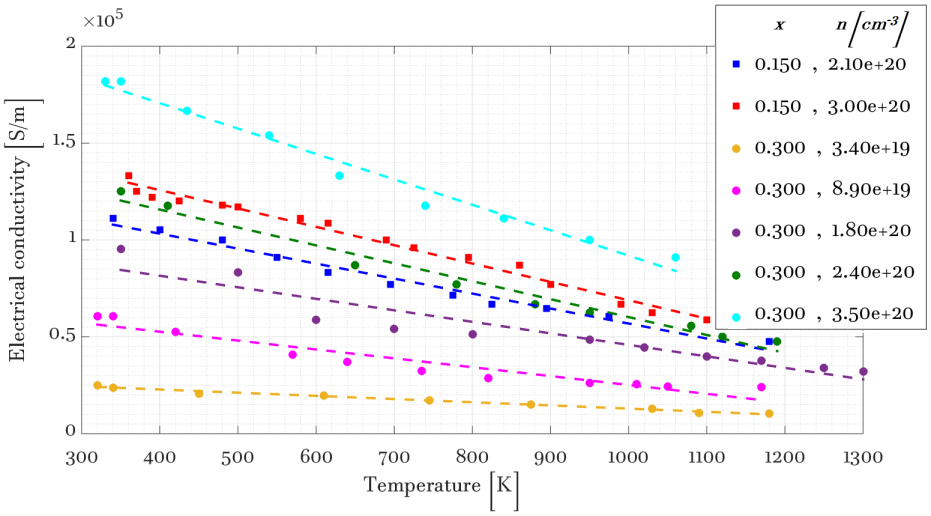



Figure 3.5: Electrical conductivity of p-type $Si_{1-x}Ge_x$ alloys for different germanium concentration, x, and doping levels, n.

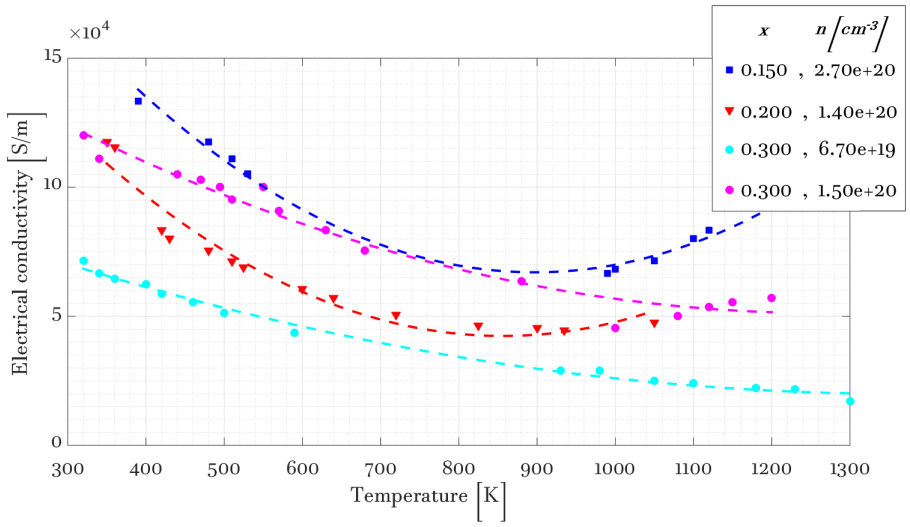



Figure 3.6: Electrical conductivity of n-type $Si_{1-x}Ge_x$ alloys for different germanium concentration, x, and doping levels, n.

### 3.2.2 Thermal Conductivity

The thermal conductivity of silicon-germanium alloys reveals substantial reductions compared to the one of the bulk counterparts, thereby highlighting the importance of the alloys for thermoelectric applications. Indeed, site substitution preserves crystallinity while creating a large mass contrast to disrupt phonon propagation [23]. However, measuring the temperature, and consequently the thermal conductivity,

have always been challenging and characterized by uncertainties mostly related to the thermal contacts between material and external probes. In [106, 107], measured values of thermal conductivity are reported for both p- and n-type silicon-germanium alloys, Figure 3.7 and 3.8.

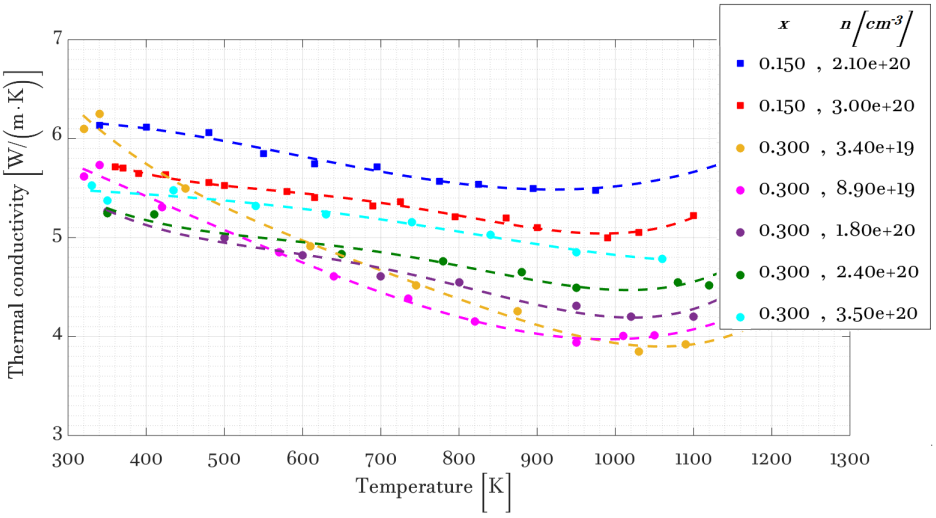



Figure 3.7: Thermal conductivity of p-type $Si_{1-x}Ge_x$ alloys for different germanium concentration, x, and doping levels, n.

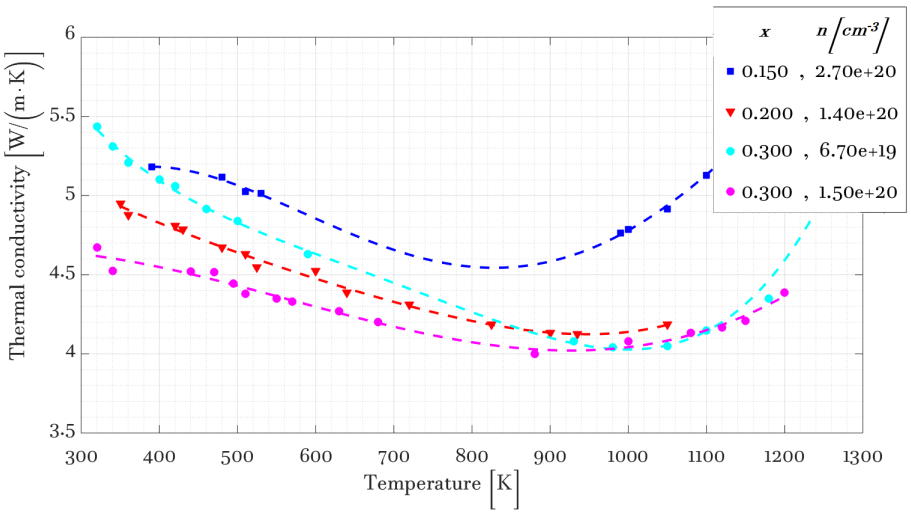



Figure 3.8: Thermal conductivity of n-type $Si_{1-x}Ge_x$ alloys for different germanium concentration, x, and doping levels, n.

For heavily doped semiconductors, according to the Wiedemann-Franz's law (equation 2.21), thermal conductivity reveals a dependence to the doping levels. From

literature values, it also appears that $Si_{0.7}Ge_{0.3}$ alloys have slightly lower thermal conductivity if compared to ones with lower germanium concentration. At around room temperature, p- and n-type heavily doped silicon-germanium alloys show comparable thermal conductivity, in the range of 4.5 to 5.5 W/mK; while, the thermal conductivity of bulk silicon and germanium are 148 W/mK and 62 W/mK respectively [108].

### 3.2.3 Seebeck Coefficient

Equation 2.16 clearly highlights the dependence of the Seebeck coefficient from carrier concentration and effective carrier mass. Lower doping levels lead indeed to a higher absolute Seebeck coefficient. Moreover, the silicon-like alloys reveal better Seebeck coefficient due to the fact that silicon has heavier effective carrier mass than germanium. Figure 3.9 and Figure 3.10 report the Seebeck coefficient values, for p- and n-type respectively, as measured in [106, 107]. At room temperature, absolute Seebeck coefficient values of around 100 $\mu V\,K^{-1}$ are reported for both p- and n-type alloys.

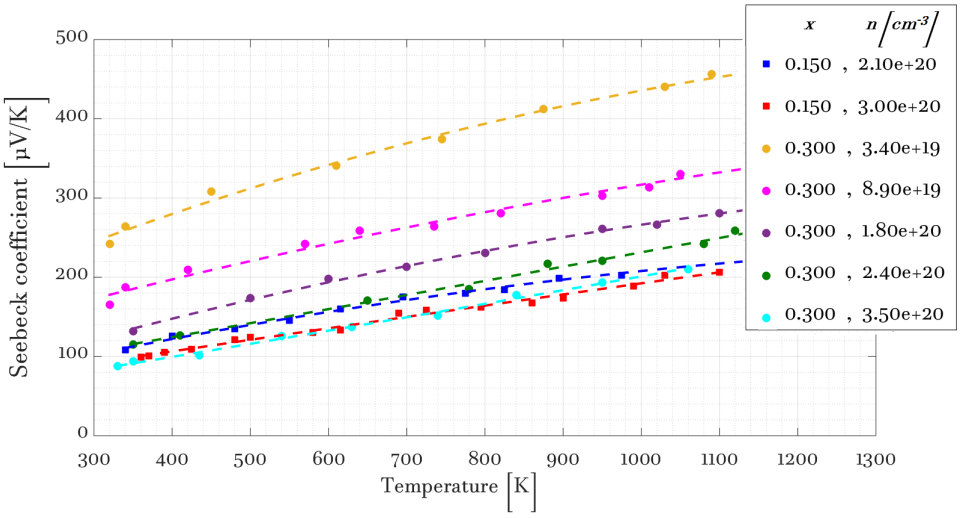



Figure 3.9: Seebeck coefficient of p-type $Si_{1-x}Ge_x$ alloys for different germanium concentration, x, and doping levels, n.

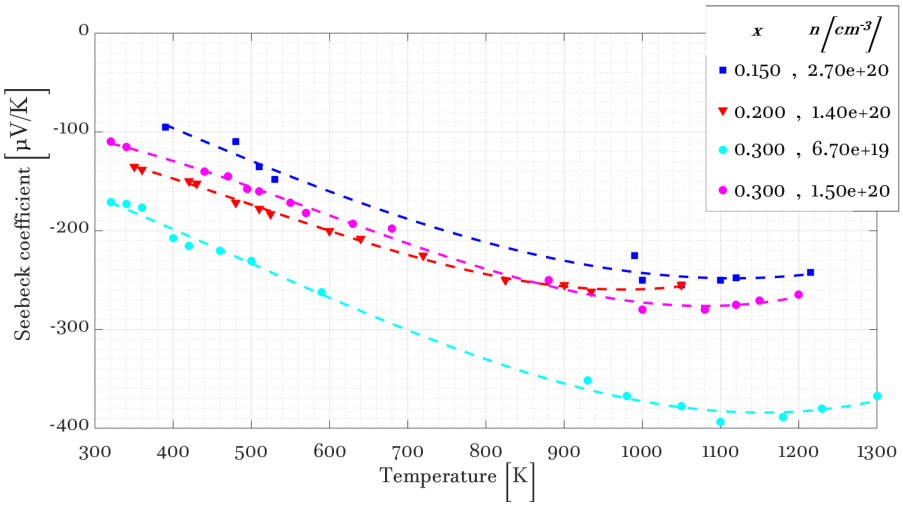



Figure 3.10: Seebeck coefficient of n-type $Si_{1-x}Ge_x$ alloys for different germanium concentration, x, and doping levels, n.

### 3.2.4 Thermoelectric Figure of Merit: ZT

As seen in Equation 2.11, the thermoelectric figure of merit, ZT, is defined as a combination of electrical conductivity, Seebeck coefficient and thermal conductivity. From the literature review of the individual material properties, one can calculate the figure of merit of silicon-germanium alloys having different germanium concentrations and doping levels. The results are summarized in Figure 3.11 and Figure 3.12.

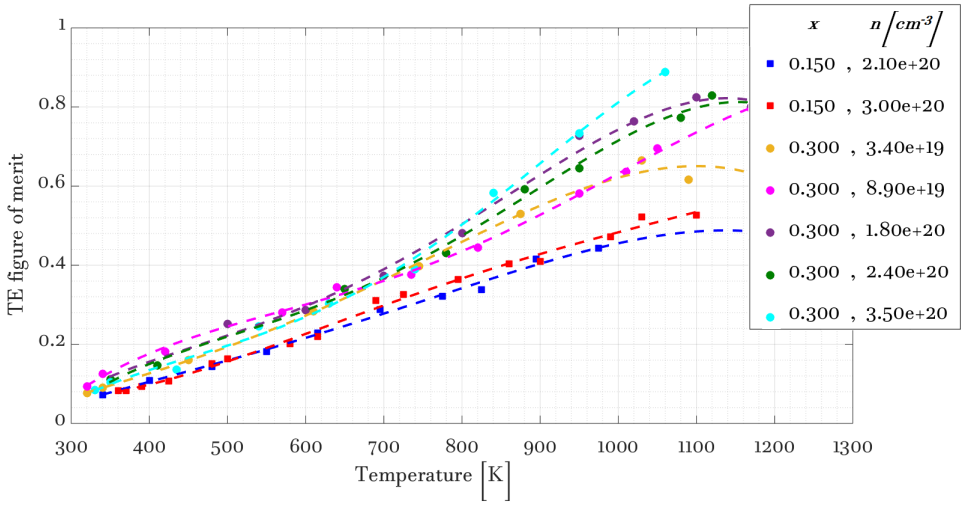



Figure 3.11: Thermoelectric figure of merit of p-type $Si_{1-x}Ge_x$ alloys for different germanium concentration, x, and doping levels, n.

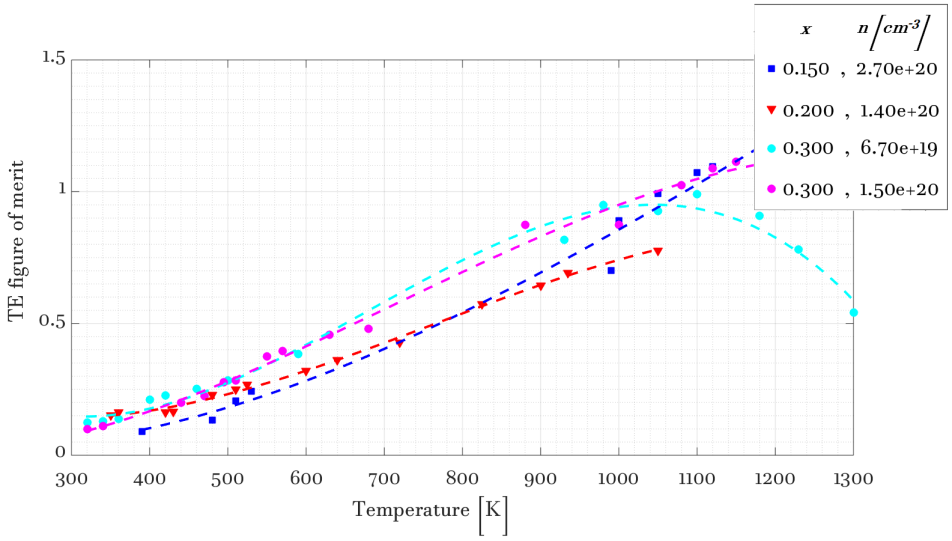



Figure 3.12: Thermoelectric figure of merit of n-type $Si_{1-x}Ge_x$ alloys for different germanium concentration, x, and doping levels, n.

The silicon-germanium alloys reveal the characteristic performance peak at high temperatures. However, $Si_{0.7}Ge_{0.3}$ alloys doped at $10^{19}\,\mathrm{cm}^{-3}$ are also reasonably performing in the mid temperature range (300 °C to 500 °C). With the intent of developing a micro device that could indeed operate in industrial environments, p- and n-type $Si_{0.7}Ge_{0.3}$ alloys doped to $1 \times 10^{19}\,\mathrm{cm}^{-3}$ respectively with phosphorous and boron were selected for the growth. The individual ZT of the materials in the indicated temperature range are respectively of about 0.3 and 0.5.

## 3.3 Epitaxial Growth

The growth mechanism is based on the adsorption of adatoms, which enter the deposition chamber in the form of precursor gases. Since the binding energy of the precursors is larger than the adsorption energy, the atoms laying on the crystal surface exhibit thermal excitation. Thereby, precise control over the diffusion energy is necessary to adsorb the adatoms that would otherwise desorb from the surface of the crystal due to thermal vibrations. Moreover, the diffusion energy is directly related to the temperature of the wafer surface.
Overall, the growth of epitaxial layers occurs through the chemical reaction between the different species (gases and dopants), that flow into the deposition chamber, and the surface of the substrate wafer. The desorbed elements return into the main gas

flow and get carried out of the chamber.

### 3.3.1 Growth Specification

The wafers characterized within this work were grown at IQE Silicon Compounds with an ASM Epsilon 2000 tool [109], see schematic in Figure 3.13.

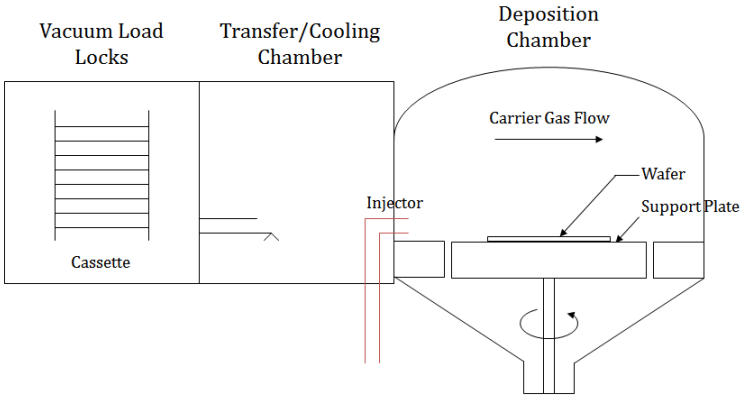



Figure 3.13: Schematic of the ASM Epsilon 2000 CVD chambers.

The Epsilon reactor is specifically designed to grow epitaxial silicon-based films using chemical vapor deposition (CVD). The tool uses a Bernoulli wand system, which allows non-contact high temperature wafer transfer. The reactor also uses integrated lamps to heat the wafer to a precisely controlled temperature, which benefits the uniformity of the silicon layers. Moreover, the tool is optimized to achieve high deposition rates at relatively lower temperatures determining a reduction on the thermal strain in the silicon layers. Silane ($SiH_4$) and germane ($GeH_4$) are the gases used for the growth of the $SiGe$ alloys, while phosphine ($PH_3$) and diborane ($B_2H_6$) were used as precursos for the p- and n-type dopants.
200 mm silicon-on-insulator (SOI) wafers, characterized by 55 nm p-type silicon on top of 155 nm silicon dioxide, were used as substrates for the growth. A 3 µm linearly graded buffer was grown doped at the same level as the active material. Then, the 20 µm $Si_{0.7}Ge_{0.3}$ alloys, doped at $1 \times 10^{19}\,\mathrm{cm}^{-3}$ respectively with phosphorous and boron for n- and p-type, were grown. For such a thick layer of growth material, the expected treading dislocation density is $5 \times 10^{6}\,\mathrm{cm}^{-2}$.

## 3.4 Chapter Conclusions

The chapter introduced the material characteristics which are most relevant for this project. Crystal structure and strain related phenomena in silicon-germanium alloys were described. The thermoelectric properties of bulk silicon-germanium alloys were also presented and analyzed as a function of germanium concentration and doping level, showing the characteristic performance peak at high temperatures ($800 - 900\,°C$). However, $Si_{0.7}Ge_{0.3}$ alloys doped at $10^{19}\,cm^{-3}$ also have good thermoelectric performances in the mid temperature range ($300\,°C$ to $500\,°C$) and were identified as suitable for the development of a micro device aimed at operating in industrial environments. P- and n-type $Si_{0.7}Ge_{0.3}$ alloys doped to $1 \times 10^{19}\,cm^{-3}$ respectively with phosphorous and boron were selected for growth. The CVD epitaxial growth mechanism was delineated.

The assessment and characterization of the grown alloys will be presented in the next chapter through CTLMs and Raman thermometry techniques.

# Chapter 4

# Material Characterization

This chapter focuses on the characterization of the bulk $Si_{0.7}Ge_{0.3}$ alloys grown by CVD for micro-scale thermoelectric applications.
A brief initial section reports an investigation of the quality of the grown material. Wafer inspection is indeed of absolute importance to evaluate whether the material is suitable for micro-/nano-fabrication.
The methods used to perform electrical and thermal characterization of the alloys, Transfer length method (TLM) and Raman thermometry, are then introduced in the following paragraphs. The description of each technique is followed by the respective measurements together with considerations on validity of the obtained results and comparisons with literature values.

## 4.1 Wafer Inspection

The case of very poor crystallinity in the deposited material can be clearly recognised, even by the naked eye, as the surface of the wafer would appear opaque. However, material characterization is generally necessary to inspect the quality of the deposited materials. Techniques such as optical microscopy, atomic force microscopy (AFM) and scanning electron microscopy (SEM) can be used to perform material inspection. Optical microscopy has been used as qualitative and quantitative tool to inspect the material surface. The typical cross-hatch morphology can be identified even with the use of optical microscope, Figure 4.1 (left). A 3D optical profilometer was used to measure the surface roughness as 34 nm rms, Figure 4.1 (right).

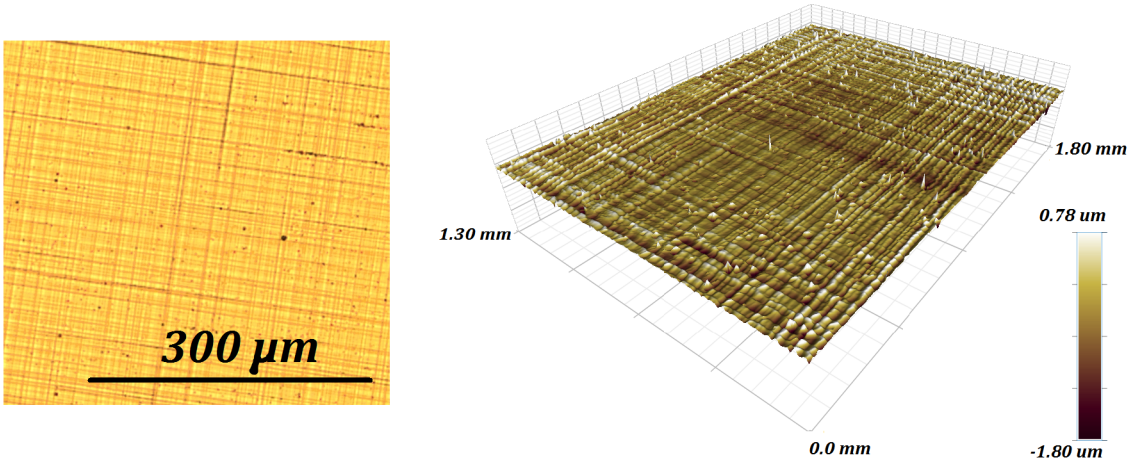



Figure 4.1: Optical microscope (left) and 3D optical profilometer (right) images of the 20 µm $Si_{0.7}Ge_{0.3}$ alloy top surface.

As briefly described in the previous chapter, the relaxation process introduces dislocations and nucleation of islands in the deposited material. SEM images of the top surface and the cross section of the deposited SiGe material clearly confirm the presence of defects, Figure 4.2. In particular, the inverted pyramidal shaped defects are stacking faults, a type of defect that characterize the disorder of crystallographic planes. The incorrect stacking of crystal planes in the deposited material is generally associated with the local presence of partial dislocations.

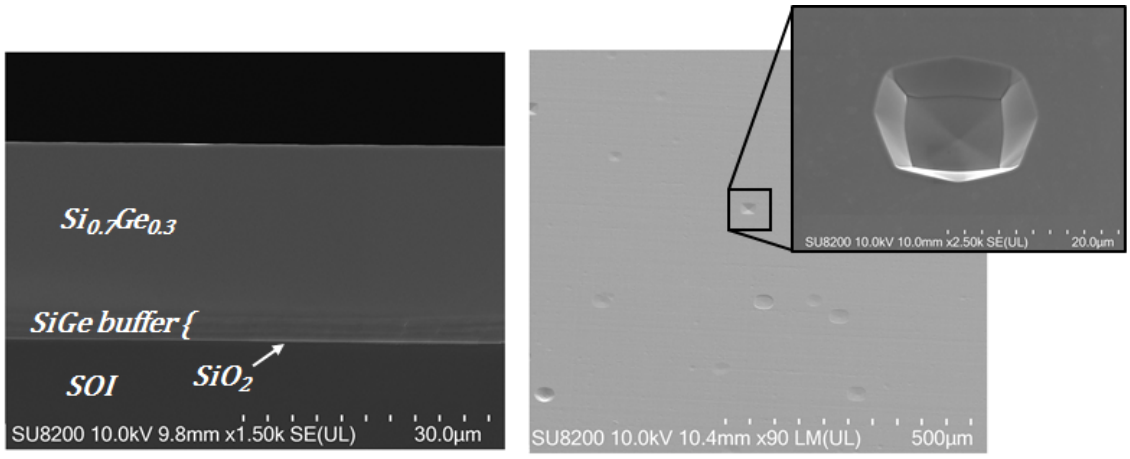



Figure 4.2: SEM images of cross-section (left) and top surface (right) of the 20 µm $Si_{0.7}Ge_{0.3}$ alloy. The inset illustrates a closer view of a stacking fault.

## 4.2 Electrical Characterization

It has already been shown in Chapter 2 that the electrical conductivity directly affects the thermoelectric performance of a material, as it appears in the formulation of the figure of merit. In addition, it is intuitively desirable for a power generator to have a small internal resistance. This concept is analytically expressed in Equation 2.15. The latter, describing the power output of a thermoelelctric generator, also highlights the relevance of the contact resistance contribution to the total internal resistance.
In this work, two different germanosilicides, formed reacting the silicon-germanium alloys with evaporated nickel and platinum, have been investigated. Particular interest was directed towards formation temperature and specific contact resistivity of the germanosilicide. The characterization of the junctions has been performed through TLM structures. The technique, as explained in the following section, also allows measurement of the sheet resistance of the semiconductor layer. Thereby, the electrical conductivity of both p- and n-type $Si_{0.7}Ge_{0.3}$ layers has been extracted.

### 4.2.1 Transfer Length Method

The transfer length method [110, 111] is a technique used to determine contact resistance, $R_c$, and specific contact resistivity, $\rho_c$, of Ohmic metal-semiconductor junctions. The method is based on the linear relationship between the resistance and the gap spacing between the contacts. Current crowding, nonhomogeneous distribution of current density at the edge of the contacts, constitutes the main limitation of the TLM technique. To avoid the problem, circular TLM (CTLM) structures have been introduced [110–112]. The typical arrangement for a CTLM pattern, shown in Figure 4.3, consists of identical circular contacts of radius $r$ and different gap spacing $d_i$.
To characterize the CTLM structures, a pair of probes is used to drive a DC current between the inner and the outer metal contacts, while a second set of probes senses the voltage drop across the gap spacing. The use of two sets of probes is recommended for more accurate measurements as it eliminates the contribution of the probe to metal contact resistance. The measured resistance increases with the size of the gap spacing of the contact under examination, as it can be seen from the measurements performed on nickel germanosilicide in Figure 4.4. However, the non-linear relationship can be then modified into a linear one through a correction factor. The total resistance, $R_T$, measured between the contacts in the circular configuration can be expressed as:

$$R_T = \frac{R_{sh}}{2\pi r}(d_i + 2L_t)C \tag{4.1}$$

where the correction factor $C$ is defined as:

$$C = \frac{r}{d_i} ln \left(1 + \frac{d_i}{r}\right) \tag{4.2}$$

The intercept of the linear fit with y-axis yields twice the value of contact resistance, while the x-axis intercept corresponds to twice the value of the transfer length, $L_t$. From the slope of the linear fit, the sheet resistance, $R_{sh}$, of the semiconducting layer can also be calculated. The electrical conductivity of the thin film can then be extracted as:

$$\sigma = \frac{1}{tR_{sh}} \tag{4.3}$$

where $t$ is the thickness of the thin film.
Finally, the specific contact resistivity can be derived as:

$$\rho_c = R_{sh} L_t^2 \tag{4.4}$$

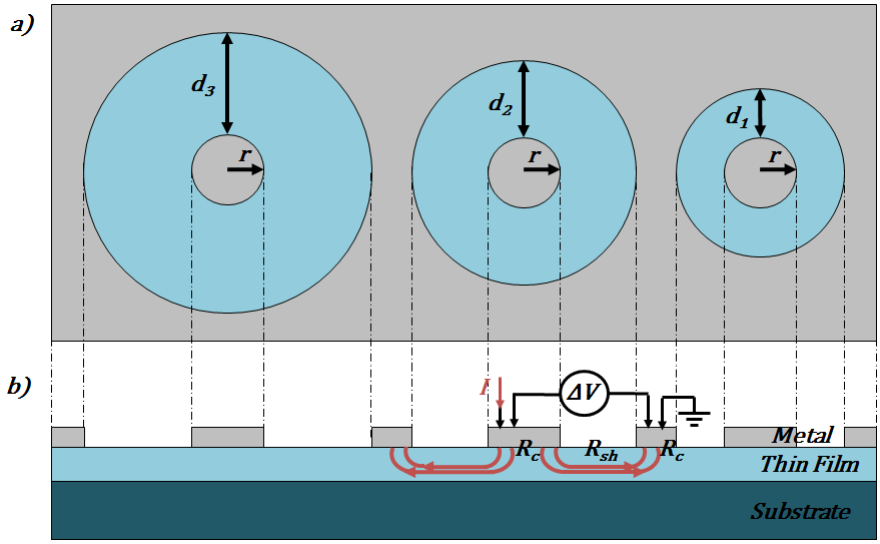



Figure 4.3: a) Top and b) cross-sectional views of the typical CTLM structure.

#### 4.2.1.1 Nickel Germanosilicide

CTLMs with 150 , 200 and 250 µm inner diameters and gap spacing ranging from 10 µm to 200 µm were patterned by photolithography. 10 nm of Ni, 50 nm of Pt and 100 nm of Ni were deposited by electron-beam evaporation and annealed at 340 °C for 30 s in $N_2$ enviromnent [113, 114]. The Ni layer at the bottom of the metal stack formed the germanosilicide, while the Pt layer acted as diffusion barrier to prevent the top Ni to diffuse in the silicon-germanium alloy. The CTLM structures were

measured as a function of the gap spacing in order to extract the contact resistivity of the metal-semiconductor junction. Figure 4.4 presents an example of the data collected in the case of 250 µm inner diameter structures patterned on both n- and p-type $Si_{0.7}Ge_{0.3}$. The resulting values for the 250 µm inner diameter arrangement are listed in Table 4.2.

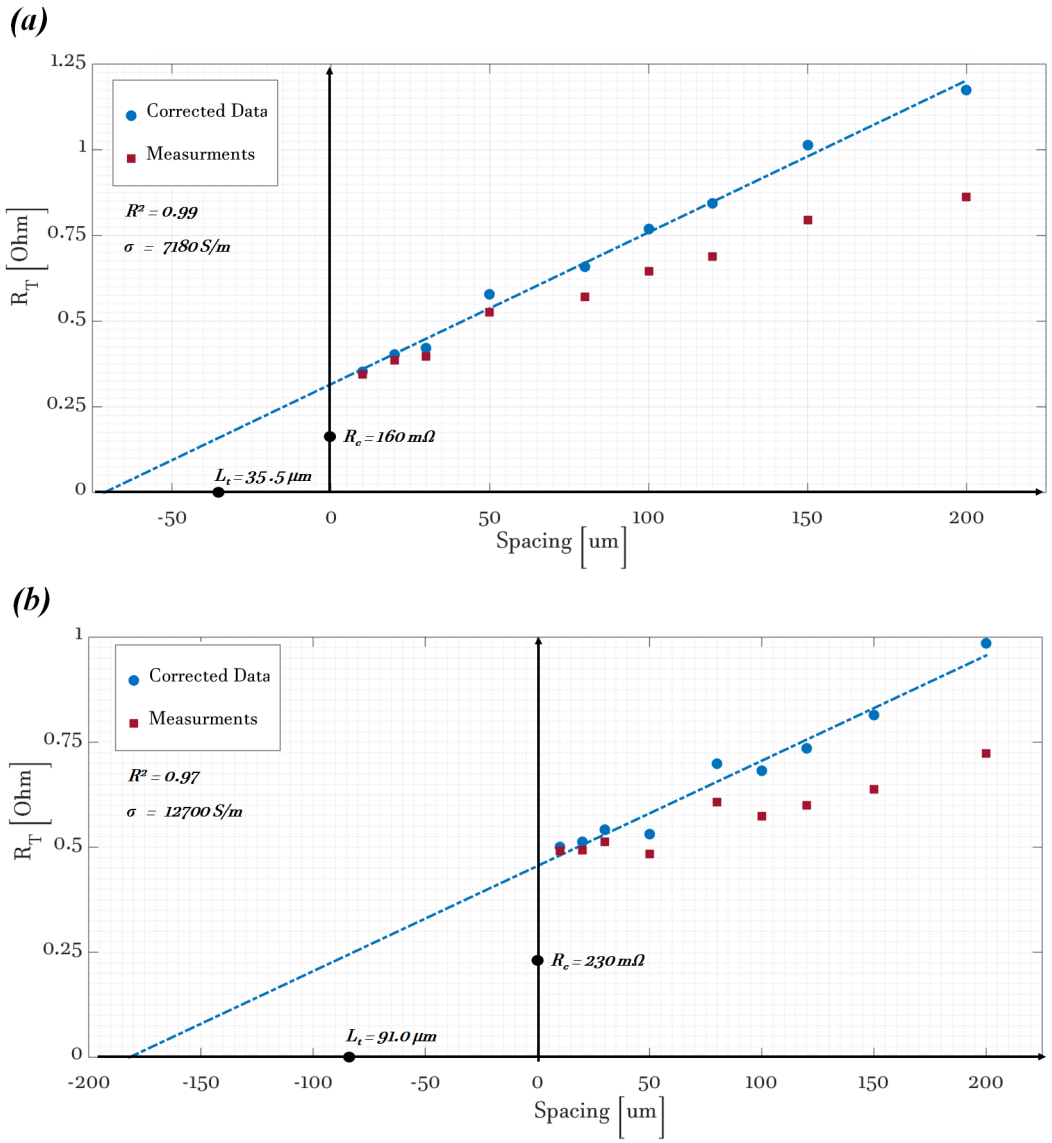



Figure 4.4: Total resistance, $R_T$, versus gap spacing for corrected and uncorrected data in the case of 250 µm inner diameter CTLM structures patterned on: (a) n- and (b) p-type $Si_{0.7}Ge_{0.3}$ respectively.

| | $r[\mu m]$ | $R^2$ | $R_c[\Omega]$ | $L_t[\mu m]$ | $\rho_c[\Omega cm^2]$ | $\sigma[S/m]$ |
|---|---|---|---|---|---|---|
| **n-type** $Si_{0.7}Ge_{0.3}$ | 250 | 0.99 | 0.160 | 35.5 | $9.0\times10^{-5}$ | 7200 |
| **p-type** $Si_{0.7}Ge_{0.3}$ | 250 | 0.97 | 0.230 | 91.0 | $3.2\times10^{-4}$ | 12700 |

Table 4.1: Summary of data extracted from the 250 µm CTLM structures. $R^2$ is the coefficient of determination; ranging from 0 to 1, it indicates the quality of the data fitting.

Ohmic contacts with contact resistivity of $9.0\pm1.8\times10^{-5}\ \Omega\,\mathrm{cm}^2$ and $3.1\pm0.4\times10^{-4}\ \Omega\,\mathrm{cm}^2$ were respectively obtained for n- and p-type highly doped $Si_{0.7}Ge_{0.3}$ alloys. The main advantage of nickel germanosilicide contacts is that less silicon-germanium is consumed compared to titanium or cobalt contacts [115, 116]; thereby, the risk of "spiking" shallow junctions is reduced. However, the low resistivity nickel germanosilicide phase is only stable up to about 400 °C, thereby it does not suit the requirements of mid-temperature thermoelectric applications.

#### 4.2.1.2 Platinum Germanosilicide

Platinum germanosilicides were also investigated through CTLMs with different inner diameters, from 150 to 250 µm, and gap spacings, from 10 µm to 200 µm, patterned by photolithography. 100 nm of Pt were deposited by electron-beam evaporation and annealed at different temperatures, ranging from 500 to 750 °C for 30 s in an $N_2$ environment. As shown in Figure 4.5, the contact resistivity of CTLM structures was extracted as a function of the annealing temperature, revealing a minimum at 600 °C. Ohmic contacts with contact resistivity as low as $6.5 \pm 0.5\times10^{-5}\ \Omega\,\mathrm{cm}^2$ and $1.5 \pm 0.5\times10^{-4}\ \Omega\,\mathrm{cm}^2$ were respectively obtained on n- and p-type highly doped $Si_{0.7}Ge_{0.3}$ alloys. The extracted values are comparable to the ones obtained for the nickel germanosilicide contacts. Moreover, the fabrication process is equally simple, as it only involves metal evaporation and rapid thermal annealing. However, the formation temperature of the platinum germanosilicide guarantees thermal stability over the desired operation temperature of the devices.
The same CLTM arrangements have been used to extract the electrical conductivity of the $Si_{0.7}Ge_{0.3}$ alloys, which was $12000 \pm 1200\,\mathrm{S\,m^{-1}}$ for the p-type and $7200 \pm 700\,\mathrm{S\,m^{-1}}$ for the n-type.

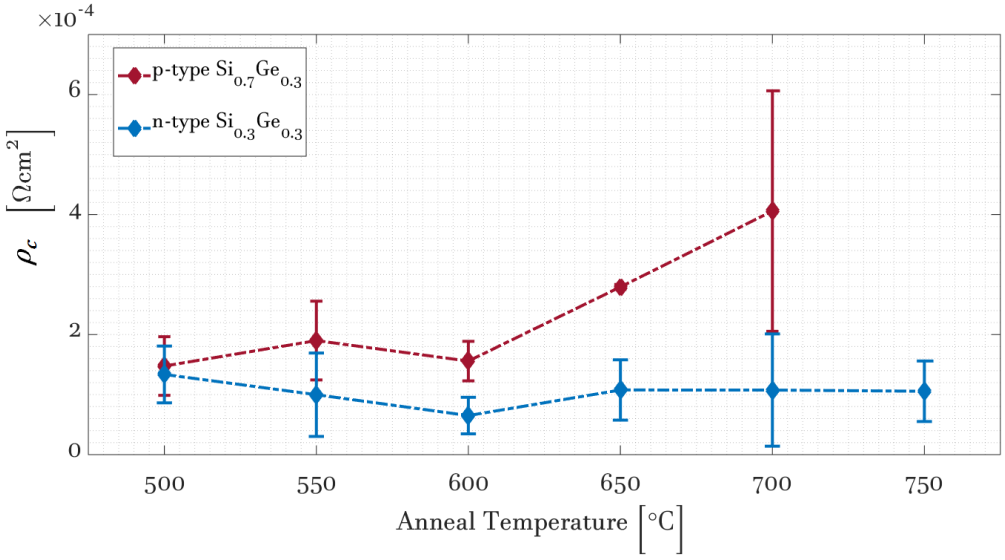



Figure 4.5: Contact resistivity, $\rho_c$, of Pt germanosilicide versus anneal temperature.

| | | $r[\mu m]$ | $R^2$ | $R_c[\Omega]$ | $L_t[\mu m]$ | $\rho_c[\Omega cm^2]$ | $\sigma[S/m]$ |
|---|---|---|---|---|---|---|---|
| 500 °C | **n-type** $Si_{0.7}Ge_{0.3}$ | 250 | 0.97 | 0.250 | 43.0 | $1.40\times10^{-4}$ | 6900 |
| | **p-type** $Si_{0.7}Ge_{0.3}$ | 250 | 0.92 | 0.290 | 62.5 | $1.60\times10^{-4}$ | 12200 |
| 550 °C | **n-type** $Si_{0.7}Ge_{0.3}$ | 250 | 0.90 | 0.210 | 47.5 | $9.90\times10^{-5}$ | 7400 |
| | **p-type** $Si_{0.7}Ge_{0.3}$ | 250 | 0.95 | 0.280 | 53.0 | $1.900\times10^{-4}$ | 10700 |
| 600 °C | **n-type** $Si_{0.7}Ge_{0.3}$ | 250 | 0.96 | 0.200 | 31.0 | $6.50\times10^{-5}$ | 7100 |
| | **p-type** $Si_{0.7}Ge_{0.3}$ | 250 | 0.94 | 0.260 | 50.5 | $1.50\times10^{-4}$ | 11900 |
| 650 °C | **n-type** $Si_{0.7}Ge_{0.3}$ | 250 | 0.97 | 0.250 | 41.0 | $1.10\times10^{-4}$ | 6700 |
| | **p-type** $Si_{0.7}Ge_{0.3}$ | 200 | 0.97 | 0.310 | 71.5 | $2.80\times10^{-4}$ | 10500 |
| 700 °C | **n-type** $Si_{0.7}Ge_{0.3}$ | 250 | 0.95 | 0.270 | 51.0 | $1.15\times10^{-4}$ | 7000 |
| | **p-type** $Si_{0.7}Ge_{0.3}$ | 200 | 0.90 | 0.350 | 60.0 | $4.10\times10^{-4}$ | 12400 |
| 750 °C | **n-type** $Si_{0.7}Ge_{0.3}$ | 250 | 0.90 | 0.290 | 32.5 | $1.20\times10^{-4}$ | 7100 |
| | **p-type** $Si_{0.7}Ge_{0.3}$ | 250 | - | - | - | - | - |

Table 4.2: Summary of data extracted from the 250 µm CTLM structures. $R^2$ is the coefficient of determination; ranging from 0 to 1, it indicates the quality of the data fitting.

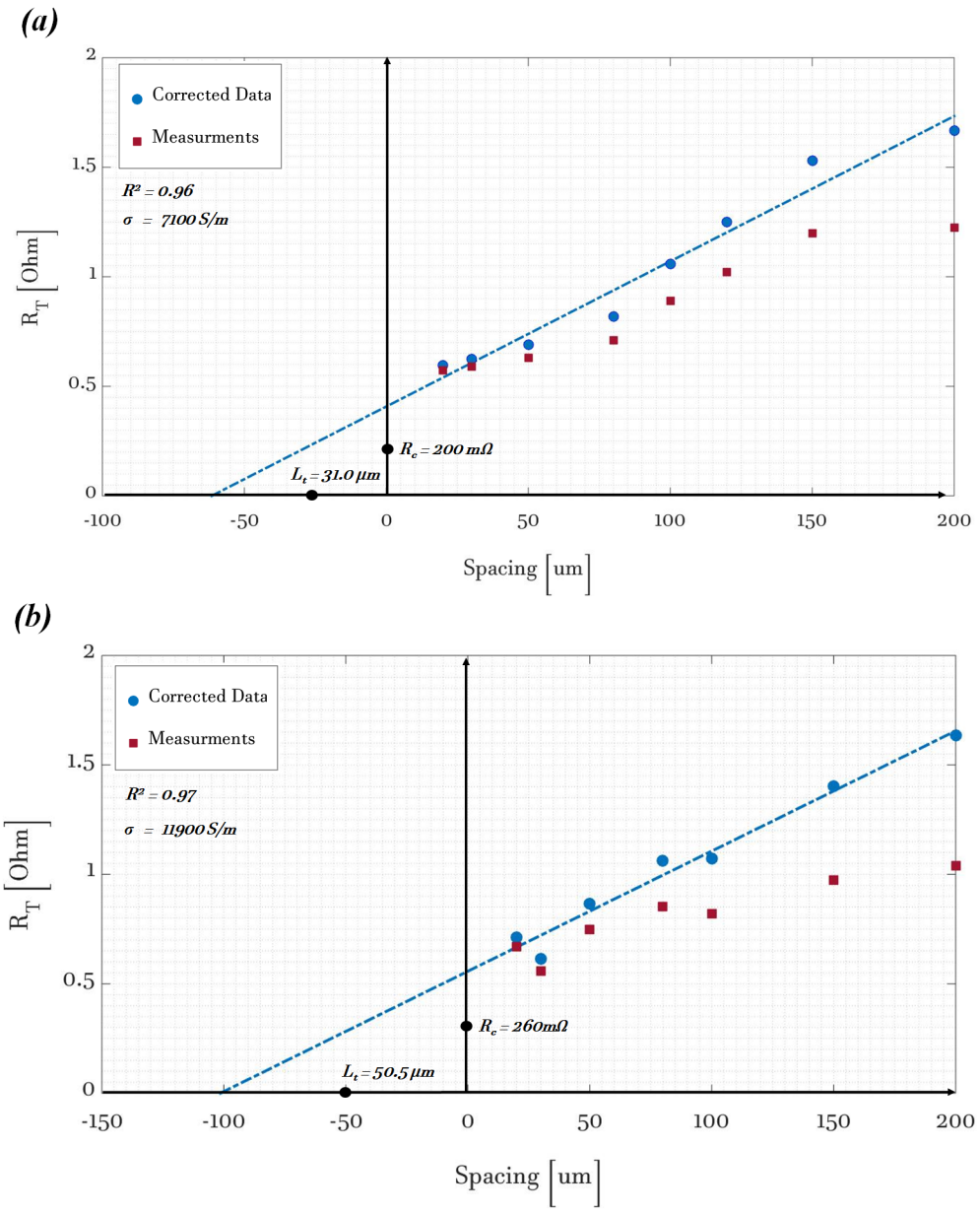



Figure 4.6: Total resistance, $R_T$, versus gap spacing for corrected and uncorrected data in the case of 250 µm inner diameter CTLM structures patterned on: (a) n- and (b) p-type $Si_{0.7}Ge_{0.3}$ respectively and annealed at 600 °C for 30 s in an $N_2$ environment.

## 4.3 Thermal Characterization

Micro-scaled thermoelectrics rely on low thermal conductivity materials and on their ability to sustain temperature differences across micro and nano structures. At these length scales, the measurement of heat transfer is extremely challenging with many of the traditional measurement techniques becoming insensitive or unsuitable.
The thermal diffusivity of samples having rather large dimensions and defined thickness can be measured by the laser flash method [117]. Flat thin films in good thermal junction with the underlying substrate can be inspected through the $3\omega$ technique [118]. Scanning thermal microscopy (SthM) can map local temperature and thermal conductivity with nano-scale resolution through the use of a thermocouple or a bolometer probe [119]. When the temperature dependence of the reflectivity of a material is well defined and known, optical pump and probe spectroscopies (time, or frequency, domain thermoreflectance (TDTR)) are ideal for the study of the thermal properties of thin films, interfaces and nanostructures [120].
The Raman shift method, also known as Raman thermometry, is another optical technique which is capable of measuring the thermal conductivity of materials. Based on Raman spectroscopy [121], the technique only became popular after being used for the thermal characterization of suspended graphene [122, 123]. It is now widely used and it has already been extended to other materials, such as carbon nanotubes, Si, SiGe, Ge and GaAs [124–127].
In the following paragraphs, the principles of the Raman shift method are presented together with calibration of the temperature metrics. Finally, the characterization performed on the SiGe films is reported.

### 4.3.1 Raman Thermometry

Raman spectroscopy has the ability of observing vibrational, rotational and other low-frequency modes in a system. The technique relies on the inelastic scattering, or Raman scattering, of the monochromatic light of a laser. The laser light interacts with both atoms/molecules and molecular vibrations, phonons or other excitations in the system. Most of the incident photons are elastically scattered (Rayleigh scattering), thereby they conserve their initial energy. However, of every $10^6$ photons, one is scattered by an excitation mode and its resulting energy is either shifted up (anti-Stokes scattering) or down (Stokes scattering). The energy shift $\Delta k$ of Stokes and anti-Stokes scattered light reveals information about the vibrational modes in the system.

Temperature directly affects energy, lifetime and population of phonons; thereby, thermal perturbations of a system determine changes in the peak position ($\nu$), linewidth ($\Gamma$) and intensity ($I_P$) of both Stokes and anti-Stokes signals in the Raman spectrum. If correctly correlated to temperature, the Stokes/anti-Stokes ratio, peak shift and linewidth broadening can be used as thermometer [128]. In practice, peak position and linewidth are the spectrum properties mostly utilized as a temperature metric. In traditional Raman thermometry, the uncertainty on the measured Raman temperature is directly related to the uncertainty in the calibration of the metric and also indirectly related to the uncertainty in the determination of the spectrum properties of interest. The random nature of the Raman process leads to a random number of photons at each wavelength being emitted from the sample surface. The integral of the number of photons over an infinite time scale converges at a distribution matching the representative fitting function. However, camera saturation and slight differences in the response of each pixel, limit the ability to converge towards the distribution function. This uncorrelated noise in the spectrum determines uncertainties in peak position, linewidth and intensity, which consequently leads to uncertainty in the temperature measurements.

#### 4.3.1.1 Experimental System

A WITech alpha 300 Raman microscope, schematics in Figure 4.7, was used for all the spectral acquisitions discussed in this study. The microscope, characterized by a 180° backscattering geometry, is connected via optical fibre to a 532 nm $Nd:YVO_4$ laser. The scattered light is fibre-coupled to the UHTS 300 spectrometer through a slit of 100 µm width. With a 1600 pixels thermoelectrically cooled charge coupled device (CCD) detector and a highly performing spectrometer (300 mm focal length and 2400 grooves/mm (BLZ=500 nm) diffraction grating) a spectral resolution of 3 $cm^{-1}$ was obtained. The discrete Raman spectra were fitted to a Voigt function in order to achieve subpixel sensitivity and uncertainties of $\pm$ 0.01 $cm^{-1}$ on the Stokes/anti-Stokes peak position. As an example, in the case of silicon, a spectral uncertainty of $\pm$ 0.01 $cm^{-1}$ translates into a temperature uncertainty of $\pm$ 1 °C.
The Raman spectrum collects the contribution of the whole region of the sample where the laser light is scattered. In most of the Raman spectroscopy experiments, the temperature distribution is not homogeneous over the volume of the sample due to the inhomogeneous excitation and the thermal conductance of the sample itself. Thereby, the temperature deduced from the Stokes shift, defined as Raman temperature $T_{Raman}$, differs from the local temperature, $T(x, y, z)$, of the sample. A physical

formulation can be developed in Cartesian coordinates assuming that the surface of the sample lays in the $xy$ plane, while the laser beam is oriented along the z direction. The Raman temperature can be analytically described as the integral of the local temperature weighted by local excitation density $H(x, y)$ and attenuation along the incident direction of the laser beam $g(T(x, y, z), z)$, [126, 129]:

$$T_{Raman} = \frac{\iiint T(x, y, z)\, H(x, y)\, g(T(x, y, z), z)\, dx\, dy\, dz}{\iiint H(x, y)\, g(T(x, y, z), z)\, dx\, dy\, dz} \tag{4.5}$$

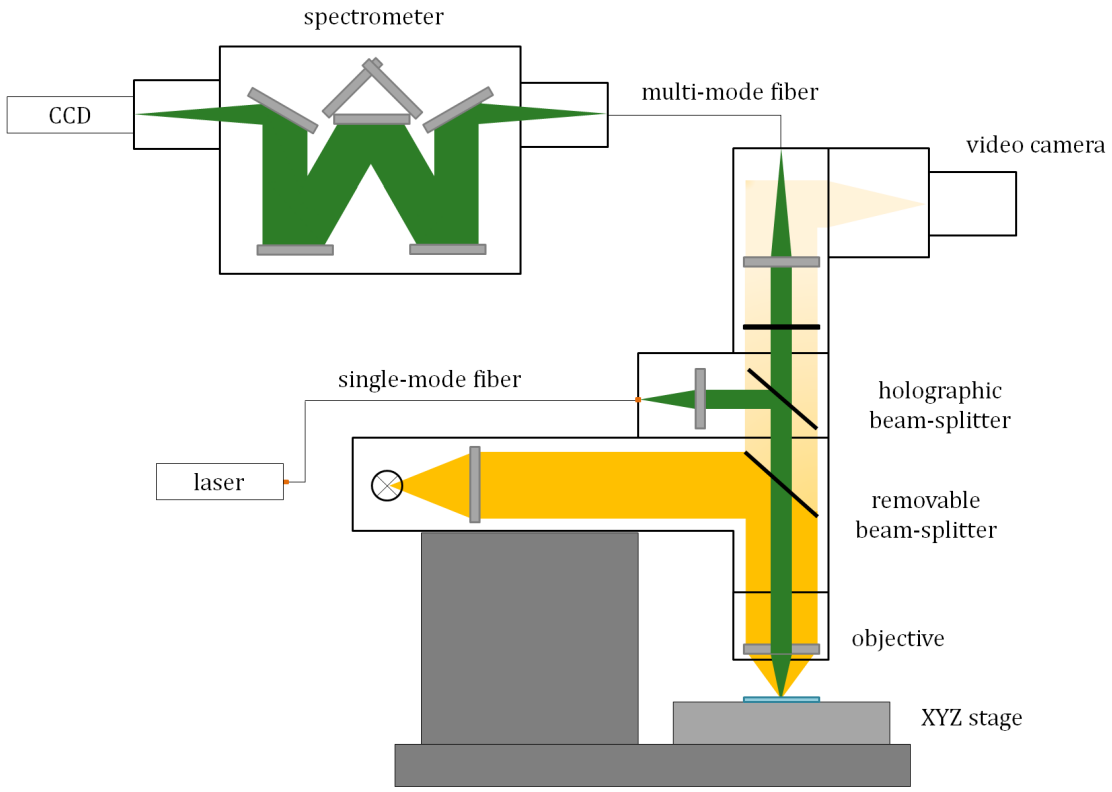



Figure 4.7: Schematic of WITech alpha 300 Raman microscope utilized in this work.

In this study, a Gaussian profile laser has been used to thermally excite the sample. Thereby, the excitation power density results: $H(x, y) = \frac{2P}{\pi w^2}\, e^{\frac{-2\,(x^2+y^2)}{w^2}}$, where $w$ is the $1/e^2$ beam radius and $P$ the total laser power. Moreover, the exponential attenuation of light in the sample depth is described by Beer-Lambert's law as: $g(T(x, y, z), z) = A_c(T(x, y, z)) \cdot e^{-A_c(T(x,y,z))z}$, where $A_c(T(x, y, z))$ is the temperature dependent absorption coefficient of the material. As a simple approximation it can be assumed that $A_c(T(x, y, z))$ is temperature independent and therefore constant for the material.

The local temperature of the sample is not only related to the excitation power, but also to the thermal properties of the sample. Heat diffusion in solids is described by the following partial differential equation:

$$q(x,y,z,t) = \rho(T(x,y,z,t))C_p(T(x,y,z,t))\frac{\partial T(x,y,z,t)}{\partial t} + \\ - \nabla \cdot (k(T(x,y,z,t))\nabla T(x,y,z,t)) \tag{4.6}$$

where $q(x,y,z,t)$ is the heat flow per unit volume and $\rho(T(x,y,z,t))$, $C_p(T(x,y,z,t))$ and $k(T(x,y,z,t))$ are respectively the temperature dependent density, heat capacity and thermal conductivity of the material.
In stationary conditions, $\frac{dT(x,y,z,t)}{dt} = 0$, Equation 4.6 becomes:

$$q(x,y,z) = -\nabla \cdot (k(T(x,y,z))\nabla T(x,y,z)) = \\ = -\nabla k(T(x,y,z))\nabla T(x,y,z) - k(T(x,y,z))\Delta T(x,y,z) \tag{4.7}$$

The volumetric thermal source $q(x,y,z)$ can be expressed, according to the Gaussian profile of the laser beam and the BeerLambert law, as:

$$q(x,y,z) = \frac{2P(1-R)A_c}{\pi w^2}\, e^{\left(\frac{-2(x^2+y^2)}{w^2}\right)} e^{-A_c z} \tag{4.8}$$

where $R$ is the reflectance of the material.

#### 4.3.1.2 Numerical Simulations

In this work, the temperature distribution has been calculated from the three dimensional stationary problem, Equation 4.7, by numerical analysis based on the finite element method (FEM) computed using the software COMSOL®. A bulk $1\,\mathrm{cm}^2$ specimen has been considered for this study. The sample is thermally excited by a green light laser beam incident on the center of its top surface. The pump-probe domain, used to both apply the volumetric excitation and to weight average the local temperature to then calculate the Raman temperature, is defined by the laser beam profile and the material absorption depth. The bottom and lateral surfaces of the specimen are assumed to be fixed at room temperature, while the top surface is considered to be exposed to natural convection with the surrounding environment. A representative scheme of the 3D heat diffusion problem is reported in Figure 4.8.

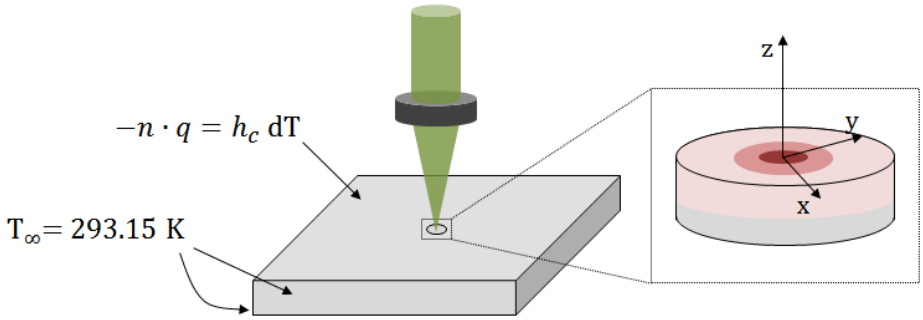



Figure 4.8: Schematic representation of the three dimensional heat diffusion problem under investigation. The inset shows the cylindrical domain where the volumetric heat source is applied. The boundary conditions are assumed to be isothermal at the bottom and sides of the sample ($T_\infty = 293.15\,\mathrm{K}$). The top surface of the sample exchanges heat with the surrounding environment via natural convection (n is the unit vector normal to the surface, q is the heat flux, $h_c$ is the convection coefficient of air and dT is the temperature difference between sample and environment).

Due to the large aspect ratio of the geometrical model, domain partitioning and adaptive mesh refinement are necessary to guarantee accuracy of the calculated solution. Figure 4.9 reveals the distribution of mesh tetrahedrons; the discrete elements are smaller in the volume surrounding the laser spot and progressively increasing in size while moving towards the specimen boundaries. The quality of the generated mesh has been checked and maintained within acceptable ranges, with an average element quality of about 0.7 and minimum element quality above 0.2. The quality index evaluates the distortion of the mesh elements, ranging from 0 (degenerated element) to 1 (perfect tetrahedron). Low element quality could lead to matrix singularities, thereby preventing the convergence of the solution.
Further tests to prove the mesh independence of the converged solution have also been performed (Figure 4.10). The test is conducted by maintaining the same mesh refinement parameters (i.e. element growth rate, curvature factor, resolution of narrow regions etc.) and only varying the size of the mesh elements in the different domain partitioning. A larger number of elements does not necessarily correspond to higher result accuracy if not coupled with correct adaptive mesh options.

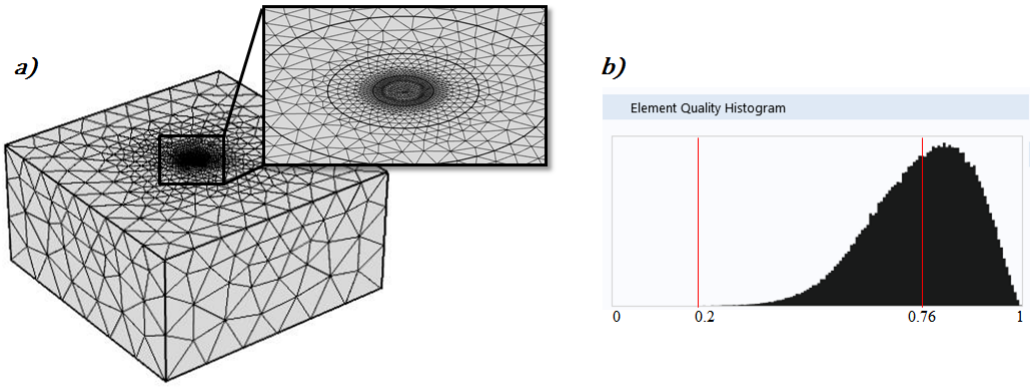



Figure 4.9: a) Illustrative schematic of the geometrical domain partitioning and adaptive meshing. The inset shows the cylindrical domain where the volumetric heat source is applied. b) The associated element quality histogram is also reported. The x-axis and y-axis respectively display element quality and number of elements.

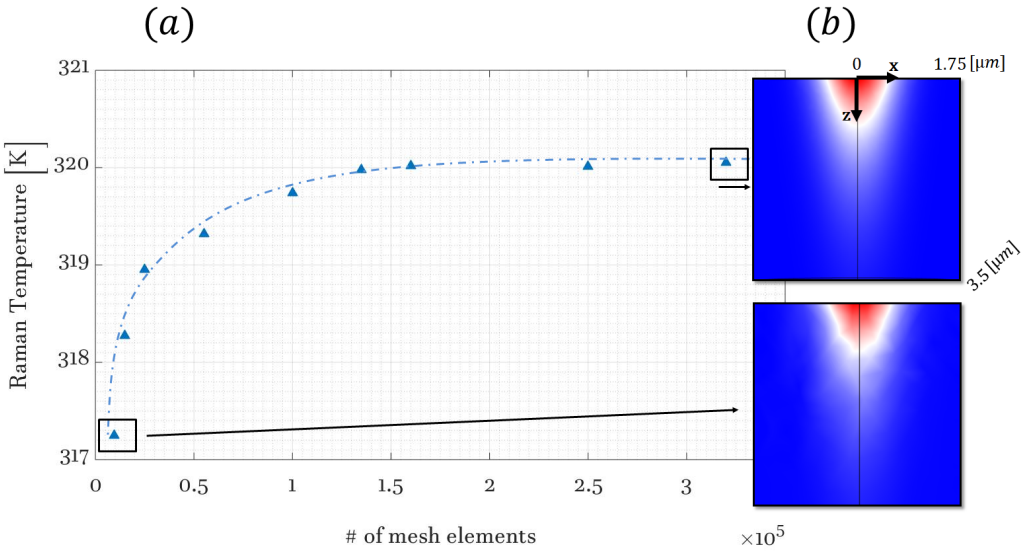



Figure 4.10: a) The graph presents the values of calculated Raman temperature for a different size/number of meshing elements discretizing the domain. b) Illustrative schematic of the laser light intensity at the cross section of the absorption domain for coarse and fine discretization. Both the graph and schematic refer to the case of a bulk silicon substrate heated by the 30 mW optical power of a 532 nm laser beam with a 860 nm $1/e^2$ radius.

#### 4.3.1.3 Measurements

A 532 nm laser beam, having Guassian intensity profile and 860 nm $1/e^2$ beam radius, was focused on the sample through a 20X objective having 0.5 numerical aperture. To avoid laser heating during the calibration process, Raman spectra were acquired for decreasing levels of power until no further shift in the Stokes peak could be detected. An incident power of 100 µW was thereby selected as described; integration times and spectrum accumulations were adjusted in order to maintain a clearly defined Stokes peak. Every acquired spectrum was then fitted to a Voigt function in order to extract the Stokes peak position. The calibration measurements were conducted for different temperatures (from 25 °C to 85 °C) of the TEG controlled heated stage.
The extracted temperature dependence of the Stokes peak position was confirmed to be linear in the temperature range examined, as shown in Figure 4.11 and Figure 4.13.
In the case of bulk silicon and bulk germanium, Stokes peak shift coefficients of $-0.0241 \pm 0.0002\,\mathrm{cm^{-1}\,K^{-1}}$ and $-0.0215 \pm 0.0002\,\mathrm{cm^{-1}\,K^{-1}}$ were obtained respectively. The results are in good agreement with data already reported in literature [129, 130].

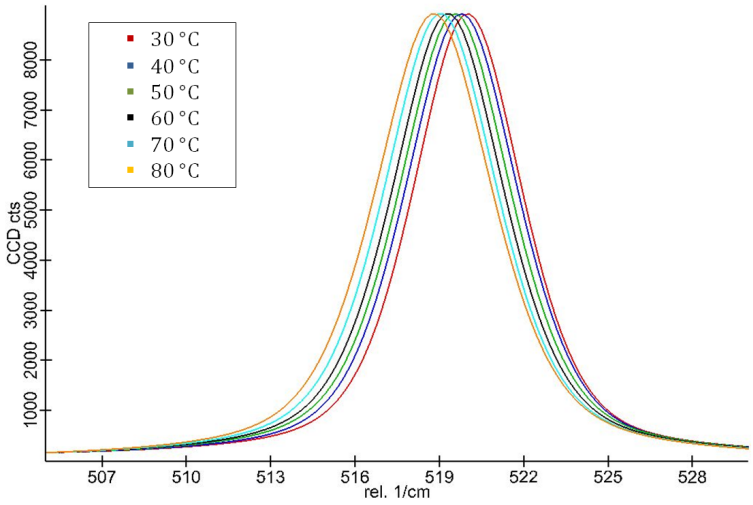



Figure 4.11: Raman spectra of a bulk silicon sample acquired for increasing temperatures of the heated stage. The background noise of the signals was filtered and the spectra were then fitted to a Voigt distribution function. The figure reveals a clear shift of the Stokes peak position with temperature.

The Raman spectrum of SiGe alloys is characterized by three Stokes peaks,

Figure 4.12, which are attributed to optic modes of Si-Si, Si-Ge and Ge-Ge atom pairs [131, 132].

The dependence of the Raman line shift on temperature was calculated for all the three different peaks and summarized in Figure 4.13 with respect to the values of bulk silicon and germanium. A Raman shift coefficient of $-0.0239 \pm 0.0008\,\mathrm{cm^{-1}\,K^{-1}}$ was obtained for the Si-Si mode, while $-0.0231 \pm 0.004\,\mathrm{cm^{-1}\,K^{-1}}$ and $-0.0133 \pm 0.004\,\mathrm{cm^{-1}\,K^{-1}}$ were respectively extracted for the Si-Ge and Ge-Ge modes. Although the values are in good agreement with earlier works [132], only the Raman shift coefficient for the Si-Si modes was used for further analysis. At such Ge concentration and optical input power, the Stokes peaks of the Ge-Si and Ge-Ge modes are less defined than the Si-Si mode peak. Being characterized by large noise levels, the Raman shift coefficients of the Ge-Ge and Ge-Si modes would lead to large uncertainties in the determination of the Raman temperature. Through the Raman shift coefficients, any shift in the Stokes peak position could now be correlated with the equivalent change in temperature.

Raman spectra were then acquired for different incident optical power. The corresponding Raman temperatures were calculated from the shift in the Stokes position. Numerical simulations were performed sweeping the value of material thermal conductivity until the Raman temperature obtained from simulation matched the value experimentally extracted.

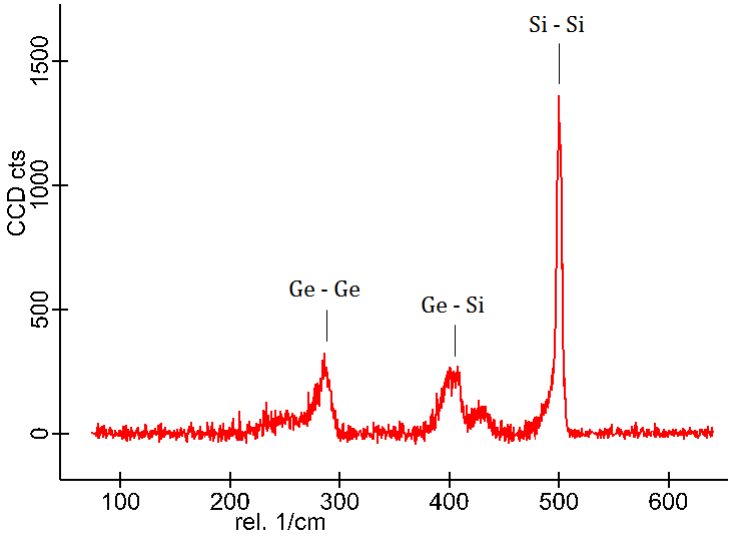



Figure 4.12: Room temperature Raman spectrum of bulk $Si_{0.7}Ge_{0.3}$.

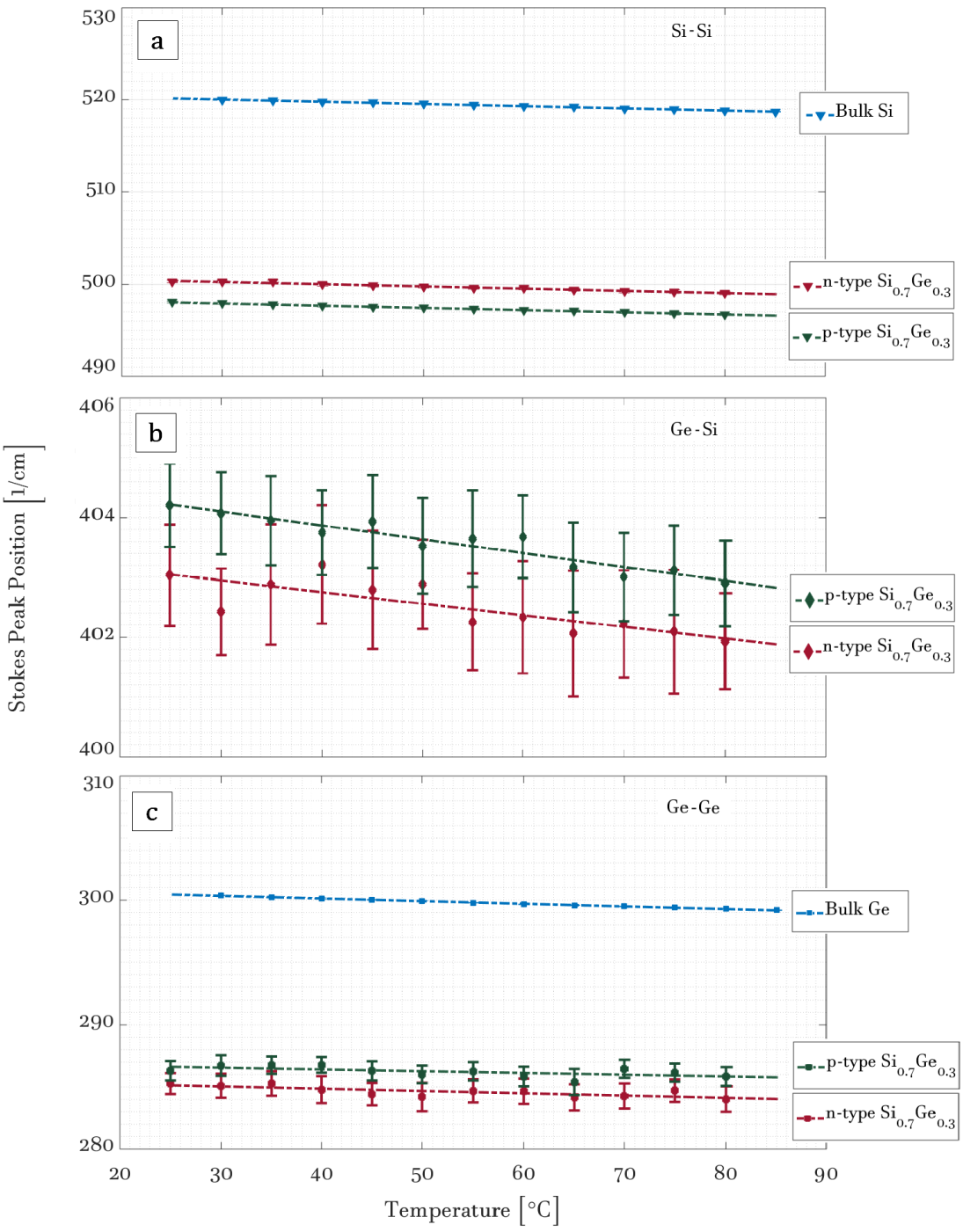



Figure 4.13: Temperature dependent Stokes peak position of the three $Si_{0.7}Ge_{0.3}$ modes in comparison to the ones of bulk silicon and germanium. The Raman shifts of the Si-Si mode are calculated from the slope of the lines in a). The same can be done for the Si-Ge mode, b), and Ge-Ge mode, c).

#### 4.3.1.4 Results

Each sample was tested at different values of incident optical power. Since the temperature rise in the experiments never exceeds 100 K, the simulations were run under the assumption of temperature-independent thermal conductivity of the material. Moreover, in the case of bulk germanium, given the small absorption depth at 532 nm, surface absorption was assumed. Finally, the parameters used for FEM simulations are listed, together with the values of thermal conductivity extracted from fitting, in Table 4.3.

| Parameter | *Bulk Si* | *Bulk Ge* | $Si_{0.7}Ge_{0.3}$ |
|---|---|---|---|
| Laser spot $1/e^2$ radius [nm][a] | 860 | 860 | 860 |
| Abs. Coeff. [$\mu m^{-1}$][b] | 0.889 | 56.40 | 2.29 |
| Reflectivity [%][b] | 37.35 | 51.8 | 40.9 |
| | | | p- / n-type |
| $\Rightarrow$ k [W/mK] | 150.5 ± 8.5 | 59.9 ± 2.3 | 5.9 ± 0.6 / 5.6 ± 0.6 |

[a] Values extracted from knife edge measurements.
[b] Values calculated from ellipsometer measurements as:
$Abs.\ Coeff. = \frac{4\pi\,\mathrm{Im}\{\underline{n}\}}{\lambda}$ and $Reflectivity = \frac{1}{2}\left(\frac{\mathrm{Re}\{\underline{n}_{air}\}\cos\theta_i - \mathrm{Re}\{\underline{n}_{material}\}\cos\theta_t}{\mathrm{Re}\{\underline{n}_{air}\}\cos\theta_i + \mathrm{Re}\{\underline{n}_{material}\}\cos\theta_t}\right)^2$
where $\underline{n}$ is the complex refractive index, $\theta_i$ and $\theta_t$ are the incidence and transmission angles lined as $\mathrm{Re}\{\underline{n}_{air}\}\sin\theta_i = \mathrm{Re}\{\underline{n}_{material}\}\sin\theta_t$.
The ellipsometer measurement are taken at Brewster's angle.

Table 4.3: Parameters used for simulation.

The values obtained for bulk silicon and germanium samples, 150.5 ± 8.5 W/mK and 59.9 ± 2.3 W/mK respectively, show good agreement with fudamental literature works [104, 107, 108], confirming confidence in the method.
In the case of $Si_{0.7}Ge_{0.3}$ alloys, the extracted thermal conductivity, 5.9 ± 0.6 W/mK and 5.6 ± 0.6 W/mK for p- and n- type respectively, also matches expectations [104].
A summary of the performed experiments and extracted values is reported in Figure 4.14 and 4.15.

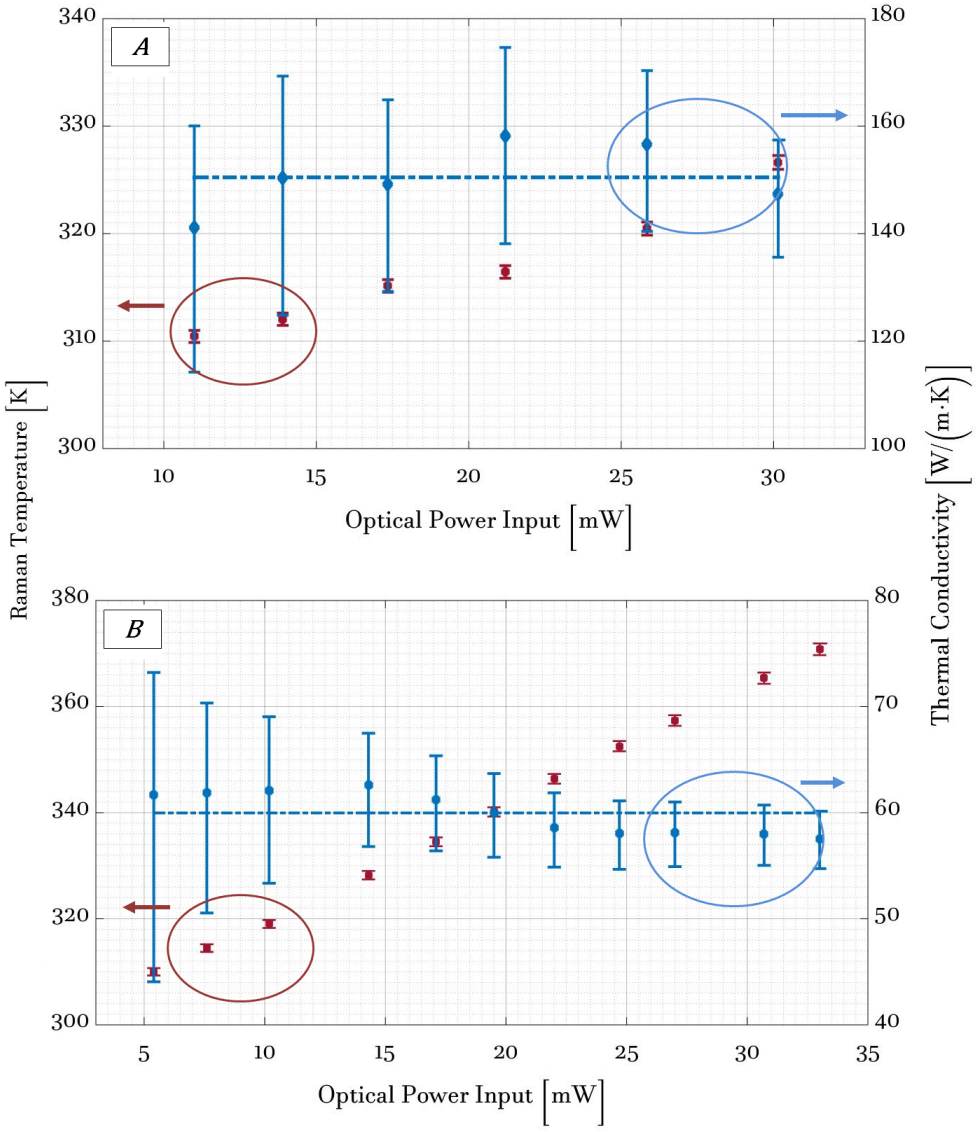



Figure 4.14: The graphs present the experimental values of Raman temperature (red dataset) and the fitted values of thermal conductivity (blue dataset) obtained at different optical incident powers in the case of bulk silicon (a) and bulk germanium (b) samples respectively.

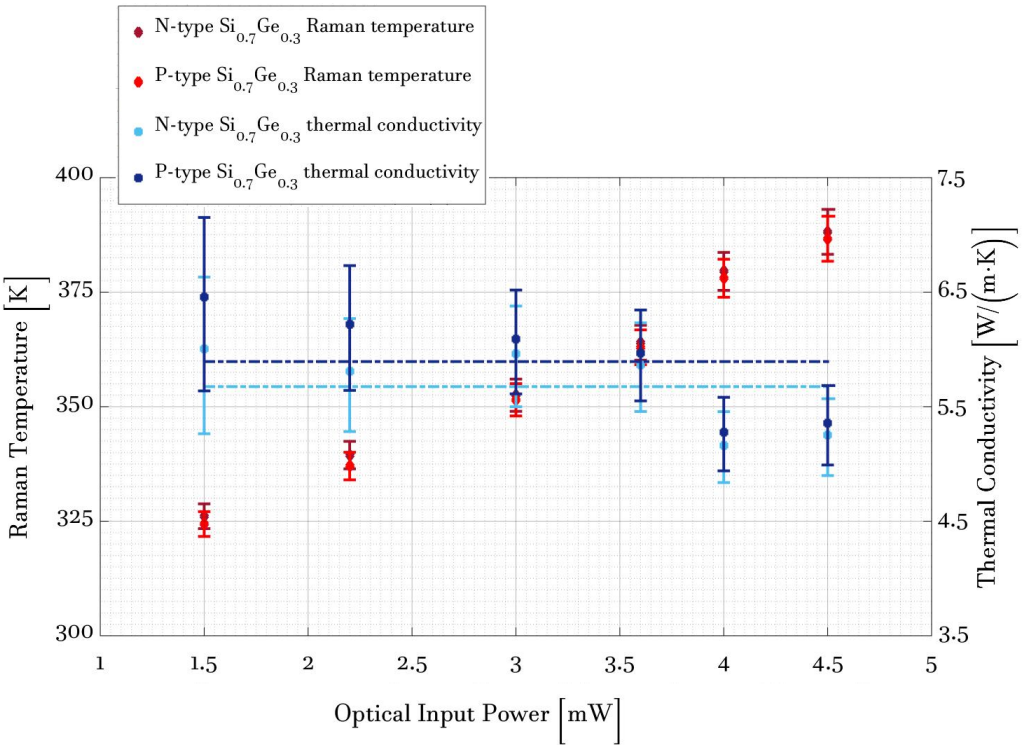



Figure 4.15: The graph illustrates the experimental values of Raman temperature and the fitted values of thermal conductivity for a given optical incident power in the case of p- and n-type $Si_{0.7}Ge_{0.3}$ samples.

## 4.4 Chapter Conclusions

P- and n-type highly doped $Si_{0.7}Ge_{0.3}$ wafers have been inspected and their eligibility for microfabrication was assessed. Despite high defectivity, the thermoelectric properties of the wafers have been examined through the application of traditional, CTLMs, and more recent, Raman thermometry, techniques.

The materials characterized showed good agreement with expectations and previous literature works. Low resistivity Ohmic contact were specifically designed to sustain the desired operation temperatures (300-500 °C).

All the values obtained from the material characterization have been used as input parameters for the design of the complete thermoelectric device, as presented in the following chapter.

# Chapter 5

# Modeling and Design of a $\mu$TEG

This chapter presents the preliminary modeling undertaken to design the $Si_{0.7}Ge_{0.3}$ $\mu$TEGs together with the device layout consequently adopted for fabrication.
First, constant temperature gradient modeling is introduced, followed by the case study of a $Si_{0.7}Ge_{0.3}$ micro-scaled thermoelectric module operating in cross-plane heat-flow geometry. The maximum power output of the micro device, performing under a fixed temperature gradient, is calculated as a function of the number and geometry of the thermoelectric legs. The simulations thereby provide design suggestions for optimized power generation in specific operating conditions. Finally, the layout selected for fabrication is presented and explained.

## 5.1 Modeling of $\mu$TEGs Operating at Constant Temperature Gradient

In most practical applications the operation of thermoelectric generators relies on the limited thermal energy available, rather than on a constant temperature gradient. However, constant temperature gradient modeling offers a much more intuitive and simplified approach to device design.
It has already been demonstrated [133, 134], that for a thermoelectric generator operating in thermal steady-state with a constant temperature gradient, the electrical power produced only depends on the electrical load connected to its terminals. Moreover, in such conditions, the power output is maximized when the impedance of the load matches the internal resistance of the generator. Thereby, the maximum electrical power is achieved at half of the open-circuit voltage, or analogously at half of the short-circuit current.

However, when the impedance of the connected load is larger than the internal resistance of the thermoelectric generator, the current flowing through the device is smaller than half of the short-circuit current. Consequently, the "parasitic" Peltier effect is reduced if compared to the case of maximum electrical power operation. Such conditions are often favorable, leading to increased thermal efficiency of the system due to the lower thermal load connected to it. On the contrary, operation at load impedance smaller than the internal resistance of the thermoelectric generator leads to reduced thermal efficiency of the system.

The field of thermoelectrics currently focuses almost its entire attention on synthesis and investigation of new promising materials, while only a niche of the literature researches improved designs and architectures for thermoelectric devices. A few works [135, 136] have already adopted numerical modeling to investigate the optimum design of thermoelectric devices working at constant temperature gradient. Analogously, constant heat operation has also been studied [137, 138].

Further investigations on the optimum ratio of the cross-sectional areas of p- and n-type thermoelectric legs also suggest the n-type design to be smaller than the p-type one [139]. Moreover, the operation of thermoelectric devices in combination with non-ideal heat sinks has also been considered in modeling case studies [140–142]. The present analysis aims at investigating the performance of a $Si_{0.7}Ge_{0.3}$ $\mu$TEG operating at constant temperature gradient for varying number, spacing and size of p- and n-type legs. The study is completely independent of the effect of heat exchangers and associated thermal contact resistances.

### 5.1.1 Modeled System

The generic thermoelectric heat recovery system, represented in Figure 5.1, has been studied under the hypothesis of one dimensional heat flow and a constant temperature gradient. In the derived analytical solution, the effect of heat exchangers and associated thermal contact resistances have been neglected. However, the electrical contact resistances, together with the effect of air conduction and convection, are considered.

The system consists of a $Si_{0.7}Ge_{0.3}$ module sandwiched between a heat source and a heat sink, respectively maintained at $T_h$ and $T_c$, and connected in series to an electric load, $R_L$. The $\mu$TEG is made of $N$ thermoelectric leg pairs. The n- and p-type legs have different cross-sectional area, respectively $A_n$ and $A_p$, and equal length, $L$.

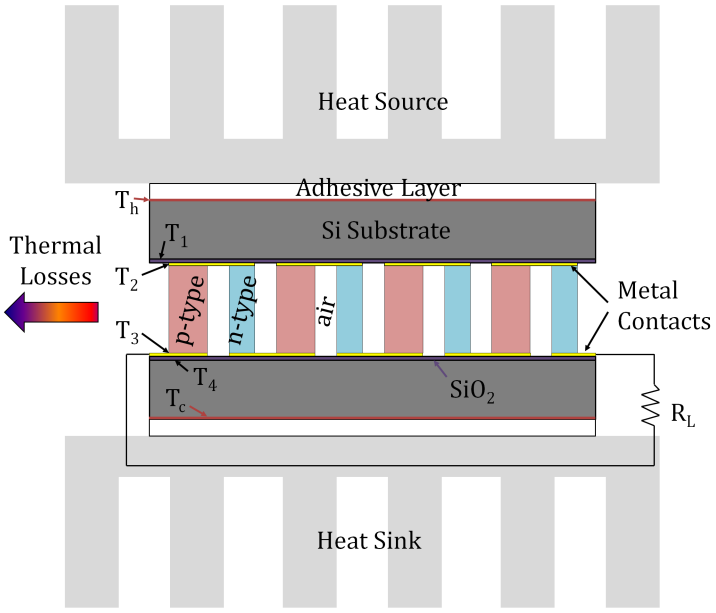



Figure 5.1: Schematic of the thermoelectric heat recovery system under investigation. The $Si_{0.7}Ge_{0.3}$ micro-module is sandwiched between heat source and heat sink and connected in series to an electric load.

In the steady state, the thermoelelctric system described above can be analytically modeled through a system of equations. The electrical equivalent of the thermal model analyzed in this study is presented in Figure 5.2.

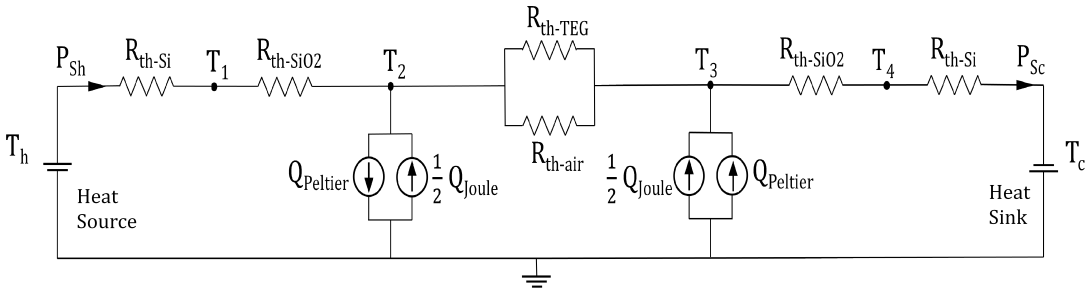



Figure 5.2: Electrical equivalent schematic of the thermal circuit employed to model the thermoelectric heat recovery system under investigation. The terms indicated with $R_{th}$ represent the thermal resistance of the specified components. The thermal resistance of heat source and sink has not been considered, as well as the corresponding thermal contact resistances at the interfaces. Moreover, any in-plane heat flow is also neglected.

The power absorbed from the heat source and flowing through the SOI substrate of the module can be expressed as:

$$P_{S_h} = \frac{kappa_{Si} A_{TEG} (T_h - T_1)}{t_{Si}} = \frac{kappa_{SiO_2} A_{TEG} (T_1 - T_2)}{t_{SiO_2}} \tag{5.1}$$

where $kappa_{Si}$ and $kappa_{SiO_2}$ are the thermal conductivity of silicon and silicon dioxide, $t_{Si}$ and $t_{SiO_2}$ are the thicknesses of the silicon and silicon dioxide layers respectively, $A_{TEG}$ is the cross-sectional area of the thermoelectric device, $T_1$ is the temperature at the interface between the silicon and the silicon dioxide insulating layer and $T_2$ is the temperature at the interface between the silicon dioxide and the $Si_{0.7}Ge_{0.3}$ thermoelectric legs.
The heat absorbed by the active thermoelectric region instead presents a combination of Fourier heat transfer, Peltier effect and Joule heating completed with the effects of air convection and conduction:

$$P_{S_h} = N(\alpha_p - \alpha_n) I T_2 + N\frac{\kappa_p A_p (T_2 - T_3)}{L} + N\frac{\kappa_n A_n (T_2 - T_3)}{L} + \\ + \frac{\kappa_{air} A_{air} (T_2 - T_3)}{L} + h_{air} A_{air} (T_2 - T_3) - \frac{1}{2} R_{int} I^2 \tag{5.2}$$

where $\alpha_p$ and $\alpha_n$ are the Seebeck coefficient of p- and n-type $Si_{0.7}Ge_{0.3}$ legs respectively, $\kappa_p$ and $\kappa_n$ are the thermal conductivity of p- and n-type thermoelectric materials, $h_{air}$ and $\kappa_{air}$ are convective coefficient and thermal conductivity of air and $A_{air}$, defined as $A_{TEG} - N(A_p + A_n)$, is the area occupied by air between the legs of the active region. $I$ is the current flowing in the system and $R_{int}$ is the internal resistance of the $\mu$TEG. The power generated inside the device by Joule heating, $R_{int} I^2$, recombines in equal parts towards heat source and heat sink.
Analogously, the heat flowing towards the heat sink can be expressed through the following equations, each of which corresponds to the different layers of the module:

$$P_{S_c} = N(\alpha_p - \alpha_n) I T_2 + N\frac{\kappa_p A_p (T_2 - T_3)}{L} + N\frac{\kappa_n A_n (T_2 - T_3)}{L} + \\ + \frac{\kappa_{air} A_{air} (T_2 - T_3)}{L} + h_{air} A_{air} (T_2 - T_3) + \frac{1}{2} R_{int} I^2 \tag{5.3}$$

$$P_{S_c} = \frac{kappa_{SiO_2} A_{TEG} (T_3 - T_4)}{t_{SiO_2}} = \frac{kappa_{Si} A_{TEG} (T_4 - T_c)}{t_{Si}} \tag{5.4}$$

where $T_3$ is the temperature at the interface between the $Si_{0.7}Ge_{0.3}$ thermoelectric legs and the silicon dioxide layer, and $T_4$ is the temperature at the interface between the silicon dioxide layer and the silicon substrate. Both $T_3$ and $T_4$ refer to interfaces on the cold side of the module.

Moreover, the balance between the heat flow through the system and the internal heat generation can be expressed as:

$$P_{S_h} - P_{S_c} = R_{int} I^2 \tag{5.5}$$

where:

$$I = \frac{N(\alpha_p - \alpha_n)(T_2 - T_3)}{R_{int} + R_L} \tag{5.6}$$

and

$$R_{int} = \frac{N\rho_p L}{A_p} + \frac{2N\rho_{pc}}{A_p} + \frac{N\rho_n L}{A_n} + \frac{2N\rho_{nc}}{A_n} \tag{5.7}$$

with $\rho_p$ and $\rho_n$ being the electrical resistivity of p- and n-type materials, while $\rho_{pc}$ and $\rho_{nc}$ are the respective contact resisitivity.
The thermolelectric conversion efficiency of the module can also be calculated as:

$$\eta = \frac{R_L I^2}{P_{S_h}} \tag{5.8}$$

Neglecting the effects of air conduction and convection, it has been already derived in Equation 2.9 and 2.10 that the efficiency of the module can be optimized through the thermoelectric figure of merit ZT, Equation 2.12. It can be further calculated that the ratio between the cross-sectional area of p- and n-type legs that maximizes the thermoelectric efficiency is [22, 133]:

$$\frac{A_p}{A_n} = \sqrt{\frac{(\rho_p L + 2\rho_{pc})\kappa_n}{(\rho_n L + 2\rho_{nc})\kappa_p}} \tag{5.9}$$

While dealing with $\mu$TEGs, the electrical contact resistivity does play a significant role in reducing the output power and it cannot be neglected during modeling. Considering the parameters listed in Table 5.1, the optimum ratio of the cross-sectional area of p- and n-type legs calculated from Equation 5.9 is 1.75. As a comparison, for a macroscale thermoelelctric systems (L>>20 µm) based on the same active materials, the electrical contact resistance can be neglected leading to an optimum cross-sectional area ratio of 0.73.
The system of nonlinear equations composed of the above expressions, from Equation 5.1 to Equation 5.7, was solved in MatLAB for different numbers and geometries of the thermoelectric legs.

### 5.1.2 Optimization of Legs Geometry and Packing Factor

In Chapter 4 of this work, the $Si_{0.7}Ge_{0.3}$ thermoelectric material was characterized at room temperature. Thereby, despite the aim of fabricating a $Si_{0.7}Ge_{0.3}$ $\mu$TEG capable of operating at mid temperatures, the initial module modeling makes the assumption of near room temperature operation for simplicity in device development and process feedback.

The cross-sectional area of the micro-generator was fixed at $1\,cm^2$. $T_h$ and $T_c$ were assumed to be 330 K and 300 K respectively. The material properties, listed in Table 5.1, were considered to be temperature independent and fixed at their room temperature values. Moreover, the on load modeling assumed an electrical load of $50\,\Omega$ to be connected in series with the $\mu$TEG.

| **Parameter** | $Si$ Substrate | $SiO_2$ Layer | Air | $Si_{0.7}Ge_{0.3}$ p-type | $Si_{0.7}Ge_{0.3}$ n-type |
|---|---|---|---|---|---|
| t [µm] | 600 | 0.155 | 20 | 20 | 20 |
| $\kappa$ [W/mK] | 148 [a] | 1.4 [a] | $2.53\times10^{-2}$ [a] | 5.9 [b] | 5.6 [b] |
| $h$ [W/m$^2$K] | - | - | 50[a] | - | - |
| $\alpha$ [µV K$^{-1}$] | - | - | - | 260 [a] | -180 [a] |
| $\rho$ [$\Omega$ cm] | - | - | - | $8.33\times10^{-3}$ [b] | $1.38\times10^{-2}$ [b] |
| $\rho_c$ [$\Omega$ cm$^2$] | - | - | - | $1.5\times10^{-4}$ [b] | $6.5\times10^{-5}$ [b] |

[a] Value from literature [104, 143, 144].
[b] Value measured in this work, see Chapter 4.

Table 5.1: Parameters used for the modeling of the $Si_{0.7}Ge_{0.3}$ $\mu$TEGs.

The performance of $\mu$TEGs was investigated as a function of the number and geometry of the thermoelectric legs. Electrical power output, Figure 5.3, and corresponding operating voltage, Figure 5.4, were plotted versus the ratio between the cross-sectional area of p- and n-type legs for different values of $N$. Such graphical results reveal the optimum number of thermoelectric legs pairs, $N = 64$, and the optimum ratio between the cross-sectional area of p- and n-type legs, 1.66, which is in good agreement with the prediction from Equation 5.9. However, it must be noted that the simulated values highlight the leg geometry that optimizes the electrical power output of the device, while Equation 5.9 refers to the maximum efficiency point. As mentioned before, the maximum power output and maximum efficiency do not necessarily match in constant temperature operation.

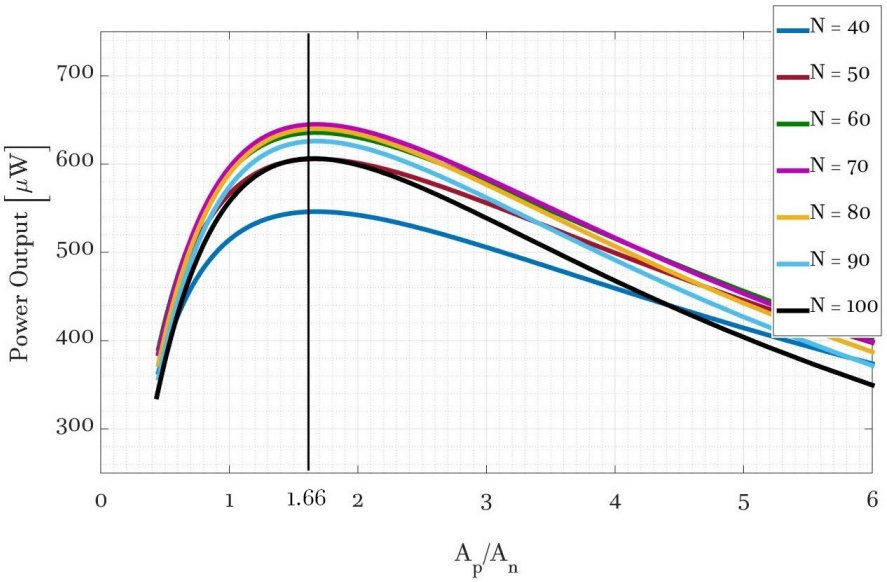



Figure 5.3: Maximum electrical power output plotted versus the ratio between the cross-sectional area of p- and n-type legs for different numbers of leg pairs. The simulations refer to the case described in Section 5.1.2 and Table 5.1.

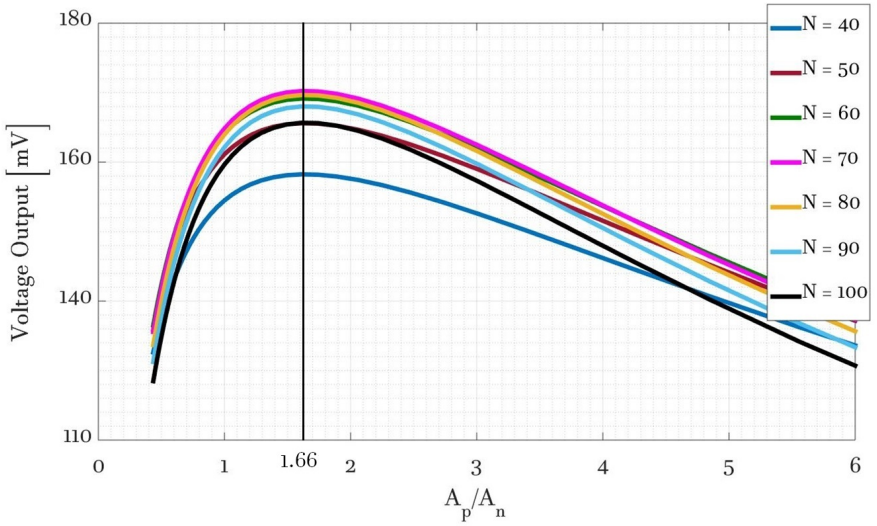



Figure 5.4: Output voltage in the maximum electrical power output operation plotted versus the ratio between the cross-sectional area of p- and n-type legs for different numbers of leg pairs. The simulations refer to the case described in Section 5.1.2 and Table 5.1.

The maximum electrical power output and the corresponding voltage are plotted for a fixed number of thermoelelctric legs pairs, $N = 64$, versus the width of p- and n-type legs in Figure 5.5 and Figure 5.6 respectively. Such investigations guided the choice of the design geometry adopted for the $\mu$TEGs fabricated in this work.
64 thermoelelctric leg pairs, with p- and n-type cross-sectional areas respectively of $250 \times 250$ µm$^2$ and $150 \times 150$ µm$^2$, were considered. The device is expected to reveal a room temperature internal resistance of 50 Ω and an effective thermal conductance of 1.61 W K$^{-1}$ at open-circuit. In addition, the micro-device is expected to produce an output power of about 640 µW at a voltage of 175 mV when operating with a 30 K temperature gradient and connected to a 50 Ω electrical load.

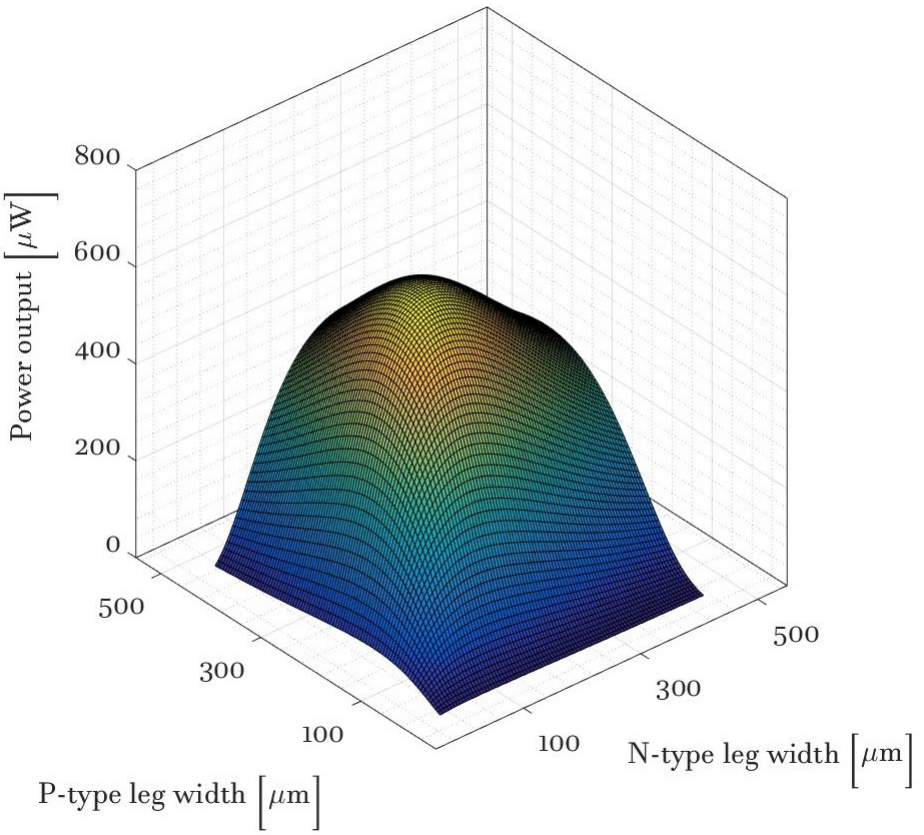



Figure 5.5: Maximum electrical power output plotted versus the width of p- and n-type legs. The study considers the case of a $Si_{0.7}Ge_{0.3}$ $\mu$TEG device made of 64 leg pairs connected to a 50 Ω electrical load and operating at 30 K temperature gradient. The simulation parameters are listed in Table 5.1.

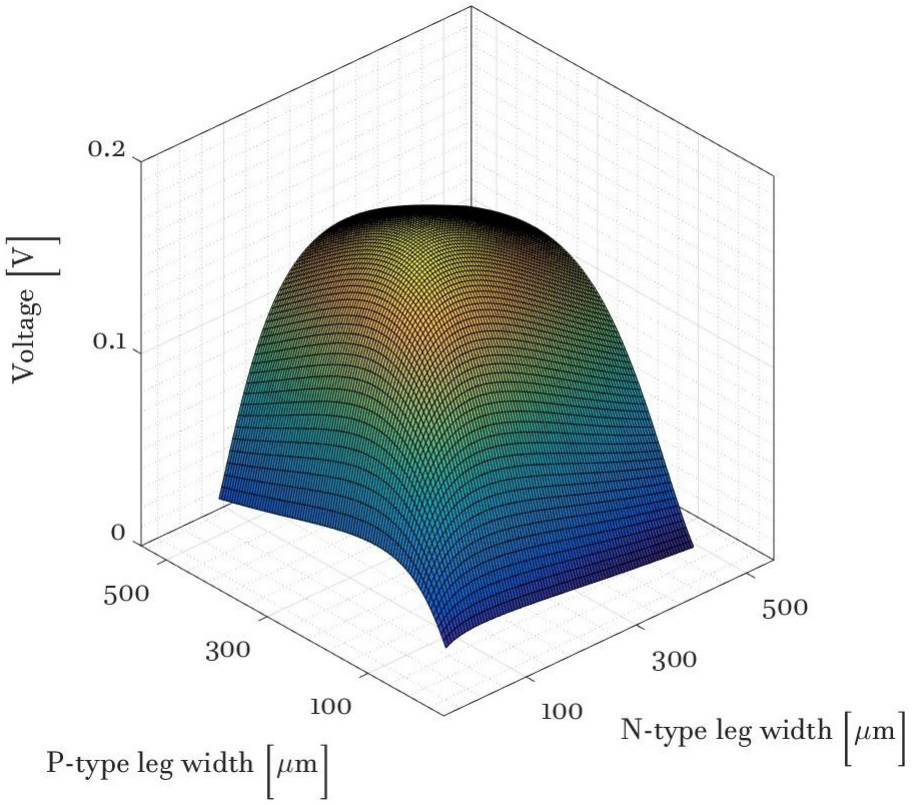



Figure 5.6: Voltage output at maximum electrical power output operation plotted versus the width of p- and n-type legs. The study considers the case of a $Si_{0.7}Ge_{0.3}$ $\mu$TEG device made of 64 leg pairs connected to a 50 Ω electrical load and operating at 30 K temperature gradient. The simulation parameters are listed in Table 5.1.

## 5.2 Micro-Fabrication Design

Once the desired geometry of the thermoelectric generator is identified, the layout of the device has to be designed in accordance with the fabrication process. In this work, the layered structure of the $\mu$TEGs is dictated by the two subsequent dry-etching steps of the active $Si_{0.7}Ge_{0.3}$ material and by the following metal depositions of contacts and electrical access lines. P- and n-type thermoelectric materials were considered to be processed separately and flip-chip bonded at a final stage. A detailed insight of the fabrication process will be however presented in Chapter 6.

The top view of the designed layout of the p- and n-type halves of the device is schematically reported in Figure 5.7. Both p- and n-type chips present 64 thermoelectric legs, each of which sits on a 5 µm thick isolation block. Such a structure is necessary to guarantee the electrical continuity of the thermoelectric legs connected

in series. Metal lines are designed to allow electrical access to structures. Moreover, a set of markers, a mix of crosses and lines, is required in order to align the different layers throughout the sequence of the fabrication processes. The metal contact layers corresponding to Ohmic contacts and bonding bumps are not included in the schematics for better clarity. However, every thermoelectric structure is designed to have metal contacts both on top of the dry-etched leg and on the isolation block.

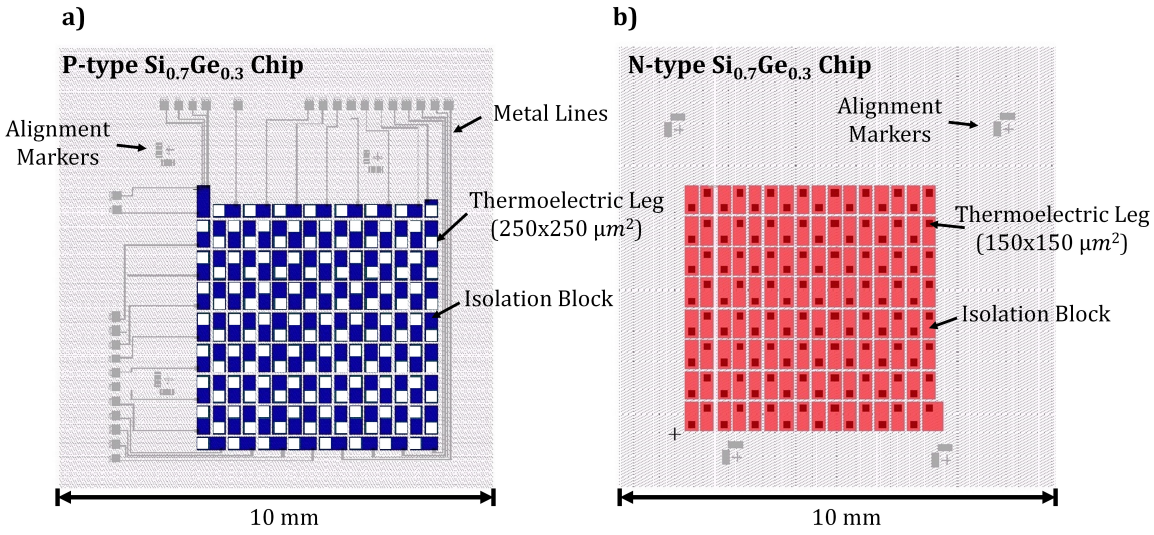



Figure 5.7: Top view of the (a) p- and (b) n-type layouts of the designed $\mu$TEG. Each chip is made of 64 thermoelectric legs sitting on 5 µm thick isolation blocks which guarantee the electrical continuity of the leg series. Aluminum metal lines are designed to allow electrical access to structures. Ohmic contacts are not presented in the above schematics for clarity and readability of the diagrams.

## 5.3 Chapter Conclusions

The chapter presented the modeling undertaken to define the legs number and geometry of the cross-plane heat flow $Si_{0.7}Ge_{0.3}$ $\mu$TEGs realized in this work. The case of a module connected in series with a 50 Ω electrical load and operating at around room temperature under constant temperature gradient, 30 K, has been studied. The $\mu$TEG design was consequently chosen and it is formed by 64 thermoelelctric leg pairs, with p- and n-type cross-sectional leg area of 250 ×250 µm$^2$ and 150 ×150 µm$^2$ respectively. According to modeling, the device is expected to have a room temperature internal resistance of 50 Ω and an effective thermal conductance of 1.61 W K$^{-1}$ at open-circuit. The device performance was investigated under the above specified operating conditions, leading to an expected output power of about 640 µW and voltage of 175 mV. The outlined design was then realized following the fabrication process presented in Chapter 6. Further design considerations will be finally presented in Chapter 7 and in the conclusion section dedicated to future work.

# Chapter 6

# Micro-Fabrication Process

The present chapter aims at describing the micro-fabrication tools and techniques employed to realize the thermoelectric devices under investigation. The first section of the chapter presents an overview of the fabrication process through a general explanation of the sequence of steps adopted. The following sections introduce the standard micro-electronic processes and present, in a detailed manner, the procedures developed and employed in this work. The description of the different fabrication steps is supported by optical and scanning electron microscope (SEM) images.

## 6.1 Process Steps

As illustrated in Chapter 2, a thermoelectric generator can be simply schematized as a series of p-n junctions electrically connected in series and thermally in parallel. In this work, p- and n-type materials were grown independently on separate SOI substrate wafers; thereby, they are also independently processed. Once the desired structures are patterned on both the p- and n-type samples, the two halves of the device are flip-chip bonded together. With reference to Figure 6.1, the fabrication of the $Si_{0.7}Ge_{0.3}$ µTEGs can be schematically summarized as follow:

- Definition of the Thermoelectric Structures: dry-etching of thermoelectric legs (2) and isolation blocks (3).
- Passivation of the Structures: plasma-enhanced CVD (PECVD) deposition of silicon nitride thin film (4) and dry-etching of openings for metal deposition (5).

– Metal Deposition: metal deposition for the realization of metal-semiconductor contacts (6) and solder layer (7).

– Flip-Chip Bonding: bonding of the p- and n-type halves of the sample (8).

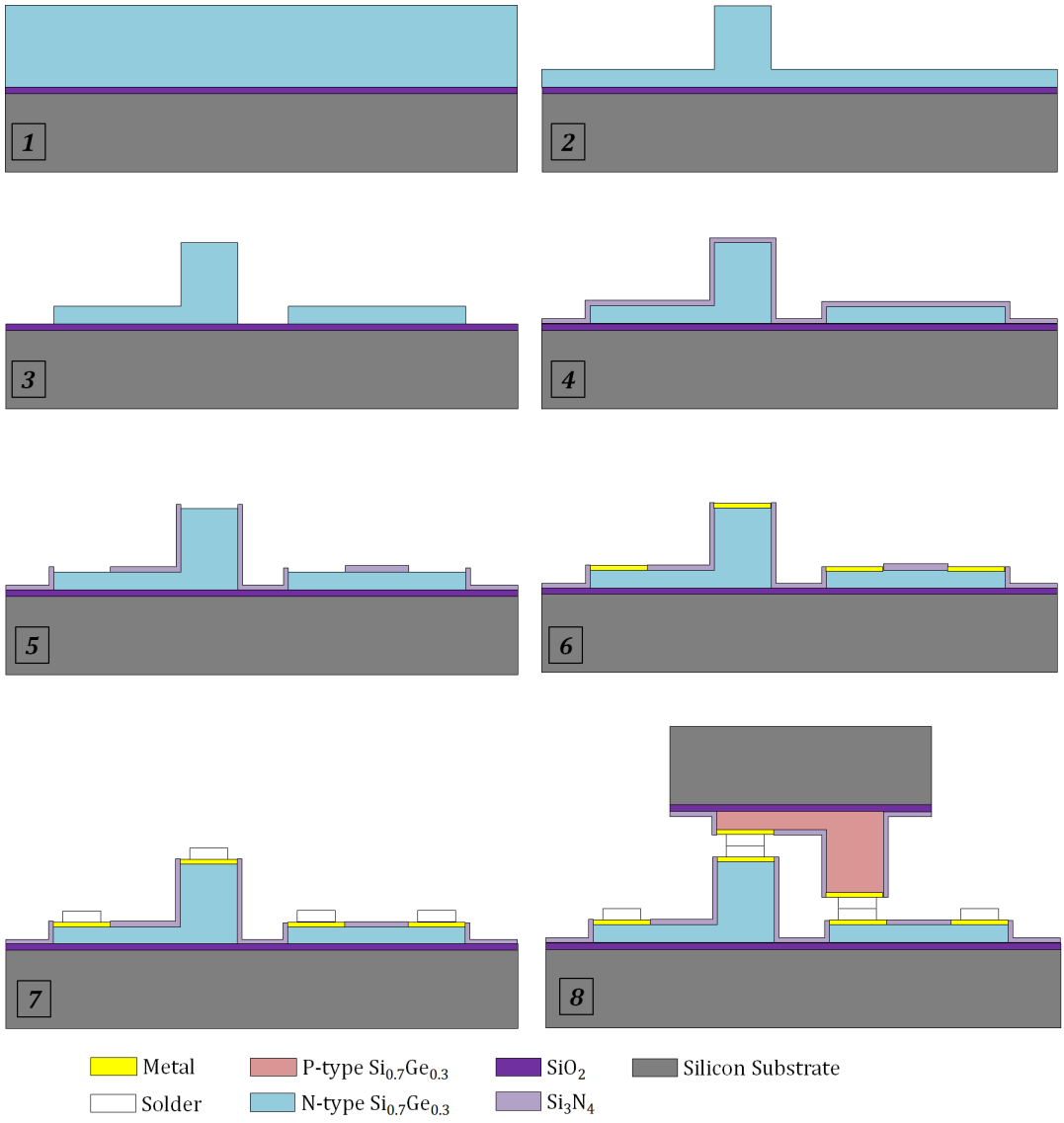



Figure 6.1: Sequential schematic illustrating the fabrication steps developed for the realization of the $Si_{0.7}Ge_{0.3}$ µTEG.

However, the block diagram in Figure 6.1 only provides a conceptual overview of the fabrication process. Each of the listed steps requires a number of subroutines to be undertaken, as presented in Figure 6.2 and Figure 6.3 in the cases of the dry-etch processes and metal depositions respectively. With reference to Figure 6.2 and Figure 6.3 every step of the overall process can be decomposed into the following subroutines:

– Resist Spinning (2).

– Resist Exposure and Patterning (3).

– Sample Processing (4).

– Removal of Resist Mask (5).

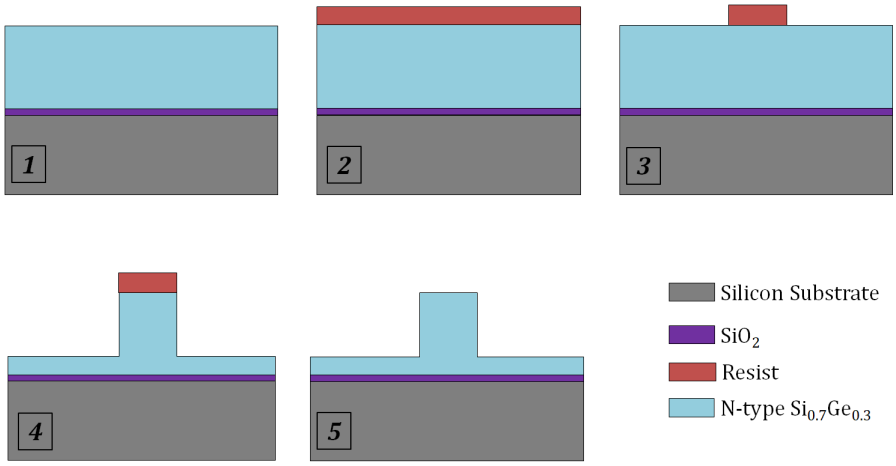



Figure 6.2: Sequential schematic illustrating the fabrication steps necessary to pattern and dry-etch a simple structure.

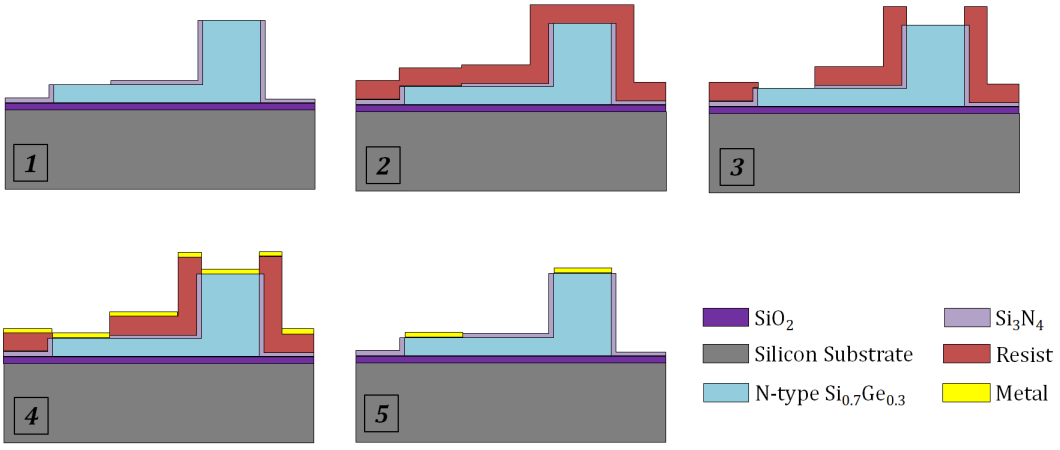



Figure 6.3: Sequential schematic illustrating the fabrication steps necessary to pattern metal contacts a through lift-off process.

## 6.2 Optical Lithography

The aim of a lithographic process is to transfer a specific pattern into a material. In micro and nanofabrication, such a pattern is outlined on the top surface of the sample by spinning a radiation sensitive polymer and exposing only specific parts of it. The patterned polymer layer is then used as a mask for the following fabrication step, generally an etching or a lift-off process. The minimum feature size achievable with a particular lithographic tool is defined by the wavelength used during exposure. Nowadays, optical lithography constitutes the fundamental lithography approach for the semiconductor manufacturing industry, especially in the fabrication of MEMS and CMOS. The technique allows simultaneous exposure, through a physical mask, of a large area of the wafer, resulting in a rapid and inexpensive process. Moreover, the CMOS industry has been pushing the resolution limits of optical lithography developing processes able to achieve transistors gate dimension below 30 nm [145].
The standard optical lithography process involves the following procedures:

- **Substrate cleaning:** Substrates can present particle contamination and/or organic impurities. General cleaning procedures suggest immersing samples in acetone inside an ultrasonic cleaner. The step is then repeated using isopropyl alcohol. Acetone is a better organic solvent, while isopropyl alcohol has lower volatility, which allows the samples to be blow-dried with dry nitrogen without leaving residual traces. Finally, the substrates undergo a dehydration bake, after which they are ready for resist processing.

- **Resist coating:** A small amount of resist in solvent is dropped onto the top surface of the sample, which is then spun at speed. The thickness of the spun resist mostly depends on the viscosity of the resist itself and on the spinning speed. During the spin, the solvent in the resist starts to evaporate until saturation is reached. The solvent concentration can be further reduced through the employment of a soft-bake step.

- **Soft-bake:** The thin layer of resist is generally cured for few minutes in order to reduce the residual solvent concentration. Such a bake also enhances the resist adhesion to the substrate and reduces stiction or contamination from the mask during the exposure phase.

- **Exposure:** Mask aligners running on a mercury lamp present a spectrum characterized by three lines (g-, h- and i-line) defined at different wavelengths

(436 nm, 405 nm and 365 nm). Photoresists are polymers designed to have a specific spectral sensitivity, which is however continuous over the entire spectrum. Thereby, the use of photoresists sensitive to specific wavelengths, together with the use of optical filters, is necessary to obtain the best lithographic resolution. Moreover, it is important to distinguish between positive and negative resists. The two types behave in opposite manners, with positive resists becoming soluble in developer after exposure.

- **Post-exposure bake:** The post exposure bake is generally an optional bake, which is more relevant when processing negative resists. It further stimulates the cross-linking mechanism started during exposure.

- **Development:** The resist is then selectively cleaned off the sample, according to the areas that have been exposed or not.

The optical lithography mask aligner used in this work is a Suss MA6 [146]. The tool runs on a 350 W mercury lamp, which provides an i-line exposure dose of 25 $mW/cm^2$. Such a mask aligner offers an alignment accuracy of around 1 µm. Given the size of the thermoelectric structures designed within this work (from tens to hundreds µm), neither the resolution achievable with optical lithography nor the alignment accuracy of the mask aligner constituted a limitation. Therefore, every resist patterning necessary for the fabrication of the thermoelectric devices has been performed by optical lithography.

### 6.2.1 Resists Processes

Being able to control the profile of thick resists is as important as it is challenging. Indeed, when the thickness of the resist is larger than the penetration depth of the exposure light, the illumination density is not homogeneous through the resist layer. Longer illumination times are then required, introducing the risk of overexposing the top of the photosensitive layer. The quality of the resist profile has substantial effects on both the side walls of dry-etched structures and the effectiveness of the lift-off process.
This work utilized the AZ4562 [147] positive photoresist for the dry-etch processes. The polymer has a 6 µm thickness and vertical profiles (Figure 6.4) if patterned with the following optimized process:

1. Spinning: 4000 rpm for 1 minute.

2. Baking: 100 °C for 6 minutes and 20 seconds.
3. Exposure: 25 seconds.
4. Development: 2 minutes in 4:1 $H_2O$: AZ400K developer with a subsequent 1 minute rinse in deionized water.
5. Oxygen Ashing: 100 W for 2 minutes.

The negative photoresist AZ2070 [148] was used for any lift-off process performed in this work. Negative resists indeed simplify the lift-off process due to their negative sloped profile, which breaks the continuity of the deposited film. 7 µm thick layers, characterized by a light undercut, were obtained (Figure 6.5) by patterning the AZ2070 photoresist as follows:

1. Spinning: 4000 rpm for 1 minute.
2. Baking: 110 °C for 1 minute and 30 seconds.
3. Exposure: 20 seconds.
4. Post-Exposure Baking: 100 °C for 1 minute.
5. Development: 1 minute and 15 seconds in MF-319 developer with subsequent 1 minute rinse in deionized water.
6. Oxigen Ashing: 100 W for 2 minutes.

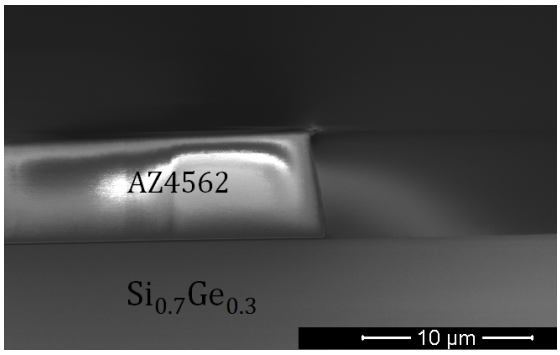



Figure 6.4: SEM image showing the slightly positive sloped profile of the AZ4562 layer. Image deformations are due to charging of the resist.

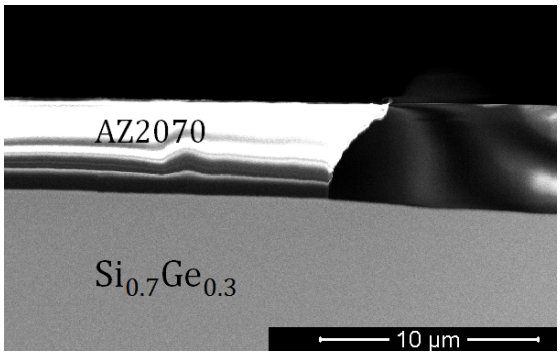



Figure 6.5: SEM image showing the characteristic undercut in the profile of the AZ2070 positive photoresist layer. Image deformations are due to charging of the resist.

However, the above process is not suitable to pattern metal layers onto 20 µm tall structures. The resist layer obtained from a single AZ2070 spin does not coat the mesas top surface sufficiently. To solve the issue, two consecutive spins of AZ2070 resist, Figure 6.6, were adopted, repeating the resist spinning and baking steps and also doubling the resist exposure and developing times.
After both dry-etch and lift-off processes, the photoresist mask needs to be cleaned off the sample. To do so, the samples are immersed in a 50 °C acetone bath and the resist dissolves.

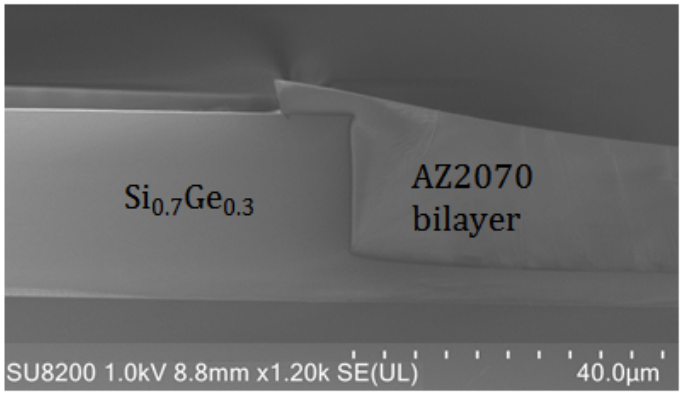



Figure 6.6: SEM cross sectional view of the AZ2070 double layer. The photoresist is able to coat the 20 µm silicon-germanium structure and pattern features on top of the latter, still revealing the negative sloped profile that characterizes positive resists.

## 6.3 Dry Etching Techniques

Plasma-based etching technology is nowadays widely used in the semiconductor industry due to its ability to control isotropy and uniformity of the etching process accurately. Moreover, dry-etching tools offer precise monitoring of processing time and compatibility with vacuum technologies. The following step sequence summarizes the general dry-etching process, Figure 6.7:

1. The sample to be etched is loaded on a capacitively coupled electrode.
2. The active species are generated from the reactive gases pumped into the chamber by radio-frequency (RF) glow discharge. The process is based on two phenomena: ionization and collision-induced electron dissociation.
3. The active species move by diffusion from the plasma to the surface of the sample.

4. Reaction phase:
   - The radicals are adsorbed onto the sample surface by ion bombardment.
   - The adsorbed radicals chemically react with the material to be etched releasing volatile species.
5. The volatile species desorb from the sample surface back into the chamber.
6. The volatile chemical byproduct is pumped out the chamber.

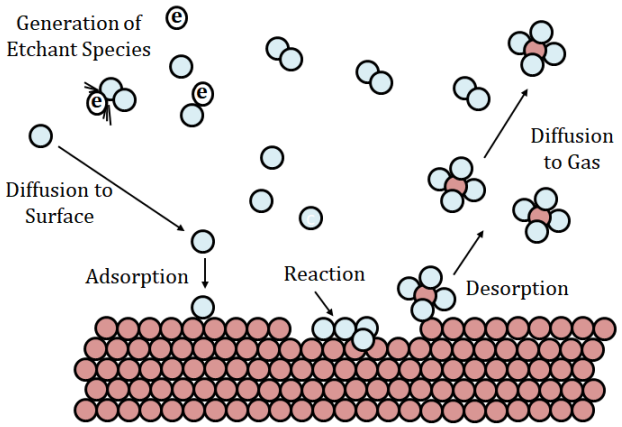



Figure 6.7: Schematic of a dry-etching process.

In the JWNC facilities, two main dry-etching technologies are available: reactive ion etching (RIE) and inductively coupled plasma (ICP).
Reactive ion etching is a plasma-based technique characterized by a combination of physical and chemical etching effects. RIE enables good control over both anisotropy of the etched profiles and selectivity between the mask layer and the actual material to be etched. However, the RF power is responsible for both plasma generation, thereby plasma density, and ion acceleration. An increase in the RF power would determine an increase in the biasing voltage of the electrode accommodating the sample. Consequently, the ion speed would increase and with it the bombardment energy. The overall effect is to intensify the physical nature of the etching process.
On the contrary, in ICP tools, plasma generation and ion acceleration are controlled independentely by two distinct RF generators and take place in two separate chambers. An inductively coupled RF generator determines the plasma density, while a capacitively coupled RF supply is responsible for the ion bombardment energy. Thereby, ICP tools enable broad process tunability to achieve the required etching

properties.
All the dry-etching processes discussed in the following paragraphs were performed on either the BP80-RIE tool from Oxford Plasma Instruments [149] or the STS-ICP machine from Surface Technology Systems [150].

### 6.3.1 RIE Etching

In this work, the BP80-RIE tool was used to perform anisotropic dry-etching of $Si_3N_4$ thin layers. Table 6.1 summarizes the parameters of the etching recipe utilized. The $CHF_3$ chemistry is directly responsible for the generation of the reactive agents, while the addition of $O_2$ has the effect of reducing the plasma density and passivating the surface to be etched.

| **Parameter** | **Value** |
|---|---|
| *Gas* | $CHF_3/O_2$ |
| *Flow (sccm)* | 50/5 |
| *Platen Power (W)* | 150 |
| *Pressure (mT)* | 55 |
| *Etch Rate (nm/min)* | 50 |

Table 6.1: BP80-RIE process parameters for anisotropic $Si_3Ni_4$ dry-etching.

### 6.3.2 ICP Etching

STS-ICP was used to dry-etch the $Si_{0.7}Ge_{0.3}$ alloys. Two separate dry-etching processes are necessary to realize the designed thermoelectric structures. A first anisotropic dry-etch is required to define the 20 µm tall thermoelectric legs, Figure 6.8. The subsequent dry-etch recipe realizes the bottom of the mesa structure determining a positive sloped side wall, Figure 6.9, which is necessary for the electrical continuity of metal lines running across such mesa step. Both the etching recipes are based on $C_4F_8 - SF_6$ chemistry, as listed in Table 6.2 and 6.3. $SF_6$ is entirely responsible for the formation of reactive species, since the chemical reaction only depends on the interaction between the fluorine radicals and the exposed silicon. On the other hand, the $C_4F_8$ dilutes the plasma density and promotes the passivation of the exposed material by depositing a thin polymeric layer that masks the surface from $SF_6$, enabling to selectively control the directionality of the etch. The obtained positive slope of about 100° is enough to guarantee the electrical continuity of the metal lines running along the side walls.

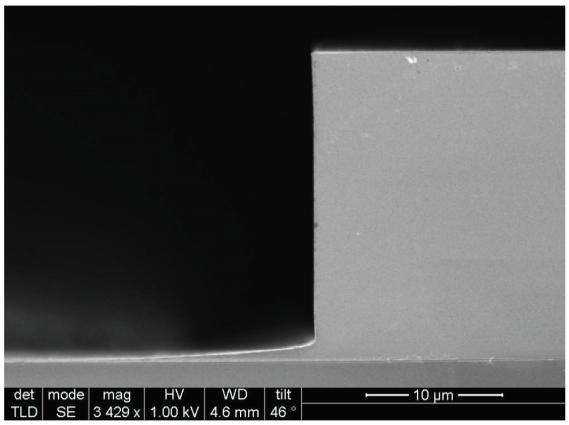



Figure 6.8: SEM image of the optimized vertical dry-etch profile.

| Parameter | Value |
|---|---|
| *Gas* | $C_4F_8/SF_6$ |
| *Flow (sccm)* | 90/130 |
| *Platen Power (W)* | 12 |
| *ICP Power (W)* | 600 |
| *Pressure (mT)* | 15 |
| *Etch Rate (nm/min)* | 1030 |

Table 6.2: ICP-STS process parameters for anisotropic SiGe dry-etching.

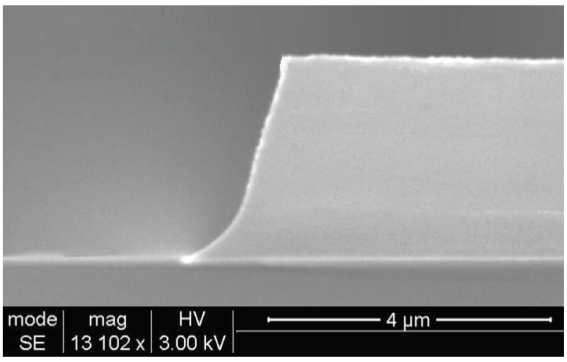



Figure 6.9: SEM image of the optimized positive sloped dry-etch profile.

| Parameter | Value |
|---|---|
| *Gas* | $C_4F_8/SF_6$ |
| *Flow (sccm)* | 90/40 |
| *Platen Power (W)* | 10 |
| *ICP Power (W)* | 700 |
| *Pressure (mT)* | 10 |
| *Etch Rate (nm/min)* | 390 |

Table 6.3: ICP-STS process parameters for the positive sloped profile dry-etching on SiGe.

Figure 6.10 and Figure 6.12 respectively show the etched thermoelectric legs and the full leg blocks. While the first etch was controlled in time, by knowing the etch rate of the material, the second etch was continued until the $SiO_2$ stop layer was reached. Optical profilometry was used to inspect the uniformity of the etch depth of the structures across the sample, Figure 6.11 and Figure 6.13.

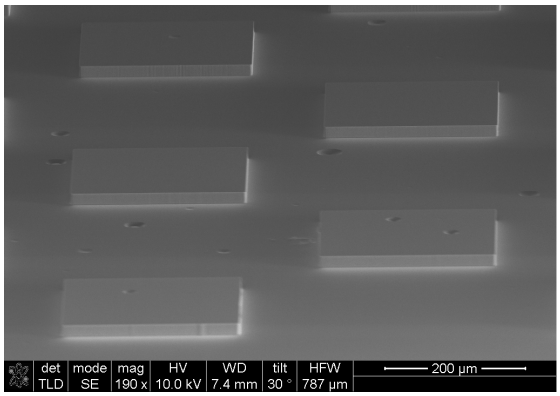



Figure 6.10: SEM image showing the etched thermoelectric legs.

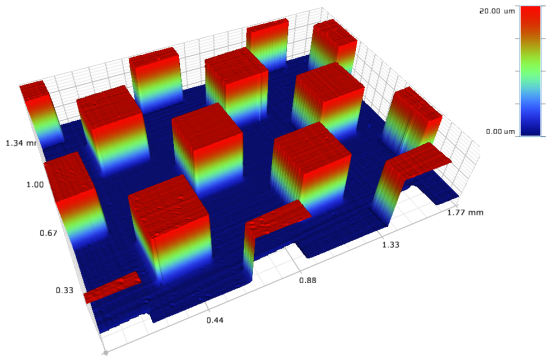



Figure 6.11: Optical profilometer image of the etched thermoelectric legs.

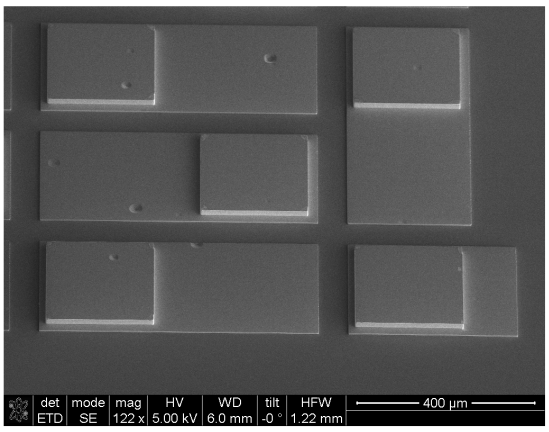



Figure 6.12: SEM image showing the full thermoelectric structures.

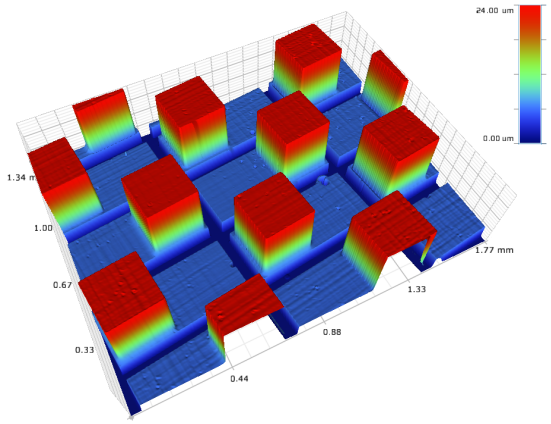



Figure 6.13: Optical profilometer image of the etched thermoelectric structures.

## 6.4 Passivation: Silicon Nitride Deposition

The developed fabrication process also includes the deposition of a thin layer of silicon nitride, $Si_3N_4$, which is necessary to passivate the thermoelectric structures and provide electrical insulation to metal lines running on top of the semiconductor. The tool used for the $Si_3N_4$ depositions was an Oxford Instruments PECVD 80+ [151]. PECVD (Plasma-enhanced Chemical Vapour Deposition) is a low temperature (around 300 °C) deposition technique in which an RF generator drives the reactants' dissociation and accelerates the radicals towards the substrate. The whole process takes place in the same chamber. The nature of the deposition depends on two main

factors: the plasma generation and the acceleration energy of the reactive species landing on the substrate. Different variables play a role in the PECVD deposition: RF power, temperature and precursor gas flow. In this work, 150 nm thick films of PECVD silicon nitride were deposited under the conditions listed in Table 6.4.

| **Parameter** | **Value** |
|---|---|
| *Gas* | $SiH_4/NH_3/N_2 : He$ (85%$He$) |
| *Flow (sccm)* | 10/16/200 |
| *Platen Power (W)* | 21 |
| *Pressure (mT)* | 1000 |

Table 6.4: PECVD 80+ process parameters for low stress $Si_3Ni_4$ deposition.

## 6.5 Metal Deposition and Lift-off Techniques

Different metal evaporation techniques, in combination with the lift-off process, were used to pattern integrated thermometers, Ohmic contacts, connection lines, bond pads and solder bumps.

At the JWNC facilities, three main categories of metal evaporation tools are available: electron-beam (Plassys MEB400S [152]), sputtering (Plassys MP900S [152]) and thermal [153] evaporators. All of these have been used throughout this work.

In electron-beam evaporators, an electron beam, generated from a charged tungsten filament under high vacuum, is directed towards a metal target anode. The bombardment causes atoms of the metal target to evaporate and move without scattering in the vacuum chamber until they precipitate into solid form by reaching the substrate. Electron-beam evaporation allows strongly anistropic metal deposition; moreover, the technique provides high control over evaporation rate, which relates to the grain size of the evaporated metals.

On the other hand, a sputter coater system induces the evaporation of metal atoms through the plasma generated by an electric field from the injected gas. The charged ions, which are generally $Ar^+$, are driven towards the metal target cathode scattering metal atoms towards the substrate loaded on the anode of the chamber. During such a process, random scattering of the evaporated particles takes place in the chamber. The chamber pressure is generally of the order of $10^{-2}$ mbar; higher than in electron-beam evaporators (generally around $10^{-7}$ mbar). This result in an isotropic metal deposition.

Finally, thermal evaporators operate by driving a current through the desired metal

target. Such metal heats up, by the Joule effect, and starts to evaporate. The evaporated material transverses the vacuum chamber reaching the surface of the substrate. Two main processes can be used to pattern metals: lift-off and metal etching. The lift-off process requires a resist to be spun and patterned, with negative sloped sidewalls, before the actual metal deposition. After the metal is evaporated on the sample, the latter is immersed in a resist solvent bath, generally acetone based. The solution dissolves the resist, lifting-off the metal laying on top of masked areas. The resist undercut is necessary to break the continuity of the metal thin film, thereby facilitating the stripping process.

Metal etching could also be used to pattern metal layers. Such a process involves an initial metal deposition followed by resist spin and patterning. The patterned polymer acts as a mask for the selective removal of the metal. However, wet-etching of metals would require the use of strong acids, which could also attack underlying layers and would isotropically attack the metal. Metal dry-etching is also possible; however, the lift-off technique is generally preferred due to reduced risk of attacking, either physically or chemically, the surfaces underneath the metal layer. In this work, lift-off has been adopted for every metallization step processed.

The fabrication process requires the deposition, by electron-beam evaporation, of a 100 nm thick platinum layer. As introduced in Chapter 2, the platinum layer is thermally annealed with the aim of creating the low resistivity platinum-germanosilicide Ohmic contacts. SEM images illustrating the platinum contacts at top and bottom of the thermoelectric structures are presented in Figure 6.14 and Figure 6.15.

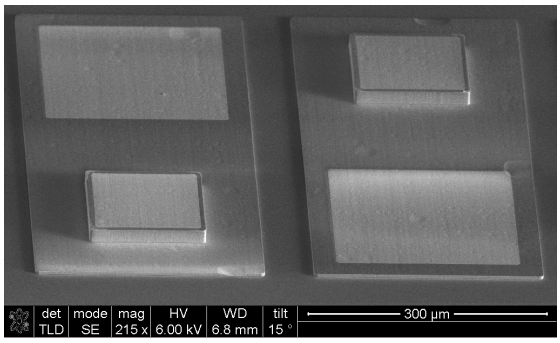



Figure 6.14: SEM image of two thermoelectric structures, composed of legs and base block. The platinum contacts are well distinguishable on both top and bottom of the structures.

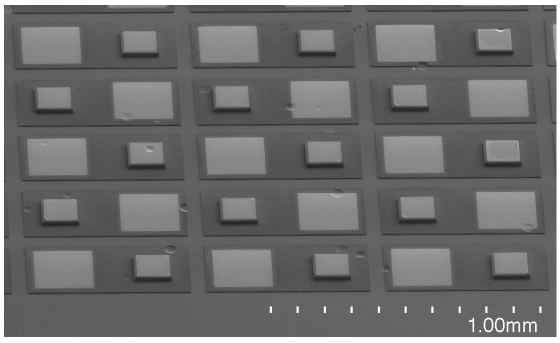



Figure 6.15: SEM image of a matrix of thermoelectric structures. The platinum contact pads are well distinguishable on both top and bottom of each structure.

A 500 nm thick aluminum layer was sputtered to realize metal lines and bond pads. The isotropic deposition that characterizes sputtering systems is necessary to guarantee the electrical continuity of the metal lines running across mesa steps, see Figure 6.16 and Figure 6.17.

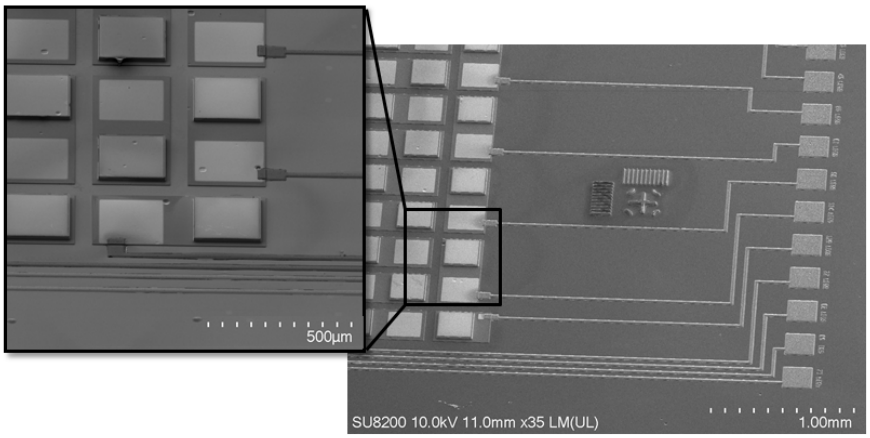



Figure 6.16: SEM image of the aluminum probing pads and connection lines. As mentioned, the metal lines run across the sloped profile of the thermoelectric structures to contact the Ohmic pads at the bottom of the thermoelectric units.

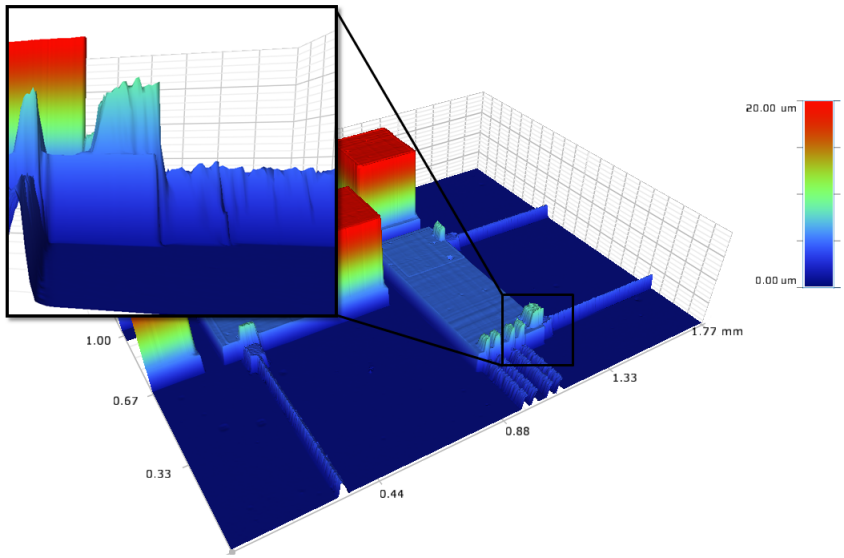



Figure 6.17: Optical profiler image of thermoelectric structures and aluminum connection lines. The inset of the image clearly shows such lines running continuously across the step of the thermoelectric blocks.

Finally, a few µm thick layer of indium based alloys was thermally evaporated to realize the solder pads, later utilized for flip-chip bonding, Figure 6.18 and 6.19. Such a process, together with the solder choice, is discussed in detail in the following paragraph.

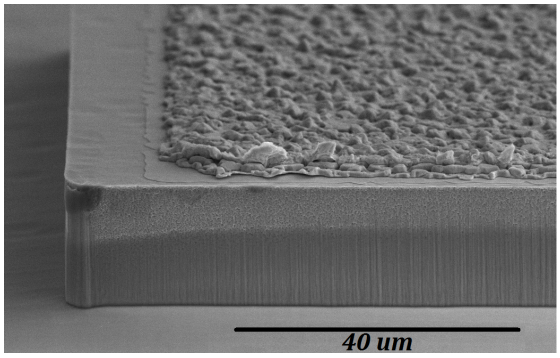



Figure 6.18: Top view SEM image of the indium layer thermally evaporated on the top a thermoelectric leg.

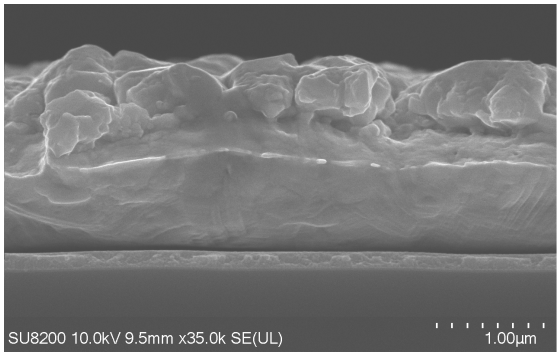



Figure 6.19: SEM cross sectional view of a 1 µm thick indium layer. The surface roughness of the layer, mostly due to the grain size of the evaporated metal, appears clear.

## 6.6 Flip-Chip Bonding

Flip-chip assembly is a technique developed to interconnect semiconductor devices to external circuitry by means of conductive solder bumps. The method started to gain popularity over traditional wire bonding as a highly performing, reliable and low-cost solution for systems-in-package. Moreover, the face-down assembly technology has the real merit of leading the way to three-dimensional integration. The idea of enhancement for micro-system architectures is historically related to lithography scaling and two-dimensional integration as described by Moore's law [154]. However, improvements of chip performance, functionality and packing density can be also achieved through multiple layers of active devices and integration of heterogeneous materials or devices.

The state of the art electronics packaging already addressed most of the fundamental technical issues, with the result of advanced solutions being available for chip-to-chip and chip-to-substrate bonding, also in the case of ultra-fine pitch systems. However, the costs of the high-end flip-chip bonding technology still cannot compete with the those of traditional face-up wire bonding. Yield improvements are also required to

approach large-scale manufacturing.

In traditional flip-chip assembly, the chips are flipped over and their contact pads are aligned to the matching ones of the substrate chip or wafer. The solder is then re-flowed in order to complete the interconnects. Such process results extremely critical for solder bumps sequences having small spacing as adiacent bumps could short-circuit during the reflow process. To overcome the issue, thermo-compression bonders, which allow local solder reflow without the exposure of the entire substrate to heat treatment, have been developed. Finally, the two halves to be bonded are brought in contact and heated under pressure.

The flip-chip bonder available at the JWNC facilities and adopted for this work is a Semiconductor Equipment Corporation Model 855 [155], schematically presented in Figure 6.20. Such semi-automatic placement systems for flip-chips are equipped with vacuum stage and pick and place tip, both of which can be heated up to 225 °C. The optics of the motorized viewer system allow the achievement of an alignment accuracy of ± 10 µm. Moreover, a bond load, adjustable in the range of 30 g to 2 kg, is also applicable during the process.

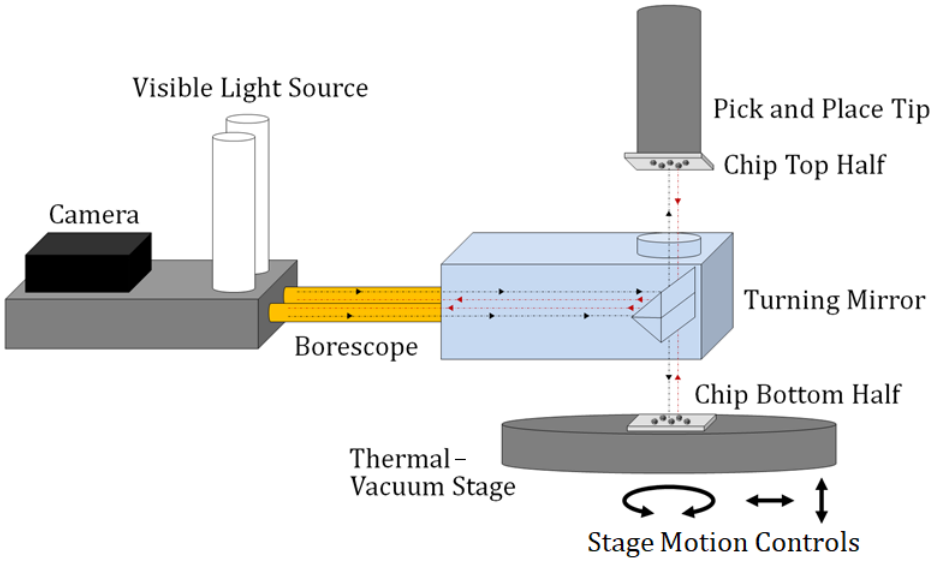



Figure 6.20: Illustrative schematic of the thermo-compression flip-chip bonder used in this work.

The choice of the solder layer is generally dictated by the application itself: substrates to be bonded, thermal budget of the bonding process, operating conditions of the device and need of an external hermetic sealing. In this work, the $Si_{0.7}Ge_{0.3}$ thermoelectric devices are expected to operate between 300 °C and 500 °C without

any hermetic sealing. In this case, operating temperature and compatibility with substrate are thereby the main drivers for selecting the solder metal. Two different materials and approaches have thereby been investigated: gold bumps and indium based layers.

### 6.6.1 Gold Micro-Bumps

Micro-bumps of high-cost (i.e. gold and copper) or low-cost (i.e. tin) metals can be used to interconnect high pin count chips. In this work, an Inseto iBond5000 ball bonder [156] was utilized to deposit the gold micro-bumps used as the solder layer for flip-chip bonding. The gold micro-bumps are placed directly onto 100 nm thick aluminium pads patterned corresponding to the structures to interconnect. Gold micro-bumps, having around 50 µm diameter and 40 µm tail, were obtained, Figure 6.21.

P- and n-type $Si_{0.7}Ge_{0.3}$ chips were then mounted on the flip-chip bonder, top and bottom structures were aligned and brought in contact. To perform the thermo-compression bonding, a 2 kg static down load was applied and the temperature was set to 200 °C for 20 minutes. Finally, the bonded sample was left to cool under natural convection, the down load was disengaged and the sample examined, Figure 6.22.

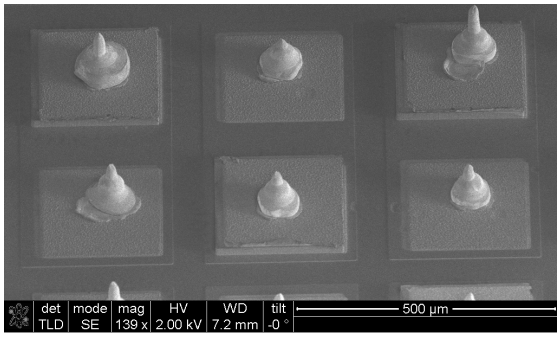



Figure 6.21: SEM image of an array of gold micro-bumps deposited on the contact pads of the patterned thermoelectric structures.

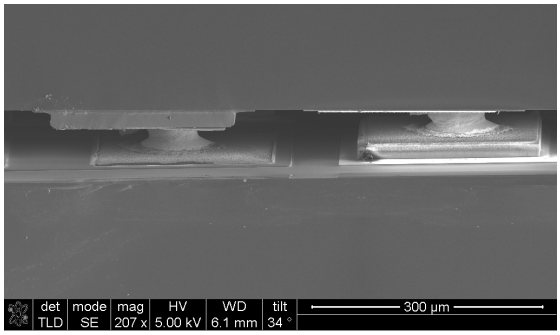



Figure 6.22: SEM cross sectional view of a flip-chip bonded sample. The thermoelectric structures on p- and n-type chips are connected through the gold micro-bumps.

Despite the fabrication advantages related to the simplicity of a process which avoids flux application and solder reflow, the described approach is not able to deliver high quality bondings. Mechanical failings of the bonded joints affected the majority of the processed samples. It is likely that heavier down loads and higher temperatures during the thermo-compression process would improve the quality and yield of the

bonded junctions. However, such input levels are out of the reach of the flip-chip bonding technology available.

### 6.6.2 Indium-Silver Intermetallic

A different bonding approach, specifically designed for high post-bonding operating temperatures, relies on the formation of intermetallic compounds. Indeed, the use of low-temperature solder (i.e indium) is generally preferred for bonding applications and it has already been largely investigated for the realization of hermetically sealed packaging. After low-temperature bonding, stable high-temperature intermetallic compounds are formed from a low-melting point component and a high melting point one.

In this work, indium and silver have been adopted to realize the bonding and form the intermetallic compound. From the phase diagram in Figure 6.23, the melting temperatures of indium and silver are 156 °C and 961 °C respectively, while the eutectic temperature of the alloy is 144 °C.

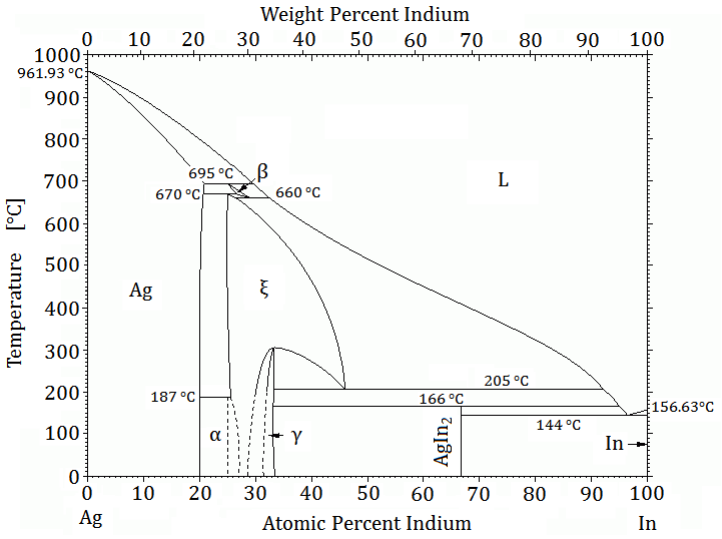



Figure 6.23: The indium-silver phase diagram [157].

By tuning the ratio between the high and the low melting point components, the intermetallic bonding layer can be designed in order to have a high melting point. In this work, the intermediate bonding layer is deposited by thermal evaporation onto 100 nm of platinum and it consists of 2 µm of silver and 1 µm of indium. Such thicknesses correspond to an indium to silver weight ratio of 25 4% implying the intermetallic to match the homogeneous phase $\alpha$. However, the actual intermetallic compound phase could also be a stable $\beta$, $\gamma$ or $\xi$ composition, each of which is seen

to be stable in specific temperature ranges up to 695 °C.
During the bonding process, the p- and n-type samples, Figure 6.25 and Figure 6.24 are aligned and brought into contact under 2 kg of down load and at 180 °C for about 1 hour. Both the bonding of the thermoelectric structures and the formation of the intermetallic compound happens at this stage.

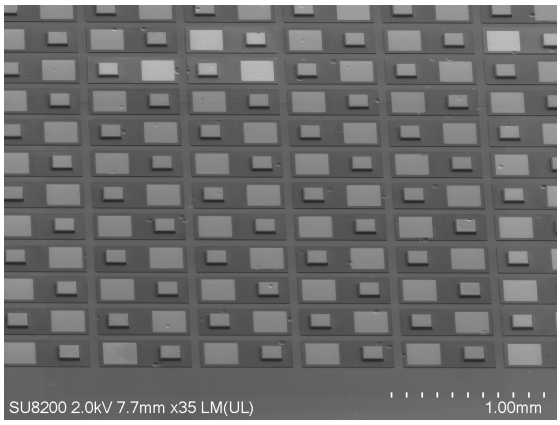



Figure 6.24: SEM top view image of a n-type sample ready for flip-chip bonding.

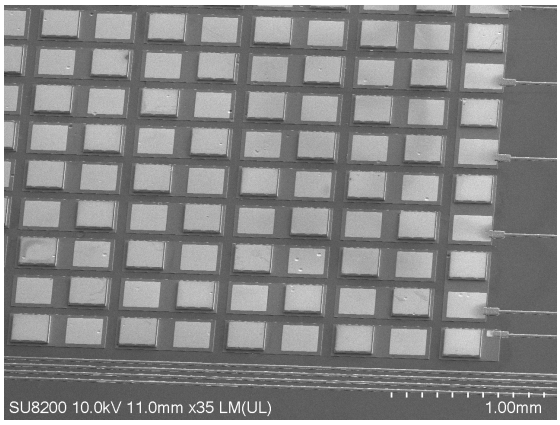



Figure 6.25: SEM top view image of a p-type sample ready for flip-chip bonding.

The cross-sectional elemental composition of the intermediate bonding layer has been characterized by energy dispersive x-ray spectroscopy (EDX) before, Figure 6.26, and after, Figure 6.27, undergoing a thermal process equivalent to the one characterizing the bonding. The results clearly show the diffusion of indium in the silver layer with the formation of the intermetallic.

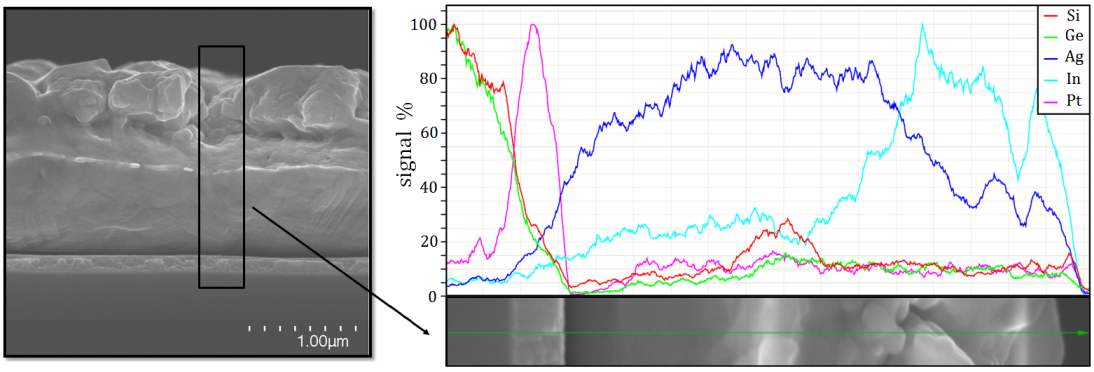



Figure 6.26: SEM cross sectional image of the silver and indium solder layer coupled with an EDX analysis of the normalized detector signal intensity revealing the elemental composition of the layer prior to heat treatments.

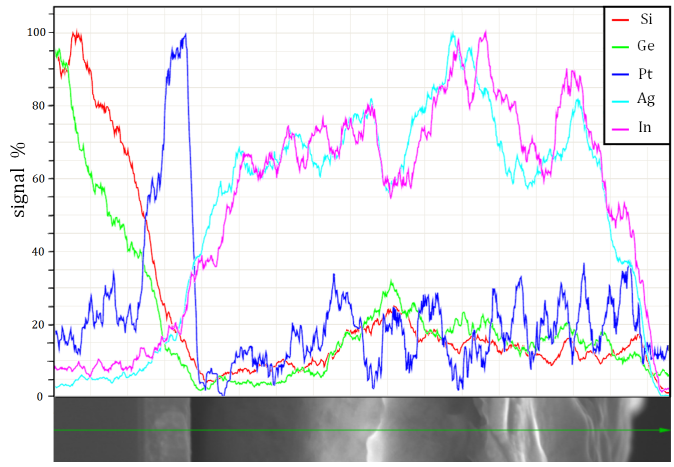



Figure 6.27: EDX analysis of the normalized detector signal intensity revealing the elemental composition of the solder layer after 1 hour temperature treatment at 180 °C.

Despite the simplicity and cleanliness of a fluxless process, a drop of Warton Metals Future HF SMT Rework Jelly [158] was applied on one half of the chip prior to bonding. The flux etches the native oxide from the surface of the indium layer, thereby promoting quality and reliability of the bonding. An SEM image of p- and n- type bonded thermoelectric legs is presented in Figure 6.28. The flux coating the interconnected structure is evident.

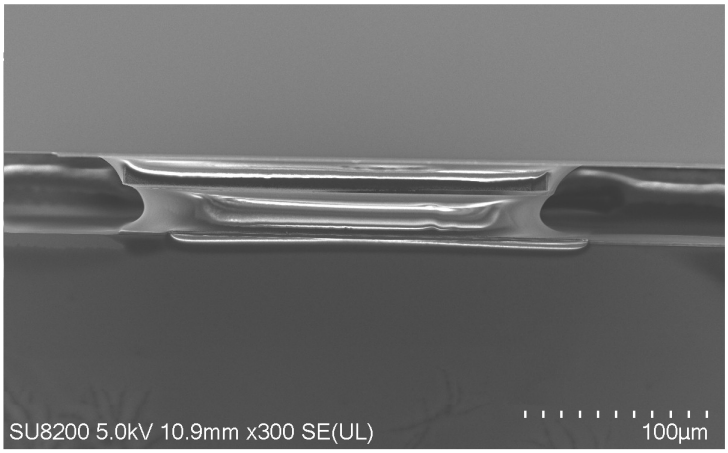



Figure 6.28: SEM cross-sectional view of p- and n-type thermoelectric legs bonded together in presence of flux coating the surfaces.

The developed process is able to guarantee repeatable and mechanically solid metal bonding, allowing the fabrication of the $\mu$TEGs, Figure 6.29 and Figure 6.30. The bonded samples were tested up to 250 °C on a hotplate without the occurrence of

any signs of debonding or melting of the metal junctions. This confirms the formation of an alloy phase between the silver and indium layers.
The fabricated $\mu$TEGs have then been tested and characterized. The electrical testing of the device also reveals qualitative information on the quality of the bonded junctions. Such considerations will be presented in the Chapter 7.
After being characterized, device SiGeTEG 17 and device SiGeTEG 21 were thermally treated at 450 °C in atmospheric environment for 48 h. No signs of debonding occurred and the internal resistance of both the devices remained unchanged, therefore proving the thermal stability of the studied electrical junctions over the temperature range of interest.

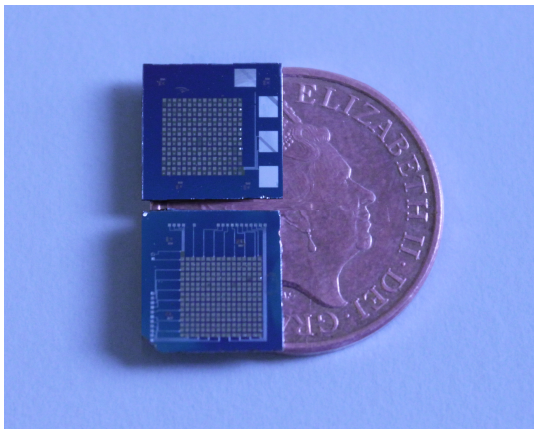


Figure 6.29: Optical image of the microfabricated p- and n-type samples compared to the size of a penny.

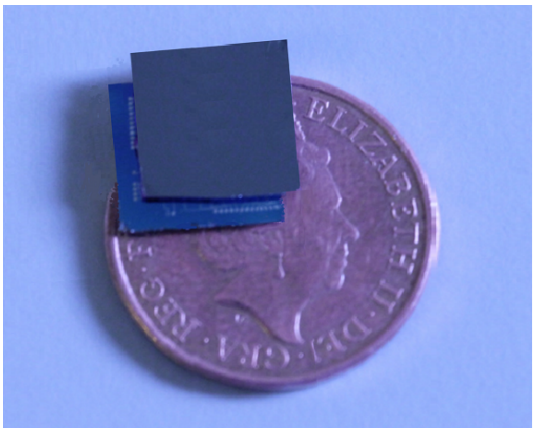
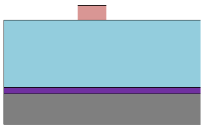
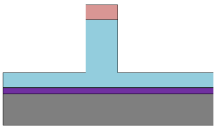
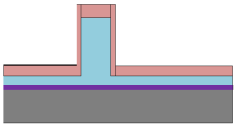
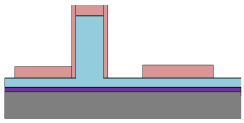
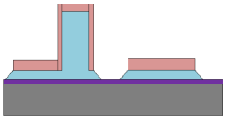
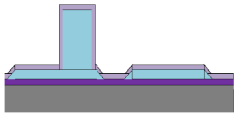
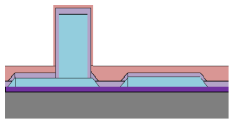
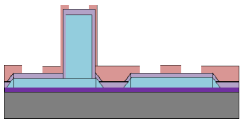
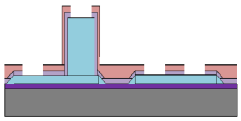
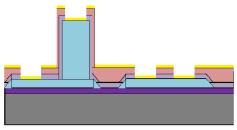
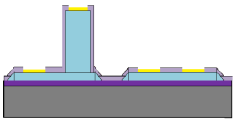
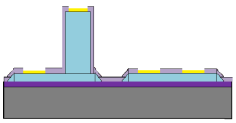
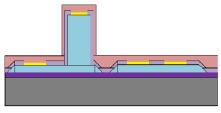


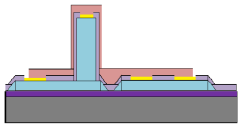
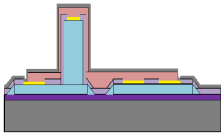
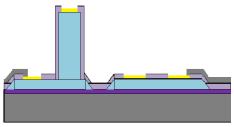
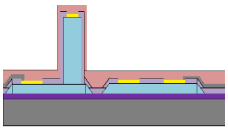
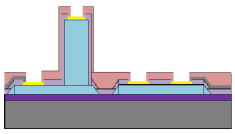
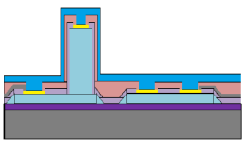
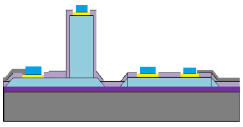
Figure 6.30: Optical image of the realized $Si_{0.7}Ge_{0.3}$ $\mu$TEG in comparison to a penny.

## 6.7 Micro-Fabrication Summary

The present section provides a detailed illustrative summary of the micro-fabrication processes employed to realize the thermoelectric devices developed in this work.

| Step | Schematic | Description |
|---|---|---|
| 1 |  | **Substrate Solvent cleaning:**<br>5 min acetone, 5 min IPA cleaning in ultrasonic bath. |
| 2a |  | **Photolithography: AZ4262 Spinning**<br>Spinning: 4000rpm, 60 s;<br>Baking: 100 °C, 6 min 20 s. |
| 2b |  | **Photolithography: Exposure and Development**<br>Exposure: contact alignment, 25 s, 25 mW/cm$^2$dose;<br>Development: 120 s in 4:1 $H_2O$:AZ400K;<br>60 s RO water rinse;<br>Oxygen Ashing: 100 W, 120 s. |
| 3 |  | **Anisotropic SiGe Dry-Etching:**<br>Etch Parameters: listed in Table 6.2;<br>Etch Time: 20 min. |
| 4 |  | **Resist Removal:**<br>1 hour acetone in 50 °C water bath;<br>5 min IPA cleaning in ultrasonic bath. |
| 5a |  | **Photolithography: AZ4262 Bilayer Spinning**<br>Layer 1 - Spinning: 4000rpm, 60 s;<br>Baking: 100 °C, 6 min 20 s.<br>Layer 2 - Spinning: 4000rpm, 60 s;<br>Baking: 100 °C, 6 min 20 s. |
| 5b |  | **Photolithography: Exposure and Development**<br>Exposure: contact alignment, 50 s, 25 mW/cm$^2$dose;<br>Development: 240 s in 4:1 $H_2O$:AZ400K;<br>60 s RO water rinse;<br>Oxygen Ashing: 100 W, 120 s. |
| 6 |  | **Sloped SiGe Dry-Etching:**<br>Etch Parameters: listed in Table 6.3;<br>Etch Time: 6 min. |

| | | |
|---|---|---|
| 7 |  | **Resist Removal:**<br>1 hour acetone in 50 °C water bath;<br>5 min IPA cleaning in ultrasonic bath. |
| 8 |  | **PECVD $Si_3N_4$ Deposition**<br>Deposition Parameters: listed in Table 6.4;<br>Deposition Thickness: 150 nm. |
| 9a |  | **Photolithography: AZ2070 Bilayer Spinning**<br>Layer 1 - Spinning: 4000rpm, 60 s;<br>Baking: 110 °C, 90 s.<br>Layer 2 - Spinning: 4000rpm, 60 s;<br>Baking: 110 °C, 90 s. |
| 9b |  | **Photolithography: Exposure and Development**<br>Exposure: contact alignment, 40 s, 25 mW/cm$^2$dose;<br>Baking: 100 °C, 60 s;<br>Development: 150 s in MF-319;<br>60 s RO water rinse;<br>Oxygen Ashing: 100 W, 120 s. |
| 10 |  | **RIE $Si_3N_4$ Etching:**<br>Etch Parameters: listed in Table 6.1. |
| 11 |  | **E-beam evaporation:**<br>100 nm Platinum. |
| 12 |  | **Metal Lift-off:**<br>1 hour acetone in 50 °C water bath;<br>5 min IPA cleaning in ultrasonic bath. |
| 13 |  | **Rapid Thermal Annealing:**<br>600 °C, 30 s in $N_2$ environment |
| 14a |  | **Photolithography: AZ2070 Bilayer Spinning**<br>Layer 1 - Spinning: 4000rpm, 60 s;<br>Baking: 110 °C, 90 s.<br>Layer 2 - Spinning: 4000rpm, 60 s;<br>Baking: 110 °C, 90 s. |

| | | |
|---|---|---|
| 14b |  | **Photolithography: Exposure and Development**<br>Exposure: contact alignment, 40 s, 25 mW/cm$^2$dose;<br>Baking: 100 °C, 60 s;<br>Development: 150 s in MF-319;<br>60 s RO water rinse;<br>Oxygen Ashing: 100 W, 120 s. |
| 15 |  | **Sputtering:**<br>300 nm Aluminum. |
| 16 |  | **Metal Lift-off:**<br>1 hour acetone in 50 °C water bath;<br>5 min IPA cleaning in ultrasonic bath. |
| 17a |  | **Photolithography: AZ2070 Bilayer Spinning**<br>Layer 1 - Spinning: 4000rpm, 60 s;<br>Baking: 110 °C, 90 s.<br>Layer 2 - Spinning: 4000rpm, 60 s;<br>Baking: 110 °C, 90 s. |
| 17b |  | **Photolithography: Exposure and Development**<br>Exposure: contact alignment, 40 s, 25 mW/cm$^2$dose;<br>Baking: 100 °C, 60 s;<br>Development: 150 s in MF-319;<br>60 s RO water rinse;<br>Oxygen Ashing: 100 W, 120 s. |
| 18 |  | **Thermal Evaporation:**<br>2 µm Silver;<br>1 µm Indium. |
| 19 |  | **Metal Lift-off:**<br>1 hour acetone in 50 °C water bath;<br>5 min IPA cleaning in ultrasonic bath. |

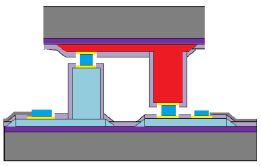
| | | |
|---|---|---|
| 20 |  | **Flip-Chip Assembly:**<br>1 h, 180 °C, 2 kg down load. |
| | $SiO_2$ <br> Silicon Substrate <br> N-type $Si_{0.7}Ge_{0.3}$ <br> P-type $Si_{0.7}Ge_{0.3}$ <br> Silver-Indium alloy <br> $Si_3N_4$ <br> Resist <br> Platinum <br> Aluminium | **Color Legend** |

Table 6.5: Detailed schematic of the micro-fabrication process developed for the realization of the silicon-germanium $\mu$TEGs.

## 6.8 Chapter Conclusions

This chapter presented all the fabrication technologies and techniques adopted in this work for the realization of thermoelectric micro-devices, which are able to reliably address specific operation requirements. Considerable time and effort were dedicated to develop every process step so to achieve a repeatable procedure. The standards of fabrication achieved are witnessed by the several building blocks being novel or, if already present in literature, representing the state-of-the-art in the field of $\mu$TEG. With the developed process structure and reproducibility, the fabrication of more complex devices could be undertaken. In the following Chapter, the devices developed will be analyzed both theoretically and practically.

# Chapter 7

# Thermoelectric Characterization of $\mu$TEGs

In this chapter, the microfabricated $Si_{0.7}Ge_{0.3}$ thermoelectric modules are characterized. Two different investigations are carried out on several micro-devices manufactured throughout this work. An initial electrical testing aims at investigating the internal resistance of the $\mu$TEGs. Particular interest is directed towards the discrimination between the contribution of active material and contacts to the overall internal resistance of the devices.
A second set of experiments allows a more "traditional" evaluation of the thermoelectric performances of the micro-modules. Firstly, experimental system and testing conditions are described; then, the main thermoelectric figures are extracted from the performed measurements and presented. The obtained results are compared with the values expected from modeling and the effects of isolation blocks and thermal interfaces, both of which were initially considered ideal, are discussed. Finally, the recorded thermoelectric performance is compared with the ones obtained in previous literature works.

## 7.1 Electrical Testing

As presented in previous chapters, the design of the micro devices includes several aluminum lines which allow electrical access to different combinations of thermoelectric leg pairs. Such a configuration enables the uniformity of the thermoelectric performance throughout the device to be checked and, most importantly, it allows the success and quality of the developed bonding process to be inspected. A check of the electrical continuity through sets of consecutive thermoelectric leg pairs constitutes a

simple test to detect bonding failures and to inspect the internal resistance of specific structure pairs.
Initial issues, related to both the alignment of the flip-chip placement system and the values of the down load applied during the thermo-compression bonding, resulted in weak and faulty connections. After some careful process development, the dependence of the contact resistance of the indium-indium interface to the bonding down load was identified. Such inspection allowed repeatable chip-to-chip bonds of electrically quantifiable quality to be achieved.
Figure 7.1 illustrates the mentioned dependence of the internal resistance of the microfabricated devices on the bonding down load. The resistance of the bonding interface is seen to reduce for increasing values of bonding pressure. Moreover, the different contributions to the internal resistance of the modules are discriminated. The resistance of the active material and the germanosilicide contacts are calculated for the fabricated geometries from the respective values of resistivity and contact resisitivity obtained in Chapter 4. From this analysis, it clearly emerges that the achieved bonding contact resistance only marginally contributes to the internal resistance of the $\mu$TEGs.

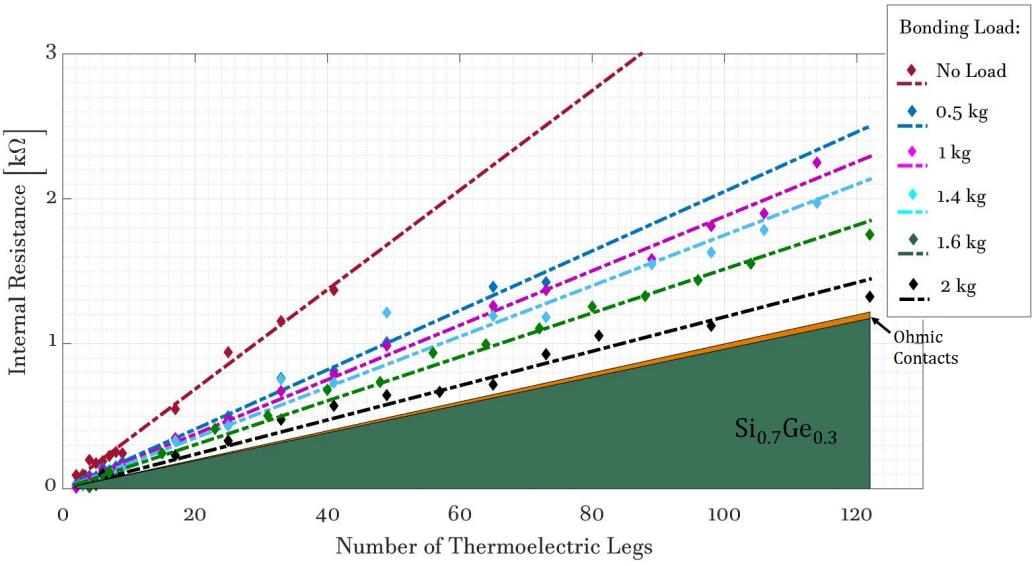



Figure 7.1: Illustrative image of the different contributions to the internal resistance of the fabricated $Si_{0.7}Ge_{0.3}$ $\mu$TEGs. The bonding contact resistance shows a clear dependence on the bonding down load. The thermoelectric material however plays the major role in contributing to the internal resistance.

With the available technology and through the process described in the previous chapter, an indium-indium bonding resistance of about 1.5 $\Omega$ per bond, corresponding

to a bonding contact resistivity of $6.631 \times 10^{-4}\,\Omega\,\mathrm{cm}^2$, was obtained.
Such values could be further improved by applying higher bonding pressures, as shown in previous work on microstructure transfer, based on flip-chip bonding using indium bumps [159]. Moreover, modern flip-chip technologies perform the bonding in a controlled $N_2$ or $Ar$ environment or in a vacuum chamber. Those conditions would prevent, or mitigate, the thermal oxidation of the metal surfaces, leading to high quality electrical contacts and to flux-less processes (unless solder reflow is needed to create the bonding bumps).
The combination of the three different contributions resulted in thermoelectric modules with internal resistances of about $1.25\,\mathrm{k}\Omega$, Figure 7.2. However, such value of internal resistance significantly differs from preliminary modeling predictions. The reason being is that the contribution of the base block geometry, which reveals to be dominant, was initially entirely neglected. The mismatch between modeled and actual internal resistance will consequently lead to significant differences between expected and recorded thermoelectric performance. A revised design for the thermocouple blocks is presented in Chapter 8.

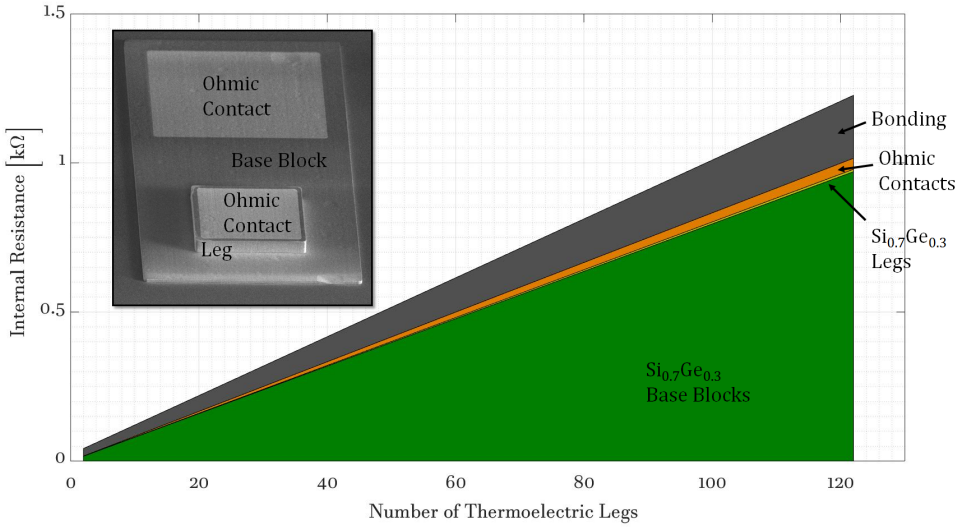



Figure 7.2: Illustrative image of the different contributions to the internal resistance of the fabricated $Si_{0.7}Ge_{0.3}$ $\mu$TEGs. The base blocks of the thermoelectric structures play the major role in contributing to the internal resistance.

## 7.2 Thermoelectric Characterization

Testing the performance of thermoelectric devices is not a straightforward task. The main reason for that lies in the need of precise measurements of heat and temperature. Moreover, the lack of recognized standards for TEG characterization often leads to difficulties in comparing different performance figures and testing conditions. Finally, the nature of the thermoelectric phenomena also has an effect in perturbing the measurements; the electrical operating point has profound influence over the thermal conditions and vice-versa.

### 7.2.1 Measurement System

The testing of $\mu$TEGs requires particular attention to some crucial details. Electrical and thermal contact resistances influence the thermoelectric performance of the device under test and they should be minimized whether possible.
As seen in Chapter 2, the power transfer between a thermoelectric generator and an external load reaches the maximum efficiency at matched impedance. A generator with high internal resistance inevitably leads to high internal energy dissipation and low energy delivered to the load. The reduction of the internal resistance by means of improved bonding resistance has already been discussed in the previous section.
Similarly, thermal interfaces contribute to the thermal resistance of the system. In particular, the interface between thermoelectric module and heat source/sink directly affects the heat flow through the generator. The use of sufficiently high mechanical compression loads, in combination with thermally conductive paste applied at the interface between different bodies to avoid air voids, is essential to guarantee good thermal contact. Moreover, thermal expansion of the TEG devices also have to be considered and compensated to maintain a stable pressure during the test.
Another criticality emerges from the need of accurate measurements of the temperature difference across the TEG under inspection. For constant temperature characterization, the temperatures of both cold and hot sides of the device have to be maintained as constant throughout the test. A drift of the average temperature of the system would indeed have effects on the performances of the device under test.
Several measurement systems have been developed and realized throughout the years by manufacturers and research groups addressing particular testing needs, budgets and specifications. In this work, the testing of the fabricated $\mu$TEGs was performed using the fully automated thermo-mechanical test rig [17] developed by Thermoelectric Conversion Systems Ltd. The system allows a number of points on the charac-

teristic current-voltage curve of the $\mu$TEGs to be collected. Increasing resistive loads are successively connected to the terminals of the thermoelectric generator under test and measurements are performed while the temperature difference across the device is maintained as constant. However, a change in the connected electrical load directly alters the heat flow through the device by the Peltier effect; thereby, it is important to achieve a thermal steady-state of the system.

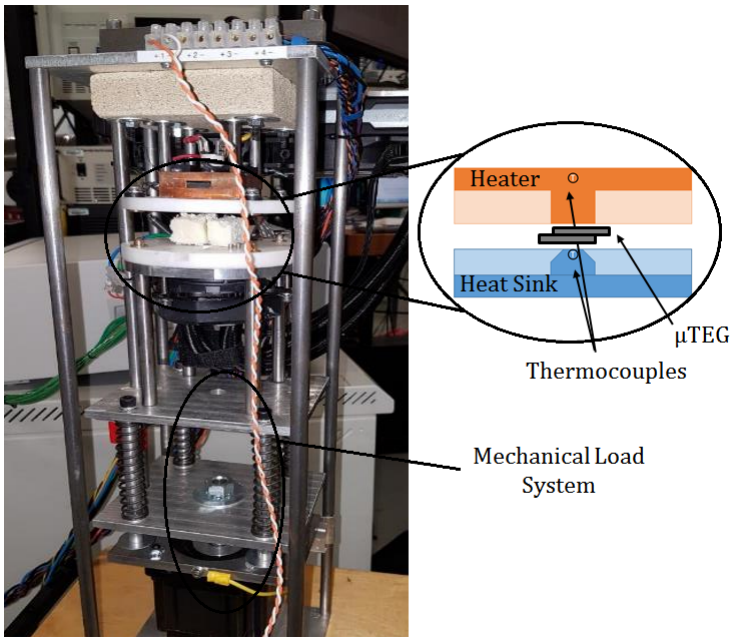



Figure 7.3: Illustrative image of the test rig used in this work. The device under characterization is mounted between the heater and the heat sink plates. Thermocouples are included to measure the temperature of the TEG hot and cold faces. A linear actuator applies the desired mechanical load to the device under test.

However, in most of the practical applications of thermoelectrics, the temperature difference across the generators is not constant, but it continuously varies depending on the heat available from the source. Therefore, although characterization at a constant temperature gradient offers useful information, such as open circuit voltage, short circuit current and internal resistance of the module under test, it does not provide information about the conversion performances of the thermoelectric device under specific operative conditions.
Unfortunately, the test system used in this work is not able to provide accurate measurements of heat flux. As a consequence, the efficiency of the power generation, Equation 2.9, and the thermal resistance of the system, defined as the ratio between temperature gradient and heat flux across the system ($R_{th} = \Delta T/Q$), cannot be directly extracted.

### 7.2.2 Effects of Mechanical Clamping Pressure

The first set of tests performed aimed to observe at inspecting the effect of the mechanical clamping pressure on the recorded thermoelectric performance of the device. Figure 7.4 and Figure 7.5 illustrate the thermoelectrical characterization curves of a fabricated micro-device, SiGeTEG7. In such characterization plots, voltage and output power are plotted on the y-axis while the corresponding values of current flowing through the device are reported on the horizontal axis. The fundamental electrical figures can all be extracted from this characterization. The intercepts with the voltage y-axis and the current x-axis respectively represent the open circuit voltage, $V_{OC}$, and the short circuit current, $I_{SC}$, of the device. Moreover, the slope of the I-V curves represents the internal resistance of the $\mu$TEGs.
The measurements reported in Figure 7.4 and Figure 7.5 were performed for different values of mechanical load, while the temperature difference between heater and heat sink was maintained constant at 10 K.

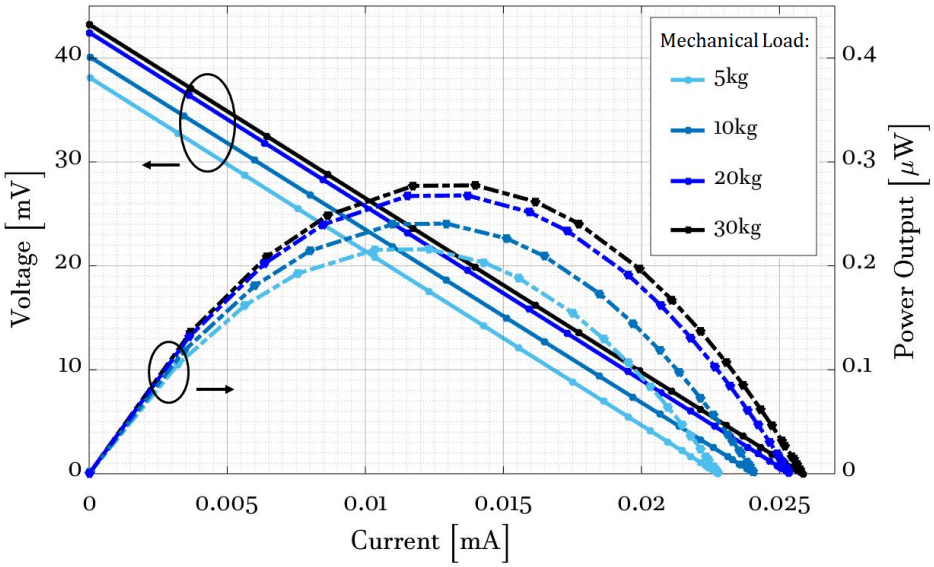



Figure 7.4: Thermoelectric characterization of the $\mu$TEG SiGeTEG7 fabricated in this work. The measurements were performed for different values of mechanical clamping load, ranging from 5 to 30 kg, while the temperature gradient across the system was maintained at 10 °C, with a heater temperature of 40 °C. Higher clamping pressures clearly lead to better performance due to reduction of the thermal resistance of the interfaces between different bodies.

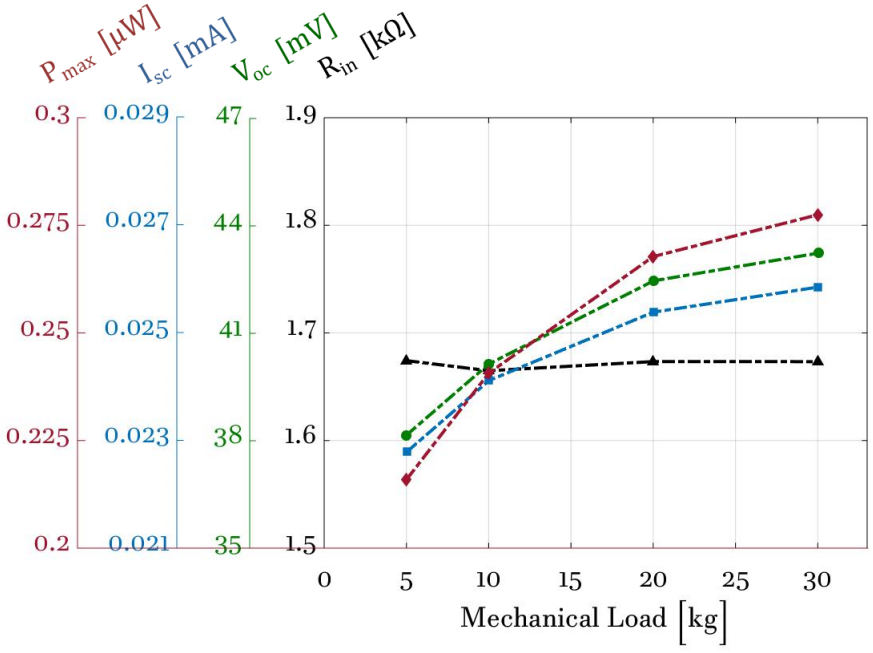



Figure 7.5: Thermoelectric figures recorded for the $\mu$TEG SiGeTEG7 tested under different mechanical clamping load. The temperature gradient across the system was maintained as constant at 10 °C, with a heater temperature of 40 °C.

The changes in recorded performance would immediately suggest the clamping pressure has an effect on the thermal resistance of the system. The thickness of the thermal grease used to mount the device on the measurement rig greatly affects the actual temperature gradient across the $\mu$TEG. The mechanical load applied during testing compresses the thermal adhesive at the interfaces, thereby affecting their thickness. Although thermally conductive pastes allow thermal contacts which are largely better than air voids, their thermal conductivity remains relatively poor, generally in the range of $0.5-3\,\mathrm{W/mK}$. Thereby, when the thickness of low thermal conductivity interfaces is comparable to that of the structures of interest, a substantial portion of the temperature gradient drops at the junctions between bodies. The results presented in Figure 7.4 and Figure 7.5 clearly show that the increase in mechanical load, from 5 to 30 kg, leads to a 12% raise in the open circuit voltage of the device under test, from 38 mV to 42.5 mV. Consequently, since the internal resistance of the $\mu$TEG remains unchanged, the maximum electrical power output increases about 30%, from 0.215 to 0.28 µW.

The above considerations already highlight the importance of thermal management in the field of micro-scaled thermoelectric devices. The effect of the thermal interfaces

was investigated under a set of simplifying assumptions and the results are presented in Figure 7.6. Considering one dimensional heat flow through a system composed of a $\mu$TEG, two thermal interfaces and heater and heat sink maintained at 10 °C temperature difference, the actual temperature gradient across the device can be calculated and plotted as a function of the thermal adhesive thickness. Unfortunately such thickness is not directly measurable under test conditions; it could however be estimated through differential measurements performed on the same system for an increasing number of interfaces. As a general indication, in the case of a 20 µm thick thermal grease layer per interface, the actual temperature gradient across the $\mu$TEG would about 5 °C, for a 10 °C temperature difference between heat source and heat sink.

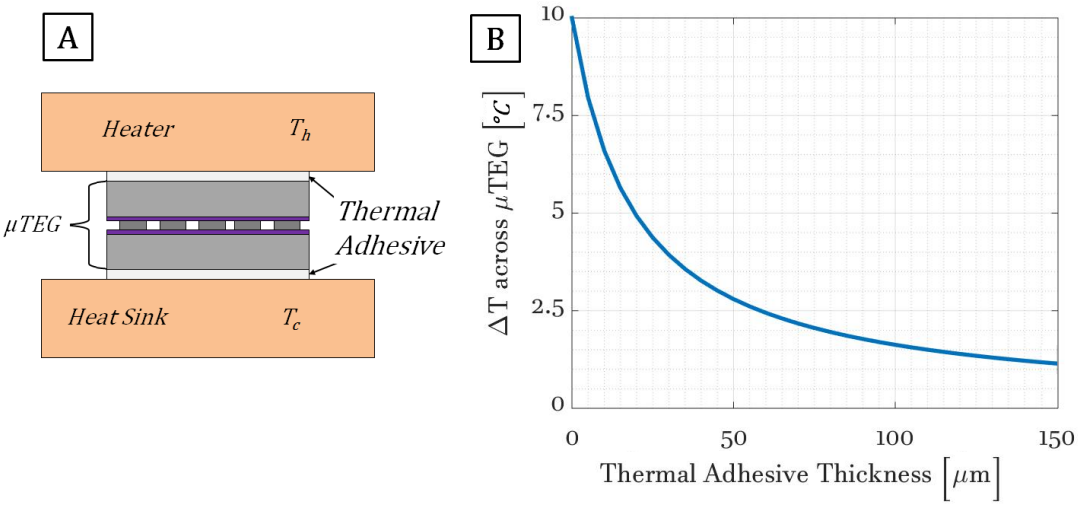



Figure 7.6: (a) Schematic of the system considered for the one dimensional heat flow simulations under constant temperature difference, $T_h - T_c$=10 °C, for different values of thermal adhesive thickness. (b) Actual temperature gradient across the $\mu$TEG calculated and plotted as a function of the thermal adhesive thickness.

Such considerations suggest characterization is performed at high values of clamping pressures in order to collect more accurate records of the performances of the micro-generators under investigation.

### 7.2.3 Thermoelectric Performance

As suggested by the analysis presented in the previous section, the manufactured $\mu$TEGs were tested and characterized under 30 kg clamping load, corresponding to a pressure of about 2.9 MPa over the 1 cm$^2$ device area. The chosen value of clamp-

ing pressure is enough to guarantee reliable thermal and electrical operation of the fabricated $\mu$TEGs, without stressing the devices to their mechanical limits. The first mechanical failures of the micro-modules only appeared for values of clamping load between 45 and 50 kg.

Figure 7.7 and Figure 7.8 summarize the thermoelectric performance of one of the microfabricated generators for different temperature gradients across the system. To limit any effect related to the temperature dependence of the material properties, the average temperature of the system is maintained constant at 30 °C throughout the entire test. The temperature of heat source and heat sink were equally increased and decreased respectively, in order to determine the desired temperature gradient while maintaining a constant average. As expected, the $\mu$TEG internal resistance remains constant; while, on the other hand, open circuit voltage and short circuit current increase linearly with the temperature gradient. Therefore, the output power curves present the characteristic quadratic dependence on the temperature gradient.

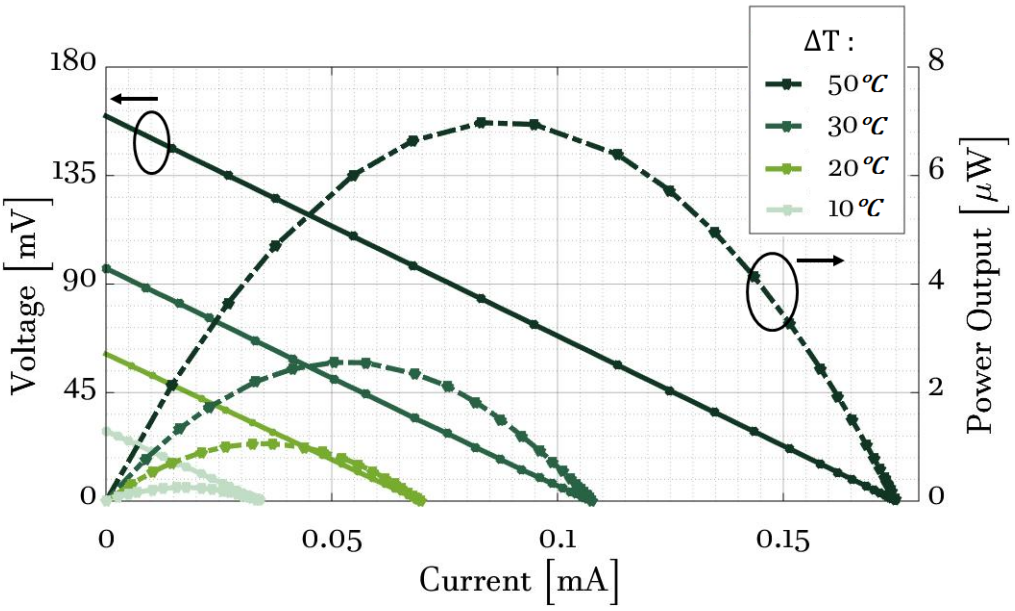



Figure 7.7: Thermoelectric characterization of the $\mu$TEG SiGeTEG16 fabricated in this work. The measurements were performed for different values of temperature gradient across the test system, ranging from 10 to 50 °C. Such measurements are taken at 30 kg clamping load.

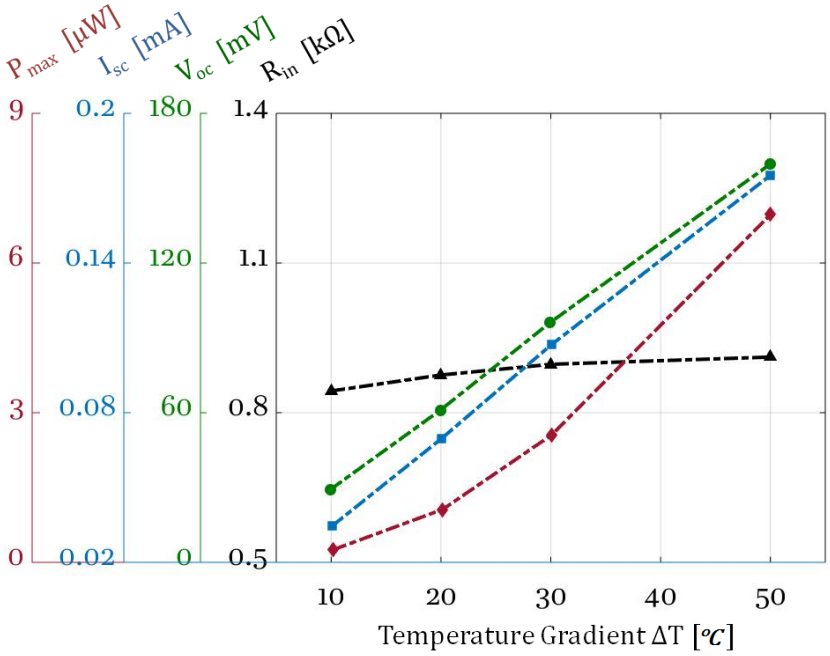



Figure 7.8: Thermoelectric figures recorded for the $\mu$TEG SiGeTEG16 tested under 30 kg clamping pressure with the temperature gradient across the system increased from 10 to 50 °C.

The maximum power output curves for the characterized micro-generators is plotted in Figure 7.9 versus the temperature gradient across the system during the measurements. Internal resistance, open circuit voltage, maximum output power and thermoelectric power factor of the characterized devices are also summarized in Table 7.1 in the case of a 50 °C temperature gradient across the system. The maximum output power density generated by one the fabricated devices, SiGeTEG21, was 24.7 µW/cm$^2$ for a 50 °C temperature gradient. On the other hand, the worst performing device, SiGeTEG11, is expected to produce 16.6 µW/cm$^2$ for the same temperature gradient. The output power density has been calculated over the area of chip occupied by the matrix of thermoelectric legs, 0.3 cm$^2$, including both the area of the active $Si_{0.7}Ge_{0.3}$ material and the spacing between structures. The whole area of the chip is indeed mostly occupied by contact lines and pads. Some spacing along the edges of the chip is also necessary in order to avoid the edge effects of the fabrication process affecting the realization of the device.

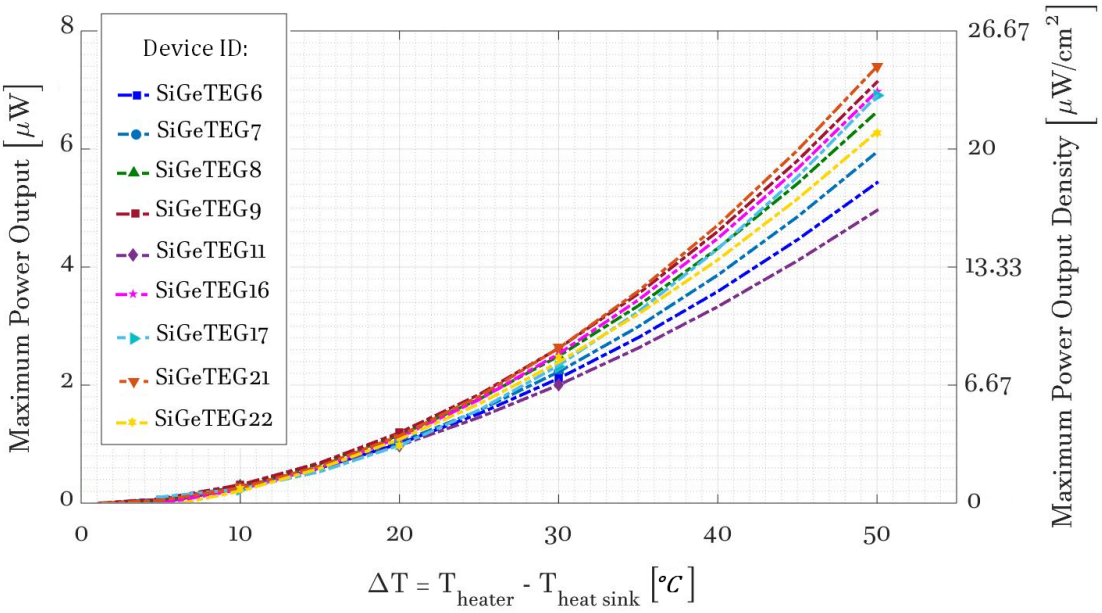



Figure 7.9: Power characteristic of some of the $\mu$TEGs developed within this work. The experiments were performed at 30 kg clamping load; the acquired measurement points are plotted with solid icons, while the dotted line presents the characteristic quadratic fitting.

The average maximum output power produced by the tested devices for a 50 °C temperature gradient is 6.41 ± 0.82 µW. The variations in the performance of the $\mu$TEGs amount to about 12.8 % and can be mainly addressed to variability in material, fabrication process and testing conditions. Material defectivity, variability and non-uniformity of the dry-etch, metal evaporation and bonding processes contribute to the variations in internal resistance of the devices. On the other hand, the variability in testing conditions directly affects the recorded thermoelectric performances, as seen for the thermal interfaces between bodies.
From the acquired measurements it is possible to calculate the thermoelectric power factor, which is defined as the ratio between the power in matched load condition and the squared temperature difference per unit area:

$$Power\ Factor = \frac{P_{max}}{\Delta T^2 A_{TEG}} \tag{7.1}$$

With thermoelectric power factors up to $9.86\times10^{-3}$ µW/(cm$^2$K$^2$), the presented $Si_{0.7}Ge_{0.3}$ $\mu$TEGs already outperform most of the previously discussed silicon-based micro-scaled thermoelectrics [77,79,93,94,98,100]. However, the thermoelectric power

factor is surely not the only parameter of interest for the application of micro-scaled thermoelectrics. The devices manufactured in this work have much smaller internal resistance and higher power output than any other silicon-based $\mu$TEG in the literature [76, 77, 79, 90, 92–94, 98–101]. As a matter of fact, the smallest internal resistance recorded in literature for a silicon-based $\mu$TEG amounts to 84 kΩ [93], with most of the other works revealing even higher internal resistance values, well in the MΩ range. From a mere output power perspective, only another silicon-based thermoelectric micro-device [76] proved to produce more than 2 µW. Moreover, being the only silicon-based $\mu$TEGs in literature designed in cross-plane configuration, the devices developed in this work have been compared to micro-modules having much longer thermoelectric legs (100 µm or more [76, 77, 79, 92–94, 98]). Such performances, together with the unique cross-plane design, make the devices fabricated in this work more suitable for application.
Changes in geometry and design could further improve the thermoelectric figures of the manufactured devices, whose performance at room temperature is however nowhere near those of the best bismuth-telluride-based technology [75].

| **Device** | $\mathbf{R}_{int}$ [kΩ] | $\mathbf{V}_{oc}$ [mV] | $\mathbf{P}_{max}$ [µW] | **Power Factor** [µW/(cm$^2$K$^2$)] |
|---|---|---|---|---|
| SiGeTEG6* | 1.41 | 182.2 | 5.43 | $7.24\times10^{-3}$ |
| SiGeTEG7* | 1.53 | 198.5 | 5.95 | $7.93\times10^{-3}$ |
| SiGeTEG8* | 1.36 | 197.7 | 6.63 | $8.84\times10^{-3}$ |
| SiGeTEG9* | 1.39 | 207.6 | 7.13 | $9.51\times10^{-3}$ |
| SiGeTEG11* | 1.42 | 175.2 | 4.96 | $6.61\times10^{-3}$ |
| SiGeTEG16 | 0.95 | 169.8 | 6.97 | $9.30\times10^{-3}$ |
| SiGeTEG17 | 1.12 | 183.2 | 6.90 | $9.21\times10^{-3}$ |
| SiGeTEG21 | 1.25 | 200.5 | 7.39 | $9.86\times10^{-3}$ |
| SiGeTEG22 | 1.21 | 181.4 | 6.28 | $8.37\times10^{-3}$ |

* Values extracted from fitting.

Table 7.1: Thermoelectric figures recorded for the $\mu$TEGs tested at a 50 °C temperature gradient under a 30 kg clamping load.

#### 7.2.3.1 Experiment vs Model

The mismatch between the expected thermoelectric performance, modeled in Chapter 5, and the experimental measurements are obvious.

The preliminary modeling suggested the micro-devices to be able to produce around 640 µW and 175 mV when operating in matched load conditions with a 30 °C temperature gradient. Moreover, the internal resistance of the device was expected to be of only 50 Ω. The fabricated $\mu$TEGs revealed an internal resistance of around 1.25 kΩ and they were able to produce around 3 µW and 50 mV with a 30 °C temperature gradient.
However, the In-In bonding contact resistance, the resistance of the $Si_{0.7}Ge_{0.3}$ isolation blocks and the thermal interfaces between the module and heater and heat sink plates were entirely neglected throughout the modeling phase.
Figure 7.10 presents the power and voltage curves calculated from modeling, considering all the contributions to the internal resistance of the micro-devices, for 30 °C and 9 °C temperature gradients. Such characteristics are compared to experimental measurements acquired for the device SiGeTEG16 at 30 °C temperature gradient.

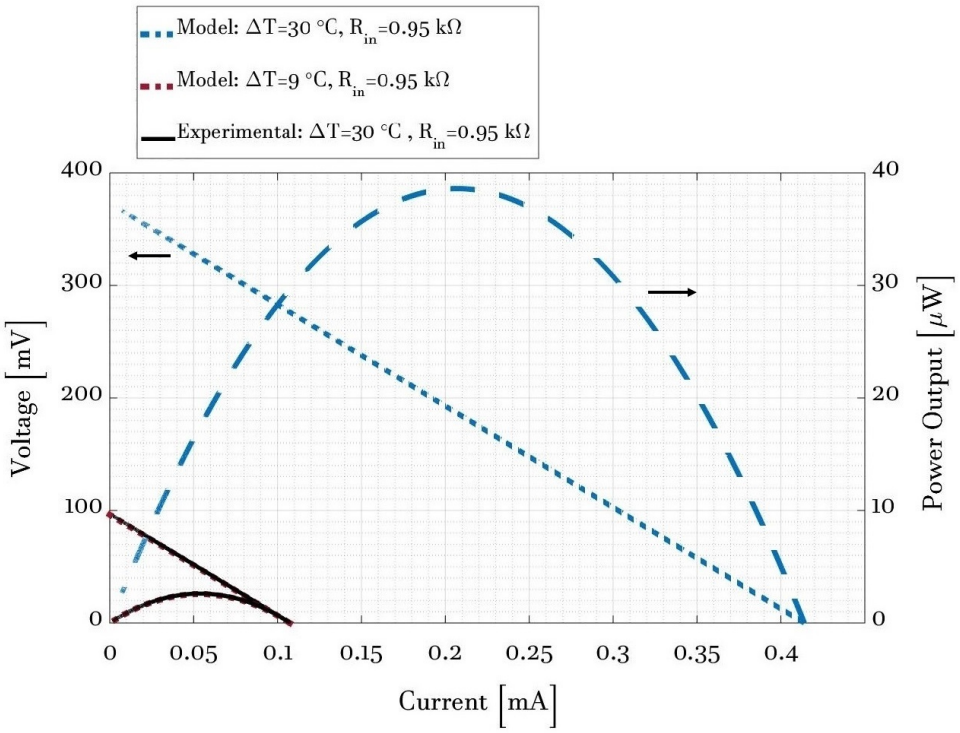



Figure 7.10: Power and voltage curves calculated from modeling for 30 °C and 9 °C temperature gradient together with the experimental measurements of device SiGeTEG16 at 30 °C temperature gradient.

It can be noted that model and experiments finally match when all the contribution to the internal resistance of the micro-modules are considered and the temperature gradient is much lower than the actual setpoint between heater and heat sink.

As previously discussed, such a mismatch can be addressed to the role played by the thermal interfaces.
Thereby, the thermoelectric performances extracted from the acquired measurements are actually an underestimate of the potential of the fabricated $\mu$TEGs as they include the effect of thermal interfaces external to the devices. Integrated thermometers would be necessary to measure the temperature difference directly across the microdevice.

### 7.2.4 Temperature Dependence of Thermoelectric Performance

It is however well known, as seen in Chapter 2, that silicon germanium alloys reveal their optimum thermoelectric performances at high temperature. The devices designed and manufactured in this work are also expected to perform at their best at operating temperatures of around 300 °C.
Unfortunately, due to the temperature limits of the utilized test rig, the fabricated $\mu$TEGs could only be characterized up to around 130 °C. In order to highlight the temperature dependence of the thermoelectric figures of the silicon germanium micromodules, the latter were tested for increasing values of the average temperature of the system. The clamping load was set to 30 kg, the temperature gradient across the system was fixed to 10 °C, while the heater temperature was varied from 20 to 125 °C. Figure 7.11 presents the thermoelectric characterization of the $\mu$TEG SiGeTEG16. The temperature dependence of the thermoelectric figures is graphically presented in Figure 7.12. The power generation of the device appears to monotonically increase, up to almost twice its initial value, over the range of temperature inspected. Consequently, the thermoelectric power factor also increases with the average temperature of the system, reaching a peak value of $13.9\times10^{-3}$ µW/(cm$^2$K$^2$), Figure 7.13.
From the fitting of such characterization measurements, a thermoelectric power factor of around 40-50$\times10^{-3}$ µW/(cm$^2$K$^2$) and a maximum power output of 1.2-1.5 mW could be expected for a 10 °C temperature gradient at around 300 °C.

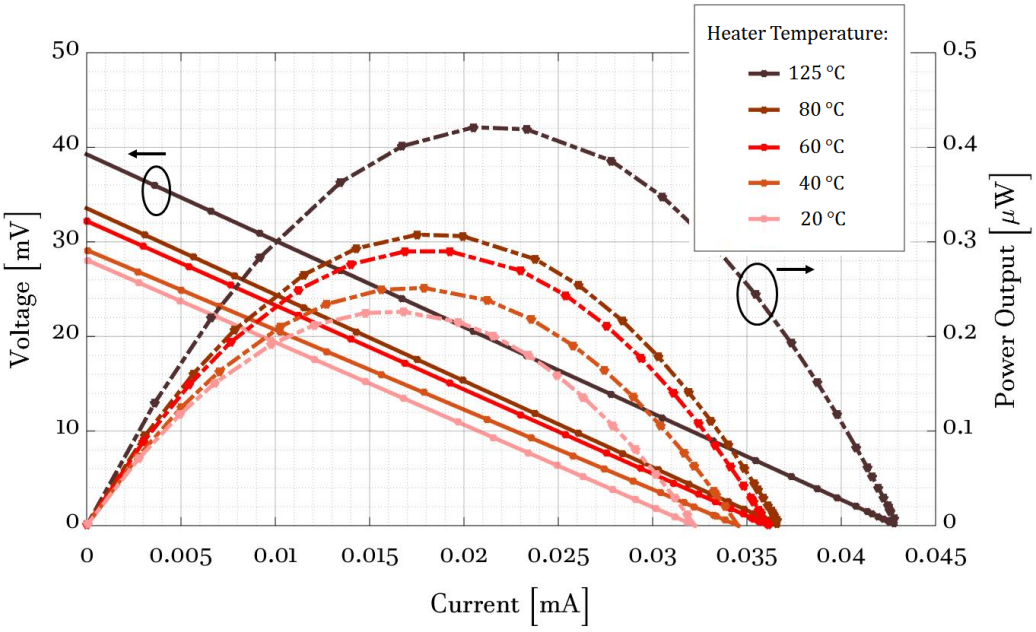



Figure 7.11: Thermoelectric characterization of the $\mu$TEG SiGeTEG16 fabricated in this work. The measurements were performed at a 30 kg clamping load and a 10 °C temperature gradient across the system. The heater temperature is varied from 20 to 125 °C, thereby determining a consequent increase in the average temperature of the system.

However, it must be noted that forecasting the device performance over a temperature range which is well distant from the one directly investigated could result in a really inaccurate approximation. The thermoelectric performance of *SiGe* alloys has proved to peak at really high temperatures (>>300 °C); thereby the thermoelectric performance of the designed and fabricated micro-modules could still be comfortably expected to improve monotonically to around 300 −400 °C. The values extracted from fitting can then provide a credible indication of the potential of the modules. The expectation would however need to be backed up by high temperature measurements.

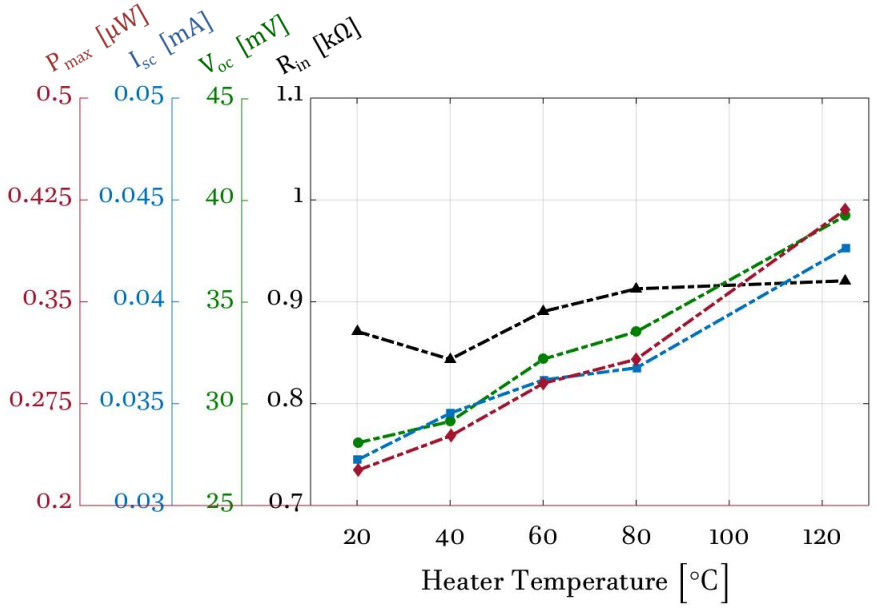



Figure 7.12: Thermoelectric figures recorded for the $\mu$TEG SiGeTEG16 tested under a 30 kg mechanical clamping load and a 10 °C temperature gradient across the system. The temperature of the heater is increased from 20 to 125 °C; the average temperature of the system increases accordingly.

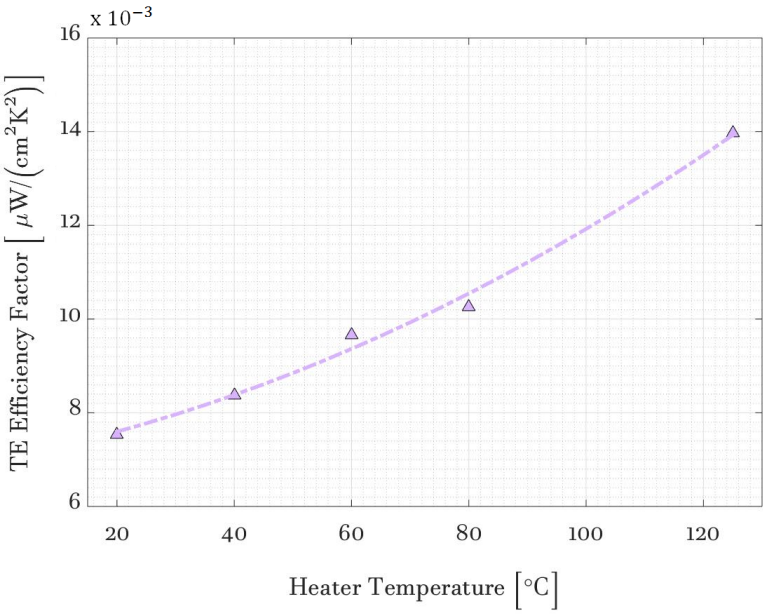



Figure 7.13: Thermoelectric power factor recorded for the $\mu$TEG SiGeTEG16 tested under a 30 kg mechanical clamping load and a 10 °C temperature gradient across the system. The temperature of the heater is increased from 20 to 125 °C, the average temperature of the system increases accordingly.

## 7.3 Chapter Conclusions

Characterization of the manufactured $\mu$TEGs, realized with a cross-plane heat flow and vertically fabricated thermocouples design on bulk $Si_{0.7}Ge_{0.3}$ grown on SOI substrate, has been successfully demonstrated. The recorded measurements present interesting figures for performance, demonstrating the capability of these structures as a power source for autonomous micro-systems.

The micro-devices were characterized with respect to their electrical and thermoelectric behavior. Although the internal resistance is revealed to be higher than expected from modeling, the devices processed in this work still present smaller electrical resistance than any other silicon-based $\mu$TEG in the literature. With a thermoelectric power factor up to $13.9\times10^{-3}$ µW/(cm$^2$K$^2$), achieved at an operating temperature of around 110 °C, the presented micro-modules outperform most of the existing silicon-based thermoelectrics, all of which rely on the advantage of longer thermoelectric legs allowed by the in-plane configuration. The presented devices also delivered the highest maximum output power density, 24.7 µW/cm$^2$ obtained at room temperature for a 50 °C temperature gradient, when compared to silicon-based $\mu$TEGs in the literature.

# Chapter 8

# Conclusions and Future Work

## 8.1 Conclusions

The world's increasing demand for energy, together with the impact of the combustion of fossil fuels, has raised a social and political awareness about the necessity of sustainable energy systems. Over the last decades, renewable energy power generation and energy harvesting systems have therefore become an object of intensive research.

As every system generates unused waste heat that could be reconverted to electricity, the potential applications of TEGs range over many different fields: from the automotive and industrial fields to wearable electronics, bio-integrated systems, cybernetics and others.

State-of-the-art micro-scaled thermoelectric generators are currently based on tellurium alloys and only address room temperature applications with an 18% Carnot efficiency and a maximum output power density per degree Kelvin of $1.12\,\mathrm{mW/cm^2K}$ [12]. State-of-the-art bulk thermoelectrics also rely on rare (i.e. tellurium is the 9th rarest element on earth) and toxic (i.e. tellurium, bismuth, lead, antimony) elements. Silicon-germanium-based thermoelectric devices represent a more sustainable option and their employment is supported by well-established and cost-effective fabrication capabilities. The technological strengths and MEMS-CMOS compatibility are the main reasons that have attracted the interest of the energy harvesting field. Silicon-germanium alloys have already proved to have the best thermoelelctric efficiency at very high temperatures (above $600\,^{\circ}\mathrm{C}$). However, very little has been done to convert the efforts spent in engineering material and designing low-dimensional structures into the fabrication of devices and micro-devices able to perform at lower temperatures and to be cost-effective in the energy harvesting market.

The work carried out throughout this Ph.D. successfully demonstrated the development of silicon-germanium alloy $\mu$TEGs for heat recovery applications. Most importantly, the configuration and the fabrication process of such silicon-based generators constitute a platform to transfer the results of decades of promising material investigations and engineering into practical micro-scaled TEGs. Thereby, in agreement with the vision of the Energy Technology Partnership, funders of this Ph.D., this work developed the technical knowledge to fill the gap between preliminary material characterization and testing, and reproducible manufacturing.

In this project, silicon-germanium alloys have been reviewed, commercially grown in wafer format and micro-processed.
The optimum germanium composition, $x$, and alloy doping density, $d$, to maximise the thermoelelctric performances of the alloy in the mid temperature range ($300 - 500\,°C$) were investigated and identified to be $x = 0.3$ and $d = 1 \times 10^{19}\,cm^{-3}$ for both p- and n-type materials. $20\,\mu m$ of highly doped p- and n-type $Si_{0.7}Ge_{0.3}$ alloys were then grown by CVD on top of separate SOI substrates at IQE Silicon Compounds [16]. Both p- and n-type wafers were inspected, and despite their high defectivity (expected treading dislocation density of $5 \times 10^6\,cm^{-2}$), they were processed for characterization.
Ohmic contacts based on the formation of platinum germanosilicide were developed and investigated through CTLMs. 100 nm of Pt was deposited by electron-beam evaporation, patterned by photolithography and annealed at 600 °C for 30 s in an $N_2$ environment. Contact resistivity values as low as $6.5 \pm 0.5 \times 10^{-5}\ \Omega\,cm^2$ and $1.5 \pm 0.5 \times 10^{-4}\ \Omega\,cm^2$ were obtained for n- and p-type highly doped $Si_{0.7}Ge_{0.3}$ alloys respectively. Moreover, the extracted values are comparable to the ones obtained for nickel germanosilicide contacts with the advantage of higher formation temperature, which guarantees thermal stability over the desired operation temperature of the devices. The electrical conductivity of the materials was investigated through CLTM arrangements and was $12000 \pm 1200\,S\,m^{-1}$ for the p-type and $7200 \pm 700\,S\,m^{-1}$ for the n-type alloy, showing good agreement with previous literature work.
The thermal conductivity of the $Si_{0.7}Ge_{0.3}$ alloys was investigated by Raman thermometry and measured to be $5.9 \pm 0.6\,W/mK$ and $5.6 \pm 0.6\,W/mK$ for p- and n-type materials respectively.
The modeling of the silicon-germanium based $\mu$TEG operating in cross-plane configuration was then undertaken and the optimum leg number and geometry were calculated for the case of a module connected in series with a $50\,\Omega$ electrical load

and operating at around room temperature under a constant temperature gradient of 30 K. The optimum $\mu$TEG design is formed by 64 thermoelelctric leg pairs, with p- and n-type cross-sectional leg areas of $250 \times 250$ µm$^2$ and $150 \times 150$ µm$^2$ respectively. According to modeling, the device is expected to have a room temperature internal resistance of 50 Ω and an effective thermal conductance of 1.61 W K$^{-1}$ at open-circuit. The device performances have also been investigated under the above specified operating conditions, leading to an expected output power of about 640 µW and voltage of 175 mV.

The micro-fabrication processes developed in this work for the realization of the cross-plane configuration thermoelectric micro-devices entirely relied on the James Watt Nanofabrication Centre (JWNC) technologies and expertise. Considerable time and effort were dedicated to develop every process step and the standards of fabrication achieved are witnessed by several building blocks being novel or, if already present in literature, representing the state-of-the-art in the field of micro-scaled thermoelectricity. Indium and silver were adopted to realize the intermetallic compound for the flip-chip bonding assembly. By tuning the ratio between the two components, the intermetallic bonding layer was designed to have a high melting point and thereby to be stable in the temperature range of interest. With the available technology, a bonding resistance of about 1.5 Ω per bond, corresponding to a bonding contact resistivity of $6.631 \times 10^{-4}\,\Omega\,\text{cm}^2$, was obtained.

The characterization of the manufactured $\mu$TEGs was performed using a fully automated thermo-mechanical test rig with the technical support of Thermoelectric Conversion Systems Limited [17]. The measurements of the micro-modules fabricated in this work reveal interesting figures for performance, demonstrating the potential of such structures as a power source for autonomous micro-systems. With thermoelectric power factors up to $13.9 \times 10^{-3}$ µW/(cm$^2$K$^2$) and maximum output power density up to 24.7 µW/cm$^2$, the presented $Si_{0.7}Ge_{0.3}$ $\mu$TEGs already outperform most of the known silicon-based micro-scaled thermoelectrics [77, 79, 93, 94, 98, 100]. Although the internal resistance of the fabricated devices, 1.25 kΩ, was higher than expected from modeling, it is still more than one order of magnitude smaller than that of any other silicon-based $\mu$TEG in literature [76, 77, 79, 90, 92–94, 98–101]. Moreover, the micro-modules developed in this work are currently the only example of cross-plane configuration silicon-based $\mu$TEGs, leading the way to broader applicability of micro-devices for energy harvesting.

At around room temperature, the micro-devices manufactured in this work are still not as high performing as the state-of-the-art bismuth-telluride based technology.

However, at around 300 °C, the silicon-based $\mu$TEG developed are expected to produce a maximum power output of 1.2-1.5 mW under a 10 °C temperature gradient, leading to an output power density per degree Kelvin of 0.39-0.50 mW/cm$^2$K, which corresponds to 35-45% of the room temperature performance of the only commercial $\mu$TEG devices [75].
In accordance with the initial aims of the project, the work carried out throughout this Ph.D. successfully achieved:

- Developement of thermally stable electrical Ohmic contacts with low specific contact resistivity based on the formation of platinum germanosilicide.
- Design of a micro-scaled thermoelelctric generator characterized by a novel cross-plane configuration.
- Development of a low contact resistance, flip-chip based, metal bonding which proved to be thermally stable over the expected operating temperature range (300-500 °C).
- Development of a complete, repeatable and reliable fabrication process for micro-scaled TEGs entirely based on ICP dry-etching, PECVD $Si_3N_4$ deposition and electron beam and thermal metal evaporation. The micro-fabrication process is fully MEMS-CMOS compatible.
- Complete thermoelectric characterization of the developed technology was performed to invesigate performance and limitation of the fabricated devices.

## 8.2 Future Work

### 8.2.1 High-Temperature Characterization and Application Case Study

Although the automotive industry was the initial target application of the technology developed in this work and the micro-devices have been realized so to sustain and perform in the 300 to 500 °C range, it was not possible to perform any high temperature device characterization throughout this Ph.D. The only thermal treatment performed on previously characterized samples consisted of the exposure to a 450 °C atmospheric environment for 48 h. No signs of debonding nor changes in the internal resistance of the devices occurred. Therefore, the natural continuation in the evaluation of the micro-modules would include high temperature measurements. A complete high-temperature characterization could also be followed by an application case study in order to quantify the potential of the technology applied to the automotive field.
Over the last decades, the car industry has been a desired application target of the energy harvesting field due to low fuel efficiency [3] and enormous market opportunities. Attempts to improve the overall system efficiency and to replace the vehicles' shaft-driven alternator with bulk TEGs mounted on the exhaust stream have already been undertaken [6–10] and more are still on going.

### 8.2.2 Design Improvement

Throughout this work, the importance of thermal management and inclusive designs have been highlighted. The effect of all the electric contact resistances, both the Ohmic contact resistance and the metal bonding one, and thermal contact resistance have shown to play a major effect on the operation of micro-scaled thermoelectrics.
Another feature that was wrongly neglected was the silicon-germanium isolation block, which is responsible for most of the internal resistance of the device. With respect to this object, a simple fabrication adjustment could help reducing its deleterious effect on the performance of the micro-devices. In fact, the design of a larger metal contact pad would allow the short-circuit of the isolation block, Figure 8.1. Such correction would largely improve the performance of the $\mu$TEGs also enhancing their applicability, especially in the field of autonomous sensors.

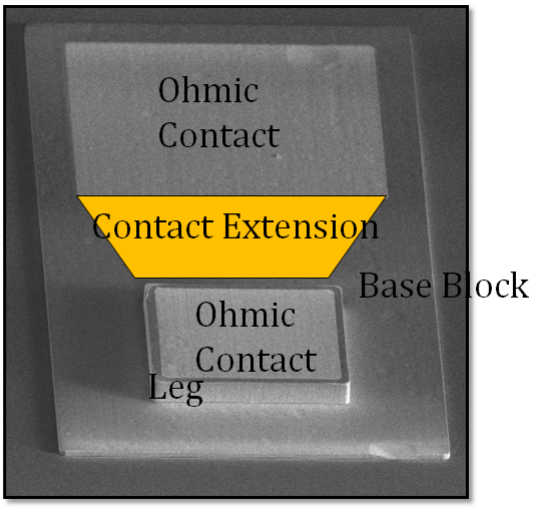



Figure 8.1: Illustrative image of a possible design improvement to reduce the internal resistance of the fabricated $Si_{0.7}Ge_{0.3}$ $\mu$TEGs. The Ohmic contact evaporated on the silicon-germanium isolation block could be patterned so to reach the bottom of the thermoelectric leg creating a low resistance path.

### 8.2.3 Integration of Low Dimensional Structures

The work carried out throughout this Ph.D. successfully demonstrated the development of the configuration and fabrication process for silicon-based devices that could constitute a platform to transfer the results of decades of material investigations into micro-scaled TEGs. Low-dimensional materials have already proved, both theoretically and experimentally, to be able to increase the thermoelelctric figures of a material by a decoupling of the transport processes. The introduction of nanostructures in bulk silicon would indeed have the effect of improving the thermoelelctric figure of merit of silicon due to a reduction of the phonon contribution to thermal conductivity which does not adversely affect the electronic transport properties.
Thin film, quantum-wells, nanowires, nanomesh and nanocristalline grains have long been studied and characterized from a thermoelectric point of view, but none of the listed has been successfully integrated into a micro-generator.
The main potential development of this work would then be the integration of low-dimensional structures into the developed silicon-based $\mu$TEG platform, Figure 8.2.

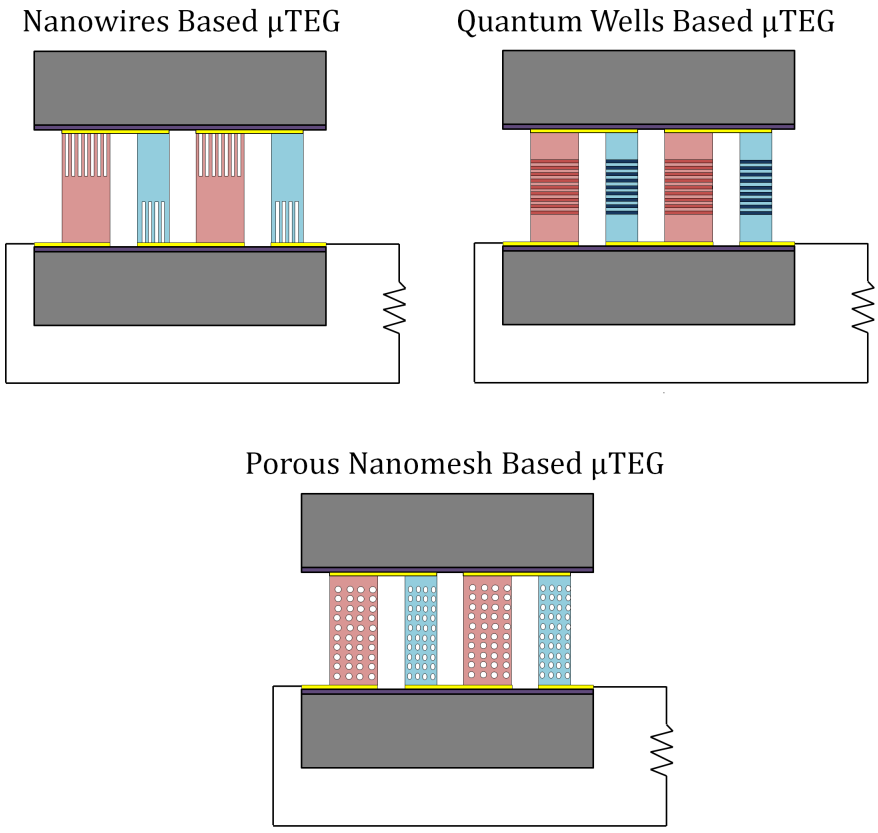



Figure 8.2: Illustrative schematics presenting the possible integration of low-dimensional structures into the silicon-based $\mu$TEG configuration developed in this work.

With a touch of optimism and vision, such low-dimensional micro-modules could be pictured to be directly integrated on-chip during the fabrication process of CMOS sensors for the realization of a complete autonomous system.

# Bibliography


[1] http://www.un-documents.net/our-common-future.pdf. Accessed: 2017-11-04.

[2] http://edgar.jrc.ec.europa.eu. Accessed: 2017-11-04.

[3] http://www.fueleconomy.gov/feg/atv.shtml. Accessed: 2017-02-06.

[4] G. Meisner, "Skutterudite thermoelectric generator for automotive waste heat recovery," *3rd Thermoelectrics Application Workshop*, 2012.

[5] https://www.afdc.energy.gov/pdfs/freedomcar_plan.pdf. Accessed: 2018-05-05.

[6] E. F. Thacher, B. T. Helenbrook, M. a. Karri, and C. J. Richter, "Testing of an automobile exhaust thermoelectric generator in a light truck," *Proceedings of the Institution of Mechanical Engineers, Part D: Journal of Automobile Engineering*, vol. 221, no. 1, pp. 95–107, 2007.

[7] N. Espinosa, M. Lazard, L. Aixala, and H. Scherrer, "Modeling a thermoelectric generator applied to diesel automotive heat recovery," *Journal of Electronic Materials*, vol. 39, no. 9, pp. 1446–1455, 2010.

[8] M. Mori, T. Yamagami, M. Sorazawa, T. Miyabe, S. Takahashi, and T. Haraguchi, "Simulation of fuel economy effectiveness of exhaust heat recovery system using thermoelectric generator in a series hybrid," *SAE International Journal of Material Manufacturing*, vol. 4, no. 4, pp. 1268–1276, 2011.

[9] J. LaGrandeur, D. Crane, S. Hung, A. Mazar, and A. Eder, "Automotive waste heat conversion to electric power using skutterudite, TAGS, PbTe and BiTe," *International Conference on Thermoelectrics*, pp. 343–348, 2006.

[10] Q. Hussain, D. Brigham, and C. Maranville, "Thermoelectric exhaust heat recovery for hybrid vehicles," *SAE International Journal of Engines*, no. 2, pp. 1132–1142, 2009.

[11] J. G. G. Fagas, L. Gammaitoni and D. Paul, *ICT- Energy Concepts for Energy Efficiency and Sustainability*. Intech, 2015.

[12] H. Böttner, J. Nurnus, A. Schubert, and F. Volkert, "New high density micro structured thermogenerators for stand alone sensor systems," *Measurement Techniques*, pp. 4–7, 2007.

[13] G. L. Bennett, "Space nuclear power: opening the final frontier," *Applied Physics*, no. June, pp. 26–29, 2006.

[14] L. A. Dudzinski, "Radioisotope power : a key technology for deep space exploration," *60th International Astronautical Congress 2009, IAC 2009*, vol. 8, pp. 6612–6633, 1961.

[15] https://www.etp-scotland.ac.uk/. Accessed: 2017-11-04.

[16] http://www.iqep.com/. Accessed: 2017-11-04.

[17] http://www.teconversion.com/tcs/test-equipment/. Accessed: 2017-09-06.

[18] D. Rowe, *Thermoelectrics Handbook: Macro to Nano*. CRC Taylor and Francis, 2006. Ch.1.

[19] E. Altenkirch, "Über den nutzeffekt der thermosäule," *Physikalische Zeitschrift*, vol. 10, no. 16, pp. 560–568, 1909.

[20] E. Altenkirch, "Elektrochemische kälteerzeugung und reversible elektrische heizung," *Physikalische Zeitschrift*, vol. 12, no. 1, pp. 920–924, 1911.

[21] C. B. Vining, "An inconvenient truth about thermoelectrics.," *Nature materials*, vol. 8, no. 2, pp. 83–85, 2009.

[22] D. M. Rowe and G. Min, "Design theory of thermoelectric modules for electrical power generation," *IEE Proceedings-Science, Measurement and Technology*, vol. 143, no. 6, pp. 351–356, 1996.

[23] G. J. Snyder and E. S. Toberer, "Complex thermoelectric materials," *Nature materials*, vol. 7, no. 2, pp. 105–114, 2008.

[24] J. Callaway, "Model for lattice thermal conductivity at low temperatures," *Physical Review*, vol. 113, no. 4, pp. 1046–1051, 1959.

[25] B. Nag, "Electron transport in compound semiconductors," *Solid State Sciences*, vol. 11, 1980.

[26] G. Chester and A. Thellung, "The Law of Wiedemann and Franz," *Proceedings of the Physical Society*, vol. 77, no. 5, pp. 1005–1013, 1961.

[27] G. A. Slack, *Thermoelectrics Handbook: Macro to Nano.* CRC Taylor and Francis, 2006. Ch. 34.

[28] C. Dames and G. Chen, "Theoretical phonon thermal conductivity of Si/Ge superlattice nanowires," *Journal of Applied Physics*, vol. 95, no. 2, pp. 682–693, 2004.

[29] Y. Hu, L. Zeng, A. Minnich, M. Dresselhaus, and G. Chen, "Spectral mapping of thermal conductivity through nanoscale ballistic transport," *Nature Nanotechnology*, vol. 10, no. 8, pp. 701–706, 2015.

[30] F. D. Rosi, E. F. Hockings, and N. E. Lindenblad, "Semiconducting materials for thermoelectric power generation," *RCA Review*, vol. 22, pp. 82–121, 1961.

[31] F. D. Rosi, "Thermoelectricity and thermoelectric power generation," *Solid State Electronics*, vol. 11, p. 833, 1968.

[32] C. Wood, "Materials for thermoelectric energy conversion," *Reports on Progress in Physics*, vol. 51, pp. 459–539, 1988.

[33] H. J. Goldsmid and R. W. Douglas, "The use of semiconductors in thermoelectric refrigeration," *British Journal of Applied Physics*, vol. 5, pp. 386–390, 1954.

[34] H. Scherrer and S. Scherrer, *In CRC Thermoelectrics Handbook: Macro to Nano.* CRC Taylor and Francis, 2006. Ch. 27.

[35] V. A. Kutasov, L. N. Lukyanova, and M. V. Vedernikov, *CRC Thermoelectrics Handbook: Macro to Nano.* CRC Taylor and Francis, 2006. Ch. 37.

[36] V. L. Kuznetsov, L. A. Kuznetsova, A. E. Kaliazin, and D. M. Rowe, "High performance functionally graded and segmented $Bi_2Te_3$-based materials for thermoelectric power generation," *Journal of Materials Science*, vol. 37, no. 14, pp. 2893–2897, 2002.

[37] Y. Gelbstein, Z. Dashevsky, and M. P. Dariel, "High performance n-type PbTe-based materials for thermoelectric applications," *Physica B Condensed Matter*, vol. 363, pp. 196–205, 2005.

[38] K. F. Hsu, S. Loo, F. Guo, W. Chen, and J. S. Dyck, "Bulk thermoelectric materials with high figure of merit," *Science*, vol. 303, pp. 818–821, 2004.

[39] E. Skrabek and D. S. Trimmer, "Thermoelectric device including an alloy of GeTe and AgSbTe as the p-type element," *US Patent*, no. US 3945855, 1976.

[40] C. M. Bhandari and D. M. Rowe, "SiliconGermanium alloys as high-temperature thermoelectric materials," *Contemporary Physics*, no. 3, pp. 219–242, 1980.

[41] M. N. Tripathi and C. M. Bhandari, "High-temperature thermoelectric performance of Si-Ge alloys," *Journal of Physics: Condensed Matter*, vol. 15, pp. 53–59, 2003.

[42] J. R. Salvador, J. Y. Cho, Z. Ye, J. E. Moczygemba, A. J. Thompson, J. W. Sharp, J. D. Koenig, R. Maloney, T. Thompson, J. Sakamoto, H. Wang, and A. A. Wereszczak, "Conversion efficiency of skutterudite-based thermoelectric modules," *Physical chemistry chemical physics : PCCP*, vol. 16, no. 1, pp. 12510–20, 2014.

[43] G. Nie, S. Suzuki, T. Tomida, A. Sumiyoshi, T. Ochi, K. Mukaiyama, M. Kikuchi, J. Q. Guo, A. Yamamoto, and H. Obara, "Performance of skutterudite-based modules," *Journal of Electronic Materials*, vol. 46, no. 5, pp. 1–5, 2016.

[44] J. Q. Guo, H. Y. Geng, T. Ochi, S. Suzuki, M. Kikuchi, Y. Yamaguchi, and S. Ito, "Development of skutterudite thermoelectric materials and modules," *Journal of Electronic Materials*, vol. 41, no. 6, pp. 1036–1042, 2012.

[45] S. Bhattacharya, a. L. Pope, R. T. Littleton, T. M. Tritt, V. Ponnambalam, Y. Xia, and S. J. Poon, "Effect of Sb doping on the thermoelectric properties of Ti-based half-Heusler compounds," *Applied Physics Letters*, vol. 77, no. 16, p. 2476, 2000.

[46] F. Casper, T. Graf, S. Chadov, B. Balke, and C. Felser, "Half-Heusler compounds: novel materials for energy and spintronic applications," *Semiconductor Science and Technology*, vol. 27, no. 6, p. 063001, 2012.

[47] G. Schierning, R. Chavez, R. Schmechel, B. Balke, G. Rogl, and P. Rogl, "Concepts for medium-high to high temperature thermoelectric heat-to-electricity conversion: a review of selected materials and basic considerations of module design," *Translational Materials Research*, vol. 2, no. 2, p. 025001, 2015.

[48] K. Bartholome, B. Balke, D. Zuckermann, M. Kohne, M. Muller, K. Tarantik, and J. Konig, "Thermoelectric modules based on half-heusler materials produced in large quantities," *Journal of Electronic Materials*, vol. 43, no. 6, pp. 1775–1781, 2014.

[49] N. N. Van and N. Pryds, "Nanostructured oxide materials and modules for high-temperature power generation from waste heat," *Advances in Natural Sciences: Nanoscience and Nanotechnology*, vol. 4, no. 2, p. 023002, 2013.

[50] S. Urata, R. Funahashi, T. Mihara, A. Kosuga, S. Sodeoka, and T. Tanaka, "Power generation of a p-type $Ca_3Co_4O_9$ / n-type $CaMnO_3$ module," *International Journal of Applied Ceramic Technology*, vol. 4, no. 6, 2007.

[51] I. Matsubara, R. Funahashi, T. Takeuchi, S. Sodeoka, T. Shimizu, and K. Ueno, "Fabrication of an all-oxide thermoelectric power generator," *Applied Physics Letters*, vol. 78, no. 23, pp. 3627–3629, 2001.

[52] R. Funahashi, S. Urata, K. Mizuno, T. Kouuchi, and M. Mikami, "$Ca_{2.7}Bi_{0.3}Co_4O_9$ - $La_{0.9}Bi_{0.1}NiO_3$ thermoelectric devices with high output power density," *Applied Physics Letters*, vol. 85, no. 6, p. 1036, 2004.

[53] S. M. Choi, K. H. Lee, C. H. Lim, and W. S. Seo *Energy Conversion and Management*, vol. 52, no. 1, pp. 335–339, 2011.

[54] L. Han, Y. Jiang, S. Li, H. Su, X. Lan, K. Qin, T. Han, H. Zhong, L. Chen, and D. Yu, "High temperature thermoelectric properties and energy transfer devices of $Ca_3Co_{4x}Ag_xO_9$ and $Ca_{1y}Sm_yMnO_3$," *Journal of Alloys and Compounds*, vol. 509, pp. 8970–8977, 2011.

[55] J. G. Noudem, S. Lemonnier, M. Prevel, E. S. Reddy, E. Guilmeau, and C. Goupil, "Thermoelectric ceramics for generators," *Journal of the European Ceramic Society*, vol. 28, no. 1, pp. 41–48, 2008.

[56] W. Shin, N. Murayama, K. Ikeda, and S. Sago, "Thermoelectric power generation using Li-doped $NiO$ and $(Ba, Sr)PbO_3$ module," *Journal of Power Sources*, vol. 103, no. 1, pp. 80–85, 2001.

[57] M. Fedorov, "Thermoelectric silicides: past, present and future," *Journal of Thermoelectricity*, pp. 51–60, 2009.

[58] A. U. Khan, N. Vlachos, and T. Kyratsi, "High thermoelectric figure of merit of $Mg_2Si_{0.55}Sn_{0.4}Ge_{0.05}$ materials doped with Bi and Sb," *Scripta Materialia*, vol. 69, no. 8, pp. 606–609, 2013.

[59] Y. Sadia and Y. Gelbstein, "Silicon-rich higher manganese silicides for thermoelectric applications," *Journal of Electronic Materials*, vol. 41, no. 6, pp. 1504–1508, 2012.

[60] K. R. Tarantik, J. D. Konig, M. Jagle, J. Heuer, J. Horzella, A. Mahlke, M. Vergez, and K. Bartholome, "Thermoelectric modules based on silicides - development and characterization," *Materials Today: Proceedings*, vol. 2, no. 2, pp. 588–595, 2015.

[61] G. Skomedal, L. Holmgren, H. Middleton, I. S. Eremin, G. N. Isachenko, M. Jaegle, K. Tarantik, N. Vlachos, M. Manoli, T. Kyratsi, D. Berthebaud, N. Y. Dao Truong, and F. Gascoin, "Design, assembly and characterization of silicide-based thermoelectric modules," *Energy Conversion and Management*, vol. 110, pp. 13–21, 2016.

[62] R. Funahashi, Y. Matsumura, T. Barbier, T. Takeuchi, R. O. Suzuki, S. Katsuyama, A. Yamamoto, H. Takazawa, and E. Combe, "Durability of silicide-based thermoelectric modules at high temperatures in air," *Journal of Electronic Materials*, vol. 44, no. 8, pp. 2946–2952, 2015.

[63] L. D. Hicks, T. C. Harman, and M. S. Dresselhaus, "Use of quantum-well superlattices to obtain a high figure of merit from nonconventional thermoelectric materials," *Applied Physics Letters*, vol. 63, no. 23, pp. 3230–3232, 1993.

[64] L. D. Hicks and M. S. Dresselhaus, "Thermoelectric figure of merit of a one-dimensional conductor," *Phisical Review B*, vol. 47, no. 24, pp. 631–634, 1993.

[65] L. D. Hicks and M. S. Dresselhaus, "Effect of quantum-well structures on the thermoelectric figure of merit," *Phisical Review B*, vol. 47, no. 19, pp. 727–731, 1993.

[66] L. D. Hicks, T. C. Harman, X. Sun, and M. S. Dresselhaus, "Experimental study of the effect of quantum-well structures on the thermoelectric figure of merit," *Physical Review B (Condensed Matter)*, vol. 53, no. 16, pp. 10493–10496, 1996.

[67] J. P. Heremans, "Low-dimensional thermoelectricity," *Acta Physica Polonica A*, vol. 108, no. 4 PART 1, pp. 609–634, 2005.

[68] L. Ferre Llin, A. Samarelli, S. Cecchi, T. Etzelstorfer, E. Müller Gubler, D. Chrastina, G. Isella, J. Stangl, J. M. R. Weaver, P. S. Dobson, and D. J. Paul, "The cross-plane thermoelectric properties of $p - Ge/Si_{0.5}Ge_{0.5}$ superlattices," *Applied Physics Letters*, vol. 103, no. 14, 2013.

[69] T. C. Harman, P. J. Taylor, M. P. Walsh, and B. E. La Forge, "Quantum dot superlattice thermoelectric materials and devices," *Science*, vol. 297, no. September, pp. 2229–2232, 2002.

[70] R. Venkatasubramanian, E. Siivola, T. Colpitts, and B. O'Quinn, "Thin-film thermoelectric devices with high room-temperature figures of merit.," *Nature*, vol. 413, no. 6856, pp. 597–602, 2001.

[71] A. Hochbaum, R. Chen, and R. Delgado, "Enhanced thermoelectric performance of rough silicon nanowires," *Nature*, vol. 451, no. 7175, pp. 163–167, 2008.

[72] A. I. Boukai, Y. Bunimovich, J. Tahir-Kheli, J.-K. Yu, W. A. Goddard, and J. R. Heath, "Silicon nanowires as efficient thermoelectric materials," *Nature*, vol. 451, no. 7175, pp. 168–71, 2008.

[73] J. Tang, H. T. Wang, D. H. Lee, M. Fardy, Z. Huo, T. P. Russell, and P. Yang, "Holey silicon as an efficient thermoelectric material," *Nano Letters*, vol. 10, no. 10, pp. 4279–4283, 2010.

[74] http://www.europeanthermodynamics.com/. Accessed: 2017-04-09.

[75] http://micropelt.com/. Accessed: 2017-04-09.

[76] S. M. Yang, M. Cong, and T. Lee, "Application of quantum well-like thermocouple to thermoelectric energy harvester by BiCMOS process," *Sensors and Actuators, A: Physical*, vol. 166, no. 1, pp. 117–124, 2011.

[77] M. Strasser, R. Aigner, C. Lauterbach, T. F. Sturm, M. Franosh, and G. Wachutka, "Micromachined CMOS thermoelectric generators as on-chip power supply," *TRANSDUCERS 2003 - 12th International Conference on Solid-State Sensors, Actuators and Microsystems, Digest of Technical Papers*, vol. 1, pp. 45–48, 2003.

[78] S. Hasebe, J. Ogawa, M. Shiozaki, T. Toriyama, S. Sugiyama, H. Ueno, and K. Itoigawa, "Polymer based smart flexible thermopile for power generation," *17th IEEE International Conference on Micro Electro Mechanical Systems. Maastricht MEMS 2004 Technical Digest*, pp. 4–7, 2004.

[79] D. Rowe, D. Morgan, and J. Kiely, "Miniature low-power/high-voltage thermoelectric generator," *Electronics Letters*, vol. 25, no. 2, p. 166, 1989.

[80] M. Stordeur and I. Stark, "Low power thermoelectric generator - self-sufficient energy supply for micro systems," *16th International Conference on Thermoelectrics*, pp. 575–577, 1997.

[81] I. Stark and M. Stordeur, "New micro thermoelectric devices based on bismuth telluride-type thin solid films," *Thermoelectrics, 1999. Eighteenth International Conference on*, pp. 465–472, 1999.

[82] M. Kishi, Y. Yoshida, H. Okano, H. Nemoto, Y. Funanami, M. Yamamoto, and H. Kanazawa, "Fabrication of a miniature thermoelectric module with elements composed of sintered Bi-Te compounds," *XVI ICT '97. Proceedings ICT'97. 16th International Conference on Thermoelectrics (Cat. No.97TH8291)*, pp. 653–656, 1997.

[83] M. Kishi, H. Nemoto, T. Hamao, M. Yamamoto, S. Sudou, M. Mandai, and S. Yamamoto, "Micro thermoelectric modules and their application to wristwatches as an energy source," *Eighteenth International Conference on Thermoelectrics. Proceedings, ICT'99 (Cat. No.99TH8407)*, no. 1 999, pp. 301–307, 1999.

[84] H. Böttner, J. Nurnus, A. Gavrikov, G. Kühner, M. Jägle, C. Künzel, D. Eberhard, G. Plescher, A. Schubert, and K. H. Schlereth, "New thermoelectric components using microsystems technologies," *Journal of Microelectromechanical Systems*, vol. 13, no. 3, pp. 414–420, 2004.

[85] http://www.thermogentech.com/. Accessed: 2017-04-03.

[86] C. Boulanger, "Thermoelectric material electroplating: a historical review," *Journal of Electronic Materials*, vol. 39, no. 9, pp. 1818–1827, 2010.

[87] J. R. Lim, G. J. Snyder, C. K. Huang, J. A. Herman, R. Ma, and J. P. Fleurial, "Thermoelectric microdevice fabrication process and evaluation at the jet propulsion laboratory," *Ict*, pp. 535–539, 2002.

[88] W. Glatz, S. Muntwyler, and C. Hierold, "Optimization and fabrication of thick flexible polymer based micro thermoelectric generator," *Sensors and Actuators, A: Physical*, vol. 132, pp. 337–345, 2006.

[89] W. Glatz, E. Schwyter, L. Durrer, and C. Hierold, "$Bi_2Te_3$-based flexible micro thermoelectric generator with optimized design," *Journal of Microelectromechanical Systems*, vol. 18, no. 3, pp. 763–772, 2009.

[90] Z. Wang, V. Leonov, P. Fiorini, and C. Van Hoof, "Realization of a wearable miniaturized thermoelectric generator for human body applications," *Sensors and Actuators, A: Physical*, vol. 156, no. 1, pp. 95–102, 2009.

[91] A. Jacquot, W. Liq, G. Chen, J. Fleurial, A. Dausder, and B. Lenoir, "Fabrication and modeling of an in-plane thermoelectric mieregenerator," *21st International Conference on Thermoelectronics*, pp. 561–564, 2002.

[92] H. Glosch, M. Ashauer, U. Pfeiffer, and W. Lang, "Thermoelectric converter for energy supply," *Sensors and Actuators, A: Physical*, vol. 74, no. 1, pp. 246–250, 1999.

[93] T. Huesgen, P. Woias, and N. Kockmann, "Design and fabrication of MEMS thermoelectric generators with high temperature efficiency," *Sensors and Actuators, A: Physical*, vol. 145-146, no. 1-2, pp. 423–429, 2008.

[94] M. Strasser, R. Aigner, M. Franosch, and G. Wachutka, "Miniaturized thermoelectric generators based on poly-Si and poly-SiGe surface micromachining," *Sensors and Actuators, A: Physical*, vol. 97-98, pp. 535–542, 2002.

[95] I.-h. Kim and D.-h. Lee, "Thermoelectric Generator Cell of Bi-Sb-Te-Se System," *15th International Conference on Thermoelectrics*, no. 1 996, pp. 425–429, 1996.

[96] G. J. Snyder, J. R. Lim, C.-K. Huang, and J.-P. Fleurial, "Thermoelectric microdevice fabricated by a MEMS-like electrochemical process.," *Nature materials*, vol. 2, no. 8, pp. 528–531, 2003.

[97] T. C. Harman, R. E. Reeder, M. P. Walsh, B. E. Laforge, C. D. Hoyt, and G. W. Turner, "High electrical power density from PbTe-based quantum-dot superlattice unicouple thermoelectric devices," *Applied Physics Letters*, vol. 88, no. 24, 2006.

[98] V. Leonov, T. Torfs, C. Van Hoof, R. J. M. Vullers, and E. A. Board, "Smart wireless sensors integrated in clothing: an electrocardiography system in a shirt powered using human body heat," *Sensors & Transducers Journal*, vol. 107, no. 8, pp. 165–176, 2009.

[99] J. Xie, C. Lee, and H. Feng, "Design, fabrication, and characterization of CMOS MEMS-Based thermoelectric power generators," *Journal of Microelectromechanical Systems*, vol. 19, no. 2, pp. 317–324, 2010.

[100] P. H. Kao, P. J. Shih, C. L. Dai, and M. C. Liu, "Fabrication and characterization of CMOS-MEMS thermoelectric micro generators," *Sensors*, vol. 10, no. 2, 2010.

[101] J. Su, V. Leonov, M. Goedbloed, Y. van Andel, M. C. de Nooijer, R. Elfrink, Z. Wang, and R. J. M. Vullers, "A batch process micromachined thermoelectric energy harvester: fabrication and characterization," *Journal of Micromechanics and Microengineering*, vol. 20, no. 10, p. 104005, 2010.

[102] R. Ambrosi, H. Williams, P. Samara-ratna, K. Tomkins, R. Slade, N. Bannister, K. Stephenson, K. Simpson, I. Dimitriadou, M. Reece, H. Ning, K. Chen, J. Sykes, T. Rice, T. Tinsley, M. Sarsfield, D. Vernon, T. Crawford, M. Stuttard, J. Koenig, and M. Jaegle, "Americium-241 radioisotope thermoelectric generator development for space applications," *2013 International Nuclear Atlantic Conference - INAC 2013*, 2013.

[103] F. Suarez, A. Nozariasbmarz, D. Vashaee, and M. C. Öztürk, "Designing thermoelectric generators for self-powered wearable electronics," *Energy Environ. Sci.*, vol. 9, no. 6, pp. 2099–2113, 2016.

[104] J. P. Dismukes, R. J. paff, R. T. Smith and R. Ulmer, "Lattice parameter and density in germanium-silicon alloys," *The Journal of Physical Chemistry*, vol. 68, no. 10, pp. 3021–3027, 1964.

[105] M. C. Steele and F. D. Rosi, "Thermal conductivity and thermoelectric power of germanium-silicon alloys," *Journal of Applied Physics*, vol. 29, no. 11, pp. 1517–1520, 1958.

[106] J. P. Dismukes, L. Ekstrom, E. F. Steigmeier, I. Kudman, and D. S. Beers, "Thermal and electrical properties of heavily doped Ge-Si alloys up to 1300K," *Journal of Applied Physics*, vol. 35, no. 10, pp. 2899–2907, 1964.

[107] C. B. Vining, W. Laskow, J. O. Hanson, R. R. Van Der Beck, and P. D. Gorsuch, "Thermoelectric properties of pressure-sintered $Si_{0.8}Ge_{0.2}$ thermoelectric alloys," *Journal of Applied Physics*, vol. 69, no. 8, pp. 4333–4340, 1991.

[108] C. J. Glassbrenner and G. A. Slack, "Thermal conductivity of silicon and germanium from 3K to the melting point," *Phys. Rev.*, vol. 134, pp. 1058–1069, 1964.

[109] http://www.asm.com/solutions/products/epitaxy-products/epsilon-epitaxy. Accessed: 2017-05-23.

[110] D. Schroder, *Semiconductor Material and Device Characterization*. A. Jhon Wiley and Sons, 2006.

[111] H. H. Berger, "Contact resistance and contact resistivity," *Journal of The Electrochemical Society*, vol. 119, no. 4, p. 507, 1972.

[112] J. Klootwijk and C. Timmering, "Merits and limitations of circular TLM structures for contact resistance determination for novel III-V HBTs," *Proceedings of the 2004 International Conference on Microelectronic Test Structures (IEEE Cat. No.04CH37516)*, vol. 17, pp. 8–13, 2004.

[113] K. Gallacher, P. Velha, D. J. Paul, I. MacLaren, M. Myronov, and D. R. Leadley, "Ohmic contacts to n-type germanium with low specific contact resistivity," *Applied Physics Letters*, vol. 100, no. 2, 2012.

[114] A. Lauwers, M. J. H. van Dal, P. Verheyen, O. Chamirian, C. Demeurisse, S. Mertens, C. Vrancken, K. Verheyden, K. Funk, and J. A. Kittl, "Study of silicide contacts to SiGe source/drain," *Microelectronic Engineering*, vol. 83, no. 11-12, pp. 2268–2271, 2006.

[115] J. Gambino and E. Colgan, "Silicides and ohmic contacts," *Materials Chemistry and Physics*, vol. 52, no. 2, pp. 99–146, 1998.

[116] R. W. Mann, L. a. Clevenger, P. D. Agnello, and F. R. White, "Silicides and local interconnections for high-performance VLSI applications," *IBM Journal of Research and Development*, vol. 39, no. 4, pp. 403–417, 1995.

[117] J. A. Cape and G. W. Lehman, "Temperature and finite pulse-time effects in the flash method for measuring thermal diffusivity," *Journal of Applied Physics*, vol. 34, no. 7, pp. 1909–1913, 1963.

[118] T. Borca-Tasciuc, A. R. Kumar, and G. Chen, "Data reduction in 3w method for thin-film thermal conductivity determination," *Review of Scientific Instruments*, vol. 72, no. 4, pp. 2139–2147, 2001.

[119] C. C. Williams and H. K. Wickramasinghe, "Scanning thermal profiler," *Microelectronic Engineering*, vol. 5, no. 1-4, pp. 509–513, 1986.

[120] D. G. Cahill, "Analysis of heat flow in layered structures for time-domain thermoreflectance," *Review of Scientific Instruments*, vol. 75, no. 12, pp. 5119–5122, 2004.

[121] C. V. Raman and K. S. Krishnan, "A New Type of Secondary Radiation," *Nature*, vol. 121, no. 3048, pp. 501–502, 1928.

[122] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, "Superior thermal conductivity of single-layer graphene," *Nano Letters*, vol. 8, no. 3, pp. 902–907, 2008.

[123] A. A. Balandin, "Thermal properties of graphene and nanostructured carbon materials," *Nature Materials*, vol. 10, no. 8, pp. 569–581, 2011.

[124] W. Cai, A. L. Moore, Y. Zhu, X. Li, S. Chen, L. Shi, and R. S. Ruoff, "Thermal transport in suspended and supported monolayer graphene grown by chemical vapor deposition," *Nano Letters*, vol. 10, no. 5, pp. 1645–1651, 2010.

[125] J. U. Lee, D. Yoon, H. Kim, S. W. Lee, and H. Cheong, "Thermal conductivity of suspended pristine graphene measured by Raman spectroscopy," *Physical Review B - Condensed Matter and Materials Physics*, vol. 83, no. 8, pp. 1–4, 2011.

[126] B. Stoib, S. Filser, N. Petermann, H. Wiggers, M. Stutzmann, and M. S. Brandt, "Thermal conductivity of mesoporous films measured by Raman spectroscopy," *Applied Physics Letters*, vol. 104, no. 16, pp. 1–5, 2014.

[127] X. Liu, X. Wu, and T. Ren, "In situ and noncontact measurement of silicon membrane thermal conductivity," *Applied Physics Letters*, vol. 98, no. 17, pp. 1–4, 2011.

[128] T. Beechem, A. Christensen, S. Graham, and D. Green, "Micro-Raman thermometry in the presence of complex stresses in GaN devices," *Journal of Applied Physics*, vol. 103, no. 12, 2008.

[129] T. Beechem, L. Yates, and S. Graham, "Invited review article: Error and uncertainty in Raman thermal conductivity measurements," *Review of Scientific Instruments*, vol. 86, no. 4, 2015.

[130] T. Beechem and J. Serrano, "Raman thermometry of microdevices: comparing methods to minimize error," *Spectroscopy*, vol. 26, no. 11, 2011.

[131] H. D. Fuchs, C. H. Grein, R. I. Devlen, J. Kuhl, and M. Cardona, "Anharmonic decay time, isotopic scattering time, and inhomogeneous line broadening of optical phonons in $^{70}$Ge, $^{76}$Ge, and natural Ge crystals," *Physical Review B*, vol. 44, no. 16, pp. 8633–8642, 1991.

[132] H. Burke and I. Herman, "Temperature dependence of Raman Scattering in GeSi alloys," *Physical Review B*, vol. 48, no. 20, p. 15016, 1993.

[133] D. M. Rowe and G. Min, "Evaluation of thermoelectric modules for power generation," *Journal of Power Sources*, vol. 73, no. Copyright 1998, IEE, pp. 193–198, 1998.

[134] S. Lineykin and S. Ben-Yaakov, "Modeling and analysis of thermoelectric modules," *IEEE Transactions on Industry Applications*, vol. 43, no. 2, pp. 505–512, 2007.

[135] R. McCarty, "Thermoelectric power generator design for maximum power: it's all about zt," *Journal of Electronic Materials*, vol. 42, pp. 1504–1508, 2013.

[136] K. Yazawa and A. Shakouri, "Cost-efficiency trade-off and the design of thermoelectric power generators," *Environmental Science and Technology*, vol. 45, no. 17, pp. 7548–7553, 2011.

[137] Y. Wang, C. Dai, and S. Wang, "Theoretical analysis of a thermoelectric generator using exhaust gas of vehicles as heat source," *Applied Energy*, vol. 112, pp. 1171–1180, 2013.

[138] A. Montecucco, J. Siviter, and A. R. Knox, "Constant heat characterisation and geometrical optimisation of thermoelectric generators," *Applied Energy*, vol. 149, pp. 248–258, 2015.

[139] A. Rezania, L. A. Rosendahl, and H. Yin, "Parametric optimization of thermoelectric elements footprint for maximum power generation," *Journal of Power Sources*, vol. 255, pp. 151–156, 2014.

[140] H. Lee, "Optimal design of thermoelectric devices with dimensional analysis," *Applied Energy*, vol. 106, pp. 79–88, 2013.

[141] J. Y. Jang and Y. C. Tsai, "Optimization of thermoelectric generator module spacing and spreader thickness used in a waste heat recovery system," *Applied Thermal Engineering*, vol. 51, no. 1-2, pp. 677–689, 2013.

[142] C. Favarel, J. P. Bédécarrats, T. Kousksou, and D. Champier, "Numerical optimization of the occupancy rate of thermoelectric generators to produce the highest electrical power," *Energy*, vol. 68, pp. 104–116, 2014.

[143] A. Delan, M. Rennau, S. E. Schulz, and T. Gessner, "Thermal conductivity of ultra low-k dielectrics," *Microelectronic Engineering*, vol. 70, no. 2-4, pp. 280–284, 2003.

[144] https://www.engineeringtoolbox.com/air-properties-d_156.html. Accessed: 2017-10-28.

[145] K. Ronse, P. Jansen, R. Gronheid, E. Hendrickx, M. Maenhoudt, V. Wiaux, A. M. Goethals, R. Jonckheere, and G. Vandenberghe, "Lithography options for the 32 nm half pitch node and beyond," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 8, pp. 1884–1891, 2009.

[146] https://www.suss.com/en/products-solutions/mask-aligner/ma-ba-6. Accessed: 2017-08-18.

[147] http://microchemicals.com/micro/az-4500-series.pdf. Accessed: 2017-08-18.

[148] http://www.microchemicals.com/micro/az-nLof-20xx-additional-informations.pdf. Accessed: 2017-08-18.

[149] http://www.oxfordplasma.de/systems/80plus.htm. Accessed: 2017-08-18.

[150] http://www.spts.com/Products/Plasma-Etch/ICP-Etch. Accessed: 2017-08-18.

[151] https://www.oxford-instruments.com/products/etching-deposition-and-growth/plasma-etch-deposition/pecvd. Accessed: 2017-08-18.

[152] https://plassys.com/. Accessed: 2017-08-18.

[153] http://www.jwnc.gla.ac.uk/metal.htmlp. Accessed: 2017-08-18.

[154] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, 1965.

[155] http://www.semicorp.com/products/flip-chip-bonders/item/model-850-flip-chip-placement-system. Accessed: 2017-08-23.

[156] https://www.inseto.co.uk/microelectronic-equipment-mpp-iBond-5000-ball-bonder.php. Accessed: 2017-08-26.

[157] A. N. Campbell, R. Wagemann, and R. B. Ferguson, "The silver-indium system: thermal analysis, photomicrography, electron microprobe, and X-ray powder diffraction results," *Canadian Journal of Chemistry*, vol. 48, pp. 1703–1715, 1970.

[158] https://www.warton-metals.co.uk/re-work.html. Accessed: 2017-08-30.

[159] A. Singh, D. A. Horsley, M. B. Cohn, A. P. Pisano, and R. T. Howe, "Batch transfer of microstructures using flip-chip solder bonding," *Journal of Microelectromechanical Systems*, vol. 8, no. 1, pp. 27–32, 1999.