Fu, Yen-Chun (2018) *Realisation of III-V Tunnel-FET with in-situ ultimate scaled gate stack for high performance power efficient CMOS*. PhD thesis.

https://theses.gla.ac.uk/30588/

Copyright and moral rights for this work are retained by the author

A copy can be downloaded for personal non-commercial research or study, without prior permission or charge

This work cannot be reproduced or quoted extensively from without first obtaining permission in writing from the author

The content must not be changed in any way or sold commercially in any format or medium without the formal permission of the author

When referring to this work, full bibliographic details including the author, title, awarding institution and date of the thesis must be given

Enlighten: Theses
https://theses.gla.ac.uk/
research-enlighten@glasgow.ac.uk

Realisation of III-V Tunnel-FET with in-situ ultimate scaled gate stack for high performance power efficient CMOS

By

Yen-Chun Fu

September 2017

A thesis submitted for the degree of

Doctor of Philosophy

to the

Department of Electronics and Electrical Engineering

School of Engineering

University of Glasgow

© Yen-Chun Fu 2017

All Rights Reserved

This thesis is dedicated to my parents, wife and parents in law.

Abstract

The main objective of this thesis is realising a non-planar III-V Tunnel-FET for low power device applications. The differentiating aspect of this work is based around clustered inductively coupled plasma (ICP) etch and atomic layer deposition (ALD) tools. This approach was intended to mitigate native oxide formation on etched III-V surfaces prior to gate stack deposition by ALD. The use of a cluster tool also offers the benefit of cleaning III-V surfaces "in-situ" using low damage plasma based approaches. In addition, activity on scaling the equivalent oxide thickness of the gate stack and evaluating different heterostructures are explored in this work for the realisation of high performance Tunnel-FET.

Initially, gate stacks on both p- and n- (110)-oriented $In_{0.53}Ga_{0.47}As$ were examined to understand the basic electrical properties of these interfaces, important for non-planar device architectures. An optimised process, based on ex-situ sulphur-based passivation before ALD of gate dielectrics, and forming gas annealing (FGA) after gate metal deposition, is demonstrated for the first time to show significant Fermi level movement through the bandgap. Quantitatively, interface state density (D_{it}) values in the range of 0.87-1.8 × 10^{12} $cm^{-2}eV^{-1}$ around the midgap energy level were obtained. The lowest D_{it} value is estimated to be 3.1 × 10^{12} $cm^{-2}eV^{-1}$ close to the conduction band edge showing the combination of sulphur passivation and (FGA) is effective is passivating the trap states in the upper half of the bandgap on $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) MOSCAPs. Furthermore, by analysis of CV hysteresis biasing at 1.1 V beyond the flatband voltage, the border trap density on n-type MOSCAPs was observed to reduce, after FGA from 1.8 × 10^{12} cm^{-2} to 5.3 × 10^{11} cm^{-2}. The result observed in p-type MOSCAPs is in contrast, with increasing border trap density from 7.3 × 10^{11} cm^{-2} to 1.4 × 10^{12} cm^{-2} under the similar bias condition, i.e. the FGA process is not as effective in passivating states close to the valence band. In addition, the analysis undertaken in this thesis determined the value of the conduction band offset at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) to be is 1.81eV – the first report of this parameter.

The non-planar devices of this work also require low damage etching processes for fin/wire formation. Therefore, the performance of in-situ deposited gate stacks to $In_{0.53}Ga_{0.47}As$ (100)- and (110)-oriented substrates which had been subjected to a $CH_4/Cl_2/H_2$ based ICP etch chemistry, which forms vertical InGaAs sidewall profiles, were assessed. Based on CV and IV, and X-ray Photo-Spectroscopy (XPS) spectral

analyses, the performance of gate stacks deposited on (110)-oriented $In_{0.53}Ga_{0.47}As$ subjected to a ICP dry etch suffers more damage compared to gate stacks on (100)-oriented $In_{0.53}Ga_{0.47}As$. To minimise the etching damage, cyclic TMA/plasma gas pre-treatment prior to ALD is introduced on both (100)- and (110)-oriented surfaces. The interface trap density of gate stacks on (110)-oriented $In_{0.53}Ga_{0.47}As$ with TMA/H_2 gas pre-treatment improves from 6×10^{11} $cm^{-2}eV^{-1}$ to 2.8×10^{11} $cm^{-2}eV^{-1}$ close to the conduction band edge.

Based on this in-situ gate stack process, a gate stack with reduced capacitor equivalent thickness (CET) on both (100) and (110) oriented surfaces are achieved by using a TiN layer deposited in-situ by ALD before ex-situ gate metal deposition. The lowest CET was around 1.09 nm for a HfO_2/TiN stack deposited on (100)-oriented $In_{0.53}Ga_{0.47}As$.

This optimised gate stack was included in an InGaAs-based tunnel-FET process flow using p-n, p-i-n, and p-n-i-n heterostructures. Comparing with p-n Tunnel-FETs, the p-i-n structure provides better electrical characteristics for $In_{0.53}Ga_{0.47}As$ with a subthreshold swing (SS) of 120 mV/dec at the condition of V_{DS} = 0.05V. The peak transconductance peak of the p-i-n Tunnel-FET at the condition of V_{DS} = 0.3V is around 6 $\mu S/\mu m$. Next, an inserted n-pocket p-n-i-n Tunnel-FET was studied. In addition to providing comparable on current with the p-i-n Tunnel-FET of 1.1 μA/μm at the bias condition of V_{DS} = 300mV, the subthreshold swing of the p-n-i-n devices improves by 46% due to the lower leakage floor from the n-pocket layer incorporation. Most importantly, the non-planar configuration of the p-n-i-n Tunnel-FET improves both the SS and on-current to 152 mV/dec at the bias condition of V_{DS} = 300mV and 1.3 μA/μm at the bias condition of V_{DS} = 500mV and V_{GS} = 900mV, respectively. Above these aspects and benchmark, all this data implies that a non-planar p-n-i-n InGaAs Tunnel-FET is a promising candidate for future generations of low power applications.

Acknowledgement

First of all, I would like to express the deepest appreciation to my supervisor Professor Iain Thayne for giving me the opportunity to work on this project and thoroughly supporting me when various issues emerged during my PhD. Thank you, Iain for your priceless mentoring and insightful guidance when needed, and also allowing me to explore my own research path and gain from failures; This not only built up my confidence but also made this PhD journey enjoyful. Many thanks to my second supervisor Professor Douglas Paul for sharing me his knowledge of nanowire device fabrication.

I would also like to thank my PhD examiners, Dr. Karim Cherkaoui, of University College Cork, and Professor Scott Roy, of University of Glasgow for providing me valuable feedbacks during the viva. Thanks to my convener, Dr. Anthony Kelly, of University of Glasgow for the encouragement and psychological comfort.

Special thanks to Dr. Xu Li and Dr. Haiping Zhou for their invaluable support in all my endeavors and constructive advisory in aspects of nanofabrication. The discussion that we have ever had about both work and life in Glasgow always inspires me and drives me to move forward bravely.

I am much indebted to Dr. Uthayasankaran Peralagu for kindly sharing his research experiences and knowledge in nanofabrication. As one of my good friends, his feedbacks always lead me to the correct path. He is one of the greatest people I have known in Glasgow. Many thanks to the present and former members of the III-V MOSFET team at University of Glasgow for their transfer of knowledge and share of practical experience in device fabrication and characterisation. The following people who have ever helped me deserve special mention. I would also like to thank one of my most respectful colleagues, David Millar for his expertise in simulations. Many thanks to Dr. Sam McFadzean for performing TEM image and EELS analysis. Dr. Matthew Steer deserves thanks for growing high-quality InGaAs epi-layers and suggesting the appropriate design of multi-layer structures to avoid causing the issues from layer relaxation. Particular thank to Dr. Muhammad Mirza for sharing his expertise on nanoscale patterning by using his HSQ process, advising me in detail about the process flow of my device fabrication and assisting me to use Cyro probe station for low temperature measurements. All the

technical staff members of James Watt Nanofabrication Centre (JWNC) deserve thanks for their technical support of facilities, especially to Helen McLelland, Susan Ferguson, Dougie Lang, Rachel Love and Thomas Relly for their assistance with fabrication.

In addition, I would like to thank all my external collaborators. Special thanks to Dr. Paul Hurley, Iain Povey and Jun Lin, of Tyndall National Institute, for offering the growth of dielectric layer by ALD tool, temperature dependent measurements and the discussion of the Journal paper. I would also like to thank Professor Ravi Droopad, of Texas State University, for growing high quality p-type & n-type (110)-oriented InGaAs epi-layers. Many thanks to Dr. Ivona Mitrovis and Siti Nurbaya Supardan, of University of Liverpool, for providing XPS analysis.

I would like specially to thank all of my good friends at Glasgow, Dr. Lourdes Ferre Llin, Dr. Boon Chong Cheah and Dr. Chengzhi, Xie for being supportive for both work and life and their kindly help for thesis proofreading.

Finally, I would like to thank my wife, Ning-Chih Chang, for her endless dedication to make my dream come true. You always light up my world when passing through the dark. Thank you being here with me from the beginning to the end of this long journey. Heartfelt thanks my father and mother in law for being supportive when I start pursing this degree. I deeply thank my parents and all my family members for your unconditional love and care in my life which motivates me to achieve my goal in the world. Thank you all!

Associated Publication

- **Fu, Y.-C.**, Peralagu, U., Lin, J., Povey, I., Millar, D. A.J., Monaghan, S., Droopad, R., Hurley, P. K. and Thayne, I. G. (2017) The impact of forming gas annealing on the electrical characteristics of sulfur passivated $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) metal-oxide-semiconductor capacitors. Applied Physics Letters, 110(14), 142905.
- Li, X., **Fu, Y.-C.**, Millar, D.A.J., Peralagu, U., Steer, M. and Thayne, I.G. (2016) The Impact of an HBr/Ar Atomic Layer Etch (ALE) Process for InGaAs Vertical Nanowire Diameter Reduction on the Interface Between InGaAs and In-situ ALD Deposited HfO_2. In: 47th IEEE Semiconductor Interface Specialists Conference (SISC 2016), San Diego, CA, USA, 8-10 Dec 2016.
- **Fu, Y.-C.**, Peralagu, U., Li, X., Millar, D. A. J., Steer, M., Zhou, H., Droopad, R. and Thayne, I. (2015) First Demonstration of Cluster Tool Based ICP Etching of (100) and (110) InGaAs MOSCAPs Followed by In-Situ ALD Deposition of HfO_2 Including Nitrogen and Hydrogen Plasma Passivation for Non-Planar III-V MOSFETs. In: 46th IEEE Semiconductor Interface Specialists Conference (SISC 2015), Arlington, VA, USA, 2-5 Dec 2015.
- **Fu, Y.-C.**, Peralagu, U., Ignatova, O., Li, X., Droopad, R., Thayne, I., Lin, J., Povey, I., Monaghan, S. and Hurley, P. (2015) Energy-Band Structure of Atomic Layer Deposited Al_2O_3 & Sulphur Passivated Molecular Beam Epitaxially Grown (110) $In_{0.53}Ga_{0.47}As$ Surfaces. In: 11th Conference on PhD Research in Microelectronics and Electronics (IEEE PRIME 2015), Glasgow, UK, 29 June - 2 July 2015.
- **Fu, Y.-C.**, Peralagu, U., Lin, J., Povey, I., Li, X., Ignatova, O., Monaghan, S., Droopad, R., Hurley, P. and Thayne, I. (2014) The impact of forming gas annealing on the properties of interfaces between atomic layer deposited Al_2O_3 and sulphur passivated molecular beam epitaxially grown (110) p- and n-type $In_{0.53}Ga_{0.47}As$ surfaces. In: 18th Workshop on Dielectrics in Microelectronics (WoDIM), Kinsale, Co Cork, Ireland, 9-11 Jun 2014.

Contents

Abstract 1
Acknowledgement 3
Associated Publication 5
List of tables 10
List of diagrams 11
I. Introduction 16
1.1 Background 16
1.2 The power dissipation issue in CMOS switching devices 17
1.3 The key challenges of alternatives 18
1.4 Scope of proposed solutions 18
1.5 Thesis outline 18
1.6 Reference 19
II. Background Theory 21
2.1 Introduction 21
2.2 Band-to-Band Tunneling Field Effect Transistors 21
2.3. Basic operation 22
2.4. Tunnel-FET characteristics 24
2.4.1. Subthreshold swing 24
2.4.2. On-current 25
2.4.3. Threshold voltage 25
2.4.4. Off-current 26
2.5. Metal-Oxide-Semiconductor capacitors 27
2.5.1. Physics 27
2.5.2. Capacitor-Voltage characteristics 30
2.5.3. Charge traps 32
2.5.3.1. Interface traps 33
2.5.3.2. Oxide defects 34
2.5.4. High-κ 36
2.5.5. Finite DOS and charge quantisation 36
2.6. Channel properties 37
2.6.1. III-V materials 38
2.6.2. Material orientation 40
2.6.3. Band-to-band tunneling mechanism 40

2.6.3.1 BTBT generation rate 40
2.6.3.2 Tunneling probability 41
2.7 Esaki diodes 43
2.8. Metal-semiconductor contacts 44
2.9. Chapter summary 45
2.10. Reference 45
III. Fabrication Techniques 49
3.1. Introduction 49
3.2. Material growth 49
3.3. Cluster tool 50
3.3.1. Atomic Layer Deposition (ALD) 51
3.3.2. ICP dry etch 54
3.4 Electron beam lithography 55
3.4.1. Apparatus and operation of e-beam lithography tool 56
3.4.2. Scattering 58
3.4.3. The proximity effect 60
3.4.4. Resist 61
3.4.5. Alignment 62
3.5. Metallisation and lift-off 62
3.6. Chapter summary 63
3.7. Reference 63
IV. Overview of Tunnel-FETs 66
4.1 Tunnel-FETs technology to date 66
4.2 Figure of merit for Tunnel-FET development 67
4.3 Introduction of Tunnel-FET configuration 68
4.4 Potential issue of experimental III-V Tunnel-FETs 69
4.5 Homojunction and Heterojunction modulation 69
4.6 Chapter summary 70
4.7 Reference 70
V. Process Development & Characterisation Metrology 73
5.1 Introduction 73
5.2 Clustering ICP etching and in-situ ALD process of MOSCAPs 73
5.2.1 Plasma H_2 or plasma N_2 passivation 74
5.3 Device fabrication 75
5.3.1 Progress of planar Tunnel-FETs 75

5.3.1.1 Process flow 76

5.3.1.2 Single gate vs. double gate 77

5.3.2 Progress of vertical nanowire Tunnel-FET 79

5.3.2.1 Top-down InGaAs nanowire formation 81

5.3.2.2 Bottom spacer 82

5.3.2.3 Gate metal definition and ohmic contact 83

5.3.2.4 Top spacer and source electrode 84

5.4 Characterisation 86

5.4.1 MOSCAP device characterisation 86

5.4.1.1 Flatband Voltage 87

5.4.1.2 Surface potential 87

5.4.1.3 Interface defect density 89

5.4.1.4 Hysteresis 90

5.4.2 TFET characterisation 91

5.4.2.1 DC characterisation 91

5.5 Contact characterisation 92

5.6. Chapter summary 94

5.7. Reference 95

VI. Interface Engineering of $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) MOSCAPs 98

6.1 Introduction 98

6.2 Surface Morphology 99

6.3 Experimental Details 99

6.4 Result and Discussion 100

6.4.1 The impact of Forming Gas Annealing 100

6.4.1.1 Qualitative analysis 100

6.4.1.2 Genuine inversion 101

6.4.1.3 C_{ox} extraction 102

6.4.1.4 Interface trap density 103

6.4.1.5 Border traps 105

6.4.2 Band parameters of $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) MOSCAPs 108

6.4.2.1 Gate Leakage 108

6.4.2.2 Energy band parameters 109

6.5 Chapter summary 110

6.6 Reference 111

VII. Enhanced scalability of gate stack on less-damaged $In_{0.53}Ga_{0.47}As$ (110) epi-layers 114

7.1 Introduction 114

7.2 Damage elimination on $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs 115

7.2.1 Function of plasma gas pre-treatment 115

7.2.2 C-V characteristics 115

7.2.3 G-V characteristics 117

7.2.4 Interfacial layers 121

7.2.5 Material analysis 122

7.3 Realisation of sub-1nm EOT $In_{0.53}Ga_{0.47}As$ (100) and (110) MOSCAPs 126

7.3.1 EOT scaling with TiN capping layer insertion 127

7.3.2 Analysis of EOT scalability on $In_{0.53}Ga_{0.47}As$ (100) and (110) MOSCAPs 130

7.4 Chapter summary 130

7.5 Reference 131

VIII. Heterojunction Tunnel-FET 133

8.1 Performance of p-n and p-i-n Tunnel-FETs 133

8.2 Optimisation of heterojunction Tunnel-FETs 136

8.3 Chapter summary 143

8.4 Reference 144

IX. Conclusion and Future work 145

9.1 Reference 147

Appendix A: 148

List of tables

Table.1.1 Dennard's scaling rules for device and circuit of a given size, where k is the scaling parameter. [1.3]……………………………..……………………………………….……..….14

Table.2.1. The material properties of Group IV and III-V for Tunnel-FET applications [2.34] ……………………………………………………………………………………………36

Table 4.1 Benchmarking of Tunnel-FETs fabricated of III-V in planar and vertical geometry…68

Table 7.1. Sample name and description…………………………………………………….123

Table 7.2. A 3d comparison of blanket InGaAs (100) and (110) samples and HfO_2/InGaAs (100) and (110) samples with and without FGA…………………………………………………..124

Table 7.3. Ga 2p comparison of blanket InGaAs (100) and (110) samples…………………..…….124

Table 7.4. Ratio of Ga oxide to the elemental Ga on blanket InGaAs (100) and (110) samples…………………………………………………………………………………..…..124

Table. 7.5. The experimental details of scaled $In_{0.53}Ga_{0.47}As$ (100) & (110) MOSCAPs……….125

List of diagrams

Fig. 1.1. The trends of (a) static power density and dynamic power density with gate length scaling [1.8] and (b) the supply voltage with the technology node scaling [1.6] ………………….....……15

Fig. 2.1. Schematic diagram of (a) n-chnnel MOSFET and (b) n-channel Tunnel-FET cross-section……………………………………………………………………………………..20

Fig. 2.2. A typical MOSFET's (black curve) and Tunnel-FET's (blue curve) (a) transfer characteristics in log-current scale, which can be divided into off-state, sub-threshold region and saturation region and (b) output characteristics. The operation mechanism of MOSFET and Tunnel-FET in each region is introduced. ……………………………………………….......21

Fig. 2.3. Equivalent circuit model of a MOS capacitor on a n-type MOSFET……....……..…...23

Fig. 2.4. (a) Schematic diagram of a metal-oxide-semiconductor (MOS) capacitor and (b) the energy band diagram of a MOS capacitor at thermal equilibrium ($V_g = 0$)……………..…..…...25

Fig. 2.5. Energy band diagram and the charge stats of a p-type MOS capacitor in (a) accumulation, (b) depletion and (c) inversion……………………………………………………………….….28

Fig. 2.6. Capacitor-Voltage characteristics of an ideal p-type MOS capacitor………...…...……29

Fig. 2.7. Schematic diagram of the charge defects associated with a MOS capacitor…........…...30

Fig. 2.8. Schematic band diagram of distributed interface traps on a MOS capacitor. For donor-like interface traps, the occupancy of interface traps shows positive interface charge or neutral interface charge when the states are empty or filled, respectively. The acceptor interface charge is neutral when there are no filled states above the Fermi level but it becomes negative when band bending results in the filled states of acceptor-like interface traps………………...………...…...32

Fig. 2.9. Schematic band diagram of border traps and fixed oxide charges on a MOS capacitor.. 33

Fig. 2.10. The possible issue of a MOS capacitor from oxide defects: (a) frequency dispersion in accumulation and (b) hysteresis observed from forward and backward C-V sweeps due to border traps. In addition, (c) negative or positive C-V shifting caused by border traps, bulk traps and fixed oxide charges……………………………………………………………………...…34

Fig. 2.11. Schematic diagram of zinc blende lattice…………………………………………….37

Fig. 2.12. Band structure of InGaAs; Eg = 0.74 ($In_{0.53}Ga_{0.47}As$) [2.38]; lower effective mass and higher effective mass are in the direction of Γ valley and L valley, respectively [2.16] ……….37

Fig. 2.13. Schematic diagram of parabolic potential barrier with transverse energy components E_T [2.16]……………………………………………………………………………………...…39

Fig. 2.14. Current-voltage characteristics of the Esaki tunneling diode (ETD) corresponding to the operation under condition of (a) equilibrium, (b) peak tunneling current and (c) diffusion current……………………….………………………………………………………...…...41

Fig. 2.15. Schematic diagram of equivalent circuit on a three-terminal device associated with source and drain series resistances……………………………………………...……………42

Fig.3.1. Plot of the energy gap vs. lattice constant for InGaAsP family [3.1] ……………………47

Fig.3.2. Relationship of the calculated critical thickness vs. strain of an InGaAs layer grown on an InP substrate [3-5] …………………………………………………………………...…........48

Fig. 3.3. Cluster tool……………………………………………………………….……….......…..49

Fig 3.4. Schematic diagram of an ALD process window (blue line) in which the growth rate is situated [3.11] …………………………………………………………….....………….......50

Fig. 3.5. The schematic diagram of an ALD growth cycle of HfO_2 deposition via the sequential reactions of precursor TEMAH and H_2O on an OH-terminated substrate surface……………….51

Fig. 3.6. Schematic diagram of a reactive ion etching (RIE) tool……………………...……....52

Fig. 3.7. The evolution of lithography tool resolution with the scaled wavelength of the light source [3.15] ……………………………………………………………………………...….54

Fig. 3.8. Schematic diagram of the Vistec VB6 UHR EWF e-beam lithography system [3.16] …………………………………………………………………………………………55

Fig. 3.9. The stepping of the beam spot, which is equal to the product of the VRU and the resolution for pattern writing…………………………………………………………………56

Fig. 3.10. Schematic diagram of the total Gaussian energy distribution, known as the point spread function (PSF), compared to contributions from both forward scattering and back scattering……………………………………………………………………………………...57

Fig. 3.11. Schematic diagram of (a) pattern distortion due to proximity effect and due to (b) the accumulated electron dose…………………………………………………………………58

Fig. 3.12. Schematic diagram of the global and cell markers for alignment……..…………….60

Fig. 3.13. The general metal lift-off process with pattern exposure/development, metallisation and lift-off activities……………………………………………………………..…………..61

Fig. 4.1. The Tunnel-FET configuration of (a) point Tunnel-FET, (b) line Tunnel-FET, (c) pocketed point Tunnel-FET and (d) pocketed line Tunnel-FET based on different gate position and doped regions……………………………………………………………………………66

Fig. 5.1. (a) Clustering ICP etch and ALD deposition of in-situ MOSCAP fabrication and (b) the schematic diagram of gate stack formation on (100) and (110) orientation of etched InGaAs surfaces………………………………………………………………………………………72

Fig. 5.2. The schematic diagram of gate stack formation with plasma gas pre-treatment on (100) and (110) orientation of etched InGaAs surfaces………………………………………………73

Fig. 5.3. Schematic diagram of planar Tunnel-FETs with the InGaAs based p-i-n heterojunction. The dotted line shows the current flow from drain to source side. ……………………………..74

Fig. 5.4. Process flow of planar Tunnel-FET………………...……………………..………74

Fig. 5.5. Schematic diagram of (a) double gate Tunnel-FET and (b) single gate Tunnel-FET with a side view……………………………………………………..…………………………….….75

Fig. 5.6. SEM inspection of etching profile with in-situ ALD deposition on (a) single gate and (b) double gate devices, (c) the gate metal covering the whole etched channel on the sidewall and (d) the drain pad patterning……………………………………………………….............……76

Fig. 5.7. The schematic diagram of the nanowire process flow for Tunnel-FET…………...….77

Fig. 5.8. The etching profile of nanowires with (a) (110)-oriented and (b) (100)-oriented surfaces…………………………………………………………………………..…………...79

Fig. 5.9. SEM inspection of nanowire etching profile with the shape of cross section including square, triangle, diamond and circle………………………………………………………….....80

Fig. 5.10. The spacer coverage from the material of (a) HSQ and (b) SiN layer……………...…..81

Fig. 5.11. The SEM inspection of (a) the nanowire without a HSQ spacer coverage, (b) with a HSQ layer coverage and (c) the removal of TiN metal and dielectric layer on the both top side of nanowire and the bottom side which is not covered by spacer……………………..…………….82

Fig. 5.12. The SEM inspection of forming ohmic pad for drain contact…………….…...………82

Fig. 5.13. The SEM inspection of (a) top HSQ spacer formation and (b) etching back to expose the top of nanowire for metal connection………………………………………..…..……..83

Fig. 5.14. The SEM inspection of the final device layout………………………..……..……..84

Fig. 5.15. Transfer characteristics of a generic Tunnel-FET showing the parameters of subthreshold swing (SS), threshold voltage (V_T) and transconductance peak ($g_{m,\ peak}$) in (a) and On-off ratio in (b)…………………………………………………………………….……………………90

Fig. 5.16. (a) Schematic diagram of TLM test structure and (b) the parameter extraction from the plot of total resistance as a function of contact separation…………………….……………………91

Fig. 6.1. The AFM images (5 μm x 5 μm) of as grown (a) p-$In_{0.53}Ga_{0.47}As$ & (b) n-$In_{0.53}Ga_{0.47}As$ (110) epi-layers…………………………………………...………………………………..97

Fig. 6.2. Cross-section of p- & n-type InGaAs (110) layers on InP (110) substrates….…………97

Fig. 6.3. Multi-frequency (1kHz to 1MHz) room temperature C-V characteristics of Au/Pt/ Al_2O_3/InGaAs (110) MOSCAPs: (a) p-type and (b) n-type before FGA, and (c) p-type and (d) n-type after FGA. Scaled conductance characteristics (G_m/ω) of p-type InGaAs (110) MOSCAPs after FGA as a function of gate voltage in (e) and frequency in (f), respectively………...………99

Fig. 6.4. TEM of p-type and n-type InGaAs (110) MOSCAPs after FGA………….…..………101

Fig. 6.5. The fitting of experimental low frequency C-V characteristics (1kHz) of Au/Pt/ Al_2O_3/InGaAs (110) MOSCAPs (110) MOSCAPs are modelled in (a) p-type and (b) n-type before FGA, and (c) p-type and (d) n-type after FGA. Horizontal dotted lines shown in the diagrams indicates the C_{ox} values derived from a comparison between experimental and modelled C-V curves…………………………………………………………………..……………………102

Fig. 6.6. Extracted D_{it} profile of p-type and n-type $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs before and after FGA……………………………………………………………………………………......……..103

Fig. 6.7. Bi-directional CV sweeps measured at 1MHz for $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs before and after FGA, using the same starting gate bias in inversion and increasing maximum gate bias in accumulation (V_{max}), with plots CV hysteresis as a function of V_{max} of (b) p-type and (c) n-type MOSCAPs, respectively…………………………………………………………………….…....104

Fig. 6.8. CV hysteresis as a function of $|V_{max} - V_{fp,up}|$ is illustrated in log-log scale for p-type and n-type InGaAs (110) samples before and after FGA……………………..…………..…106

Fig. 6.9. The gate leakage characteristics of sulphur passivated $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) MOSCAPs before and after FGA…………………………………………………….……..……..107

Fig. 6.10. Plot of log scaled J/E^2_{ox} as a function of E_{ox} for $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) and (110) MOSCAPs. The gate leakage characteristics is shown in the inset………………..………..…108

Fig. 7.1 Room temperature C-V frequency variation of in-situ Au/Pt/HfO2 (25 cycles)/ etched (100)- and (110)-oriented n-$In_{0.53}Ga_{0.47}As$/InP MOSCAP with FGA (top and bottom row) subjected to without and with 10 cycles of TMA/plasma N_2 and TMA/plasma H_2 pre-treatment……………………………………………………………………….…………..114

Fig. 7.2 The metrics of frequency dispersion in accumulation, stretch-out and hysteresis of all capacitors.……………………………………………………….……………..……115

Fig. 7.3 Map of parallel conductance as a function of gate voltage and frequency for (110)-oriented n-$In_{0.53}Ga_{0.47}As$/InP MOSCAP (a) without and (b) with in-situ plasma H_2 pre-treatment. ……………………………………………………………………………..……...117

Fig. 7.4 (a) the plot of trap response frequency as a function of trap energy level obtained by Equation 7.6 using the parameter of a capture cross section $\sigma = 1\,x\,10^{-16} cm^{-2}$, the values of average thermal velocity obtained and majority band of DOS obtained by equation of $v_{th} = \sqrt{3k_BT/m^*}$ [7.8] and ,$D_{dos} = 2(2\pi m^* k_BT/h^2)^{2/3}$ [7.8] respectively and (b) the D_{it} value as a function of measurement frequency …………………………………………….……………..118

Fig. 7.5. EELS map of Au/Pt/HfO_2 (25 cycles)/etched (100)-oriented n-$In_{0.53}Ga_{0.47}As$/InP MOSCAP with FGA subjected to (a) without and (b) with 10 cycles of TMA/plasma H_2 pre-treatment and in-situ Au/Pt/HfO_2 (25 cycles)/etched (110)-oriented n-$In_{0.53}Ga_{0.47}As$/InP MOSCAP with FGA subjected to (c) without and (d) with 10 cycles of TMA/plasma H_2 pre-treatment.……………………………………………………………………..………….120

Fig. 7.6. XPS As 3d of HfO_2/InGaAs (100) and (110) samples with and without FGA……………………………………..…………………………………………………..…122

Fig. 7.7. XPS Ga 2p of HfO_2/InGaAs (100) and (110) samples with and without FGA ……………………………………………………………………………………..…..122

Fig. 7.8. Ga 2p comparison of InGaAs (100) and (110) blanket samples.……………………………………………………..……………….…………123

Fig. 7.9. Deconvoluted XPS Ga $2p_{3/2}$ for: (a) InGaAs (100) and (b) InGaAs (110).…………………………………………………………………………………..123

Fig. 7.10. Process flow of in-situ InGaAs gate stack formation subjected to plasma gas pre-treatment on (100) and (110) orientation of etched InGaAs surfaces via in-situ TiN capping layer insertion. …………………………………………..……………………………...……..125

Fig. 7.11. C-V characteristics of (a) 25 cycles and (b) 20 cycles of HfO_2 dielectric deposition subjected to TMA/plasma H_2 pre-treatment with ~10nm TiN capping layer insertion………………………………………………………………………….…………126

Fig. 7.12. Metrics of hysteresis and flatband voltage verse CET………………...……………127

Fig. 7.13. C-V characteristics of TiN capping layer inserted $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs with 25 cycles of HfO_2 dielectric deposition subjected to TMA/plasma H_2 pre-treatment……………………………………………………………………………...…..127

Fig. 7.14. CET vs. leakage curent……………………………......………………………128

Fig. 8.1. Layer structure of $In_xGa_{1-x}As$ (a) p-n and (b) p-i-n Tunnel-FETs…………..………..131

Fig. 8.2. Measured (a) transfer characteristics, (b) subthreshold swing as a function of drain current of p-n and p-i-n Tunnel-FET and (c) transconductance characteristics of p-i-n Tunnel-FET. The device figures of merit are as follows: SS_{min} = 120mV/de at drain bias of 50mV for p-i-n Tunnel-FET. The threshold voltage of 0.23V is extracted by linear extrapolation of the transfer characteristics at the drain bias of 300mV. On-off ratio: 1 order at the drain bias of 300mV (I_{off} at V_{th} – 1/3 V_d and I_{on} at V_{th} + 2/3 V_d) [8.1]………………………………..…………………132

Fig. 8.3. Output characteristics of (a) p-n Tunnel-FET and (b) p-i-n Tunnel-FET with R_{on} value of 2100 and 90kΩ/µm, The $I_{d,max}$ for p-i-n Tunnel-FET is around 5µA/µm obtained at the drain bias of 500mV and the gate bias of 900mV……………………………..………...……….134

Fig. 8.4. (a) transfer characteristics and (b) the SS as a function of drain current for p-i-n Tunnel-FETs with 20 and 25 cycles of $HfO_2/In_{0.53}Ga_{0.47}As$ gate stack, respectively………………...…135

Fig. 8.5. Layer structure of p-n-i-n heterojunction……………………………………………..136

Fig. 8.6. Plot of (a) transfer and transconductance characteristics at condition of V_{ds} = 300mV, (b) transfer characteristics at condition of V_{ds} = 50mV, 100mV, 300mV and 500mV and (c) output characteristics of p-n-i-n Tunnel-FET……………………………………..……………..137

Fig. 8.7. Plot of SS as a function of drain current for the comparison of p-i-n and p-n-i-n Tunnel-FETs……………………………………………………………………………………...…138

Fig. 8.8. (a) transfer characteristics and (b) output characteristics of single gate and double gate p-n-i-n Tunnel-FETs………………………………………………………....…………...139

Fig. 8.9. I_{on} vs. I_{off} at V_{DD} = 0.3V among the published vertical nanowire Tunnel-FETs based on III-V materials [8.2-9]. Some points are with other V_{DS} values due to data availability………..140

Fig. 8.10. Output characteristics of fin/wires based p-n-i-n Tunnel-FET…………..…………141

I. Introduction

1.1 Background

The first logic circuits to merge p-channel and n-channel metal-oxide-semiconductor transistors (MOSFETs) to form complementary metal oxide semiconductor (CMOS), were demonstrated in 1963 by C. T. Sah and Frank Wanlass of the Fairchild R & D Laboratory [1.1]. This circuit topology has the theoretical potential to have zero power dissipation in standby mode. This capability of CMOS technology for very low power dissipation integrated circuits (ICs) has driven the development of consumer electronics in the past five decades, as CMOS technology is widely used in microprocessor and memory applications. From a manufacturing perspective, based on the observation of Gordon E. Moore, Moore's law [1.2] indicates the processing speed of CMOS-based integrated circuits (ICs), doubles and costs half in the period of roughly every two years, which serves the purpose of pursuing high speed ICs in semiconductor industry enabled by boosting both p and n-MOSFET performance as a results of the scaling rules [1.3] shown in Table. 1.1.

Parameters	Scaling
Device dimensions	$x', d'_{ox}, d'_j \rightarrow x/k$
Voltages	$V' \rightarrow V/k$
Substrate	$N'_{sub} \rightarrow N_{sub} \cdot k$
Current	$I'_d = \mu_{eff} \frac{W}{L} \frac{\varepsilon_{ox}}{t_{ox}/k} \frac{(V_g - V_{th})^2}{2k^2} \rightarrow I_d/k$
Power	$P' = I'V' \rightarrow P/k^2$
Energy-delayed product (EDP)	$P', t' \rightarrow Pt/k^3$

- *Device dimentions* x: *channel width* (W) *or length* (L), d_{ox}: *oxide thickness*, d_j: *junction depth*
- *Voltages* V: *supply voltage* (V_{DD}) *or thershold voltage* (V_{th})
- *Substrate* N_{sub}: *substrate doping concentration*
- *Current* I_d: *drive current in saturation*, V_g: *gate voltage*
- *Power* P: *power dissipation per device*, t: *gate delay (switching speed)*
- μ_{eff}: *effctive mobility*, ε_{ox}: *permitivity of dielectric layer*, t_{ox}: *thickness of dielectric layer*

Table. 1.1. Dennard's scaling rules for device and circuit of a given size, where k is the scaling parameter. [1.3].

1.2 The power dissipation issue in CMOS switching devices

Despite the benefit of the scaling rules, which provides enhancement of device performance, the issue of power consumption in Fig. 1.1 (a), which results from the increased power density of ICs, also occurs. As the diagram shows, the power consumption is divided by the static power and dynamic power consumption that is related to the switching energy of a logic operation. The total switching energy can be written as [1.4,1.5]:

$$E_{total} = E_{dynamic} + E_{leakage} = \alpha L_d C {V_{DD}}^2 + L_d I_{OFF} V_{DD} \tau_{delay}$$

$$\approx L_d C {V_{DD}}^2 \left(\alpha + 10^{\frac{-V_{DD}}{S}}\right), \quad (1.1)$$

where L_d is the logic node, C is the switching capacitor, τ_{delay} is the delay time, s is the average subthreshold swing (SS) and α is the switching activity factor. As a result, scaling supply voltage (V_{DD}) is very important for low power device application. However, the scaling of V_{DD} is not proportional to transistor density below the 90nm technology generation as shown in Fig. 1.1 (b) [1.6]. In addition, the unscaled thermal voltage, while reducing the V_{DD}, result in an exponential increase in off-state current [1.5] that also results in higher static power dissipation [1.7].

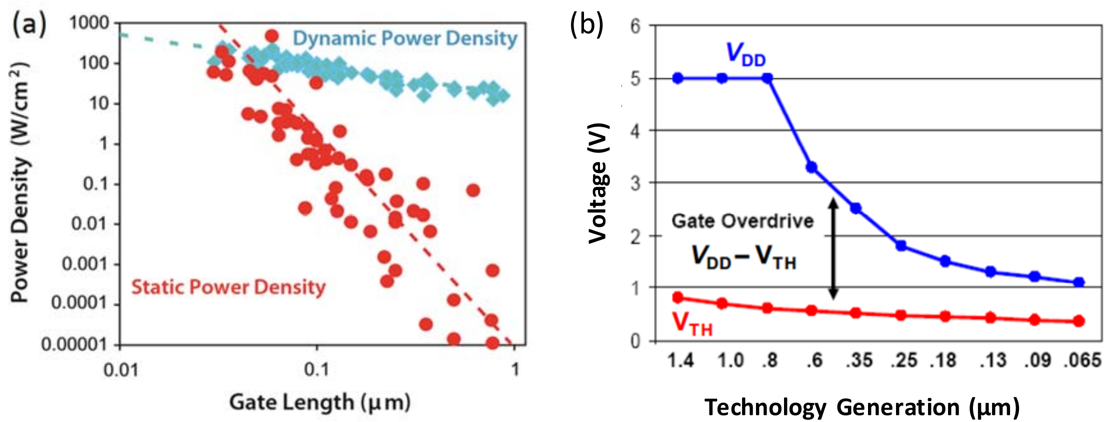


Fig. 1.1. The trends of (a) static power density and dynamic power density with gate length scaling [1.8] and (b) the supply voltage with the technology node scaling [1.6].

1.3 The key challenges of alternatives

To solve the issue of V_{DD} scaling and the realisation of low off-state current, minimising the SS is required. For a MOSFET, the SS can be written as [1.9]:

$$SS = \frac{\Delta V_g}{\Delta \log_{10} I_D} = \frac{d\varphi}{d(\log_{10} I_D)} \times \frac{dV_g}{d\varphi} = ln10 \left(\frac{d\varphi}{dI_D}\right)\left(\frac{dV_g}{d\varphi}\right) = 2.3\frac{kT}{q}\left(1 + \frac{C_d}{C_{ox}}\right), \quad (1.2)$$

where φ is the surface potential of the semiconductor. I_D which flows from source to drain is exponentially increasing with the surface potential at subthreshold region [1.10], refer to Equation (2.1). Therefore, the first derivative term of $\left(\frac{d\varphi}{dI_D}\right)$ obtained at subthreshold region is kT/q (k is Boltzmann constant and T is the absolute temperature) dominated by diffusion current transport as the subthreshold current is independent of the drain voltage [1.10]. In addition, the second term can be represented as $1 + C_d/C_{ox}$ [1.10], refer to Equation (2.2). C_d and C_{ox} is the channel depletion capacitor and gate oxide capacitor, respectively. Therefore, only by overcoming the first term (transport factor) or reducing the second term (body factor) below 1 [1.11] can improve the SS below 60mV/dec at the room temperature.

1.4 Scope of proposed solutions

The previous sections indicate that reduction of power dissipation requires the operation of transistors at reduced supply voltage and the importance of overcoming the rising of transistor off-state leakage current by providing superior subthreshold swing. One possible solution to reducing subthreshold swing below 60mV/dec at room temperature is by utilizing alternate switching effects such as band-to-band tunneling (BTBT) which is the basis of the tunnel-field effect transistor (Tunnel-FET) [1.12]. As BTBT-based device operation does not depend on carrier injection $over$ a barrier, the room temperature SS limitation of 60mV/dec, which is fundamentally defined by Boltzmann statistics for device operation [1.13], can be overcome. This thesis explores the possibilities of III-V Tunnel-FETs as an alternative to traditional MOSFETs to realise power efficient transistors for low power CMOS applications.

1.5 Thesis outline

This research explores the potential of power efficient n-channel transistors with Tunneling-based switching using III-V compound semiconductors for next generation CMOS technology. III-V materials are considered due to their low effective electron mass and flexible bandgap modulation. Following background theory explanations in Chapter II, a description of generic fabrication techniques in Chapter III, an overview of Tunnel-

FET operation, in Chapter IV ,and a description of the experimental details and various characterisation methods is given in Chapter V. A description of experimental work starts in Chapter VI with the study of the characteristics of an atomic layer deposited high-k gate stack on (110) oriented $In_{0.53}Ga_{0.47}As$, an important semiconductor crystallographic orientation for non-planar devices. Next, Chapter VII includes the first reported evaluation of the properties of a high-k gate stack deposited in-situ on InGaAs surfaces of various orientations which have been subjected to a plasma etch process of the type to form a non-planar III-V transistor geometry. The incorporation of plasma H_2 and N_2 pre-treatments after plasma etching and before in-situ dielectric deposition is also described in this chapter. In addition, this chapter describes routes to scaling the effective oxide thickness of gate stacks on InGaAs using approaches that do not introduce damage to the semiconductor. These process module developments are brought together in the demonstration in Chapter VIII of the first demonstration of planar p-n, p-i-n and p-n-i-n Tunnel-FETs with an in-situ gate stack. This chapter also describes the performance of the first demonstration of a non-planar p-n-i-n III-V Tunnel-FET. The thesis concludes with Chapter IX, which also describes possible future work.

1.6 Reference

[1.1] "Progress Reports—Solid State Physics Section," 1 June 1963, 23, Box 8, Binder, Fairchild Camera and Instrument Technical Papers and Progress Reports, Collection M1055, Department of Special Collections, Stanford University, Stanford, California (hereafter FCI); "Progress Reports—Solid State Physics Department," 1 October 1963, 18, Box 9, Binder, FCI; "Progress Reports—Solid State Physics Section," 1 November 193, 10, 21-23, Box 9 Binder, FCI.

[1.2] G. E. Moore, *Cramming more components onto integrated circuits*, New York, McGraw-Hill, 1965.

[1.3] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous and A. R. LeBlanc Design of ion-implanted MOSFET's with very small physical dimensions", in *IEEE J. Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, 1974.

[1.4] H. Kam, T.-J. King-Liu, E. Alon and M. Horowitz, "Circuit-level requirements for MOSFET-replacement devices*", Tech. Digest IEEE Int. Electron Devices Meet*. 1, 2008.

[1.5] S. Hanson, M. Seok, D. Sylvester and D. Blaauw, "Nanometer device scaling in subthrehold logic and SRAM", *IEEE Trans. Electron Devices,* 55, 175–185, 2008.

[1.6] P. Packan, “Device and Circuit Interactions”, *IEEE International Electron Device Meeting (IEDM '07) Short Course: Performance Boosters for Advanced CMOS Devices*, 2007.

[1.7] H. Iwai, “Roadmap for 22 nm and beyond (invited paper)”, *Microelectronic Engineering*, vol. 86, no. 79, pp. 1520-1528, 2009.

[1.8] B. Meyerson, *Semico Impact Conference,* Taiwan, January 2004.

[1.9] S. M. Sze, and K. K. Ng, *Physics of Semiconductor Devices*, Hoboken, New Jersey: Wiley, 2007, pp. 315.

[1.10] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, New York: Cambridge University Press, 2009, pp. 164-165.

[1.11] S. Salahuddin and S. Datta, “Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices”, *Nano Letters*, 8, 405-410.

[1.12] A. M. Ionescu and H. Riel, “Tunnel field-effect transistors as energy-efficient electronic switches”, *Nature.* 479, 329-337, 2011.

[1.13] A. Biswas and M.A. Ionescu, “Tunnel Field Effect Transistors: from Steep-Slope Electronic Switches to Energy Efficient Logic Applications”*,* Lausanne, EPFL, 2015.

II. Background Theory

2.1 Introduction

The Tunnel Field Effect Transistor (Tunnel-FET), based on the operation principle of band-to-band tunneling (BTBT), is being actively explored as a device for low power logic devices and digital applications by a number of teams worldwide. This chapter will briefly provide the overview of the basic principles and operational concepts that are required to understand and analyse Tunnel-FETs. First, device-related metrics for the evaluation of device performance will be introduced, followed by representations of the signature gate stack module, alongside details of some possible issues that should be addressed when realising Tunnel-FETs. Then, an explanation will be given for the importance of III-V materials in device enhancement, followed by a discussion of the characteristics of Esaki diode components. Finally, the chapter will conclude with a section on the theory describing contacts between metal and semiconductor.

2.2 Band-to-Band Tunneling Field Effect Transistors

The schematic diagram of traditional MOSFET is shown in Fig. 2.1 (a). The structure contains three terminals: source, drain and gate. The traditional n-channel or p-channel device is doped symmetrically in the source and drain region either side of the gate such as $n^+/p/n^+$ or $p^+/n/p^+$ [2.1]. The concept of an n-channel Tunnel-FETs shown in Fig. 2.1 (b) which in contrast to a traditional MOSFET utilises a p-doped source instead to minimize the band-gap between the conduction band and valence band for the band-to-band tunneling (BTBT) [2.2,2.3]. Compared with the traditional MOSFETs, Tunnel-FETs can potentially provide sharper switching characteristics under the condition of lower V_{DD} operation due to less restriction of thermionic emission from the source into the channel region, where the carrier injection relies on modulating the channel potential with respect to the gate voltage [2.4]. Quantitatively, the switching, based on the Boltzmann distribution, is estimated to be 60 mV/decade according to the theory [2.5]. The typical value in a state-of-the-art MOSFET is approximately in the range 90mV/decade to 100mV/decade due to other problems such as the short channel effect [2.6,2.7]. The simplified sub-threshold current formula, in the traditional MOSFET results from the carriers of n-channel or p-channel under the V_{GS} of gate terminal, can be expressed as below [2.4]:

$$I_{DS} \cong e^{\frac{V_{GS}}{mV_T}}, \quad (2.1)$$

where V_T is the thermal voltage, defined as the kT/q (k is Boltzmann constant and T is the absolute temperature). The m factor is the ideal subthreshold factor [2.4], which can be defined as $(1 + C_d/C_{ox})$. C_d and C_{ox} is the channel depletion capacitor and gate oxide capacitor, respectively. The $1/m$ term can be represented as the contribution of surface potential by applied gate voltage.

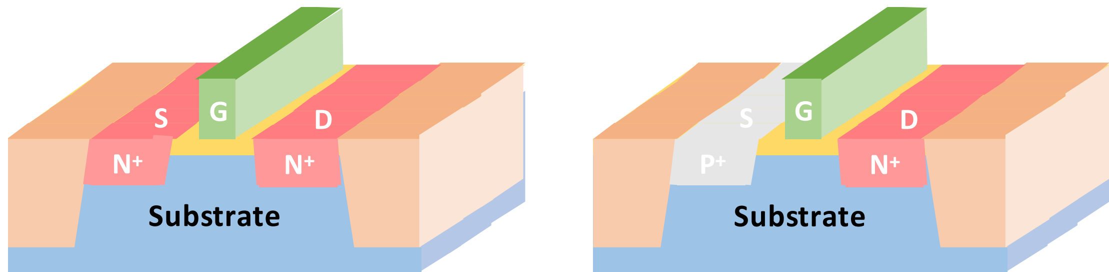


Fig. 2.1. Schematic diagram of (a) n-channel MOSFET and (b) n-channel Tunnel-FET cross-section.

2.3. Basic operation

In the previous section, the basic structure of Tunnel-FET was introduced. Next, the details of Tunnel-FET operation will be discussed in this section. In Fig. 2.2, the schematic diagram shows the principles of operation of a MOSFET and Tunnel-FET. The operation of a Tunnel-FET is similar to that of a MOSFET where the potential barrier for carrier injection from the source to the channel region is modulated with a gate bias. The mechanism of carrier injection for Tunnel-FET however is tunneling *through* the barrier via BTBT instead of the carriers being injecting *over* the potential barrier as in a MOSFET. In a traditional three-terminal field effect transistor such as MOSFET, the on current and off-current can be divided by the threshold voltage. Based on the relationship of gate bias, drain bias and threshold voltage current, the current can be divided in three regions: saturate, linear and sub-threshold regions, which together explain the operation mechanism of a traditional MOSFET [2.8]. For a Tunnel-FET, the division of subthreshold region however is not obvious. In terms of the device switching, the difference between MOSFET and Tunnel-FETs is associated with their carrier injection mechanisms. The steepness of MOSFET switching completely depends on the thermal distribution of mobile charge carriers in the source region but the sharper switching of

Tunnel-FET results from overcoming the limitation of kT/q [2.9]. On the other hand, the on current of MOSFET from source to drain region relies on lowering the potential barrier with respect to gate voltage and increasing the current proportional to gate bias, as given by Equation (2.1), which describes exponential growth. In contrast, the current of Tunnel-FETs is decided by the probability of tunneling through the source-channel barrier according to the Wemtzel-Kramers-Brillouin (WKB) approximation [2.10].

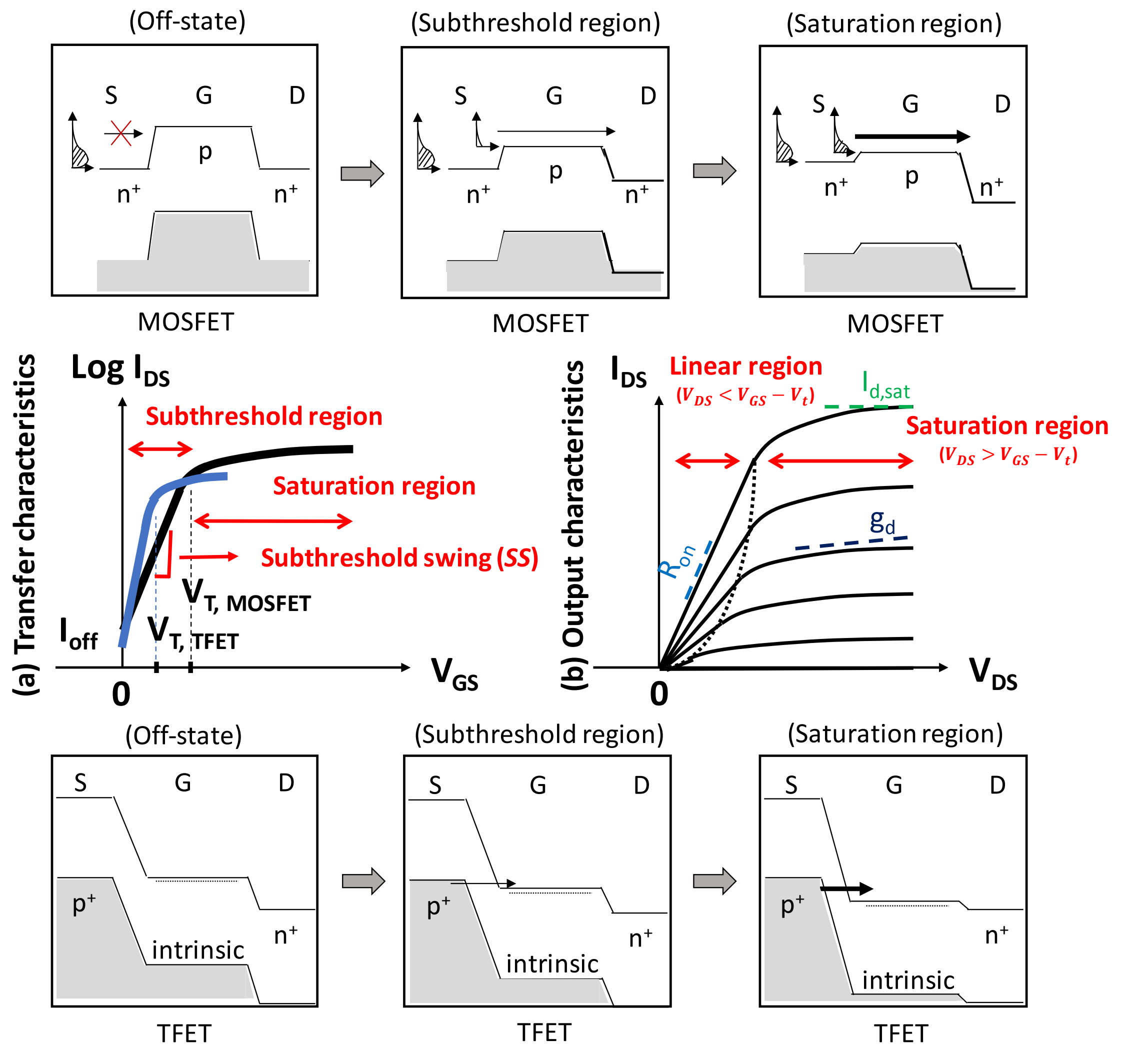


Fig. 2.2. A typical MOSFET's (black curve) and Tunnel-FET's (blue curve) (a) transfer characteristics in log-current scale, which can be divided into off-state, sub-threshold region and saturation region and (b) output characteristics. The operation mechanism of MOSFET and Tunnel-FET in each region is introduced.

2.4. Tunnel-FET characteristics

2.4.1. Subthreshold swing

One of the common metrics used to evaluate Tunnel-FET for low-power device application is the minimum value of sub-threshold swing (SS) defined as $\left[\partial(\log I_{ds})/\partial V_{gs}\right]^{-1}$ for a standard MOSFET. Using the circuit model of capacitance-voltage shown in Fig. 2.3, the formula can be expressed below as [2.4],

$$SS = \left[\frac{\partial(\log I_{ds})}{\partial V_{gs}}\right]^{-1} = \frac{\partial V_{gs}}{\partial \varphi_s}\frac{\partial \varphi_s}{\partial[\log I_{ds}]} = \left(1+\frac{C_s}{C_{ox}}\right)\frac{kT}{q}\ln 10, \qquad (2.2)$$

where C_s is equal to C_d in the sub-threshold region. Based on the first term of Equation (2.2), the surface potential, coupled to gate voltage, is obtained. The sub-threshold current, associated with the Boltzmann distribution of free carriers is fundamentally limited to 60 mV/decade at room temperature (if $C_d \ll C_{ox}$), while in practice the ideal subthreshold factor of $\frac{\partial V_{gs}}{\partial \varphi_s}$ is greater than one for MOSFET. In contrast, the sub-threshold exponential region associated the sub-threshold current does not occur in Tunnel-FETs due to the transport mechanism of tunneling. The SS can be determined by the derivative of Kane-Sze formula and expressed as [2.11]:

$$SS = \ln 10 \left[\frac{1}{Veff}\frac{dVeff}{dVgs} + \frac{\xi + b}{\xi^2}\frac{d\xi}{dVgs}\right]^{-1}, \qquad (2.3)$$

where $Veff$ is the effective bias of band bending on tunneling junction, ξ is the internal electric field and the coefficient b is $4\sqrt{m^*}{E_g}^{3/2}/3q\hbar$, which is associated with the material properties of tunneling junction that m^* is the carrier effective mass, E_g is the energy band gap and $\hbar$ is Planck's constant normalized by 2π. These two terms, which contribute to SS show that the value is not limited by kT/q. Based on the Equation (2.3), there are two ways to enhance the performance of Tunnel-FETs. The first term relies on the gate-source voltage strengthening the gate electrostatic control on the device channel, which depends on the device geometry and gate stack. Therefore, an ultra-thin channel with low equivalent oxide thickness (EOT) gate stack is required. The second term aims to maximize the internal junction electric field, which is highly dependent on tunnel-junction bias, and therefore material and band-gap engineering, which indicates that high mobility and low band-gap materials (e.g. III-V materials) should be considered. In addition, the leakage mechanism of Tunnel-FET is in the sub-threshold region which may affect the sub-threshold swing. This should be addressed through, for example, Trap-Assisted-Tunneling (TAT) and the trap occupation in the semiconductor or oxide

interface [2.12,2.13]. These unwanted effects caused by defects increase the off-current floor for Tunnel-FET. On the other hand, I_{60}, defined as the current for which the subthreshold swing equals to 60 mV/dec, has become a common figure of merit to evaluate device performance, as it indicates the transition of sub-60 mV/dec and super-60 mV/dec behaviours with respect to the gate bias or drain current, [2.14]. The I_{60} for those devices that are compatible with MOSFETs should be an order of magnitude below the on-state current and requires the value to be importantly larger than the off-state current. Typical values of the off-state current for standby power and low power operating applications are 10^{-4} μA/μm and 10^{-2} μA/μm, respectively. Meanwhile, an on-state current higher than 100 μA/μm is expected [2.15].

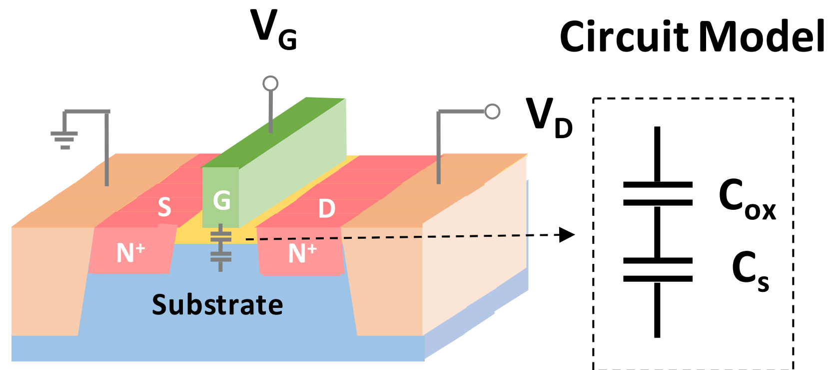


Fig. 2.3. Equivalent circuit model of a MOS capacitor on a n-type MOSFET.

2.4.2. On-current

For a typical MOSFET, the saturation region is approximately proportional to $(V_{DD} - V_t)$ but the saturation current of Tunnel-FET is strongly related to the electrical field. According to the drain current formula of Zener tunneling, the resulting transport characteristics on a heavily doped p-n tunnel junction can be expressed as [2.16],

$$\mathrm{I} = \left(\mathrm{A}q^3\sqrt{2m^*/E_g}/4\pi^2\hbar^2\right)V_{eff}\,\xi\, e^{-\left(\frac{b}{\xi}\right)}, \tag{2.4}$$

where the first term inside the parentheses, which is similar to b in Equation (2.3), combine the material-dependent properties, and A is the cross-sectional area of Tunnel-FET. The current is based on the tunneling probability and band-to-band generation rate, which originally results from the derivative of the WKB approximation [2.16].

2.4.3. Threshold voltage

Threshold voltage is defined as the turn-on point of conventional MOSFETs. As described by the model for MOSFET operation, which relies on the barrier height

modulated by the application of a gate voltage, the threshold voltage for a long-channel silicon based MOSFET is defined as "the gate voltage when the surface potential or band bending reaches $2\psi_B$ and silicon charge is equal to bulk depletion charge for that potential." [2.4] However, there is no pure identification of threshold voltage definition for Tunnel-FET due to the difficulties of distinguishing between the turn-on point contributing to gate threshold voltage vs. drain threshold voltage, which is unique to Tunnel-FET. The physical definition of gate threshold voltage is defined as "the voltage marking the transition between an exponential dependence, and a linear dependence of drain current on applied bias. This also marks the transition between the strong control and the weak control of the tunneling energy barrier at the tunnel junction by that voltage" [2.17]. The practical extraction for gate threshold voltage is done by using the transconductance charge (TC) method, where the gate threshold voltage for any non-linear devices is the gate voltage corresponding to the maximum of the transconductance derivative (dg_m/dV_{gs}) [2.17, 2.18]. The transconductance of a device is defined as the derivative of the drain current with an applied gate bias under the fixed condition of drain bias, refer to Section 2.8. On the other hand, the drain threshold voltage, which has similar physical meaning as the gate threshold voltage, is introduced and shows up in the same way as the gate threshold voltage definition. This marks the transition point, which distinguishes the transition of the drain current from quasi-exponential to linear. Neither gate voltage nor drain voltage can drive important current flow through the device, because the complexity of narrowing the energy for the switch-on current requires control of both gate and drain voltages, especially the drain voltage. The value of the drain threshold voltage is estimated to be half that of the gate voltage threshold voltage under the extraction by the same technique. [2.17]

2.4.4. Off-current

Observed by Equation (2.1), the off state current for a MOSFET is not zero because of the effect of thermionic emission, which can still allow a few carriers to be emitted over the potential barrier. In contrast, the off state current for a Tunnel-FET is highly dependent on the leakage current of the reversed-biased tunneling diode, which can be potentially smaller than the off-current of MOSFET [2.19]. For a typical tunneling diode, the leakage current on the side of reverse bias is dominated by the mechanism of Shockley-Read-Hall (SRH) generation-recombination and TAT [2.20, 2.21].

2.5. Metal-Oxide-Semiconductor capacitors

2.5.1. Physics

One of the key modules for MOSFETs and Tunnel-FETs, is the metal-oxide-semiconductor (MOS) capacitor. It is used in both devices to control the channel potential by an applied gate bias to allow the electron emission (for MOSFET) or the electron tunnel through the barrier (for Tunnel-FET). Fig. 2.4 (a) shows the schematic diagram of a MOS capacitor cross-sectional view. The basic structure of MOS capacitor comprises a sandwich structure of metal, oxide film and semiconductor substrate. Fig. 2.4 (b) is the band diagram of an ideal p-type MOS capacitor using the concept of energy barriers at thermal equilibrium ($V_g = 0$). Therefore, the bias, called flat band voltage, is the difference of potential between the work function and the semiconductor surface potential when the surface electric field in the substrate and the net charge in the substrate are both zero.

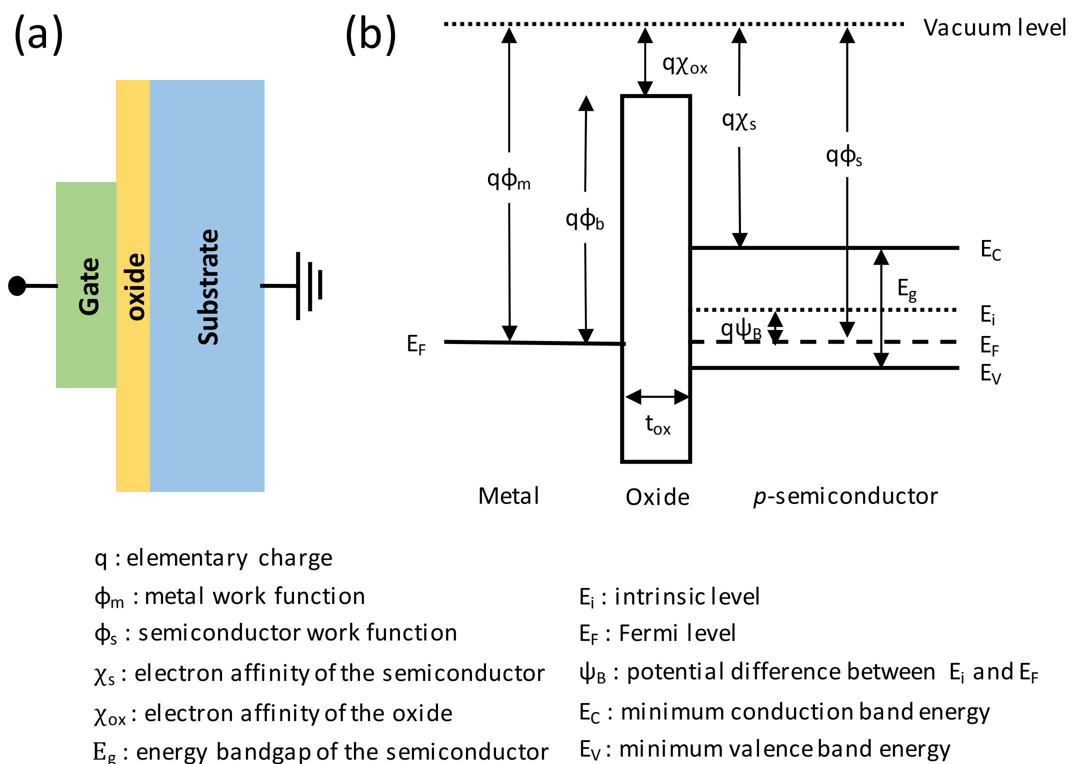


Fig. 2.4. (a) Schematic diagram of a metal-oxide-semiconductor (MOS) capacitor and (b) the energy band diagram of a MOS capacitor at thermal equilibrium ($V_g = 0$).

In addition, the surface band bending under different gate bias voltages in the band diagram shows each charge status. The transition of these statuses can be divided into the following regions: accumulation, depletion, weak inversion and strong inversion.

Accumulation

In the accumulation region, the carrier close to the interface between the oxide layer and semiconductor gives rise to a charge, mediated by band bending in the semiconductor, from the free carrier state to the state characterized by majority carriers. In, Fig. 2.5 (a), the majority carrier (hole for p-type semiconductor substrate; electron for n-type semiconductor substrate) is accumulated while the surface potential is smaller than the flat-band voltage for p-type materials and larger for n-type materials. The hole concentration at the interface of oxide and semiconductor can be represented by:

$$p_s = n_i e^{q(\psi_B - \psi_s)/kT}, \tag{2.5}$$

where the hole concentration is a function of absolute temperature, k is the Boltzmann constant and n_i is the intrinsic concentration, which is defined as:

$$n_i = \sqrt{N_C N_V} e^{(E_c - E_v)/2kT}, \tag{2.6}$$

where N_C and N_V is the effective density of states in the conduction and valence band, respectively.

Depletion

The depletion region starts in the bias condition of the flat-band voltage described previously. The charge in the substrate gradually becomes negative and the hole concentration decreases importantly due to the removal of the hole close the interface between the oxide and the semiconductor when bias exceeds the flat-band voltage, resulting in downward band bending ($\psi_B > \psi_s > 0$). Therefore, the depleted charge for a p-type semiconductor close to the surface can be represented as the negatively charged acceptor ions (${N_A}^-$). This carrier free region is also known as the depletion region where the concentration of acceptor doping can be written as:

$$N_A = n_i e^{q\psi_B/kT}. \tag{2.7}$$

The depletion width can be obtained by solving the one-dimensional Poisson equation shown below:

$$X_d = \sqrt{\frac{2\epsilon_s \epsilon \psi_s}{qN_A}}, \tag{2.8}$$

where X_d is the width of the depletion region and ϵ_s is the relative permittivity of the semiconductor.

Weak Inversion

The energy bands continue bending down under the gate bias, making the surface band bending more positive. The surface becomes weakly inverted while energy E_F meets at the energy of E_i at the interface of oxide and semiconductor ($\psi_s = \psi_B$). Under this condition of the gate bias, the intrinsic concentration of semiconductor is equal to the hole and electron concentrations:

$$p_s = n_s = n_i. \tag{2.9}$$

Strong Inversion

The surface moves into strong inversion with the further increase of intrinsic level of semiconductor downward to the Fermi level. This results in the attraction of electrons at the interface of oxide and semiconductor (Fig. 2.5). The surface electron concentration can be expressed as:

$$n_s = n_i e^{-q(\psi_B - \psi_s)/kT}. \tag{2.10}$$

The surface potential at strong inversion can be derived by combining Equations (2.7) and (2.10):

$$\psi_{s,strong\ inversion} = 2\psi_B = \frac{2kT}{q} \ln\left(\frac{N_A}{n_i}\right). \tag{2.11}$$

On the other hand, the depletion region reaches its maximum limit at the strong inversion region. This represents the fact that there is only generation of electron rather than the width extension with any further increase in positive gate bias. By substituting Equation (2.11) into (2.8), the maximum depletion width can be obtained as follows:

$$x_{d,maximum} = \sqrt{\frac{4\epsilon_s \epsilon kT ln(N_A/n_i)}{q^2 N_A}}. \tag{2.12}$$

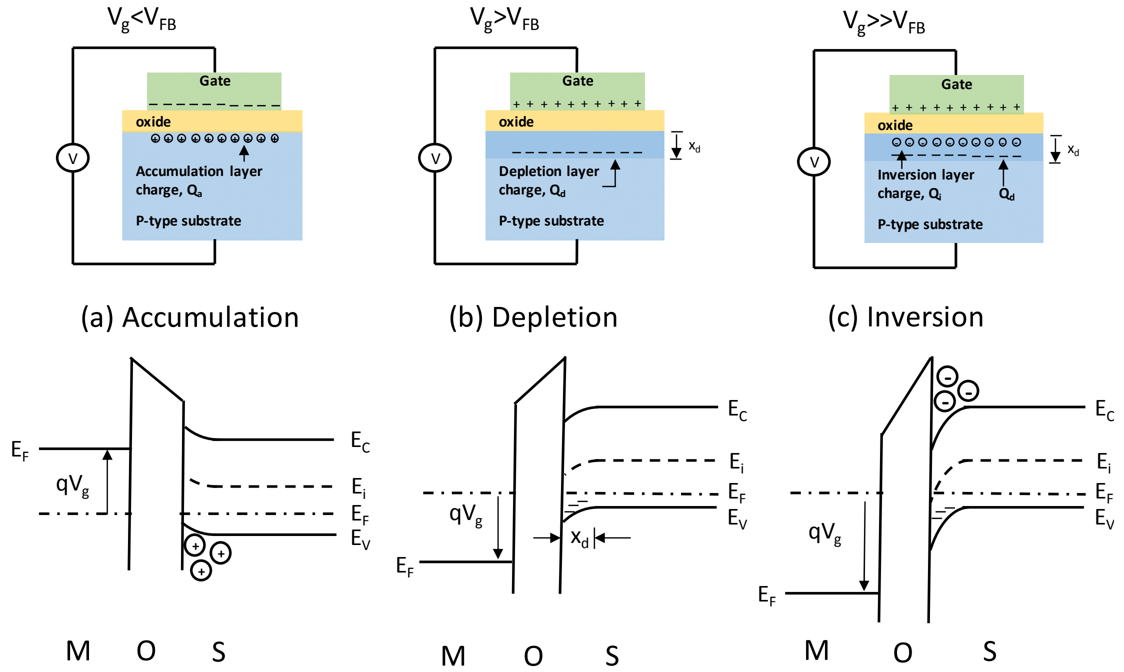


Fig. 2.5. Energy band diagram and the charge states of a p-type MOS capacitor in (a) accumulation, (b) depletion and (c) inversion.

2.5.2. Capacitor-Voltage characteristics

This section will discuss the characteristics of Capacitor-Voltage (C-V) characteristics at the condition of thermal equilibrium. The capacitor responds by a DC gate bias and small amplitude AC signals from hundreds of Hz to a few MHz. The Fermi level position at the interface is determined by the DC bias due to induced space charge and band bending. The oscillations around the energy level position depend on the AC signal frequencies. Considering the small-signal circuit for a MOS capacitor shown in Fig. 2.6, the total capacitance can be expressed as the combination of a fixed-voltage independent oxide capacitor and a voltage-dependent semiconductor capacitor $C_s(\psi_s)$ as shown below:

$$\frac{1}{C} = \frac{1}{C_s(\psi_s)} + \frac{1}{C_{ox}}, \tag{2.13}$$

where the oxide capacitance can be represented as $\epsilon_{ox}\epsilon_0/t_{ox}$. The t_{ox} means the physical thickness of oxide layer, ϵ_{ox} is the relative permittivity of the selected materials and ϵ_0 is the permittivity of free space. The frequency dependent C-V characteristics depends on the carrier response times. The majority and minority carrier response times can be represented, respectively [2.22]:

$$\tau_{majority} = \frac{\epsilon_s\epsilon_0}{q\mu N_A}, \tag{2.14}$$

$$\tau_{minority} = \frac{1}{\sqrt{2}}\frac{N_A}{n_i}\sqrt{\tau_{Lp}\tau_{Ln}}\left(\sqrt{1-\frac{\psi_T}{\psi_B}}\right), \tag{2.15}$$

where τ_{Lp} and τ_{Ln} are the bulk hole and electron lifetimes, respectively, $\sqrt{\tau_{Lp}\tau_{Ln}}$ is the minority carrier lifetime and ψ_T is the potential that signifies the bulk trap level above the intrinsic level [2.22]. If the period of the AC signal is much longer than the majority or minority carrier response time, the carriers will follow the applied signal frequency.

C-V characteristics in accumulation

In the accumulation region, the dominant charge at the semiconductor-oxide interface is comprised of majority carriers. When the signal frequency is applied in the MHz range, the majority carriers can follow the AC signal. Due to the high concentration of accumulated sheet charge, the accumulation capacitance, which reaches a maximum value, can be estimated to be C_{ox}.

C-V characteristics in depletion

Based on the Equation 2.8 showing the enlarged depletion width with respect the gate bias, this gives voltage-dependent semiconductor capacitance in the depletion region. The depletion-layer capacitance can be given based on the parallel-plate analogy below:

$$C_d = \frac{\epsilon_s\epsilon_0}{x_d} \tag{2.16}$$

$$\frac{1}{C_{dep}} = \frac{1}{C_{ox}} + \frac{x_d}{\epsilon_s\epsilon_0}. \tag{2.17}$$

The depletion capacitance is the oxide capacitance in series with the depletion layer capacitance.

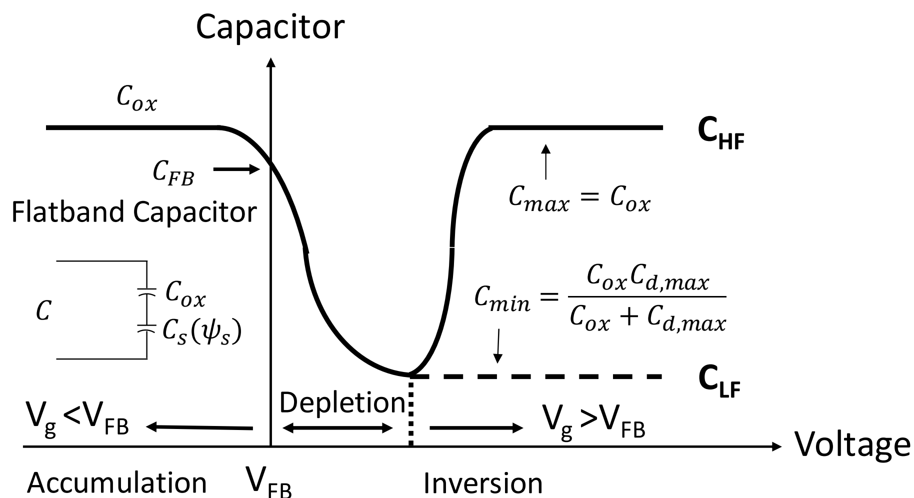


Fig. 2.6. Capacitor-Voltage characteristics of an ideal p-type MOS capacitor.

C-V characteristics in inversion

The C-V characteristics in inversion are highly dependent on the frequency of AC signals, a phenomenon shown in Fig. 2.6, which depicts two cases with respect to the thermal generation-recombination rate of minority carrier response. First, we introduce the low-frequency (LF) response in inversion. This case happens if the period of the AC signal is much shorter than the minimum minority carrier response time. Therefore, the sheet charge is rapidly accumulated and then saturated in the inversion layer. Similarly, to the case of accumulation, the value of total capacitance has a maximum value close to C_{ox}. On the other hand, the high-frequency (HF) response in inversion indicates that the minority carrier cannot continue following the signal while the period of AC signals remains shorter than the minimum minority carrier response time. The corresponding inversion capacitance saturates at the value of C_{min} determined by the maximum depletion width, as shown in Equation (2.12). Hence, C_{min} can be derived further below from Equation (2.17):

$$C_{min} = \frac{\epsilon_s \epsilon_{ox} \epsilon}{\epsilon_{ox} x_{d,max} + \epsilon_s t_{ox}} . \quad (2.18)$$

2.5.3. Charge traps

In practice, the MOS capacitor system presents some non-ideal effects that result in the degradation of electrical characteristics. These effects mainly come from the charge defects at the interface of oxide and semiconductor or inside the oxide itself, as shown in Fig. 2.7. According to the location of defects, the defect can be categorized as interface defects or oxide defects

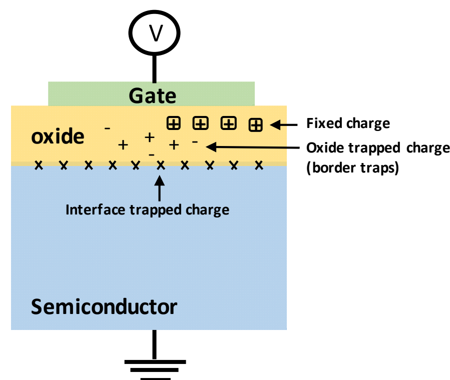


Fig. 2.7. Schematic diagram of the charge defects associated with a MOS capacitor.

2.5.3.1. Interface traps

Defects, such as interface traps, are depicted in Fig. 2.7. The interface traps, which can be also understood as localized states, distributed with energy at the interface between the dielectric layer and semiconductor can trap electrons or holes in these localized surface states, where the probability of occupation for these carriers is determined by the surface-state energy corresponding to the Fermi-level. [2.4]. Carrier exchange at the certain energy level of a surface state happens by a thermally activated capture and emission process over a range of time scales. The associated trapping lifetime (τ_{it}) is shown below [2.23],

$$\tau_{it} = \frac{e^{(E_{maj}-E_{tr})/kT}}{\sigma \upsilon_t N_{maj}}, \tag{2.19}$$

where E_{tr} is the interface trap energy position and E_{maj} is the energy of the majority carrier band edge, σ is the capture cross-section of the trapping state, υ_t is the thermal velocity of majority carriers and N_{maj} is the density of states in the majority carrier band. The interface traps can either be donors or acceptors. The donor-like traps are neutral in charge when all the traps below the Fermi level are occupied by electrons and positively charged when empty. In contrast, acceptor-like traps are negatively charged when occupied and neutral when empty. The nature of the traps' distribution is dependent on the system's specific oxide and semiconductor, and the case above presumes that the upper half band-gap is comprised of acceptor-like traps and the lower half band-gap is comprised of donor-like traps. In addition, the occupancy of traps varies with the change in gate bias. How C-V characteristics are affected depends on the frequency of measurement, especially under the condition of low frequency, when the traps can respond to AC signals. Considering the simple equivalent circuit, the total capacitance at low frequency ($\tau_{it} < 1/\omega$) can be written as:

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_d + C_{it}}. \tag{2.20}$$

The equation above explains the most common stretch-out behaviour in the *x*-axis obtained from C-V characteristics. The reason lies in the charge exchange of those interface traps at the trap energy location (E_{tr}) that can follow the AC signal and even slowly follow DC gate bias, which requires further band bending than the ideal MOS capacitor under a given gate bias. In contrast, if the C-V measurement is operated under the condition of high frequency ($\tau_{it} < 1/\omega$), the contribution of the total capacitor will

be importantly reduced. However, the traps are still responsive to the DC bias, which causes a similar behaviour of stretch-out shown in the LF curve in Fig. 2.10.

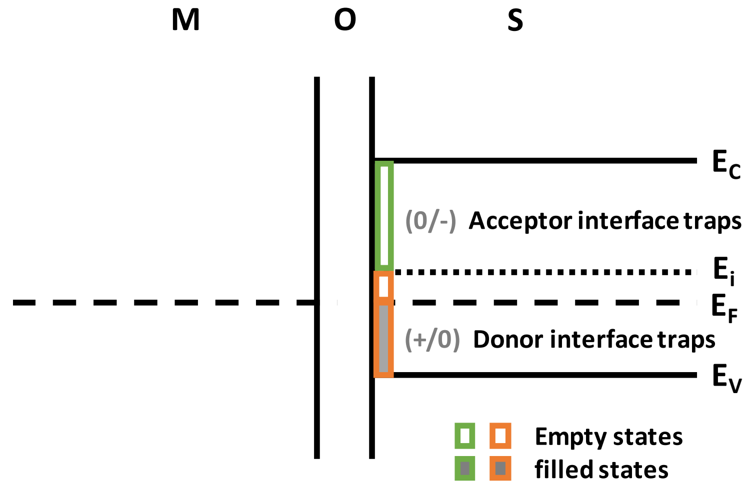


Fig. 2.8. Schematic band diagram of distributed interface traps on a MOS capacitor. For donor-like interface traps, the occupancy of interface traps shows positive interface charge or neutral interface charge when the states are empty or filled, respectively. The acceptor interface charge is neutral when there are no filled states above the Fermi level but it becomes negative when band bending results in the filled states of acceptor-like interface traps.

2.5.3.2. Oxide defects

Oxide defects distributed in the dielectric layer are shown in Fig. 2.9. The defects can be divided into two types of traps: one is the fixed oxide charge, and the other is the oxide trapped charge. The fixed-oxide charge features less electrical communication with the underlying substrate because its high or low energy position makes it difficult to reach the Fermi level. Fixed-oxide charge can be positively or negatively charged, which depends on the charge characteristics being donor-like or acceptor-like and their energy position. As the C-V curves shifts in a parallel manner toward the direction of positive, the negatively charge is full of acceptor-like oxide traps. In contrast, a negative shift of the C-V curve means the fixed-oxide charge is full of the donor-like oxide traps. [2.24]

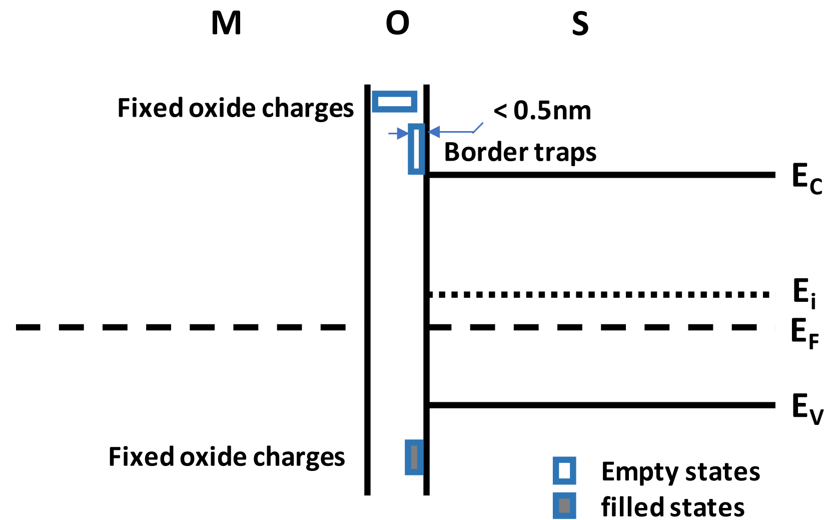


Fig. 2.9. Schematic band diagram of border traps and fixed oxide charges on a MOS capacitor.

On the other hand, oxide trapped charges that are usually neutral can be grouped into border traps and bulk oxide traps. The border traps are in a slow state and are switching oxide traps located at the near-interfacial position. While their energy level is aligned with the conduction band, border traps can electrically communicate with the substrate through a temperature-independent tunneling process. This tunneling only depends on the distance of the defects from the interface and the frequency of AC excitation with the C-V measurement [2.24]. The main issue with border traps is that they cause frequency dispersion in the measured capacitance in accumulation, as shown in Fig 2.10 (a). Because these traps are exponentially decreasing with their distance from the interface within these timescales, the participating traps exponentially decrease with measurement frequency [2.25,2.26]. Under different conditions of gate bias, the border traps also result in differences in the charge trapping or de-trapping time constant [2.23]. Bulk oxide traps, unlike border traps, do not electrically communicate with the semiconductor for all measurement frequencies due to their location being far enough from the interface. Based on the net charge of these traps, the only effect predicted would be a positive or negative shift of C-V characteristics along the voltage axis. The other oxide defect shown in Fig. 2.9 is fixed oxide charges. These traps, which feature similar characteristics of as those of bulk oxide traps (i.e. positive or negative shift of C-V characteristics) are unable to be free in the dielectric layer, and the shift is determined by charge polarity. Also, fixed oxide charges do not communicate electrically with the underlying substrate either.

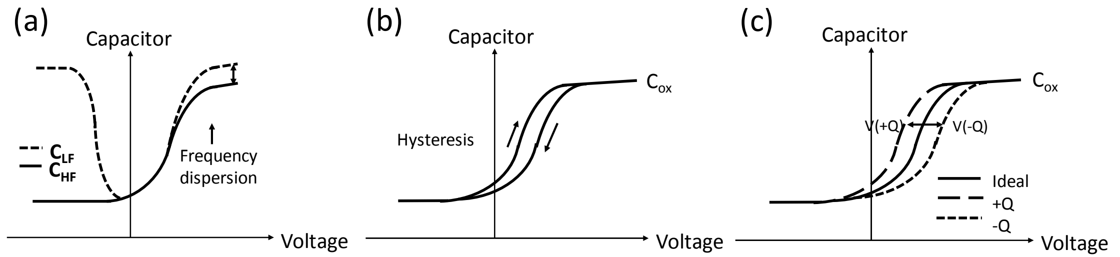


Fig. 2.10. The possible issue of a MOS capacitor from oxide defects: (a) frequency dispersion in accumulation and (b) hysteresis observed from forward and backward C-V sweeps due to border traps. In addition, (c) negative or positive C-V shifting caused by border traps, bulk traps and fixed oxide charges.

2.5.4. High-κ

Over a decade ago, the enhancement of device performance in conventional MOSFETs was driven by scaling rules. One of the main scaling rules in the past was dielectric layer scaling. However, the SiO_2/Si gate stack met the limitations of the gate leakage current while when scaling beyond the CMOS 45 nm technology node [2.27], High-κ dielectric layers, which provide higher permittivity dielectric constants then SiO_2, were introduced to increase the capacitance-equivalent oxide thickness (CET) without thinning down the physical thickness of the gate dielectrics. Similar to the conventional MOSFET, Tunnel-FET also requires a high electric field in the gate stack to increase the tunneling probability for drive current boosting [2.28]. Meanwhile, continued equivalent oxide thickness (EOT) increase can also reduce the sub-threshold swing of Tunnel-FET [2.29].

2.5.5. Finite DOS and charge quantisation

One of the non-ideal effects for MOSCAPs is the density of capacitance or quantum capacitance, which originates from the finite density of states in the conduction or valence bands, contributing to the total capacitance in inversion or accumulation [2.30, 2.31]. Increased carrier concentration is required to overcome the issue of the finite density of states (DOS), causing a finite amount of change in the surface potential. The quantum capacitance can be written as [2.32]:

$$C_{DOS} = \frac{4\pi m^* q^2}{h^2}, \tag{2.21}$$

where h is Planck's constant and $m*$ is the effective carrier mass. Another effect for MOS capacitors causes a deviation from the ideal behaviour, such as charge quantisation at inversion, in which the peak charge density (centroid) is located away from the interface

between oxide and semiconductor by some distance. This effect contributes to the two-dimensional quantisation of charge carriers in the inversion layer [2.31]. Therefore, the capacitance associated with the charge quantisation contributes to the total measured capacitance, and the maximum capacitance in accumulation can be used to obtain the capacitive equivalent thickness of SiO_2. Also, the capacitance associated with the inversion layer thickness can be represented as:

$$C_{cen} = \frac{\varepsilon_s \varepsilon_0}{t_{cen}}. \quad (2.22)$$

Based on the capacitances mentioned above, the equivalent inversion capacitance can be written as a series combination of the oxide capacitance, centroid capacitance and quantum capacitance, given by:

$$\frac{1}{C_{inv}} = \frac{t_{ox}}{\varepsilon_{ox}\varepsilon} + \frac{t_{cen}}{\varepsilon_s \varepsilon} + \frac{h^2}{4\pi m^* q^2}. \quad (2.23)$$

The effect of centroid and quantum capacitance is not prominent when the oxide capacitance is not scaled. However, it becomes more important when the value of oxide thickness approaches or is comparable to the value of the inversion layer thickness, especially in semiconductors with a smaller effective mass [2.31].

2.6. Channel properties

The potential of Tunnel-FET performance originates at the material level, from the channel band-to-band generation rate of effective mass and the energy band-gap. Compared with the Group IV materials shown in Fig. 2.11, III-V materials with low effective mass and energy band-gap seem to have the potential to obtain larger drive current for the applications of Tunnel-FET [2.28]. In addition, compound III-V materials feature adjustable energy gaps by changing the alloys composition, for example to achieve narrower band-gaps to increase the band-to-band tunneling generation rate. On the other hand, improving the other metric of off-current requires fewer defects in the channel and lower doping concentration in the drain region to minimize the ambipolar effect [2.33].

	Si	Ge	GaAs	InP	$In_{0.53}Ga_{0.47}As$	$In_{0.7}Ga_{0.3}As$	InAs
Lattice constant (Å)	5.431	5.658	5.653	5.869	5.869	5.937	6.058
Electron Effective Mass (m^*/m_0)	0.19	0.082	0.067	0.077	0.041	0.034	0.023
Electron Affinity (eV)	4.05	4	4.07	4.38	4.5	4.65	4.9
Bandgap (eV)	1.12	0.66	1.42	1.35	0.74	0.58	0.35
Hole Mobility (cm^2/V-s)	450	1900	400	150	300	400	460
Electron Mobility (cm^2/V-s)	1500	3900	8500	46800	12000	20000	33000

Table. 2.1. The material properties of Group IV and III-V for Tunnel-FETs application [2.34].

2.6.1. III-V materials

III-V materials are compounds composed of one element belonging to Group III atoms such as Al, Ga or In and the other element from Group V atoms like As, P, N or Sb. Most of these alloys are structured with zinc blende lattice, which is shown in Fig. 2.11. For the visualization of the zinc blende lattice, the structure is formed by two face-centred cubic (fcc) structures [2.16]. Also, it can be formed by two atoms belonging to each group, which are located at each point of the lattice [2.35]. The lattice constant of the crystal is determined by the edge distance of the cubic unit cell.

The covalent bond that results from the outer electrons of the atoms is the main force for the compound formation of III-V materials. Based on the Pauli principle, those electrons provided by Group III and Group IV atoms possess opposite spins. Due to thermal energy, some electrons have enough energy to escape from bond electrons. Then, these few escaped electrons result in the intrinsic carrier concentration [2.36]. Moreover, doping material with ionic atoms is a common technique to increase the carrier concentration (electrons or holes). The case of doping III-V compound semiconductors such as n-type dopant for InGaAs, for instance, involves using Si atom to replace In or Ga of Group III atom at the crystal lattice to obtain the additional electron, which can move in the crystal. The different doping concentration in the semiconductor decides the movement of the Fermi level, which represents the point at which there is a 50% probability of electron occupation at this energy level under a specific temperature (derived from the Fermi-Dirac distribution function). For undoped materials, the Fermi level lies in the mid-gap of the whole band-gap. The Fermi level moves toward the conduction band edge once the materials are doped by n-type dopant.

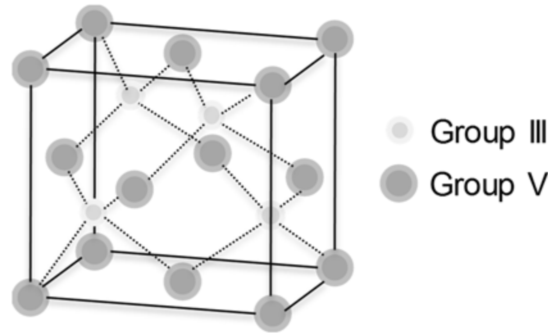


Fig. 2.11. Schematic diagram of zinc blende lattice.

Furthermore, the energy level can be plotted as a function of the wave vector to understand the material characteristics such as its direct or indirect band-gap. The benefit of direct band-gap materials for band-to-band tunneling is that there is less of an effect on phonon scattering [2.37], such as InGaAs, shown in Fig. 2.12. As the diagram shows, the band-to-band tunneling of electrons occur in the Γ valley. In addition, information on the effective mass of the electrons, which is affected by the periodic potential of atoms in free space, can be obtained by the curvature of the conduction band valley. The formula of effective mass as introduced in Equation (2.3), under the assumption of conduction valleys with a parabolic shape can be represented as [2.16]:

$$m_e^* = \hbar^2 \left(\frac{d^2E}{dk^2}\right)^{-1}. \tag{2.24}$$

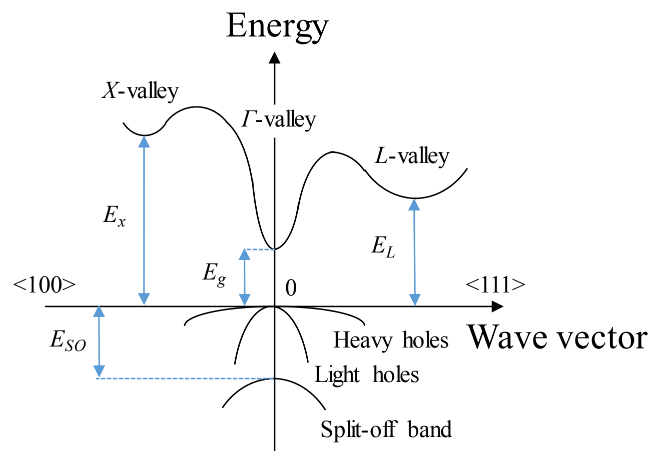


Fig. 2.12. Band structure of InGaAs; Eg = 0.74 ($In_{0.53}Ga_{0.47}As$) [2.38]; lower effective mass and higher effective mass are in the direction of Γ valley and L valley, respectively [2.16].

2.6.2. Material orientation

The III-V materials introduced in Section 2.6.1 are being considered for the n-channel transistors of future generations of CMOS technology due to their high electron velocities; In addition, non-planar architectures, such as FINFETs or nanowires, is very important to increase gate electrostatic control. Realising these devices with high performance requires a high quality metal-oxide-semiconductor interface on a variety of surface orientations especially (110) orientation. The reason is that the channel of these 3D logic devices on the vertical sidewall is dominated by (110)-orientated surfaces. These (110) surfaces lack Group V dimers and intrinsic surface defects compared to (100) surfaces due to a lack of homodimers and the relaxed bonding structure, whereas the Group V and the Group III atoms are left with filled dangling bonds in a near-tetrahedral sp3 geometry and empty dangling bonds in a near-planar sp2 geometry [2.39].

2.6.3. Band-to-band tunneling mechanism

As discussed in the previous Section 2.3, the operation of a Tunnel-FET utilises the quantum mechanical phenomenon of increasing gate bias to create the tunneling paths across the band-gap of a semiconductor for the realisation of electron band-to-band tunneling [2.40]. The related physical parameters include the BTBT current, derived from a closed form expression of the BTBT generation rate, and the tunneling probability, which is based on the Wentzel-Kramers-Brillouin (WKB) approximation [2.16].

2.6.3.1 BTBT generation rate

Regarding the tunneling phenomena, the formula of the BTBT current from a closed form expression of BTBT generation rate, based on the assumptions below, can be given by [2.41]:

$$G_{BTBT} = \frac{\sqrt{2m^*}q^2}{2\pi^3\hbar^2\sqrt{E_g}}\varepsilon^2 e^{-\left[\frac{\pi\sqrt{m^*}E_g^{\frac{3}{2}}}{2\sqrt{2}q\varepsilon\hbar}\right]}, \tag{2.25}$$

where the formula indicates the BTBT current is a function of the energy band-gap and the effective mass. Also, those underlying assumptions for the derivative of formula are included below [2.41],

(a) The closed form solution for band-to-band generation rate can be obtained based on the assumption that the semiconductor for band-to-band tunneling is a direct band-gap. Thus, the phonon scattering that would cause the momentum contribution can be neglected [2.42].

(b) The electric field across the tunnel junction is constant. [2.16].

(c) The Fermi levels of highly doped materials perfectly align with the valence band ($E_V = F_P$) of p-doped semiconductor materials and the conduction band ($E_C = F_N$) of n-doped semiconductors, respectively. Meanwhile, the valence band states should be fully occupied and the conduction band status entirely empty. Therefore, the Fermi distributions here are simplified [2.16].

(d) Symmetric 2-band relation is assumed for the model of the band-gap with regards to the imaginary wave vector dispersion relation [2.43]. Thus, the closed form, which shows the correct behaviour at the band edges, is allowed for the band-to-band tunneling generation rate [2.41].

2.6.3.2 Tunneling probability

Based on the WKB approximation, the tunneling probability can be written as [2.16];

$$T = e^{-2\left[\int_{x_1}^{x_2} k(x)dx\right]}, \tag{2.26}$$

where the classical tunneling path is from x_1 to x_2, as shown in Fig. 2.13, and $k(x)$ is the imaginary wave factor, based on the *E-k* relationship [2.16], which can be written as:

$$k(E_x) = \sqrt{\frac{2m^*}{\hbar^2}(E_x - U)}, \tag{2.27}$$

where E_x and U are respectively the energy of the incident carrier and the potential barrier height of the carriers shown in Fig. 2.13.

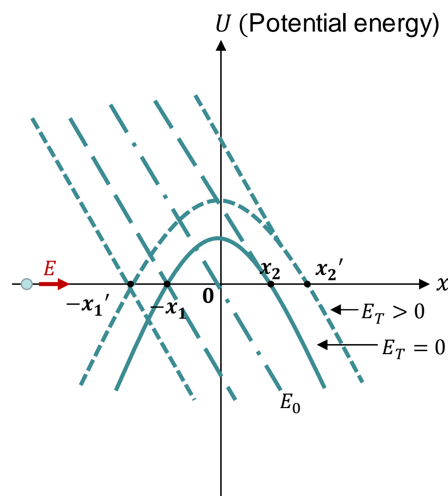


Fig. 2.13. Schematic diagram of parabolic potential barrier with transverse energy components E_T [2.16].

Furthermore, using the symmetric 2-band relation based on the assumption of uniform electric field within the tunnel junction and the boundary condition ($U = E_g/2\,, x = 0$), we can obtain the potential barrier height can be obtained [2.43]:

$$(E_x - U) = -2\left[\frac{\left(\frac{E_g}{2}\right)^2 - (q\varepsilon x)^2}{E_g}\right]. \tag{2.28}$$

Using the equation above and considering the momentum of incident electrons, including the transverse tunneling direction (E_T) [2.42], the tunneling probability can be expressed as:

$$T(E_x, E_T) = \exp\left[-2\int_{x_1'}^{x_2'} \sqrt{\frac{2m^*}{\hbar^2}\left[2\frac{\left(\frac{E_g}{2}\right)^2 - (q\varepsilon x)^2}{E_g} + E_T\right]}\, dx\right]. \tag{2.29}$$

Because the original path is limited by the integration of the formula with an extra damping factor in the wave function, the effective point barrier should be modified as the distance between x_1'and x_2' obtained below [2.43]:

$$2\frac{\left(\frac{E_g}{2}\right)^2 - (q\varepsilon x)^2}{E_g} + E_T = 0 \;\therefore\; x_{1,2} = \pm\frac{1}{q\varepsilon}\sqrt{\left[\left(\frac{E_g}{2}\right)^2 + \left(\frac{E_g E_T}{2}\right)\right]}. \tag{2.30}$$

The following coordinate transformation can help evaluate the integral in Equation 2.29 [2.43].

$$y = \frac{q\varepsilon}{\sqrt{\left[\left(\frac{E_g}{2}\right)^2 + \left(\frac{E_g E_T}{2}\right)\right]}}x. \tag{2.31}$$

Then, the tunneling probability based on the Equation 2.29 and 2.31 can be simplified as [2.43]:

$$T(E_x, E_T) = exp\left[-2\int_{-1}^{1}\sqrt{\frac{2m^*}{\hbar^2}}\left[\frac{\left(\frac{E_g}{2}\right)^2 + \left(\frac{E_g E_T}{2}\right)}{q\varepsilon\sqrt{E_g}}\sqrt{(1-y^2)}\right]dy\right]. \tag{2.32}$$

To obtain the simplified equation of tunneling probability in Equation 2.32, the integral can be written as [2.41]:

$$T(E_x, E_T) = \exp\left[-\frac{\pi\sqrt{m^*}\sqrt[3]{E_g}}{2\sqrt{2}q\varepsilon\hbar}\right] exp\left[-\frac{E_T}{\frac{\sqrt{2}q\varepsilon\hbar}{\pi\sqrt{m^* E_g}}}\right] = T_O \exp\left[-\frac{E_T}{E_O}\right]. \tag{2.33}$$

2.7 Esaki diodes

One signature phenomenon of Tunnel-FETs is that the electrical response exhibits negative resistance, which originates from the same current transport mechanism as that of the quantum Esaki tunneling diode (ETD) [2.44]. Similarly, the layer structure of two terminal ETDs consists of a sandwich structure consisting of heavily doped p-type layer, intrinsic layer and heavily doped n-type layer. The current-voltage characteristics correspond to ETD operation, are shown in Fig. 2.14. With zero applied bias in Fig. 2.14 (a), there is only a small current flowing through the ETD. During this time, there is still no obvious injection current under a small forward bias due to the high potential barrier before the current reaches the peak in Fig. 2.14 (b), where the energy of electrons in the conduction band is equal to that of empty states of holes in the valence band. As the applied forward bias is increased continuously, the tunneling current starts decreasing due to the reduced number of tunneling electrons in the conduction band. The noticeable forward current occurs due to the start of electron-hole injection after the tunneling current drops to zero in Fig. 2.14 (c). Furthermore, the current-voltage of ETD becomes similar to that of a regular p-n diode.

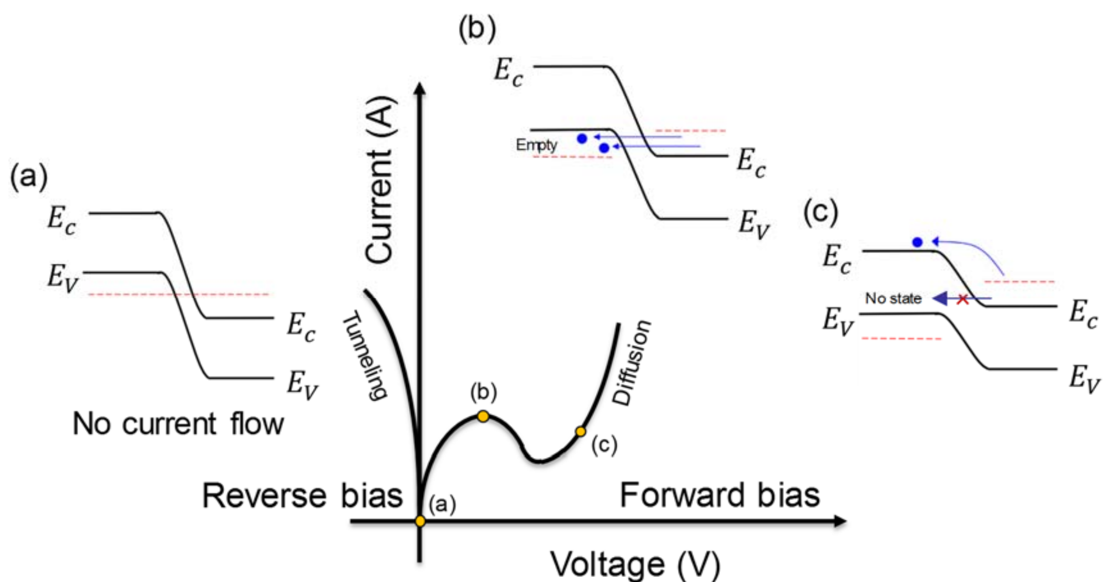


Fig. 2.14. Current-voltage characteristics of the Esaki tunneling diode (ETD) corresponding to the operation under conditions of (a) equilibrium, (b) peak tunneling current and (c) diffusion current.

2.8. Metal-semiconductor contacts

As discussed in the previous chapter about three terminal devices, DC performance may be limited by parasitic components such as parasitic series resistance related to the source and drain regions. Consider the effect of series resistance in a FET, the output characteristics based on the following equations can be separated into two situations, shown in Fig. 2.15, in which the drain-source and the gate-source drop access the intrinsic region and extrinsic region can be written as[2.45];

$$\boldsymbol{V_d = V_D + I_d(R_s + R_d)}, \tag{2.34}$$

$$\boldsymbol{V_g = V_G + I_d R_s}, \tag{2.35}$$

where V_G *and* V_g is the gate voltage dropped in the intrinsic region and extrinsic region, respectively. Also, V_D *and* V_d is the drain voltage dropped in the channel and in the actual terminals from source to drain.

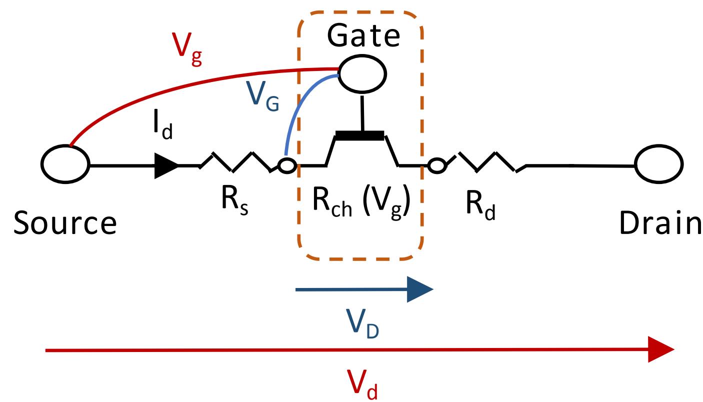


Fig. 2.15. Schematic diagram of equivalent circuit on a three-terminal device associated with source and drain series resistances.

The degradation of device performance associated with the series resistance becomes more dominant as the device continues scaling to smaller dimensions. One of the important impacts is the reduction of drain current and another impact is the drop of the output conductance in both linear region and saturation region of output characteristics, which causes the degradation of intrinsic gain dominated by R_{out} [2.46]. Therefore, decreasing the series resistance is expected to enhance the on-current of a channel scaled MOSFET when R_{on} is not influenced by R_{DS} [2.47]. On the other hand, the series resistance may have an impact on the measured transconductance. The extrinsic

transconductance (g_m), defined as $\frac{\partial I_d}{\partial V_g}$, can be expressed as a function of intrinsic transconductance (g_{mi}), defined as $\frac{\partial I_d}{\partial V_G}$ and the series resistance [2.45]:

$$g_m = \frac{g_{mi}}{1+g_{mi}R_s}. \qquad (2.36)$$

As the equation shown, the extrinsic conductance for the device may decrease significantly in the case of high series resistance. Meanwhile, the extrinsic transconductance becomes highly related to $1/R_s$ while $g_{mi}R_s \gg 1$. For three-terminal devices such as Tunnel-FETs, it is a requirement that the system has comparable Ohmic contact in the p-type and n-type region.

2.9. Chapter summary

This chapter has presented the background theory including basic III-V material properties, the semiconductor physics of key modules such as gate stack and Esaki diode and the principle of device operation that leads to the implementation of high performance power efficient Tunnel-FET.

2.10. Reference

[2.1] C. C. Hu, *Modern Semiconductor Devices for Integrated Circuits,* Upper Saddle River, New Jersey: Prentice Hall, 2010, pp. 213-217.

[2.2] E. O. Kane, "Zener Tunneling in Semiconductors", *Journal of Physics and Chemistry of Solids*, Vol. 12, pp. 181, 1959.

[2.3] E. O. Kane, "Theory of tunneling", *Journal of Applied Physics,* Vol. 32, pp. 83, 1961.

[2.4] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices,* New York: Cambridge University Press, 2009, pp. 164-165.

[2.5] S. M. Sze, *Physics of Semiconductor Devices*, 1st edn, John Wiley, 1969.

[2.6] H.-J. Cho et al., "Bulk Planar 20nm High-K/Metal Gate CMOS Technology Platform for Low Power and High Performance Applications", *IEEE International Electron Device Meeting*, 2011, pp. 350-353

[2.7] K. Ratnakumar, "Short-channel MOST threshold voltage model", *IEEE Journal of Solid-State Circuits*. 17, 937-948, 1982.

[2.8] Y. Byun, K. Lee, and M. Shur, "Unified charge control model and subthreshold current in heterostructure field effect transistors", *IEEE Electron Device Lett.*, EDL-11, 50–53; (see erratum (1990) IEEE Electron Device Lett., EDL-11, 273)

[2.9] J. L. Moll, *Physics of Semiconductors*, New York: McGraw-Hill, pp. 249-253, 1964.

[2.10] D. J. Griffiths, *Introduction for Quantum Mechanics,* Upper Saddle River, New Jersey: Prentice Hall, 2005.

[2.11] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-Subthreshold-Swing Tunnel Transistors", *IEEE Electron Device Letters*, 27, 297-300, 2006.

[2.12] U.E. Avci et al., "Study of TFET non-ideality effects for determination of geometry and defect density requirements for sub-60mV/dec Ge TFET", *Technical Digest - International Electron Devices Meeting, IEDM*. 2016-February, 34.5.1-34.5.4.

[2.13] R. N. Sajjad, W. Chern, J. L. Hoyt and D. A. Antoniadis, "Trap assisted tunneling and its effect on subthreshold swing of tunnel FETs", *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4380–4387, Nov. 2016.

[2.14] W. G. Vandenberghe, A. S. Verhulst, B. Soree, W. Magnus, G. Groeseneken, Q. Smets, M. Heyns, and M. V. Fischetti, "Figure of merit for and identification of sub-60 mV/decade devices", *Applied Physics Letters*, vol. 102, no. 1, p. 013510, 2013.

[2.15] T. Nirschl, et al., "The tunneling field-effect transistor (TFET) as an add-on for ultra-low voltage analog and digital processes", *IEDM Tech. Dig.,* Dec. 2004, pp. 195–198.

[2.16] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. Hoboken, New Jersey: Wiley, 2007, pp. 315.

[2.17] K. Boucart, and A. M. Ionescu, A new definition of threshold voltage in Tunnel FETs", *Solid-State Electronics,* 52, 1318-1323, 2008.

[2.18] R. Booth, M. White, H. Wong and T. Krutsick, "The effect of channel implants on MOS transistor characterization", *IEEE Trans Elec Dev*; ED-34:2501–9, 1987.

[2.19] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-k gate dielectric", *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725–1733, Jul. 2007.

[2.20] Q. SMETS et al., "Calibration of Bulk Trap-Assisted Tunneling and Shockley-Read-Hall Currents and Impact on InGaAs Tunnel-FETs", *IEEE Transactions on Electron Devices*. 64, 3622-3626, 2017.

[2.21] U.E. Avci et al., "Study of TFET non-ideality effects for determination of geometry and defect density requirements for sub-60mV/dec Ge TFET*", Technical Digest - International Electron Devices Meeting, IEDM. 2016-February*, 34.5.1-34.5.4.

[2.22] E. Nicollian and J. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New Jersey, NJ: Wiley, 2002, pp. 139, 130; 331.

[2.23] G. Brammertz, K. Martens, S. Sioncke, A. Delabie, M. Caymax, M. Meuris and M. Heyns, "Characteristic trapping lifetime and capacitance-voltage measurements of GaAs metaloxide-semiconductor structures", *Applied Physics Letters*, vol. 91, no. 13, p. 133510, 2007.

[2.24] B. Shin, J. R. Weber, R. D. Long, P. K. Hurley, C. G. V. de Walle, and P. C. McIntyre, Origin and passivation of fixed charge in atomic layer deposited aluminum oxide gate

insulators on chemically treated InGaAs substrates", *Applied Physics Letters,* vol. 96, no. 15, p. 152908, Apr. 2010. [Online]. Available: http://dx.doi.org/10.1063/1.3399776

[2.25] G. Brammertz, A. Alian, D.-C. Lin, M. Meuris, M. Caymax, and W. E. Wang, "A Combined Interface and Border Trap Model for High-Mobility Substrate MetalOxide-Semiconductor Devices Applied to $In_{0.53}Ga_{0.47}As$ and InP Capacitors. Electron Devices", *IEEE Transactions*, vol. 58, no. 11, p. 3890, Nov. 2011. [Online]. Available: http://dx.doi.org/10.1109/TED.2011.2165725

[2.26] Y. Yuan, L. Wang, B. Yu, , B. Shin, J. Ahn, P. C. McIntyre, P. Asbeck, M. J. W. Rodwell and Y. Taur, "A Distributed Model for Border Traps in Al_2O_3-InGaAs MOS Devices", *Electron Device Letters, IEEE*, vol. 32, no. 4, p. 485, Apr. 2011. [Online]. Available: http://dx.doi.org/10.1109/LED.2011.2105241

[2.27] K. Mistry et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging", *IEDM Electron Devices Meeting*, pp. 247-250, 2007.

[2.28] G. Dewey, et al., "Fabrication, characterization, and physics of III-V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing", *Technical Digest - International Electron Devices Meeting, IEDM.* 33.6.1-33.6.4, 2011.

[2.29] A. Alian et al. "InGaAs tunnel FET with sub-nanometer EOT and sub-60 mV/dec sub-threshold swing at room temperature", *Applied Physics Letters*. 109, 2016

[2.30] S. Takagi, and A. Toriumi, "Quantitative understanding of inversion-layer capacitance in Si MOSFET's", *IEEE Transactions on Electron Devices*, vol. 42, no. 12, pp. 2125-2130, 1995.

[2.31] P. K. Hurley, R. Long, T. O'Regan, E. O'Connor, S. Monaghan, V. Djara, M. A. Negara, A. O'Mahony, I. Povey, A. Blake, R. Nagle, D. O'Connell, M. Pemble and K. Cherkaoui, "Equivalent oxide thickness correction in the high-k/$In_{0.53}Ga_{0.47}As$/InP system", *ECS Transactions,* vol. 33, no. 3, pp. 433-444, 2010.

[2.32] S. Luryi, "Quantum capacitance devices", *Applied Physics Letters,* vol. 52, no. 6, pp. 501-503, 1988.

[2.33] J. Wu, and Y. Taur, "Reduction of TFET OFF-Current and Subthreshold Swing by Lightly Doped Drain", *IEEE Transactions on Electron Devices*, 63, 3342-3345, 2016.

[2.34] F. Xue, "III-V MOSFETs from planar to 3D", 2013. [Online]. Available: https://repositories.lib.utexas.edu/bitstream/handle/2152/21457/XUE-DISSERTATION 2013.pdf.

[2.35] M. Shur, *GaAs devices and circuits*, Plenum Press, New York, 1987.

[2.36] W. Liu, *Fundamentals of III-V Devices: HBTs, MESFETs and HFETs/HEMTs*, Willey, 1999.

[2.37] S. O. Koswatta, M. S. Lundstrom and D. E. Nikonov, "Influence of phonon scattering on the performance of p-i-n band-to-band tunneling transistors", *Applied Physics Letters*, 92, 043125, 2008.

[2.38] R. E. Nahory, M. A. Pollack, W. D. Johnston and R. L. Barns, Band gap versus composition and demonstration of Vegard's law for In1−xGaxAsyP1−y lattice matched to InP", *Applied Physics Letters*, 33, 659-661, 1978.

[2.39] T. J. Kent, Passivation of Interface Defects on GaAs and InGaAs (001) and (110) Surfaces and Improvement of Low Temperature HfO_2 ALD Nucleation", 2015. [Online]. Available: http://wwwlib.umi.com/cr/fullcit?p3716547.

[2.40] W. M. Reddick and G. A. J. Amaratunga, "Silicon Surface Tunnel Transistor", *Applied Physics Letter*, Vol. 67, 1995, pp. 494-496, 1995.

[2.41] S. H. Kim, "Germanium-Source Tunnel Field Effect Transistors for Ultra-Low Power Digital Logic", 2012. [Online]. Available: http://digitalassets.lib.berkeley.edu/etd/ucb/text/Kim_berkeley_0028E_12473.pdf.

[2.42] J. L. Moll, *Physics of Semiconductors*, New York: McGraw-Hill, pp. 249-253, 1964.

[2.43] C. Kittel, *Introduction to Solid State Physics,* Hoboken, New Jersey: Wiley, pp. 317, 1971.

[2.44] L. Esaki, "New Phenomenon in Narrow Germanium p − n Junctions", *Physical Review*, 109, 603-604, 1958.

[2.45] S. Chou and D. Antoniadis, "Relationship between measured and intrinsic transconductances of FET's. Electron Devices", *IEEE Transactions*, vol. 34, no. 2, pp. 448-450, 1987.

[2.46] D. Jiménez, B. Iñíguez, J. Suñé and J. J. Sáenz, Analog performance of the nanoscale double-gate metal-oxide-semiconductor field-effect-transistor near the ultimate scaling limits", *Journal of Applied Physics*, 96, 5271-5276, 2004.

[2.47] A. Ali, H. Madan, R. Misra, E. Hwang, A. Agrawal, I. Ramirez, P. Schiffer, T. Jackson, S. E. Mohney, J. B. Boos, B. Bennett, I. Geppert, M. Eizenberg and S. Datta, "Advanced composite high-k gate stack for mixed anion arsenide-antimonide quantum well transistors", *IEEE International Electron Devices Meeting (IEDM) Technical Digest*, 2010, pp. 134-137, 2010.

III. Fabrication Techniques

3.1. Introduction

In this chapter, various techniques are introduced for Tunnel-FET device realisation and vertical nanowire Tunnel-FET fabrication; namely e-beam lithography for device patterning (especially important in the mask definition for the vertical nanowire); the etching process for pattern transfer via the patterned mask defined by e-beam lithography; atomic layer deposition (ALD) for dielectric layer deposition of MOSCAP; and the lift-off and metallisation process for gate, source and drain metal contact. Most importantly, the use of a cluster tool will be described for in-situ gate stack formation after inductively coupled plasma etching for non-planar device realisation. This in-situ gate stack fabrication on etched InGaAs material and the integration of these developed modules for vertical nanowire Tunnel-FET will be described in detail in Chapter V.

3.2. Material growth

The substrate material plays one of the most important roles for device realisation. As mentioned in Chapter II, this work mainly focuses on III-V compound semiconductors, especially various compositions of the $In_xGa_{1-x}As$ alloy ($x = 0.53\sim1$) due to the feasibility of heterostructure formation. The band-gap of the $In_xGa_{1-x}As$ alloy decreases when increasing the percentage of Indium as shown in Figure 3.1. Therefore, using InAs as the channel of Tunnel-FET tends to enhance the tunneling current, as discussed in Section 2.6.

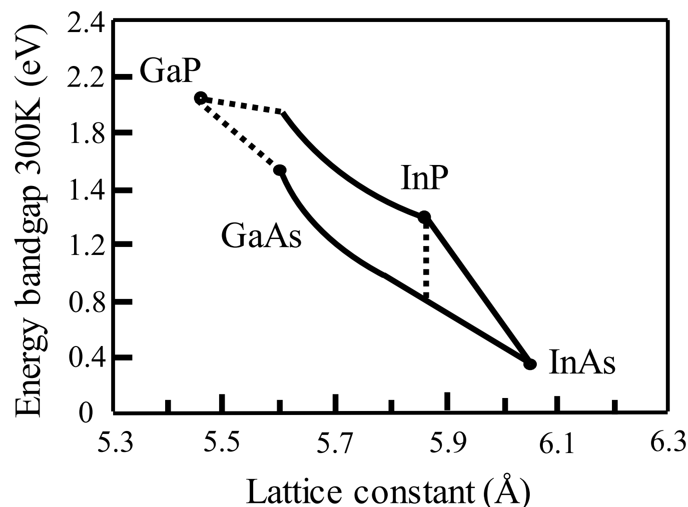


Fig. 3.1. Plot of the energy gap vs. lattice constant for InGaAsP family [3.1].

The lattice mismatch between $In_{0.53}Ga_{0.47}As$ [3.2] and InAs [3.2] is approximately 0.19 Å (~3.1%) whilst $In_{0.53}Ga_{0.47}As$ and InP have similar lattice constants [3.3], therefore the InAs layer grown on InP will relax once the thickness of InAs thin film is above 5nm. In addition, the critical thickness of $In_{0.7}Ga_{0.3}As$ on InP is around 10nm. Both of hese are shown in Fig 3.2.

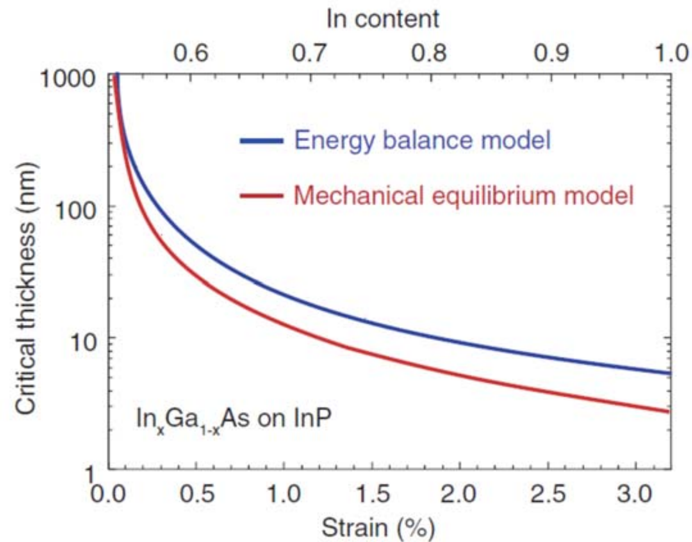


Fig. 3.2. Relationship of the calculated critical thickness vs. strain of an InGaAs layer grown on an InP substrate [3.4].

One of the most common epitaxy tools for III-V compound semiconductor growth is Molecular Beam Epitaxy (MBE) [3.5], which enables the growth of different doped or undoped semiconductor layers using high purity molecular beams under the condition of ultra-high vacuum (~10^{-8} Pa) in the process chamber. The growth technique of MBE can provide accurate doping levels and precise layer thickness and alloy composition of III-V compounds. Therefore, all the epitaxy of materials in this work on the heterostructure of Tunnel-FET and all other modules, such as InGaAs MOSCAPs, are grown using the MBE technique.

3.3. Cluster tool

The cluster tool in the James Watt Nanofabrication Centre (JWNC), shown in Fig. 3.3, provides a unique device fabrication capability for specific key modules without any impact of air exposure, which may cause issues at the interface of materials, resulting in device degradation, especially in nanoscale III-V compound semiconductor devices.

Clustering inductively coupled plasma (ICP) etching and atomic layer deposition (ALD) techniques is the most important breakthrough in this work to accomplish the in-situ ALD dielectric layer deposition on a top-down vertical nanowire device etched by ICP RIE via transfer system, under vacuum, and mitigating the etch damage through in-situ plasma gas pre-treatment in this work, which will be described in Chapter V.

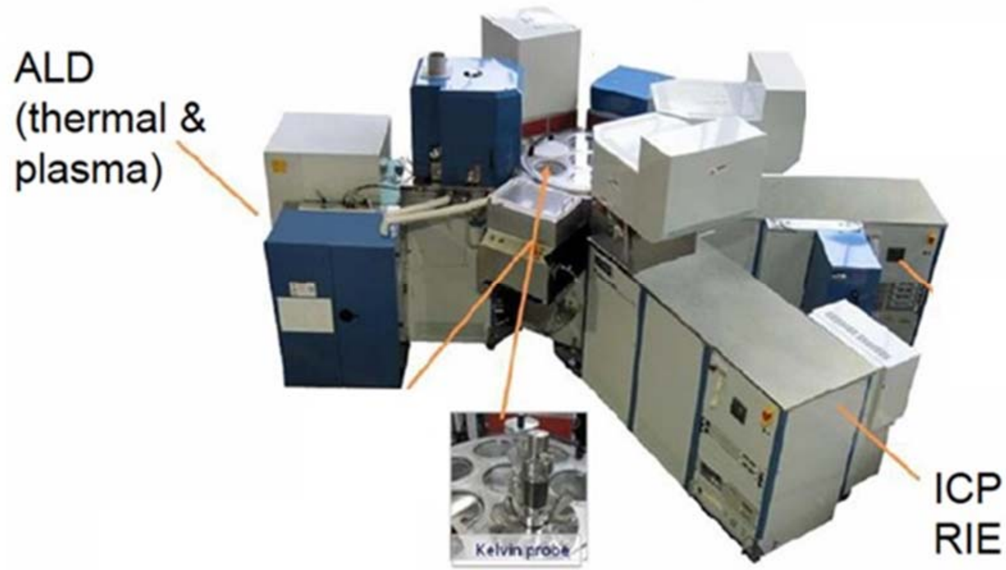


Fig. 3.3. Cluster tool.

3.3.1. Atomic Layer Deposition (ALD)

Among all technologies developed over last 30 years, ALD has become one of the most important methods for thin film deposition due to its many advantages, such as precise thickness control, excellent step coverage, highly conformal deposition and high-quality films (pinhole-free) with negligible stress [3.6]. Furthermore, ALD growth at low temperature (<400°C) suits the requirement of III-V processing. The concept of ALD is a cyclic process based on a self-terminating reaction mechanism [3.7]. Each cycle comprises four sequential steps shown below [3.8],

1. Pulse the first precursor gas into the chamber for surface chemisorption.
2. Purge the chamber to remove the excess gases.
3. Pulse the second precursor which reacts with the first precursor.
4. Purge the chamber for the removal of excess gases.

Compared with other CVD processes, the ideal case of ALD growth will not be influenced by the precursor pulse length, pressure and temperature, but there are many critical issues in practical ALD, such as precursor choice and the optimal growth temperature. As a key element for ALD process, a good precursor should meet certain conditions: first, the precursor must contain the characteristics of high reactivity without self-reacting to the initial surface and subsequent layer with the existing precursor; second, the precursor must be thermally stable apart from a sufficient volatility above a certain temperature, with a consistent growth rate. The oxidants of the precursor reaction for the deposition of metal-oxide [3.9] and metal-nitride [3.10] are water/plasma, O_2/ozone and NH_3, respectively. Constant growth rate can only be obtained within the ALD temperature window shown in Fig. 3.4. The diagram of the relations between ALD deposition rate and temperature indicates that there might be an insufficient reaction rate at the surface, resulting in slower growth rate when the temperature is too low. Meanwhile, the higher growth rate at low temperature means that physiosorption of precursor occurs at the surface. The growth rate at elevated temperature will also become faster or slower due to precursor decomposition or desorption from the surface, respectively. Most importantly the initial surface of the substrate must enable the precursor to chemically react to the surface; then, all the circumstances for ALD process that were mentioned above will happen.

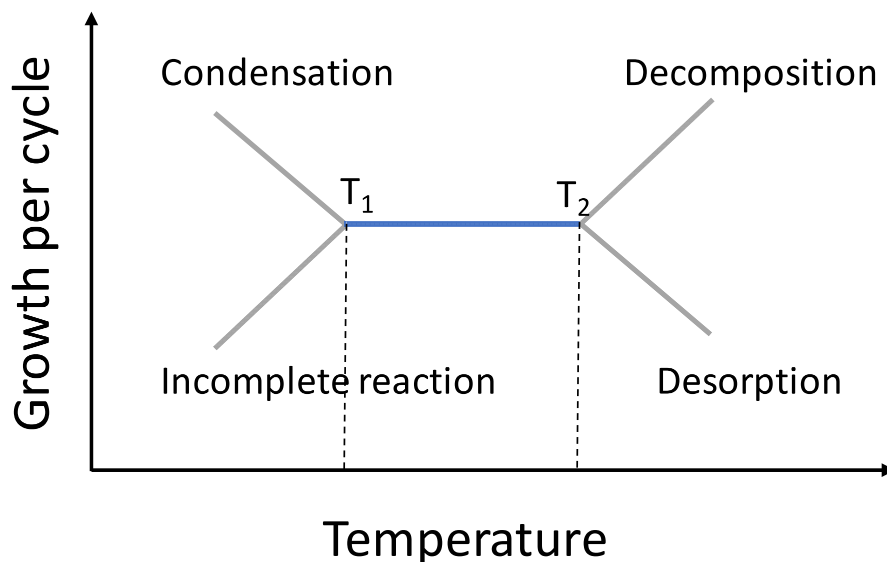
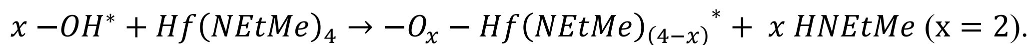


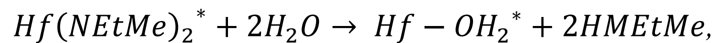
Fig 3.4. Schematic diagram of an ALD process window (blue line) in which the growth rate is situated [3.11].

The stepwise ALD growth process of well-established HfO_2 deposition on a substrate containing hydroxyl (OH) groups can be demonstrated using the precursors of tetrakis(ethylmethylamide)hafnium {TEMAH; $Hf[N(CH_3)(C_2H_5)]_4$ or $Hf(NEtMe)_4$}and water (H_2O), as shown in Fig. 3.5. First, the temperature on the substrate surface is stabilised via heat treatment, followed by an injection of heated gas-phase TEMAH molecules into the chamber for surface chemisorption; then, TEMAH reacts with the OH ligands on the substrate, which results in the formation of Hf-O bonds in the first half of the reaction described by [3.12]:



$$x - OH^{*} + Hf(NEtMe)_4 \rightarrow -O_x - Hf(NEtMe)_{(4-x)}{}^{*} + \ x\ HNEtMe \ (\mathrm{x} = 2).$$

where the symbols * and x are surface species and the number of hydroxyl groups reacting per $Hf(NEtMe)_4$, respectively. Prior to moving to the second half reaction, the excess gases containing with the unreacted precursor molecules and reaction by-products are evacuated by a purge process in the chamber. The second half-cycle initially starts at the injection of H_2O precursor for the reaction of the $(NEtMe)$-terminated surface, described by [3.12]:



$$Hf(NEtMe)_2{}^{*} + 2H_2O \rightarrow \ Hf - OH_2{}^{*} + 2HMEtMe,$$

Similar to the first half-cycle, a purge is also carried out to remove all the excess gases in the chamber, and the top surface is left with OH-terminated bonds [3.12]. Overall, this is one cycle of ALD growth with one monolayer created by HfO_2 deposition. The desired film thickness during deposition can be decided by tuning the number of repeated cycles.

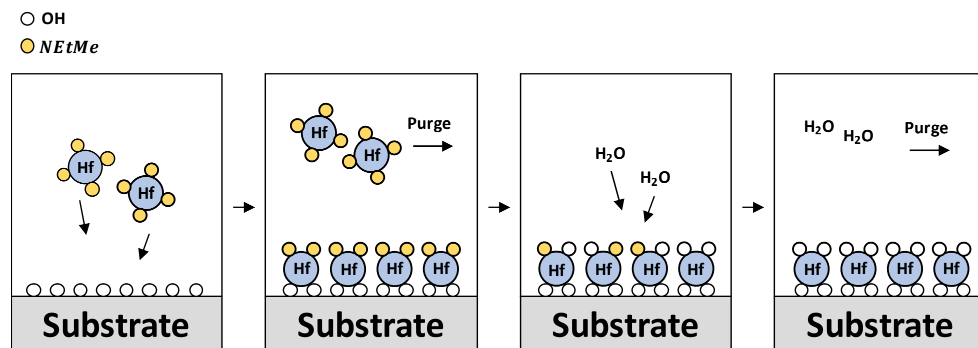


Fig. 3.5. The schematic diagram of an ALD growth cycle of HfO_2 deposition via the sequential reactions of precursor TEMAH and H_2O on an OH-terminated substrate surface.

3.3.2. ICP dry etch

Dry etching refers to the material removed by using a plasma chemistry. It is commonly applied for desired pattern transfer with an etching mask required for the fabrication of nanowires with high aspect ratio features and precise etching depth. The realisation of anisotropic etching profile is done using the methods of chemical etching, chemical passivation and physical bombardment in one of the common dry etching techniques, reactive ion etching (RIE), as shown in Fig. 3.6. By applying the RF power between two electroplates, the plasma is generated (composed of mixed chemical species of electrons, ions and neutral radicals) and the functionality of RF sources enables isolation of the energetic radicals from heavy ions and accelerates the ions toward to the sample surface. The etching properties—such as the etching rate, smoothness of sidewalls or the formation of isotropic, diagonal or vertical of sidewalls—are influenced by many parameters including the ratio of multiple gases, the selection of gas composition, the chamber pressure and power levels for plasma gas generation. The processing temperature and the etching depth can be obtained through laser interferometric techniques by observing the intensity oscillations that result from the superposition of beams with separated phases [3.13].

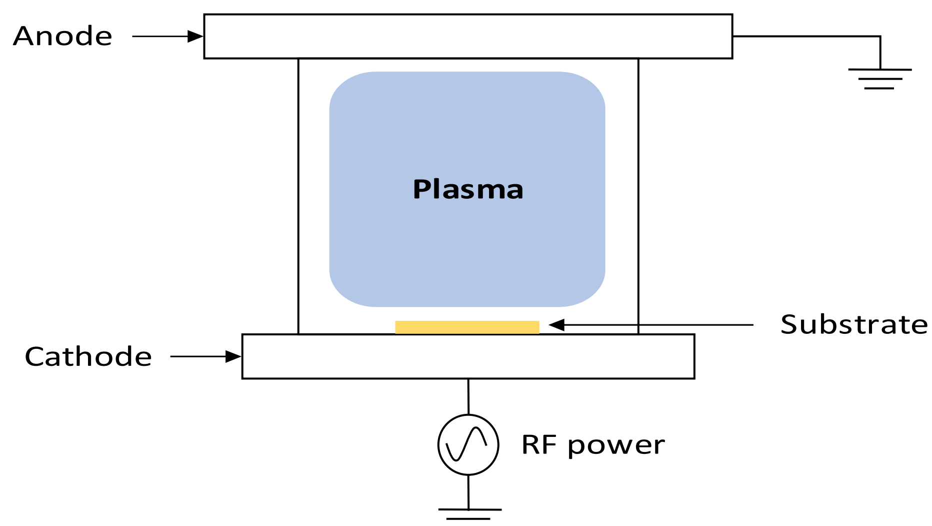


Fig. 3.6. Schematic diagram of a reactive ion etching (RIE) tool.

According to the etching mechanism, the anisotropic profile with lower selectivity is formed by physical sputtering, that is, using high acceleration voltages to gain more energetic ions. In addition, the chemical reactions with low ion energies would only result

in an isotropic sidewall profile with higher selectivity. Therefore, the anisotropic profile with higher selectivity can be achieved by combining both mechanisms of dry etching. However, the sputtering mechanism, with its violent reactions between energetic ions and surface, may cause dislocations in the lattice that can propagate deeper in the substrate. Therefore, the area covered by the resist mask, which would vanish more quickly prior to the end of the process due to the sputtering of the sample surface, should be further protected by increasing the thickness of resist mask. In addition, the damage of undesired etching into the area uncovered by the resist should be minimised.

3.4 Electron beam lithography

For feature sizes smaller than 20 nm, optical lithography through masks seems challenging when the requirements of throughput and resolution must be met at the same time [3.14]. From a research perspective, choosing a suitable processing technology that contains high resolution and accurate alignment is required in this work. The direct writing approach, such as electron beam lithography (EBL), utilises software mask to generate patterns efficiently via a computer system that reads the layout files. Compared with photolithography, the advantage of this technology is that it can avoid some issues such as the latitude of changing the resulting patterns, the inconvenience of modifying patterns/processes and the defects that cause degradation of the patterns.

The process of e-beam lithography involves spinning e-beam resists, exposing the e-beam resists for the desired pattern without masks and then developing the written patterns. There are a few factors that determine the resolution, accuracy and reliability of pattern definition in EBL. First, the resolution is influenced by the spot size of the e-beam, which is strongly related to the backscattering of the electron-resist and electron-substrate interaction during exposure. In addition, some parameters have profound effects on the resolution of pattern definition, such as the substrate material, e-beam resists and the specific developers used, and these should be also considered. Moreover, the achievable resolution of optical lithography, which is referred to as the minimum feature size, is limited by the diffraction of light, as shown in Fig, 3.7, but an e-beam lithography process during operation is not limited by the light diffraction due to the smaller de Broglie wavelength of an electron beam (about 4-12 pm at accelerating voltages of 10-100 kV). On the other hand, the accuracy of aligning a desired pattern to the other existing defined one relies on the e-beam alignment technique, which will be briefly introduced in the following sections.

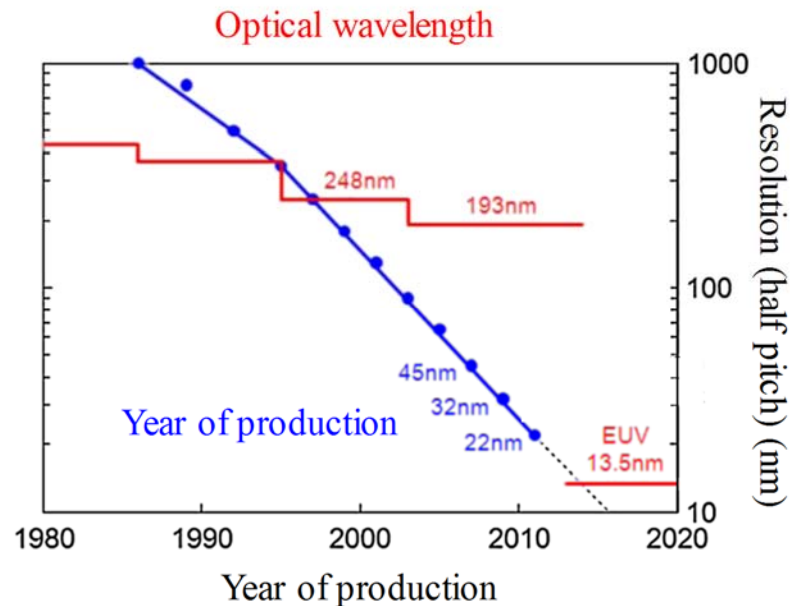


Fig. 3.7. The evolution of lithography tool resolution with the scaled wavelength of the light source [3.15].

3.4.1. Apparatus and operation of e-beam lithography tool

In this work, a Vistec VB6 Ultra High Resolution Extra Wide Field (UHR EWF) e-beam lithography tool placed in a Class 10 cleanroom of James Watt Nanofabrication Centre at University of Glasgow is utilized. The schematic diagram shown in Figure 3.8, the tool is composed of the electron-optical column (EOC), detector electronics, support system and pattern generator. The EOC, which is the core part of VB6 tool, provides the function of a direct electron beam generation and the control of beam intensity, focus and deflection to obtain a desired spot size on the substrate at the bottom-tier. The suppressor electrode first limits the electrons emitted by the cathode tip, followed by a high electric field between the cathode to increase the level of electron energy, which typically is 50 kV or 100 kV. The extractor excites these electrons and a last electrode focuses the beam below the anode before the accelerated electrons are emitted from the gun. In the middle of the electron-optical column, there are two deflection coils performing the function of tilting and shifting, which help align the electron beam with the optical axis of the system. In addition, the electrostatic lens C1 and the magnetic lens C2 control the stability of the focus point and the current density before the beam exits the lens C2. On the other hand, the blanking cell functionalises by switching the on/off state of the beam by diverging the beam from the optical axis to avoid the angular deflection interrupted by an aperture. The other blanker, known as the conjugate beam blanker, can ensure that the increase of

blanker voltage to the point of the beam swathing off is independent of the beam position so that beam movement would not cause any issue of unintended exposure on the substrate. The dose that is exposed on the resist is determined by the current density and the duration of exposure time and is corrected by the adjustment of the blanking cell. The final stage before the beam is assigned to the resist on the substrate is using the magnetic lens C3 to focus the beam. Higher resolutions of exposure require increasing the usable beam current but also require a longer dwell time, thereby decreasing throughput.

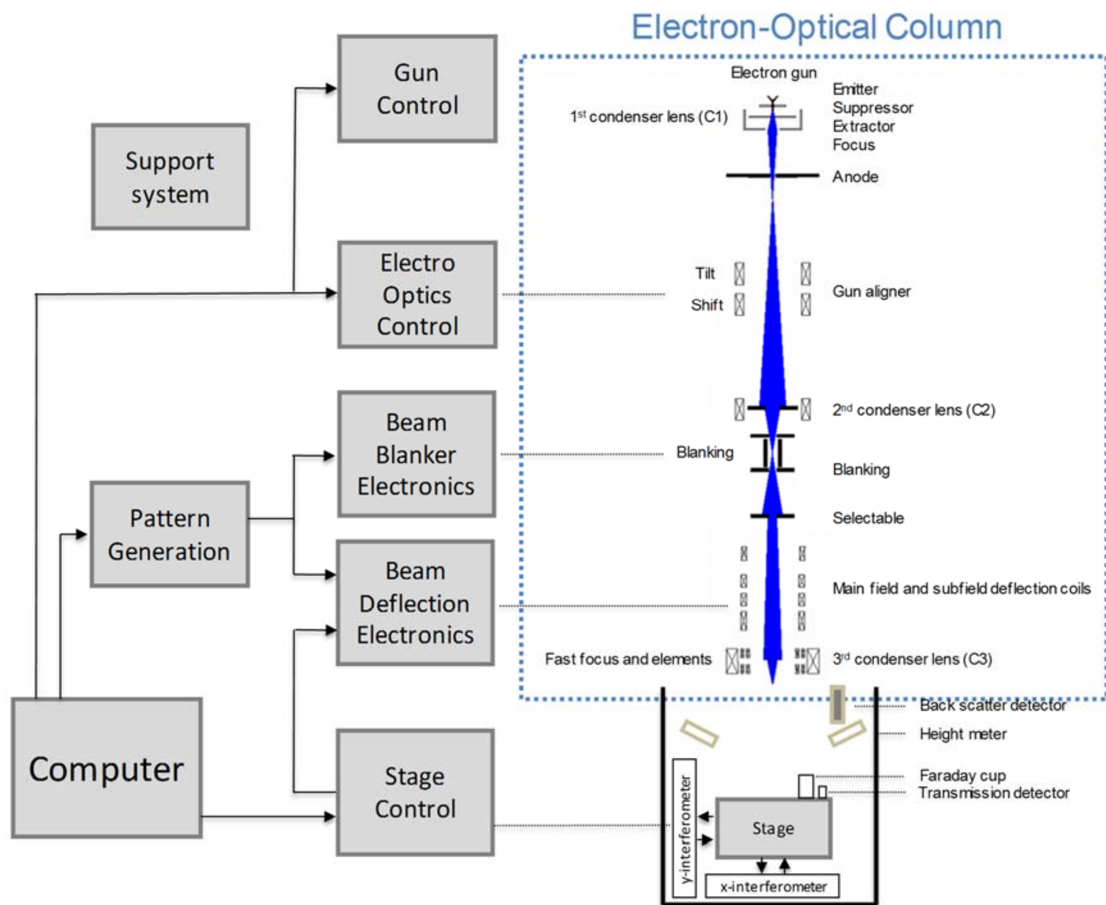


Fig. 3.8. Schematic diagram of the Vistec VB6 UHR EWF e-beam lithography system [3.16].

The steps of the EBL technique for pattern exposure involves the formation of the beam, setting the size and current of the beam and locating the beam at the intended position on the substrate. Then the main field is provided by the main field deflection coils, which perform further angular deflections, resulting in increased aberrations and a restricted maximum distance of beam deflections. Therefore, the main fields are divided by the

fracturing software with 64 x 64 subfields. Also, the large angles of deflection limit the speed of beam writing. Subfield deflections within a main field provided by subfield deflection coils can have faster writing due to smaller angular deflections. Exposure sequence is realised by moving the beam to the centre of each subfield, followed by subfield deflection, which scans the beam over each pixel within the total area of the subfield and then repeats the writing process on all subfields within each main field. Higher resolution corresponds to decreased size of the main field and the related subfields. Also, the distance between two areas in a desired pattern, known as the product of variable resolution unit (VRU) and the resolution, shown in Fig. 3.9, is kept as small as possible to ensure continued exposure in the desired area.

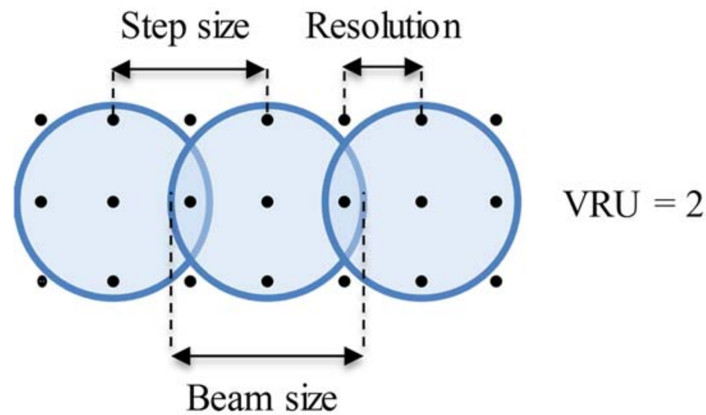


Fig. 3.9. The stepping of the beam spot, which is equal to the product of the VRU and the resolution for pattern writing.

3.4.2. Scattering

One of the most important factors that limit the resolution of feature size is the scattering phenomena when the beam impinges on and penetrates into the resist-coated substrate. This results in both elastic and inelastic scattering from electron-nucleus interaction and electron-electron interactions, respectively. The secondary electrons that are generated from the excitation and ionisation of atoms arise due to inelastic scattering. Although low energy secondary electrons (a few tens of eV) are only concerned with the several nm range of lateral straggle from the excitation and ionisation of atoms, the much higher one (a few keV) may increase in large numbers. Therefore, the secondary electron contribution is important because the obtained energy distribution (exposure) in the resist is determined by the inelastic scattering [3.17]. In addition, the inelastic scattering, which

comes along with the small-angle deflection, is known as the forward scattering, which produces a beam of incident electrons that gets broader laterally with a Gaussian distribution [3.18]. On the other hand, the secondary scattering occurs when the primary electron reaches the interface of resist and substrate. This effect results in some electrons penetrating over the interface in various depths and the other electrons elastically scattering back with large angle, known as the back scattering. Thus, this will lead to undesired resist exposure when the scattered electron travels back away from the original point of e-beam incidence [3.19]. The trend of the forward scattering distribution, which tends to be narrower, is opposite to that of back scattering, in which the distribution becomes wider. Thus, the overall energy distribution profile, known as the point spread function (PSF), is comprised of both scattering mechanisms, as shown in Fig. 3.10.

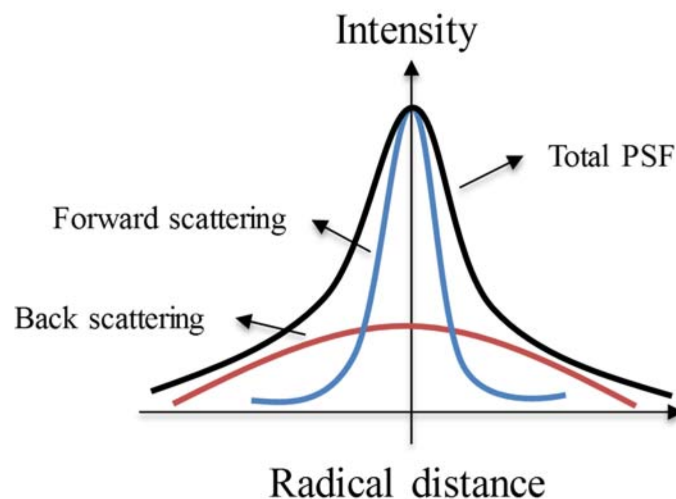


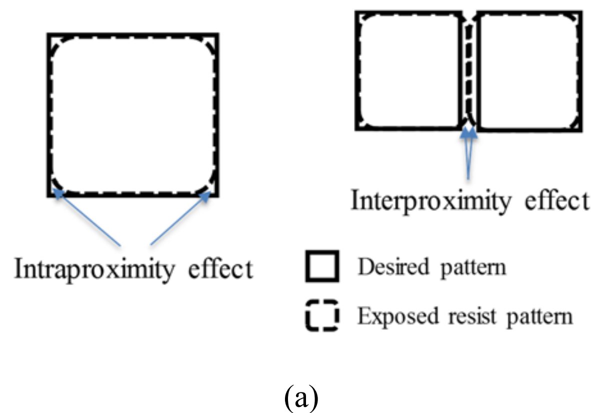
Fig. 3.10. Schematic diagram of the total Gaussian energy distribution, known as the point spread function (PSF), compared to contributions from both forward scattering and back scattering.

In general, the effect of PSF on the resist profile, which results from the contribution of both scattering, is highly dependent on conditions such as the substrate materials, the thickness of resists and the incident energy of the electron beam [3.20]. The exposure profile resulting from the penetration of electron beams with high acceleration voltage gives a wider range to the backscattered area. The thinner resist layer can reduce scattering effects on the beam size and decrease the chance of losing energy during the process of electron incidence. Compared with silicon, a material with higher atomic

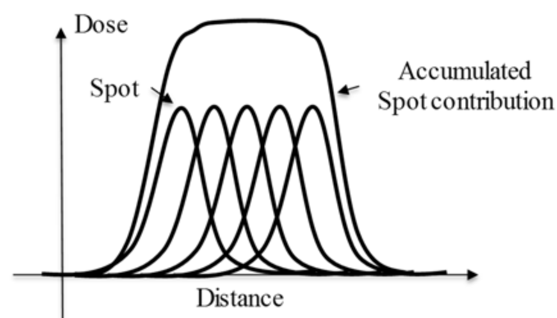
number such as GaAs results in increased scattering probability and intensity but decreased range of back scattering [3.20, 3.17].

3.4.3. The proximity effect

This section introduces an additional effect that induces pattern distortion after back scattering, known as the proximity effect. The effect is comprised of intra-proximity and inter-proximity effects, as shown in Fig.3.11 (a), which separately cause the non-uniform exposure at the edge of a single pattern and the gaps between patterns due to accumulation from each spot contributing a Gaussian distribution from the centre to the edge of a pattern element in Fig. 3.11(b), respectively. This leads to higher electron dose at the centre but reduced dose around the edge [3.21,3.22]. As a result, a large geometry or a high density of patterns gives rise to overexposure, in contrast to smaller or isolated patterns. Therefore, considering how to minimize both effects for well-defined and distributed features is important for the fabrication of high resolution and density patterns.



(a)



(b)

Fig. 3.11. Schematic diagram of (a) pattern distortion due to the proximity effect and due to (b) the accumulated electron dose.

One of the ways to compensate for the proximity effect is adopting corrective action with software. Also, the effect can be minimized by following the design rules governing the proximity effects on patterned geometries and gaps or inserting a thicker intermediate layer with low density characteristics between the resist and the substrate.

3.4.4. Resist

In addition to the effect of e-beam exposure on resist, achieving high resolution pattern definition also requires a good resist, especially one with low sensitivity and high contrast [3.20]. From a process perspective on pattern definition, the parameters of exposure dose and e-beam energy should be considered. Apart from that, it is also important to manage development for resist dissolution, taking into account temperature, time, resist thickness, resist molecular weight and exposure dose [3.20, 3.23].

There are a few ways to minimize the sensitivity, including: thinner resists, high electron beam exposure and lower density substrate with less dense patterns, [3.23] or using the resist with higher molecular weight to slow the dissolution rate in a longer process duration. In contrast, high temperature, which speeds the dissolution rate of the resist, could increase sensitivity. According to process contrast, both the strength and selection of the developer would change the resolution. Therefore, the optimization of the developing process to define a new pattern requires a dose test that gives a different dose to a series of identical patterns.

In this work, most resists used for the lift-off process is poly-methyl methacrylate (PMMA), a positive tone resist. The advantage of using PMMA is that the resist features the characteristics of high resolution (~5 nm). In addition, the other advantage of using this ebeam resist is its wide selection of molecular weight, which allows users to adjust sensitivity by increasing or decreasing molecular weight [3.20]. Therefore, PMMA is a low sensitive resist that can be used simultaneously onto multilayers in the lift-off process. At the same time, different diluted ratios of Methyl isobutyl ketone(MIBK)/Isopropyl Alcohol(IPA) for the development of exposed patterns give different levels of contrast and resolution. Lower ratios, such as 1:3, provide higher contrast and lower sensitivity, which enables extremely high resolution. In contrast, pure MIBK delivers poor resolution, which results from low contrast and high sensitivity [3.20]. On the other hand, hydrogen silsesquioxane (HSQ), which is composed of silicon dioxide with Si-H bonds, a negative tone resist, is used for sub-10 nm nanowire patterning. The principle for resist exposure relies on breaking the Si-H bonds to generate crosslinking in the HSQ layer [3.24]. Tetramethylammonium hydroxide (TMAH) is commonly used for development.

3.4.5. Alignment

Each device fabrication requires the integration of several processes on a desired substrate. Thus, the registration marker definition is important at the beginning to ensure the accurate alignment of multiple layers for each process. For instance, the misalignment between gate, source and drain for a device may cause issues with device performance. In this work, a two-stage alignment is adopted to circumvent the increased positional uncertainties between the separations of markers. As shown in Fig 3.12, the first stage uses a global marker located at the corner of the whole sample for normal alignment. Then, the use of cell markers with a smaller marker grid, which are placed around the smaller area of the desired region, can enhance the alignment accuracy. The marker used in this work consists of gold-free metal and is fabricated by a metal lift-off process, which will be introduced in Section 3.5. Triple layers of Ti (15nm)/Pt (30 nm) are made with e-beam metallisation to form global and cell markers that can be easily detected with the e-beam lithography tool. In general, high contrast is related to the thickness of marker and the material of the metal markers and semiconductor substrate.

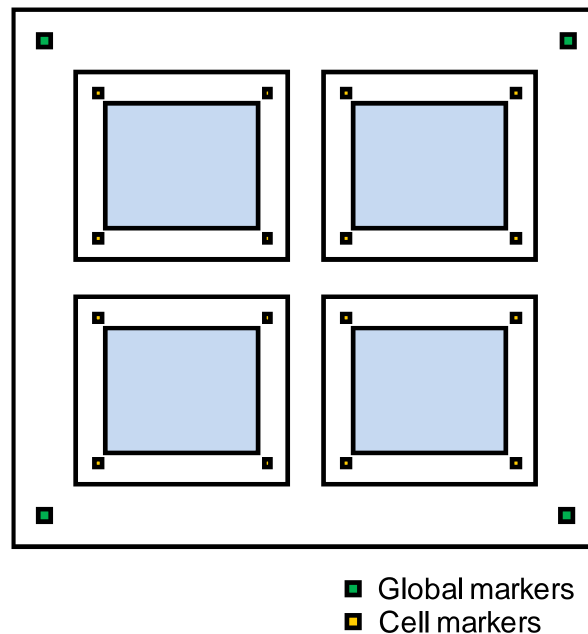


Fig. 3.12. Schematic diagram of the global and cell markers for alignment.

3.5. Metallisation and lift-off

Most processes steps require metallisation for metal contacts on the device or the modules, including alignment markers, gate pads, drain/source contacts and bond pads. Achieving

these processes with patterned definition requires the use of lithography with lift-off, as shown in Fig. 3.13 and the key strategy to obtain the precise patterns from e-beam exposure is using bi-layer resist with different dissolution rates. Most importantly, the resist with the higher molecular weight (related to higher sensitivity) should be set on the top. First, desired patterns are defined by using the e-beam to expose the bi-layer resist. Then, the resist is developed to remove the exposed regions and the metal is placed in an ultra-high vacuum environment that allows for e-beam metallisation to cover the whole surface. Afterward, the lift-off process involves putting the sample in pre-warmed acetone (~50°C) to dissolve the rest of the resist to remove any residual metal.

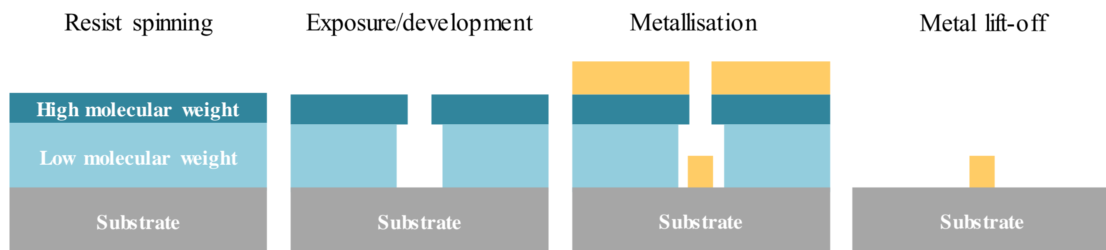


Fig. 3.13. The general metal lift-off process with pattern exposure/development, metallisation and lift-off activities.

3.6. Chapter summary

In this chapter, the general fabrication techniques for the realisation of III-V Tunnel-FETs are introduced. The importance of e-beam lithography in this work for the nanoscale nanowire patterning was described. Most importantly, the cluster tool based on ICP etch and atomic layer deposition were strongly emphasized due to their unique capability of realising in-situ dielectric layer formation on etched sidewalls of non-planar devices. In addition, the effectiveness of plasma gas pre-treatment to minimize the etching damage on the sidewalls of device channels has important implications for this work, and these will be discussed in the next chapter.

3.7. Reference

[3.1] R. E. Nahory, M. A. Pollack, W. D. Johnson Jr and R. L. Barns, "The electro-optic applications of InP", *Journal of Crystal Growth,* 54 , pp. 1-8, 1981.

[3.2] S. Adachi, “Lattice thermal resistivity of III–V compound alloys”, *Journal of Applied Physics*, 54, 1844-1848, 1983.

[3.3] E. Kuphal, “Phase Diagrams of InGaAsP, InGaAs and InP Lattice-Matched to (100) InP”, *Journal of Crystal Growth,* 67, pp. 441-457, 1984.

[3.4] T. Sato, M. Mitsuhara and Y. Kondo, “InAs quantum-well distributed feedback lasers emitting at 2.3m for gas sensing applications”, *NTT Tech. Rev*., vol. 7, pp. 1–7, 2009.

[3.5] A. Y. Cho and J. R. Arthur, “Molecular beam epitaxy”, *Progress in solid-state chemistry*, vol. 10, Part 3, pp. 157-191, 1975.

[3.6] S. M. George, “Atomic Layer Deposition: An Overview”, *Chemical Reviews*, 110, 111-131, 2010.

[3.7] A. Foroughi-Abari and K. Cadien, “Atomic layer deposition for nanotechnology”, In: *Nanofabrication*, M. Stepanova and S. Dew, Eds. Springer Vienna, 2012, pp. 143-161, 2012.

[3.8] J. Kim and T. Kim, “Initial surface reactions of atomic layer deposition”, *MRS Proceedings*, vol. 61, pp. 17-22, 2009.

[3.9] M. Leskela and M. Ritala, “Atomic layer deposition (ALD): from precursors to thin film structures”, *Thin Solid Films.* 409, 138, 2002.

[3.10] H. Kim, “Atomic layer deposition of metal and nitride thin films: Current research efforts and applications for semiconductor device processing”, *J. Vac. Sci. Technol*. B, *21*, 2231, 2003.

[3.11] J. S Ponraj, G. Attolini and M. Bosi, “Review on Atomic Layer Deposition and Applications of Oxide Thin Films”, *Critical Reviews in Solid State and Material Sciences*, 38, 203-233, 2013.

[3.12] W. Chen, Q.Q. Sun, M. Xu, S.J. Ding, D.W. Zhang and L.K. Wang, ”Atomic layer deposition of hafnium oxide from tetrakis(ethylmethyamino)-hafnium and water precursors”, *J. Phys. Chem. C*, 111, 6495-6499, 2007.

[3.13] P. Hariharan, *Basics of Interferometry*, Elsevier Inc, 2007.

[3.14] B.J. Lin, “Making lithography work for the 7-nm node and beyond in overlay accuracy, resolution, defect, and cost”, *Microelectronic Engineering.* 143, 91-101, 2015.

[3.15] M. L. Rieger, Communication theory in optical lithography”, *Journal of Micro/Nanolithography, MEMS, and MOEMS*. 11, 013003, 2012.

[3.16] *Vectorbeam Operator Manual*, Leica Microsystems.

[3.17] J. N. Helbert, *Electron-beam ULSI applications, in Handbook of VLSI Microlithography*, W. Andrew, Ed. London, 2001, pp. 670-755.

[3.18] G. Wiederrecht, *Handbook of Nanofabrication*. Chapter 4, Elsevier, 2010.

[3.19] C. S. Wu, Y. Makiuchi and C. Chen, *High-energy electron beam lithography for nanoscale fabrication. In: Lithography*, Wang, M., Ed. InTech, 2010, pp. 241-266.

[3.20] Z. Cui and Z. Cui, "Nanofabrication by charged beams", In: *Nanofabrication*, Springer US, 2008, pp. 77-127.

[3.21] L. Ren and B. Chen, "Proximity effect in electron beam lithography", In: *International Conference on Solid-State and Integrated Circuits Technology Proceedings,* vol. 1, 2004, pp.579-582.

[3.22] T. H. P. Chang, "Proximity effect in electron beam lithography", *Journal of Vacuum Science and Technology*, vol. 12, no. 6, pp. 1271-1275, 1975.

[3.23] M. Mohammad, M. Muhammad, S. Dew and M. Stepanova, "Fundamentals of electron beam exposure and development", In: *Nanofabrication*, Eds. Springer Vienna, 2012, pp. 11-41.

[3-24] S. Rivzi, *Handbook of Photomask Manufacturing Technology*. CRC Press, pp. 327-335, 2005.

IV. Overview of Tunnel-FETs

Scaling of transistors have driven CMOS integrated circuits industry in last two decades by the evolution of advanced lithography, exploration of thin-film technology and realisation of non-planar device configurations [4.1]. However, scaling gradually slows down and the power issues rise for technology nodes below 10nm [4.2]. Beyond this generation, it is a challenge to maintain performance with supply voltages below 0.5V, which is desirable to reduce power consumption. Therefore, numerous approaches for low power devices have been discussed and benchmarked, for instance Ferroelectric [4.3], Spin torque [4.4], Magneto electric [4.5] and Tunneling devices [4.6]. Of these, this work focuses on Tunnel-FETs, starting by reviewing the state of the art for this kind of device, followed by going through the current progress with some key factors that can enhance the performance of device, and then further discussing the challenge of realising a high quality device. Finally, the benchmark of Tunnel-FET on a variety of materials, based on planar and non-planar architectures, such as nanowires will be given to pave the path of Tunnel-FET development.

4.1 Tunnel-FETs technology to date

Due to the limitations of thermalionic emission, the subthreshold sing of conventional transistors are limited to 60meV at room temperature, as discussed in Section 2.4.1. From the equations governing device operation in the subthreshold region, it is notable that the operational mechanism of band-to-band tunneling seems potentially to be one of the solutions to overcome this restriction. Tunnel-FETs comprise two key modules i) the tunneling junction and ii) the gate stack, as described in chapter II. Struetzer [4.7] firstly investigate a transistor containing the basic component of a Tunnel-FET in 1952 by applying a field electrode to a p-n junction to demonstrate ambipolar current-voltage device characteristics with different gating conditions. By narrowing the depletion region between the junction between heavily doped p- and n-type germanium, Esaki report the first tunneling diode named as the Esaki diode exhibiting the characteristics of negative differential resistance (NDR) which enables the decrease of diode current with respect to the increase of gate voltage [4.8]. In 1977, Quinn introduced this idea into the current n-channel transistors with the replacement of the doping on source region from n-type to p-type to accomplish the lateral configuration of Tunnel-FETs [4.9]. After the first vertical device was proposed by Leburton [4.10], the aim was

to fabricate a high-speed transistor using the gate controllability of NDR characteristics. The first observation of NDR characteristics at room temperature using the proposed surface tunnel transistor (STT), named by Baba, was reported by Uermura and Baba in GaAs in 1994 [4.11]. Continuously, numerous research focus on boosting the devices on silicon and compound materials. High performance of TFETs with the current density over 1mA/um^2 has been demonstrated on the system of InGaAs/InP [4.12]. On the other hand, the subthreshold-slope has initially been discussed and considered by many groups with experimental results or analytical modelling [4.13]. Of these, analytical expression shows the way to realise the device with the subthreshold swing less than 60mV/decade by applying the gate control on the internal field of tunnel junction and the overlapping region of band-to-band tunnel. Over last decades, the most encouraging results firstly demonstrated by Intel accomplishing the n-channel device with the subthreshold swing less than 60mV/decade on $In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ heterojunction grown on the InP due to its narrow bandgap and low effective mass [4.14]. The advantage of broken bandgap hetero-junctions can offer the high Tunnel-FETs drive current and achieve low subthreshold swing at the same time.

4.2 Figure of merit for Tunnel-FET development

Figures of merit to evaluate Tunnel-FET were introduced in Section 2.4. The solution to realise high quality Tunnel-FETs that can compete with current MOSFETs in terms of drive current and subthreshold swing are mostly determined by material junction and gate stack engineering. Higher drive current Tunnel-FETs, accomplished by modulating the energy bandgap of III-V materials, has been widely demonstrated [4.15]. For instance, one of the best results on drive current for III-V based Tunnel-FETs is realised on GaSb/InAs hetero-structure materials with broken energy bandgap compared to homogeneous junction (InGaAs/InAs), as mentioned in Section 4.1. By the observation of temperature independence of subthreshold characteristics on Tunnel-FETs, the degradation of subthreshold swing results from the leakage floor influenced by the aforementioned trap-assist-tunneling (TAT) mechanism [4.16]. Furthermore, ultimately scaling gate stack on III-V materials are also being reported as a key factor to deliver a subthreshold swing of sub-60mV [4.17]. Therefore, realising a sub-nm level gate stack with low interface defect density between dielectric layer and III-V semiconductors can possibility offer steeper sub-threshold swing Tunnel-FETs.

4.3 Introduction of Tunnel-FET configuration

The interest of Tunnel-FET configuration on III-V materials arise from manufacturability perspective, especially for process feasibility and device scalability. To date, most configurations originate at point-Tunnel-FETs [4.18], and line-Tunnel-FET [4.19], as shown in Fig. 4.1. (a) and (b), respectively. For the configuration of the point-Tunnel-FET, based on the common p-i-n layer structure, the gate metal overlaps only the intrinsic region, in which the tunneling is occurring close to the joint region of source, intrinsic region and gate oxide [4.18]. In this device, the drive current is strongly dependent on the oxide thickness and the gated device width, which is perpendicular to the current direction [4.19]. The configuration of the line-Tunnel-FET, also named as the gate normal Tunnel-FET, has the gate metal overlapping only on the source region, in which the strengthen of band bending for band-to-band tunneling can increase by scaling the distances between gate and source. Furthermore, a thin n-doped layer or n-doped pocket can be inserted between the p-doped region and intrinsic layer on both aforementioned point Tunnel-FET and line Tunnel-FET to increase the electric field for higher drive current, as shown in Fig. 4.1 (c) and (d), respectively.

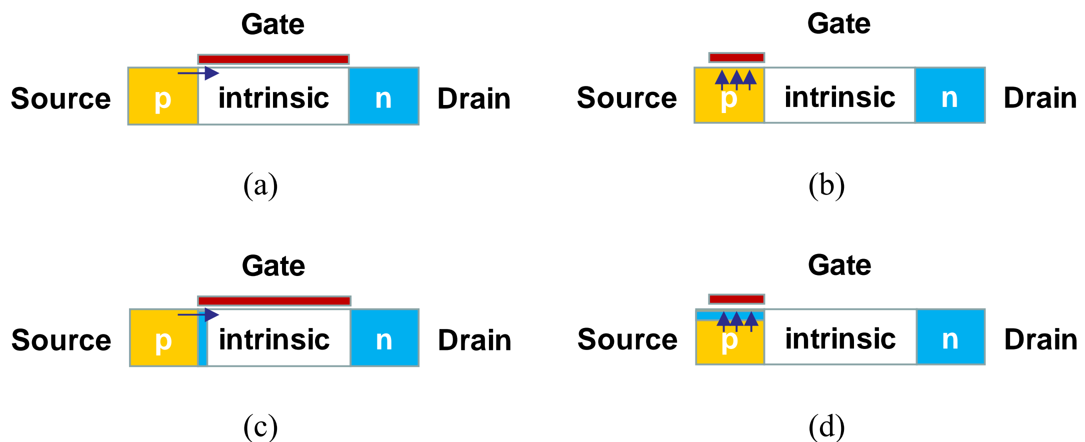


Fig. 4.1. The Tunnel-FET configuration of (a) point Tunnel-FET, (b) line Tunnel-FET, (c) pocketed point Tunnel-FET and (d) pocketed line Tunnel-FET based on different gate position and doped regions.

Of these, considering the issue of gate alignment, a mixed point- and line-Tunnel-FET is adopted for III-V Tunnel-FETs to minimize the variation and complexity of device fabrication by covering all the region of source, intrinsic layer and drain. Even though an overlapping drain may result in additional tunneling current, the leakage current can be minimized by lowering the doping concentration in the drain [4.20].

4.4 Potential issue of experimental III-V Tunnel-FETs

As mentioned in Section 4.2, realising high performance III-V Tunnel-FETs requires an ultimately scaled gate stack with low interface defect density on III-V materials. In addition, the exploration of the most suitable configuration for Tunnel-FET is important. Even though a few planar III-V Tunnel-FETs, based on the mixed point- and line-Tunnel-FET configuration, have achieved the sub-60mV/decade subthreshold characteristics, the current architecture such as FinFETs may be challenged to suit these configurations of Tunnel-FETs, especially the device fabricated with the homojunction or heterojunction of multi III-V epitaxy layers grown by Molecular Beam Epitaxy (MBE), unless the bottom-up or top-down approach, as known as vertical device integration, is utilized. Therefore, a Tunnel-FET may require a pillar-based architecture fabricated through bottom up or top-down fabrication. The bottom-up method uses the concept of molecular self-assembly to produce devices, whereas the top-down method achieves the desired structure by using externally control tools such as the lithography and dry etching tools, as mentioned in Chapter III.

This work mainly focuses on the top-down approach. One of the key challenges to realise a high quality pillar-based III-V Tunnel-FET especially for low subthreshold swing is obtaining clean etched surfaces on the sidewall of vertical nanowire with low surface roughness and the formation of an ultimate scaled gate stack on the etched sidewall with low interface defect density which contributes the leakage current floor, as introduced in Section 4.2. To date, it is still challenging to minimize the interface defect density of III-V gate stacks such as InGaAs MOSCAP below to 10^{12} $cm^{-2}eV^{-1}$ which results in poor subthreshold swing of most experimental III-V Tunnel-FET [4.21], supported by the temperature dependence of subthreshold characteristics [4.22]. Although the ex-situ wet etching such as sulphur passivation prior to ALD can effectively remove the native oxide at the interface for cleaning surface preparation, it is difficult to avoid the native oxide re-growth due to air exposure of the sample. Therefore, a cluster tool based ICP etch and in-situ ALD is developed in this thesis to fabricate the gate stack on the sidewall of vertical nanowire to avoid the formation of native oxide. Furthermore, plasma gas pre-treatment is utilized to mitigate the degradation of MOSCAP quality due to etching damage.

4.5 Homojunction and Heterojunction modulation

Due to the direct bandgap of III-V materials without phonon scattering, there is an advantage in providing higher possibility of band-to-band tunneling which results in larger drive current on Tunnel-FETs [4.23]. The other benefit of III-V materials enables

narrowing the energy bandgap via modulating the ratio of compound semiconductor for homojunction or the formation of broken bandgap between conduction band and valence band through two different compound semiconductors with less lattice mismatch such as the heterojunction of GaSb/InAs, on which the current highest drive current of Tunnel-FET can be achieved around 310uA/um at V_{DS}=0.5V [4.24]. Also, the benchmarking of published work for Tunnel-FETs are show in Table. 4.1.

Material	Configuration	EOT (nm)	V_{GS} (V)	V_{DS}(V)	SS_{min} (mV/dec)	$I_{SS,min}$ (uA/um)	I_{ON} (V_{DS}=0.3V) (uA/um)	I_{ON}/I_{OFF}
$In_{0.53}Ga_{0.47}As$ [4.25]	Planar	1.4	1	0.15	64	10^{-4}	4	$>10^{6}$
$In_{0.53}Ga_{0.47}As$ [4.17]	Planar	0.8	1	0.5	<60	10^{-4}	5	$\sim10^{5}$
$In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As$ [4.26]	Planar	0.8	2	1	80	10^{-2}	~7	$>10^{4}$
$In_{0.53}Ga_{0.47}As/InAs$ [4.14]	Planar	1.1	0.8	0.05	<60	10^{-3}	4	$\sim10^{3}$
$In_{0.53}Ga_{0.47}As/InAs$ [4.27]	Vertical nanowire	1.5	0.3	0.3	<60	5×10^{-4}	0.5	$>10^{4}$
InAs/GaAsSb/GaSb [4.28]	Vertical nanowire	1.4	0.05	0.3	<60	3.1×10^{-2}	3	$>10^{4}$

Table 4.1 Benchmarking of Tunnel-FETs fabricated of III-V in planar and vertical geometry.

4.6 Chapter summary

The key factors, which enables performing a high quality Tunnel-FET, have been highlighted including the aspect of gate stacks, layer structure and device configuration, which will pave the way to realise a promising transistors for low power CMOS application.

4.7 Reference

[4.1] C.-H. Jan, et al., "A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications", *Technical Digest - International Electron Devices Meeting, IEDM*. 3.1.1-3.1.4, 2012.

[4.2] E. 1. Nowak, Maintaining the Benefit of CMOS Scaling when Scaling Bogs Down", *IBM Journal of R&D*, vol. 46, iss. 2, pp. 169-180, 2002.

[4.3] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices", *Nano Lett.,* vol. 8, no. 2, pp. 405–410, 2008.

[4.4] D. E. Nikonov and G. I. Bourianoff, "Spin gain transistor in ferromagnetic semiconductors-the semiconductor Bloch-equations approach", *IEEE Trans. Nanotechnol*., vol. 4, no. 2, pp. 206–214, Mar. 2005.

[4.5] D. E. Nikonov and I. A. Young, Benchmarking spintronic logic devices based on magnetoelectric oxides", *J. Mater. Res.,* vol. 29, no. 18, pp. 2109–2115, Sep. 2014.

[4.6] A. Biswas and M. A. Ionescu, "Tunnel Field Effect Transistors: from Steep-Slope Electronic Switches to Energy Efficient Logic Applications", Lausanne, EPFL, 2015.

[4.7] O. M. Stuetzer, "Junction fieldistors", *Proc. IRE*, vol. 40, no. 11, pp. 1377–1381, Nov. 1952.

[4.8] L. Esaki, "New phenomenon in narrow germanium p-n junctions", *Phys. Rev*., vol. 109, no. 2, pp. 603–604, 1958.

[4.9] J. Quinn, G. Kawamoto and B. McCombe, "Subband spectroscopy by surface channel tunneling", *Surface Sci*., vol. 73, no. 1, pp. 190–196, 1978.

[4.10] J. P. Leburton, J. Kolodzey and S. Biggs, "Bipolar tunneling field-effect transistor: A three-terminal negative differential resistance device for high-speed applications", *Appl. Phys. Lett.,* vol. 52, no. 9, pp. 1608–1620, May 1988.

[4.11] T. Uemura and T. Baba, "First observation of negative differential resistance in surface tunnel transistors", *Jpn. J. Appl. Phys*., vol. 33, pp. L207–L210, 1994.

[4.12] T. Kopp and J. Mannhart, "Calculation of the capacitances of conductors--Perspectives for the optimization of electronic devices", *J. Appl. Phys*., vol. 106, art. 064504, Sep. 2009.

[4.13] Q. Zhang, W. Zhao and A. Seabaugh, "Analytic expression and approach for low subthreshold-swing tunnel transistors", In: *Device Res. Conf. Dig*., pp. 161–162, 2005.

[4.14] G. Dewey, et al., "Fabrication, characterization, and physics of III-V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing", *Technical Digest - International Electron Devices Meeting, IEDM*. 33.6.1-33.6.4, 2011.

[4.15] R. Pandey et al., "Demonstration of p-type $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ and n-type $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ complimentary Heterojunction Vertical Tunnel FETs for ultra-low power logic", *Digest of Technical Papers - Symposium on VLSI Technology*. 2015-August, T206-T207.

[4.16] R.N. Sajjad, W. Chern, J.L. Hoyt and D.A. Antoniadis, "Trap Assisted Tunneling and Its Effect on Subthreshold Swing of Tunnel FETs", *IEEE Transactions on Electron Devices.* 63, 4380-4387, 2016.

[4.17] A. Alian, et al. "InGaAs tunnel FET with sub-nanometer EOT and sub-60 mV/dec sub-threshold swing at room temperature", *Applied Physics Letters*. 109, 2016.

[4.18] P. F. Wang, "Complementary tunneling-fets (CTFET) in CMOS technology", Ph.D. dissertation. PhD thesis, Technische Universitat Munchen, 2003.

[4.19] D. Verreck, A. S. Verhulst, K.-h. Kao, W. G. Vandenberghe, K. De Meyer and G. Groeseneken, "Quantum Mechanical Performance Predictions of p-n-i-n Versus Pocketed Line Tunnel Field-Effect Transistors", *IEEE Transactions on Electron Devices*, vol. 60, pp. 2128–2134, Jul 2013.

[4.20] J. Wu, Y. Taur, “Reduction of TFET off-current and subthreshold swing by lightly doped drain”, *IEEE Transactions on Electron Devices*, vol. 63, pp. 3342-3345, Aug 2016.

[4.21] U.E. Avci et al., “Study of TFET non-ideality effects for determination of geometry and defect density requirements for sub-60mV/dec Ge TFET”, *Technical Digest - International Electron Devices Meeting, IEDM.* 2016-February, 34.5.1-34.5.4.

[4.22] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan and S. Datta, “Temperature-Dependent I-V Characteristics of a Vertical $In_{0.53}Ga_{0.47}As$ Tunnel FET”, *IEEE Electron Device Letters* , 31, 564, 2010.

[4.23] S. O. Koswatta, M. S. Lundstrom and D. E. Nikonov ,”Influence of phonon scattering on the performance of p-i-n band-to-band tunneling transistors”, *Applied Physics Letters*. 92, 043125, 2008.

[4.24] A.W. Dey, B.M. Borg, B. Ganjipour, M. Ek, K.A. Dick, E. Lind, C. Thelander and L.-E. Wernersson, “High-current GaSb/InAs (Sb) nanowire tunnel field-effect transistors”, *IEEE Electron Device Lett*. 34, 211-213, 2013.

[4.25] M. Noguchi, S. H, Kim, M. Yokoyama, O. Ichikawa, T, Osada, M, Hata, M. Takenaka and S. Takagi, “High Ion/Ioff and low subthreshold slope planar-type InGaAs tunnel field effect transistors with Zn-diffused source junctions”, *J. Appl. Phys*., vol. 118, art. 045712, July. 2015.

[4.26] A F. Xue, “III-V MOSFETs from planar to 3D”, 2013. [Online]. Available: https://repositories.lib.utexas.edu/bitstream/handle/2152/21457/XUE-DISSERTATION 2013.pdf.

[4.27] X. Zhao, A. Vardi, and J. A. Del Alamo, “ Sub-thermal Subthreshold Characteristics in Top-down InGaAs/InAs Heterojunction Vertical Nanowire Tunnel FETs,” *IEEE Electron Device Letters.* VOL. 38, NO. 7, pp. 858-865, 2017.

[4.28] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, “Vertical InAs/GaAsSb/GaSb tunneling fieldeffect transistor on Si with S=48 mV/decade and Ion=10 μA/μm for Ioff =1 nA/μm at Vds=0.3 V,” in *IEDM Tech. Dig*., Dec. 2016, pp. 500–503.

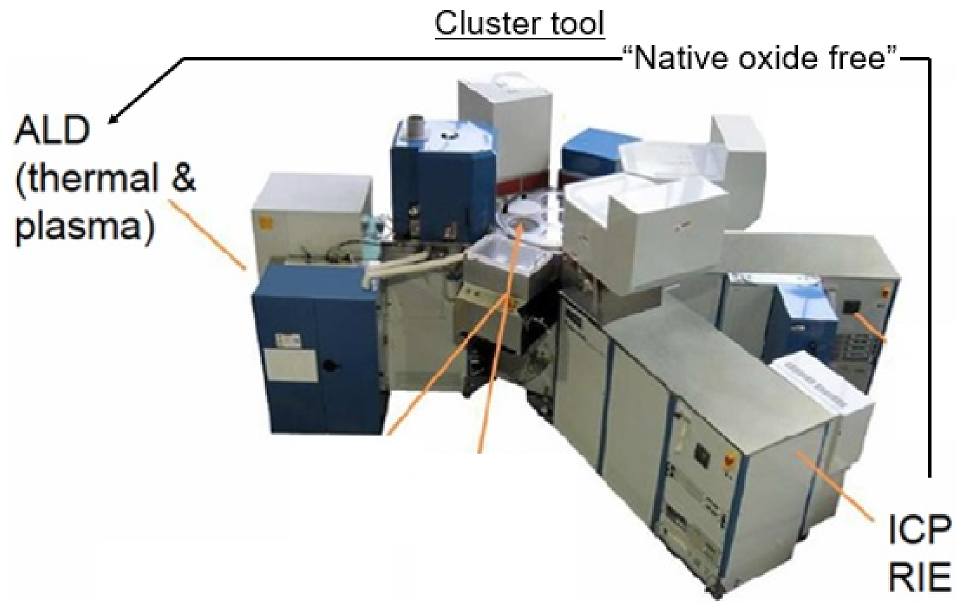
V. Process Development & Characterisation Metrology

5.1 Introduction

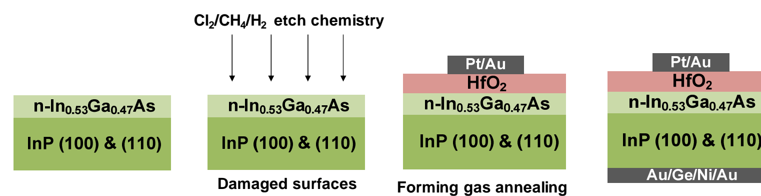
High performance III-V Tunnel-FETs require high quality modules for device integration, in addition to hetero-structure substrates. A key aspect is developing a high quality gate stack on different orientations of InGaAs for non-planar device configurations. To realise defect-free methods and to move away from wet cleaning processes such as the common method of ammonia sulphur passivation for native oxide removal, the cluster tool mentioned in Section 3.3 provides an innovative strategy, i.e. clustering ICP etching and ALD deposition to fulfil native oxide free in-situ MOS capacitors (MOSCAPs). In addition, the functionality of the cluster tool enables incorporated plasma gas pre-treatment prior to ALD deposition for the mitigation of etch damage caused by ICP etch. The following sections will present the integration of nanowire etch and gate stack fabrication modules via an in-situ process for the device fabrication of Tunnel-FETs with both planar and non-planar configurations.

5.2 Clustering ICP etching and in-situ ALD process of MOSCAPs

From a manufacturing perspective regarding the realisation of non-planar Tunnel-FETs, there is a desire for no wet chemical cleans/passivation treatments in the process flow. In spite of sulphur passivation delivering one of the best electrical results on InGaAs MOSCAPs in a variety of orientations, the duration of transferring the sulphur passivated sample to ALD chamber may impact gate stack performance due to undesired air exposure for the sample. In Fig. 5.1(a), clustering ICP etch and ALD tools offers the benefit of preventing native oxide formation on etched surfaces and the ability to perform a sequence of processes to form highly anisotropic structures, all in a controlled environment. In previous work, inductively coupled plasma (ICP) etching in a $Cl_2/CH_4/H_2$ based chemistry has been demonstrated to achieve nearly vertical InGaAs sidewall profiles [5.1]. In this section, the cluster tool is used to form gate stacks on plasma etched InGaAs surfaces with both (100) and (110) orientations. Fig. 5.1(b) shows the schematic diagram of the in-situ MOSCAP fabrication on both etched InGaAs (100)- and (110)-oriented surfaces.



(a)



(b)

Fig. 5.1 (a) Clustering ICP etch and ALD deposition of in-situ MOSCAP fabrication and (b) the schematic diagram of gate stack formation on (100) and (110) orientation of etched InGaAs surfaces.

5.2.1 Plasma H_2 or plasma N_2 passivation

In addition to the benefit of native-oxide free MOSCAP fabrication, the cluster tool also offers the advantage of in-situ surface clean with a low damage plasma approach, as shown in Fig. 5.2. Each pre-treatment cycle comprised a H_2 or N_2 plasma pulse (2s), a pump step (5s), a short tri-methyl-aluminium (TMA) pulse (40ms), followed by an Ar gas draw/purge step and a plasma H_2 or N_2 pulse followed by H_2 or N_2 stabilisation step. The well-known process of cyclic TMA plasma gas pre-treatment with N_2 and H_2 prior to high-κ gate dielectric deposition can accomplish sulphur-free native III-V surface preparations with low interface defect density [5.2]. Therefore, further investigation is

also reported assessing the impact of in-situ plasma processing on (100)- and (110)-oriented InGaAs MOSCAPs which have been subjected to a $Cl_2/CH_4/H_2$ based ICP etch chemistry. The result of comparison with in-situ cyclic plasma N_2/TMA and H_2/TMA processes after ICP etching and prior to ALD deposition of HfO_2 will be discussed in Chapter VII.

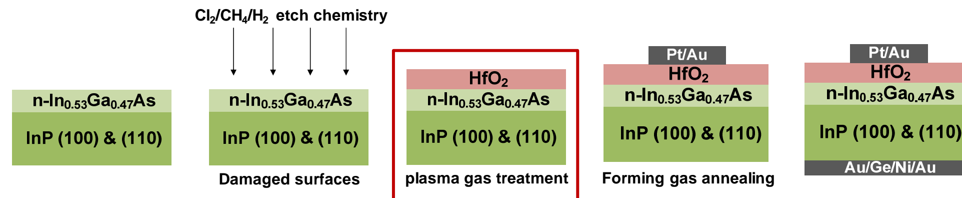


Fig. 5.2. The schematic diagram of gate stack formation with plasma gas pre-treatment on (100) and (110) orientation of etched InGaAs surfaces.

5.3 Device fabrication

There are many methods to qualify the heterostructure design of Tunnel-FETs and the material grown by MBE prior to fabricate vertical nanowire Tunnel-FETs such as module testing of tunnel diode or MOSCAPs. However, the most practical way to assess the material is characterizing the planar device of Tunnel-FETs with DC measurement. Therefore, the following Section 5.3.1 will introduce the process flow of planar Tunnel-FETs that is firstly conjunction with the in-situ process of ICP etching and ALD in this work, followed by scaling the channel width to achieve double gate Tunnel-FETs to understand the effectiveness of gate control compared to single gate Tunnel-FET. The geometrical difference between single gate and double gate are shown in Fig. 5.5 Moreover, the strategy of pattern transfers via a variety of different masks, such as materials or shapes of masks, for the formation of scaled vertical nanowire will be discussed. The complete process development for vertical nanowire Tunnel-FETs in this work will be briefly discussed at the end of the chapter.

5.3.1 Progress of planar Tunnel-FETs

The material layer structure of Tunnel-FETs is from bottom to top, the channel of planar device (intrinsic layer) for the gate terminal shown in the Fig. 5.3 is placed at the sidewall that is formed by the ICP dry etch. For the achievement of high quality material growth, the MBE commonly starts at n-type material. Therefore, the drain terminal of planar device (n-type layer) is set on the bottom while the other side is set for source terminal (p-type material) on the top. The current path generally flows from the bottom of drain

side via the band-to-band tunneling region controlled by gate terminal and ends in the top of source side.

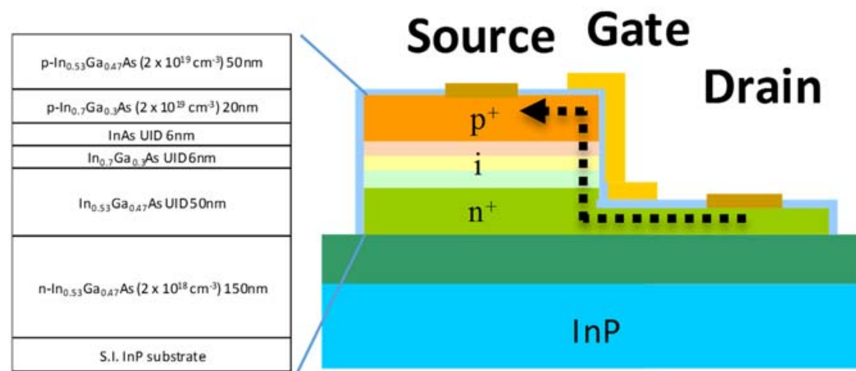


Fig. 5.3. Schematic diagram of planar Tunnel-FETs with the InGaAs based p-i-n heterojunction. The dotted line shows the current flow from drain to source side.

5.3.1.1 Process flow

In Fig. 5.4, the process flow for planar device fabrication starts from blanket molybdenum metallization of top ohmic contact first to avoid misalignment followed by marker preparation including global and cell markers, then depositing the source contact of Ti/Pt and followed by 20nm SiN deposition. Continuously, the sidewall channel is formed by ICP dry etch tool via the pattern transfer of a defined HSQ mask on the top of the SiN layer, then HfO_2 dielectric layer and a TiN layer are subsequently in-situ deposited by ALD. Afterward, the sample is treated by forming gas annealing (FGA) prior to the gate region definition. The metal pad of Ni/Ti/PdAu on drain is prepared after both HfO_2 dielectric layer and TiN metal being etched and then annealed for ohmic contact by RTA.

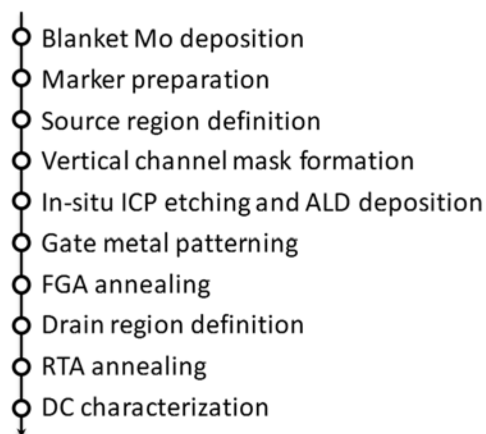


Fig. 5.4. Process flow of planar Tunnel-FET.

5.3.1.2 Single gate vs. double gate

For the planar Tunnel-FET with top-down layer structure in this work, the channel length is determined by the triple intrinsic layer of $InAs/In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ (~60nm) of p-i-n tunneling diode as shown in Fig.5.3. The effect of shrinking the channel length in a traditional MOSFET, known as the short-channel effect, is the appearance of threshold voltage roll-off [5.3]. However, based on the simulation result, the Tunnel-FET suffer severe performance degradation with increased off-current and sub-threshold slope as the channel length is scaled [5.4]. Initially, the p-n layer structure of Tunnel-FET can be seen as a short channel device which can be considered to understand the electrical properties of such this device. To date, the solution to solve the short channel effect is utilizing such a double gate structure to enhance the electrostatic control of gate. Therefore. achieving the double gate configuration for Tunnel-FET is desired in this work. As the aforementioned sidewall channel of Tunnel-FETs, the channel width is determined by surrounded gate metal on the sidewall. The architecture of single-gate is similar as the conventional planar Tunnel-FET, as shown in Fig. 5.5 (b). The realisation of double-gate like Tunnel-FET is made by narrowing the area of band-to-band tunneling region wrapped around by gate metal, as given in Fig. 5.5 (a). Meanwhile, this can provide a good angle to understand the electrical properties while further scaling the channel thickness of Tunnel-FETs, defined by the epi-layer design such as p-n tunneling diode.

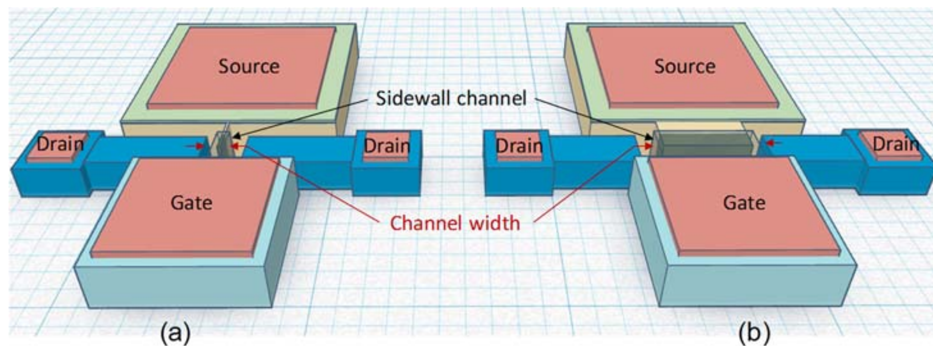


Fig. 5.5. Schematic diagram of (a) double gate Tunnel-FET and (b) single gate Tunnel-FET with a side view.

The SEM images of single and double gate planar Tunnel-FETs are shown in Fig. 5.6 (a) and (b), respectively. Both single gate and double gate Tunnel-FET are fabricated with in-situ ALD deposited HfO_2 and TiN gate metal. An additional gate metal of Pd/Au is

patterned across part of the complete etched region on the top and sidewall, which is marked as grey in Fig. 5.5 (a) and (b), for the metal pad connection. Fig. 5.6 (c) shows the double-gate structures with metal pad. After etching the TiN metal and HfO_2 dielectric layer on both the bottom and sidewall sides, the ohmic contact of drain region are deposited, as given in Fig. 5.6 (d).

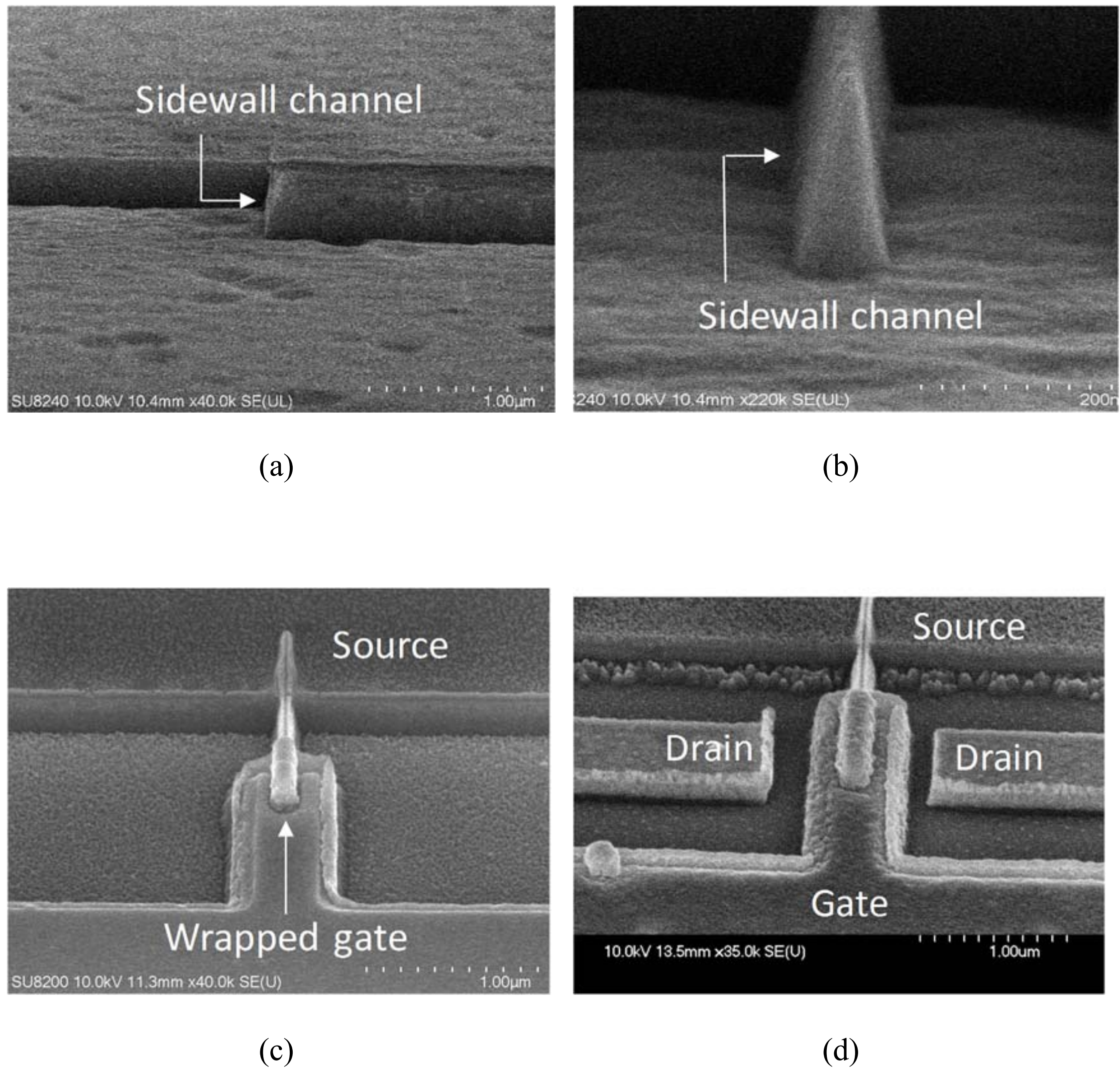
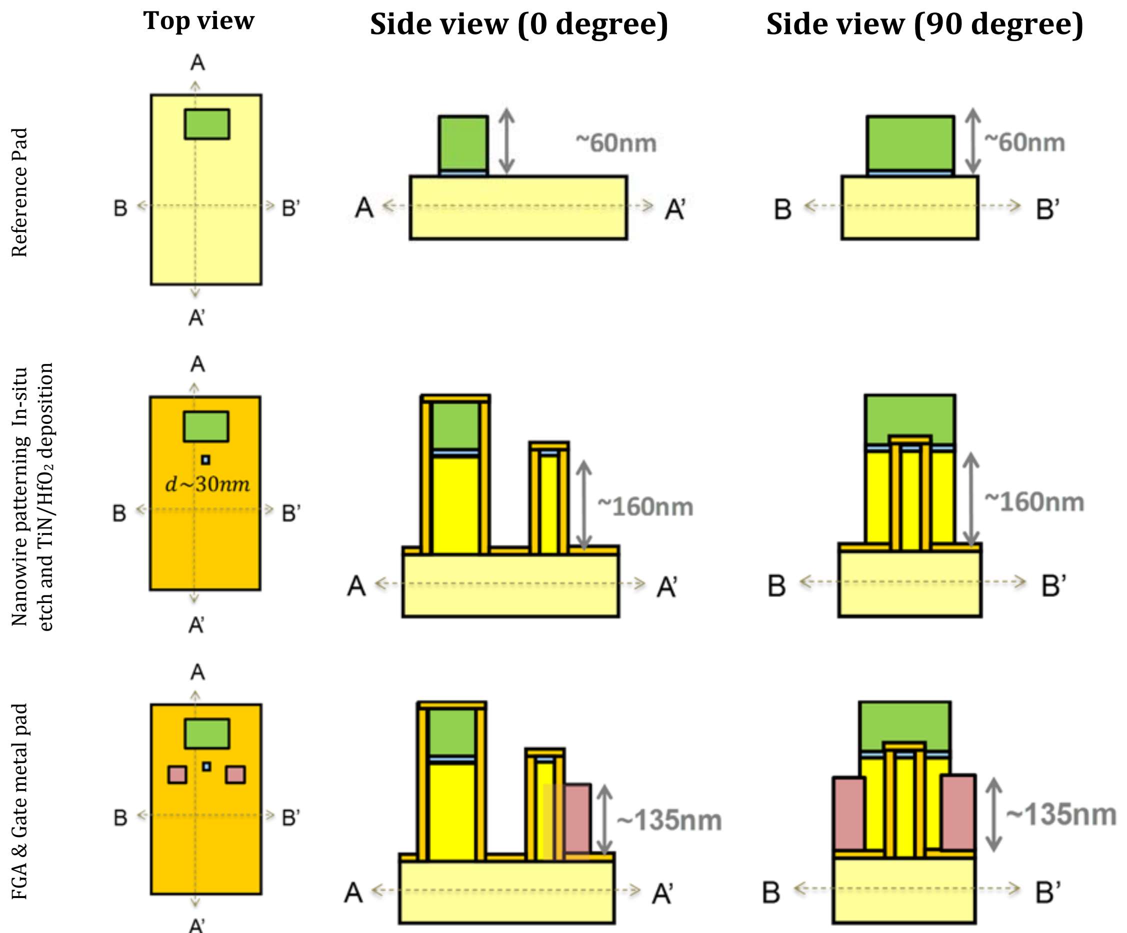


Fig. 5.6. SEM inspection of etching profile with in-situ ALD deposition on (a) single gate and (b) double gate devices, (c) the gate metal covering the whole etched channel on the sidewall and (d) the drain pad patterning.

5.3.2 Progress of vertical nanowire Tunnel-FET

The transistor scaling trend, based on the Moore's law, has driven the improvement of CMOS technology in past decades [5.5]. However, it becomes challenging to push the limitation of channel dimensions below 5 nm due to intrinsic problems such as quantum confinement and scattering effects [5.6]. In addition, the aforementioned short-channel control will also increase the difficulties to stabilize the threshold voltage. One of the best solutions is adopting the nanowire device architecture. Therefore, the electrical properties of nanowire based Tunnel-FETs, considered as the alternatives of traditional MOSFET, should be further addressed. First of all, the schematic diagram of the nanowire process flow for Tunnel-FET is shown in Fig. 5.7. In addition, the key processes that enable the realisation of nanowire Tunnel-FET—such as top-down nanowire etching, gate-all-around gate metal, and spacer engineering for top contact—will be described in the following sections. The details for each step of the whole process are included in the Appendix A.



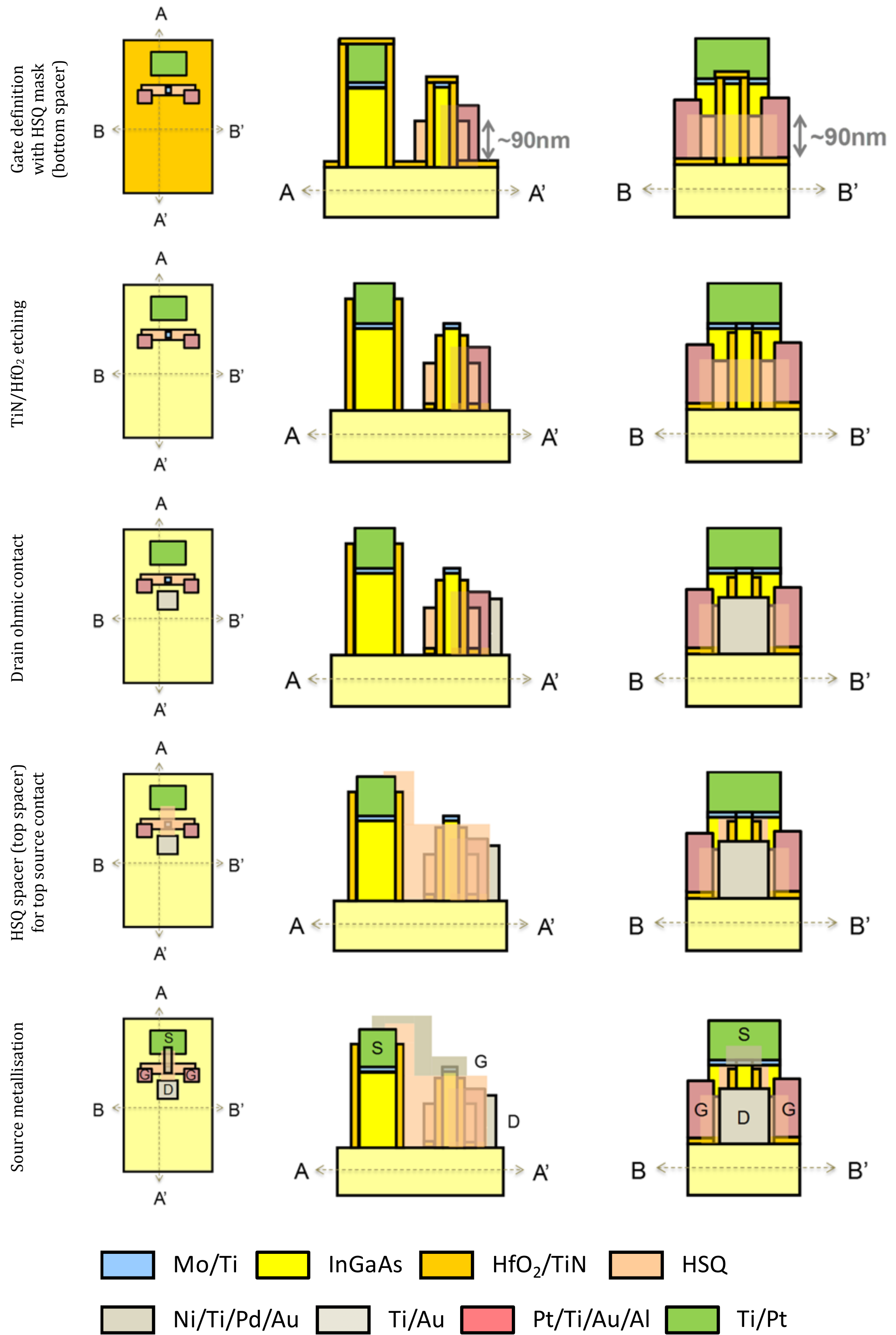
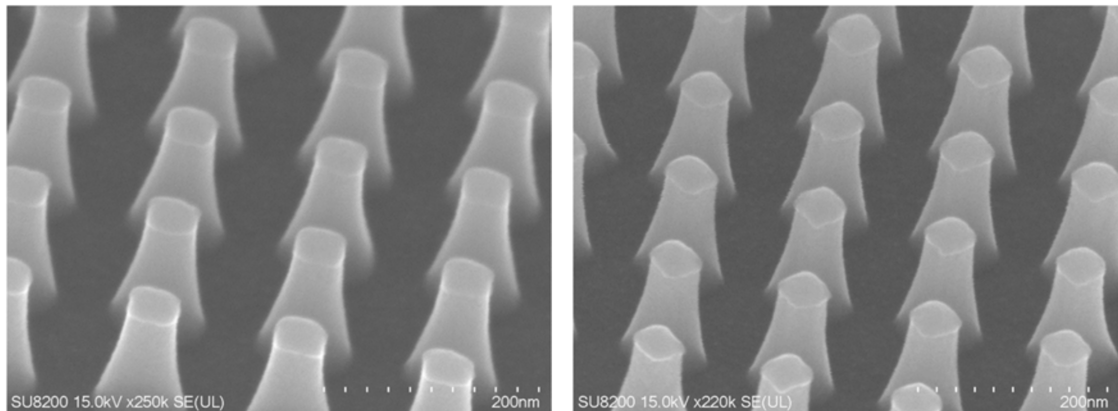


Fig. 5.7. The schematic diagram of the nanowire process flow for Tunnel-FET.

5.3.2.1 Top-down InGaAs nanowire formation

In this work, the top-down method, which contains two steps of mask definition and ICP etching, is adopted for nanowire formation. The mask selection for nanowire definition is the aforementioned HSQ, a negative tone e-beam resist. The quality of the mask, which will highly influence the pattern transfer, is determined by the appropriate dose for e-beam lithography. Meanwhile, the dose is sensitive to the material that directly contacts with the HSQ. In addition, the adhesion of HSQ is highly related to the contact surface of the semiconductor. Therefore, selecting an intermediate layer of appropriate material is very important to pattern a high quality HSQ mask. In this work, an intermediate layer of molybdenum metal is selected for the etching mask due to the convenience of device integration and high adhesion between HSQ and semiconductor. Based on the optimal etching condition for minimising etching damage [5.1], the etching profile of nanowires with (110)-oriented and (100)-oriented surfaces on the sidewall are transferred from the defined square patterns, shown in Fig. 5.8 (a) and (b), respectively.



(a) (b)

Fig. 5.8. The etching profile of nanowires with (a) (110)-oriented and (b) (100)-oriented surfaces.

Furthermore, the narrower nanowire can be achieved by means of designing different shapes, for instance, the shape of triangle, diamond or circle. The scaled nanowire is obviously observed in Fig. 5.9. Comparing to the other shapes, the circle is formed by one beam shot without any beam steps. The diamond shape is adopted due to the stability of nanowire formation. In addition to dielectric layer deposition after nanowire etching,

an in-situ ALD TiN layer (10nm) is added to all the nanowires shown in the Fig 5.9 to achieve gate-all-around nanowires for device integration.

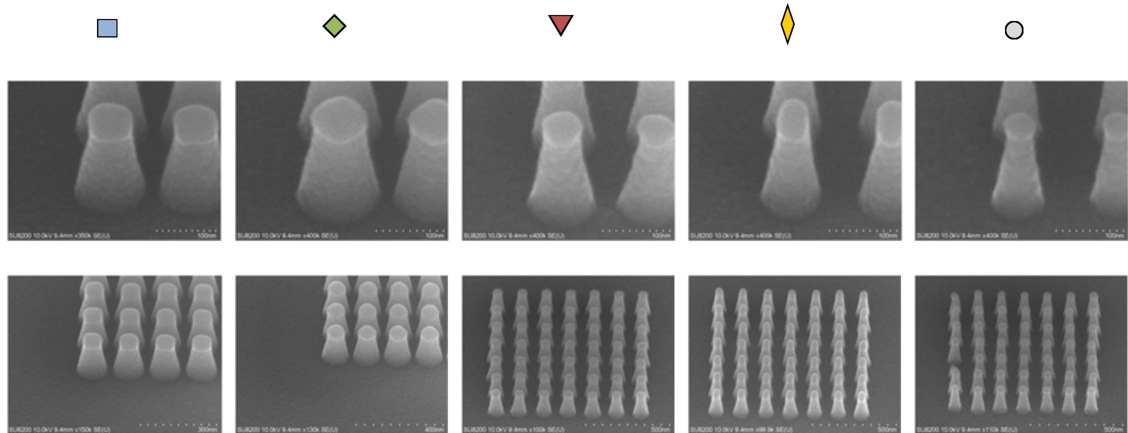


Fig. 5.9. SEM inspection of nanowire etching profile with the shape of cross section including square, triangle, diamond and circle.

5.3.2.2 Bottom spacer

The process flow for nanowire formation with in-situ dielectric layer deposition and a TiN layer insertion for gate all around gate stack has been introduced in Fig. 5.7. There is another challenge for top-down fabrication of nanowire devices – the issue of isolating gate, source and drain terminals. The formation of spacers is required to electrically isolate the gate, source and drain terminals. The spacer technique used in this work only isolates the source metal on the top side and the wrapped around gate metal on the sidewall of a pillar-based fin/wire structure.

In this work, HSQ is used as the spacer due to similar physical and chemical characteristics of SiO_x after being exposed or curing [5.7]. The other reason for the usage of ebeam resist is that spinning technique can perform a desired coverage, compared to the spacer deposited by CVD tool, shown in the Fig. 5.10. In addition, the etching back is required to remove undesired spacer covering on the top of the nanowire. Despite a SiN layer, which is commonly used for sidewall spacer formation, can perform the protection of gate stack on the sidewall, it also increases the design complexity of gate stack contact on the sidewall. For instance, it is difficult to create a contact path for this in-situ gate stack on the sidewall after spacer formation via a process of etching back and gate patterning. Therefore, HSQ spacer layer is preferred in this work to accomplish the required contact path between a large gate pad and the gate stack on the sidewall.

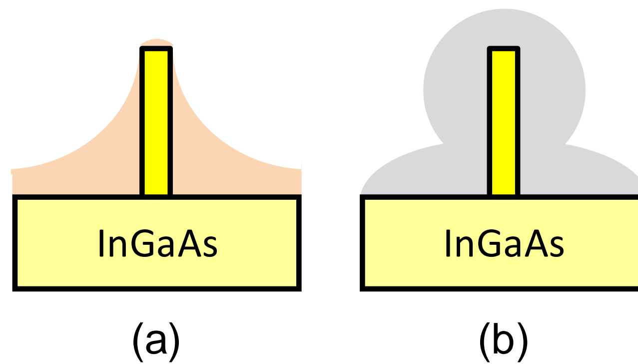
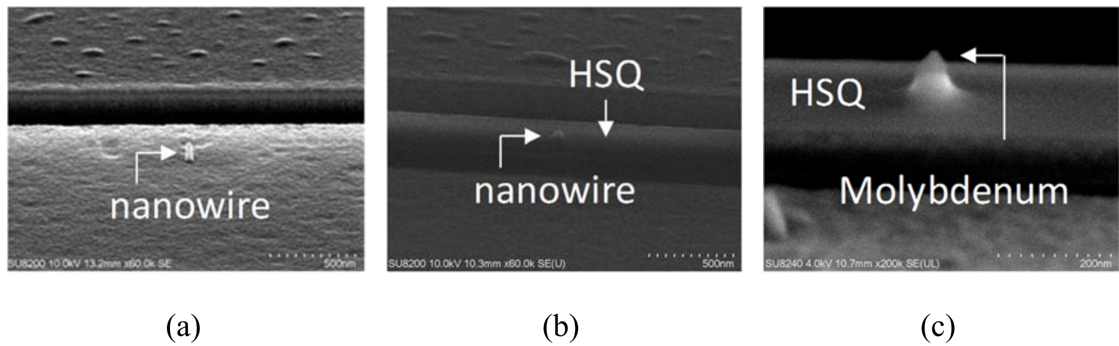


Fig. 5.10. The spacer coverage from the material of (a) HSQ and (b) SiN layer.

5.3.2.3 Gate metal definition and ohmic contact

As shown in Fig, 5.7, the realisation of gate metal definition for practical nanowire device fabrication requires three steps which are listed below: i) Forming a large metal pad for gate contact. ii) Spinning a HSQ layer for the sidewall gate stack protection and exposing the gate metal area which crosses all the nanowires and large pad for connection. iii) Etching back for the removal of undesired resist, TiN and dielectric layer on both top and bottom side of nanowire, which is not overlapped by spacer. The process of FGA for the improvement of gate stack on the sidewall is achieved prior to pattering the gate metal region. Fig. 5.11 (a) and (b) show the SEM inspection of actual device fabrication before and after metal gate patterning via a HSQ spacer layer, respectively. Furthermore. the removal of HfO_2 and TiN on nanowire with ICP etching is shown in Fig. 5.11 (c). As shown in Fig. 5.11 (b), the top side of nanowire can still be inspected and covered by a thin HSQ layer. After etching back, the nanowire (lighter) and molybdenum metal on the top of nanowire (darker) can be obviously found in Fig. 5.11 (c). Also, this molybdenum metal layer can still be observed after etching back the layer of TiN metal and HfO_2 dielectric layer. Most importantly, the diagram of Fig, 5.11 (c) shows the good coverage of HSQ on the sidewall of nanowire for the protection of gate stack. Afterward, the ohmic contact is deposited and followed by RTA annealing shown in Fig. 5.12.



(a) (b) (c)

Fig. 5.11. the SEM inspection of (a) the nanowire without a HSQ spacer coverage, (b) with a HSQ layer coverage and (c) the removal of TiN metal and dielectric layer on the both top side of nanowire and the bottom side which is not covered by spacer.

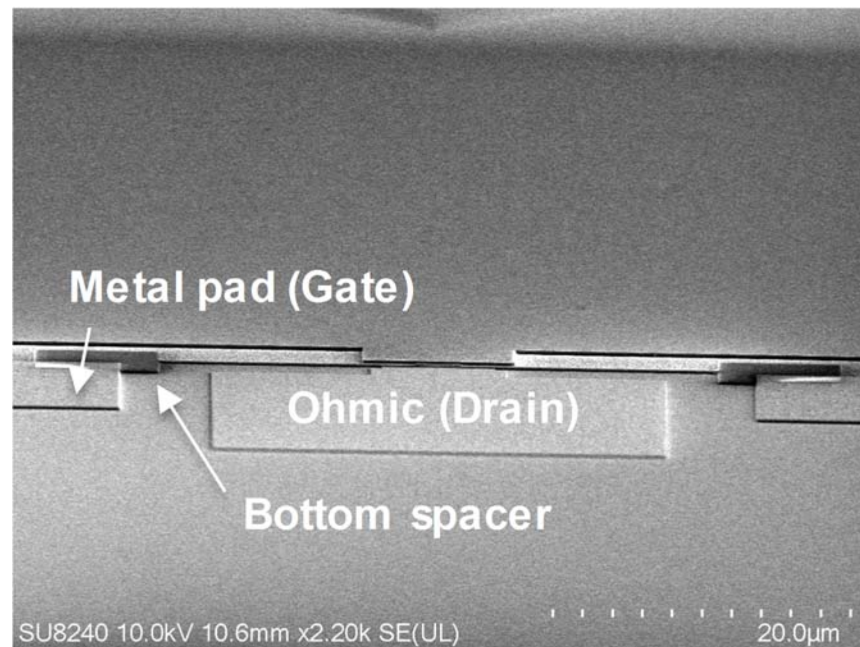
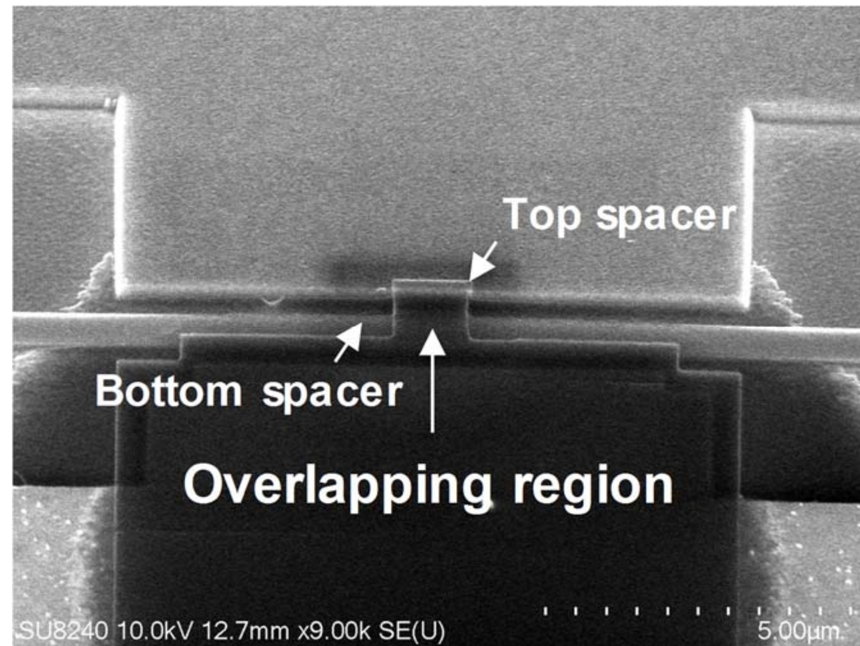


Fig. 5.12. The SEM inspection of forming ohmic pad for drain contact.

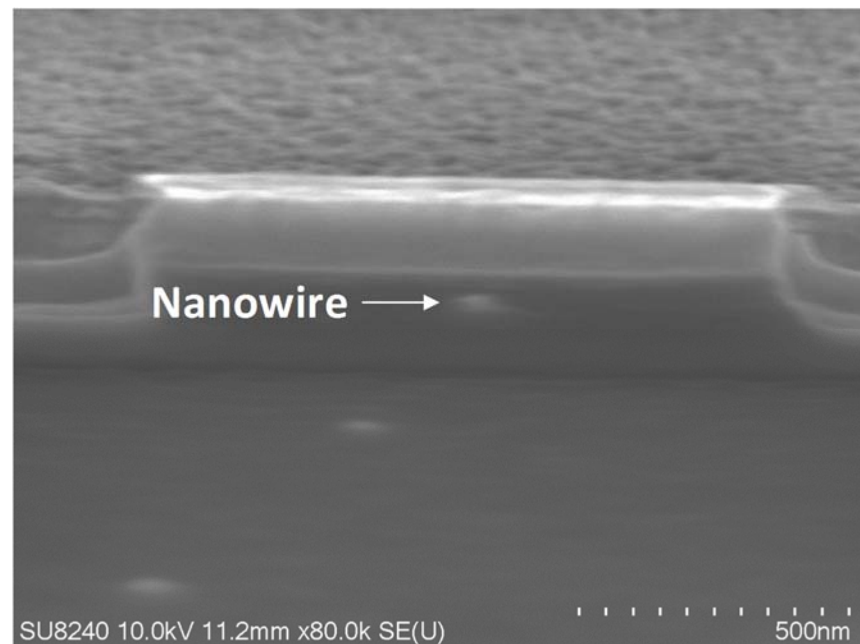
5.3.2.4 Top spacer and source electrode

Here, the additional spacer is still required to improve the isolation of the gate metal on the sidewall and the source contact on the top side of nanowire after etching the TiN layer and HfO_2 dielectric layer. Fig. 5.13 (a) is an SEM image of the top HSQ spacer formation. The nanowire is surrounded by HSQ layers in the region where the bottom and top HSQ spacer overlap. Also, the top of nanowire is covered by a thin HSQ layer. Reducing the thickness of the HSQ layer to expose the top side of the nanowire for connection is important. Therefore, the etching back technique repeats here to open the contacted area

of nanowire on the top shown in Fig. 5.13 (b). Afterward, the metal bridge between the top side of the nanowire and another metal pad is prepared for the source. The complete Tunnel-FET device geometry is shown in Fig. 5.14.



(a)



(b)

Fig. 5.13. SEM inspection of (a) top HSQ spacer formation and (b) etching back to expose the top of nanowire for metal connection.

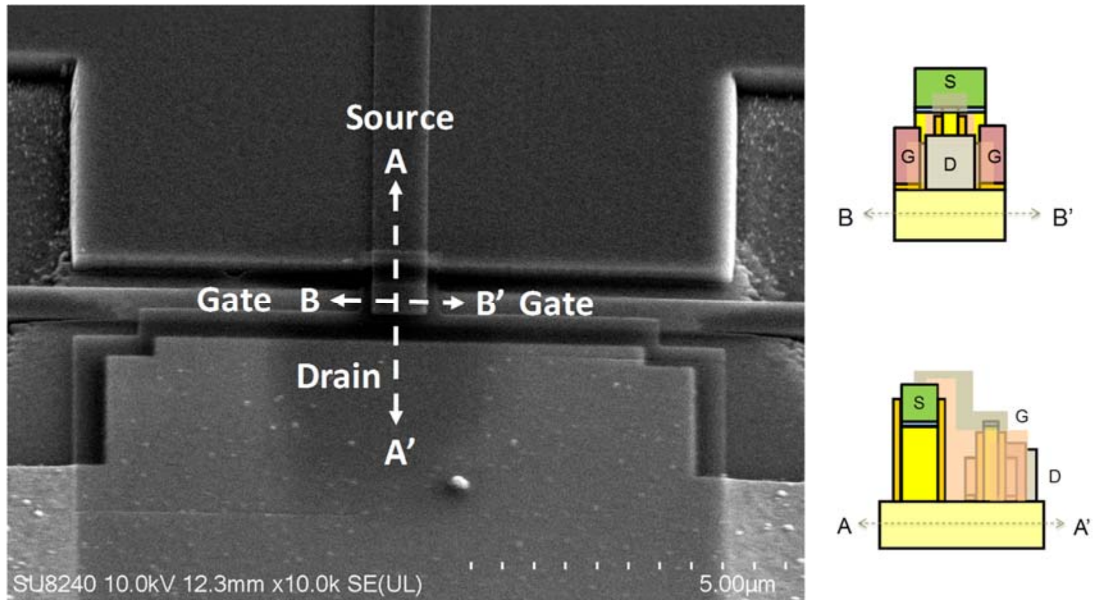


Fig. 5.14. The SEM inspection of the final device layout.

5.4 Characterisation

To complement the information in Sections 2.5 and 5.2, this section will initially introduce the method to extract the key parameters from C-V measurement for analysis which enables quantification of the interface quality of MOSCAPs. This is followed with a prescription of device DC characteristics. The metrology of contact characterisation will be further presented.

5.4.1 MOSCAP device characterisation

As mentioned in section 2.5.3, non-ideal effects in a MOSCAP result from defects in the oxide or at the oxide/semiconductor interface. These defects will directly influence the performance of both MOSFETs [5.8] and Tunnel-FETs [5.9]. Therefore, electrically characterising these defects is desired. One of the valuable tools is C-V measurement which can provide the significant insight into the interface defect density (D_{it}) mentioned in the Section 2.5.3.1 and oxide traps introduced in the section 2.5.3.2. In addition, the physical information corresponding to both interface and bulk oxide traps can be evaluated to understand the non-ideal C-V behaviour. The following sub-section will further describe those important parameters and introduce the method for the quantification of D_{it} and oxide trap charges of MOSCAPs. Thus, the comparison of FGA effect on sulphur passivated InGaAs (110) MOSCAPs and the assessment of sulphur-free in-situ plasma passivated InGaAs (110) MOSCAPs which have been subjected to a ICP etch can path the way to improve the practical vertical nanowire Tunnel-FETs.

5.4.1.1 Flatband Voltage

As discussed in the MOSCAPs band diagrams of Fig. 2.5, the band bending at the interface of dielectric layer and semiconductor varies with respect to the applied bias. The voltage under flatband condition, known as the flatband voltage (V_{FB}) means this applied voltage results in zero electric field across the gate dielectric layer and flat energy band of the semiconductor. The practical V_{FB} extraction provides important information. For instance, Fermi-level pinning or unpinning can be observed from the shifts of V_{FB} from MOSCAPs with a different metal gate work functions [5.10]. In addition, the surface energy profile which indicates the energy position of D_{it} can be further calculated using Berglund integral method which originates at V_{FB} [5.11]. There are a variety of methods to extract the practical V_{FB} from C-V measurement of a MOSCAP. In general, the C-V sweep under high frequency condition is commonly used to minimize the non-ideal C-V behaviour from D_{it} [5.12]. Despite the non-ideal effect of experimental results shifts the V_{FB}, the ideal or practical flatband capacitance should be only related to the oxide capacitance (C_{ox}), the permittivity of semiconductor and the Debye length. Therefore, the practical V_{FB} can be determined by the ideal flatband capacitance expressed as [5.13]:

$$C_{FB} = \frac{C_{ox}C_{FBS}}{C_{ox}+C_{FBS}}, \tag{5.1}$$

where C_{FBS} is a function of the permittivity of semiconductor and the Debye length shown below,

$$C_{FBS} = \frac{\epsilon_s \epsilon_0}{\lambda_d}, \tag{5.2}$$

where λ_d is the Debye length, and ϵ_s and ϵ_0 are the relative permittivity of the semiconductor and permittivity of free-space, respectively.

On the other hand, the C_{ox} should be addressed for the correct C_{FB} extraction because the oxide capacitance obtained from C_{max} in accumulation only suits a case of ideal MOSCAP. However, using the C_{max} of a real MOSCAP in accumulation results in C_{ox} being underestimated due to the effects of low DOS and charge quantisation in semiconductors [5.14]. Therefore, an additional method is required to determine the accurate C_{ox} to evaluate C_{FB}. In this work, the metrology for all the C_{ox} extraction is based on the comparison of experimental and modelled CV curves [5.15].

5.4.1.2 Surface potential

The surface potential is defined as the energy level with respect to the vacuum level at which the electron is free [5.16]. The movement of surface potential, known as surface

band bending, close to the interface between the dielectric layer and semiconductors depends on the electric field in the dielectric layer with respect to the applied voltage. Observing the relationship of surface potential and applied voltage can provide information of Fermi-level pinning or unpinned for a MOSCAP system. The unpinned Fermi level of MOSCAP should have band bending across half bandgap of semiconductor (midgap) while the maximum voltage is applied [5.15]. Furthermore, the most significant information obtained from MOSCAP evaluation and most relevant to device performance is acquiring the plot of the interface traps as a function of trap energy level, across the whole semiconductor bandgap as shown in Section 2.5.3.1. In this work, the Berglund integral is adopted to extract the surface potential as a function of gate voltage, Ψs(Vg), from measured CV data, which allows the position of an extracted D_{it} profile to be calculated in relation to the band gap [5.11]. It can be shown that

$$\psi_s(V_g) = {\psi_s}^0 + \int_{{V_g}^0}^{V_g} \left(1 - \frac{C_{tot}^{lf}(V_g)}{C_{ox}}\right) dV_g, \tag{5.3}$$

where $C_{tot}^{lf}(V_g)$ is the measured capacitance at low freqneucy and ${\psi_s}^0$ is the surface potential while the voltage is ${V_g}^0$. It is common to choose the flatband voltage as ${V_g}^0$ [5.19]. Therefore, the accuracy of flatband voltage extraction becomes significant. The gate voltage that corresponds to the flat band capacitance, V_{FB}, can be taken as the lower limit of integration as its position in the band gap is known. Errors are introduced however when extracting V_{FB} if either the D_{it} is large, and/or if the measured high frequency curve is not the true high frequency response, but includes contributions due to interface traps and minority carriers. Such errors result in a misalignment of the D_{it} profile with respect to the band gap, but do not affect the magnitude of the D_{it}.

For semiconductors with a high DOS, such as silicon, with conduction and valence band DOS of 3 x 10^{19} cm^{-3} and 2 x 10^{19} cm^{-3}, respectively, the lower limit of integration in the Berglund integral is usually taken at gate biases in either accumulation or inversion, where it is assumed that the Fermi level resides at the edge of the corresponding band as there is sufficient charge to screen further movement. As such, the required Vg-Ψs curves can be correctly obtained. For semiconductors with a low DOS, this assumption becomes invalid as the Fermi level can move beyond the band edges. This is particularly an issue for the InGaAs conduction band with a DOS value of 2x10^{17} cm^{-3}. As such, the Fermi level can move beyond the conduction band edge. It is only in the case of a large C_{ox}, where the electric field applied to the semiconductor becomes large, resulting in a large

band bending, that the Fermi level moves deep into the conduction band. Given the low C_{ox} values of our work which will be discussed in chapter VI, this is not likely the case.

5.4.1.3 Interface defect density

Qualitatively, the interface defect density will stretch out the C-V curves of a MOSCAP at the voltage of flatband. Therefore, this method can simply provide an indication of the quality of the interface between dielectric and semiconductor prior to quantitively analysing the D_{it}. The metric of stretch-out is defined as:

$$\text{Stretch-out}\left(\frac{F}{cm^2V}\right) = \frac{\Delta C_{HF}}{\Delta V_g}, \quad (5.4)$$

where the slope of stretch-out is extracted at flatband voltage. Although this method cannot be used to obtain the value of D_{it}, it is useful to acquire qualitative results between C-V characteristics of MOSCAPs subject to different process conditions of gate stack formation or interface pre-treatment engineering.

Several methods being proposed to quantitatively determine D_{it} profiles, such as the Terman method [5.17], the low frequency method [5.11] and the high-low frequency method [5.18]. Each methodology has their specific requirement to ensure the accuracy of D_{it} extraction. For the Terman method, the methodology utilizes the comparison of the stretch-out, which is obtained from a measured C-V curve at the high frequency, and an ideal C-V curve. This is based on the idea that C-V curves measured at sufficiently high frequency are only influenced by the stretch-out with respect to the gate bias instead of any ac contribution from interface traps. In contrast, low frequency method, known as the Berglund method, is using the measured C-V curve at sufficient low frequency, when all the interface traps are able to follow the ac signal response and contribute the measured capacitance with an additional C_{it}, which can be used to evaluate the interface trap density by comparing to the ideal C-V profiles. Despite both methods being able to extract the D_{it} profile across the whole energy bandgap, there is still an assumption of ideal C-V profile which is modelled accurately. The errors of modelled ideal C-V curve which may result from insufficient information from material parameters or process deviations will cause the underestimation or overestimation of interface defect density [5.19]. Therefore, the metrology used in this work adopts the combined high and low frequency C-V measurements, proposed by Castagn´e and Vapaille [5.18], to exclude the errors from theoretical modelling. The interface trap density is obtained by comparing the low frequency response to the high frequency response. However, the accuracy may be limited by the determination of C-V profiles measured at the true “low” and “high”

frequency. For low frequency measured C-V curves, the D_{it} may be underestimated if all the traps cannot respond to the AC frequency, which will contribute to the C_{it}. In addition, D_{it} would also be underestimated if the high frequency C-V profiles, even at 1MHz, are not enough to exclude the response from interface traps [5.13]. Therefore, the modified high-low frequency C-V measurement which performs high frequency curves at reduced temperature to minimize the errors from the AC response [5.13]. The interface trap density of the modified metrology can be represented as:

$$D_{it}(V_g) = \frac{C_{ox}}{q}\left(\frac{C_{LF}/C_{ox}}{1-C_{LF}/C_{ox}} - \frac{C_{HF(LT)}/C_{ox}}{1-C_{HF(LT)}/C_{ox}}\right). \tag{5.5}$$

On the other hand, there are still some drawbacks for modified high and low frequency CV measurement comparing to Terman method and Berglund method. For instance, it cannot probe the trap levels across all the bandgap because it is only valid for the trap levels from majority band edge to the surface potential at beginning of inversion [5.19]. The trap levels in the lower half of the band gap can be only probed in a n-MOS capacitor. Similarly, a p-MOS capacitor only allows the trap levels in the higher half of the bandgap to be probed. Therefore, acquiring the D_{it} distribution across the whole bandgap requires both type of MOSCAPs.

5.4.1.4 Hysteresis

Hysteresis is another significant factor that may degrade the device performance, especially reliability, apart from the aforementioned interface trap density [5.20], refer to Fig. 2.10 (b). It originates at the charge trapping site, which referred as slow state traps or border traps, in the oxide. In addition, the frequency dispersion in the accumulation is also caused by the contribution of both the charge trapping site which locates at the interfacial transitional region between the dielectric layer and semiconductor and the fast interface states which aligns with energy level in the conduction band of semiconductor [5.21], refer to Fig 2.10 (a). This can be defined as:

$$Frequency\ Dispersion\ \left(\%\frac{}{dec}\right) = \frac{C_{LF,max}-C_{HF,max}}{C_{LF,max}} \times \frac{100\%}{N_{dec}}. \tag{5.6}$$

For the device reliability perspective, quantifying the charge trapping density via the method of analysing the C-V hysteresis is studied in this work to further understand the FGA effect of InGaAs (110) MOSCAP. The double sweeps including upwards and downwards sweep measured at 1MHz subject to an increased V_{max} is set as the essential measurement for C-V hysteresis response. For those C-V responses with different V_{max}, the hysteresis of each C-V profile is determined by the difference of flatband voltage

extracted from flatband voltage capacitor. Plotting the hysteresis as a function of V_{max} can obtain the linear distribution. Based on the slope of curves, the trapped charge density in the accumulation can be evaluated according to the bias with the offset of flatband voltage [5.22].

5.4.2 TFET characterisation

The methodology of current-voltage (I-V) measurement is commonly utilized to evaluate the performance of three terminal transistors such as Tunnel-FETs. Despite the fact that there is no obvious sub-threshold region for Tunnel-FETs, the transfer characteristics which can capture some electrical properties such as on-off ratio, subthreshold swing (SS), threshold voltage (V_T) and transconductance (g_m), as shown in Fig. 5.15 (a) and (b), can still provide useful information related to the quality of semiconductor materials, gate stack, and the design of device layout or process flow. In addition, the temperature dependent transfer characteristics with further analysis can determine the effective barrier of band-to-band tunneling. On the other hand, the output characteristics which can exhibit saturation current and on current resistance is linked to the quality of contact resistance between source and drain terminal. More details for each parameter will be introduced in this section.

5.4.2.1 DC characterisation

The aforementioned transfer characteristics and output characteristics used to evaluate the DC characteristics of a transistor are obtained by means of sweeping the gate voltage at a constant drain voltage or the drain voltage at a constant gate voltage, respectively. Furthermore, both characteristics can provide the information on those parameters below,

- Subthreshold swing (SS): as discussed in Chapter II, the SS is defined as the inverse slope of logarithmic drain current versus gate voltage. The minimum SS is commonly used to benchmark the performance of Tunnel-FET. In addition, the plot of SS as a function of drain current at the constant drain voltage ($V_{DS}<0.5V$) is applied for the comparison of low power device performance.

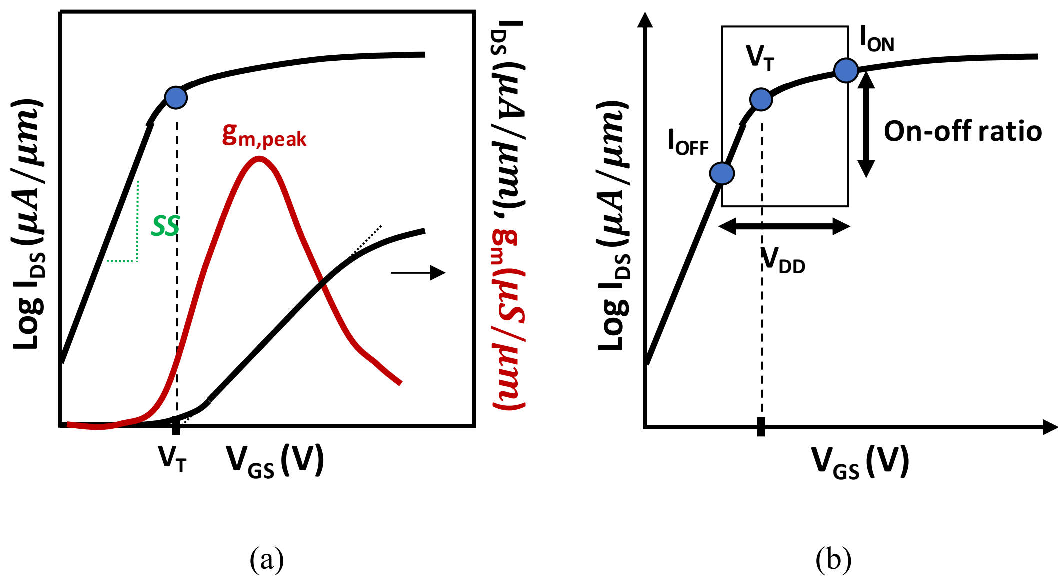
- Threshold voltage: The extraction of threshold voltage, at which the transistor switches from off-state to on-state, is also introduced in Chapter II. The typical extraction of threshold voltage is using the extrapolating line obtained from the tangent of the drain current at the voltage.

- Transconductance: The transconductance can be separated in extrinsic transconductance obtained from the measured transfer characteristics and intrinsic

transconductance that is calculated excluding the effect of series resistance from source and drain.

- On-off ratio: On-off ratio exhibits the window between on and off current. 10nA/um can be defined as off-current while on current is given by the voltage which is offset from off-current voltage at the constant drain voltage, for instance, $V_{on} = V_{th} + 2/3\ V_{DD}$; $V_{off} = Vth - 1/3V_{DD}$ [5.23].

These above parameters will be used to analyse both the single gate, double gate and nanowire Tunnel-FETs in Chapter VIII.



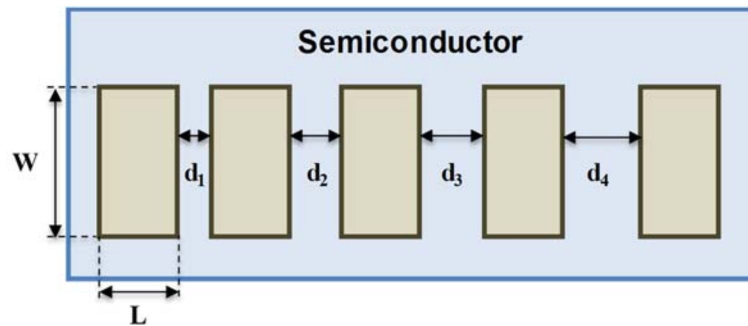
(a) (b)

Fig. 5.15. Transfer characteristics of a generic Tunnel-FET showing the parameters of subthreshold swing (SS), threshold voltage (V_T) and transconductance peak ($g_{m,\ peak}$) in (a) and On-off ratio in (b).

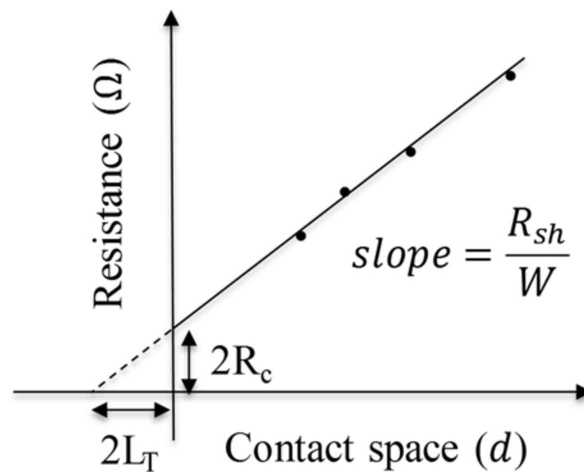
5.5 Contact characterisation

As discussed in Section 2.8, the transistor performance especially for small feature size devices suffer degradation by high contact resistance that is limiting access to the intrinsic characteristics of devices. The Transfer Length Method structure (TLM) originally proposed by Shockley is introduced to characterise the contact performance between metal to planar semiconductor by measuring the total resistance between two adjacent contacts with a specific separated distance and generating the plot of resistance as a function of increasing contact separation [5.24]. As shown in the Fig. 5.16, this test

structure method comprises an array of contact pads with identical width/length and increasing distance d between each pad.



(a)



(b)

Fig. 5.16. (a) Schematic diagram of TLM test structure and (b) the parameter extraction from the plot of total resistance as a function of contact separation.

The total resistance (R_T) obtained from the current by applying the potential drop between two adjacent pads is composed of the contact resistance between the metal to semiconductor and semiconductor sheet resistance (R_{sh}). This linear curve can be formulated as:

$$R_T = \frac{R_{sh}}{W} d + 2R_C, \tag{5.7}$$

as known in the above equation, the parameter of sheet resistance (R_{sh}) in Ω/sq unit can be obtained from the slope of linear regression of the total resistance as a function of

contact spacing. Extending the fitted regression to cross the y-axis, the intercept is expressed as two times the contact resistance (R_C), for which the parameter is usually normalized by the contact width of 1mm, thereby the unit can be represented in Ω.mm. Furthermore, the parameter of transfer length (L_T) defined as the effective length of an electron travels in the semiconductor to the beneath of contact with $1/e$ current dropped before flowing up into the contact is extrapolated from the regression at the intercept of x-axis while the total resistance is zero [5.25]. Due to the current crowding effects, there is a need for contact spacing which should be at least two times or longer transfer length [5.26]. On the other hand, another good figure of merit for comparison is contact resistivity defined as:

$$\rho_C = \left(\frac{\delta J}{\delta V}\right)^{-1}_{V=0}, \tag{5.8}$$

where J is the current density flowing through the contact and the V is the potential drop across the area of the contact. The evaluation of specific contact resistivity based on the extracted transfer length and the semiconductor sheet resistance be expressed as [5.27]:

$$\rho_C = R_{sh}{L_T}^2. \tag{5.9}$$

In addition, the sheet resistance underneath the contacts (R_{sk}) should be considered to avoid the inaccurate extraction of transfer length and specific contact resistance [5.27]. Also. The alloying effect of metal contacts is an important factor to take into account. The resulting modification to the TLM method to account for this effect is reported in [5.27].

5.6. Chapter summary

This chapter has initially presented the fabrication in this work including the achievement of in-situ gate stack and optimisation with the technique of plasma gas pre-treatment. Furthermore, the nanowire formation based on the pattern transferring of dry etching via the high resolution mask prepared by ebeam lithography introduced in chapter III has been accomplished. Based on these well-developed modules, the first III-V Tunnel-FET with in-situ gate stack is demonstrated in this work and will be discussed further in Chapter VIII. On the other hand, the characterisation techniques used for the assessment of gate stack module and the evaluation of device characteristics were given afterward including quantification of interface quality on MOSCAPs and DC characterisation of III-V Tunnel-FET performance.

5.7. Reference

[5.1] O. Ignatova, et al., ”Towards vertical sidewalls in III-V FinFETs: dry etch processing and its associated damage on the electrical and physical properties of (100)-oriented InGaAs”, *SISC*, Arlington, VA, 5-7 Dec. 2013.

[5.2] V. Chobpattana, J. Son, J.J.M. Law, S. Stemmer, R. Engel-Herbert and C.-Y. HuangNitrogen-passivated dielectric/InGaAs interfaces with sub-nm equivalent oxide thickness and low interface trap densities”, *Applied Physics Letters.* 102, 2013.

[5.3] L. Yau, “A simple theory to predict the threshold voltage of short-channel IGFET's”, *Solid-State Electronics.* 17, 1059-1063, 1974.

[5.4] J. Wu, J. Min and Y. Taur, “Short-Channel Effects in Tunnel FETs”, *IEEE Transactions on Electron Devices*, 2015.

[5.5] G. E. Moore, *Cramming more components onto integrated circuits*. New York, McGraw-Hill, 1965.

[5.6] K. J. Kuhn, “Considerations for Ultimate CMOS Scaling”, *IEEE Transactions on Electron Devices*. 59, 1813-1828, 2012.

[5.7] J. K. W. Yang, V. Anant and K. K. Berggren, “Enhancing etch resistance of hydrogen silsesquioxane via postdevelop electron curing”, *Journal of Vacuum Science and Technology B Microelectronics and Nanometer Structures*, 24, 3157-3161, 2006.

[5.8] Y.-C Fu et al., “High mobility high on/off ratio C-V dispersion-free Ge n-MOSFETs and their strain response”, *Electron Devices Meeting (IEDM),* 2010 IEEE International, 18.5.1-18.5.4.

[5.9] T.P. Xiao, X. Zhao, S. Agarwal and E. Yablonovitch,” Impact of Interface Defects on Tunneling FET Turn-on Steepness”, In: *2015 Fourth Berkeley Symposium on Energy Efficient Electronic Systems (E3S)*, 2015.

[5.10] E. J. Kim, E. Chagarov, J. Cagnon, Y. Yuan, A. C. Kummel, P. M. Asbeck, S. Stemmer, K. C. Saraswat and P. C. McIntyre, “Atomically abrupt and unpinned Al_2O_3/In0:53Ga0:47As interfaces: experiment and simulation”, *Journal of Applied Physics,* vol. 106, no. 12, p. 124508, 2009.

[5.11] C. N. Berglund,” Surface states at steam-grown silicon-silicon dioxide interfaces”, *IEEE Trans. Electron Devices*, vol 13, 701-705, 1966.

[5.12] R. D, Long, B. Shin, S. Monaghan, K. Cherkaoui, J. Cagnon, S. Stemmer, P. C. McIntyre and P. K. Hurley, “Charged defect quanti_cation in Pt/Al_2O_3/$In_{0.53}Ga_{0.47}As$/InP MOS capacitors”, *Journal of The Electrochemical Society*, vol. 158, no. 5, pp. G103-107, 2011.

[5.13] D. Schroder, “Oxide and interface trapped charges, oxide thickness”. In: *Semiconductor Material and Device Characterization,* 3rd ed. John Wiley & Sons, Inc., 2005, pp. 319{388.

[5.14] P. K. Hurley, R. Long, T. O'Regan, E. O'Connor, S. Monaghan, V. Djara, M. A. Negara, A. O'Mahony, I. Povey, A. Blake, R. Nagle, D. O'Connell, M. Pemble and K. Cherkaoui, “Equivalent oxide thickness correction in the high-k/$In_{0.53}Ga_{0.47}As$/InP system”. *ECS Transactions*, vol. 33, no. 3, pp. 433-444, 2010.

[5.15] R. Engel-Herbert, Y. Hwang and S. Stemmer, “Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces”, *J. App. Phys.*, vol. 108, p. 124101, 2010.

[5.16] Y. Taur, and T. H. Ning, *Fundamentals of Modern VLSI Devices*. New York: Cambridge University Press, 2009, pp. 164-165.

[5.17] L. Terman, “An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes”, *Solid-State Electronics*, vol. 5, no. 5, pp. 285-299, 1962.

[5.18] R. Castagne and A. Vapaille, “Description of the SiO2-Si interface properties by means of very low frequency MOS capacitance measurements”, *Surface Science*, vol. 28, no. 1, pp. 157-193, 1971.

[5.19] D. Mui, Z. Wang, and H. Morko, “A review of IIIV semiconductor based metal-insulator semiconductor structures and devices”, *Thin Solid Films*, vol. 231, no. 12, pp. 107{124, 1993.

[5.20] D. M. Fleetwood, M. R., Shaneyfelt, W. L. Warren and J. R. Schwank, “Border traps: issues for MOS radiation response and long-term reliability”, *Microelectronics and Reliability*. 35, 403, 1995.

[5.21] E. O’Connor, S. Monaghan, R. D. Long, A. O’Mahony, I. M. Povey, K. Cherkaoui, M. E. Pemble, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas’ev and P. K. Hurley, “Temperature and frequency dependent electrical characterization of HfO_2/$InxGa_{1-x}As$$HfO_2$/$InxGa_{1-x}As$ interfaces using capacitance-voltage and conductance methods”, *Appl. Phys. Lett*. 94, 102902, 2009.

[5.22] J. Lin, Y. Y. Gomeniuk, S. Monaghan, I. M. Povey, K. Cherkaoui, É. O'Connor, M. Power and P. K. Hurley, ”An investigation of capacitance-voltage hysteresis in metal/high-k/$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors”, *Journal of Applied Physics*. 114, 144105, 2013.

[5.23] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz and M. Radosavljevic, “Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications”, *IEEE Transactions On Nanotechnology*. 4, 153-158, 2005.

[5.24] A. Goetzberger, R. Scarlett and W. Shockley, “Research and investigation of inverse epitaxial UHF power transistors”, 1964. [Online]. Available: http://www.dtic.mil/get-tr-doc/pdf?AD=AD0605376.

[5.25] D. Sawdai, D. Pavlidis and D. Cui, “Enhanced transmission line model structures for accurate resistance evaluation of small-size contacts and for more reliable fabrication”, *IEEE Transactions on Electron Devices*, vol. 46, no. 7, pp. 1302-1311, 1999.

[5.26] H. Murrmann and D. Widmann, “Current crowding on metal contacts to planar devices”, *Electron Devices, IEEE Transactions*, vol. 16, no. 12, pp. 1022-1024, 1969.

[5.27] G. Reeves and H. B. Harrison, “Obtaining the specific contact resistance from transmission line model measurements”, *IEEE Electron Device Letters*, vol. 3, no. 5, pp. 111-113, 1982.

VI. Interface Engineering of $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) MOSCAPs

6.1 Introduction

The gate stack, considered as one of the key modules for device integration has been widely investigated on the InGaAs material system [6.1]. Throughout the revolution of device scaling, non-planar architectures have become mainstream which has resulted in several demonstrations of InGaAs FinFETs [6.2], nanowire MOSFETs [6.3] and nanowire Tunnel-FETs [6.4] on (100)-oriented substrates. Among these devices, the gate stack is defined on the both top and sidewalls of the fin/wire, where the (110) or (111) orientations can be dominant surfaces. Focus, therefore, has been placed in this work on the development of a high quality gate stack on (110) oriented InGaAs essential to the realisation of high performance non-planar InGaAs channel devices.

Based on the large density of trap states at the interface of high-κ/(100) oriented InGaAs, the surface preparation method prior to atomic layer deposition of high-κ gate dielectrics is similar to that in the SiO_2/Si system where hydrogen fluorine (HF) is used for native oxide removal and to terminate surface dangling bonds for the high-κ/InGaAs interface [6.5]. Numerous approaches have been explored to improve surface quality such as sulphur-based chemical cleans, As capping and decapping [6.6], trimethylaluminum (TMA) pre-dosing [6.7], cyclic plasma (H_2 or N_2) and TMA exposures [6.8] and AlN interface control layer [6.9]. Of these methods above, wet sulphur passivation has been reported to enable the interface quality of InGaAs (111) surfaces compatible to that achieved on InGaAs (100) surfaces [6.10]. However, the properties of a gate stack deposited on a sulphur passivated InGaAs (110) had not previously explored. In the following sections, details of the impact of sulphur-based passivation approach to the interface between Al_2O_3 grown by ALD and p- and n-type InGaAs (110) surfaces as well as the evaluation of forming gas annealing effect are highlighted [6.11]. In addition, the first determination of the conduction band offset on the Al_2O_3/InGaAs (110) MOSCAP is reported [6.12]. The chapter concludes with a systematic evaluation of the material and electrical properties of the Al_2O_3/InGaAs (110) interface.

6.2 Surface Morphology

Atomic force microscopy (AFM) was used to evaluate the surface roughness of the p-type and n-type InGaAs (110) epi-layers of this study that were grown by molecular beam epitaxy (MBE) on p+ and n+ InP (110) substrates respectively. Figure 6.1 illustrates the root mean square (RMS) roughness results determined from 5μm × 5 μm AFM scan areas from both p-type and n-type samples. It indicates the quality of MBE growth from the resulting RMS roughness of ~0.2nm on both samples.

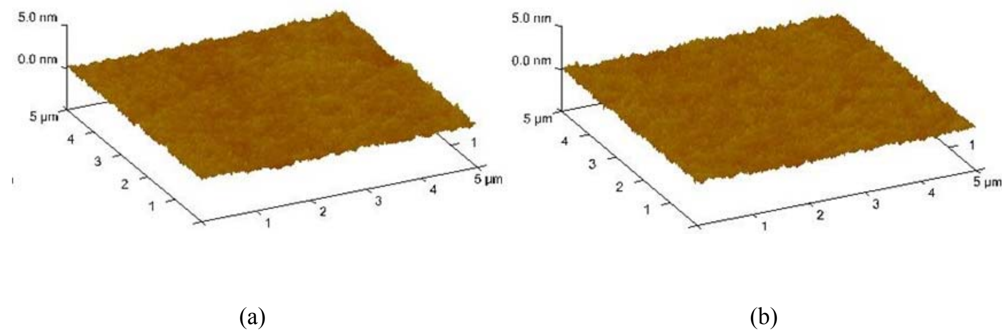


Fig. 6.1. The AFM images (5 μm x 5 μm) of as grown (a) p-$In_{0.53}Ga_{0.47}As$ & (b) n-$In_{0.53}Ga_{0.47}As$ (110) epi-layers.

6.3 Experimental Details

The wafers used in this study, as depicted in Figure 6.2, were provided by Texas State University. They employed heavily p- and n-type doped InP (110) substrates in which the epitaxial growth of p-type Be-doped (4×10^{17} cm^{-3}) and n-type Si-doped (4×10^{17} cm^{-3}) $In_{0.53}Ga_{0.47}As$ (110) layers with a thickness of 200nm were accomplished.

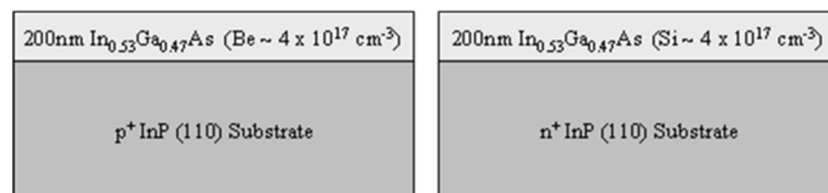


Fig. 6.2. Cross-section of p- & n-type InGaAs (110) layers on InP (110) substrates.

A typical cleaning procedure on the surface of samples from both wafers started by degreasing in each of acetone, methanol and isopropanol for 1min. Following the ex-situ treatment of immersion of the samples in diluted $(NH_4)_2S$ (10% in deionized H_2O) for 20 minutes at room temperature (~295K), the samples were quickly transferred to the ALD chamber prior to Al_2O_3 dielectric layer deposition. 8nm films were formed by ALD at 300°C using alternative pulses of TMA and H_2O precursor with the first pulse being TMA. MOSCAPs were fabricated by firstly electron beam evaporating a Pt/Au gate contact through a shadow mask, and completed with Au/Zn/Au (p-type) and Au/Ge/Ni/Au (n-type) ohmic contacts to the back of the p- and n-type samples, respectively. Post-metallization FGA (forming gas annealing) was performed in a H_2/N_2 (5%/95%) ambient for 30mins at 350°C. Electrical results were characterized using an impedance analyser (E4980A) in a microchamber probe station (Cascade, Summit 12971B).

6.4 Result and Discussion

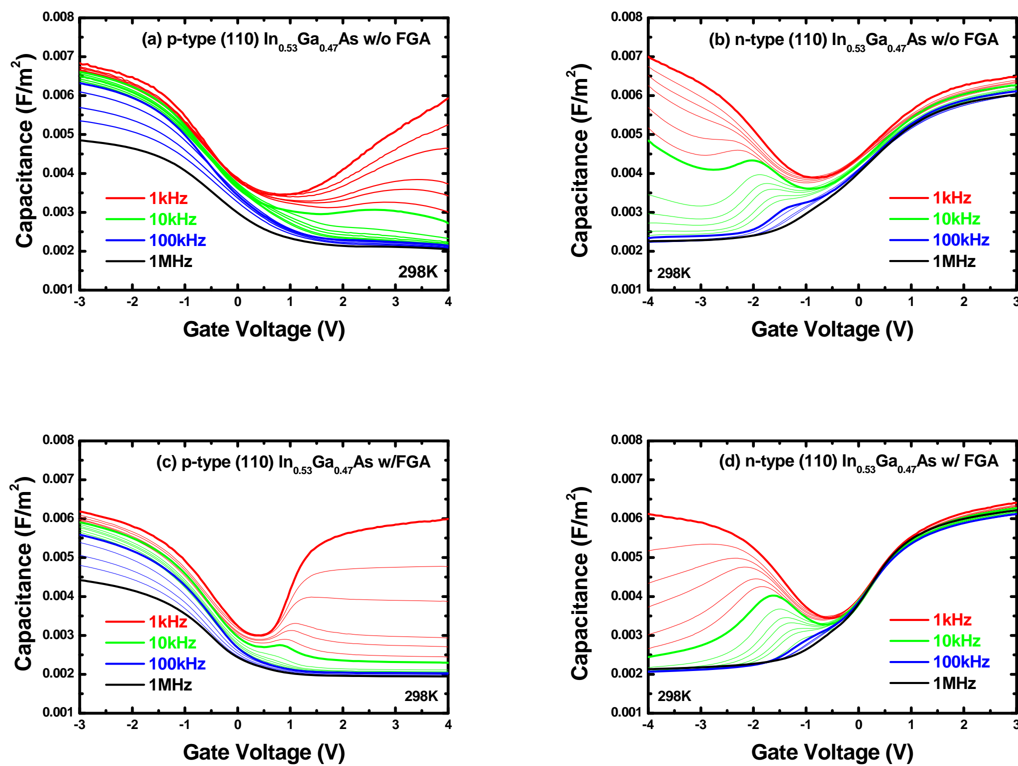
6.4.1 The impact of Forming Gas Annealing

6.4.1.1 Qualitative analysis

Room temperature frequency-dependent (1kHz to 1MHz) capacitance-voltage (CV) characteristics of sulphur passivated p- and n-type InGaAs (110) MOSCAPs before and after FGA are illustrated in Fig. 6.3(a-d). A qualitative assessment of the samples prior to FGA in Fig. 6.3 (a) and (b) reveals a large frequency dispersion in the accumulation region of the p-type (110) MOSCAP, akin to that observed in $In_{0.53}Ga_{0.47}As$ (100) MOSCAPs [6.13]. The observed dispersion is ascribed to the tunneling of carriers into electrically active, near interface border traps in the oxide [6.14-16], and fast interface states [6.17, 6.18]. The larger frequency dispersion in the depletion region of p-type MOSCAP also suggests a higher density of interface traps in the lower half of the bandgap. Following FGA, the frequency dispersion in accumulation and depletion is more than marginally improves for the p-type MOSCAP in Fig. 6.3 (c). In the case of n-type MOSCAP, the frequency dispersion in accumulation and depletion and the CV stretch-out are noticeably reduced following the FGA treatment in Fig. 6.3 (d). These observations can be interpreted as reduced D_{it} in the bandgap as a consequence of the FGA process. The C-V characteristics is significantly improved by the combination of sulphur pre-treatment and FGA which enables Fermi-level movement through the bandgap of both p- and n-type InGaAs (110) MOSCAPs and the reduction of interface trap density (D_{it}).

6.4.1.2 Genuine inversion

Notable though in the CV response of the p-type structure is the plateau as the gate bias is increased to more positive voltages as shown in Fig. 6.3(c). This behaviour is consistent with a genuine minority carrier response in inversion as opposed to a defect-dominated response [6.19]. The transition frequency, defined as the capacitance in inversion that is half way between the highest capacitance measured at low frequency and the lowest capacitance measured at high frequency, and for which the frequency scaled measured conductance (G_m/ω) at strong inversion is also a maximum shown in Fig. 6.3 (e), provides a measure of the minority carrier response time (τ_R) [6.19]. For the p-type MOSCAP after FGA, G_m/ω shown in Fig 6.3 (f) is at maximum at transition frequency of 3kHz, from which τ_R is estimated as 0.25ms. This value is comparable with τ_R of ~1ms reported on MBE grown InGaAs (100), for which inversion was observed [6.20, 6.21]



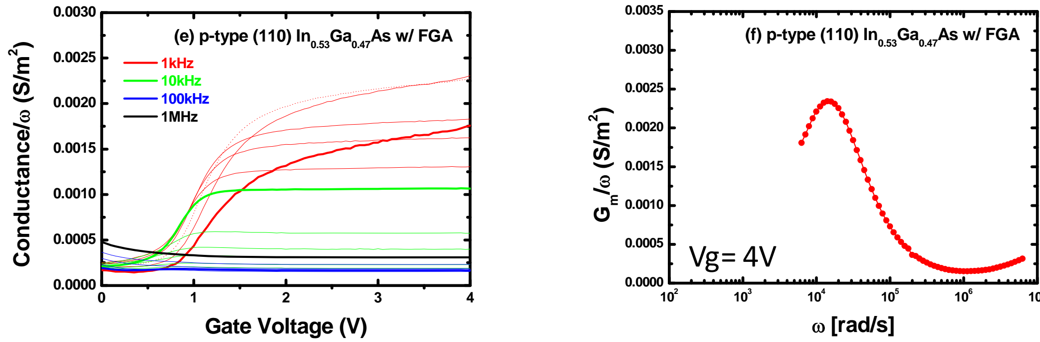


Fig. 6.3. Multi-frequency (1kHz to 1MHz) room temperature C-V characteristics of $Au/Pt/Al_2O_3$/InGaAs (110) MOSCAPs: (a) p-type and (b) n-type before FGA, and (c) p-type and (d) n-type after FGA. Scaled conductance characteristics (G_m/ω) of p-type InGaAs (110) MOSCAPs after FGA as a function of gate voltage in (e) and frequency in (f), respectively.

6.4.1.3 C_{ox} extraction

D_{it} is an important figure of merit for the interface quality and so its determination is important in understanding the impact of various process steps on capacitor performance. Obtaining an accurate estimating of the oxide capacitance (C_{ox}) is crucial as this has a direct bearing on the accuracy of the extracted D_{it}. Often C_{ox} is deduced from the maximum accumulation capacitance, which is prone to error due to the effects of density of states (DOS) and charge quantization in the semiconductor [6.22].A smaller DOS in either the conduction band or valence band would reduce the density of states capacitance, known as the quantum capacitance. The effect of charge quantization is to move the charge centroid of the accumulation or inversion layer further into the semiconductor, away from the dielectric layer, and in the process decrease the centroid capacitance. For a lower DOS the charge centroid moves further away from the interface, resulting in a reduction in C_{max} in accumulation [6.23]. An alternative is to calculate C_{ox} based on the dielectric constant (κ) and physical thickness obtained from transmission electron microscopy (TEM). Fig. 6.4 shows the TEM of p-type and n-type of MOSCAPs after FGA with thicknesses of ~9nm and 8.4nm, respectively. In literature, the κ-value of Al_2O_3 is reported to be between 7 and 9 [6.24]. However, this can also be erroneous given by the uncertainty of the κ-value resulting in an assumed value of the dielectric constant to be used in the C_{ox} calculation. In addition, there could be an interfacial transition region between InGaAs (110) and the Al_2O_3, whose dielectric constant is unknown. Instead, here we derived the theoretical value of C_{ox} for each sample by comparing the experimental

and modelled CV curves. This modelling was based on the work of Engel-Herbert et al. [6.25] and the obtained C_{ox} values plotted as horizontal lines and 1 kHz modelling curves are illustrated in Fig. 6.5.

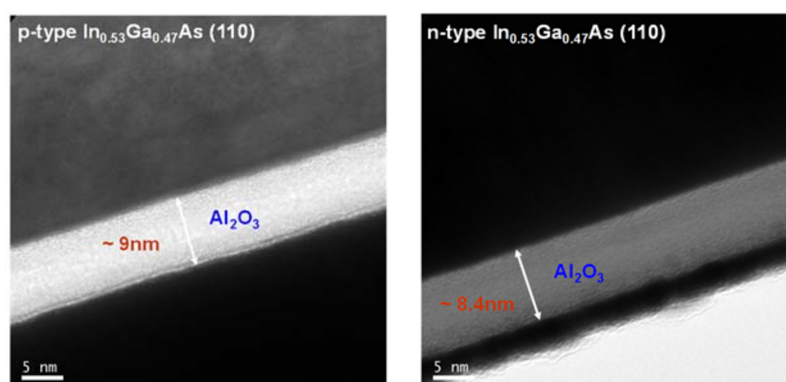
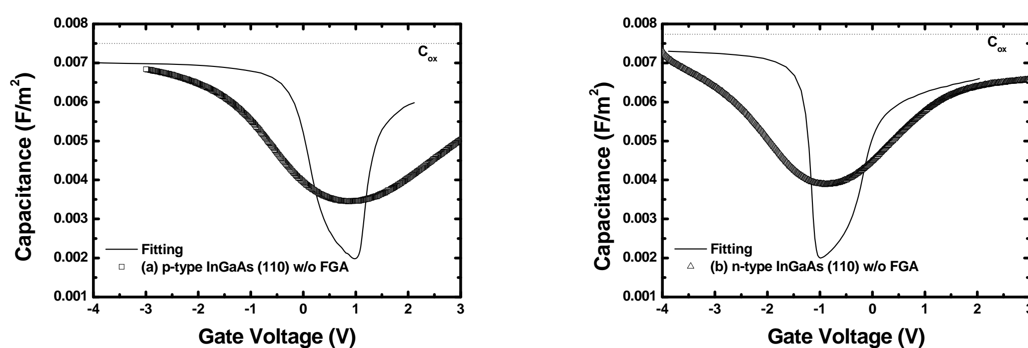


Fig. 6.4. TEM of p-type and n-type InGaAs (110) MOSCAPs after FGA.

6.4.1.4 Interface trap density

To quantify the D_{it} profiles of the p- and n-type samples before and after FGA as a function of the surface potential (ψ), a temperature modified version of the combined high-low frequency C-V method, discussed in Section 5.4.1, is employed. In the method, the 100 Hz capacitance response at room temperature was used along with the 1 MHz capacitor response measured at -50ºC. This method creates a more "ideal-like" C-V characteristic with less effect of interface defect response and therefore a more accurate estimation of the D_{it} distribution. The calculation of surface potential determined from the Berglund integral was split into two parts referred to the flatband voltage (V_{FB}). One integration is from the flatband voltage into accumulation, and the other from flatband voltage to weak inversion. The flatband voltage used in this integral, and in the further analysis, was obtained from the flatband capacitance using the C_{ox} derived from the technique discussed in the previous section.



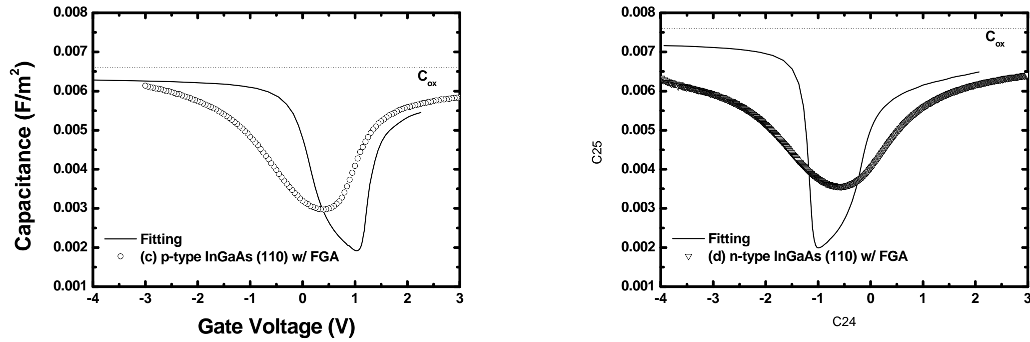


Fig. 6.5. The fitting of experimental low frequency C-V characteristics (1kHz) of Au/Pt/Al_2O_3/InGaAs (110) MOSCAPs (110) MOSCAPs are modelled in (a) p-type and (b) n-type before FGA, and (c) p-type and (d) n-type after FGA. Horizontal dotted lines shown in the diagrams indicates the C_{ox} values derived from a comparison between experimental and modelled C-V curves.

In Fig, 6.6, the resulting D_{it} distribution of the p-type and n-type (110) samples before (and after) FGA at the midgap are estimated to be 2.7×10^{12} (1.8×10^{12}) $cm^{-2}eV^{-1}$ and 2.2×10^{12} (8.7×10^{11}) $cm^{-2}eV^{-1}$, respectively. Furthermore, the U-shaped D_{it} profile of n-type sample after FGA close to conduction band edge is reduced by almost an order of magnitude and obtained with the minimum D_{it} value of 3.1×10^{11} $cm^{-2}eV^{-1}$. According to the label, the U-shaped profile is from samples after FGA. This indicates the combination of sulphur pre-treatment and FGA is advantageous in passivating trap states in the upper half of the bandgap of (110) oriented $In_{0.53}Ga_{0.47}As$. In addition, this work is comparable to the previous reported D_{it} profiles of sulphur passivated $In_{0.53}Ga_{0.47}As$ (100) and (111) oriented MOSCAPs. This shows the D_{it} profile in the upper half of the bandgap is comparable between different surface orientations of $In_{0.53}Ga_{0.47}As$ [6.10]. A D_{it} profile values to midgap below 1×10^{12} $cm^{-2}eV^{-1}$ suggests that there is minimal impact of subthreshold swing and off-current on Tunnel-FETs [6.26].

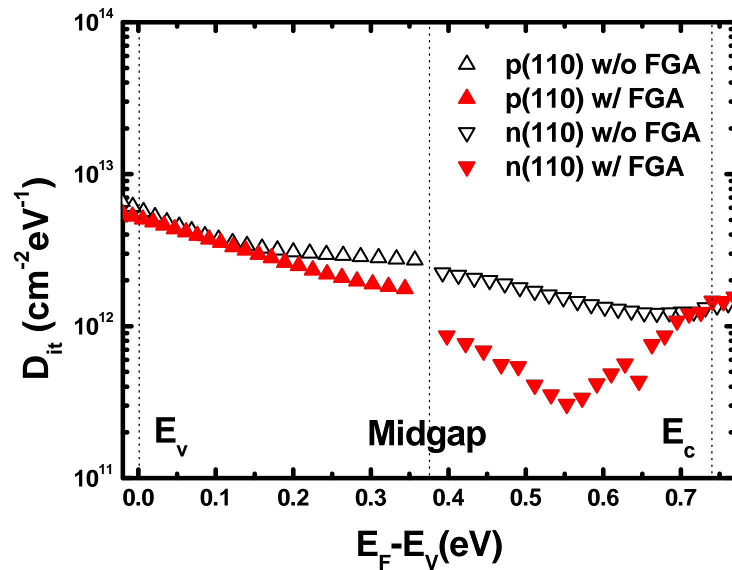


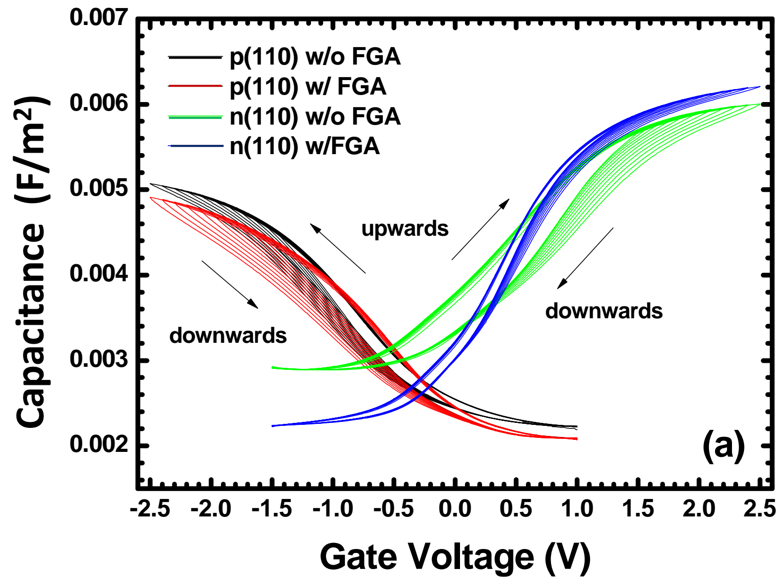
Fig. 6.6. Extracted D_{it} profile of p-type and n-type $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs before and after FGA.

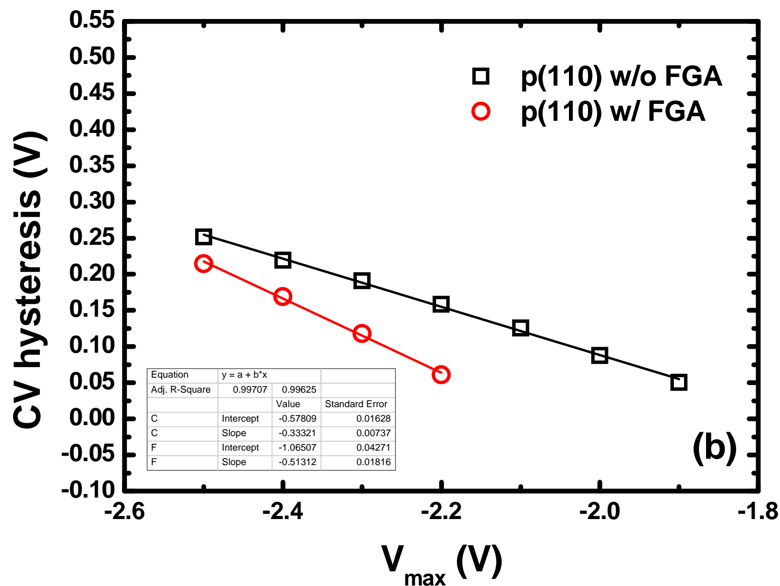
6.4.1.5 Border traps

Besides the D_{it} distribution, border traps, known as the active interface defect that can electrically communicate with the substrate by charge trapping/de-trapping, is also important from the perspective of device stability [6.27]. To investigate the border traps response of the samples before and after FGA, C-V hysteresis measured at room temperature starting from inversion and sweeping towards accumulation was analysed [6.28]. Fig. 6.7 shows the bi-directional CV sweeps of the p-type and n-type $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs, obtained for the increasing maximum gate bias in accumulation (V_{max}) before and after FGA. The bi-directional CV sweeps were performed at 1MHz to minimize the contribution of D_{it} to the C-V response as shown in Fig. 6.7 (a) [6.29]. The voltage hysteresis is taken to be the difference in flatband voltage observed from the upsweep to downsweep. A linear relationship between voltage hysteresis and V_{max} is obtained as shown in Fig. 6.7 (b) and 6.7 (c). This suggests the trapped charge density increases as the Fermi-level is moved towards the band edges. Compared with the sample without FGA, the FGA treatment result in a reduction in the CV hysteresis of both p- and n-type samples. For the p-type sample, the reduction in hysteresis after FGA treatment becomes less pronounces with V_{max}. This is in obvious contrast to the n-type sample for which the FGA treatment provides a larger (negative) significant reduction of CV hysteresis with larger (positive) V_{max}. To quantity the level of charge trapping in the samples. Equation 6.1 is used to quantify the amount of charge trapping.

$$N_t = \frac{C_{ox} \times \Delta V}{q}, \tag{6.1}$$

where N_t is the trapped charge density (cm^{-2}), ΔV is the CV hysteresis and q is the electronic charge. To enable to valid comparison, the same applied electric field across the oxide should be the same for all samples [6.28].





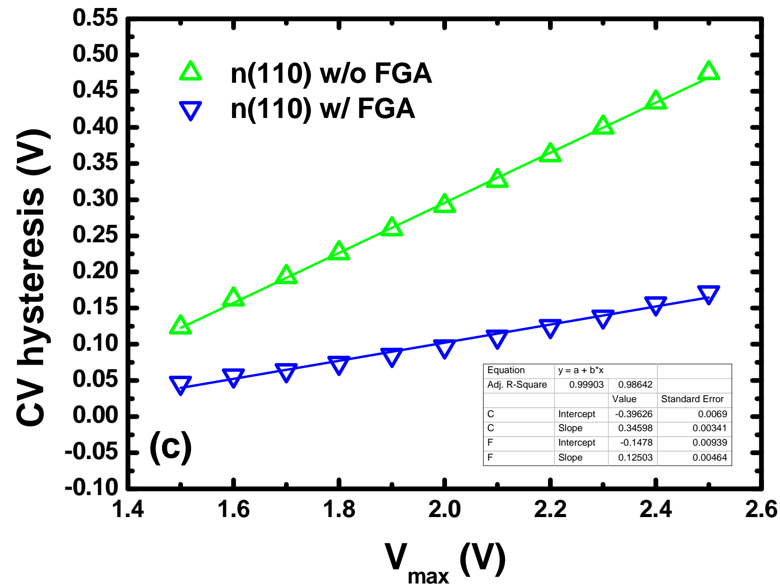


Fig. 6.7. (a) Bi-directional CV sweeps measured at 1MHz for $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs before and after FGA, using the same starting gate bias in inversion and increasing maximum gate bias in accumulation (V_{max}), with plots CV hysteresis as a function of V_{max} of (b) p-type and (c) n-type MOSCAPs, respectively.

This requires that the ΔV term in Equation 6.1 should be evaluated at the same value of $|V_{max} - V_{fp,up}|$, where $V_{fp,up}$ is the flatband voltage of the upward measurement sweep. Using this approach, the trapped charge density before (and after) FGA can be estimated to be 7.3×10^{11} (1.4×10^{12}) cm^{-2} for p-type MOSCAP and 1.8×10^{12} (5.3×10^{11}) with the $|V_{max} - V_{fp,up}|$ of 1.1V. It should be noted that CV hysteresis measured at 1MHz likely does not capture all border traps, as some border traps do exist within the oxide, with a spatial density that varies with depth into the oxide. Consequently, the trapped charge measured from CV hysteresis will determine the population of border traps whose time constants are comparable to, or longer than, that of the CV sweep. However, the approach described should remain useful as a technique to explore how the border traps with long time constants vary with FGA.

All samples show CV hysteresis following a relationship with respect to power-law $|V_{max} - V_{fp,up}|$ as shown in the log-log plot of Fig. 6.8. The voltage acceleration factor (γ), marked in the plot, is given by the exponent of the power-law dependence and is found to improve for both p-type and n-type $In_{0.53}Ga_{0.47}As$ MOSCAPs after FGA. It can be further seen as a projection of improved reliability at lower operation voltages [6.30].

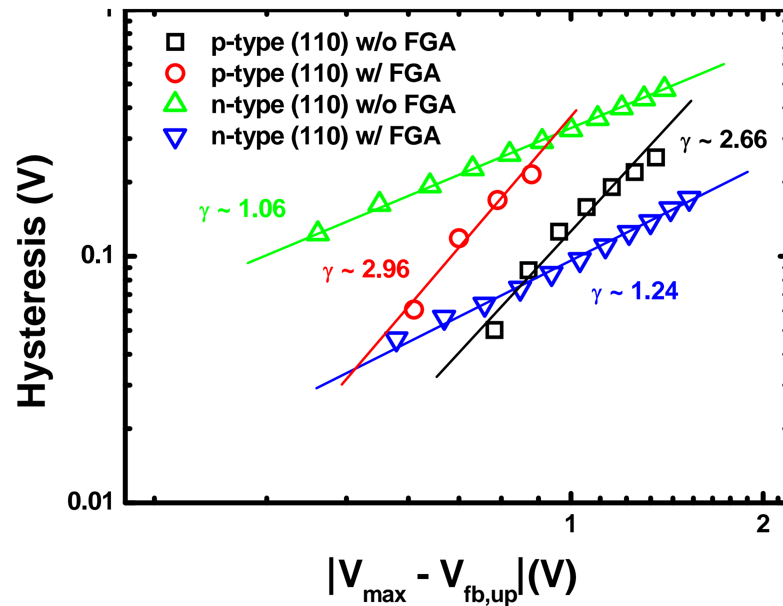


Fig. 6.8. CV hysteresis as a function of │$V_{max} - V_{fp,up}$│is illustrated in log-log scale for p-type and n-type InGaAs (110) samples before and after FGA.

6.4.2 Band parameters of $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) MOSCAPs

Although reducing D_{it} can result in superior subthreshold swing of device, providing sufficient conduction and valence band offset which acts as the barrier between high-κ and substrate is a requirement to lower off-current while reducing the physical thickness of the dielectric layer in the gate stack. The conduction band offsets of Al_2O_3 and HfO_2 on InGaAs (100) have been analysed by using the method of Fowler-Nordheim tunneling (F-N) current extraction. However, there is little information in the literature on the band parameters at the interfaces of $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) MOSCAPs. Work in this area is described in the following sections.

6.4.2.1 Gate Leakage

In Fig. 6.9., the leakage characteristics of the capacitors are plotted as a function of gate bias. All samples have leakage current density (J_g) in the range of 1×10^{-7} A/cm^2, orders of magnitude lower than the J_g requirement reported by International Technology Roadmap for Semiconductors.

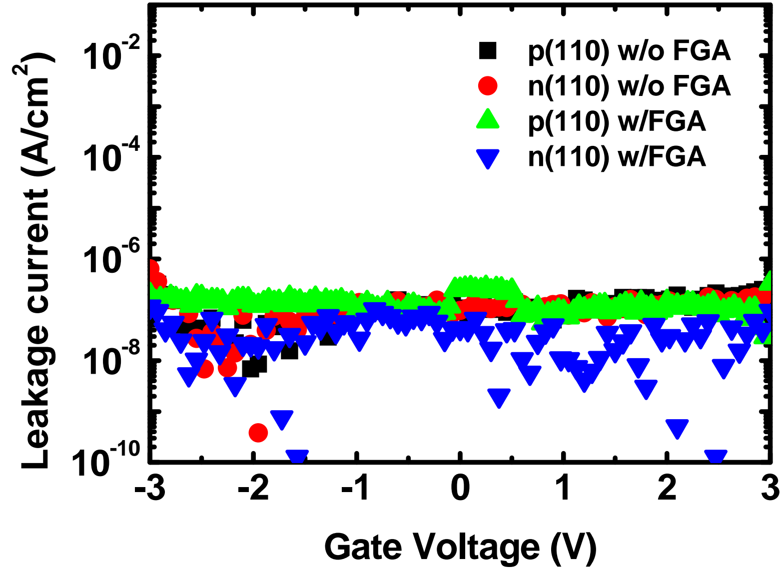


Fig. 6.9. The gate leakage characteristics of sulphur passivated $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) MOSCAPs before and after FGA.

6.4.2.2 Energy band parameters

The conduction band offset at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) interface can be obtained by the measurement of F-N tunneling current using the slope of log scaled J/E^2_{ox} as a function of E_{ox} where E_{ox} is the oxide electric field, given in Equation (6.2)

$$E_{ox}(V_g) = \frac{1}{\varepsilon_{ox}} \int_{V_{fb}}^{V_g} C(V_g)\, d\, V_g, \tag{6.2}$$

where ε_{ox} is the permittivity of the oxide and E_{ox} is equal to zero by given $V_g = V_{FB}$ [6.31]. In addition, the F-N tunneling current can be described as Equation (6.3)

$$\mathrm{S} = \frac{\mathrm{d}[\ln(J/E^2)]}{\mathrm{d}(1/E)} = \frac{4\sqrt{2m^*}}{3q\hbar}(\Phi)^{3/2}, \tag{6.3}$$

where m^* is the electron effective mass of Al_2O_3 and Φ is the tunneling barrier height. In terms as the conduction band offset, the barrier height under that condition of the forward bias can be expressed as $\Phi^+ = \Delta Ec$, where $\Delta Ec = \chi_s - \chi$, where χ and χ_s are the electron affinity of Al_2O_3 and InGaAs layers, respectively [6.32]. Relatively, the barrier height can be written as Φ^- equal to the difference of metal work function and electron affinity of Al_2O_3. The conduction band offset can be determined from $\Phi^+ - \Phi^-$ adopting the electron affinity of $In_{0.53}Ga_{0.47}As$ and the reported value of around 1.6 eV for conduction band offset between Al_2O_3 and InGaAs (100) [6.33]. Consequently, the conduction band offset between Al_2O_3 and InGaAs (110) is estimated to be 1.81 eV based on the diagrams shown in the Fig. 6.10.

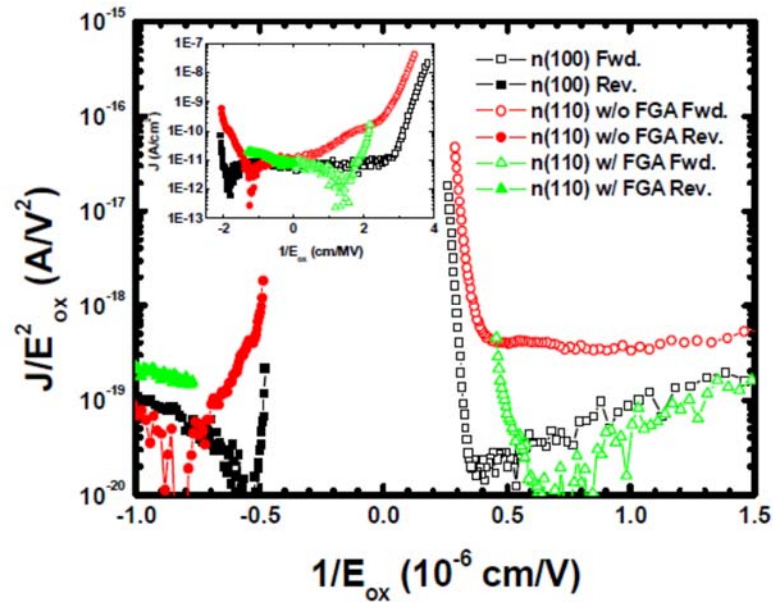


Fig. 6.10. Plot of log scaled J/E^2_{ox} as a function of E_{ox} for $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) and (110) MOSCAPs. The gate leakage characteristics is shown in the inset.

6.5 Chapter summary

An interface passivation technology with sulfur pre-treatment prior to ALD deposition has been demonstrated for the first time on both the p-type and n-type $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) MOSCAPs. In addition, the study indicates the combination of surface pre-treatment and a post-metal FGA enables significant Fermi level movement through the bandgap of both MOSCAPs. Quantitively, the D_{it} values were obtained to be in the range of 0.87-1.8 × 10^{12} $cm^{-2}eV^{-1}$ around the midcap energy level. The lowest D_{it} value is estimated to be 3.1 × 10^{12} $cm^{-2}eV^{-1}$ close to the conduction band edge. These data are in agreement with previous reports of sulphur passivated $In_{0.53}Ga_{0.47}As$ MOSCAPs on (100) and (111) orientation. This shows that the combination of sulphur passivation and FGA is effective to passivate the trap states in the upper half of the bandgap on $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) MOSCAPs. Furthermore, the border trap density on n-type MOSCAPs is reduced after FGA from 1.8 × 10^{12} cm^{-2} to 5.3 × 10^{11} cm^{-2} , determined from CV hysteresis biasing at 1.1V beyond the flatband voltage. The result observed in p-type MOSCAPs is in contrast with increasing border trap density from 7.3 × 10^{11} cm^{-2} to 1.4 × 10^{12} cm^{-2} under the similar bias condition before and after FGA. Consequently, the FGA is not as effective in passivating states close to the valence band. In addition, the conduction band offset of $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) is extracted using the method of Fowler-Nordheim current at first time. A value of 1.81eV is estimated by this approach.

6.6 Reference

[6.1] N. Goel, P. Majhi, C. O. Chui, W. Tsai, D. Choi and J. S. Harris,"InGaAs metal-oxide-semiconductor capacitors with HfO2~ gate dielectric grown by atomic-layer deposition", *Applied Physics Letters*. 89, 163517, 2006.

[6.2] J. A. Del Alamo, "Nanometre-scale electronics with III–V compound semiconductors", *Nature,* 479, 317-323, 2011.

[6.3] K. Tomioka, M. Yoshimura and T. Fukui, "A III-V nanowire channel on silicon for high-performance vertical transistors", *Nature,* 488, 189-92, 2012.

[6.4] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches", *Nature,* 479, 329-337, 2011.

[6.5] T. Kent et al., "The influence of surface preparation on low temperature HfO2 ALD on InGaAs (001) and (110) surfaces", *The Journal of Chemical Physics.* 143, 164711, 2015.

[6.6] J. Kim, E. Chagarov, J. Cagnon, Y. Yuan, A. C. Kummel, P. M. Asbeck, S. Stemmer, K. C. Saraswat and P. C. McIntyre, "Atomically abrupt and unpinned $Al_2O_3/In_{0.53}Ga_{0.47}AsAl_2O_3/In_{0.53}Ga_{0.47}As$ interfaces: Experiment and simulation", *Journal of Applied Physics,* 106, 124508, 2009.

[6.7] J. Ahn, T. Kent, E. Chagarov, K. Tang, A. C. Kummel and P. C. McIntyre, "Arsenic decapping and pre-atomic layer deposition trimethylaluminum passivation of Al_2O_3/InGaAs(100) interfaces", *Appl. Phys. Lett*., 103, 071602, 2013.

[6.8] A. D. Carter, W. J. Mitchell, B. J. Thibeault, J. J. M. Law and M. J. W. Rodwell, "Al_2O_3 growth on (100) $In_{0.53}Ga_{0.47}As$ initiated by cyclic trimethylaluminum and hydrogen plasma exposures", *Applied Physics Express,* 4, 091102, 2011.

[6.9] Q. H. Luc, E. Chang, H. D. Trinh, Y. C. Lin, H. Q. Nguyen, Y. Y. Wong, H. B. Do, S. Salahuddin and C. Hu, "Electrical Characteristics of n, p-$In_{0.53}Ga_{0.47}As$ MOSCAPs With In Situ PEALD-AlN Interfacial Passivation Layer", *IEEE Trans. Electron Devices,* 61, 2774, 2014.

[6.10] M. Yokoyama, N. Taoka, R. Suzuki, O. Ichikawa, H. Yamada, N. Fukuhara, M. Hata et al., "Sulfur cleaning for (100), (111)A, and (111)B InGaAs surfaces with In content of 0.53 and 0.70 and their Al_2O_3/InGaAs MOS interface properties", *Proc. Int. Conf. Indium Phosphide and Related Materials*, 167-170, 2012.

[6.11] Y.-C. Fu et al., "The impact of forming gas annealing on the electrical characteristics of sulfur passivated $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) metal-oxide-semiconductor capacitors", *Applied Physics Letters*., 110, 14, 2017.

[6.12] Y.-C. Fu, U. Peralagu, O. Ignatova, X. Li, R. Droopad, I. Thayne, J. Lin, I. Povey, S. Monaghan and P. Hurley, "Energy-Band Structure of Atomic Layer Deposited Al_2O_3 & Sulphur Passivated Molecular Beam Epitaxially Grown (110) $In_{0.53}Ga_{0.47}As$ Surfaces", In: *11th Conference on PhD Research in Microelectronics and Electronics (IEEE PRIME 2015),* Glasgow, UK, 29 June - 2 July 2015,

[6.13] E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace and P. K. Hurley, "A systematic study of (NH4)(2)S passivation (22%, 10%, 5%, or 1%) on the interface properties of the $Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ system for n-type and p-type $In_{0.53}Ga_{0.47}As$ epitaxial layers", *J. Appl. Phys.* 109, 024101, 2011.

[6.14] E.J. Kim, L. Wang, P. M. Asbeck, K. C. Saraswat and P. C. McIntyre, "Border traps in $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) gate stacks and their passivation by hydrogen anneals", *Applied Physics Letters.* 52 (1): 012906, 2010.

[6.15] S, Yoshida, S. Taniguchi, H. Minari, D. Lin, T. Ivanov, H. Watanabe, M. Nakazawa, N. Collaert and A. Thean, "The impact of energy barrier height on border traps in the metal insulator semicondoctor gate stacks on III–V semiconductors", *Japanese Journal of Applied Physics*. 55 (8S2): 08PC01l, 2016.

[6.16] Y. Yuan, L. Wang, B. Yu, P.M. Asbeck, Y. Taur et al., "A distributed model for border traps in Al_2O_3 - InGaAs MOS devices", *IEEE Electron Device Letters.* 32 (4): 485-487, 2011.

[6.17] N. Taoka, M. Yokoyama, S. H. Kim, R. Suzuki, T. Hoshii, R. Iida, S. Lee et al., "AC response analysis of C–V curves and quantitative analysis of conductance curves in Al_2O_3/InP interfaces", *Microelectronic Engineering*. 88 (7): 1087-1090, 2011.

[6.18] G. Brammertz, H-C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, "On the interface state density at $In_{0.53}Ga_{0.47}As$/oxide interfaces", *Applied Physics Letters*. 95 (20): 202109, 2009.

[6.19] E. Nicollian, and J. Brews, *MOS Physics and Technology*. Wiley, New Jersey, 2002.

[6.20] H. D. Trinh, E. Y. Chang, P. W. Wu, Y. Y. Wong, C. T. Chang, Y. F. Hsieh, C. C. Yu, H. Q. Nguyen, Y. C. Lin, K. L. Lin, and M. K. Hudait, "The influences of surface treatment and gas annealing conditions on the inversion behaviors of the atomic-layer-deposition $Al_2O_3/n\text{-}In_{0.53}Ga_{0.47}AsAl_2O_3/n\text{-}In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitor", *Applied Physics Letters*, 97, 042903, 2010.

[6.21] Y. C. Chang, M. L. Huang, K. Y. Lee, Y. J. Lee, T. D. Lin, M. Hong, J. Kwo, T. S. Lay, C. C. Liao, and K. Y. Cheng, "Atomic-layer-deposited HfO_2 on $In_{0.53}Ga_{0.47}AsIn_{0.53}Ga_{0.47}As$: Passivation and energy-band parameters", *Applied Physics Letters*, 92, 072901, 2008.

[6.22] P. K. Hurley, R. Long, T. O'Regan, E. O'Connor, S. Monaghan, V. Djara, M. A. Negara, A. O'Mahony, I, Povey, A. Blake, R. Nagle, D. O'Connell, M. Pemble, and K. Cherkaoui, "Equivalent Oxide Thickness Correction in the High-k/$In_{0.53}Ga_{0.47}As$/InP System", *ECS Transactions*, 33, 433, 2010.

[6.23] S. Luryi, "Quantum capacitance devices", *Applied Physics Letters*, vol. 52, no. 6, pp. 501-503, 1988.

[6.24] E. O'Connor, K. Cherkaoui, S. Monaghan, B. Sheehan, I. Povey, and P. Hurley, "Effect of forming gas annealing on the inversion response and minority carrier generation lifetime of n and p-$In_{0.53}Ga_{0.47}As$ MOS capacitors", *Microelectronic Engineering*. 147, 325-329, 2015.

[6.25] R. Engel-Herbert, Y. Hwang, and S. Stemmer, "Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces", *J. App. Phys*., vol. 108, p. 124101, 2010.

[6.26] U.E. Avci et al., "Study of TFET non-ideality effects for determination of geometry and defect density requirements for sub-60mV/dec Ge TFET", *Technical Digest - International Electron Devices Meeting,* IEDM. 2016-February, 34.5.1-34.5.4.

[6.27] D. M. Fleetwood, M. R. Shaneyfelt, W. L. Warren, and J. R. Schwank,"Border traps: issues for MOS radiation response and long-term reliability", *Microelectronics and Reliability*. 35, 403, 1995.

[6.28] J. Lin, Y. Y. Gomeniuk, S. Monaghan, I. M. Povey, K. Cherkaoui, E. O'Connor, M. Power, and P. K. Hurley, "An investigation of capacitance-voltage hysteresis in metal/high-k/$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors", *J. Appl. Phys*. 114, 144105, 2013.

[6.29] E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace and P. K. Hurley, "A systematic study of (NH4)(2)S passivation (22%, 10%, 5%, or 1%) on the interface properties of the Al2O3/In0.53Ga0.47As/InP system for n-type and p-type In0.53Ga0.47As epitaxial layers", J. Appl. Phys. 109, 024101, 2011.

[6.30] A. Seabaugh, Z. Jiang, and G. Klimeck, *III-V tunnel transistors. In: CMOS and Beyond: Logic Switches for Terascale Integrated Circuits*, K. Kuhn and T.-J. King-Liu, Eds. Cambridge, U.K.: Cambridge Univ. Press, 2014.

[6.31] E. Rosenbaum, and L. F. Register, "Mechanism of stress-induced leakage current in MOS capacitors", *IEEE Trans. Electron Devices*, 44, 317, 1997.

[6.32] M. L. Huang, Y. C. Chang, Y. H. Chang, T. D. Lin, J. Kwo, and M. Hong, "Energy-band parameters of atomic layer deposited Al_2O_3 and HfO_2 on InxGa1−xAs", *Appl. Phys. Lett.,* 94, 052106, 2009.

[6.33] M. L. Huang, Y. C. Chang, T. D. Lin, J. Kwo, T.B. We, and M. Hong, "Energy-band parameters of atomic-layer-deposition Al_2O_3 / InGaAs heterostructure", *Appl. Phys. Lett*.,89, 012903, 2006.

VII. Enhanced scalability of gate stack on less-damaged $In_{0.53}Ga_{0.47}As$ (110) epi-layers

7.1 Introduction

As discussed in Chapter IV, the realisation of non-planar Tunnel-FETs on III-V materials requires a high performance gate stack on both the top and sidewalls of the fins and wires that have various crystallographic orientations. In Chapter VI, the FGA effect on improving the interface defect density of InGaAs (110) gate stack has been demonstrated. Continuously, there is desire in the practical situation to assess those MOSCAPs on various surface orientations that have been subjected to the etching processes. Therefore, the cluster tool based on ICP etch and ALD tools, introduced in Chapter III, offers the benefit of excluding native oxide formation on etched surfaces and performing a sequence of etch processes to form highly anisotropic structures and in-situ ALD deposition without wet chemical cleaning/passivation treatments. In this work, (100)- and (110)-oriented InGaAs MOSCAPs which have been subjected to the optimized etching condition, a $Cl_2/CH_4/H_2$ based ICP chemistry, are studied. In addition, the preparation of low D_{it} native III-V surfaces are accomplished by cyclic trimethylaluminum (TMA) precursor and plasma gas pre-treatment with N_2 and H_2 prior to high-κ gate dielectric layer deposition. Furthermore, accomplishing an ultimate scaled gate stack on both InGaAs (100) and (110) orientation is required for steep subthreshold swing and large drive current Tunnel-FETs [7.1], as discussed in Chapter IV. To achieve a scaled gate stack, the effectiveness of inserting a TiN capping layer, commonly used to scavenge oxygen between the dielectric layer and the semiconductor, into both InGaAs (100) and (110) MOSCAPs is also investigated. In the following sections, the effectiveness to mitigate etch damage with TMA/plasma H_2 gas will be first discussed with reference to electrical and chemical analysis. This is followed by an explanation of the difficulties of scaling the gate stack by only reducing the thickness of the dielectric layer. Finally, the electrical properties of a scaled MOSCAP on less damaged (100) and (110) orientated InGaAs are reported.

7.2 Damage elimination on $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs

7.2.1 Function of plasma gas pre-treatment

The cyclic TMA/plasma gas pre-treatment prior to ALD deposition, for instance plasma H_2 and N_2, which enables low interface defect density around the mid-gap on InGaAs MOSCAP, has been demonstrated [7.2]. It has been reported that TMA/plasma H_2 is more effective to improve surface quality of InGaAs MOSCAP compared to TMA/plasma N_2. However, in addition to the influence of native oxide, the process of etching may cause surface damage, which causes performance degradation of MOSCAPs, due to insufficient cleaning/passivation after etching process even if sulphur passivation is employed [7.3]. Therefore, alternative in-situ cyclic precursor and plasma gas pre-treatments have been investigated for the effectiveness of damage mitigation from ICP dry etch in this work, based on cluster tool excluding the factor of native oxide formation.

7.2.2 C-V characteristics

The process flow of realising InGaAs (100) and (110) MOSCAPs subjected to the ICP etching has been introduced in section 5.2. Fig. 7.1 shows the C-V characteristics of in-situ Au/Pt/HfO_2 (25 cycles)/ etched (100)- and (110)-oriented n-$In_{0.53}Ga_{0.47}As$/InP MOSCAP with FGA (top and bottom row) subjected to either 10 cycles of TMA/plasma N_2 or TMA/plasma H_2 pre-treatments. measured at 295K. Qualitatively, according on the C-V curves, the control samples (before cyclic plasma/TMA treatments) show that the InGaAs (110) surfaces suffer larger etch damage than the InGaAs (100) surfaces. After cyclic plasma/TMA treatment, the in-situ etched (100) MOSCAP shown in the top row of Fig. 7.1 have a slight reduction in frequency dispersion and bumps around mid-gap. Both parameters were improved significantly in the (110) MOSCAP shown in the bottom row of Fig. 7.1 especially for plasma H_2. According to the similar result in [7.4], plasma H_2 is more effective in removing surface layers than plasma N_2. It can be assumed that there are more As-O bonds at the interface between HfO_2 and etched (110) surfaces when excluding the factor of native oxide left on etched interface. Therefore, plasma H_2 is more effective in mitigating etch damage. Furthermore, the metrics of frequency dispersion in accumulation, stretch-out and hysteresis of all capacitors are captured in Fig. 7.2 that also reports the percentage variation of the metrics for capacitors, with plasma N_2 and H_2 pre-treatment compared to the control samples. In relation to both control (100) and (110) samples, ~17% and ~49% increases in dC/dV with H_2 pre-treatment and ~5% and ~18% with plasma N_2 pre-treatment were observed, respectively. This also shows that plasma H_2 is more effective to mitigate the etch damage on both oriented InGaAs layers. In

addition, the hysteresis was improved by both plasma gas pre-treatments on these etched surfaces.

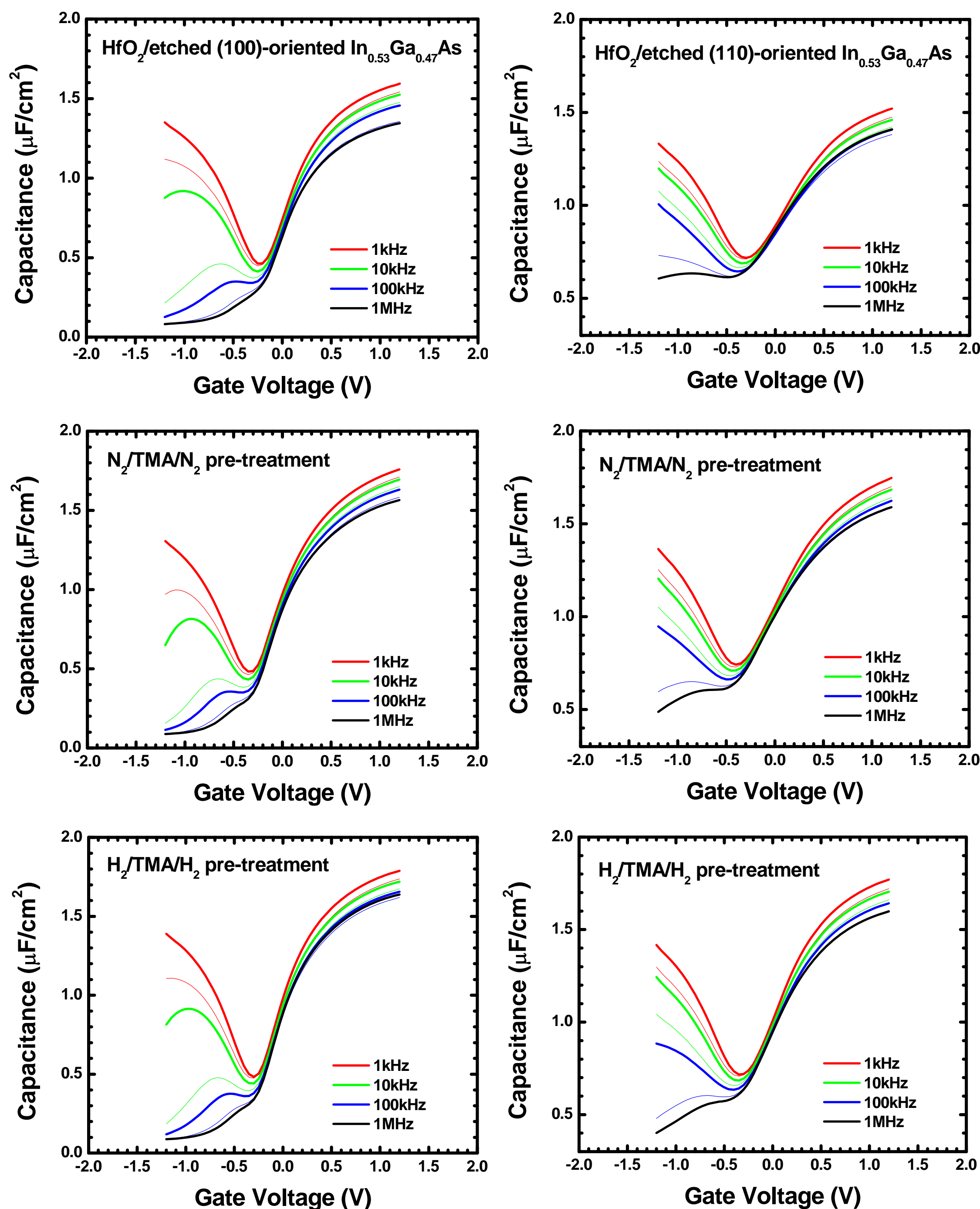


Fig. 7.1. Room temperature C-V frequency variation of in-situ Au/Pt/HfO_2 (25 cycles)/ etched (100)- and (110)-oriented n-$In_{0.53}Ga_{0.47}As$/InP MOSCAP with FGA (top and bottom row) subjected to without and with 10 cycles of TMA/plasma N_2 or TMA/plasma H_2 pre-treatment.

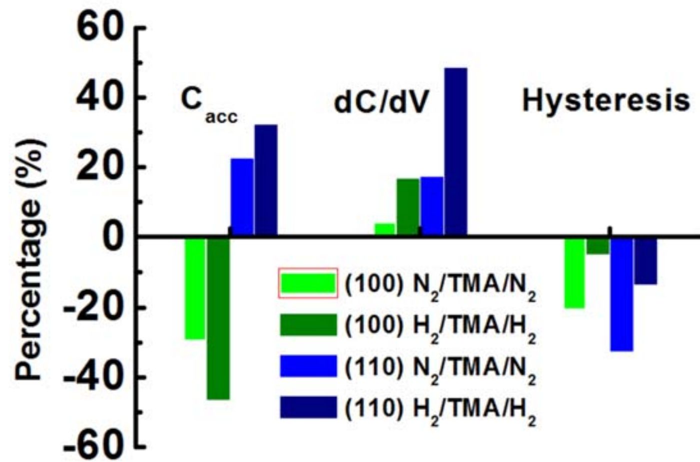


Fig. 7.2. The metrics of frequency dispersion in accumulation, stretch-out and hysteresis of all capacitors.

7.2.3 G-V characteristics

Based on the conductance method [7.5], the interface trap density can be determined by the parallel conductance peak that is obtained by the equivalent circuit for a MOS capacitor in depletion without minority carrier response and given by [7.5]:

$$G_p = \frac{\omega^2 {C_{ox}}^2 G_m}{{G_m}^2 + \omega^2 (C_{ox} - C_m)^2}, \tag{7.1}$$

where ω is the angular frequency of ac signal. The time constant of interface trap (τ) physically represents the average response time before the interface trap captures mobile carriers. The formula can be approximately considered as [7.6]:

$$\frac{G_p}{\omega} = \frac{\omega\tau}{1+\omega^2\tau^2}, \tag{7.2}$$

where the trap time constant is much shorter than the period of the excitation signal given by impedance analyser. That indicates there is no energy loss for interface traps that can rapidly change the occupation. In addition, there is also no energy loss for the longer period when the interface traps cannot follow the ac signals. The considerable energy loss only occurs between the above two cases when the angular frequency is comparable to the trap constant time. The trap response is just delayed behind the AC signal. As a result, the value of interface defect density can be estimated by:

$$D_{it} = \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{max}, \tag{7.3}$$

where A is the area of a MOS capacitor and q is the elementary charge. In Fig. 7.3, the map of parallel conductance as a function of gate bias and frequency measured at 14K for (110)-oriented n-$In_{0.53}Ga_{0.47}As$ with and without in-situ H_2 plasma pre-treatment is shown. According to the maximum value across the map, the conductance peak of sample with H_2 plasma pre-treatment moves vertically with less frequency dependent shifts, which indicates the band bending is more efficient, compared to the sample without H_2 plasma pre-treatment which indicates the Fermi-level is pinned around the band edge of conduction band. As discussed in Section 5.4, the Berglund integral has been introduced to extract the energy level of the interface traps in the band gap. However, there are some issues using this analysis for scaled InGaAs MOSCAPs as the Fermi level can move deep into conduction band due to low DOS that overestimates the semiconductor band bending without including the contribution of density of state capacitors. Therefore, the trap energy position is obtained by the trap time constant given by Shokley-Read-Hall statistics of capture and emission rate [7.7].

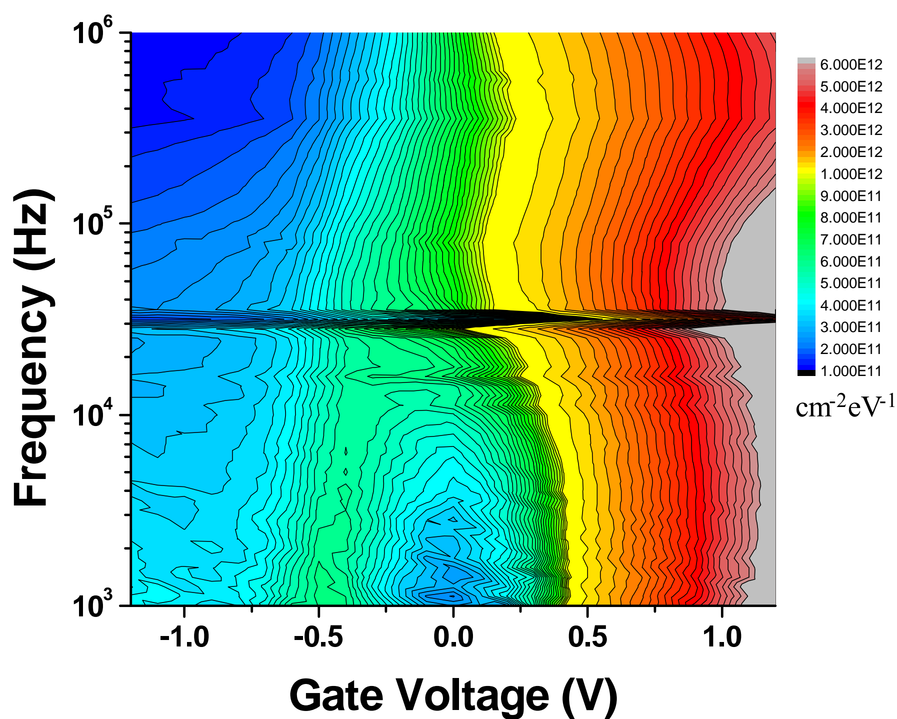
$$\tau = \frac{1}{n_s v_{th} \sigma}, \tag{7.4}$$

where n_s is the carrier concentration of semiconductor, v_{th} is the thermal velocity and σ is the capture cross-section. Furthermore, the n_s for the interface traps inside the band-gap can be approximately estimated by:

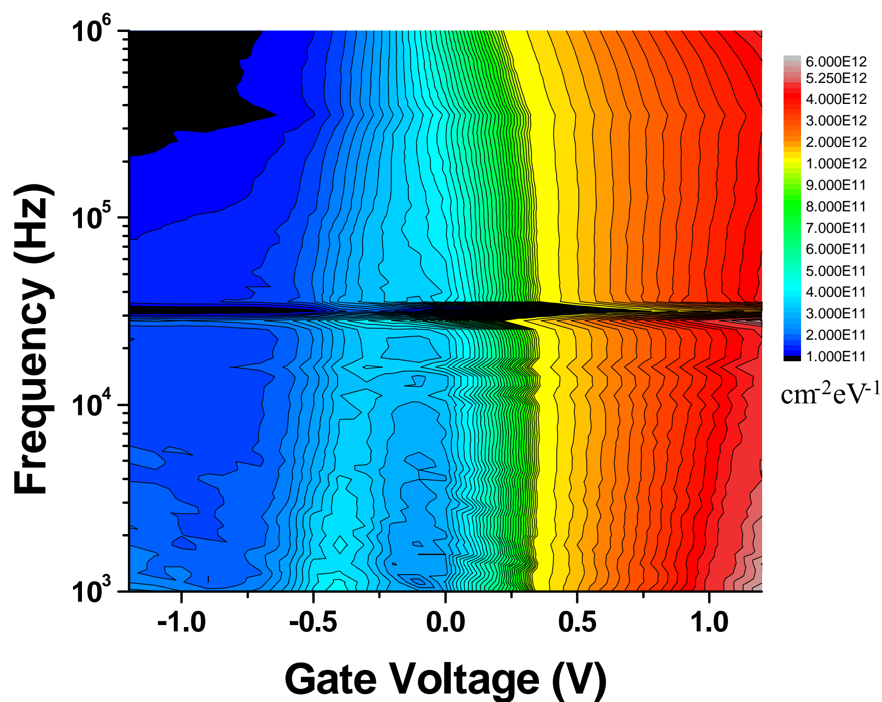
$$n_s = N_{DOS} e^{-(\Delta E/kT)}, \tag{7.5}$$

where N_{DOS} is density of state for conduction or valence band. ΔE represents the energy difference of trap and the band edge. k and T is the Boltzmann constant and absolute temperature. Using Equation 7.5 to substitute Equation 7.4, the trap time constant can be written as:

$$\tau = \frac{\exp(\Delta E/kT)}{N_{DOS} v_{th} \sigma}, \tag{7.6}$$



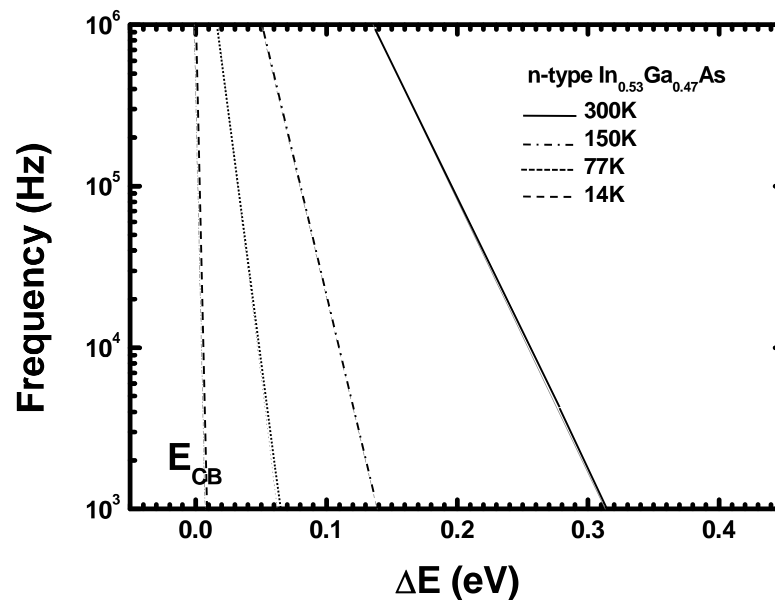
(a)



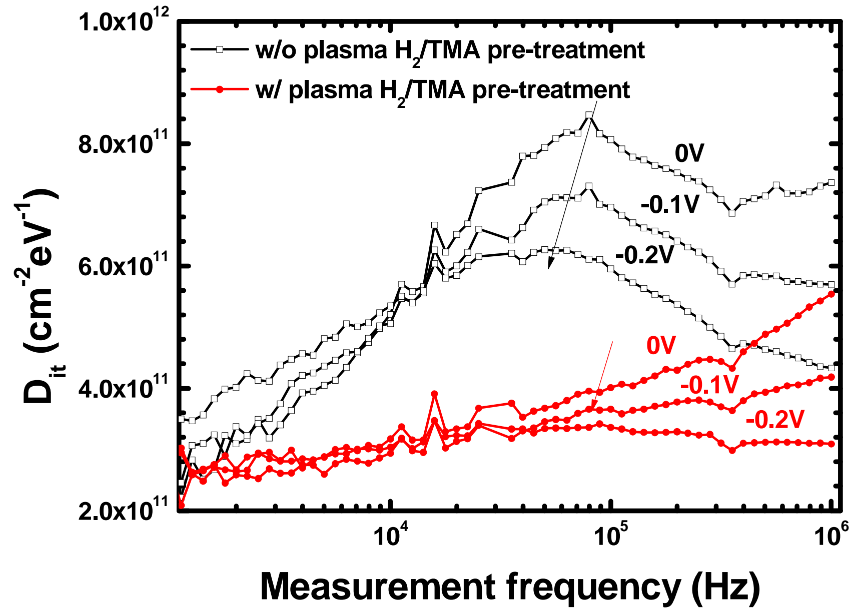
(b)

Fig. 7.3. Map of parallel conductance as a function of gate voltage and frequency for (110)-oriented n-$In_{0.53}Ga_{0.47}As$/InP MOSCAP (a) without and (b) with in-situ plasma H_2 pre-treatment.

Based on Equation (7.6), it is obvious that the trap time constant exponentially decreases with temperature. Furthermore, using the condition of $\omega\tau = 1$, the interface trap energy position can be characterized at the frequency related to the trap time constant. Therefore, the frequency as a function of energy differences between traps energy level to the band edge with specific parameters of N_{DOS}, v_{th}, σ from $In_{0.53}Ga_{0.47}As$ under the condition of 14K, 77K, 150K and 300K is estimated shown in Fig. 7.4 (a). According to the curves, the parallel conductance peak characterized at the condition of 14K can only detect the traps close to the band edge. For the sample of in-situ InGaAs (110) MOSCAPs with and without plasma H_2 pre-treatment, the parallel conductance peak is only obvious at 14K. The parallel conductance peak at the condition of 14K is extracted in Fig. 7.4 (b). Based on the diagram of Fig. 7.4 (a) and (b), the interface trap density of in-situ InGaAs (110) MOSCAPs with and without plasma H_2 pre-treatment is $6\,x\,10^{11}\,cm^{-2}eV^{-1}$ and $2.8\,x\,10^{11}\,cm^{-2}eV^{-1}$around the conduction band, respectively, based on the curves of Fig. 7.4 (b) at the condition of -0.2V. As a result, it represents that plasma H_2 pre-treatment can reduce the traps caused by etching damage.



(a)

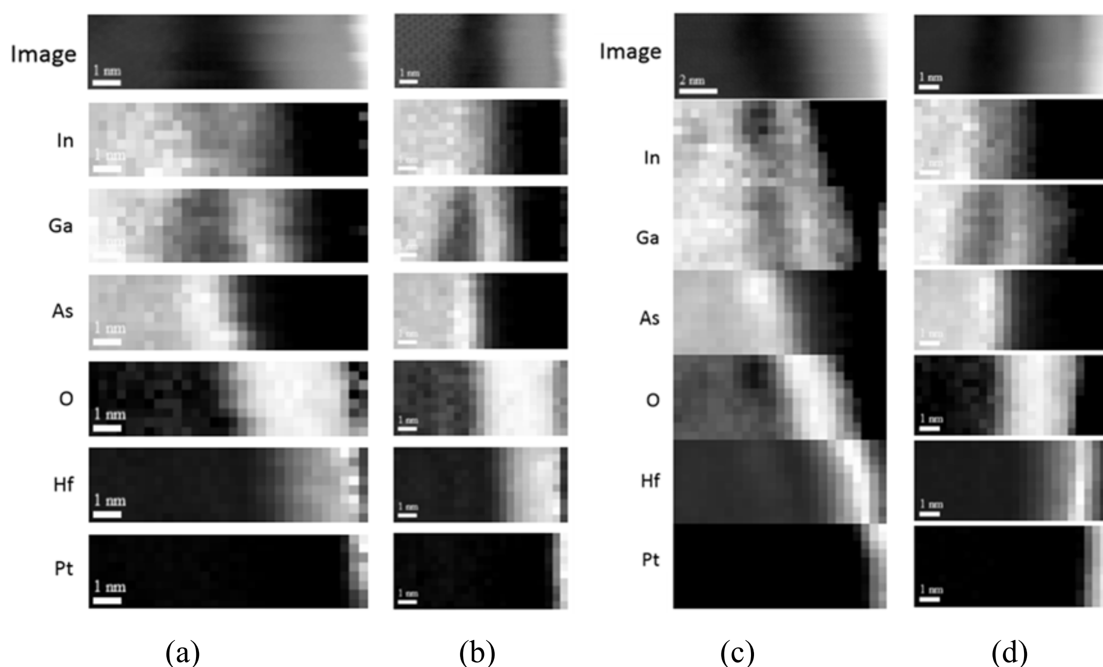


(b)

Fig. 7.4. (a) the plot of trap response frequency as a function of trap energy level obtained by Equation 7.6 using the parameter of a capture cross section $\sigma = 1\ x\ 10^{-16} cm^{-2}$, the values of average thermal velocity obtained and majority band of DOS obtained by equation of $v_{th} = \sqrt{3k_{\boldsymbol{B}}T/m^*}$ [7.8] and , $D_{dos} = 2(2\pi m^* k_B T/h^2)^{2/3}$ [7.8] respectively and (b) the D_{it} value as a function of measurement frequency

7.2.4 Interfacial layers

Based on the electrical analysis in the Section 7.2.3, the InGaAs (110) MOSCAPs subjected to an ICP etch are improved via TMA/plasma H_2 pre-treatment prior ALD deposition. However, the capacitance equivalent thickness (CET) of these MOSCAPs is rather large (>2nm), based on the value of C_{max} in the accumulation region, to provide high electrical field for the enhancement of Tunnel-FET performance [7.9]. According to C_{ox} of ideal modelled C-V curve, the CET of both (100) and (110) with or without plasma gas pre-treatment is still be higher than 1.5nm, but for a high performance Tunnel-FET [7.1]. EOT should around 1nm. High resolution STEM is provided in Fig. 7.5 to inspect the interface region of these in-situ etched InGaAs (100) and (110) MOSCAPs including the sample with and without plasma pre-treatment in H_2 gas.



(a) (b) (c) (d)

Fig. 7.5. EELS map of Au/Pt/HfO_2 (25 cycles)/etched (100)-oriented n-$In_{0.53}Ga_{0.47}As$/InP MOSCAP with FGA (a) without and (b) with 10 cycles of TMA/plasma H_2 pre-treatment and Au/Pt/HfO_2 (25 cycles)/etched (110)-oriented n-$In_{0.53}Ga_{0.47}As$/InP MOSCAP with FGA (c) without and (d) with 10 cycles of TMA/plasma H_2 pre-treatment.

The layer between HfO_2 and InGaAs (100) and (110) which may result in the difficulties of EOT scaling on MOSCAPs is clearly shown by the STEM imaging. As shown in Fig 7.5, the appearance of In and Ga migrating is observed based on the increase of As concentration in the substrate. Meanwhile, similar trend is obtained in the X-ray maps. Also, these indicate that the intermixed region has little Hafnium. Both intermixing layers on InGaAs (100) and (110) surfaces seem to be reduced after plasma pre-treatment. Therefore, it assumed that the interfacial layer may result from GaO_x or AsO_x between HfO_2 and etched (100) and (110) surfaces. Next, XPS technique is utilized for further material analysis.

7.2.5 Material analysis

The electrical results show a difference between capacitors processed on (100) and (110) InGaAs substrates that have been identically fabricated by plasma etching of the InGaAs surface and followed by in-situ ALD of HfO_2. Based on TEM result, an interlayer is observed between HfO_2 and InGaAs substrate, Hence, X-ray photoelectron spectroscopy

(XPS) is utilized to understand the source of the differences between the (100) and (110) oriented InGaAs MOSCAPs.

Based on the experimental details and XPS result, the observations can be summarized as,

- For all the samples that has been fabricated by plasma etching of InGaAs surface and followed by in-situ ALD of HfO_2, there is sub-peak presenting on the higher binding energy side to the main As 3d peak, referring to As-O bond. Based on the fitting of two spin-orbit components, AsO_x can refer to As $3d_{5/2}$ and As $3d_{3/2}$ in Fig. 7.6. These sub-peaks shift toward binding energy after FGA for both (100) and (110) InGaAs MOSCAPs without H_2/TMA plasma pre-treatment, from ~43.5eV to 43.4 eV for As-O As $3d_{5/2}$ component (Fig.7.6, Table 7.1). The biggest difference between the (100) and (110) oriented structures occurs around the As-O bond peak.For (100) orientation, there is no significant change in the area of AsO_x sub-peak after FGA. In contrast, the area of AsO_x sub-peak for (110) orientation is significantly reduced after FGA and also appears to be smaller than (100) orientation with FGA. It can be deduced that $HfO_2/In_{0.53}Ga_{0.47}As$ (110) MOSCAP after FGA has the smaller and more stoichiometric AsO_x interfacial layer (the centroid shifts to lower binding energy (BE); less defective) in comparison to all the other samples.
- Some difference can be seen in the Ga $2p_{3/2}$ peak in Fig. 7.7. The regions of Ga $2p_{3/2}$ are broadened for the FGA samples. This could indicate a small amount of Ga_2O_3 present in HfO_2/InGaAs MOSCAPs after FGA. In addition, (110)-oriented InGaAs surface seems to be more prone to oxygen compared to (100)-oriented InGaAs surface based on the observation of the sub-peak to Ga $2p_{3/2}$ which refers to Ga-O bond is more pronounced for (110) orientation than for (100) shown in Fig.7.8 and Fig.7.9 and Table 7.2 and Table 7.3
- For the sample of HfO_2/InGaAs (100) MOSCAP after FGA, the intensity of In-O is slightly reduced in comparison to the sample without FGA. On the contrary, the InO intensities of HfO_2/InGaAs (110) MOSCAP after FGA slightly increased. This may indicate some oxygen is bonded to In due to the significant decrease of As-O intensities. Furthermore, InOx at the interface is less affected by orientation than AsO_x where more pronounced change has been observed for the sample of different InGaAs orientation after FGA.

Based on the material analysis above and aforementioned electrical characterisation, compared to the (100) oriented InGaAs surfaces, the etched InGaAs (110) surfaces are more influenced by AsO_x bonding which appears to be the origin for the degradation of the C-V characteristics. This is an interesting observation as both sets of samples were fabricated together using the cluster tool. Furthermore, it can be assumed that the AsO_x intensities may drop after plasma TMA/H_2 plasma pre-treatment.

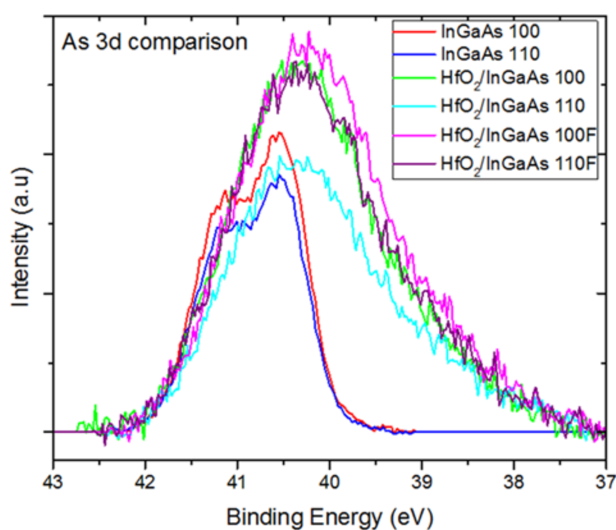


Fig. 7.6. XPS As 3d of HfO_2/InGaAs (100) and (110) samples with and without FGA.

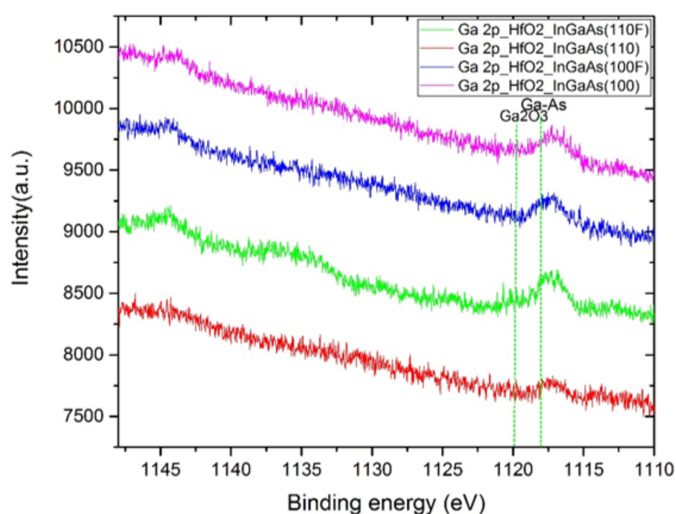


Fig. 7.7. XPS Ga 2p of HfO_2/InGaAs (100) and (110) samples with and without FGA.

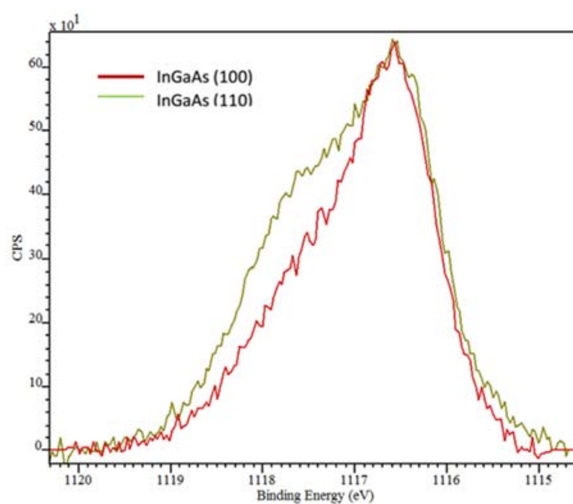


Fig. 7.8. Ga 2p comparison of InGaAs (100) and (110) blanket samples.

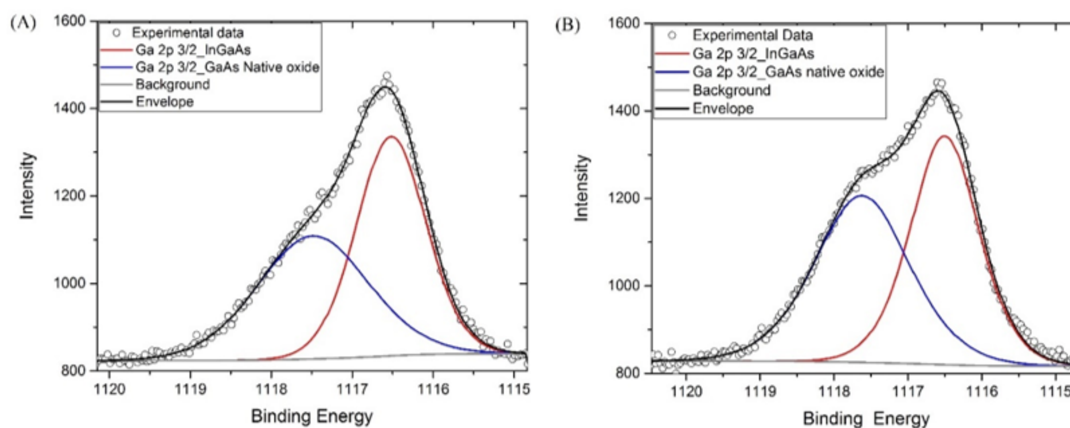


Fig. 7.9. Deconvoluted XPS Ga $2p_{3/2}$ for: (a) InGaAs (100) and (b) InGaAs (110).

Sample name	Sample description
HfO_2/InGaAs (100)	HfO_2/InGaAs (100) without FGA
HfO_2/InGaAs (100) F	HfO_2/InGaAs (100) with FGA
HfO_2/InGaAs (110)	HfO_2/InGaAs (110) without FGA
HfO_2/InGaAs (110) F	HfO_2/InGaAs (110) with FGA
InGaAs (100)	blanket InGaAs (100)
InGaAs (110)	blanket InGaAs (110)

Table 7.1. Sample name and description.

Sample name	As 3d 5/2 InGaAs (BE)	As 3d 3/2 InGaAs (BE)	As 3d 5/2 As_2O_3 (BE)	As 3d 3/2 As_2O_3 (BE)	Hf-O 5P1/2 (BE)
HfO_2/InGaAs 100	40.14	40.84	43.47	44.17	38.90
HfO_2/InGaAs 100 F	40.02	40.72	43.36	44.06	38.71
HfO_2/InGaAs 110	40.20	40.90	43.52	44.22	38.91
HfO_2/InGaAs 110 F	40.18	40.88	43.41	44.04	39.08
InGaAs 100	40.52	41.22	**NA**	**NA**	**NA**
InGaAs 110	40.52	41.21	**NA**	**NA**	**NA**

Table 7.2. As 3d comparison of blanket InGaAs (100) and (110) samples and HfO_2/InGaAs (100) and (110) samples with and without FGA.

Sample type	Ga 2p 3/2_InGaAs		Ga 2p 3/2_GaAs native oxide	
	Position (eV)	FWHM	Position (eV)	FWHM
InGaAs 100	1116.52	1.01	1117.49	1.62
InGaAs 110	1116.50	1.08	1117.62	1.50

Table 7.3. Ga 2p comparison of blanket InGaAs (100) and (110) samples.

Sample type	Ratio of Ga oxide and elemental Ga peak intensity
InGaAs 100	0.90
InGaAs 110	1.01

Table 7.4. Ratio of Ga oxide to the elemental Ga on blanket InGaAs (100) and (110) samples.

7.3 Realisation of sub-1nm EOT $In_{0.53}Ga_{0.47}As$ (100) and (110) MOSCAPs

From the perspective of novel InGaAs Tunnel-FETs [7.10], a low interface density is mandatory for simultaneous exploitation of the steep subthreshold swing and drive current properties that these devices offer [7.11]. Previous sections showed scaled, high performance $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs by using in-situ plasma gas passivation prior to ALD of the gate dielectric. However, the enhancement of drive current on Tunnel-FETs still requires an aggressively scaled gate stack. As discussed in Section 7.2.4, the formation of an interfacial layer, as observed by TEM, in a series of oxide capacitor decreases the total capacitance, and as a result, the EOT evaluated from $HfO_2/In_{0.53}Ga_{0.47}As$ (100) and (110) MOSCAPs are estimated to be 1.53nm and 1.6nm,

respectively based on the C_{ox} of ideal C-V curves. To achieve a more scaled gate stack, an oxygen scavenging technique utilising an ALD deposited TiN layer as part of the gate stack is incorporated to minimize the interfacial layer to reduce the equivalent oxide thickness below 1 nm.

7.3.1 EOT scaling with TiN capping layer insertion

As introduced in Section 5.2, in the process flow of in-situ $HfO_2/In_{0.53}Ga_{0.47}As$ (100) and (110) MOSCAPs, the metal gate is prepared by ex-situ e-beam metallisation. For manufacturability perspective of ultimate scaled MOSCAP, the process of in-situ ALD of TiN layer insertion prior e-beam metallisation is shown in Fig. 7.10.

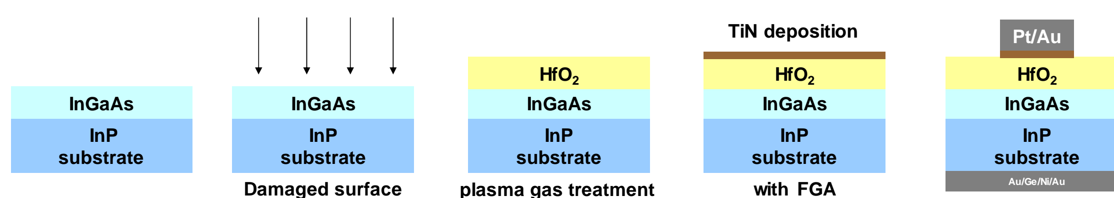


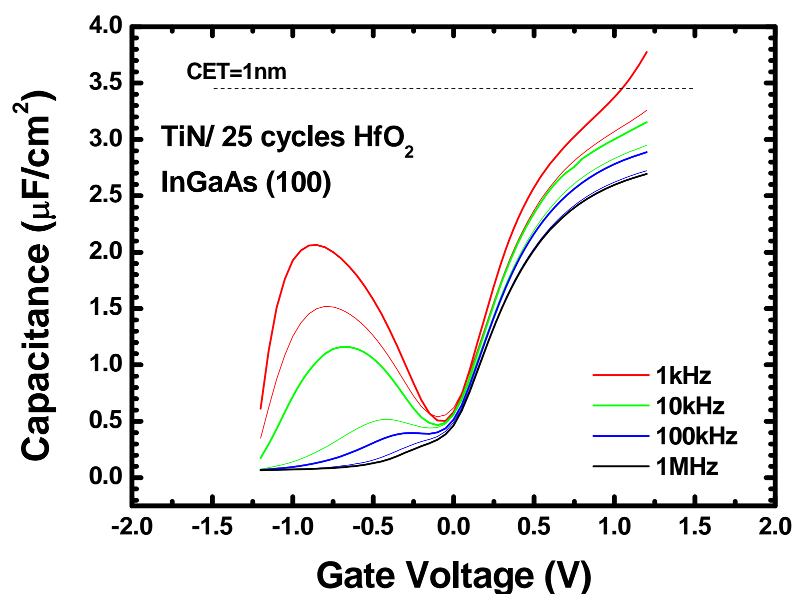
Fig. 7.10. Process flow of in-situ InGaAs gate stack formation subjected to plasma gas pre-treatment on (100) and (110) orientation of etched InGaAs surfaces via in-situ TiN capping layer insertion.

At first, the fabrication on InGaAs (100) orientation is investigated. In addition to the sample A, which had 25 cycles of HfO_2 dielectric deposition subjected to TMA/plasma H_2 pre-treatment, as introduced in section 5.2.1, samples B and C were included in the experiment. In the work reported here, ~10nm TiN is deposited at 350ºC by ALD immediately following HfO_2 deposition on sample B and C before ex-situ e-beam metallisation of Pt/Au contact, then followed by FGA in (H2:N2 = 5%:95%) at 350ºC for 5mins. Sample B and C respectively has 25 and 20 cycles of HfO_2 prior to TiN deposition. Table 7.5 lists all the experimental details of scaled $In_{0.53}Ga_{0.47}As$ (100) and (110) MOSCAPs subject to a ICP etching in a $CH_4/Cl_2/H_2$ based chemistry.

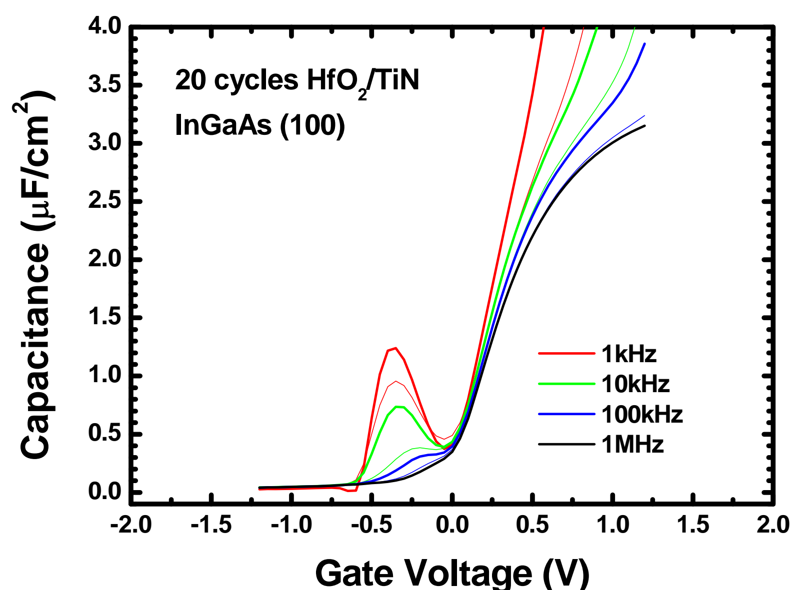
Etched $In_{0.53}Ga_{0.47}As$	(100)-oriented MOSCAP	(110)-oriented MOSCAP
25 cycles HfO_2 without TiN	Sample A	
25 cycles HfO_2 with TiN	Sample B	Sample D
20 cycles HfO_2 with TiN	Sample C	

Table. 7.5. The experimental details of scaled $In_{0.53}Ga_{0.47}As$ (100) & (110) MOSCAPs.

Fig. 7.11 shows the multi-frequency room temperature C-V characteristics of sample B in (a) and sample C in (b). Compared to the sample A, accumulation capacitance of sample B and C significantly increased by 64% and 92%, respectively. This result implies that oxygen scavenging is effective in reducing the interlayer in $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs. The positive shift of flatband voltage shown in Fig. 7.12 further supports the argument. The high frequency dispersion is observed in sample C results from high leakage current.



(a)



(b)

Fig. 7.11. C-V characteristics of (a) 25 cycles and (b) 20 cycles of HfO_2 dielectric deposition subjected to TMA/plasma H_2 pre-treatment with ~10nm TiN capping layer insertion.

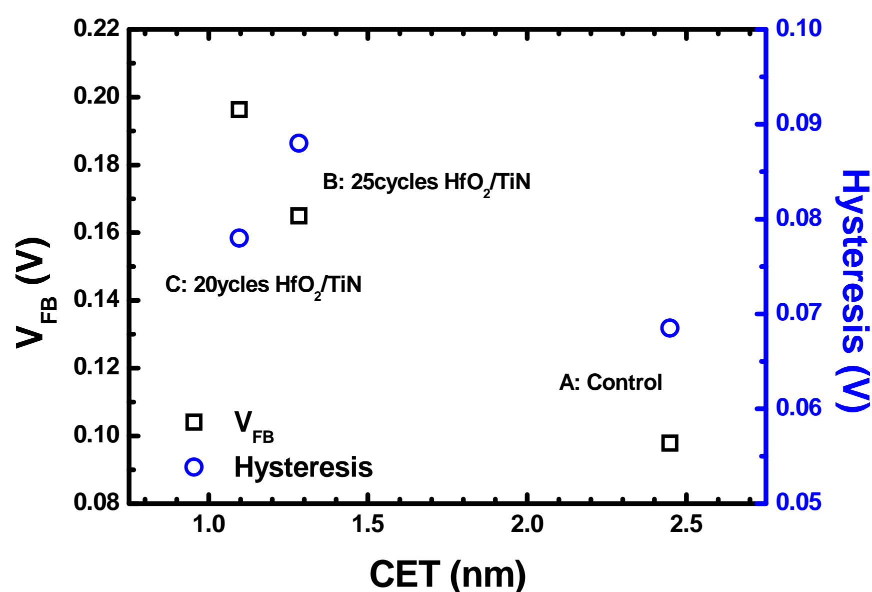


Fig. 7.12. Metrics of hysteresis and flatband voltage verse CET.

The result of the additional TiN capping layer in the gate stack of an etched $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs with 25 cycles of HfO_2 dielectric deposition subjected to TMA/plasma H_2 pre-treatment is shown in Fig 7.13. Accumulation capacitor also increased by 80%, compared to the control sample.

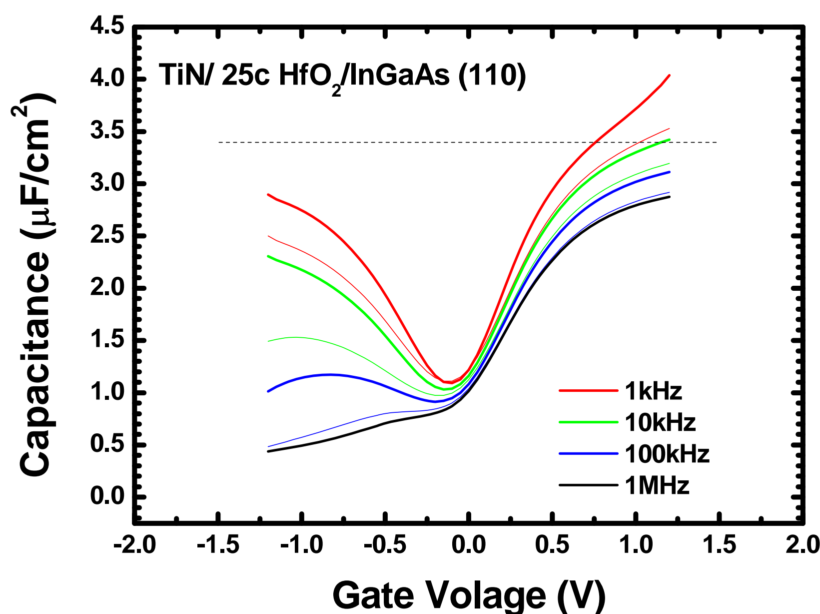


Fig. 7.13. C-V characteristics of TiN capping layer inserted $In_{0.53}Ga_{0.47}As$ (110) MOSCAPs with 25 cycles of HfO_2 dielectric deposition subjected to TMA/plasma H_2 pre-treatment.

7.3.2 Analysis of EOT scalability on $In_{0.53}Ga_{0.47}As$ (100) and (110) MOSCAPs

In Fig. 7.14, the gate leakage current obtained at the voltage of V_{FB}+1V is plotted as the function of CET, which is extracted from accumulation capacitance of 1MHz C-V characteristics at room temperature. The insert of diagram shows the gate leakage of all samples, refer to Table 7.4. For comparison, the dotted line in Fig. 7.15 is for the HfO_2/Si system; the data of Suzuki et al is also included [7.12].

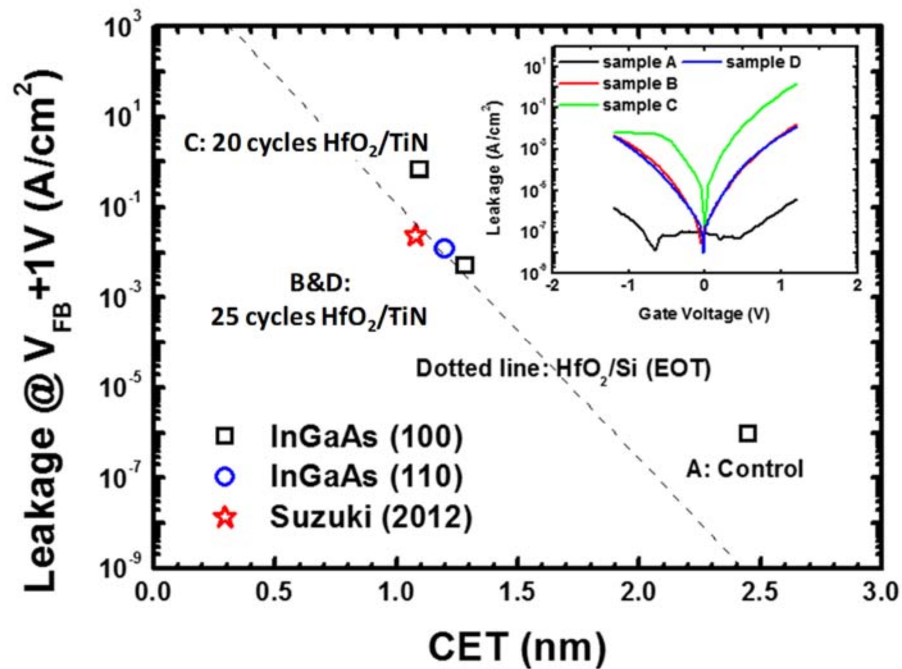


Fig.7.14. CET vs. leakage current.

Based on the result in Fig. 7.14, CET scaling of low D_{it} HfO_2/InGaAs (100) gate stack to 1.09 nm has been demonstrated by the insertion of a TiN layer. In addition, the scaled InGaAs (110) gate stack from the CET of ~2.2nm to 1.2nm is realised with this technique. According to the Section 4.2, this work enables the path to realize superior Tunnel-FETs for low power application.

7.4 Chapter summary

This chapter has discussed the use of a clustered ICP etch and ALD tool to assess the impact of in-situ plasma processing on (100) and (110) oriented $In_{0.53}Ga_{0.47}As$ MOSCAPs which have been subjected to a $Cl_2/CH_4/H_2$ based ICP etch chemistry. In addition, a comparison is made of the use of in-situ cyclic plasma N_2/TMA and plasma H_2/TMA processes after ICP etching and prior to ALD deposition of HfO_2. Based on

the qualitative analysis from C-V characteristics and metrics of stretch-out, the sample that is subject to plasma H_2/TMA pre-treatment performs better than plasma N_2/TMA pre-treatment by 17% for $In_{0.53}Ga_{0.47}As$ (100) orientation and by 48% for $In_{0.53}Ga_{0.47}As$ (110) orientation. Furthermore, quantitative analysis of (110) oriented InGaAs MOSCAPs with and without H_2/TMA has be conducted using the conductance method. After plasma H_2/TMA pre-treatment, the interface defect density is improved around the conduction band edge from $6\,x\,10^{11}\,cm^{-2}eV^{-1}$ to$2.8\,x\,10^{11}\,cm^{-2}eV^{-1}$, which implies plasma H_2/TMA pre-treatment can reduce the etching damage after nanowire formation. One of the main reason for 25 cycles of HfO_2 being not capable of scaling CET below 2nm results from an intermixing layer (AsOx interfacial layer) between HfO_2 and $In_{0.53}Ga_{0.47}As$ as shown by EELS and XPS analysis. To reduce CET to around 1nm, the insertion of a TiN layer between Pt and HfO_2 has been explored. Based on the electrical result of 20 cycles of HfO_2 for $In_{0.53}Ga_{0.47}As$ (100) orientation, the best CET in this work is around 1.09nm. In addition, for both $In_{0.53}Ga_{0.47}As$ (100) and (110) orientation, the scaled gate stack can be achieved around 1.2nm for 25 cycles of HfO_2 with leakage current comparable to HfO_2/Si system. In conclusion, CET scaling of the low D_{it} $HfO_2/In_{0.53}Ga_{0.47}As$ gate stack has been accomplished on (100) and (110) oriented $In_{0.53}Ga_{0.47}As$.

7.5 Reference

[7.1] A. Alian, Y. Mols, C. C. M. Bordallo, D. Verreck, A. Verhulst, A. Vandooren, R. Rooyackers, P. G. D. Agopian, J. A. Martino, A. Thean, D. Lin, D. Mocuta, and N. Collaert, "InGaAs tunnel FET with sub-nanometer EOT and sub-60 mV/dec sub-threshold swing at room temperature," *Appl. Phys. Lett*., vol. 109, no. 24, p. 243502, Dec 2016.

[7.2] V. Chobpattana et al., "Nitrogen-passivated dielectric/InGaAs interfaces with sub-nm equivalent oxide thickness and low interface trap densities," *Appl. Phys. Lett*., vol. 102, p. 022907, Jan. 2013.

[7.3] Y.-C Fu et al., "The impact of forming gas annealing on the electrical characteristics of sulfur passivated Al2O3/$In_{0.53}Ga_{0.47}As$ (110) metal-oxide-semiconductor capacitors," *Appl. Phys. Lett*. 110, 142905, 2017.

[7.4] J.-Y. Yun, S.-W. Rhee, S. Park, and J.-G. Lee, "Remote plasma enhanced metalorganic chemical vapor deposition of TiN from tetrakis-dimethyl-amido-titanium," *J. Vac. Sci. Technol*. A, 18, 2822, 2000.

[7.5] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* Wiley, New York, 1982.

[7.6] E. H. Nicollian and A. Goetzberger, “The Si-SiO_2 interface-electrical Properties as Determined by the Metal-Insulator-Silicon Conductance Technique,” *Bell System Technical Journal*, vol.46, no. 6, pp. 1055-1133, 1967.

[7.7] W. Shockley and W. T. Read,” Statistics of the Recombinations of Holes and Electrons” *Phys. Rev*. 87, 835, 1952.

[7.8] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, “Band parameters for III–V compound semiconductors and their alloys,” *J. Appl. Phy*s. 89, 5815, 2001.

[7.9] K. Boucart and A. M. Ionescu, “Double-gate tunnel FET with high-k gate dielectric,” *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725–1733, Jul. 2007.

[7.10] A. M. Ionescu and H. Riel, “Tunnel field-effect transistors as energy efficient electronic switches,” *Nature*, vol. 479, no. 7373, pp. 329–337, Nov. 2011.

[7.11] U. E. Avci et al., “Understanding the feasibility of scaled III-V TFET for logic by bridging atomistic simulations and experimental results,” in *Proc. VLSIT’12*, Honolulu, HI, USA, pp. 183–184.

[7.12] R. Suzuki, N. Taoka, M. Yokoyama, S. Lee, S. H. Kim, T. Hoshii, T. Yasuda, W. Jevasuwan, T. Maeda, O. Ichikawa, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, “1-nm-capacitance-equivalent-thickness HfO_2/Al_2O_3/InGaAs metal-oxide-semiconductor structure with low interface trap density and low gate leakage current density,” *Applied Physics Letters*, vol. 100, no. 13, p. 132906, 2012.

VIII. Heterojunction Tunnel-FET

As described in the previous chapter, the use of clustered plasma etch and ALD tools enables the realisation of a scaled, low interface state density gate stack. Based on the electrical result shown in Chapter VII, the surface damage mitigation on InGaAs (110) orientation, which dominates the channel of non-planar devices, has been realised by incorporating a plasma H_2 pre-treatment. In this chapter, devices based on the $In_xGa_{1-x}As$ p-n, p-i-n heterostructures configurations shown in the Fig. 8.1, are investigated using the processes described in previous chapters. The chapter starts with a comparison of p-n and p-i-n Tunnel-FET that have been fabricated using 25 cycles of ALD HfO_2 with plasma H_2 pre-treatments. This is followed by a discussion on the effect of gate oxide scaling of p-i-n Tunnel-FETs. Furthermore, the effectiveness of incorporating a doped n-pocket via a p-n-i-n Tunnel-FET structure is evaluated including orientation effect on both types of Tunnel-FET. The chapter concludes with a benchmarking of the devices against the current state of the art.

8.1 Performance of p-n and p-i-n Tunnel-FETs

Fig. 8.1 illustrates the layer structure of the $In_xGa_{1-x}As$ p-n and p-i-n Tunnel-FET wafers. Apart from the difference of doping configuration, the wafer in Fig. 8.1 (b) utilizes InAs as a channel material instead of InGaAs with 70% In-content channel in the wafer of Fig. 8.1 (a).

25cycle HfO_2
p-$In_{0.53}Ga_{0.47}As$ (2×10^{19} cm^{-3}) 50nm
p-$In_{0.7}Ga_{0.3}As$ (2×10^{19} cm^{-3}) 6nm
n-$In_{0.7}Ga_{0.3}As$ (2×10^{18} cm^{-3}) 6nm
n-$In_{0.53}Ga_{0.47}As$ (4×10^{17} cm^{-3}) 100nm
n-$In_{0.53}Ga_{0.47}As$ (2×10^{18} cm^{-3}) 200nm
S.I. InP substrate

(a) p-n

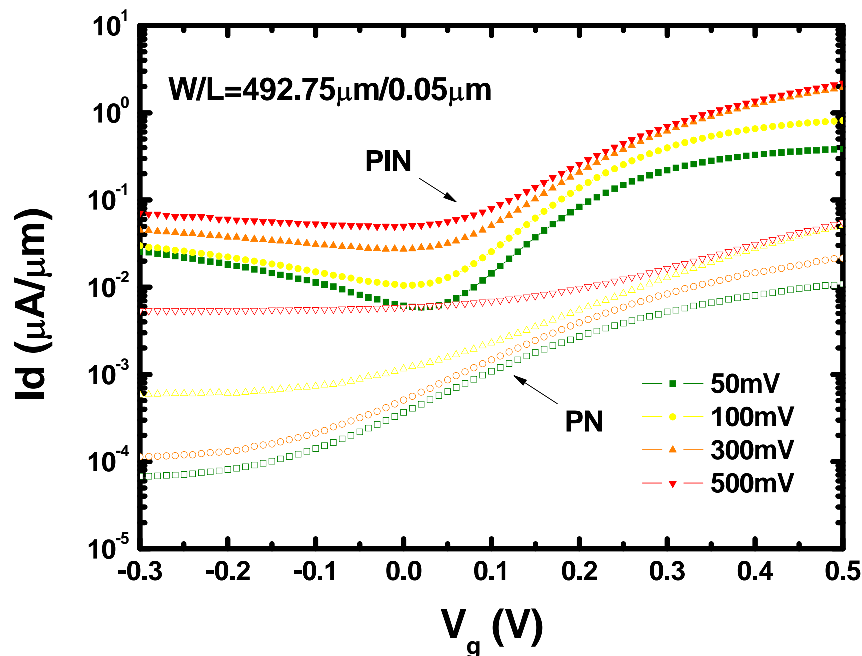
25cycle HfO_2
p-$In_{0.53}Ga_{0.47}As$ (2×10^{19} cm^{-3}) 50nm
p-$In_{0.7}Ga_{0.3}As$ (2×10^{19} cm^{-3}) 20nm
InAs UID 6nm
$In_{0.7}Ga_{0.3}As$ UID 6nm
$In_{0.53}Ga_{0.47}As$ UID 50nm
n-$In_{0.53}Ga_{0.47}As$ (2×10^{18} cm^{-3}) 150nm
S.I. InP substrate

(b) p-i-n

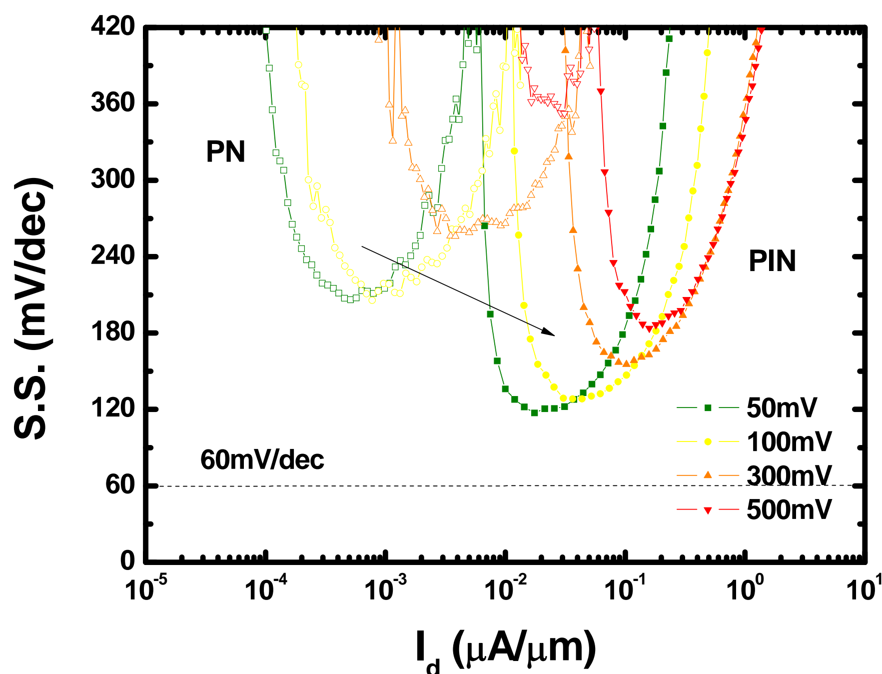
Fig. 8.1. Layer structure of $In_xGa_{1-x}As$ (a) p-n and (b) p-i-n Tunnel-FETs.

DC electrical characteristics of double gate channel transistor of p-n and p-i-n Tunnel-FETs are illustrated in Fig. 8.2.

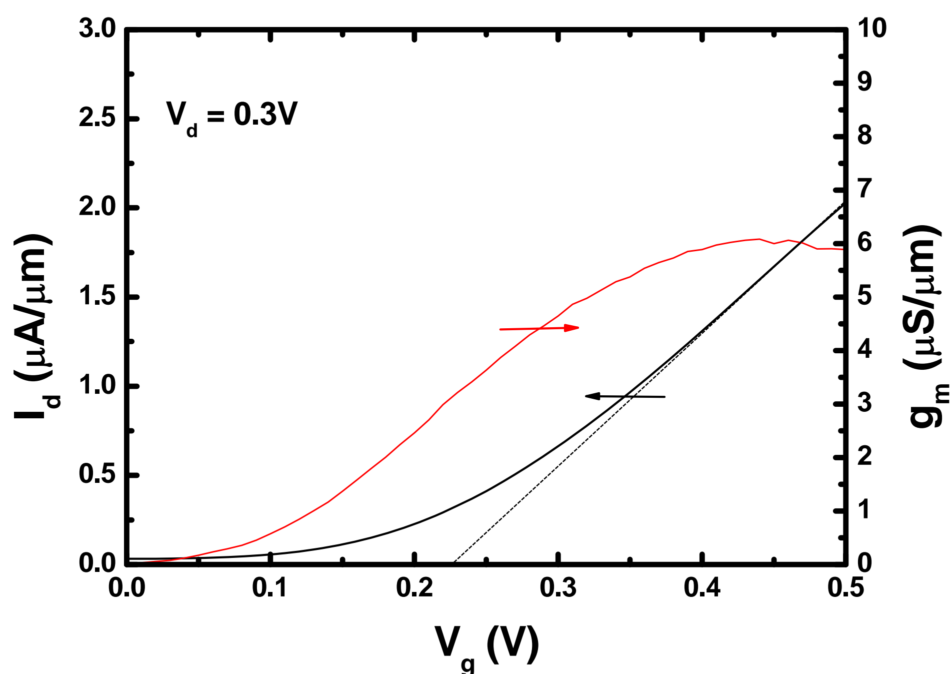
Fig. 8.2 (a) shows the transfer characteristics of both devices. Comparing to p-n Tunnel-FET, p-i-n Tunnel-FET have better subthreshold swing, although the p-n Tunnel-FET have signature off-current under the drain bias of 50mV. The subthreshold swing as a function of drain current at drain bias of 50mV, 100mV, 300mV and 500mV for both devices is shown in Fig. 8.2 (b). This indicates that minimum SS and the drain current at minimum SS of p-i-n Tunnel-FET is superior to p-n Tunnel-FET. A minimum subthreshold swing of 120mV/dec was obtained at V_d = 50mV with drain current of 0.02uA/um for the p-i-n device structure. A peak transconductance, around 6.1 uS/um at drain bias of 300mV, for p-i-n Tunnel-FET is shown in Fig. 8.2 (c). In addition, the threshold voltage of ~0.23V is extracted by extrapolation method in linear region. Based on the threshold voltage, the metrics of on-off ratio, which is defined as the ratio between the drain current at the gate bias of V_{th} + 2/3 V_d considered as on state voltage and V_{th} – 1/3 V_d as off-state at the specific drain bias [8.1], can be obtained. The on-off ratio of p-i-n Tunnel-FET is around 20 at drain bias of 300mV.



(a)



(b)



(c)

Fig. 8.2. Measured (a) transfer characteristics, (b) subthreshold swing as a function of drain current of p-n and p-i-n Tunnel-FET and (c) transconductance characteristics of p-i-n Tunnel-FET. The device figures of merit are as follows: SS_{min} = 120mV/dec at drain bias of 50mV for p-i-n Tunnel-FET. The threshold voltage of 0.23V is extracted by linear extrapolation of the transfer characteristics at the drain bias of 300mV. On-off ratio: 1 order at the drain bias of 300mV (I_{off} at $V_{th} – 1/3\ V_d$ and I_{on} at $V_{th} + 2/3\ V_d$ [8.1])

The output characteristics of p-n and p-i-n devices are shown in Fig. 8.3 (a) and (b). The characteristic feature of a Tunnel-FET is the appearance of negative differential resistance (NDR). As Fig. 8.3 shows, the NDR characteristics of p-i-n Tunnel-FET is stronger than p-n Tunnel-FET. In addition, similar trend to transfer characteristics is observed that the drain current of p-i-n Tunnel-FET is larger than p-n Tunnel-FET under the same condition of gate bias. The maximum of drain current for p-i-n Tunnel-FET is around 5μA/μm obtained at the drain bias of 500mV and the gate bias of 900mV shown in Fig. 8.3 (b) According to the plot at gate bias of 900mV and drain bias of 500mV, the on resistance (R_{on}) of p-n and p-i-n Tunnel-FET are 2100k and 90kΩ/μm, respectively.

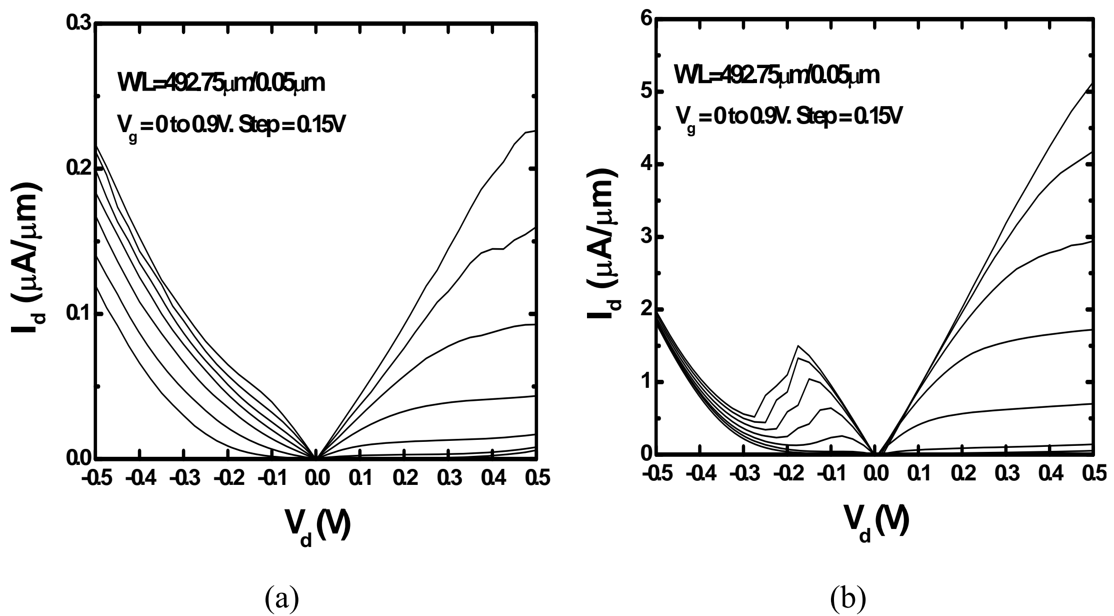


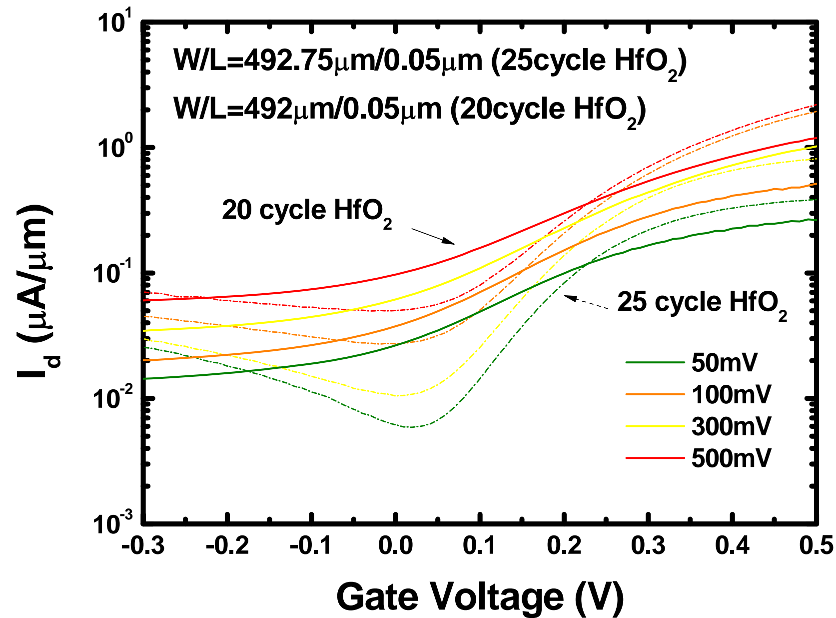
Fig. 8.3. Output characteristics of (a) p-n Tunnel-FET and (b) p-i-n Tunnel-FET with R_{on} value of 2100 and 90kΩ/μm, The $I_{d,max}$ for p-i-n Tunnel-FET is around 5μA/μm obtained at the drain bias of 500mV and the gate bias of 900mV.

8.2 Optimisation of heterojunction Tunnel-FETs

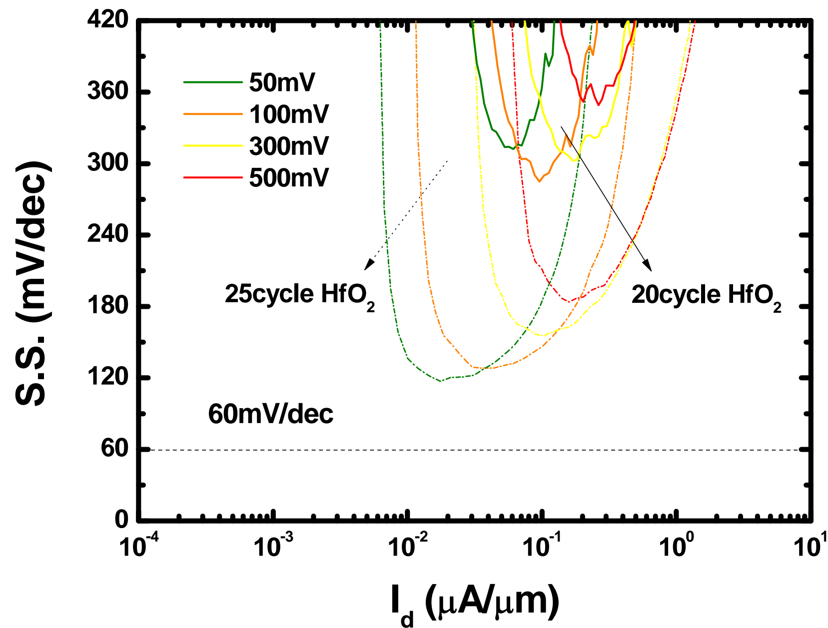
To optimise the p-i-n Tunnel-FET, there are three aspects being considered in this work including scaling gate dielectric layer, designing new layer structure of heterostructure Tunnel-FET and utilizing the double gate configuration to increase electrostatic control of Tunnel-FET.

As discussed in Chapter VII, CET of gate stack around 1nm on 20 cycles of $HfO_2/In_{0.53}Ga_{0.47}As$ gate stack has been demonstrated. Fig. 8.4 (a) shows the transfer characteristics of p-i-n Tunnel-FET with 25 (solid lines) and 20 (dotted lines) cycles gate stacks, respectively. It is obvious that there is no significant benefit on the SS of device

after scaling gate stacks from 25 cycles to 20 cycles of HfO_2 dielectric layer. The minimum SS based on the plot of subthreshold swing as a function of drain current in Fig. 8.4 (b) is obtained by ~285mV/dec (V_d=100mV). This mainly results from the increasing the floor of off leakage current.



(a)



(b)

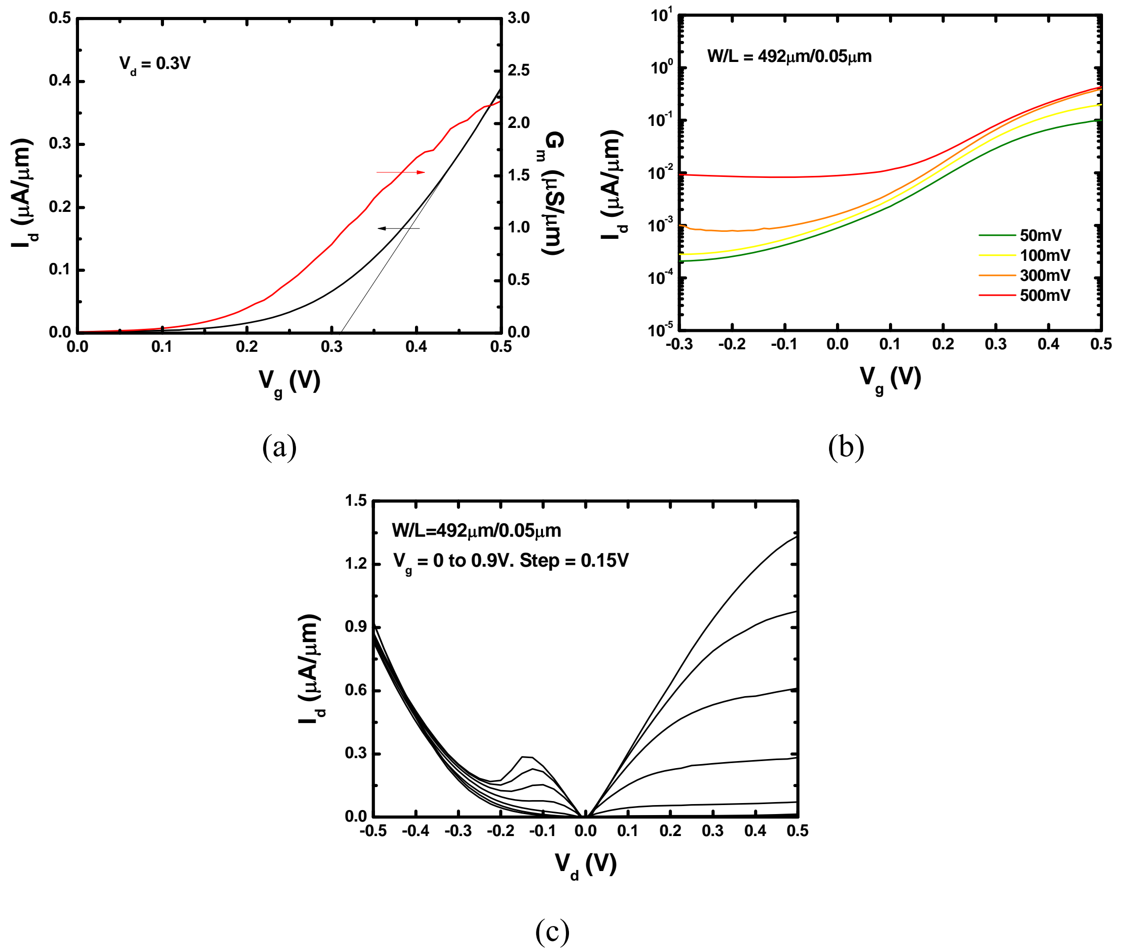
Fig. 8.4. (a) transfer characteristics and (b) the SS as a function of drain current for p-i-n Tunnel-FETs with 20 and 25 cycles of $HfO_2/In_{0.53}Ga_{0.47}As$ gate stack, respectively.

Furthermore, as introduced in Chapter IV, adding a n-pocket layer between p-doped and intrinsic layer can effectively increase on-current. Therefore, a further layer structure with a p-n-i-n heterojunction for the optimisation of p-i-n Tunnel-FET shown in Fig, 8.5, was grown, The p-n-i-n structure is different from p-i-n in that the both intrinsic layer of InAs and $In_{0.7}Ga_{0.3}As$ are heavily doped by n dopant.

25cycle HfO_2
p-$In_{0.53}Ga_{0.47}As$ (2 x 10^{19} cm^{-3}) 50nm
p-$In_{0.7}Ga_{0.3}As$ (2 x 10^{19} cm^{-3}) 20nm
n-InAs (5 x 10^{18} cm^{-3}) 6nm
n-$In_{0.7}Ga_{0.3}As$ (5 x 10^{18} cm^{-3}) 6nm
$In_{0.53}Ga_{0.47}As$ UID 50nm
n-$In_{0.53}Ga_{0.47}As$ (2 x 10^{18} cm^{-3}) 150nm
S.I. InP substrate

Fig. 8.5. Layer structure of p-n-i-n heterojunction.

The electrical characterisation of transconductance, transfer characteristics and output characteristics for p-n-i-n Tunnel-FET with 20 cycles of $HfO_2/In_{0.53}Ga_{0.47}As$ gate stack is shown in Fig. 8.6 (a), (b) and (c), respectively. From Fig. 8.6 (a), the threshold voltage of p-n-i-n at the condition of V_{ds} = 300mV is 310mV. Comparing to the p-i-n Tunnel-FET with the same condition of gate stack shown in Fig. 8.4 (a), the off-current defined as the current with the bias of V_{th} – 1/3 V_d drops from 4x10^{-1} $\mu A/\mu m$, as shown in Fig. 8.4 (a), to 2x10^{-1} $\mu A/\mu m$ as shown in Fig. 8.5 (b). In addition, the on-current for p-n-i-n Tunnel-FETs, which is given at the bias of V_{th} + 2/3 $V_{d,}$ also increases 1.4 times. Therefore, total the I_{on}/I_{off} of p-i-n and p-n-i-n Tunnel-FETs is 8.8 and 25, respectively, which means the switch for p-n-i-n Tunnel-FET is more efficient than p-i-n Tunnel-FET. However, the transconductance of p-n-i-n Tunnel-FET decreases to 2.1 $\mu S/\mu m$.



(a) (b)

(c)

Fig. 8.6. Plot of (a) transfer and transconductance characteristics at condition of V_{ds} = 300mV, (b) transfer characteristics at condition of V_{ds} = 50mV, 100mV, 300mV and 500mV and (c) output characteristics of p-n-i-n Tunnel-FET.

In 8.6 (c), the output characteristics of p-n-i-n Tunnel-FET which is similar to p-i-n Tunnel-FET also shows the NDR characteristics at the forward bias region. The SS as a function of drain current is represented in Fig. 8.7 for the comparison of p-i-n and p-n-i-n Tunnel-FETs based on the diagram of Fig, 8.6 (b). The minimum SS is obtained by 152mV/dec at the drain current of $1.8\text{x}10^{-2}$ $\mu A/\mu m$. Therefore, based on the observation of electrical characteristics in this work, that n-doped pocket significantly improves SS by 46% but transconducance at the condition of V_{ds} = 300mV decreases 31%.

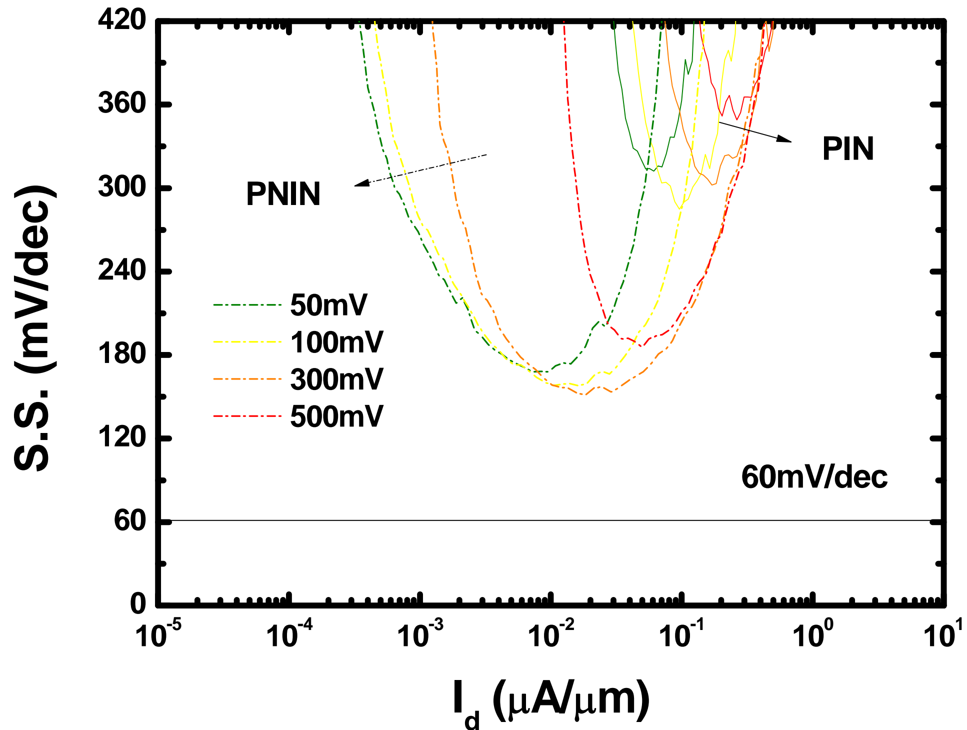
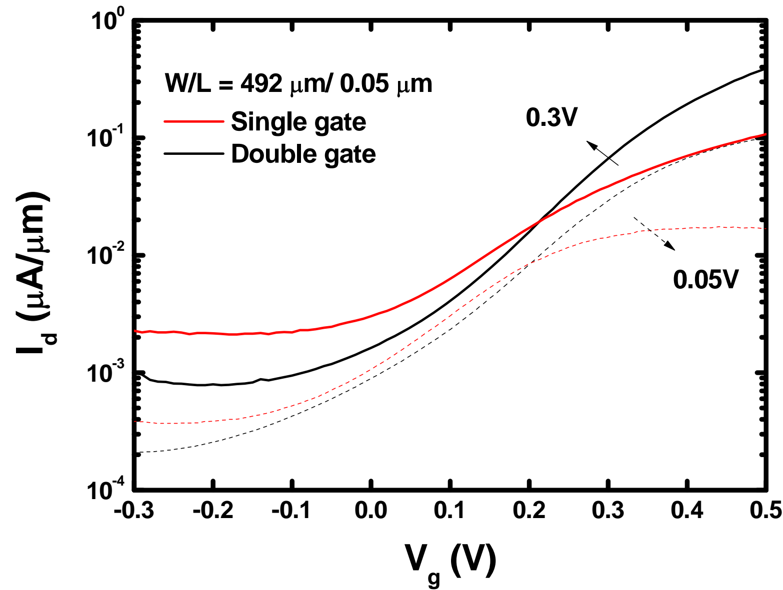
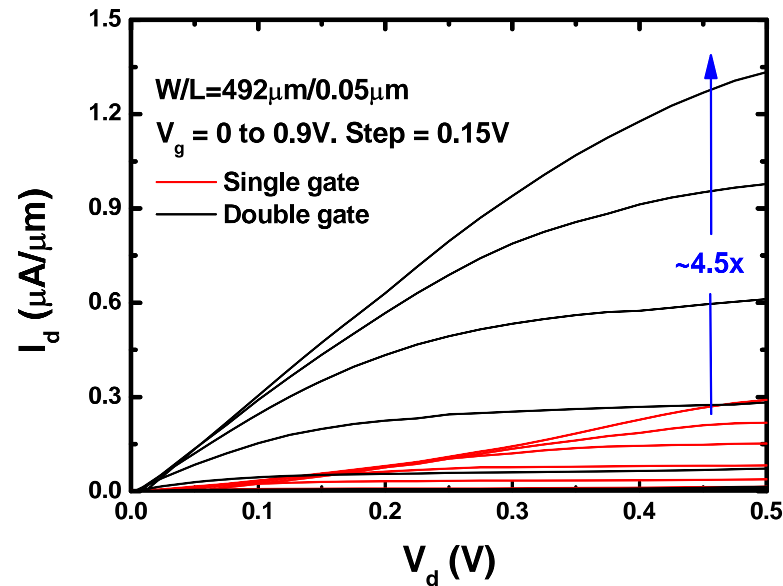


Fig. 8.7. Plot of SS as a function of drain current for the comparison of p-i-n and p-n-i-n Tunnel-FETs.

As discussed in section 8.1 and 8.2, all the configurations of p-n, p-i-n and p-n-i-n Tunnel-FET are double gate transistors, introduced in Section 5.3.1.2. To further understand the effectiveness of improving device characteristics with double gate configurations, single gate devices were also fabricated and examined. Fig. 8.8 (a) and (b) show the transfer characteristics and output characteristics for the comparison of single gate and double gate p-n-i-n Tunnel-FETs. The transfer characteristics in Fig. 8.8 (a) clearly indicates the SS of double gate device can provide superior performance of SS for both conditions of V_{ds} = 50mV and 300mV. In addition, the drain current of output characteristics shown in Fig. 8.8 (b) shows the drain current for double p-n-i-n Tunnel-FET at the condition of V_{gs} = 900mV and V_{ds} = 500mV is 4.5 times larger than single gate p-n-i-n Tunnel-FET. Therefore, it implies that double gate configuration can effectively switch device and offer larger drive current.



(a)



(b)

Fig. 8.8. (a) transfer characteristics and (b) output characteristics of single gate and double gate p-n-i-n Tunnel-FETs.

According to these three aspects of optimising Tunnel-FETs in this work, there is a significant improvement in SS and on-current as a result of scaling the equivalent oxide thickness of the gate stack. Utilizing the p-n-i-n configuration enables the enhancement of SS but sacrifices the on current and transconductance. It seems that the function of n-pocket would be reduce the leakage floor of devices but the device still requires an intrinsic InAs as the channel of Tunnel-FETs. Double gate structure can provide the improvement of SS and on current at the same time. All these three aspects above provide

useful insight toward the realisation of a high performance and low power Tunnel-FET. The p-n-i-n Tunnel-FET with nanowire structure is considered as one of the most promising candidate for low power device applications. Fig. 8.9 shows the benchmark of I_{on} as a function of I_{off} among the published vertical nanowire Tunnel-FETs based on III-V materials [8.2-9]. The non-planar p-i-n and p-n-i-n Tunnel-FETs in this work are also included in Fig. 8.9. Compared to other works, the devices of this work demonstrates compatible values of on current. Also, the p-n-i-n structure shows potential on reduced for reducing off current.

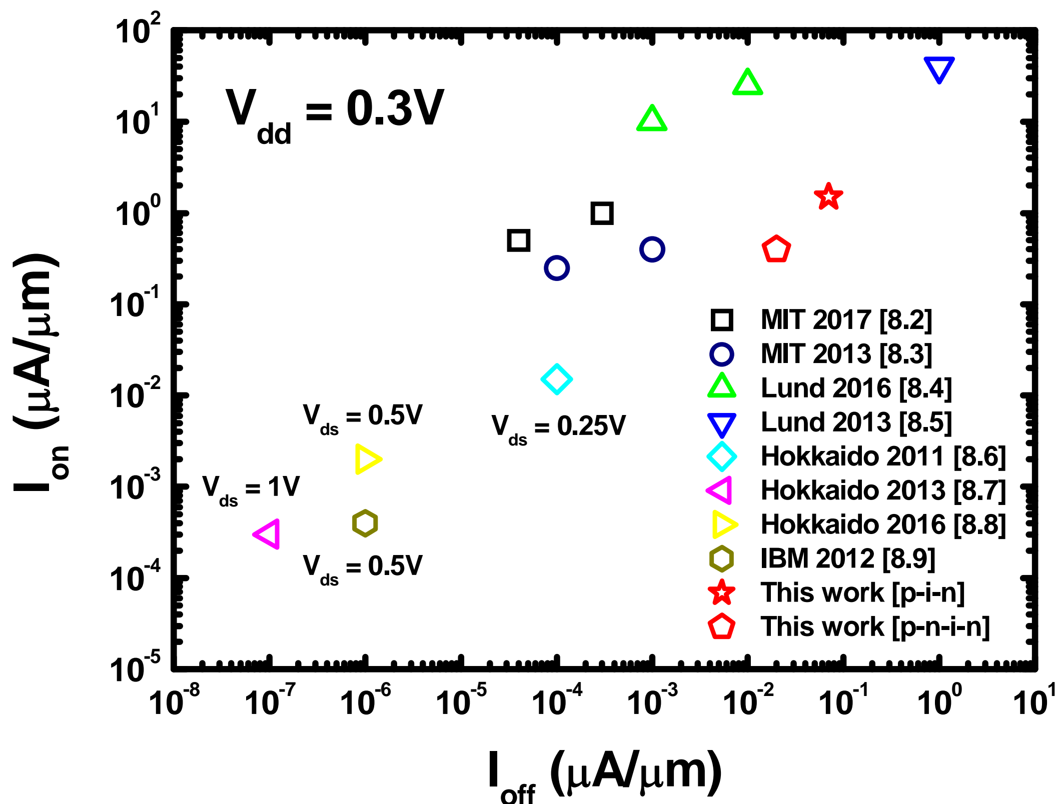


Fig. 8.9. I_{on} vs. I_{off} at V_{DD} = 0.3V among the published vertical nanowire Tunnel-FETs based on III-V materials [8.2-9]. Some points are with other V_{DS} values due to data availability.

Fig. 8.10 show the output characteristics of the p-n-i-n vertical nanowire Tunnel-FET in this work. Although the device was unable to perform the switch off characteristics due to fabrication process deviation, it demonstrated high on current, which can potentially be a high efficiency Tunnel-FET.

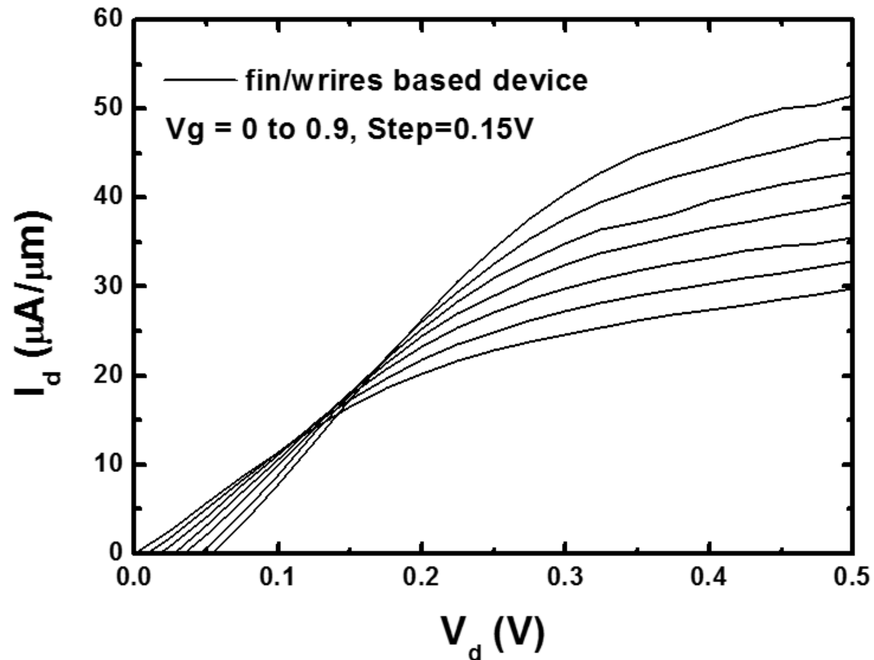


Fig. 8.10. Output characteristics of fin/wires based p-n-i-n Tunnel-FET.

8.3 Chapter summary

According to the aforementioned well-developed $In_{0.53}Ga_{0.47}As$ MOSCAPs with low D_{it} and CET, planar and non-planar Tunnel-FETs have been realised on p-n, p-i-n and p-n-i-n layer III-V heterostructures. Tunnel-FET operation has been confirmed by the observation of negative differential resistance in the experimental current/voltage characteristics. Comparing with p-n Tunnel-FET, the p-i-n Tunnel-FET provides better electrical characteristics in terms of SS with a minimum value of 120 mV/dec at the bias condition of V_{DS} = 0.05V. The transconducance peak of p-i-n Tunnel-FET at the condition of V_{DS} = 0.3V is around 6 $\mu S/\mu m$. Although the p-n-i-n Tunnel-FET demonstrates comparable on-current to the p-i-n Tunnel-FET by 1.1 $\mu A/\mu m$ at the bias condition of V_{DS} = 0.3V, the subthreshold swing improves in 46% due to the lower leakage floor by the n-pocket layer. Importantly, the non-planar Tunnel-FET configuration with a double gate structure can both improve SS from 228mV/dec to 152mV/dec the condition of V_{DS} = 500mV and on-current to 1.3 $\mu A/\mu m$ at the condition of V_{DS} = 500mV and V_{GS} = 900mV. Benchmarking of I_{on} and I_{off} for this work and recently published results based on III-V materials indicate the devices of this project are comparable of the state-of-the-art in terms of on and off current. Overall, the devices demonstrated provided important insight into routes for further optimisation in future.

8.4 Reference

[8.1] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, and M. Radosavljevic, “Benchmarking nanotechnology for high-performance and low-power logic transistor applications,” *IEEE Trans. Nanotechnol.*, vol. 4, no. 2, pp. 153–158, Mar. 2005.

[8.2] X. Zhao, A. Vardi, and J. A. Del Alamo, “ Sub-thermal Subthreshold Characteristics in Top-down InGaAs/InAs Heterojunction Vertical Nanowire Tunnel FETs,” *IEEE Electron Device Letters.* VOL. 38, NO. 7, pp. 858-865, 2017.

[8.3] X. Zhao, A. Vardi, and J. A. Del Alamo, “InGaAs/InAs heterojunction vertical nanowire tunnel FETs fabricated by a top-down approach,” in *IEDM Tech. Dig.*, Dec. 2014, pp. 590–593.

[8.4] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, “Vertical InAs/GaAsSb/GaSb tunneling fieldeffect transistor on Si with S=48 mV/decade and Ion=10 μA/μm for Ioff =1 nA/μm at Vds=0.3 V,” in *IEDM Tech. Dig.*, Dec. 2016, pp. 500–503.

[8.5] A. W. Dey, B. M. Borg, B. Ganjipour, M. Ek, K. A. Dick, E. Lind, C. Thelander, and L.-E. Wernersson, “High-current GaSb/InAs(Sb) nanowire tunnel field-effect transistors,” *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 211–213, Feb. 2013.

[8.6] K. Tomioka and T. Fukui, “Tunnel field-effect transistor using InAs nanowire/Si heterojunction,” *Appl. Phys. Lett.*, vol. 98, no. 8, p. 083114, Feb. 2011.

[8.7] K. Tomioka, M. Yoshimura, E. Nakai, F. Ishizaka, and T. Fukui, “Integration of III–V nanowires on Si: From high-performance vertical FET to steep-slope switch,” in *IEDM Tech. Dig.,* Dec. 2013, pp. 88–91.

[8.8] K. Tomioka and T. Fukui, “Recent progress in integration of III–V nanowire transistors on Si substrate by selective-area growth,” *J. Phys. D, Appl. Phys.*, vol. 47, no. 39, p. 394001, Sep. 2014.

[8.9] K. E. Moselund, H. Schmid, C. Bessire, M. T. Bjork, H. Ghoneim, and H. Riel, “InAs–Si nanowire heterojunction tunnel FETs,” *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1453–1456, Oct. 2012.

IX. Conclusion and Future work

In this thesis, the role of a high quality scaled gate stack and appropriate heterostructures have been explored to realise low supply voltage Tunnel-FET devices. The motivation to realise a high device current and low subthreshold swing transistor is initially brought to light through the inspection of the theory of operation of such a Tunneling-based three terminal transistors to overcome the limitation of a basic MOSFET operation in theory on subthreshold swing. Then, the necessary parameters to optimise this kind of device is highlighted to ensure the maximum performance such as low interface defect density of III-V MOSCAPs on a variety of orientations, ultimate EOT scaling of III-V gate stacks and the suitable layer structure for heterojunction.

In this thesis, the main findings and accomplishments towards the objective is summarised below,

- The impact of FGA on the electrical characteristics of sulphur passivated p-and n-type $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110)-oriented MOSCAPs has been investigated. A midgap D_{it} value in the range of 0.87 – 1.8 x 10^{12} $cm^{-2}eV^{-1}$ is observed form the samples after FGA and a D_{it} value of 3.1 x 10^{11} $cm^{-2}eV^{-1}$ is obtained close to the conduction band edge. These data indicate the combination of sulphur pre-treatment and FGA enables effectively passivating trap state in the upper half of the bandgap of (110)-oriented $In_{0.53}Ga_{0.47}As$. Meanwhile, the further result in reduction of border trap density on n-type $In_{0.53}Ga_{0.47}As$ (110)-oriented MOSCAP after FGA from 1.8 x 10^{12} cm^{-2} to 5.3 x 10^{11} cm^{-2} is observed.
- Cluster tool based ICP etching of (100) and (110) oriented $In_{0.53}Ga_{0.47}As$ MOSCAPs followed by in-situ ALD of HfO_2 including nitrogen and hydrogen plasma passivation is demonstrated in this work as a route to the realisation of a gate stack on the sidewall excluding any impact of native oxide for non-planar III-V Tunnel-FETs. Based on the C-V characteristics, TMA/H_2 gas pre-treatments significantly improve $In_{0.53}Ga_{0.47}As$ (110)-oriented MOSCAP, which have been subjected to a nanowire etch chemistry. The assumption of more As-O bonds at the interface between HfO_2 and (110)-oriented $In_{0.53}Ga_{0.47}As$ was observed by XPS analysis. Using the conductance method, the D_{it} value of in-situ $In_{0.53}Ga_{0.47}As$ (110)-oriented MOSCAP after plasma H_2 pre-treatment is improved from 6 x 10^{11} $cm^{-2}eV^{-1}$ to 2.8 x 10^{11} $cm^{-2}eV^{-1}$ around the conduction

band edge, which is comparable to the result of the combination of sulphur pre-treatment and FGA. This shows a viable route to an “all plasma” based route for etch damage mitigation has been found for InGaAs.

- Lack of EOT scalability was observed when using 25cycles of HfO_2 as a gate dielectric on InGaAs. XPS data suggests this is due to the formation of an As-O interfacial layer. Therefore, an oxygen scavenge technique [9.1] on both $In_{0.53}Ga_{0.47}As$ (100) and (110) orientation has been demonstrated in this work via inserting a TiN capping layer between Pt and HfO_2 to unable scaling of the EOT of these $HfO_2/In_{0.53}Ga_{0.47}As$ gate stacks. The CET is effectively reduced on both $In_{0.53}Ga_{0.47}As$ (100) and (110)-oriented MOSCAPs at the same condition of 25 cycles of HfO_2 dielectric layer with Pt as a gate metal. In addition, CET scaling of the $In_{0.53}Ga_{0.47}As$ gate stack to 1.09nm on (100) orientation has been achieved.
- According to the aforementioned well-developed $In_{0.53}Ga_{0.47}As$ MOSCAPs with low D_{it} and CET, planar and non-planar Tunnel-FETs have been demonstrated. Based on three aspects on realising high performance Tunnel-FETs on the gate stack, layer structure and device configuration, this work firstly evaluate the device performance on p-n and p-i-n heterojunctions of InGaAs based material. Based on the output characteristics, p-i-n Tunnel-FET shows more obvious NDR characteristics than p-n Tunnel-FET at the forward bias region of Tunneling diode. Comparing with p-n Tunnel-FET, p-i-n Tunnel-FET can provide better electrical characteristics including a minimum subthreshold swing of 120 mV/dec at the bias condition of V_{DS} = 0.05V. The transconducance peak of p-i-n Tunnel-FET at the condition of V_{DS} = 0.3V is around 6 $\mu S/\mu m$. Further scaling the gate stack on Tunnel-FETs demonstrated no significant improvement in either SS or on current measured at a bias on $V_{th} + 2/3\, V_D$. Moreover, an inserted n-pocket of p-i-n Tunnel-FET as p-n-i-n Tunnel-FET was studied. Although the p-n-i-n Tunnel-FET provides only comparable on-current to the p-i-n Tunnel-FET, the subthreshold swing improves by 46% due to the lower leakage floor inhibited by n-pocket layer. Most importantly, a non-planar configuration with a double gate structure was shown to improve both SS and on-current by 152mV/dec and 1.3 $\mu A/\mu m$, respectively. Benchmarking of I_{on} and I_{off} with recently published results based on III-V materials indicate the device performance of this work comparable with state-of-the-art. This work, therefore, provides very useful insight to the optimisation of a high performance and power efficient device. These aspects and the result of benchmarking indicates that non-planar p-n-i-n Tunnel-FET

especially for pillar based nanowire structure seems a promising candidate for low power CMOS. The nanowire based p-n-i-n Tunnel-FET results in poor performance due to process issues shown in Appendix B.

Future work includes,

- For the perspective of process integration, further improving the process of nanowire device fabrication to avoid device failure especially leakages between G/D/S is required. Adding a spacer between gate and drain to reduce series resistance is also necessary. As lateral etching based on the atomic layer etching to further scale nanowire being demonstrated, it is potential to realise sub-10nm vertical nanowire Tunnel-FET for device integration.
- According to gate stack optimisation, double dielectric layer structure such as ZrO_2/HfO_2 may effectively solve the gate leakage issue while the dielectric layer of HfO_2 continues decreasing.
- Based on the layer structure, new heterojunction of p-n-i-n Tunnel-FET should be considered as the structure with the reduced thickness of the current InAs layer with adding an additional InAs n-pocket layer or the structure of GaSb/InAs with broken bandgap material for the improvement of subthreshold swing, on-current and off-current.

9.1 Reference

[9.1] S. Yoshida, D. Lin, A. Vais, A. Alian, J. Franco, S. El Kazzi, Y. Mols, Y. Miyanami, M. Nakazawa, N. Collaert, H. Watanabe, and A. Thean, "Systematic study of interfacial reactions induced by metal electrodes in high-*k*/InGaAs gate stacks," *Applied Physics Letters*, vol. 109, no. 17, p. 172101, 2016.

Appendix A:

A.1 Baseline planar InGaAs Tunnel-FET (EBL)

1. <u>Marker</u>

   Clean Substrate – 5min ultrasonic Acetone, 5min ultrasonic IPA, water rinse and N_2 blow dry.

   Metallisation – 30s 4:1 H_2O: HCl de-oxidise, H_2O rinse, Ar etch 30s, 15nm Mo/5nm Ti

   Spin Resist – 8% 2010 PMMA., 4krpm, 60s

   Bake – 137°C, 2mins

   Spin Resist – 8% 2042 PMMA., 5krpm, 60s

   Bake – 137°C, 2mins

   Exposure – VB6 e-beam lithography. Dose 475 $\mu C/cm^2$, 16nA beam, VRU13.

   Develop – 45s IPA: MIBK (2.5:1) at 23°C, 20s IPA rinse and N_2 blow dry.

   Metallise – Ti15nm/Pt30nm/Ti15nm/Pt30nm/ Ti15nm/Pt30nm.

   Lift-off – 2hrs 50°C acetone, 5mins IPA and N_2 blow dry.

2. <u>Source</u>

   Clean Substrate – 5min Acetone, 5min IPA, DI water rinse and N_2 blow dry.

   Spin Resist – 8% 2010 PMMA., 4krpm, 60s

   Bake – 137°C hotplate, 2mins

   Spin Resist – 8% 2042 PMMA., 5krpm, 60s

   Bake – 137°C hotplate, 2mins

   Exposure – VB6 e-beam lithography. Dose 475 $\mu C/cm^2$, 16nA beam, VRU13.

   Develop – 45s IPA: MIBK (2.5:1) at 23°C, 20s IPA rinse and N_2 blow dry.

   Metallise – Ti10nm/Pt30nm

   Lift-off – 2hrs 50°C acetone, 5mins IPA and N_2 blow dry.

   Dry etch – STS-ICP etching: 15 sccm/ 25sccm SF_6/C_4F_8. Platen power 2W, coil power 600W, 5mTorr, 20% over-etch time

3. <u>Sidewall MOS Channel</u>

   Deposition – ICP dep: 20nm SiN_x

   Clean Substrate – 5min Acetone, 5min IPA, DI water rinse and N_2 blow dry.

   Spin Resist – 1:3 HSQ: MIBK, 3krpm, 60s.

   Bake – 90°C hotplate, 2min

   Exposure – VB6 e-beam lithography. Dose 5000 $\mu C/cm^2$, 1nA beam, VRU2.

   Develop – 30s TMAH: H_2O (1:3) at 23°C, 60s water rinse, 15s IPA rinse and N_2 blow dry.

Dry etch – T-gate etching: 25 sccm/ 50sccm SF_6/N_2, power 20W, 15mTorr, 20% over-etch time

Dry etch – Cobra etching: 6 sccm/ 10sccm/ 15sccm $CH_4/Cl_2/H_2$, Platen power 25W, coil power 750W, 8mTorr, 20% over-etch time

Pre-treatment – ALD: 10 cycles of H_2/TMA pulse

In-situ deposition – ALD: 20 cycles of plasma HfO_2 at 300°C and 130 cycles of plasma TiN at 350°C

4. Gates

Clean Substrate – 5min Acetone, 5min IPA, DI water rinse and N_2 blow dry.

Spin Resist – 8% 2010 PMMA., 4krpm, 60s

Bake – 137°C hotplate, 2mins

Spin Resist – 8% 2042 PMMA., 5krpm, 60s

Bake – 137°C hotplate, 2mins

Exposure – VB6 e-beam lithography. Dose 475 $\mu C/cm^2$, 16nA beam, VRU13.

Develop – 45s IPA: MIBK (2.5:1) at 23°C, 20s IPA rinse and N_2 blow dry.

Metallise – Pd40nm; tilt Pd80nm/Au60nm

Lift-off – 2hrs 50°C acetone, 5mins IPA and N_2 blow dry.

Dry etch – T-gate etching: 25 sccm/ 25sccm SF_6/N_2, power 100W, 15mTorr, 20% over-etch time

Dry etch – T-gate etching: 25sccm $SiCl_4$, power 100W, 8mTorr, 20% over-etch time

5. Ohmic contact

Clean Substrate – 5min Acetone, 5min IPA, DI water rinse and N_2 blow dry.

Spin Resist – 8% 2010 PMMA., 4krpm, 60s

Bake – 137°C hotplate, 2mins

Spin Resist – 8% 2042 PMMA., 5krpm, 60s

Bake – 137°C hotplate, 2mins

Exposure – VB6 e-beam lithography. Dose 475 $\mu C/cm^2$, 16nA beam, VRU13.

Develop – 45s IPA: MIBK (2.5:1) at 23°C, 20s IPA rinse and N_2 blow dry.

Metallise – 30s 4:1 H_2O: HCl de-oxidise, H_2O rinse, Ar etch 30s, 8nm Ni/15nm Ti/15nm Pd/100nm Au

Lift-off – 2hrs 50°C acetone, 5mins IPA and N_2 blow dry.

A.2 Baseline non-planar InGaAs Tunnel-FET (EBL)

1. Marker

   Clean Substrate – 5min ultrasonic Acetone, 5min ultrasonic IPA, water rinse and N_2 blow dry.

   Metallisation – 30s 4:1 H_2O: HCl de-oxidise, H_2O rinse, Ar etch 30s, 15nm Mo/5nm Ti

   Spin Resist – 8% 2010 PMMA., 4krpm, 60s

   Bake – 137°C, 2mins

   Spin Resist – 8% 2042 PMMA., 5krpm, 60s

   Bake – 137°C, 2mins

   Exposure – VB6 e-beam lithography. Dose 475 $\mu C/cm^2$, 16nA beam, VRU13.

   Develop – 45s IPA: MIBK (2.5:1) at 23°C, 20s IPA rinse and N_2 blow dry.

   Metallise – Ti15nm/Pt30nm/Ti15nm/Pt30nm/ Ti15nm/Pt30nm.

   Lift-off – 2hrs 50°C acetone, 5mins IPA and N_2 blow dry.

2. Bondpad

   Clean Substrate – 5min Acetone, 5min IPA, DI water rinse and N_2 blow dry.

   Spin Resist – 8% 2010 PMMA., 4krpm, 60s

   Bake – 137°C hotplate, 2mins

   Spin Resist – 8% 2042 PMMA., 5krpm, 60s

   Bake – 137°C hotplate, 2mins

   Exposure – VB6 e-beam lithography. Dose 475 $\mu C/cm^2$, 16nA beam, VRU13.

   Develop – 45s IPA: MIBK (2.5:1) at 23°C, 20s IPA rinse and N_2 blow dry.

   Metallise – Ti10nm/Pt30nm

   Lift-off – 2hrs 50°C acetone, 5mins IPA and N_2 blow dry.

3. Non-planar MOS Channel

   Clean Substrate – 5min Acetone, 5min IPA, DI water rinse and N_2 blow dry.

   Spin Resist – 1:3 HSQ: MIBK, 3krpm, 60s.

   Bake – 90°C hotplate, 2min

   Exposure – VB6 e-beam lithography. Dose 3700 $\mu C/cm^2$, 1nA beam, VRU2.

   Develop – 30s TMAH: H_2O (1:3) at 23°C, 60s water rinse, 15s IPA rinse and N_2 blow dry.

   Dry etch – STS-ICP etching: 15 sccm/ 25sccm SF_6/C_4F_8. Platen power 2W, coil power 600W, 5mTorr, 20% over-etch time

   Dry etch – Cobra etching: 6 sccm/ 10sccm/ 15sccm CH_4/Cl_2/ H_2, Platen power 25W, coil power 750W, 8mTorr, 20% over-etch time

   Pre-treatment – ALD: 10 cycles of H_2/TMA pulse

   In-situ deposition – ALD: 20 cycles of plasma HfO_2 at 300°C and 130 cycles of plasma TiN at 350°C

4. Gate Pad

   Clean Substrate – 5min Acetone, 5min IPA, DI water rinse and N_2 blow dry.

   Spin Resist – 8% 2010 PMMA., 4krpm, 60s

   Bake – 137°C hotplate, 2mins

   Spin Resist – 8% 2042 PMMA., 5krpm, 60s

   Bake – 137°C hotplate, 2mins

   Exposure – VB6 e-beam lithography. Dose 475 $\mu C/cm^2$, 16nA beam, VRU13.

   Develop – 45s IPA: MIBK (2.5:1) at 23°C, 20s IPA rinse and N_2 blow dry.

   Metallise –Pd80nm/Au60nm

   Lift-off – 2hrs 50°C acetone, 5mins IPA and N_2 blow dry.

5. Bottom spacer

   Clean Substrate – 5min Acetone, 5min IPA, DI water rinse and N_2 blow dry.

   Spin Resist – 1:3 HSQ: MIBK, 3krpm, 60s.

   Bake – 90°C hotplate, 2min

   Exposure – VB6 e-beam lithography. Dose 3000 $\mu C/cm^2$, 16nA beam, VRU13.

   Develop – 30s TMAH: H_2O (1:3) at 23°C, 60s water rinse, 15s IPA rinse and N_2 blow dry.

   Dry etch – T-gate etching: 25 sccm/ 25sccm SF_6/N_2, power 100W, 15mTorr, 20% over-etch time

   Dry etch – T-gate etching: 25sccm $SiCl_4$, power 100W, 8mTorr, 20% over-etch time

   Dry etch – ICP180 etching: 6 sccm/ 10sccm/ 15sccm $CH_4/Cl_2/H_2$, Platen power 25W, coil power 750W, 8mTorr, 15s.

6. Ohmic contact

   Clean Substrate – 5min Acetone, 5min IPA, DI water rinse and N_2 blow dry.

   Spin Resist – 8% 2010 PMMA., 4krpm, 60s

   Bake – 137°C hotplate, 2mins

   Spin Resist – 8% 2042 PMMA., 5krpm, 60s

   Bake – 137°C hotplate, 2mins

   Exposure – VB6 e-beam lithography. Dose 475 $\mu C/cm^2$, 16nA beam, VRU13.

   Develop – 45s IPA: MIBK (2.5:1) at 23°C, 20s IPA rinse and N_2 blow dry.

   Metallise – 30s 4:1 H_2O: HCl de-oxidise, H_2O rinse, Ar etch 30s, 8nm Ni/15nm Ti/15nm Pd/100nm Au

   Lift-off – 2hrs 50°C acetone, 5mins IPA and N_2 blow dry.

7. Top spacer

   Clean Substrate – 5min Acetone, 5min IPA, DI water rinse and N_2 blow dry.

   Spin Resist – 1:3 HSQ: MIBK, 3krpm, 60s.

   Bake – 90°C hotplate, 2min

Exposure – VB6 e-beam lithography. Dose 1000 $\mu C/cm^2$, 16nA beam, VRU13.

Develop – 30s TMAH: H_2O (1:3) at 23°C, 60s water rinse, 15s IPA rinse and N_2 blow dry.

Dry etch – ICP etching: 6 sccm/ 10sccm/ 15sccm $CH_4/Cl_2/H_2$, Platen power 25W, coil power 750W, 8mTorr, 30s.

8. Source

Clean Substrate – 5min Acetone, 5min IPA, DI water rinse and N_2 blow dry.

Spin Resist – 8% 2010 PMMA., 4krpm, 60s

Bake – 137°C hotplate, 2mins

Spin Resist – 8% 2042 PMMA., 5krpm, 60s

Bake – 137°C hotplate, 2mins

Exposure – VB6 e-beam lithography. Dose 475 $\mu C/cm^2$, 16nA beam, VRU13.

Develop – 45s IPA: MIBK (2.5:1) at 23°C, 20s IPA rinse and N_2 blow dry.

Metallise –Ar etch 30s, 15nm Mo/15nm Ti