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University of Glasgow

MM-Wave Frequencies GaN-on-Si HEMTs and MMIC Technology Development

by

Abdalla Eblabla

A thesis submitted in fulfilment for the degree of Doctor of Philosophy

in the

Division of Electronics and Electrical Engineering

School of Engineering

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Abstract

Gallium Nitride (GaN)-based High Electron Mobility Transistors (HEMTs) grown on Silicon (Si) substrates technology is emerging as one of the most promising candidates for cost effective, high-power, high-frequency Integrated Circuit (IC) applications; operating at Microwave and Millimetre (mm)-wave frequencies. To capitalise on the advantages of RF GaN technology grown on Low resistivity (LR) Si substrates; RF losses due to the Si substrate must be eliminated at the active devices, passive devices and interconnect. Low resistivity Si substrates are intrinsic prone to RF losses and high resistivity (HR) Si substrates shown to exhibit RF losses as a result of operating substrate temperature at the system level. Therefore, obtaining a viable high-performance RF GaN-on both LR and HR Si device remains a challenge for this technology. In an attempt to overcome these issues, Microwave Monolithic Integrated Circuit (MMIC)-compatible technology was developed for the first time aiming to eliminate the substrate coupling effect for the realisation of high performance passive and active devices on GaN-on-Si substrates for mm-wave MMIC applications.

To validate the novel RF GaN-on-Si substrates developed technology in this work, several fabrication techniques approaches were investigated and developed in order to improve the DC and RF performance of developed AlGaN/GaN HEMTs. The electrical characteristics were analysed based on the extracted small-signal equivalent circuit model from the measured data using on-wafer probes. Device parasitic effects associated with input/output contact pads were minimised by optimising the layout of the device. Consequently, using a proper device layout design, downscaling the AlGaN Schottky barrier and inserting an AlN interlayer in the material structure were found to have effectively improve the RF performance, where a maximum cut-off frequency, f_T of 79.75 GHz and maximum oscillation frequency, f_{MAX} of 82.5 GHz were obtained. To our knowledge, these results were the best performance AlGaN/GaN HEMTs grown on LR Si, and comparable to AlGaN/GaN HEMTs grown on Semi Insulating (SI)-SiC and HR Si substrates with similar gate lengths.

Novel low-loss transmission media technology on GaN-on-LR Silicon was also developed and demonstrated in this work. Two design structures were successfully realised providing complete isolation of the conductive substrate by employing a ground plane, a 5 μm-thick

benzocyclobutene (BCB) and an additional elevation of elevated line traces supported by air-bridges. Consequently, an attenuation constant, α, of better than 0.06 Np/mm and 0.45 Np/mm were achieved at frequencies of up to 76 GHz and 750 GHz, respectively, with matching (S_{11}) of better than -15 dB over the whole frequency range. These results for the passive components and transmission media interconnect performance exhibited a better performance than those currently used in MMICs' conventional transmission media technology, such as Microstrip and Coplanar waveguide (CPW) on a standard SI-GaAs substrates. To prove the capabilities and efficiency of the developed transmission media, low-loss in-line series and shunt Metal-Insulator-Metal (MIM) capacitors were presented. In addition, High-Q on-chip inductors employing elevated traces and a BCB interface layer were also realized. A peak Q-factor of 22 at 24 GHz and f_{SRF} of 59 GHz was achieved for 0.81 nH inductors. The realised MIM capacitors and spiral inductors were characterized based on the extracted small-signal equivalent circuit model. The developed transmission media and passive devices technology offered a promising platform for integrated RF GaN-HEMTs on Si for the realisation of high-performance monolithic integrated circuits for mm-wave applications.

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Associated Publications

Journal papers

1. **A. Eblabla**, X. Li, D. J. Wallis, I. Guiney and K. Elgaid, "High Performance MMIC Inductors for GaN-on-Low Resistivity Silicon for Microwave Applications," in *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 2, pp. 99-101, 2018.
2. **A. M. Eblabla**, X. Li, D. J. Wallis, I. Guiney and K. Elgaid, "GaN on Low-Resistivity Silicon THz High-Q Passive Device Technology," in *IEEE Transactions on Terahertz Science and Technology*, vol. 7, no. 1, pp. 93-97, Jan. 2017.
3. **A. Eblabla**, B. Benakaprasad, X. Li, D. J. Wallis, I. Guiney and K. Elgaid, "Low-Loss MMICs Viable Transmission Media for GaN-on-Low Resistivity Silicon Technology," in *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 1, pp. 10-12, Jan. 2017.
4. **A. Eblabla**, X. Li, I. Thayne, D. J. Wallis, I. Guiney and K. Elgaid, "High Performance GaN High Electron Mobility Transistors on Low Resistivity Silicon for X-Band Applications," in *IEEE Electron Device Letters*, vol. 36, no. 9, pp. 899-901, Sept. 2015.
5. **A. Eblabla**, D. J. Wallis, I. Guiney and K. Elgaid, "Novel Shielded Coplanar Waveguides on GaN-on-Low Resistivity Si Substrates for MMIC Applications," in *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 7, pp. 427-429, July 2015.

Conference papers

1. **A. Eblabla**, B. Benakaprasad, X. Li, D. J. Wallis, I. Guiney, C. Humphreys and K. Elgaid "Passive components technology for THz-Monolithic Integrated Circuits (THz-MIC)," *2017 18th International Radar Symposium (IRS)*, Prague, Czech Republic, 2017, pp. 1-7.
2. **A. Eblabla**, X. Li, I. Thayne, D. J. Wallis, I. Guiney and K. Elgaid, "MMIC-Compatible Microstrip Technology for GaN-HEMTs on Low Resistivity Silicon Substrate" *the International Workshop on Nitride Semiconductors (IWN 2016)*, October 2-7, 2016, Orlando, Florida.

3. **A. Eblabla**, X. Li, D. J. Wallis, I. Guiney & K. Elgaid, “GaN-based HEMTs on Low Resistivity Silicon Technology for Microwave Applications” *the* 8th *Wide Bandgap Semiconductor and Components Workshop*, ESA/ECSAT, Harwell, UK, 2016.

4. **A. Eblabla**, B. Benakaprasad, X. Li, I. Thayne, D. J. Wallis, I. Guiney, C. Humphreys and K. Elgaid, “High Frequency Active and Passives Devices using GaN on Low Resistivity Silicon”, *ARMMS RF & Microwave Society Conference*, The Oxford Belfry, UK 2016.

5. **A. Eblabla**, B. Benakaprasad, X. Li, D. J. Wallis, I. Guiney, C. Humphreys and K**.** Elgaid, “Effect of AlN Spacer in the Layer Structure on High RF Performance GaN-Based HEMTs on Low Resistivity Silicon at K-Band Application”, 11th *International Conference on Nitride Semiconductors (ICNS-11),* Beijing, China, 2015.

6. B. Benakaprasad, **A. Eblabla**, X. Li, D. J. Wallis, I. Guiney and K. Elgaid, "Design and performance comparison of various terahertz microstrip antennas on GaN-on-low resistivity silicon substrates for TMIC," *2016 Asia-Pacific Microwave Conference (APMC)*, New Delhi, 2016, pp. 1-4.

7. B. Benakaprasad, **A. Eblabla**, X. Li, D. J. Wallis, I. Guiney, C. Humphreys and K. Elgaid "Terahertz microstrip elevated stack antenna technology on GaN-on-low resistivity silicon substrates for TMIC," *2016 46th European Microwave Conference (EuMC)*, London, 2016, pp. 413-416.

8. B. Benakaprasad, **A. Eblabla**, X. Li, D. J. Wallis, I. Guiney, C. Humphreys and K. Elgaid "Terahertz monolithic integrated circuits (TMICs) array antenna technology on GaN-on-Low resistivity silicon substrates," *2016, 41st International Conference on Infrared, Millimetre, and Terahertz waves (IRMMW-THz)*, Copenhagen, 2016, pp. 1-2.

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List of Abbreviations

2DEG: Two-Dimensional Electron Gas

5G: Fifth Generation

ABF: Ajinomoto Build-up Film

ALD: Atomic Layer Deposition

AlGaN: Aluminium Gallium Nitride

AlN: Aluminium Nitride

BCB: Benzocyclobutene

BELL: Beam-writer Exposure for Lithography Engineers

CAD: Computer Aided Design

CVD: Chemical Vapour Deposition

DC: Direct Current

DHFET: Double-Heterostructures Field Effect Transistor

DUT: Device Under Test

EBL: Electron Beam Lithography

GaN: Gallium Nitride

GHz: Gigahertz

HCL: Hydrochloric Acid

HEMT: High Electron Mobility Transistor

HF: Hydrofluoric Acid

HFSS: High Frequency Structure Simulator

HR: High Resistivity

ICP-CVD: Inductively-Coupled Plasma Chemical Vapour Deposition

ICP-RIE: Inductively-Coupled Plasma Reactive Ion Etching

IP: Internet Provider

ISS: Impedance Standard Substrate

LDMOS: Laterally Diffused Metal Oxide Semiconductor

LOR: Lift-Off Resist

LR: Low Resistivity

MAX: Maximum Available Gain

MESFET: Metal-Semiconductor Field Effect Transistor

MIM: Metal-Insulator-Metal

MMIC: Microwave Monolithic Integrated Circuit

MOCVD: Metal-Organic Chemical Vapor Deposition

PECVD: Plasma Enhanced Chemical Vapour Deposition

PMMA: Poly-Methyl Methacrylate

RF: Radio Frequency

RIE: Reactive Ion Etching

SCE: Short Channel Effect

SEM: Scanned Electron Microscopy

SI: Semi-Insulating

Si: Silicon

Si_3N_4: silicon nitride

SiC: silicon carbide

SiO_2: silicon dioxide

SOLT: Short-Open-Load-Thru

SRF: Self-Resonance Frequency

TE: Transverse Electric

TEM: Transverse Electromagnetic

TM: Transverse Magnetic

TMIC: THz Monolithic Integrated Circuits

UV: Ultra-Violet

VDP: Van-Der-Pauw

WLAN: Wireless Local Networks

Chapter 1

Introduction and the State of the Art

1.1 Demand for High Output Power and High Frequency Transistors at mm-wave Frequencies

The demand for creating smaller chip sizes along with greater functionality has led to tremendous semiconductor technology development and the establishment of a new market for semiconductor devices. Silicon (Si)-based devices offer a cost-effective and promising performance technology for data processing applications. Recently, there has been significant research and development aiming to increase the frequency of operation in order to satisfy the requirements for high frequency and high power applications. The broadcasting of telecommunication signals is an example of the power amplifiers' market [1]. Figure 1.1 shows how rapidly the worldwide telecommunications sector has grown since 2001. The number of internet/mobile users has intensively increased as a result of the development of wireless local networks (WLAN) and the enhancement of mobile phone technologies. According to studies from CISCO, it is expected that by 2021 there will be nearly 4.6 billion global internet users, and consequently the Internet Provider (IP) traffic will reach an annual run rate of 3.3 zettabytes [2]. This will lead to a massive demand on bandwidths and high data rate requirements. Therefore, efficient power amplifiers operating in the mm-wave frequency range are essential for today's telecommunication market.

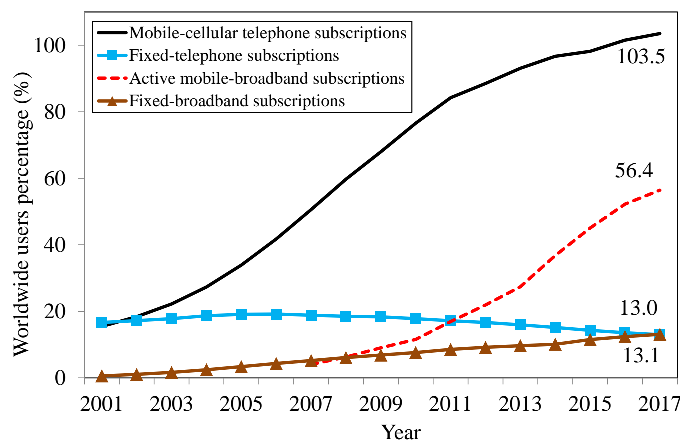


Figure 1.1: Wireless communications and internet access services growth over the last decades. Source: ITU World Telecommunications / ICT Indicator Database.

The availability of the 57-64 GHz licence-free frequency range has made high-power amplifiers operating at frequencies beyond 50 GHz attractive candidates for various applications, including short-range point-to-point wireless Gbit/s and inter-satellite communications. At V-band frequency range (50-57 GHz), the existence of atmospheric attenuation makes it possible to identify multiple users in a compact area with mitigated signal interference. This could be ultimately utilised for the next generation WLAN technologies. In addition to wireless communication applications, high power devices are commonly used at W-band frequency ranges (74-77 GHz) for automotive radar applications, which are essentially used for adaptive cruise and safety systems.

Gallium nitride (GaN)-based devices are emerging as promising solid-state microwave power devices because of their capabilities in enabling power-switching operations at high voltages/currents at high speed and greater efficiency at frequencies beyond 50 GHz [3]. This is attributed to their inherent material properties, such as a wide bandgap (> 3 eV), a high critical electrical field (2-4 MV/cm) and high saturation electron drift velocity (> 2×10^7 V/cm). Table 1.1 demonstrates the properties of the widely used semiconductor materials [4] [5]. For heat dissipation purposes and high frequency operation, GaN is typically grown on high thermal and Semi-Insulating (SI) substrates, such as silicon carbide (SiC) and Diamond) to allow high power and high frequency operation [6] [7]. SiC is more desirable for GaN-based devices since it has a close lattice match with III-nitrides [5]. Therefore, GaN-based transistors are considered as superior candidates that could be utilized in many of the above applications.

Table 1.1: Physical properties for group III-Nitrides compared with other semiconductor of interest.

Material	Lattice constant (Å)	Energy bandgap E_G (eV)	Maximum electrical field (MV/cm)	Dielectric constant (ε_r)	Thermal conductivity (w/cmK)	Carrier mobility (cm^2/Vs)
GaN	3.189	3.4	2	7.8	1.4	2000
AlN	3.112	6.2	-	8.5	1.8-5.5	300
SiC	3.081	3.3	2.5	9.8	4.9	980
Diamond	3.567	5.5	10	5.5	10-20	1800
Si	5.73	1.1	0.3	11.9	1.5	1350

5.1 GaN-based High Electron Mobility Transistors (HEMTs) on Si Technology

As a n example of utilising GaN-on-LR Si technology, recent work on the integration of GaN HEMT based gate driver and buck converters on SI-SiC substrates has achieved envelope tracking bandwidths of 20 MHz with power device switching frequencies up to 200 MHz [8]. The potential use of this circuit for 5G applications using GaN on Si substrates were both power and RF GaN on the same chip will offer the additional benefit of lower cost. Currently GaN grown on SI-SiC substrates are likely the best solution in terms of output power, thermal management and operation frequency. This technology have been rapidly developed over the last two decades, where current densities in excess of 3 A/mm and RF performance with cut-off frequency/maximum oscillation frequency (f_T/f_{MAX}) 453/446 GHz have been demonstrated [9]. However, SI-SiC substrates are expensive and have limited availability in large substrate diameters, which is considered as a major concern for GaN-electronics. These factors coupled with the more demanding back side fabrication process for the realization of Microstrip Microwave Monolithic Integrated Circuits (MMICs) ultimately increase the cost of GaN-on-SiC electronics [10]. To leverage the economies of scale offered by large wafer diameters, GaN-based HEMT structures grown on high-resistivity (HR) Si substrates of diameters of up to 100 mm have been realized. Outstanding DC and RF performance have been achieved as a result of the advanced epitaxial material growth, where a current density of nearly 1 A/mm and an RF performance with f_T/f_{MAX} of 78/190 GHz respectively, have been demonstrated [11]. Table 1.2 summarises the most recent research and development of GaN-based heterostructures grown on Si substrates. It can clearly be seen that innovative fabrication technology and material structure optimisation are strongly required for high current densities (> 0.8 mA/mm) along with high RF characteristics (f_T > 60 GHz), as indicated in Figure 1.2. The major breakthroughs can be summarised as follows:

- Development of regrowth based source/drain ohmic contacts (R_C) for power loss reduction and RF characteristics enhancement [12].
- Adoption of in-situ Si_3N_4 cap layer early passivation as part of the material growth process for device reliability enhancement and gate-leakage mitigation [13].
- Ultra-thin Schottky barrier layers which allow scaling the gate length and thus improving the DC and RF performance [11] [14].

- Insertion of an optimised AlN spacer layer and the use of AlGaN back barriers for better electron confinement and higher current densities [15].

Table 1.2: State of the art DC and RF performance of GaN-based heterostructures grown on Si.

Technology	Schottky barrier (nm)	L_G (nm)	2DEG (cm^{-2})	DC					RF		Ref.
				µ (cm^2/V.s)	R_{SH} (Ω/□)	R_C (Ω/mm)	I_{DS_MAX} (A/mm)	G_{MAX} (mS/mm)	f_T (GHz)	f_{MAX} (GHz)	
-	AlGaN	150	-	-	-	-	-	-	60	160	[16]
-	12.5 AlGaN	90	1.17×10^{13}	2000	314	0.45	0.82	440	100	206	[17]
-	AlGaN	500	-	-	-	0.3	0.75	220	24.6	45.4	[18]
Regrowth contacts	20 AlGaN	75	1.44×10^{13}	1006		0.11	1.3	290	153	22	[19]
In-situ AlN	18 AlGaN	203			322	0.6	0.93	335	54	182	[20]
	30 AlGaN	170	8×10^{12}	1600	500	-	0.55	215	46	92	[21]
-AlN spacer -Si-based contacts	20 AlGaN	150	-	-	-	-	0.9	320	55	130	[22]
BCB encapsulation	25 AlGaN	150	8×10^{12}	1456		0.2	0.953	300	50	47	[23]
AlGaN back barrier	17.5 AlGaN	160	9.4×10^{12}	1550	430	0.3	0.8	260	63	226	[24]
Ta/Si contacts	18 AlGaN	150	1.1×10^{13}	1450		0.24	0.83	250	39	39	[25]
-In-situ Si_3N_4 -AlGaN back barrier	25 AlGaN	300	-	1500	530	-	0.85	220	24	47	[26]
	6 AlN	100	2×10^{13}	1400	240	0.35	1.8	500	80	192	[13]
-In-situ Si_3N_4 -AlGaN back barrier	9 AlInN	100	2.6×10^{13}	400	460	0.54	1.3	330	102	89	[15]
-In-situ Si_3N_4 -AlGaN back barrier	6 AlN	200	2×10^{13}	1400	240	0.35	1.8	470	52	91	[14]
-	6 AlN	120	2×10^{13}	1400	240	0.4	1.5	550	75	102	[27]
-	4 AlN	120	1.5×10^{13}	1250	310	0.35	1	390	78	190	[11]

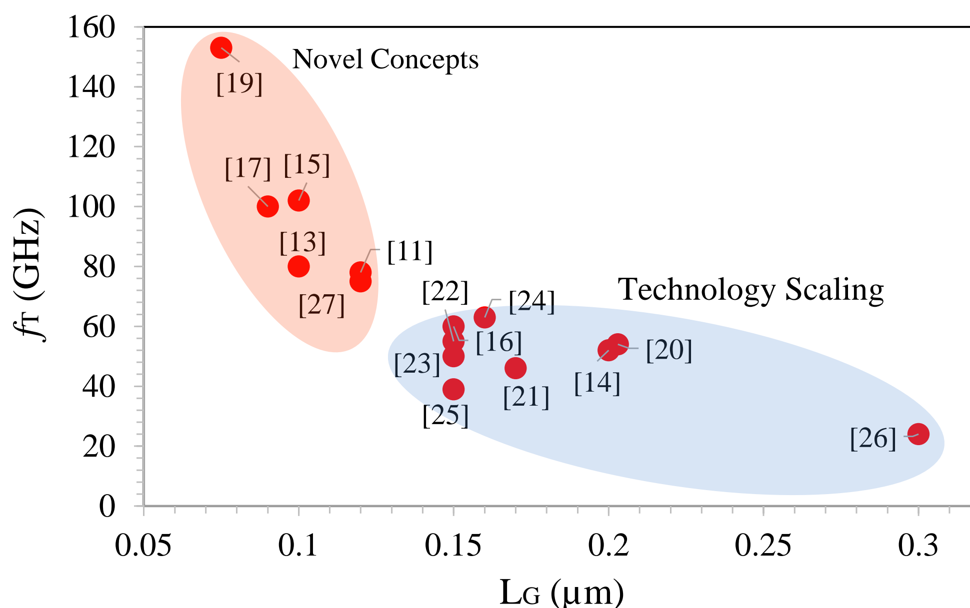


Figure 1.2: Summary of 'State of the Art' GaN-based heterostructures on Si performance (f_T) versus gate-length (L_G), achieved by the international research laboratories.

One of the major issues associated with growing GaN epitaxial layers on HR Si substrates is RF losses, as a result of the formation of a thin conductive layer at the interface following the diffusion of Ga into the Si substrate. This can be classified as an epitaxial material growth issue and has been resolved by controlling the Ga discussion throughout the growth process [28] [29]. In addition to the outstanding DC and RF performance obtained by GaN-based HEMTs on HR Si, HR Si substrates are still relatively expensive compared to the more commonly used LR Si substrates and maintaining high resistivity through the high temperature GaN growth process is challenging. Several research teams have realized RF GaN HEMTs on LR Si. Despite the well-behaved DC performance, these devices have shown a lower RF performance than that achieved using SiC, Sapphire or HR Si [30] [31]. The lower RF performance is mainly because of the RF signal coupling to the conductive Si substrate.

The technology development for these applications initially aims to demonstrate MMICs. However, not only does the parasitic loss associated with LR Si substrate negatively affect the RF performance of transistors but also makes it impossible to realise standard transmission media technology for MMIC applications.

5.2 Transmission Media Technology for GaN-on-LR Si Substrates.

Realization of low-loss waveguides, capacitors and inductors with high-quality factors at mm-wave frequencies are of great importance for circuit application where interconnects and passive components are needed. Therefore, low-loss transmission media are necessarily required for cost-effective GaN-based MMIC technology.

Previously, a number of researchers have attempted to develop high quality transmission media on LR Si substrates. Some reports have shown a reduction in losses using thick insulators such as polyamide [32], Ajinomoto Build-up Film (ABF) and SU-8 [33] but these still have relatively high attenuation at mm-wave frequencies. On the other hand, reports have shown that attaching silicon dioxide (SiO_2) to the surface of the Si substrate, induces a low-resistivity layer at the interface between the SiO_2 and the Si surface [34]. These phenomena cause degradation of the attenuation constant. Several approaches have been suggested to avoid such undesirable effects, such as introducing polysilicon at the Si-SiO_2 interface [35], removing the Si substrate from the backside substrate by micromachining [36] and using the floating shield technique [37]. However, each of these methods requires complex and lengthy fabrication processes. Insertion of a low-losses, low dielectric constant, *k*, layer of benzocyclobutene (BCB) as an insulator was proved to be another technique for substrate coupling reduction [38]. This approach, compared to other more complicated techniques [36] [37], has the advantage of accommodating active circuits underneath the passive components and interconnectors with no degradation of active device performance [39].

5.3 Research Goal and Objects

The main focus of this project is to develop a viable MMIC technology for GaN-based HEMTs grown on LR and HR Si substrates for mm-wave frequencies applications. The challenge in this technology development is to decouple the substrate from both active, passive devices and transmission media interconnect. LR Si substrates are intrinsic lossy to the mm-wave signal. In addition, recent studies of AlGaN/GaN HEMTs grown on HR Si substrates have shown degradation of mm-wave performance at high temperature (i.e. telecommunication basestation applications where devices are operated at high power); this is due to the increase of the intrinsic carrier density in the HR Si substrate [40]. Despite that much lower temperature

dependence on mm-wave signal was observed on the AlGaN/GaN HEMTs grown on LR Si and exhibits better performance at high temperature than that of AlGaN/GaN HEMTs grown on HR Si, it remains not viable technology for mm-wave applications. This proves that the technology developed in this work can effectively be utilised independent of substrate technology with better performance at mm-wave and THz frequencies than that of conventional Microstrip and Coplanar waveguide (CPW). As mentioned earlier, the RF performance of GaN-on-LR Si substrates technology remains relatively poor, compared to those grown on SI-SiC and HR Si substrates at room temperatures. This is mainly because of the parasitic loss caused by the conductive substrate. Mitigating this issue is the first step towards the realisation of high performance MMIC circuits' technology at mm-wave frequencies. The main objectives of this work are to:

- develop a reliable, high yield, cost-effective and MMIC-compatible fabrication process for GaN-on-LR Si technology.
- demonstrate high DC and RF performance AlGaN/GaN HEMTs on LR Si for V-band and higher frequencies applications.
- realise a low-loss transmission media technology that can be integrated with the demonstrated active devices for future MMIC applications.

5.4 Thesis Outline

This thesis consists of five chapters:

Chapter 1 provides a brief overview of the state-of-the-art GaN-based heterostructures grown on Si substrates technology, followed by the introduction of GaN-on-LR Si technology as an alternative solution for cost-effective MMIC applications. The challenges associated with the realisation of both active and passive MMIC devices at mm-wave frequencies using this technology are also addressed.

Chapter 2 describes the fabrication techniques required for the realisation of MMIC-compatible active and passive devices using GaN-based on LR Si technology for mm-wave applications. It begins by introducing the material properties used in this work, followed by a brief description of the main fabrication processing techniques, such as sample preparation,

lithography, metallisation and dry etch. Then, the detailed fabrication process of AlGaN/GaN HEMTs on LR Si is provided. Finally, the fabrication process of novel transmission media technology and various passive components is introduced.

Chapter 3 focuses on the active devices, namely AlGaN/GaN HEMTs on LR Si. This includes a summary of the theory and operation of HEMTs in briefly and with special emphasis on the most critical figures of merit that influence the DC and RF performance of the devices. In addition, the RF performance of HEMTs fabricated is further analysed using the RF small-signal equivalent circuit model. Next, the DC and RF characteristics of the AlGaN/GaN HEMTs developed on LR Si are systematically introduced; various material structures and device geometries are investigated aiming for performance enhancement.

Chapter 4 is devoted to the development of a low-loss MMIC interconnect transmission media technology for GaN-on-LR Si technology. An overview of the basic operation of Microstrip lines and passive elements, such as Metal-Insulator-Metal (MIM) capacitors and spiral inductors, is provided. Novel transmission media interconnect for MMIC technology (Shielded-Microstrip and Shielded-Elevated Microstrip lines) is also presented. 3-D full wave electromagnetic simulations using Ansoft HFSS^{TM} of the proposed transmission media are carried out as per fabrication requirements. In-line shunt and series MIM capacitors, and High-Q inductors are introduced, proving the viability of the new proposed transmission media for MMIC technology compatibility. The equivalent circuit models for the demonstrated passive components are also discussed.

Chapter 5 concludes this research report by summarising its findings along with a discussion on the potential for future work.

Chapter 2

Fabrication Techniques

2.1 Introduction

This chapter outlines the vertical material layer structures and the fabrication process required for the realisation of active and passive devices on GaN-based HEMTs grown on LR Si substrates. The fabrication process was carried out at the James Watt Nanofabrication Centre (JWNC) at the University of Glasgow. All levels of device definition utilised in this work are compatible with MMIC technology. The material vertical layer structures used in device fabrication are described. Next, the main fabrication process including sample preparation, Electron-beam (e-beam) lithography, photolithography, dry etch and deposition of dielectrics and metals are presented, followed by a detailed description of each step in the fabrication process of AlGaN/GaN HEMTs and transmission media on LR Si substrate. The limitations and challenges faced while carrying out the technology development are outlined. Finally, the conclusions are summaries.

2.2 Material Structure

GaN-based HEMT structures are based on the growth of stack layers with different bandgaps and polarisation fields, which enables the creation of discontinuity in the polarisation field and surface charges at the heterointerface. The two dimensional electron gas (2DEG) channel is formed by the electron compensation of the induced positive charge, where electrons are confined into a quantum well. Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD) are among the most commonly used techniques for the epitaxial material growth. The following layers, from bottom to top, form the typical epitaxial layer structure of GaN-based HEMTs:

- *Nucleation buffer layers*: Thin intermediate layers of AlN, GaN, AlGaN or graded AlGaN are usually grown on the non-native substrate (e.g. Si) to compensate the lattice mismatch and stress between the GaN and substrate.

- *Buffer layer*: A lower bandgap material (e.g. GaN) is usually grown on the nucleation layers. High-quality buffer material with low defect density and high resistivity is essential for optimal device performance (e.g. full channel pinch-off, low gate leakage current, high drain-source current saturation and low microwave frequencies losses) [41].

- *Spacer layer*: A thin optimised AlN interlayer between the buffer layer and barrier layer plays an important role in decreasing electron scattering and hence improving the device 2DEG mobility [42].

- *Barrier layer*: A material with wider bandgap than the buffer layer is used as a barrier layer, e.g. $Al_xGa_{1-x}N$ and AlN. Device performance is strongly affected by the quality of this layer. The aluminium alloy concentration (x) and layer thickness determine the 2DEG density.

- *Cap layer*: A thin GaN cap layer (1-2 nm) is grown on the barrier layer to enhance gate current leakage as a result of increased effective Schottky barrier height, and to protect the epitaxial layer from oxidation [43].

2.3 Band diagram

Figure 2.1 illustrates the energy band diagram of AlGaN/GaN and AlGaN/AlN/GaN heterostructures. A conduction band offset is observed as a result of the conduction band energy variation at the material interfaces. This creates a triangular-like quantum well with lower energy levels, which attract electrons resulting in the formation of the 2DEG at the interface. The diagrams also show that a large effective conduction band offset is produced when inserting a thin AlN interlayer in the heterointerface of AlGaN/GaN. This is because of the potential drop across the spacer layer owing to large piezoelectric and spontaneous polarisation field. The conduction band offset increase in the presence of the AlN interlayer is evaluated by [42]:

$$\Delta E_c^{AlN} - \Delta E_c^{AlGaN} = \exp\left(\frac{\sigma_{AlN} - N_{2DEG}}{\varepsilon_{AlN}}\right) d_{AlN} \quad (2.1)$$

Where the offsets in the conduction bands between the AlGaN/AlN/GaN and AlGaN/GaN are indicated by ΔE_c^{AlN} and ΔE_c^{AlGaN}, respectively. N_{2DEG} represents the sheet carrier concentration of the structure with the AlN interlayer. ε_{AlN} is the AlN spacer dielectric constant, σ_{AlN} is the polarisation induced charge at the AlGaN/GaN interface and d_{AlN} is the AlN spacer thickness.

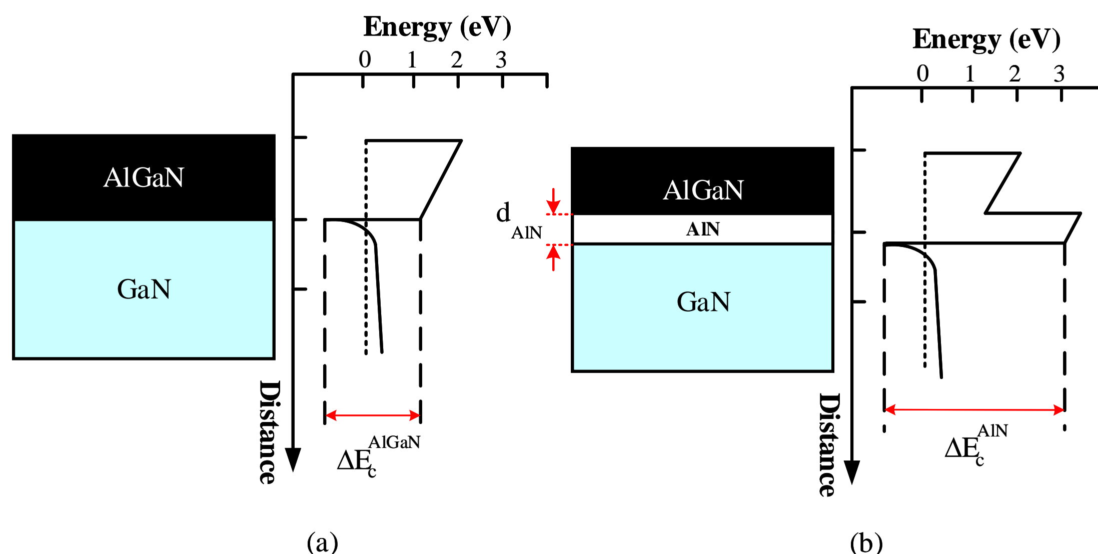


Figure 2.1: Illustration of the pattern of energy band diagram for the (a) AlGaN/GaN. And (b) AlGaN/AlN/GaN HEMTs [42]

The study in this work was carried out on AlGaN/GaN HEMTs supplied by the Cambridge Centre for GaN at the University of Cambridge. The epitaxial structures were grown by MOCVD on a 150 mm diameter p-type LR Si (σ < 10 Ω.cm) substrates. A number of material structures with identical layer stack order and slightly different thickness were used in this work, as shown in Figure 2.2. The layer stack, from the substrate up, consists of a 250/220 nm AlN nucleation layer followed by a 850/900 nm Fe-doped AlGaN graded buffer (to accommodate the lattice and thermal expansion miss-match), a 1.4/2.6 µm insulating Fe-doped GaN buffer layer and a GaN channel layer. The channel includes a 1 nm AlN spacer layer, a 27/9 nm $Al_{0.25}Ga_{0.75}N/Al_{0.35}Ga_{0.65}N$ barrier and a 2 nm GaN cap. Fe-doping in the GaN buffer makes the fabricated devices suitable for high power switching operation [44].

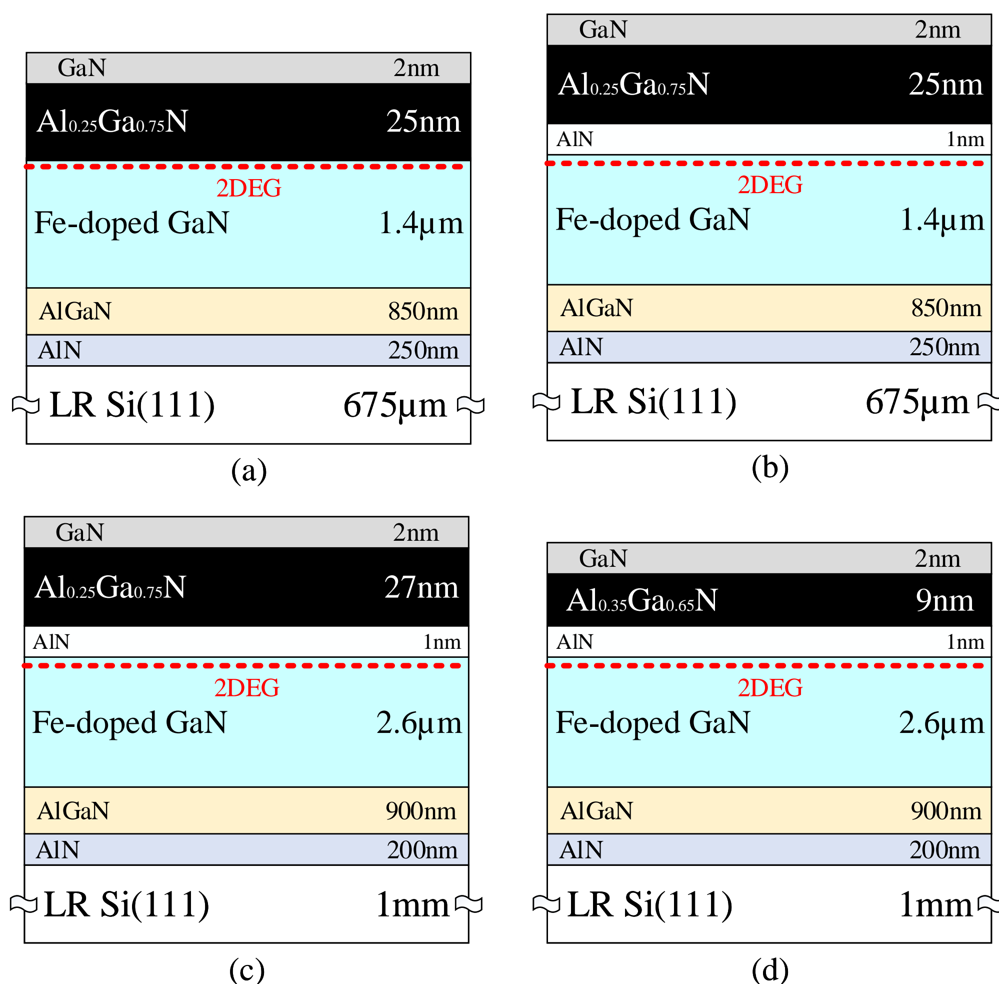


Figure 2.2: Schematic cross-sections of GaN-based HEMT layer sequences grown on LR Si epitaxial wafer structures used in this work.

2.4 Sample Preparation

Surface treatment and cleaning procedures are crucial prior to any fabrication process. There are two purposes in sample preparation; the removal of residues or debris resulting from cleaving the wafer and the removal of native oxide layers as a result of exposing the surface of a semiconductor to air. All samples used in this work were initially cleaned using standard cleaning procedures. The organic contamination of the sample surface was chemically and physically removed by soaking the sample in acetone, followed by isopropyl alcohol (IPA) in an ultrasonic water bath for five minutes. Finally, the sample was rinsed with de-ionised (DI) water and blown dry with a nitrogen N_2, gun. Commonly used Hydrochloric (HCL): H_2O and Hydrofluoric (HF): H_2O diluted acids can effectively remove oxide layers and carbon/hydrocarbon contamination, respectively [45].

2.5 Lithography

Lithography is one of the most critical processes required for the fabrication of modern micro-electronic integrated circuits [46]. The process involves the transformation of designed patterns into the sample surface coated with a radiation-sensitive film (resist) using a masking layer. Optical and e-beam are the most commonly used lithography techniques, and can be chosen based on the required minimum feature size and alignment accuracy. E-beam lithography is preferable for the fabrication of sub-micron devices. On the other hand, optical lithography is faster and cheaper compared to e-beam but has limited resolution and registration because of diffraction [47]. In this report, optical lithography was employed for the fabrication of passive components; active devices were fabricated using e-beam.

2.5.1 Optical Lithography

Optical lithography, also referred to as photolithography, can be defined as the process of transferring patterns from a mask plate to a wafer surface [47]. The process involves the ultra-violet (UV) light through an optical mask onto a substrate coated with photo-sensitive resist. In this work, the contact photolithography method was used for optimal pattern transfer from the mask. The optical mask (normally defined by e-beam or laser beam) was held in contact with the sample using a vacuum, while the UV light was focussed through a lens to ensure a

uniform and coherent exposure. Extra care was required during this process to reduce the risk of damaging the mask and contaminating the sample by a physical contact. This issue can be resolved by elevating the mask above the substrate. However, light diffraction around the mask features may consequently cause a slight deterioration in the achievable resolution. The optical system of a mask aligner used to replicate a mask pattern during photolithography is shown in Figure 2.3.

A resist image was obtained by replicating the mask pattern using a mask aligner, the UV light was collected from the source, and the mask pattern was illuminated by the condenser. Next, an aerial image was formed in order to provide a selective resist exposure. This was done by passing the illuminated light through the imaging lens. The patterned resist can be used for the subsequent fabrication process, e.g. dry etch, lift-off, plating, metallisation or implantation. Photoresists used for photolithography are generally classified into two types:

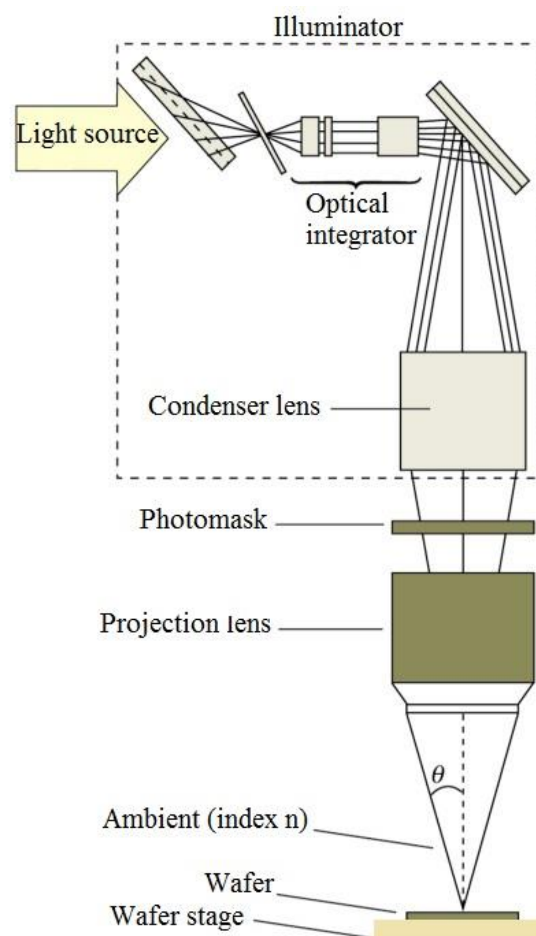


Figure 2.3: Illustration of the optical system of a mask aligner used to replicate a mask pattern during optical lithography [48].

positive and negative. Figure 2.4 illustrates the outcome of a positive and negative resist once a mask pattern is exposed onto a resist-coated wafer and the pattern is etched after resist development of the mask pattern. The reaction of the photoresists to UV light or radiation determines the type of the resist. For example, the areas exposed to UV light of the positive photoresist become more soluble in developer solutions and are then removed during the development process. As a consequence, the pattern transferred on the resist-coated sample will be a replication of the pattern on the mask. On the other hand, negative photoresists react oppositely to UV light exposure, where the unexposed regions become more soluble in developer solutions and are then removed during the development process.

In this report, contact photolithography was carried out using a Karl Suss MA6 mask aligner, which has a light source of λ = 365 nm [49]. This, however, limits the resolution to nearly 1 μm. Since a minimum feature size of 5 μm is required for passive component fabrication, the optical lithography technique was adequate to satisfy the resolution requirements. However, at frequencies beyond X-band, active device realisation required the use of gate technology of 0.3 μm or less along with good alignment accuracy, where several levels of lithography were needed. In this case, e-beam lithography had to be employed.

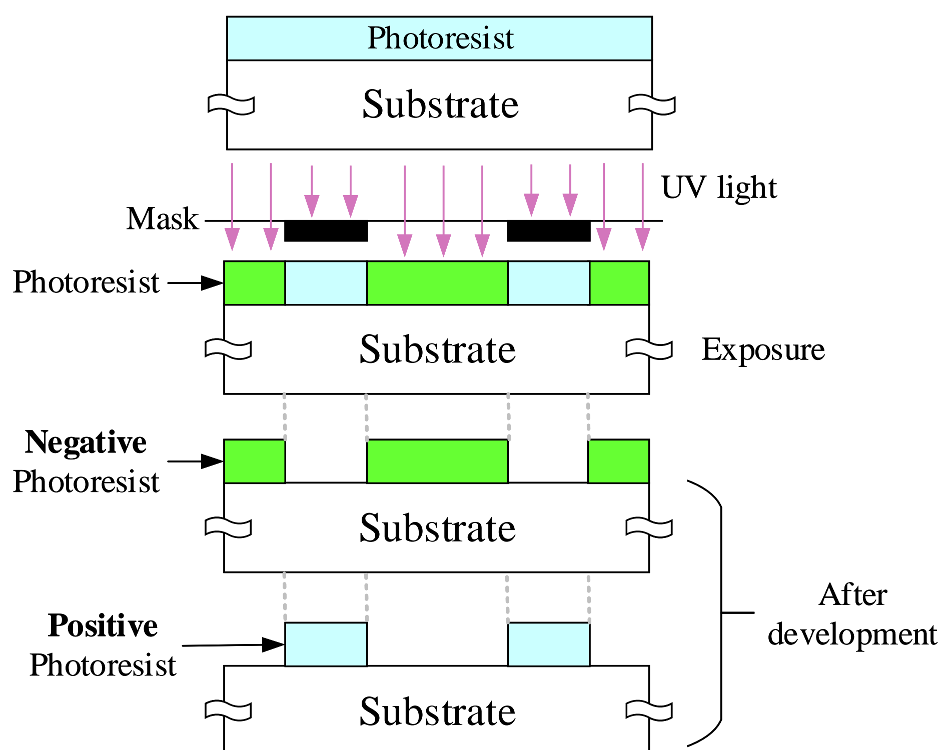


Figure 2.4: An image of a negative photoresist and positive photoresist after exposure.

2.5.2 E-beam Lithography

In electron beam lithography, which is also known as "e-beam" or EBL, patterns are written directly onto the resist-coated sample using a focussed electron beam. Unlike photolithography, EBL does not need a mask plate for pattern transfer. The patterns are initially generated or designed in software and then transferred to a computer-controlled exposure system which controls the highly confined electron beam for pattern production.

The principal components of a typical EBL machine are outlined in Figure 2.5. The pattern is written on the resist-coated substrate using a beam of electrons generated by the electron gun. Heating a tungsten filament results in electron emission, where the electrons gain sufficient energy to overcome their work function barrier. Moreover, the emission properties of the electron source are controlled by incorporating the electron gun with an electron or more. Electron optics within the column can accurately control the diameter, profile and direction of the electron beam, whereas, fine control of the stage positioning mechanism within the chamber can perform precise alignment. The vacuum system provides two main functions during operation; maintaining a constant pressure throughout the column and at the gun assembly, and controlling the pressure variation which is needed for loading and unloading samples. The supporting electronic system is used for power generation and signal transmission, which works as a system variation regulators throughout the e-beam machine. A master computer is used to drive the whole e-beam tool. In this work, electron beam lithography was carried out using a Vistec VB6-UHREWF, which has a maximum field size of 1.2 mm, minimum resolution of 0.5 nm and a minimum spot size of approximately 4 nm [50].

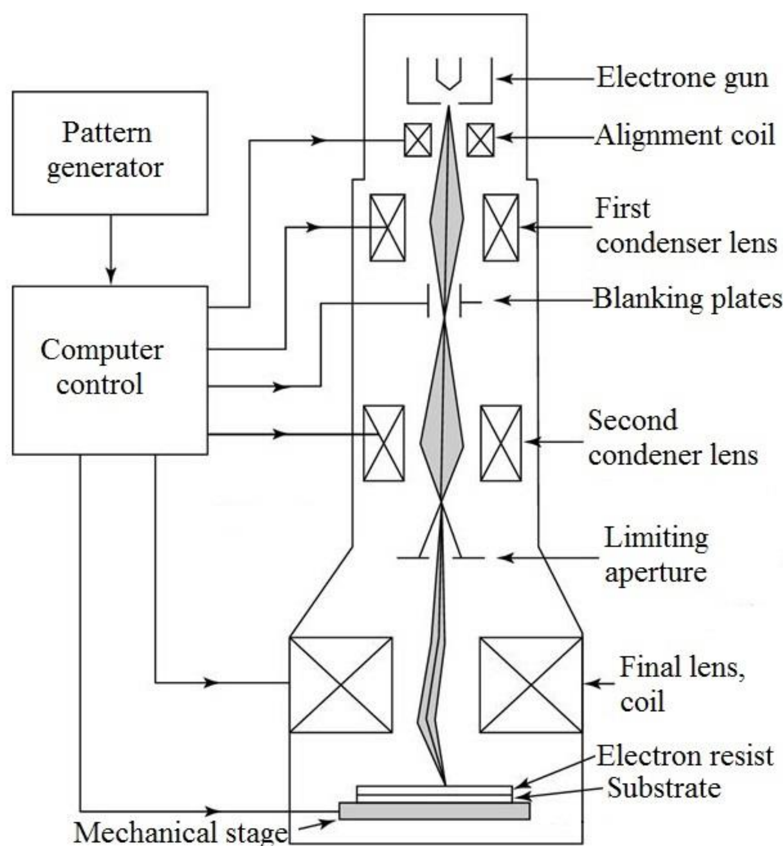


Figure 2.5: E-beam lithography system [51].

2.5.3 Pattern Definition

Standard approaches using CAD packages are widely used to transfer patterns to the e-beam tool. The large structures on the pattern were initially divided into smaller shapes that can be achieved by the pattern generator, as large patterns were written from conjoined small fields in the e-beam tool. This can be realised using the fracture process where large shapes are broken into trapezoidal sub-shapes. Figure 2.6 summarises the general fracture process from design to lithography. The GDS layout file, which was generated using CAD package, is fractured by using commercial fracturing tools, e.g. the CATS package from Synopsys. The fractured patterns are then exposed using a computer-controlled system at given positions related to substrate corners at specific exposure. Belle (Beam-writer Exposure for Lithography Engineers) software, which was developed at the University of Glasgow, was used to create these files. Further layers can be aligned relative to the first metallization layer to produce multi-level devices. In this case, several lithography levels could be written and accurately aligned based on scanning the edges of alignment markers with a specific size. [50].

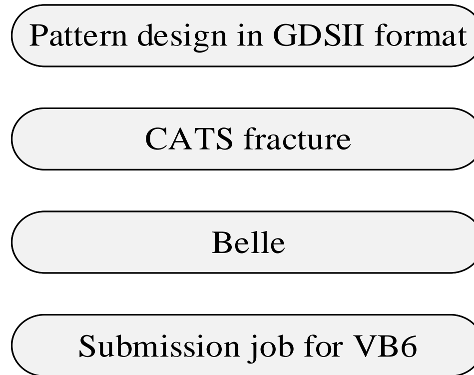


Figure 2.6: General data processing flow for e-beam submission job.

Polymers are used as e-beam resits for e-beam lithography. They behave in a similar way to those of photoresists where radiation can chemically or physically change the e-beam resist in order to pattern the resist. For positive tone e-beam resists, molecular fragments are generated by breaking the chemical bonds of resist exposed areas to electrons. This causes the exposed areas to be dissolved more quickly in the development process. On the other hand, irradiation can result in radiation-induced polymer linking when using negative tone e-beam resists, causing complexity in the three-dimensional structure. Hence, the exposed areas become harder to dissolve in the development solution.

The main benefit of the e-beam tool is that when using electrons instead of light to expose the radiation-sensitive resist, it overcomes the resolution restrictions by light diffraction. E-beam lithography resolution is limited by the minimum achievable beam spot size and the interactions of incident electrons with the resist and substrate during exposure [50].

Some advantages of using EBL include:

- Sub-micron features patterning
- Highly automated and precisely controlled operation
- Precise layer to layer alignment
- Fixable and no mask plate required as the designed patterns are directly transferred and written on the resit-coated sample
- Ease of editing layout design during the fabrication run

However, some disadvantages existed when comparing EBL to photolithography, including a long processing time and relatively higher operation costs and low throughput. In summary, photolithography is only preferred when a minimum feature size of 2 μm and alignment accuracy of 1 μm are required.

2.5.4 Mask Plate

The mask plate is needed for optical lithography pattern transfer. The GDS file pattern is initially generated in CAD package (L-Edit) prior to fracturing in CATS. Next, the fractured pattern is handled in BELL software using several given parameters, e.g. substrate size, dose and resolution, as described in Section 2.5.2. Having finished the CAD design and e-beam job submission, the mask plates are processed by the technical staff of JWNC where submitted pattern is written using e-beam tools. The mask plate substrate is quartz coated with chrome. The process starts by patterning the e-beam resist on the substrate which is used as a mask for the subsequent chemical wet etch process. The exposed areas of the chrome on the mask are then etched away using a chemical wet etch, prior to ashing, so that the original pattern is transferred into the chrome.

2.6 Dry Etch

As a result of the chemical stability of group III-Nitride semiconductors and the requirements of defining sub-microns trenches along with high alignment accuracy, dry etching (also called plasma-assisted etching) is considered the dominant etching technique in this project for both active and passive devices. Amongst all dry etching techniques, reactive ion etching (RIE) and inductively-coupled plasma reactive ion etching (ICP-RIE) have been commonly utilised in III-nitride materials etching process. This section is devoted to these dry etch process approaches.

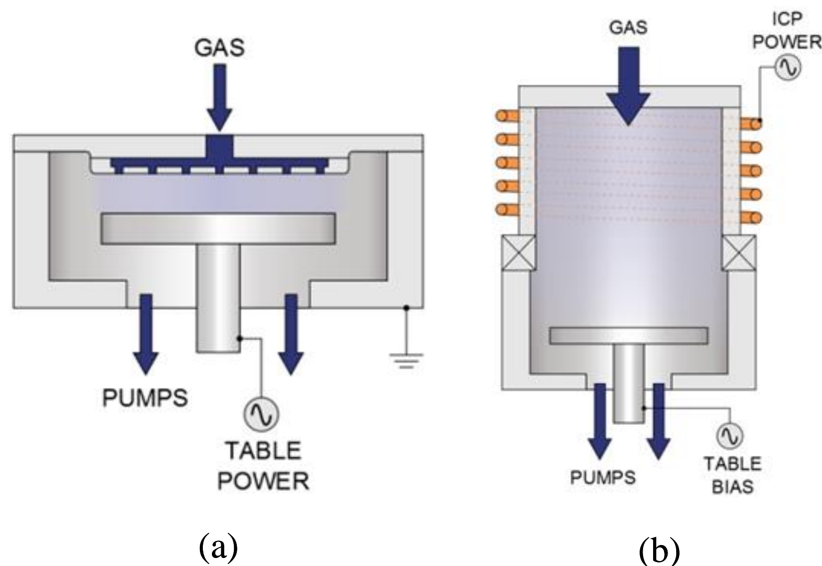
2.6.1 Reactive Ion Etching

In Reactive Ion Etching (RIE), anisotropic profiles, fast etch rates and dimensional control are realised by the use of both chemical and physical components of an etch mechanism. A typical RIE system is schematically indicated in Figure 2.7a [52]. An RF power at 13.56 MHz applied between two parallel electrodes in a reactive gas is optimally used to generate RIE plasmas.

The substrate to be etched is located on the powered electrode, where a voltage is applied and ion energies, which are ideally a few hundred electron-volts, are defined as they pass the plasma sheath. Because of the low pressures (ranging from a few mTorr up to 200 mTorr) required to operate the RIE, anisotropic etching profiles result the rise in mean free paths and reduction in collisional scattering of ions during acceleration in the sheath [53]. However, difficulties are encountered in the achievement of independent control of both physical and chemical components during the etching process in traditional RIE tools. This will noticeably affect the etch profile shape, in particular for III-Nitride materials, where breaking the bonds between their forming atoms needs relatively high ion energy. The RIE process was carried out in this project using an Oxford Instruments Plasmalab RIE 80 Plus and System 100 (T-gate).

2.6.2 Inductively-Coupled Plasma Reactive Ion Etching

A high-density plasma etch platform to pattern group III-Nitrides is obtained using high-density plasma etch systems. Inductively-Coupled Plasma Reactive Ion Etching (ICP-RIE) has improved etching characteristics for GaN-based devices [53]. The ICP-RIE system is schematically indicated in Figure 2.7b. ICP plasmas are generated in a dielectric vessel, which is encircled by an inductive coil into which RF power is applied. A strong alternating magnetic field is induced by the varying electric field between the coils. As a consequence, electrons are trapped in the centre of the chamber and a high density plasma is generated. Transformation of uniform density and energy distributions, while maintaining low ion and electron energy, can be obtained as a result of the effective decoupling between ion energy and plasma density. Therefore, low damage along with fast etch rates is produced using ICP-RIE etching. The PlasmaPro 100 Cobra ICP etch system from Oxford Instruments was used to perform ICP-RIE process in this project.



(a) (b)

Figure 2.7: Overview of (a) RIE etching. And (b) ICP-RIE etching [52].

2.7 Dielectric Deposition

MMIC fabrication process requires extensive use of thin films of dielectrics for various applications, including passivation layers for GaN-based HEMTs and insulator layers to form Metal-Insulator-Metal (MIM) capacitors [54]. Inductively-coupled plasma chemical vapour deposition (ICP-CVD), plasma enhanced chemical vapour deposition (PECVD) and atomic layer deposition (ALD) are among the deposition techniques used on GaN-based devices. In this work, ICP-CVD was chosen as a dielectric deposition technique for best device performance [55].

2.7.1 Inductively-Coupled Plasma Chemical Vapor Deposition

In this technology, inductively coupled plasma (ICP) is used as a source to deposit dielectric films by plasma-enhanced chemical vapour deposition. Dense films are deposited in conventional PECVD systems using high substrate temperatures of more than 200 ^{0}C. Similarly, such film densities deposited by PECVD could be also performed using the high density plasma of the ICP source at room temperature. An ICP-CVD system from Oxford Instruments is schematically indicated in Figure 2.8 [56]. The gas distribution line, which is situated above the wafer, is fed with reagents gasses, which is normally SiH_4 for both SiO_2 and Si_3N_4 deposition. Therefore, the system requires less cleaning as a result of the reduced

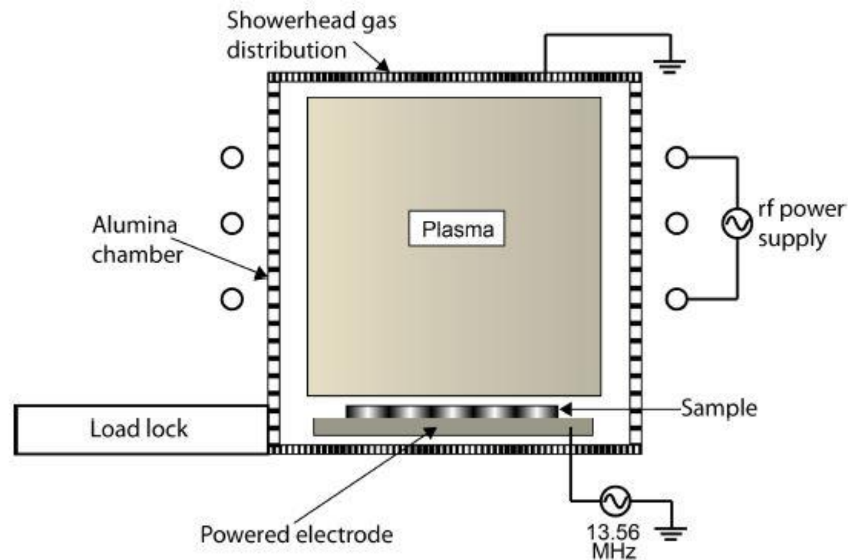


Figure 2.8: A Schematic of an ICP-CVD tool [57].

deposition in the source area. Next, using the top of the ICP source, the chamber is fed with inert gasses, which are usually O_2 and N_2 for SiO_2 and Si_3N_4, respectively. The use of high conductance chamber and vacuum system makes it possible for these gasses to flow at a relatively high rate along with low process pressures, ranging from to 1 to 10 mTorr. This is essential for sustaining high density plasma.

The advantages of using the ICP-CVD over PECVD can be summarised as flowing:

- Better deposition rate control (nearly 15 nm/min) of dielectric thickness along with good step convergence.
- Better control of the deposited films' stress, where several parameters, including process pressure, temperature, RF power and process gas ration can be adjusted.
- High-quality dielectric films' deposition as a result of the deposition at low pressure.
- Better uniformity.
- Possible film deposition on devices with high sensitivity to temperature.

However, despite the advantages offered by ICP-CVD, PECVD systems are much cheaper.

2.8 Metallisation and Lift-off

Having defined the pattern in the resist using the suitable lithography technique, the sample is now ready for metallisation for metal contact formation, such as alignment markers, source/drain contacts, and bond pads. This is a standard approach to cover the sample surface with metal selectively. In this work, Plassys MEB 450 and Plassys MEB 550 Electron beam evaporation tools were used for metallisation. These systems have several metal targets allowing the deposition of multi-layer stack of metals at a pressure in the order of 10^{-6} – 10^{-7} Torr using a vacuum chamber. A quartz crystal thickness monitor is utilised to accurately measure the deposited metal thickness. In electron beam evaporators, the metal target surface was initially heated up to reach the melting point temperature of the metal when the metal vaporises using electron beam. The metal atoms are then deposited on the sample. This allows the production of a non-conformal metal layer along with free sidewall coverage which facilitated the subsequent lift-off process.

In the metallisation fabrication step, a bilayer resist process was used to generate an overhang resist profile, as shown in Figure 2.9 [58]. Therefore, the deposited metal on the resist sidewalls was minimised, producing a discontinuity in the metal film. This facilitates the lift-off process allowing the resist-removal solvent to access the resist. Initially, the desired metal layer is deposited on the exposed, developed resist-coated bilayer resist. Next, samples are oxygen-ashed at a low power oxygen plasma etching. This is done to remove any organic resist residues, while the low power is crucial to avoid any possible damage to the exposed semiconductor material. Samples are then de-oxidised using Hydrochloric acid: RO water (4 HCl: H_2O) solution straight away prior to the metallisation process. This is to ensure the removal of any native oxide layer resulting from exposing the sample surface to air. The diluted acid solution is washed away using DI water. After metallization, samples are finally immersed in warm acetone for lift-off.

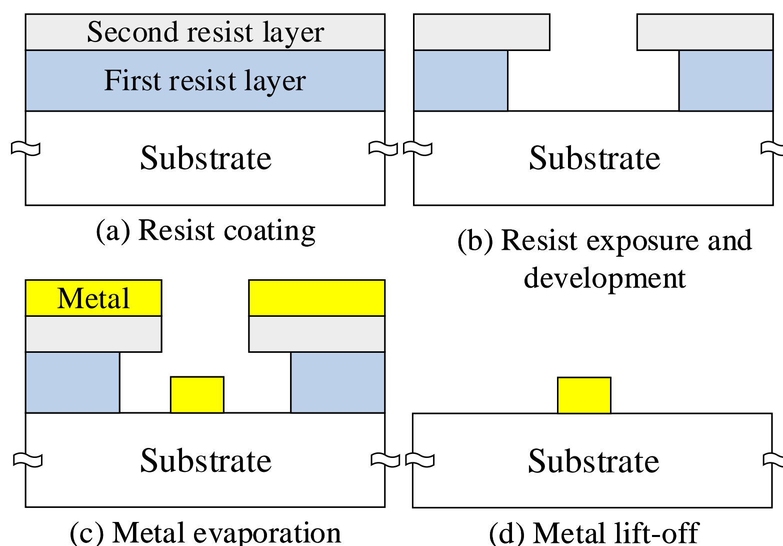


Figure 2.9: Illustration of metallisation and lift-off process using bilayer resit process.

2.9 GaN-based HEMT Process Flow

Definition of all levels of devices of GaN-based HEMTs was realised using e-beam for its flexibility and superior pattern definition capabilities. This section describes the major purposes and methods of each lithography step in turn. The order of the process is crucial for best device characteristics.

2.9.1 Alignment Markers

Because there are several lithography steps along with small feature sizes required for MMICs device fabrication at frequencies beyond X-band, accurate alignment markers are of a great importance for the realisation of high fabrication yield with reproducibility. In this project, the fabricated GaN-based HEMTs devices required the use of gate lengths of 0.27 µm which were accurately aligned in the centre of source-drain gaps of less than 2 µm.

The alignment markers were fabricated using e-beam lithography, metallisation and a lift off process, as described in Section 2.8. The lift-off process was achieved using bilayers of Poly-Methyl Methacrylate (PMMA) with different molecular weights; PMMA 2010 and PMMA 2041, which has a higher molecular weight [59]. A 12 % PMMA 2010 resist was initially coated on the cleaned surface of the wafer and then placed in the 180 ^{0}C oven for an hour. Next, the second layer of 4% PMMA 2041 resist was spun and baked at 180 ^{0}C in the oven for

two hours to ensure that all solvents had evaporated from the resit film. Having exposed the sample using the VB6, it was then developed in a mixture of a 4-methylpentan-2-one (methyl isobutyl ketone or MIBK, $C_6H_{12}O$) and IPA solution (2.5 MIBK: IPA) for 60 seconds at 23 ^{0}C prior to IPA cleaning for 30 seconds. The exposed areas were then ashed and de-oxidized prior to the metallization. Finally, Ti/Pt (10/100 nm) metal stack was deposited using an electron beam evaporator and lifted-off. The Ti/Pt markers were purposely chosen to withstand annealing to beyond 800 ^{0}C (required for ohmic contacts realisation) but to still retain the necessary surface morphology and edge acuity required for subsequent registration in the e-beam tool.

2.9.2 Ohmic Contacts

Multiple-finger design, developed at the University of Glasgow, was used for the layout of the fabricated devices [58]. The design consisted of two gates connected at one side, centred drain patch and two separate sources. Both gate fingers shared one drain and were located between the source and drain pads. The source-drain gap needs to be well-controlled as it has a significant influence on device performance.

Lithography challenges are involved during the pattern transfer process of the three large contacts, which were located at a considerable small separation as a consequence of the proximately effect. This is because of the possible overexposed resist in the middle regions of the contacts. Consequently, the source-drain gap was reduced because of the exiting of variable electrical fields along the gate width. Figure 2.10 shows an optical microscope image of the required layout using proximity corrections. Proximity effect arises from the fact that the middle areas of the ohmic contacts are more likely to be overexposed when compared to the corner regions [50]. Having defined the source and drain areas using VB6 (as described in Section 2.9.1), the wafer was then washed and cleaned in HCL: H_2O (4:1) solution for de-oxidisation. Next, argon gun treatment was performed inside the evaporator chamber under vacuum prior to the electron beam evaporation of Ti/Al/Mo/Au (15/60/35/50 nm) metal-stack using Plassys MEB 550. The wafer is then lifted-off using the method described in Section 2.8.1. The argon gun treatment helped to remove the thin native oxide layer caused by exposing the wafer to air and to etch the top GaN cap layer. Consequently, the ohmic contact resistance could be reduced. Finally, the wafer was subsequently alloyed at 800 °C for 30 s in nitrogen (N_2) ambient. The contact resistance was extracted using transmission line model (TLM)

technique which requires simple I-V measurements of standard ohmic structures using four-probe measurements [60]. The probes and cables resistances are eliminated by applying the voltage through one pair, while the current is measured by the second pair. The standard gap lengths used in this work are 1.5 – 5.5 µm with a step of 1 µm.

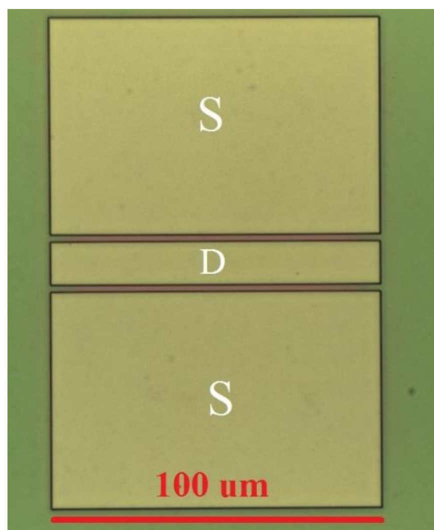


Figure 2.10: Ohmic contact patterns after development for a two-finger device using bilayer PMMA.

2.9.3 Mesa Isolation

Mesa isolation is the process of isolating the individual devices electrically from each other. This can be done by etching away the top active layers down to the semi-insulation buffer layer, which is typically 150-200 nm etch depth [61]. Device isolation can be alternatively realised using ion implantation in order to damage the 2-DEG conductivity [62]. This technique introduces major advantages, including wafer planarity and conformal metal coverage and mesa-sidewall gate leakage elimination. However, because it was not possible to use the implantation equipment, mesa isolation was performed by plasma etch tools for GaN-based HEMTs fabrication thought this project.

Mesa isolation fabrication steps started with the sample cleaning as discussed in Section 2.4, followed by spinning 15 % PMMA 2010 resist and e-beam exposure for islands where mesa was required for active devices. After development of the isolation level, wafers were post-baked at 120 ^{0}C for 10 minutes in order to drive away any residual solvent and to enhance adhesion of the resist. This step prevented the removal of the resist mask during the subsequent

dry etching process. A final resit thickness of approximately 1.1 µm was obtained. Device isolation was achieved with low damage ICP-RIE etching using PlasmaPro 100 Cobra ICP etch system. The gases used were Cl_2 and Ar at flow rate of 30 sccm and 15 sccm, respectively. During this process, an RIE/ICP power of 750/75 W and a pressure of 4 mTorr were used at room temperature. This resulted in an etching rate of approximately 3.2 nm/sec with an anisotropic etching profile. Advantages of such isolation mesa formed by this dry etch process include the overcoming of any possible discontinuities in the gate metal and mesa side walls, which would be covered by Si_3N_4 dielectric layer during device passivation. Consequently, the gate leakage currents and breakdown voltages can be improved [61] [63]. The remaining resist mask was finally removed using warm acetone. Figure 2.11 summarises the mesa isolation process.

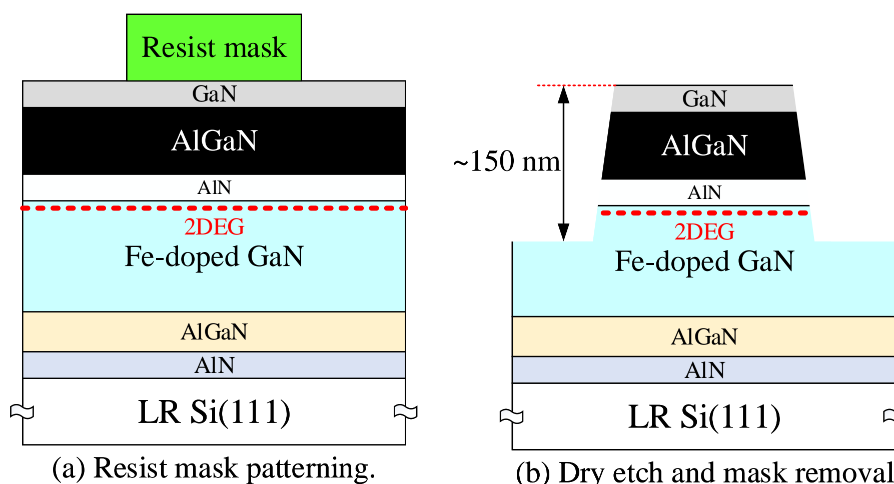


Figure 2.11: Mesa isolation process.

2.9.4 Passivation

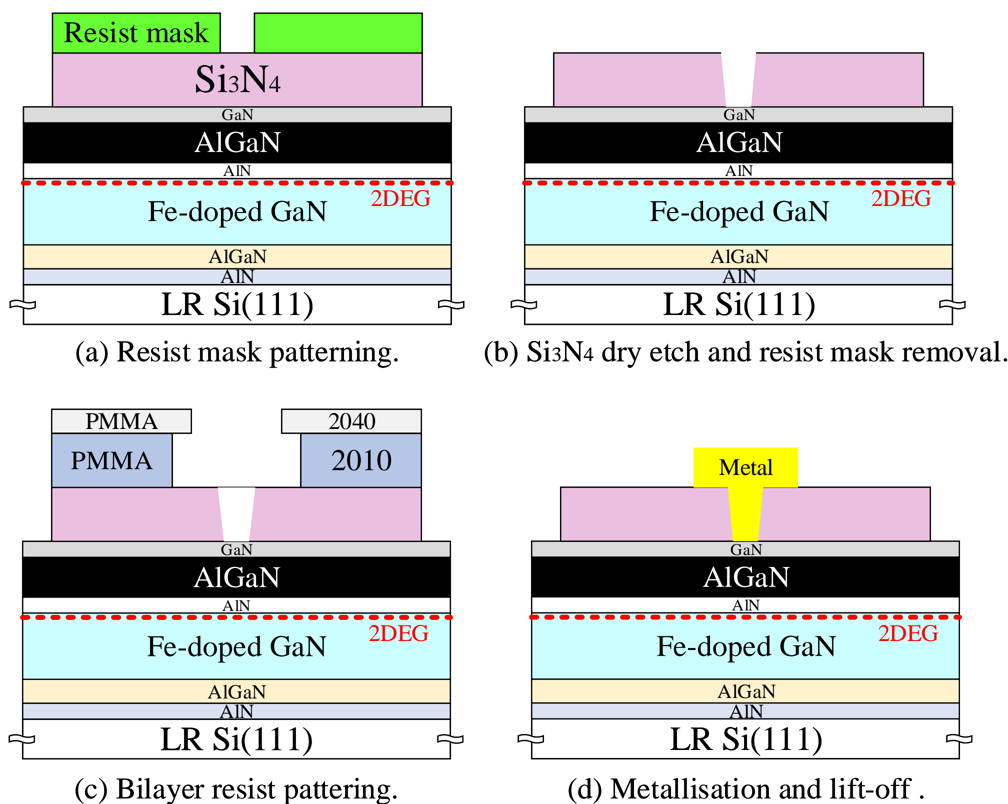
The performance of GaN-based HEMTs is limited by the trapping effects through drain-source collapse, resulting from the stress-induced polarisation effect on the GaN HEMTs. Much more attention has been focused on the reduction of surface states using different passivation dielectrics [54] [64]. The surface trapping effect is dramatically reduced when using ICP-CVD Si_3N_4 passivation technique, which provides better DC and RF device performance when compared to PECVD passivation [65]. In this work, device passivation was performed by depositing a blank 200 nm Si_3N_4 by ICP-CVD at room temperature on the whole wafer. This required the use of an accurate deposition process along with slow deposition rate in order to

achieve high homogeneity of the deposited layer, which is crucial for the following T-shaped gate fabrication process.

2.9.5 Gates

Because of the small feature size, complex geometry and high accurate alignment requirements of the fabrication process of the gates, they are considered to be the most crucial step in HEMTs fabrication. Controlled formation of stable Schottky contacts with sufficient high barrier and low leakage current are critical factors for the realisation of GaN-based HEMTs. In this work, Ni/Au (20/200 nm) metal layer was deposited for the gates because of their high barrier height and good thermal stability. In addition, T-gate (which enables the realisation of large cross-sectional area while reducing the gate foot print) was used to reduce gate resistance, R_g, and hence improve device performance.

T-gates in this work were fabricated by two EBL steps. First, the gate foot was aligned between the source and drain contact and then transferred into the Si_3N_4 using a low bias and a low damage plasma etch, to minimise damaging the exposed GaN surface. This was achieved by spinning and developing a 8% PMMA 2010 resist, which was used as a mask for the subsequent dry etch process. A corresponding mask thickness of approximately 375 nm was achieved. Next, the gate-foot trenches were opened in the Si_3N_4 layer using the Oxford Instruments Plasmalab System 100 RIE (T-gate). During this process, an RF power of as low as 18 watts and a pressure of 15 mTorr, and SF_6/N_2 gases with a flow rate of 25/50 sccm were used. An etch rate of approximately 15-17 nm/minutes along with an anisotropic etching profile were obtained. In addition, to ensure a successful complete removal of the Si_3N_4 in the gate-foot trenches, end point detection using an interferometer was used during etching [61]. Having etched the gate-foot trenches, the gates were formed by spinning a bilayer of 8 % PMMA 2010 and 4 % PMMA 2041, followed by the metallisation and lift off process method of a Ni/Au (20/200 nm), as described in Section 2.8. Figure 2.12 summarises the T-gate fabrication process.



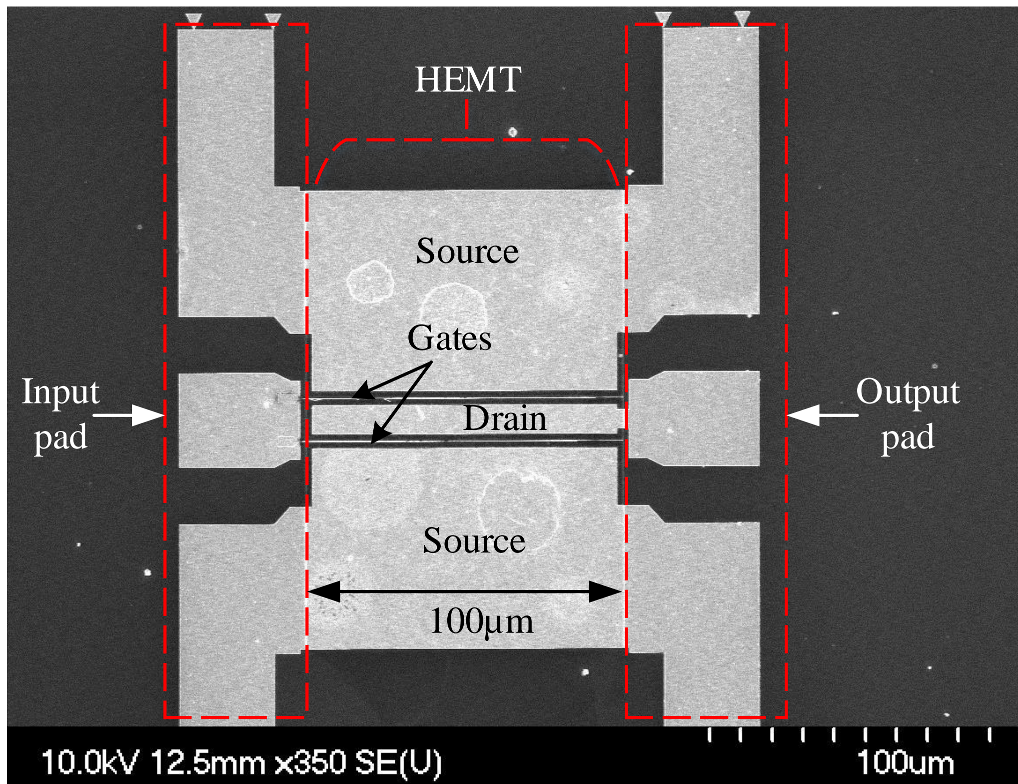
(a) Resist mask patterning. (b) Si_3N_4 dry etch and resist mask removal.

(c) Bilayer resist pattering. (d) Metallisation and lift-off .

Figure 2.12: T-gate fabrication process.

2.9.6 Contact Pads

Contact pads are needed to connect the fabricated HEMT devices to the outside world for DC and RF device characterisation. The pads are designed as CPW, where a ground-signal-ground topology is utilised to ensure RF signal integrity. The characteristic impedance of the line is matched to that of the measurement system (50 Ω) by adjusting its signal-line width and signal-ground separation [66]. However, since contact pads add extra capacitances to the HEMT devices at microwave frequencies, contacts significantly influence device performance. In this work, the layout of the input and output feeds were designed to accommodate a minimum RF probe tip pitch of 50 µm and RF probing required for skating distances. A minimum skating distance of 25 µm is defined as a role of thumb. Fabrication of contact pads was realised using two steps. Initially, windows in the Si_3N_4 at the Ohmic contact areas were etched, whilst the other areas were kept entirely passivated (to avoid any GaN-exposed surface) using the dry etch process described in Section 2.9.5. Next, a NiCr/Au (50/450 nm) metal stack was deposited and lifted-off using the method described in Section 2.9.1. Contact pads definition completed the standard HEMT process flow. The general completed device layout of a standard two-finger device is shown on Figure 2.13.



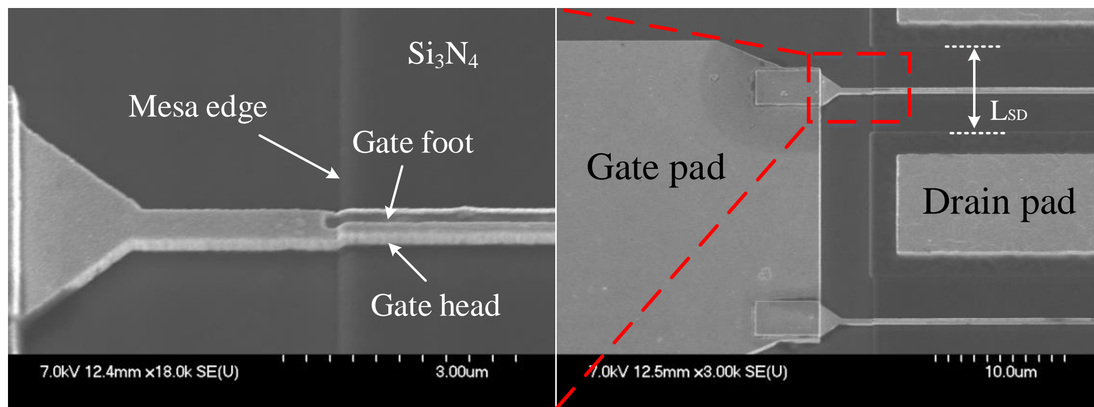


Figure 2.13: Top-view SEM images of the fabricated 2×100 µm wide T-gate GaN-based HEMT of LR Silicon substrate.

2.10 Passive Devices Fabrication Process

Low-loss waveguides, capacitors and inductors with high quality-factor at mm-wave frequencies are of great importance for circuit application where interconnects and passive components are needed. Therefore, low-loss transmission media are required for cost-effective GaN-based MMIC technology. In this work, newly-developed transmission media technology were performed on a GaN-based material structure that could be used to realize AlGaN/GaN HEMTs on LR Si substrate (details of material structure are described in Section 2.2).

Optical lithography was used for all levels of device definition and all steps required to realize the proposed transmission media technology were compatible with standard MMICs technology. The transistor active region (the upper two layers) was etched away prior to transmission media fabrication. As in a standard MMIC process, the passive devices were fabricated on the isolation mesa floor on top of a 200 nm Si_3N_4 dielectric layer. Two types of transmission media technology were realised to supress substrate coupling caused by the conducting of the Si substrate: shielded and shielded-elevated transmission lines. Fabrication process details of the proposed transmission media technology will be introduced in the following sections.

2.10.1 Shielded Transmission Media Technology

Fabrication process of the newly-developed shielded transmission media technology in this work requires several lithography steps:

(a) Markers and Ground Planes

Markers and ground planes were formed by metallisation and a lift-off of Ti/Au (50/600 nm) metal stack, described in Section 2.8. A bilayer lift-off technique utilises a coating of Lift-Off Resist (LOR), which is not photo-sensitive but is highly soluble in conventional aqueous TMAH developer. The optical lithography fabrication technique started by coating LOR 10A onto the cleaned surface of the sample, followed by the photoresist coating. Shipley S1805, which is a positive photoresist, was chosen as an image resist. The LOR 10A and S1805 were pre-baked on a hot plate at 170 ^{0}C and then at 115 ^{0}C for 2 minutes prior to UV pattern

exposure. After imaging, the photoresist and LOR are simultaneously developed in MF-319 developer. The degree of LOR undercut can be easily controlled using a range of parameters in the development process, namely developing time and wafer agitation speed in the developer. In this process, an undercut depth and LOR etch rate of approximately 1 µm and 13 nm/sec were obtained, respectively. Finally, the sample was ashed and de-oxidised prior to the e-beam evaporation of Ti/Au metallisation using Plassys tools. A summary of the process flow is indicated in Figure 2.14.

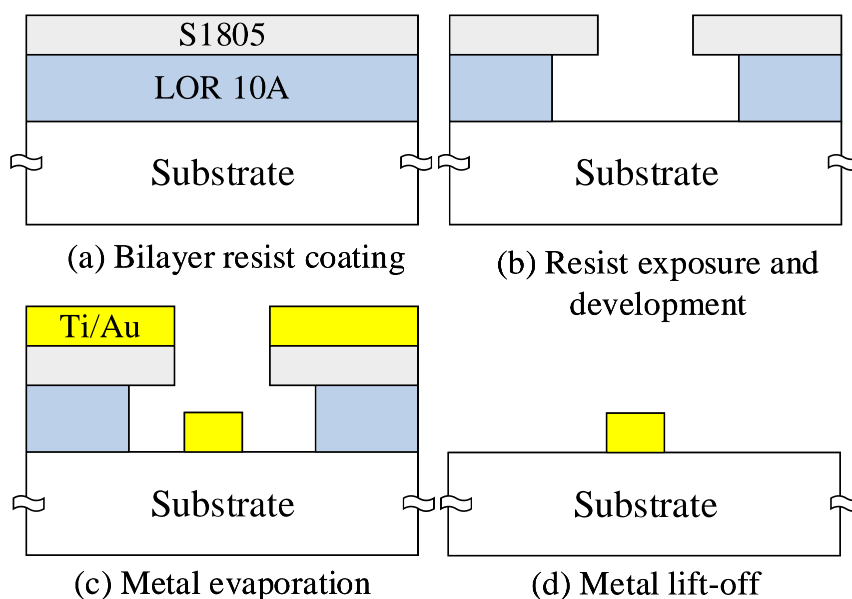


Figure 2.14: Dual-layer lift-off technique using LOR 10/ S1805 resists.

(b) BCB Dielectric Deposition

Benzocyclobutene (BCB) is an interesting thermoset polymer largely considered for high performance electronic integrated circuits (within Si and III/V technologies) and optical applications because of its low dielectric permittivity ε_r (2.65), a small dielectric loss tangent ($\tan\delta < 0.02$ below a terahertz), low optical absorption at telecommunication wavelengths, good charge stability and excellent thermal resistance [38]. With regards to the fabrication process, BCB has a good compatibility with a range of metals. Moreover, BCB is fully compatible with standard semiconductor techniques. The deposit procedure consists of spin coating, and the curing requires a relatively low temperature (250 ^{0}C). This has the advantage of accommodating active circuits underneath the passive components and interconnectors with

no degradation of active device performance [67]. Additionally, spin coating allows a greater control of the layer thickness and subsequent curing for network formation.

The dry etch BCB (CYCLOTENE 3022-57 from DOW Chemicals) was used throughout this work. The adhesion promotor (AP3000) was initially applied on the cleaned surface of the sample prior to BCB application to enhance the adhesion to substrate surface. Next, the BCB was spun-coated onto two steps to insure good uniformity of the BCB surface. The BCB was initially spun at low spin speed (500 rpm) for a short time (5 sec) prior to the final spin speed which determined the final desired BCB thickness. After the spin coating process, the BCB film was baked at 130 ^{0}C on a hotplate for 60 seconds to remove solvents and to “stabilize” the film in order to avoid material flow during subsequent handling and curing. Finally, the BCB was fully cured at 250 ^{0}C for 5 hours in N_2 atmosphere to achieve its final properties. It is crucial that the BCB films are kept in the environment with oxygen content of less than 100 ppm during the curing process. This is because the BCB films at temperatures above 200 ^{0}C and in the presence of oxygen oxidise. The dependency of the film thickness on final spin speed is shown in Figure 2.15.

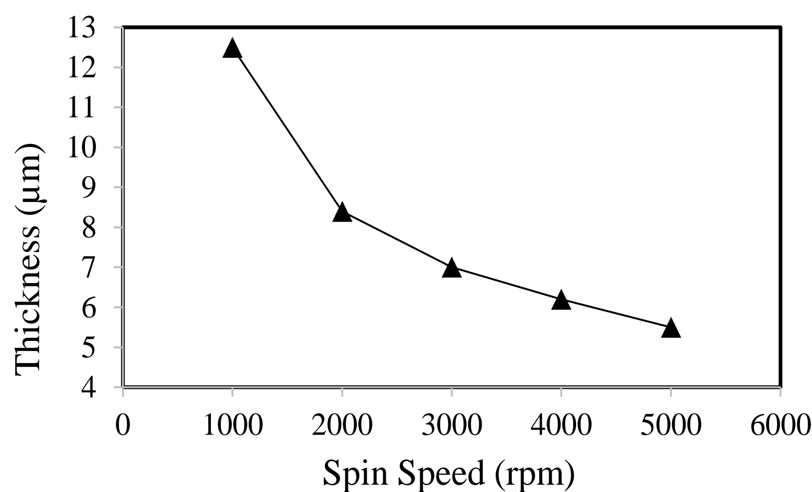


Figure 2.15: Final thickness of cured BCB versus spin speed.

(c) Soft mask Process

A through-hole (via-hole) is required through the BCB to enable the connection of passive devices patches to the ground planes. In this process, the photoresist was employed for through hole pattern definition which also used a sacrificial mask for the subsequent dry etch process.

Since the etch rate for BCB and photoresist films was similar, the resist thickness should be greater than the BCB thickness. Compatibility of the resist stripper with BCB was also considered. The sample was initially coated with AZ4562 photoresist at 2000 rpm for 30 seconds, followed by baking at 90 ^{0}C for one hour to evaporate solvents. After exposure, the resist was then developed in AZ 400K: H_2O (1:4) for three minutes. This provided a resist thickness of around 9.5 µm. The sample was finally ashed and de-oxidized, as described in Section 2.8. The sample was now ready for dry etch process.

(d) Through Opening Process

The through opening process was required through the BCB to connect the ground plane to the line tracks located on top of the BCB. Therefore, anisotropic etching profile was needed. This fabrication process is critical as any misalignment or under etching of the BCB will result in device failure. RIE dry etching is widely used to etch BCB. The plasma used to etch

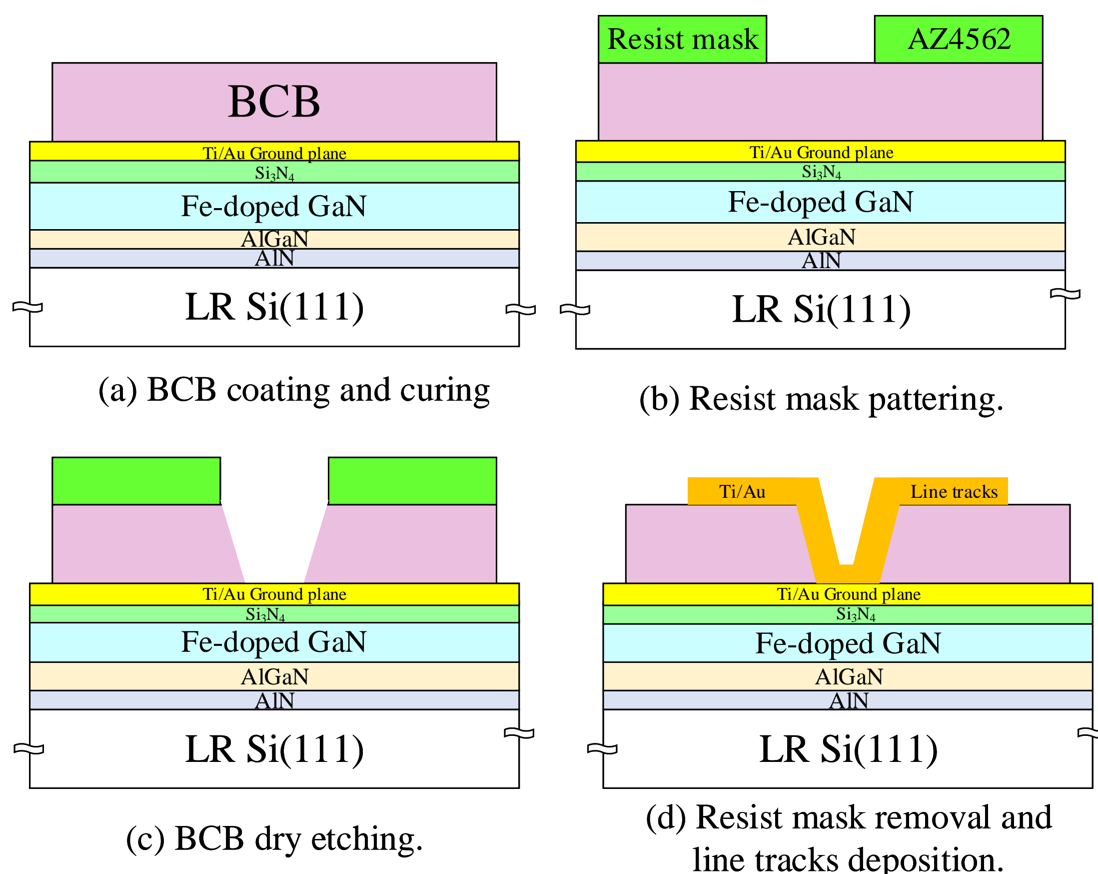


Figure 2.16: Fabrication process of BCB via opening.

dry-etch BCB films generally requires both oxygen and fluorine species as silicon is present in the backbone of the polymer [68]. In this work, a mixture of oxygen (O_2) and fluorine-containing gas (CF_4) produced a controlled etch rate and profile along with a smooth surface using Plasmalab 80 Plus RIE dry etch tool. Gases flow rate, power and pressure of O_2/CF_4 = 20/5 sccm, 200 W and 55 mTorr were used, respectively at room temperature. To ensure a successful complete removal of the BCB down to the ground plane, end point detection technique using interferometer was used during etching [69]. An etch rate of approximately 458 nm/mins with anisotropic etching profile and damage free through the side walls was obtained. Finally, the AZ4562 mask was removed prior to patterning the line tracks using a standard lift-off process with a Ti/Au (50/600 nm) metal stack, as described in part (a) of this Section. A summary of the fabrication process flow is shown in Figure 2.16. A complete view of the fabricated shielded transmission media technology is shown in Figure 2.17.

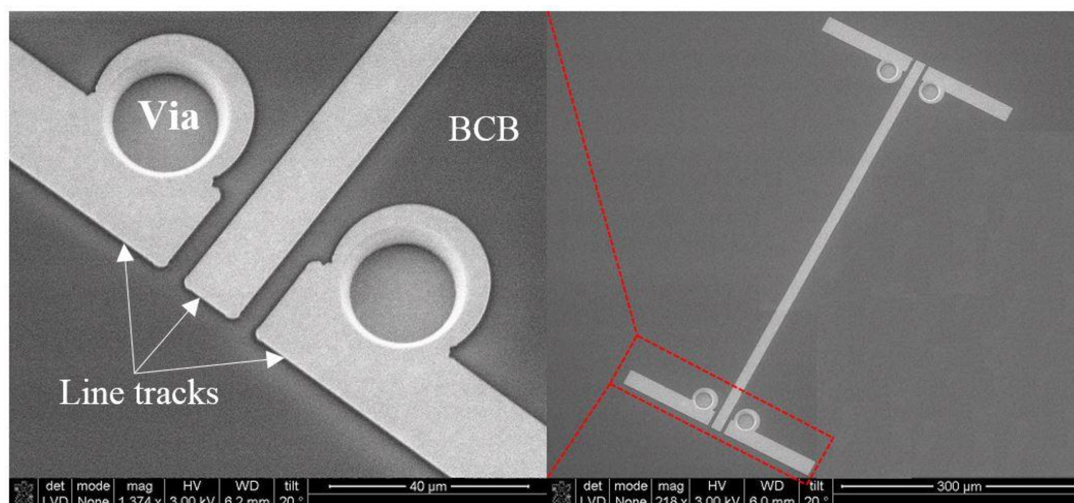


Figure 2.17: SEM images of the fabricated shielded-microstrip technology.

2.10.2 Shielded-Elevated Transmission Media Technology

Shielded-elevated transmission lines were fabricated in a similar way to the transmission media technology described in Section 2.10.1 - where 5 µm-BCB were initially spun and cured prior to the definition of markers and ground planes levels. Next, air-bridge technology was employed to form the elevated line tracks structures. Therefore, in this technology, opening through the BCB was not required as the ground plane was situated on top of the BCB. This made the fabrication process of this technology less complicated compared to that of shielded transmission media technology.

Air-bridge Technology

The air-bridge process was performed in two steps. First, the air-bridge supports are defined in a AZ4562 photoresist which was spun at 4000 rpm for 30 sec. Following this, the sample was baked at 90 ^{0}C for 30 minutes prior to exposure and development. The total thickness of the resist was approximately 6.2 µm, which determines the height of the air-bridges. Therefore, air-bridge height can be simply controlled by varying the spin speed of the AZ4562 resist. A hard bake of 10 minutes at 120 ^{0}C was then required to evaporate any remaining solvents, and make the resit hard enough for the subsequent metallisation process. Next, the sample was ashed and de-oxidised prior to the deposition of Ti/Au (50/ 50 nm) seed layer using e-beam evaporation. The Ti layer provided adhesion for the air-bridge contact, whereas the 50 nm Au layer prevented the Ti layer from oxidising. Next, the air-bridge tracks were defined in 2.8 µm thick Shipley S1828 photoresist followed by electroplating 2µm of gold onto the seed layer. The gold plating solution was maintained at 50˚C during plating. The plating current was set by the equation [58].

$$\text{Plating Current (mA)} = (\text{sample holder area - sample area})\ \text{mm}^2 \times 0.013 \qquad (2.1)$$

The top layer of photoresist was removed by a flood exposure and development. The seed layer was then removed by etching the top gold layer in KI/I_2 for 20 seconds, followed by etching the Ti layer in 10:1 buffered HF for 30 seconds. Finally, the bottom AZ4562 resit was removed using warm acetone. Figure 2.18 indicates a complete view of the fabricated devices using air-bridge technology.

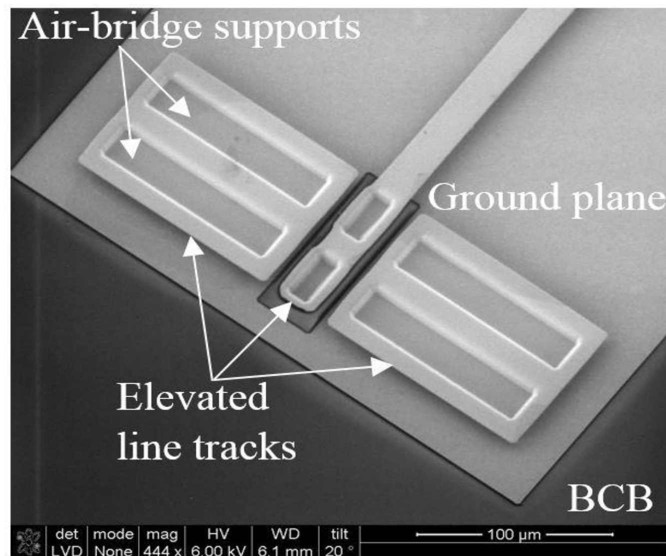


Figure 2.18: SEM images of the fabricated shielded-elevated transmission media technology.

2.11 Conclusion

This chapter has covered the fabrication techniques required for the realisation of RF GaN-based HEMTs technology on LR Si substrates. The fabrication process of the developed passive and active devices is reliable and compatible with standard III-V MMIC technology. The developed technology in this work is not only suitable for LR Si substrates, but can also be used on other SI substrates, such as SiC, Sapphire and HR Si, for mm-wave circuits applications.

Having introduced the device fabrication, the performance of the implemented active and passive devices is presented in the following chapters.

Chapter 3

AlGaN/GaN HEMTs on Low Resistivity Si Substrates

3.1 Introduction

AlGaN/GaN HEMTs grown on LR Si continue to be the focus of interest for high power and high frequency applications; also they have potential for higher level of integration, e.g. in sensor applications. This is because of the inherent advantages that can be offered by such devices, including large wafer size, low cost (compared to Si-LDMOS, GaAs-based devices and GaN-on-SiC/diamond [70]) and the ease of removing the Si substrate under the active and passive devices. This has potentially made GaN-based HEMTs on LR Si substrates an alternative candidate to those grown on SI substrates, such as SiC and Sapphire. However, other challenges need to be overcome such as high mm-wave signal loss, low Q-factor passives and epitaxial buffer growth [71] [72]. The challenges associated with mm-wave signal loss and passive structures have been addressed in this work with viable solutions to realise RF GaN-on-LR Si MMIC technology.

This part of the thesis is devoted to the development of high-performance AlGaN/GaN HEMTs on LR Si technology for RF MMIC circuit applications. A brief description of the HEMT operation is first outlined, followed by a discussion on device parameters that critically affect the DC and RF characteristics. Then, the proposed fabrication process technology of AlGaN/GaN HEMTs on LR Si is presented. Devices with different epitaxial layer structures and design layouts were investigated for possible performance enhancement. Next, a study on the effect of inserting an AlN interlayer on both DC and RF device performance was conducted. Following, the influence of the thickness of the top AlGaN Schottky barrier (27 nm and 9 nm) was studied in the presence of an AlN spacer. Finally, the DC and RF performance of devices with varying source-drain distances (L_{SD}) was investigated. The RF results were analysed using the small-signal equivalent circuit model to extract device parasitic elements.

3.2 Operation of HEMT

The basic operation of a HEMT is similar to that of the Metal-Semiconductor Field Effect Transistor (MESFET). A schematic view of basic AlGaN/GaN HEMT is shown in Figure 3.1. The source, drain and gate contacts are placed directly on the top AlGaN barrier layer. Both drain and source terminals are ohmic contacts, where the contact to the two-Dimensional Electron Gas (2DEG) is obtained by thermal annealing. A metal-semiconductor rectifying contact (Schottky barrier contact) is associated to the gate terminal.

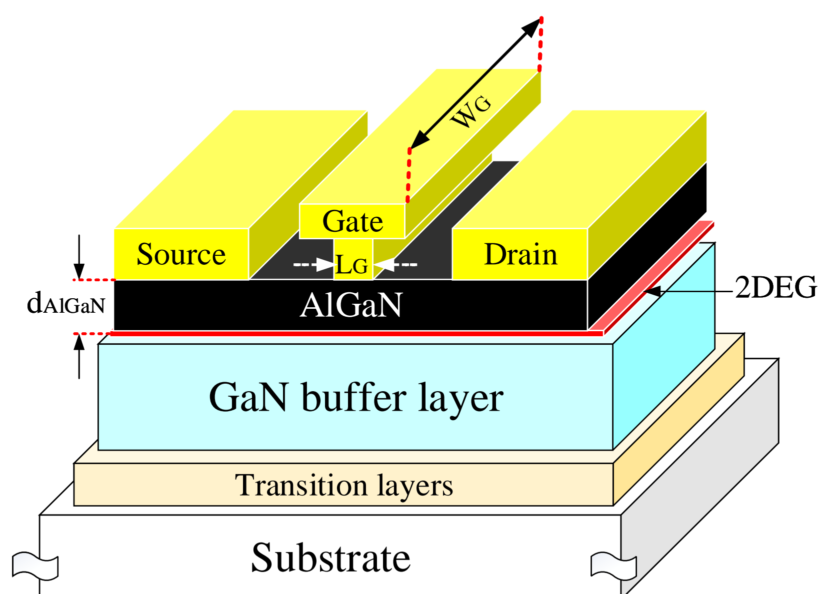


Figure 3.1: Schematic draw of general AlGaN/GaN HEMT structure.

The voltage applied to the gate contact causes a variation in the space charge, which in turn regulates the current flow between the source and drain (I_{DS}) through the two-Dimensional Electron Gas (2DEG). Device performance and the transport of electrons along the interface are strongly affected by the 2DEG quality, which, in particular, depends on the epitaxial layer structure and growing approach. Interface, alloy and dislocation scattering mainly affect the mobility of the 2DEG. Equation 3.1 indicates the current flow across the channel and between the source and drain terminals [73]:

$$I_{DS} = qn_s v_{\mathrm{eff}} W_{\mathrm{G}} \tag{3.1}$$

where v_{eff} is the effective velocity of the electrons in the channel, n_{s} is the charge density of the 2DEG and W_{G} is the width of the device. The electron mobility (μ_{n}) and the applied electric field (E) determine the electron velocity, as indicated in Equation 3.2 [74].

$$v = \mu_{\mathrm{n}} E \tag{3.2}$$

Considering the gate metal and the 2DEG channel as a capacitor, the sheet carrier density is a function of the dielectric constant of the AlGaN Schottky barrier layer ($\epsilon_{\mathrm{AlGaN}}$), the thickness of the AlGaN Schottky barrier layer (d_{AlGaN}), the effective distance between the 2DEG and the hetero-interface (Δd), the gate bias (V_{GS}) and the threshold voltage (V_{T}), which is the gate bias voltage required to pinch-off the 2DEG channel, as follows [73]:

$$n_s = \frac{\epsilon_{\mathrm{AlGaN}}}{q(d_{\mathrm{AlGaN}} + \Delta d)} (V_{\mathrm{GS}} - V_{\mathrm{T}}) \tag{3.3}$$

The expression $\epsilon_{\mathrm{AlGaN}}/(d_{\mathrm{AlGaN}} + \Delta d)$ refers to the gate to channel capacitance [75].

Figure 3.2 shows a typical DC behaviour of a HEMT. The linear regime operation can be defined as the region where the electron velocity is proportional linear to the applied electrical field. Therefore, at low fields, $V_{\mathrm{DS}} < (V_{\mathrm{GS}} - V_{\mathrm{T}})$, I_{DS} increases linearly. However, saturation in the electron velocity occurs as the applied field increases, $V_{\mathrm{DS}} > (V_{\mathrm{GS}} - V_{\mathrm{T}})$. This operation region is called a saturation regime, where $v_{\mathrm{eff}} = v_{\mathrm{sat}}$ at which I_{DS} cannot be further increased by increasing V_{DS} [76]. Degradation in the maximum drain current is observed when applying higher drain voltage and positive gate voltage, resulting in a negative output transconductance. This attributes to the current collapse connected with the thermal effect and traps charging and discharging in the material.

3.3 Summary of Important HEMTs Parameters

The voltage gain (A_{V}), which has a direct relationship to the power gain for a HEMT is an important figure of merit value and can be written as:

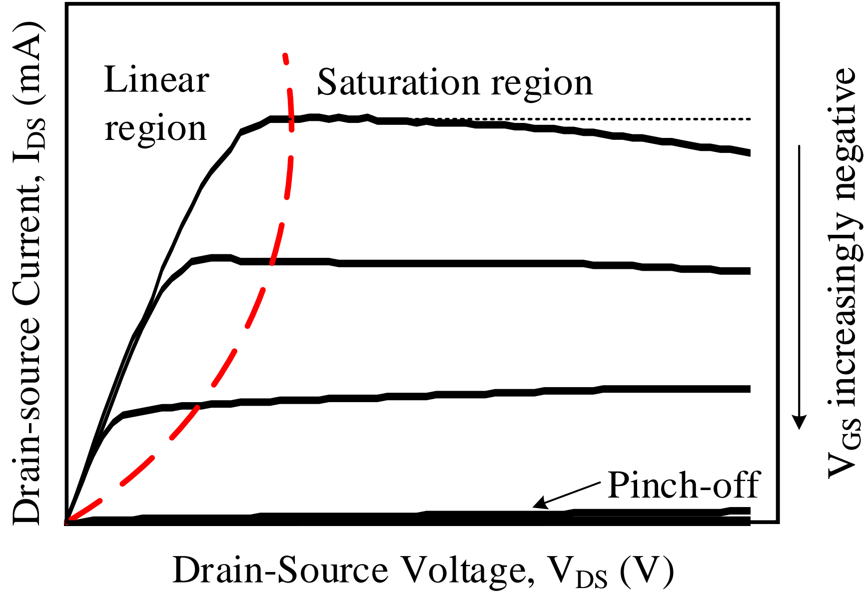


Figure 3.2: Typical output characteristics for AlGaN/GaN HEMT.

$$A_v = \frac{\delta V_{\mathrm{DS}}}{\delta V_{\mathrm{GS}}} = \frac{g_{\mathrm{m}}}{g_{\mathrm{d}}} \tag{3.4}$$

where, g_{m} is the transconductance and g_{d} is output conductance. g_{m} is defined as the modulation of the channel current (I_{DS}) by the gate voltage (V_{GS}) at a constant drain voltage (V_{DS}), and can be written as:

$$g_{\mathrm{m}} = \frac{\delta I_{\mathrm{DS}}}{\delta V_{\mathrm{GS}}} \tag{3.5}$$

At the saturation regime, g_{m} can be estimated as:

$$g_{\mathrm{m}} = \frac{\epsilon_{\mathrm{AlGaN}}\, v_{\mathrm{sat}}\, W_{\mathrm{G}}}{(d_{\mathrm{AlGaN}} + \Delta d)} \tag{3.6}$$

Therefore, according to Equation 3.6, higher saturation velocity and shallow depletion region (smaller AlGaN barrier thickness) are essential for obtaining higher g_{m}. Since the depletion region mainly depends on the applied gate voltage (V_{GS}) and the gate length (L_{G}), g_{m} is expected to increase with negatively increased V_{GS} and smaller gate lengths (L_{G}) [58]. Downscaling of the gate length is limited to the thickness of AlGaN barrier, something called “the short channel effects (SCEs)”. These effects have been effectively eliminated by

maintaining an aspect ratio (L_G/d_{AlGaN}) of as high as 15 [77]. Lower AlGaN barrier thickness results in an increase to the parasitic part of the gate capacitance, and can lead to degradation in RF performance, as indicated in the Equation 3.7:

$$C_g = \frac{\epsilon_{AlGaN} L_G W_G}{d_{AlGaN}} \tag{3.7}$$

The output transconductance (g_d) is the slope of the I_{DS}-V_{DS} plot (indicated in Figure 3.2) at a fixed gate voltage (V_{GS}), and can be written as follows:

$$g_d = \frac{\delta I_{DS}}{\delta V_{DS}} \tag{3.8}$$

Deterioration in the output transconductance is observed for transistors with an aspect ratio of below 15 [77]. Therefore, SCEs need to be mitigated for successful development of mm-wave technology.

3.4 HEMT RF Behaviour

The small-signal characteristics of the HEMTs are normally evaluated based on the measurement of scattering-parameters (*S*-parameters) at the input and output terminals. Assuming the HEMT is operated in the common source mode, the input port corresponds to the gate-source, whereas the output terminal corresponds to the drain-source. The *S*-parameters of two-port network are shown in Figure 3.3.

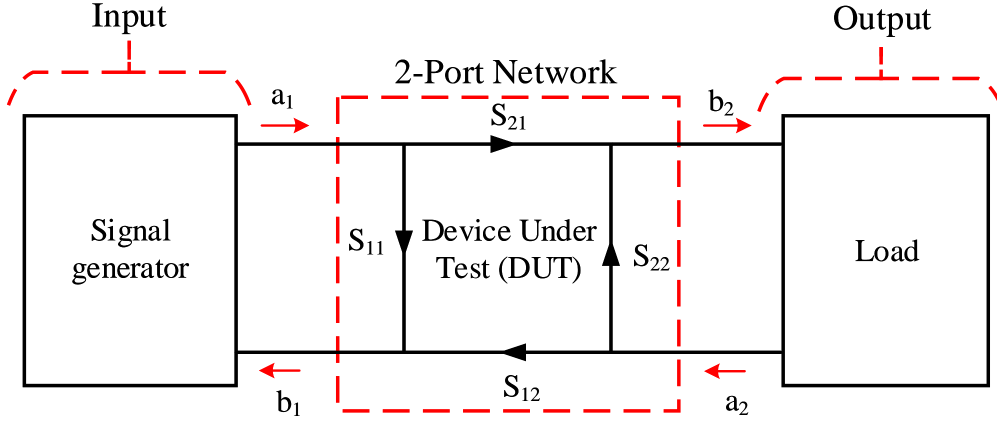


Figure 3.3: Schematic diagram of the two-port concept used for device characterisation.

Equation 3.9 shows the relationship between the input and output power waves of the two-port component.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.9}$$

where S_{11} and S_{22} indicate the reflection coefficients. S_{12} and S_{21} indicate the transmission coefficients. *S*-parameters are usually measured over a wide frequency range in order to be able to fully characterise the devices. Several figures of merit can be calculated based on the measured S-parameters:

- **Current Gain Cut-off Frequency f_T**

The frequency at which the current gain $\frac{I_{out}}{I_{in}} = \frac{I_d}{I_g}$ falls to unity is called f_T.

$$f_T: h_{21}(f_T) = 1 \tag{3.10}$$

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \tag{3.11}$$

- **Maximum frequency of oscillation f_{MAX}**

The frequency at which the device power gain (G_P) drops to unity is called f_{MAX}. G_P is defined as the ratio of the power delivered to the load to the power input to the HEMT, and is evaluated by the product of current and voltage gains ($G_P = G_i \,.\, G_v$).

$$f_{MAX}: G_P(f_{MAX}) = 1 \tag{3.12}$$

$$G_P = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2\left[K\left|\frac{S_{21}}{S_{12}}\right| - Re\left(\frac{S_{21}}{S_{12}}\right)\right]} \tag{3.13}$$

where K is called the stability factor which determines the stability of the devices, and expressed as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{3.14}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. An unconditionally stable HEMT must meet the requirements of $K > 1$ and $|\Delta| < 1$.

3.4.1 Small-signal Equivalent Circuit Model

The equivalent circuit model of the device is of great importance in MMIC circuit design [58]. This represents the electrical characteristics of the device, where the electrical characteristic of a specific region of the device is described by each circuit element. The values of the circuit elements are based on the measured *S*-parameters at a single bias point (V_{DS}, V_{GS}). The basic equivalent circuit model that represents the electrical properties of the HEMT physical structure at mm-wave frequencies is shown in Figure 3.4 [58] [50] [78].

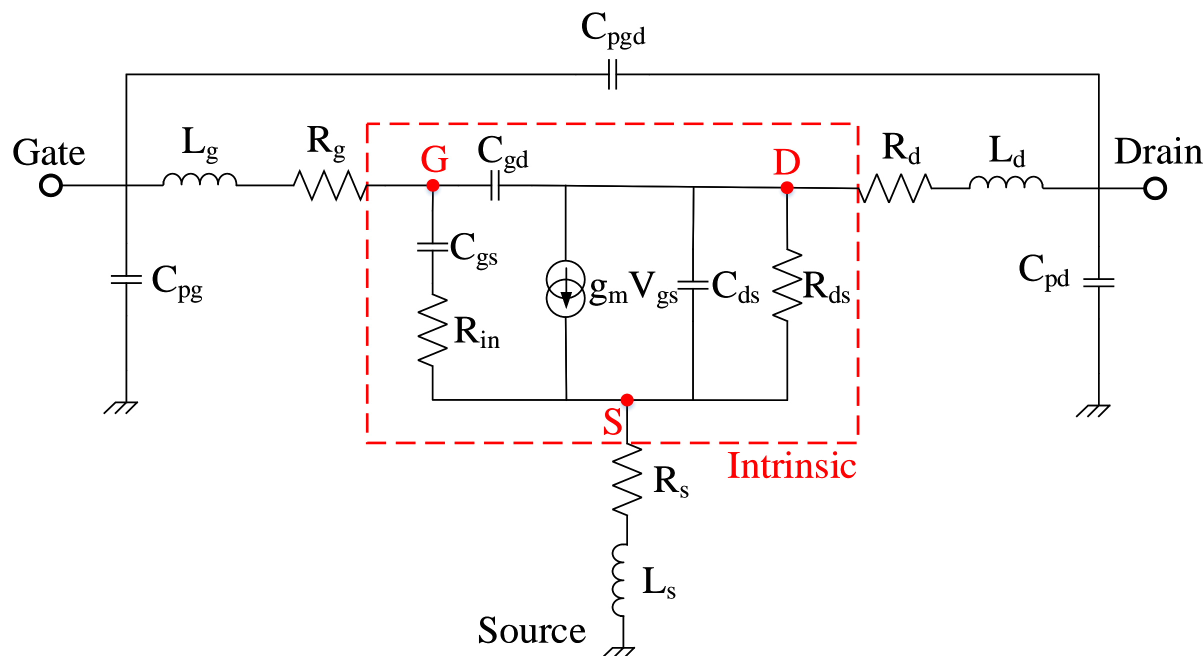


Figure 3.4: HEMT small-signal equivalent circuit model. Elements inside the dashed box show the intrinsic device, whereas the elements outside represent device Parasitics.

As indicated in Figure 3.4, the small-signal equivalent circuit consists of two regions - intrinsic and extrinsic. The transistor function is presented by the intrinsic elements, whereas, the parasitic elements of the devices are described by the extrinsic elements. The parasitic elements are mostly dependent on device geometry/layout design and have a strong influence on RF device performance.

Intrinsic Equivalent Circuit

The charge in the depletion region beneath the gate towards the source and drain sides is represented by gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}), respectively. The input resistance (R_{in}) is the charging resistance. The transistor gain is indicated by the current generator $g_m V_{gs}$. The finite output resistance of the device is represented by source-drain resistance, R_{ds}.

Extrinsic Equivalent Circuit

The source/drain ohmic contacts and bulk resistance leading up to active channel are accounted for by the series parasitic source resistance (R_s) and drain resistance (R_d). The gate resistance (R_g) arises from the metallisation resistance of Schottky contact, and can be estimated based on Equation 3.15 [58].

$$R_g = \frac{\rho W_G}{3n^2 h_G L_G} \tag{3.15}$$

where ρ is the gate metal resistivity. L_G, W_G and h_G are the gate length, width and height, respectively.

The metal contact pads are represented by the gate, source and drain parasitic inductances L_g, L_s and L_d, respectively. The electrical field distributions between the metal contacts in the HEMT are represented by the parasitic capacitances C_{pg}, C_{pg} and C_{pgd}. These capacitances are geometrically dependant on the design layout of the transistor.

Based on the definitions of f_T and f_{MAX} indicated in Section 3.4., f_T and f_{MAX} can be also calculated as function of the values of parasitic elements indicated in Figure 3.4 as follows [79] [80]:

$$f_T = \frac{g_m}{2\pi\left[\left(C_{gs} + C_{gd}\right)\left(1 + \frac{R_s + R_d}{R_{ds}}\right) + g_m C_{gd}(R_s + R_d)\right]} \tag{3.16}$$

$$f_{MAX} = \frac{f_T}{2\sqrt{\frac{R_{in} + R_s + R_g}{R_{ds}} + 2\pi f_T R_g C_{gd}}} \tag{3.17}$$

Having introduced the basic operation of a HEMT along with the most critical figures of merit that affect the DC and RF performance of the transistor, the following sections will be devoted to the measurement techniques and fabrication process and characterisation of high performance GaN-based HEMTs on LR Si.

3.5 Measurement Techniques

The DC and RF measurement configuration used at the University of Glasgow is shown in Figure 3.5 . B1500A Semiconductor Parameter Analyser was used for DC measurements [81]. Nucleus software was used to control the applied DC bias to the transistor [82]. To evaluate the RF response of these devices, on-wafer small-signal *S*-parameter measurements were performed from 0.01 to 67 GHz using an Agilent PNA network analyser (E8361A). Cascade Microtech RF probes were used for device probing. The system was calibrated with an off-wafer calibration Impedance Standard Substrate (ISS), using a Short-Open-Load-Thru (SOLT) calibration. WinCal software was utilised to remotely control the PNA during system calibration and RF measurements [83].

In this work, the DC and RF characteristics of the fabricated HEMTs were conducted over the frequency range 10 MHz to 120 GHZ at Fraunhofer Institute for Applied Solid State Physics IAF, Freiburg, Germany. Transistor pad parasitics were de-embedded from the measured *S*-parameters using the Open-Short de-embedding technique, which will be introduced in the following section.

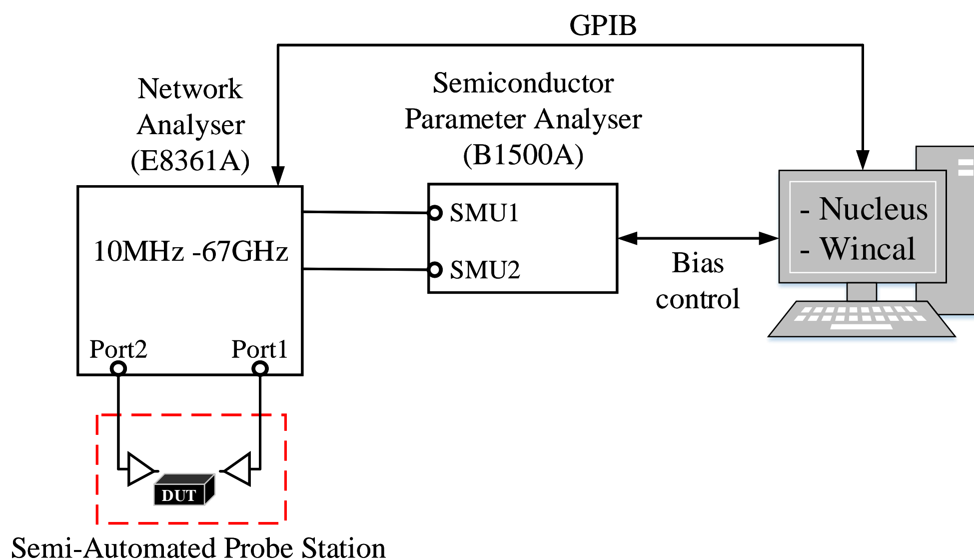


Figure 3.5: DC and RF measurement system at the University of Glasgow.

3.5.1 On-wafer Small-signal Open-Short De-embedding

De-embedding methodology is essentially required to eliminate the effect of the parasitics in the CPW test structure from the measured raw data. This enables a precise extraction of the RF

model parameters for the device-under-test (DUT), as these parasitics are not part of the device performance.

Open-Short de-embedding method is one of the most commonly used de-embedding approaches for GaN-based heterostructures on Si technology [84] [85] [86] [87]. The influence of the HEMT region between the RF probes, probe pads and DUT can be removed after de-embedding. This approach requires the use of open and short dummy structures, as shown in Figure 3.6. Substrate losses introduced by the input/output CPW test structure are mainly due to the parasitic capacitances and pad inductances. An open-circuited test structure is used to account for the parasitic capacitances, whereas the pad inductances are represented by a short-circuited pad structure. To ensure optimum results accuracy, de-embedding patterns need to be realised on wafer together with the DUT.

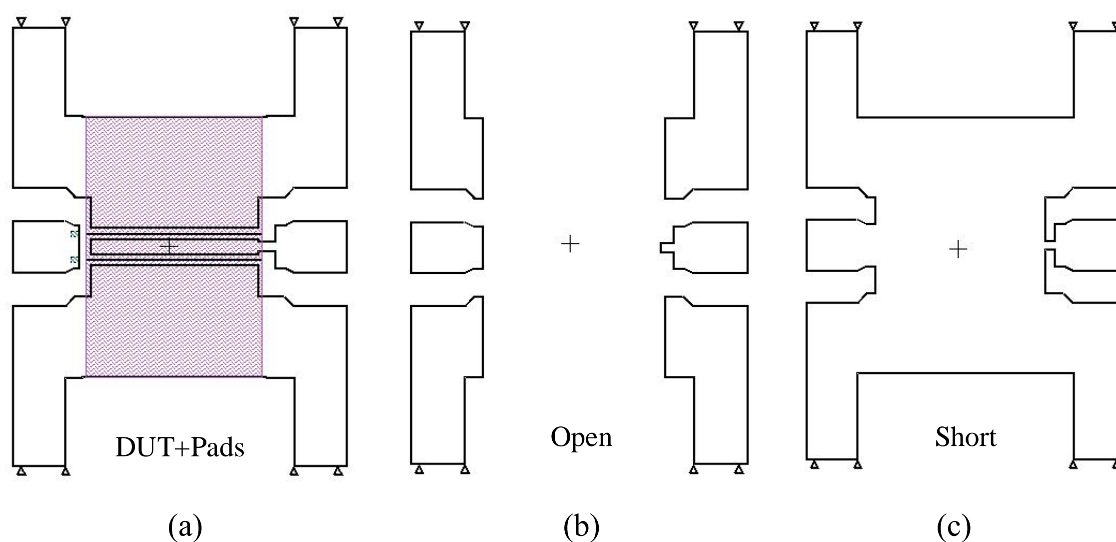


Figure 3.6: Open-Short de-embedding structures. (a) DUT with the measurement pads. (b) Open dummy structure. And (c) short dummy structure.

Figure 3.7 shows the equivalent circuit model of a typical DUT with parasitics from the test structures. The influence of the parallel parasitic elements is represented by Y_{P1}, Y_{P2} and Y_{P3}, whereas the series parasitic elements are represented by Z_{s1}, Z_{s2} and Z_{s3}.

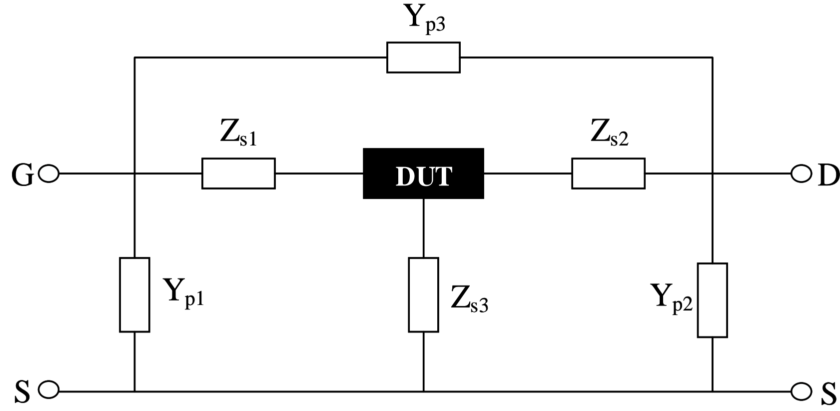


Figure 3.7: Equivalent circuit used for two-step de-embedding of measured high-frequency data of HEMTs

The parallel parasitic elements are eliminated using the measured data of the open dummy structure, whereas the series parasitic elements are eliminated using the measured data of both open and short dummy structures, as follows:

$$Y_{\mathrm{P3}} = -Y_{12,\mathrm{Open}} = -Y_{21,\mathrm{Open},} \tag{3.18}$$

$$Y_{\mathrm{P1}} = Y_{11,\mathrm{Open}} + Y_{12,\mathrm{Open},} \tag{3.19}$$

$$Y_{\mathrm{P2}} = Y_{22,\mathrm{Open}} + Y_{21,\mathrm{Open}.} \tag{3.20}$$

$$\begin{bmatrix} Z_{s1} + Z_{s3} Z_{s3} \\ Z_{s3} Z_{s2} + Z_{s3} \end{bmatrix} = \left(Y_{\mathrm{Short}} - Y_{\mathrm{Open}}\right)^{-1} \tag{3.21}$$

Equation 3.22 can be accordingly used to obtain the measured data corresponding to the DUT, that is,

$$Y_{\mathrm{transistor}} = \left[\left(Y_{\mathrm{DUT+Pads}} - Y_{\mathrm{open}}\right)^{-1} - \left(Y_{\mathrm{short}} - Y_{\mathrm{open}}\right)^{-1}\right]^{-1} \tag{3.22}$$

According to the above, several steps are required to perform the Open-Short de-embedding technique as summarised in the flowchart indicated in Figure 3.8 [88].

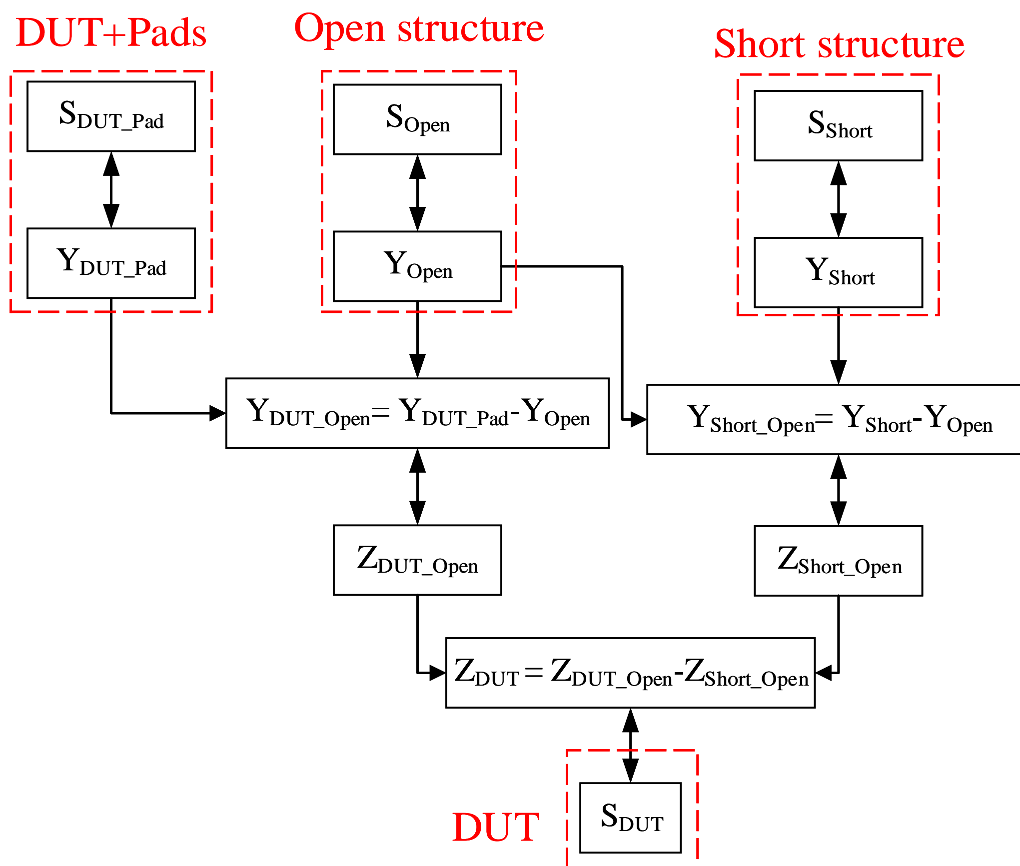


Figure 3.8: Open-Short de-embedding procedure.

The de-embedding procedure begins with measuring the *S*-parameters of the DUT with the measurement pads (S_{DUT_Pad}), open structure (S_{Open}) and short structure (S_{Short}), which are subsequently converted to *Y*-parameters. The converted *Y*-parameters are then passed through several operations to obtain the final *S*-parameters excluding the pads (S_{DUT}). Then, Equation 3.11 and Equation 3.13 can be used to evaluate f_T and f_{MAX} based on the de-embedded *S*-parameters S_{DUT}, respectively.

3.6 Fabrication Process

EBL was adapted for whole levels of device definition. For accurate comparison, it is worth mentioning that the fabrication process of any compared device structures was performed simultaneously, with identical fabrication and dielectric passivation techniques. This was done to ensure accurate comparison and avoid any possible uncertainties.

The fabrication process began with the definition of Ti/Pt (10/100 nm) alignment markers, which can withstand annealing to beyond 800 °C and still retain the necessary surface morphology and edge acuity required for subsequent registration in the e-beam tool. Next, the wafer was cleaned in HCl: H_2O (4:1) solution prior to the definition and ion beam evaporation of source/drain Ohmic contacts with various separation distances using a Ti/Al/Mo/Au (15/60/35/50 nm) metal-stack which was subsequently alloyed at 800 ^{0}C for 30 s in a N_2 ambient. Contact resistance (R_c) and specific contact resistivity (ρ_c) of ~ 0.6 Ω.mm and 5.71 × 10^{-6} Ω.cm^2 were obtained respectively. After mesa isolation using Cl_2 / Ar-based RIE/ICP, 200 nm-thick Si_3N_4 was deposited by ICP-CVD at room temperature as a passivation layer. To form the gate, a 0.27/0.3 µm feature (gate foot) was first aligned between the source and drain contacts, and transferred into the Si_3N_4 using a low bias, low damage SF_6 / N_2 plasma etch to form the gate-foot trenches. Ni/Au (20/200 nm) was then evaporated and lifted off. Windows in the Si_3N_4 at the ohmic contact areas were etched, whilst the other areas were kept entirely passivated (to avoid any GaN-exposed surface). Finally, the 700 nm gate-head was defined above the gate feed and in additional optimized bond-pads were also defined simultaneously. Finally a NiCr/Au (50/450 nm) metal-stack was deposited in the gate head and bond-pad resist developed regions. Fabrication process summary and schematic view of the fabricated devices is shown in Figure 3.9.

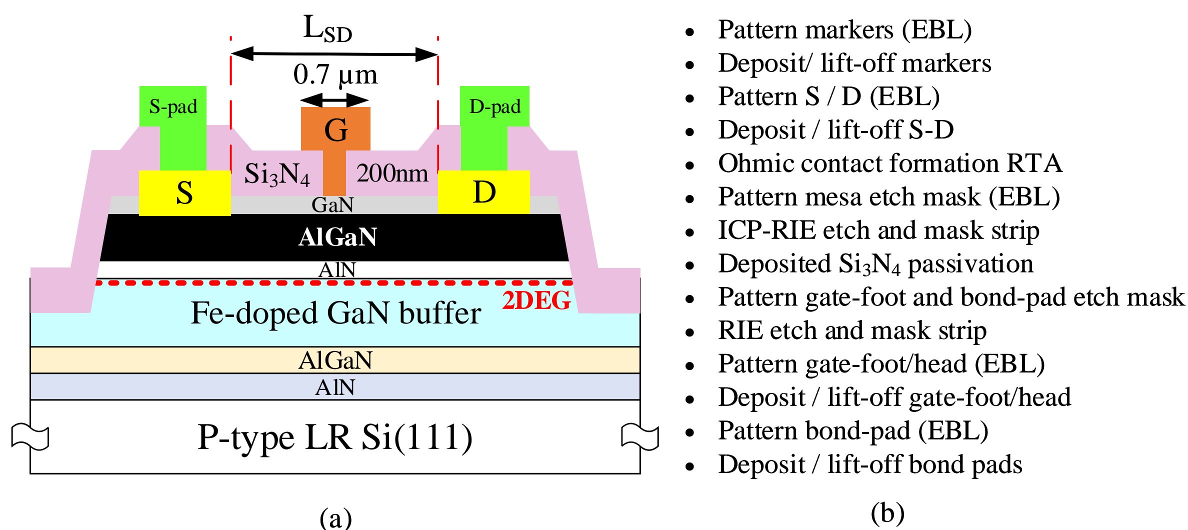


Figure 3.9: (a) Cross-sectional schematic view. And (b) the process flow for the fabrication of T-gate AlGaN/GaN HEMT on LR Si with Si_3N_4 passivation.

3.7 Impact of AlN Spacer on Device Characteristics.

Since the internal distribution of the ternary alloy components, e.g. AlGaN, is partially disordered, alloy scattering is more likely to exist in these compounds, where electrons may scatter as a result of natural aperiodicity. This makes binary semiconductors more beneficial when considering alloy scattering issue.

An optimized AlN interlayer thickness in the AlGaN/GaN HEMT structure resulted in the reduction of alloy scattering which plays a dominant factor in the 2DEG concentration and mobility [42]. Consequently, additional enhancement in the electrical properties of GaN-based HEMTs was obtained with an inserted thin AlN spacer between the AlGaN and GaN channel. This section focuses on the effect of inserting an AlN spacer between the GaN channel and buffer in AlGaN/GaN HEMTs grown on LR Si on both DC and RF performances. The effect of an AlN spacer layer insertion on the RF performance of GaN HEMTs grown on LR Si was analysed based on the small-signal equivalent circuit elements values.

3.7.1 Material and Devices

Two different types of AlGaN/GaN HEMTs materials, with and without AlN interlayer, were grown on a 675 µm thick 150 mm diameter P-type LR Si ($\sigma < 10$ Ω.cm) substrate by Metal-Organic Chemical Vapor Deposition (MOCVD). The layer stack, from the substrate up, consists of a 250 nm AlN nucleation layer followed by a 850 nm Fe-doped AlGaN graded buffer (to accommodate the lattice and thermal expansion miss-match), a 1.4 µm insulating Fe doped GaN buffer layer and a GaN channel layer (includes, a 1 nm AlN spacer layer, a 25 nm $Al_{0.25}Ga_{0.75}N$ barrier and a 2 nm GaN cap), as shown in Table 3.1. Hall measurements showed carrier density of 8.1×10^{12} cm^{-2} and 7.1×10^{12} cm^{-2} with associated mobility of 1700 cm^2/V.s and 1580 cm^2/V.s and sheet resistivity of 412 Ω/sq. and 552 Ω/sq. for both epitaxial layers with and without an AlN interlayer, respectively.

Table 3.1: Epitaxial layer structure of the compared devices; with and without the AlN interlayer.

Layer *	Sample A		Sample B	
	x	d (nm)	x	d (nm)
GaN cap	-	2	-	2
$Al_xGa_{1-x}N$ barrier	25 %	25	25 %	25
AlN interlayer	-	1	-	N/A
GaN buffer	-	1.4	-	1.4
AlGaN nucleation layer	-	850	-	850
AlN nucleation layer	-	250	-	250
P-type LR silicon (111)	675 µm			
* (d) stands for thickness and (x) stands for Al concentration				

3.7.2 Results and Discussion

A. DC Characteristics

Typical DC output characteristics of an L_G = 0.3 µm, W_G = 2 × 100 µm wide devices are shown in Figure 3.10a. The HEMT with AlN spacer layer exhibits comparatively higher drain current density, I_{DS} by 18 % than conventional AlGaN/GaN HEMT. A maximum I_{DS} of 1.4 A/mm at V_{DS} = 10 V and V_{GS} = +1 V was obtained. However, the insertion of AlN spacer layer caused a slight degradation in the switching performance, with on-resistance, R_{ON} of 2.76 Ω.mm compared to 2.24 Ω.mm of conventional AlGaN/GaN HEMTs.

Since the alloy scattering of binary compounds (AlN) is less than ternary compounds (AlGaN) [42], the insertion of AlN spacer layer at the heterojunction increased the quantum well depth and reduced alloy scattering, resulting in improvement in mobility of the charge carriers in the 2DEG channel.

Both devices performed well-behaved pinch-off voltages with a reduction of 0.8 V associated with little enhancement in the peak extrinsic transconductance, G_m in the absence of AlN interlayer. A maximum G_m, of 433 mS/mm was obtained at V_{DS} = 5 V and V_{GS} = -2.4 V compared to 425 mS/mm at V_{DS} = 5 V and V_{GS} = -3.2 V when the AlN spacer layer was presented, as indicated by the transfer characteristics measurements shown in Figure 3.10b.

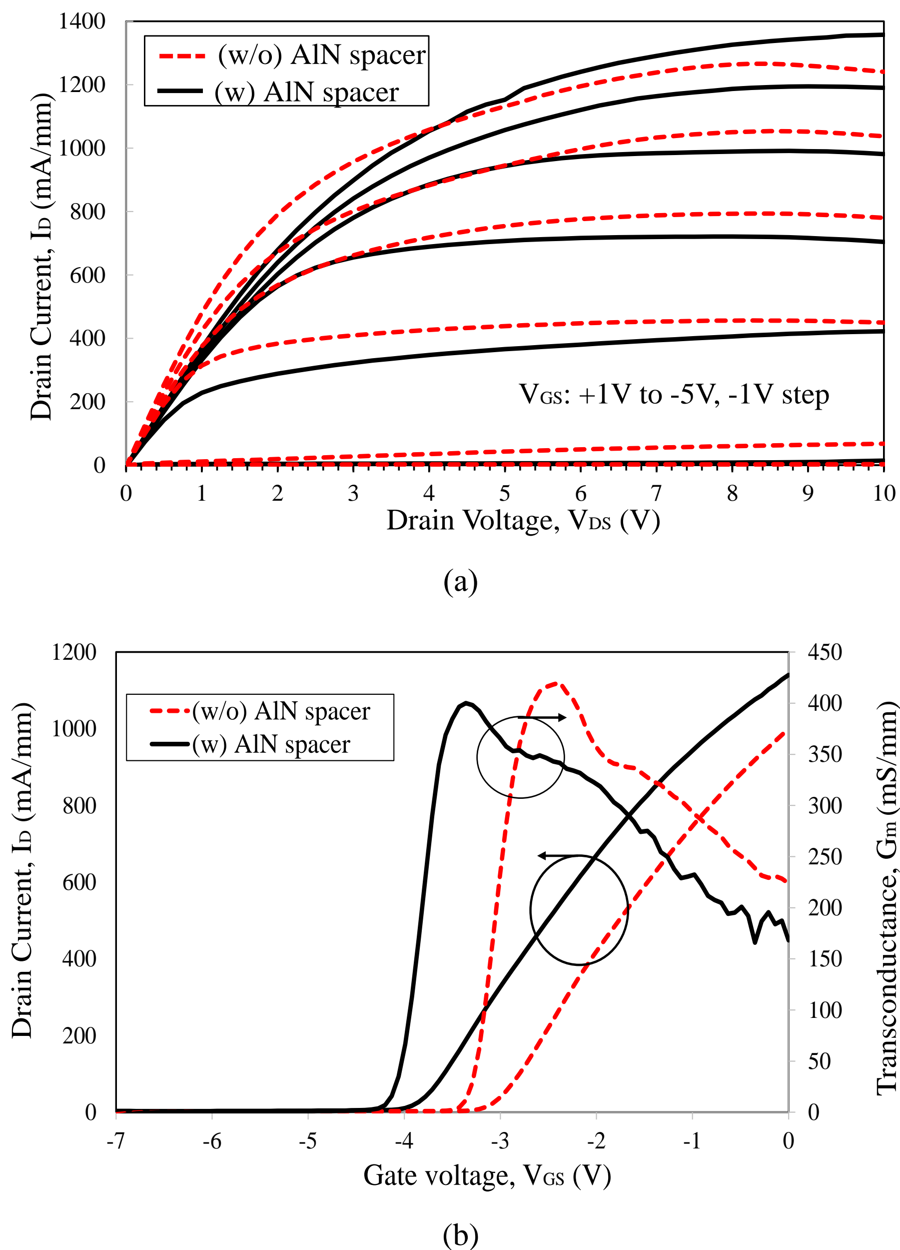
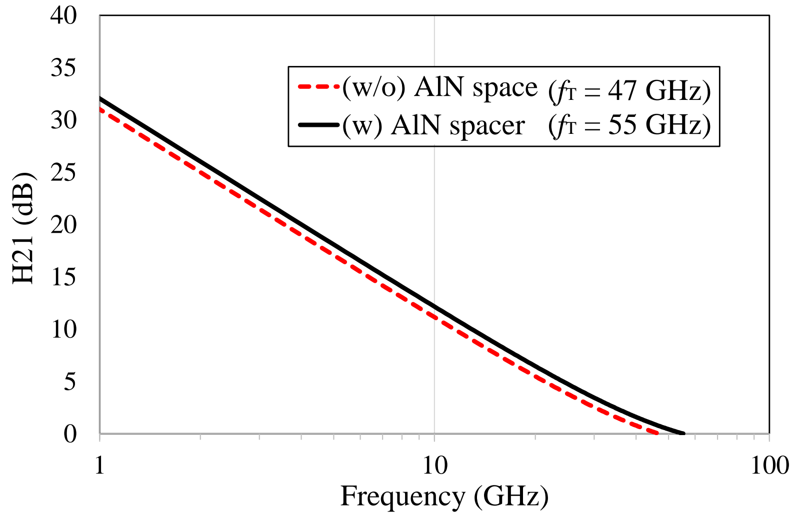


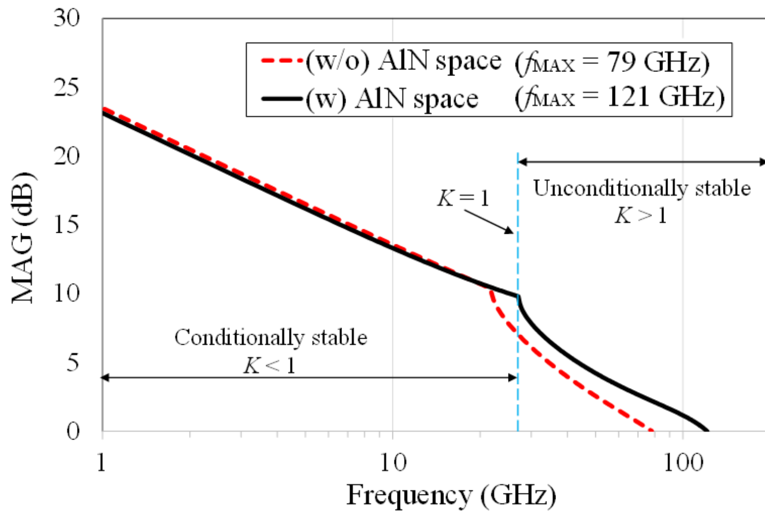
Figure 3.10: (a) Output. And (b) Transfer characteristics at a fixed drain voltage, V_{DS} = 5V of 2 × (0.3 × 100) μm^2 AlGaN/GaN HEMTs on LR Si with (w) and without (w/o) the AlN interlayer.

B. RF Characteristics

Figure 3.11 shows the de-embedded small-signal gain characteristics of 0.3 μm T-gate GaN-based HEMTs on LR Si, with and without the AlN interlayer. The devices were biased at their



(a)



(b)

Figure 3.11: Small-signal gain characteristics based on extracted *S*-parameters of a 0.3 µm × 200 µm AlGaN/GaN HEMTs on LR Si (111) substrate at V_{DS} = 5 V and V_{GS} = -3.2 V(with AlN spacer), and V_{GS} = -2.4 V (without AlN spacer). (a) H_{21}. And (b) MAG.

best RF performance where the highest current gain (H_{21}) and Maximum Available Gain (MAG)/power gain existed. Since the intersection of both H_{21} and MAG with frequency, at which $H_{21}(f)$ = MAG (f) = 0, occurs within the measurement frequency range, extrapolation of H_{21} and MAG using a -20 dB/decade slope is not required [89]. Significant improvements in RF performance were observed when incorporating the AlN spacer in the layer structure. A maximum f_T of 55 GHz and f_{MAX} of 121 GHz were achieved for the AlGaN/GaN HEMT with AlN spacer in comparison to an f_T of 47 GHz and f_{MAX} of 79 GHz for the conventional AlGaN/GaN HEMTs.

The effect of the AlN interlayer on RF performance was quantified based on the bias-dependent equivalent-circuit element values as summarized in Table 3.2. The observed enhancement in microwave performance is mainly attributed to reducing the electron trap effect because of the negative charges captured by surface states [22]. This reduction in trapped charges caused a decrease of 36 % in device intrinsic capacitance C_{gs} (from 145 fF to 92 fF), which had a significant influence on f_T and f_{MAX}. Consequently, the modulated signal and electrical field under the gate edge towards the drain were increased despite the 11 % deterioration in the channel current modulation efficiency, G_m.

Table 3.2: Fitted values for all model parameters in the equivalent circuit for a L_G = 0.3 µm and W_G = (2 × 100) µm transistors at V_{DS} = 5 V and V_{GS} = -3.2 V (Sample A), and V_{GS} = -2.4 V (Sample B).

Extrinsic Parameters			**Intrinsic Parameters**		
Parameter	**Sample A**	**Sample B**	**Parameter**	**Sample A**	**Sample B**
C_{pg} (fF)	43.9	43.9	C_{gd} (fF)	*10.5*	*9.1*
C_{pd} (fF)	43.8	43.1	C_{gs} (fF)	*92.4*	*145.4*
L_s (pH)	0.03	0.03	C_{ds} (fF)	*11.8*	*15.6*
L_g (pH)	23	23	τ (ps)	*1.2*	*1.5*
L_d (pH)	25	25	G_m (mS/mm)	*530*	*602*
C_{pgd} (fF)	15	16	R_{in} (Ω)	*13.11*	*20.3*
R_s (Ω)	10.5	10.5	R_{gd} (Ω)	*500*	*500*
R_g (Ω)	17.9	17.9	R_{ds} (Ω)	*415*	*415*
R_d (Ω)	12.3	12.3			

The insertion of an AlN interlayer was very effective in providing the confinement to the 2DEG, preventing them from overflowing into the buffer and towards the conductive Si substrate. This is because of the large conduction band offset, high polarization field and high barriers [42]. Therefore, interaction of carriers to electron traps at surfaces and crystalline defects were reduced. AlN interlayer will be considered for the next epitaxial layer structures in the following sections.

3.8 Impact of Scaling the AlGaN Schottky Barrier on Device Characteristics

To further improve the DC and RF performance of AlGaN/GaN HEMTs, it was necessary to both reducing the T-shaped gate length (L_G) and downscaling the AlGaN barrier layer (d_{AlGaN}) were both necessary. These help to maintain a sufficiently high aspect ratio (L_G/d_{AlGaN}) in order to suppress SCEs and keep the parasitic capacitance values C_{gs} and C_{gd} relatively low [90]. However, reducing the barrier layer thickness in the AlGaN/GaN HEMTs requires the use of high Al mole fraction AlGaN material growth. This is because a thinner barrier makes the 2DEG more sensitive to surface state traps causing an increase in the current collapse [91]. Moreover, the transport properties of $Al_xGa_{1-x}N$/GaN structure with $x > 0.5$ have been degraded, limiting the minimum achievable barrier thickness [92]. The DC and microwave performance were severely affected by both the mole fraction of Al and thickness of the barrier. For example, a higher Al mole fraction caused a degradation in G_m, whereas improvements in the polarisation strength (hence the increase in the 2DEG density) were obtained [93]. Therefore, these growth parameters need to be carefully optimised for high-power high-frequency applications.

This section mainly deals with the influence of reducing the AlGaN barrier thickness (from 27 nm to 9 nm) and correspondingly increasing the mole fraction of Al (form 25 % to 35 %) on AlGaN/GaN HEMTs on LR Si performance for better device performance. The RF performance of the fabricated devices was further analysed using the small-signal equivalent circuit.

3.8.1 Material and Devices

Two different types of AlGaN/GaN HEMT material structure, with two different AlGaN barrier thicknesses (27 nm and 9 nm), were grown on a 1 mm thick 150 mm diameter P-type LR Si (σ < 10 Ω.cm) substrate. The layer stack, from the substrate up, consists of a 200 nm AlN nucleation layer followed by a 900 nm Fe-doped AlGaN graded buffer (to accommodate the lattice and thermal expansion miss-match), a 2.6 µm insulating Fe doped GaN buffer layer and a GaN channel layer (includes, a 1 nm AlN spacer layer, a 27 nm $Al_{0.25}Ga_{0.75}N$/ 9 nm $Al_{0.35}Ga_{0.65}N$ barrier and a 2 nm GaN cap), as shown in Table 3.3. However, because of the presence of defects on all the areas where Van-Der-Pauw (VDP) test structures exist on the

fabricated samples, hall measurements on these devices were unsuccessful. This is because VDPs test structures occupied relatively large areas compared to the HEMT structures, where it is more likely to find a defect in a large area.

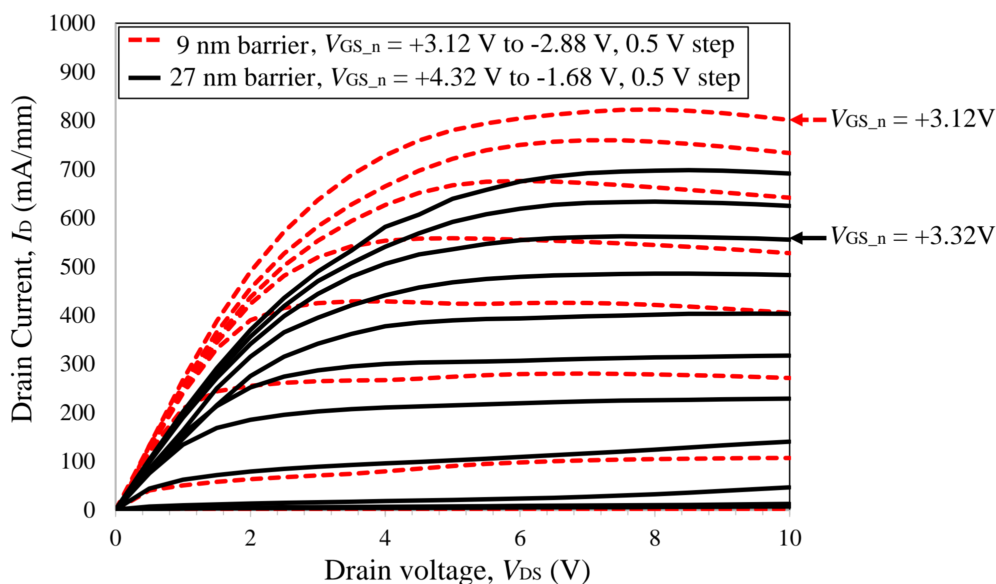
Table 3.3: Epitaxial layer structure of the compared samples, with different AlGaN Schottky barriers

Layer *	Sample C		Sample D	
	x	d (nm)	x	d (nm)
GaN cap	-	2	-	2
$Al_xGa_{1-x}N$ barrier	25 %	9	35 %	27
AlN interlayer	-	1	-	1
GaN buffer	-	2.6	-	2.6
AlGaN nucleation layer	-	900	-	900
AlN nucleation layer	-	200	-	200
P-type LR silicon (111)	1000 µm			
* (d) stands for thickness and (x) stands for Al concentration				

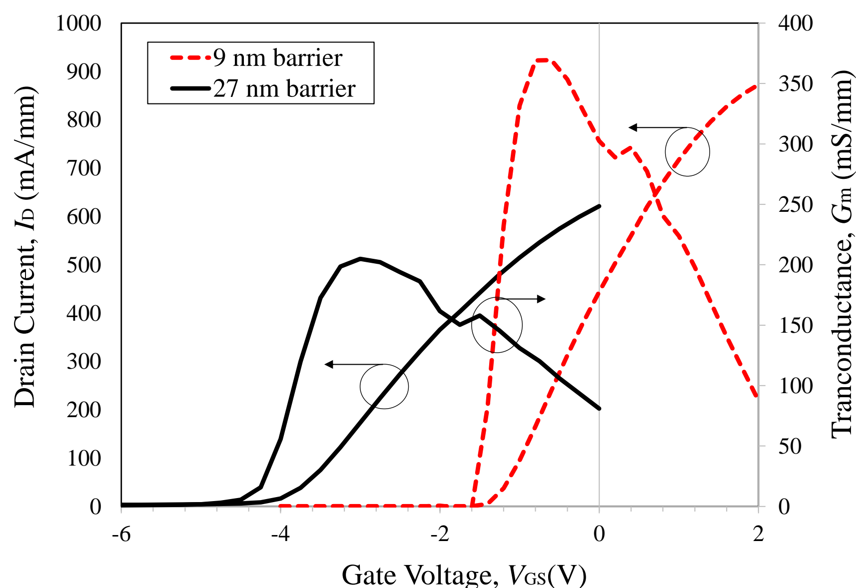
3.8.2 Results and Discussion

A. DC Characteristics

Typical DC output characteristics of an L_G = 0.27 µm, source-to-drain spacing, L_{SD} = 1.8 µm, W_G = 2 × 100 µm wide devices are shown in Figure 3.12a. Since there was a nearly 3 V difference in V_T between the compared devices, V_{GS} was normalized to a V_T of -1.12 V and V_T = -4.32 for the HEMTs with 9 nm and 27 nm barrier layers, respectively. In other words, the device turn-on voltage (V_T) was used as reference. It can be seen that an optimized scaling of the barrier thickness has effectively improved the mobility of the charge carriers in the 2DEG channel as a result of the increased polarization strength. Therefore, the I_{DS} was enhanced by 32.5 % when biasing both devices at a similar V_{GS_n} of + 3.32 and + 3.12 V and a fixed V_{DS} of 8 V, compared to the HEMT with its 27 nm barrier layer, where a maximum I_{DS} of 825 mA/mm



(a)



(b)

Figure 3.12: (a) Output. And (b) Transfer characteristics of 2 × (0.27 × 100) µm^2 AlGaN/GaN HEMTs on LR Si with two different top barriers; 27 nm $Al_{0.25}Ga_{0.75}N$ and 9 nm $Al_{0.35}Ga_{0.65}N$. V_{GS_n} is V_{GS} normalised to V_T.

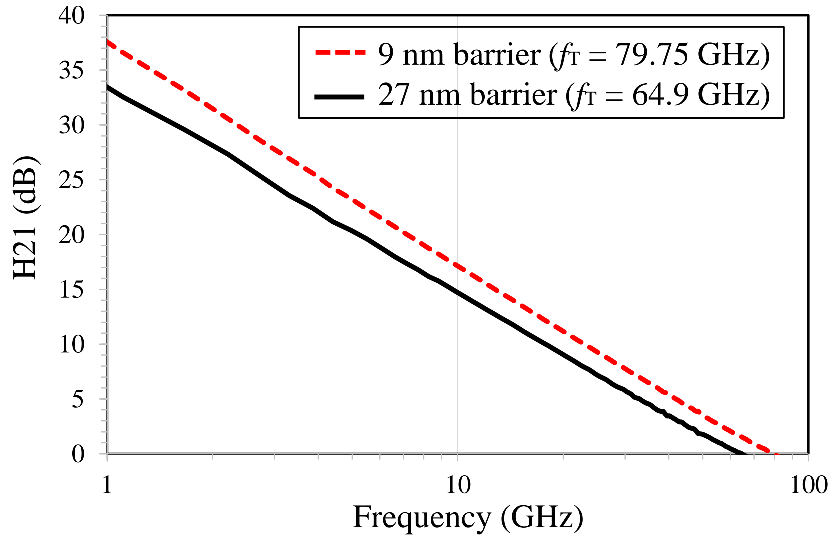
at V_{DS} = 8 V and V_{GS} = +2 V was achieved. In addition to the increase in the 2DEG density, the switching performance was also improved for the HEMT with a 9 nm barrier, with an R_{ON} of 1.87 Ω.mm compared to 2.35 Ω.mm of 27 nm barrier HEMT. In addition, scaling of the barrier has drastically suppressed gate leakage (I_G), where an I_G of 0.05 mA/mm was obtained for thicker barrier devices, compared to 1×10^{-20} nA/mm for devices with a thinner barrier at V_{DS} = 10 V and V_{GS} = -6 V.

The transfer characteristics of the fabricated devices are shown in Figure 3.12b. Both devices exhibited well-behaved pinch-off voltages with a positive shift of 3.2 V in the threshold voltage, V_T associated with ultra-low gate leakage current for the 9 nm barrier HEMT. This meant that the 9 nm barrier HEMT was working closer to an enhancement mode than the 27 nm barrier HEMT, where only low voltage (-1.12 V) was required to pinch-off the channel. In addition, this technology can be utilised as an alternative method of shifting the V_T without the need to use other complicated techniques, such as gate-recess or dielectric gated techniques [94]. However, gate-recess techniques are difficult to control precisely and may result in high gate leakage currents and a reliability issue because of the generation of surface defects [29]. The dielectric gated technique results in an increase in the overall Schottky barrier thickness degrading the microwave performance of the devices as a result of reducing the device transconductance. This also limits the minimum applicable L_G required to eliminate SCEs. Moreover, contamination could be introduced in the interface between the Schottky barrier and gate dielectric, resulting in device stability issues.

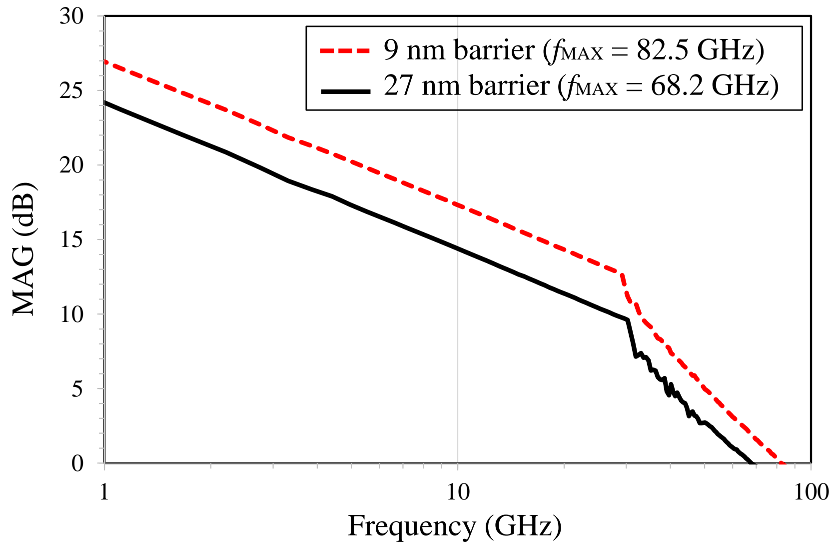
In addition, an enhancement of more than 80% in the peak extrinsic transconductance, G_m in the HEMT with scaled barrier of 9 nm was observed. A maximum G_m, of 369 mS/mm were obtained at V_{DS} = 5 V and V_{GS} = -0.6 V compared to 205 mS/mm at V_{DS} = 5 V and V_{GS} = -3 V for the 27 nm barrier HEMT. These findings agree with Equation 3.6, where G_m is reversal proportional to the depletion region depth/ barrier high.

B. RF Characteristics

Figure 3.13 shows the de-embedded small-signal gain characteristics of 0.27 µm T-gate GaN-based HEMTs on LR Si with two different top barrier designs; 27 nm $Al_{0.25}Ga_{0.75}N$ and 9 nm $Al_{0.35}Ga_{0.65}N$. Both devices were biased at their peak f_T. The RF performance was significantly enhanced when scaling the AlGaN barrier to 9 nm. Therefore, a maximum f_T of 79.75 GHz and f_{MAX} of 82.5 GHz were achieved for the AlGaN/GaN HEMT with 9 nm barrier, compared to an f_T of 64.9 GHz and f_{MAX} of 68.2 GHz for the 27 nm barrier AlGaN/GaN HEMT. These were the best combinations of f_T and f_{MAX} achieved to date for AlGaN/GaN HEMTs on LR Si technology.



(a)



(b)

Figure 3.13: Small-signal gain characteristics based on extracted *S*-parameters of a 0.27 µm × 200 µm AlGaN/GaN HEMTs LR Si at V_{DS} = 5.5 V and V_{GS} = -0.5 V (9 nm barrier), and V_{DS} = 3 V and V_{GS} = -3 V (27 nm barrier). (a) H_{21}. And (b) MAG.

The effect of scaling the AlGaN barrier thickness on RF performance was analysed using the bias-dependent equivalent-circuit element values, as summarized in Table 3.4. It can be seen that the observed improvement in microwave performance of the HEMT with 9 nm AlGaN, despite the increase in C_{gs}, is mainly attributed to two main factors: increasing the transconductance, G_m from 173 mS/mm to 405 mS/mm, and reducing the intrinsic delay time, τ (1.23 ps to 1.06 ps). C_{gs} is expected to increase when reducing the barrier thickness as its value is proportional to the gate-to-channel distance, as indicated in Equation 3.7. These

findings indicate the successful material engineering of scaling the AlGaN Schottky barrier with an improvement in both DC and microwave performance.

Table 3.4: Fitted values for all model parameters in the equivalent circuit for a L_G = 0.27 µm and W_G = (2 × 100) µm transistors at V_{DS} = 5.5 V and V_{GS} = -0.5 V (sample C), and V_{DS} = 3 V and V_{GS} = -3 V (sample D).

Extrinsic Parameters			**Intrinsic Parameters**		
Parameter	**Sample C**	**Sample D**	**Parameter**	**Sample C**	**Sample D**
C_{pg} (fF)	44.3	42.15	C_{gd} (fF)	*13.6*	*11.4*
C_{pd} (fF)	41.7	40.7	C_{gs} (fF)	*148*	*96*
L_s (pH)	0.05	0.05	C_{ds} (fF)	*8.3*	*8.3*
L_g (pH)	20.4	20.4	τ (ps)	*1.06*	*1.23*
L_d (pH)	25.1	25.1	G_m (mS/mm)	*405*	*173*
C_{pgd} (fF)	26.05	26.05	R_{in} (Ω)	*8.11*	*12.31*
R_s (Ω)	11.2	11.2	R_{gd} (Ω)	*330*	*330*
R_g (Ω)	16.91	16.91	R_{ds} (Ω)	*405*	*413*
R_d (Ω)	11.7	11.7			

3.9 Impact of Source-to-drain Separation on Device Characterises.

Dramatic improvements in the breakdown voltage, V_{BV} while maintaining high f_T were obtained by increasing Source/Drain (S/D) gaps for GaN HEMTs realized on SI substrates, such as HR Si and SiC [95] [89]. However, unlike SI substrates, the microwave performances of GaN HEMTs grown on LR Si substrates are expected to be prone to device dimensions and material growth quality, mainly because of the RF signal coupling effect in the conductive Si substrate. The study of the effect of L_{SD} on both DC and RF performance of AlGaN/GaN HEMTs on LR Si helped to identify a trade-off between frequency and breakdown properties which was crucial for the realization of the optimized GaN-on-Si HEMT technology platform that allows integration of RF and power converter functionality for a range of high efficiency/high frequency applications. This study was carried out on the same materials used in Section 3.8.1.

3.9.1 Results and Discussion

A. DC Characteristics

Figure 3.14 shows a typical DC output and transfer characteristics of a 2 × (0.27 × 100) μm^2 9 nm-thick barrier devices with L_{SD} = 1.8 and 8.15 µm. Degradation in the DC performance was observed as the S/D spacing increased, as a result of the increased access resistances. Therefore, devices with the smallest L_{SD} of 1.8 µm achieved a maximum I_{DS} of 825 mA/mm at V_{DS} = 8 V and V_{GS} = +2 V, compared to I_{DS} of 622 mA/mm at V_{DS} = 6.5 V and V_{GS} = +2 V for the devices with L_{SD} = 8.15 µm. A negative I_{DS} slope/negative transconductance is observed in the device with L_{SD} = 8.15 µm at V_{DS} > 7 V and V_{GS} = +2 V. This attributes to the current collapse connected with the thermal effect and traps charging and discharging in the material. .A rise of 89 % in R_{ON} was noticed when the S/D gap increased from 1.8 to 8.15 µm; R_{ON} = 1.87 and 3.44 Ω.mm for the devices with L_{SD} = 1.8 µm and 8.15 µm respectively.

All devices exhibited excellent pinch-off characteristics of -1.12 V, where the best G_m of 369 mS/mm was obtained at V_{DS} = 5 V and V_{GS} = -0.5 V for L_{SD} = 1.8 µm. However, G_m dropped by 33 % (G_m = 247 mS/mm) when the L_{SD} was increased to 8.15 µm, as indicated by the transfer characteristics measurements shown in Figure 3.14b. Generally, devices with thicker barrier (27 nm) exhibit similar DC characteristics to those of thinner barrier (9 nm) devices when the S/D gap was increased.

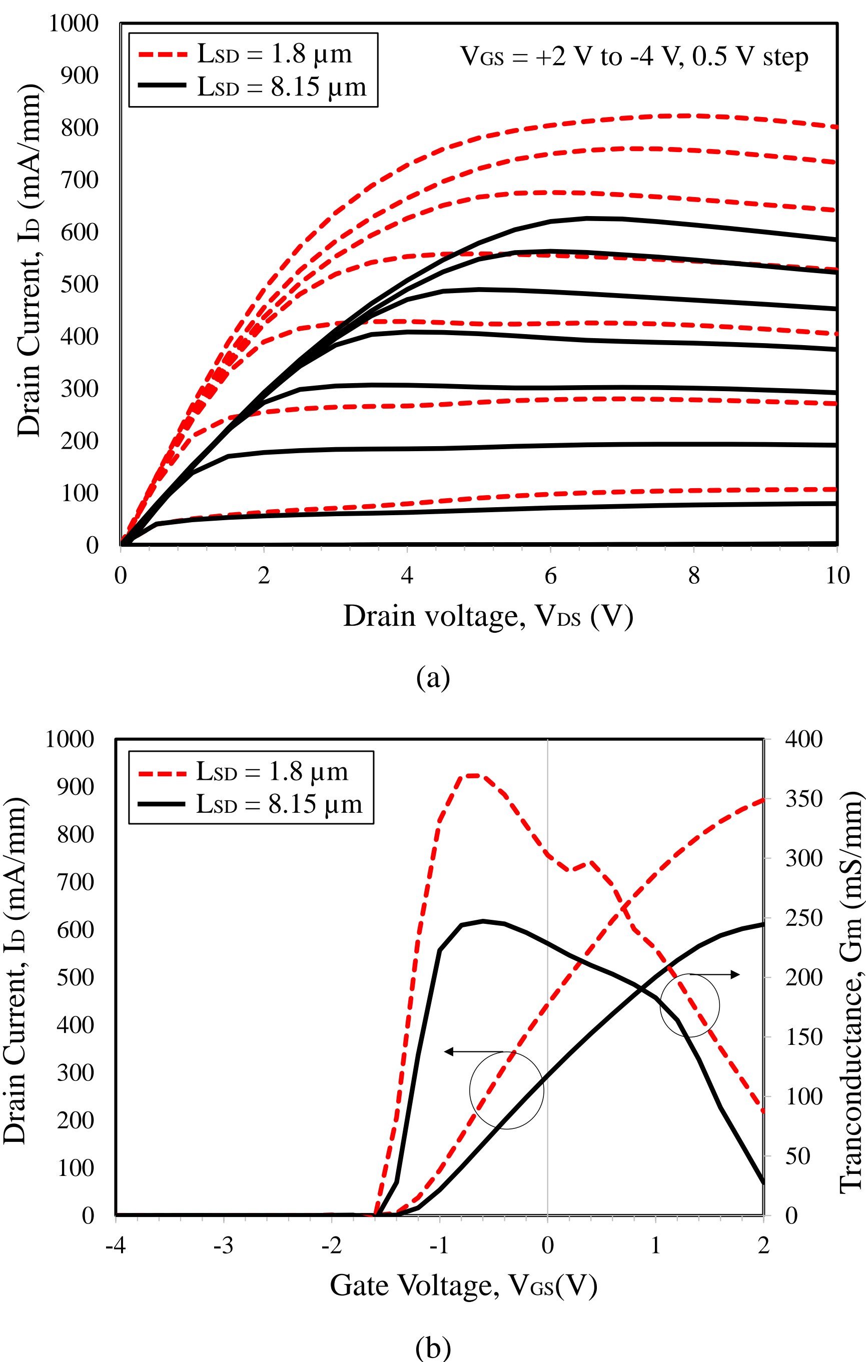
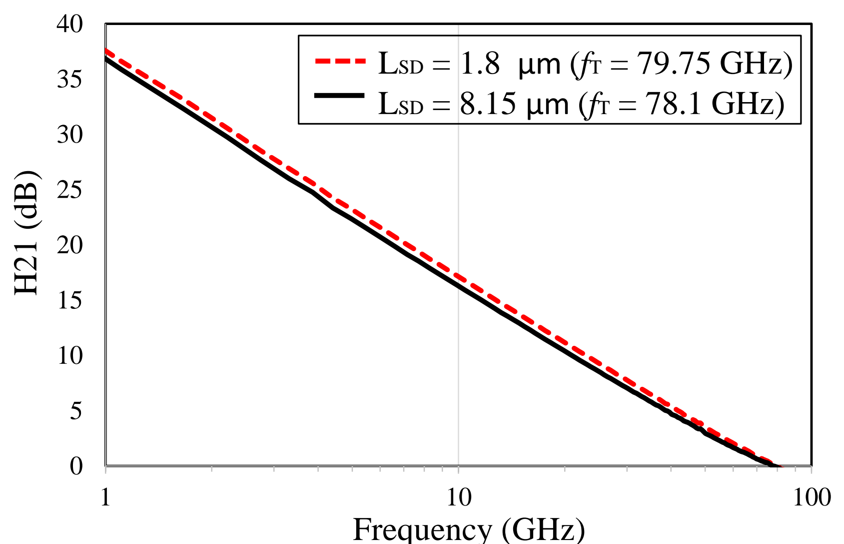


Figure 3.14: (a) Output. And (b) Transfer characteristics of 2 × (0.27 × 100) µm^2 AlGaN/GaN HEMTs on LR Si with L_{SD} = 1.8 µm and 8.15 µm

B. RF Characteristics

Figure 3.15 shows the de-embedded transistor microwave performance of a 2 × (0.27 × 100) µm^2 9 nm-thick barrier devices at the peak f_T bias point of (V_{DS}, V_{GS}) = (5.5 V, -0.5 V) and (V_{DS}, V_{GS}) = (6.5 V, -0.5 V) for devices with L_{SD} = 1.8 µm to 8.15 µm, respectively. Generally, it can be seen that there is no significant degradation observed in microwave performance when

increasing the L_{SD} from 1.8 µm to 8.15 µm, where f_T and f_{MAX} were only decreased by 2 % and 9 %, respectively.



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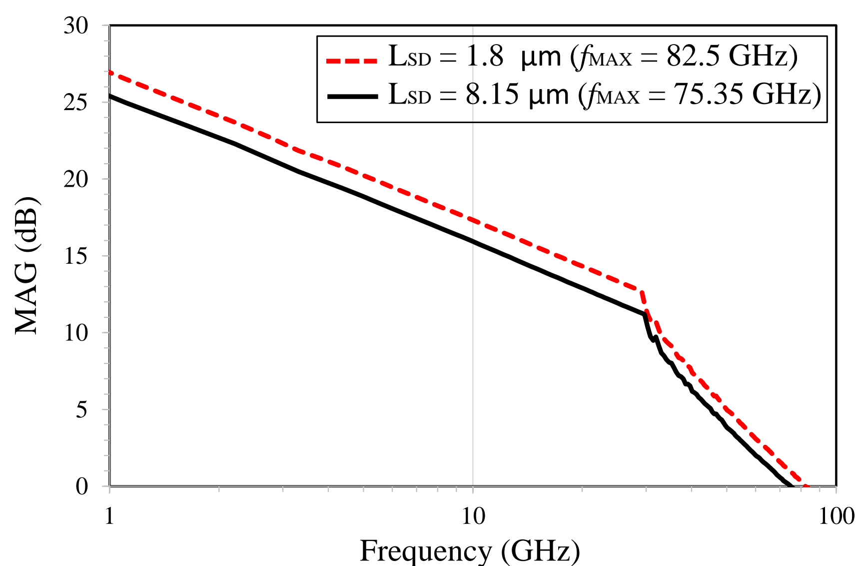


(b)

Figure 3.15: Small-signal gain characteristics based on extracted *S*-parameters of a 2 × (0.27 × 100) µm^2 AlGaN/GaN HEMTs LR Si at V_{GS} = -0.5 V, and V_{DS} = 5.5 V (L_{SD} = 1.8 µm) and V_{DS} = 6.5 V (L_{SD} = 8.15 µm). (a) H_{21}. And (b) MAG.

The effect of scaling the S/D gap on RF performance was analysed based on the bias-dependent equivalent-circuit elements values, as summarized in Table 3.5. It can be clearly seen that increasing the S/D spacing resulted in a reduction in parasitic capacitances (particularly C_{gs}), whereas an increase in parasitic resistances was observed. This could be the reason why

increasing L_{SD} had no major impact on the microwave performance of devices with 9 nm AlGaN barrier.

Table 3.5: Fitted values for all model parameters in the equivalent circuit for a L_G = 0.27 µm and W_G = (2 × 100) µm transistors at V_{GS} = -0.5 V, and V_{DS} = 5.5 V (L_{SD} = 1.8 µm) and V_{DS} = 6.5 V (L_{SD} = 8.15 µm).

Extrinsic Parameters			**Intrinsic Parameters**		
Parameter	L_{SD} = 1.8 µm	L_{SD} = 8.15 µm	**Parameter**	L_{SD} = 1.8 µm	L_{SD} = 8.15 µm
C_{pg} (fF)	44.3	42.15	C_{gd} (fF)	*13.6*	8.6
C_{pd} (fF)	41.7	40.7	C_{gs} (fF)	*148*	101
L_s (pH)	0.05	0.05	C_{ds} (fF)	*8.3*	5.7
L_g (pH)	20.4	20.4	τ (ps)	*1.06*	1.74
L_d (pH)	25.1	25.1	G_m (mS/mm)	*405*	269
C_{pgd} (fF)	26.05	10.8	R_{in} (Ω)	*8.11*	9.91
R_s (Ω)	11.2	11.2	R_{gd} (Ω)	*330*	460
R_g (Ω)	16.91	16.91	R_{ds} (Ω)	*405*	1300
R_d (Ω)	11.7	11.7			

Figure 3.16 summarises the effects of L_{SD} on device speed, f_T at V_{DS} = 9 V and a V_{GS} value corresponding to the best result obtained for f_T for both 9 nm and 27 nm thick AlGaN barrier thicknesses. For higher drain-source potential, the electrical field across the barrier will be high enough to facilitate carrier tunneling to the 2DEG [96]. This makes the modulated RF signal under the gate more likely to couple to the LR Si substrate rather than drain. It is clear that the S/D separation increase has a negligible effect on the f_T (which is a measurements with the drain AC-grounded) of devices with a thinner barrier, whereas its effect was noticeable on the thicker barrier devices. This could be a result of the excellent-engineered material growth of the devices with thinner barriers where electrons were effectively confined to the 2DEG, preventing them from overflowing into the buffer and towards the conductive Si substrate.

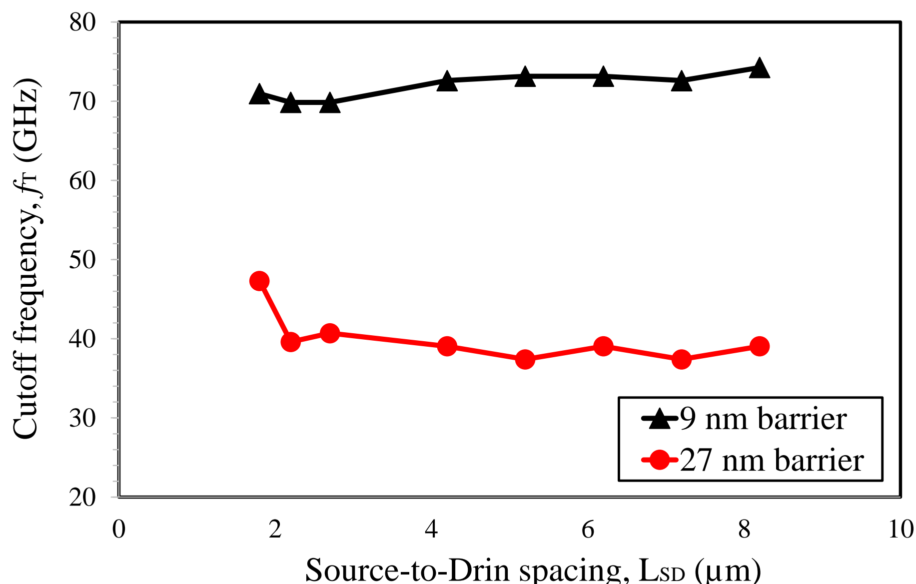
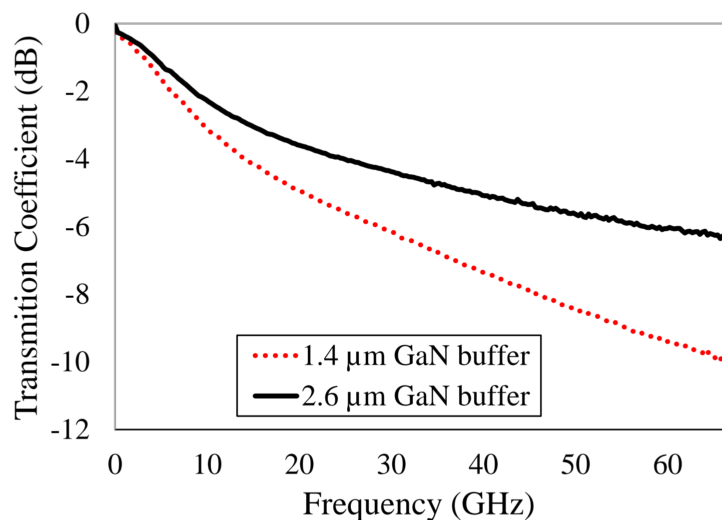


Figure 3.16: Unity current gain frequency against source-to-drain spacing of a 2 × (0.27 × 100) μm^2 AlGaN/GaN HEMTs LR Si.

3.10 Effect of GaN Buffer Thickness on Device Performance

The influence of the GaN buffer thickness on DC performance has already been studied in AlGaN/GaN HEMTs grown on SI SiC substrates. It has been found that devices with thinner GaN buffer achieved better DC characteristics as a result of the reduction in buffer leakage current. This is because of the higher concentration of dislocations threading to the surface of a thin buffer [41]. In this work, AlGaN/GaN HEMTs on LR Si substrates exhibited a similar trend but this was more obvious, where degradation in the DC characteristics was observed when increasing the buffer thickness from 1.4 µm to 2.6 µm. As shown in Figure 3.10 and Figure 3.12, the DC performance seems to be more sensitive to GaN buffer thickness for GaN-on-LR Si as compared to GaN-on-SI SiC substrates. However, no accurate discussion can be made with regard to these findings, as the material with thicker buffer used in this work (Table 3.3) was rich in obvious surface defects, where the material properties were not successfully characterized (Section 3.8.1).

On the other hand, improvements in the RF performance were expected for thicker GaN buffer thicknesses for GaN-on-LR Si technology. This was attributed to the reduced RF losses following the better isolation from the conductive Si substrates. For RF loss extraction, 0.5 mm-length transmission lines were realized on the mesa etched areas. The RF transmission



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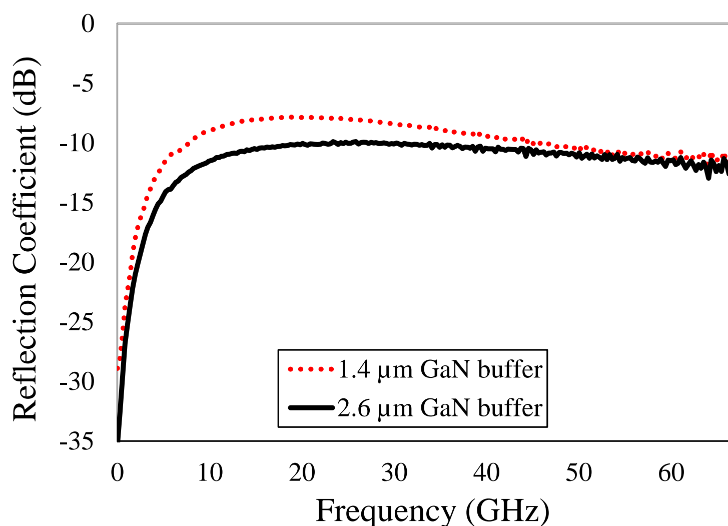

(b)

Figure 3.17: Measured *S*-parameters (without de-embedding) results of 50 Ω transmission media fabricated on GaN-on-LR Si with GaN buffer thicknesses of 1.4 µm and 2.6 µm on the mesa etched areas. (a) Transmission coefficient. And (b) Reflection coefficient.

loss of a 1.4 µm and 2.6 µm buffer thicknesses are indicated in Figure 3.17. It can be seen that both material structures exhibited relatively high RF losses and poor matching characteristics despite the enhancement observed on the material with thicker GaN buffer.

The RF performance of fabricated HEMTs with 1.4 µm and 2.6 µm GaN buffer thicknesses are shown in Figure 3.11 and Figure 3.13. It can be seen that devices with thicker GaN buffer are slightly faster (higher f_T) than those with thinner GaN buffer layer. However, as both devices

have different gate lengths (0.27 μm and 0.3 μm) and epitaxial structures, comparison is difficult. Therefore, more investigation is required on identical devices layouts, fabrication processing and material growth conditions to accurately investigate the effect on GaN buffer thickness on both DC and RF performance. This will be suggested in the future work introduced in Chapter 5.

3.11 Conclusion

The physical electronics and operation of HEMTs have been briefly outlined in this chapter; various parameters and figures of merit of the HEMT characteristics at DC and RF were highlighted. An insight into the RF performance of devices was obtained by utilising the small-signal equivalent circuit model. This was followed by a description of the fabrication steps developed to realise the high-performance GaN-based HEMTs on LR Si in this work. The performance of the developed HEMTs obtained by DC and RF characterisation and applying the equivalent circuit model, where equivalent circuit elements and performance parameters been extracted after de-embedding. From this work, the HEMTs performance is shown to be dependent on layer structure and device layout geometry. Consequently, using proper device layout, using an AlN spacer in the material structure and downscaling the AlGaN Schottky barrier to 9 nm resulted in a maximum f_T of 79.75 GHz and f_{MAX} of 82.5 GHz. The device mm-wave performance has the potential to supply a GaN HEMTs MMIC platform technology on LR silicon at much lower cost than that of GaN on SiC with potential integration with power electronics such as Envelop Tracking techniques and sensors applications [97].

Chapter 4

MMIC Transmission Media and Passive Devices Technology for GaN-on-LR Si

4.1 Introduction

Low loss transmission media technology is key requirement to the realisation of high-quality interconnects and passive elements of integrated circuits operating at mm-wave frequencies. RF substrate coupling is the main cause of performance degradation when considering LR Si as a substrate. Therefore, substrate loss suppression is a crucial step towards the commercialisation of GaN-on-LR Si technology. MMIC transmission media interconnects and passive devices need to be accurately simulated prior to fabrication by 3-D full-wave electromagnetic simulation. In addition, equivalent circuit modelling of passive devices is essential for verification of the developed technology and for MMICs design.

This chapter begins with a brief introduction to the design rules of Microstrip lines and passive components. These include MIM capacitors and on-ship spiral inductors. Simulated and experimental characterisation of these components using the newly-developed transmission media technology will be outlined in the following sections. Equivalent circuit models of microstrip discontinuities, such as MIM capacitors and spiral inductors are also derived from the on-wafer measured *S*-parameters for further loss mechanism analysis. To demonstrate the viability of the technology developed across an ultra-wideband of frequencies, measurements on devices up to 750 GHz are included in this chapter.

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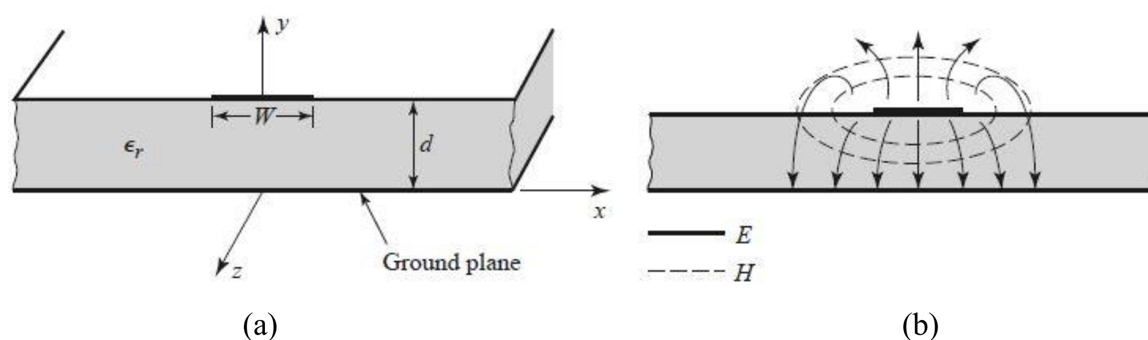
4.2 Design of Passive Components

4.2.1 Microstrip Lines

Among planar transmission media, Microstrip lines are among those most commonly used. This is basically because of the possibility of fabrication using standard optical lithographic process as well as miniaturization and integration to passive and active MMIC devices [98]. In this project, Microstrip, in particular, was adopted as the transmission media because it has lower parasitic modes, higher-power handling capabilities and better field confinement, as compared to CPW [58] [99]. In addition, the Microstrip line technology developed in this project was completely realised on the top of the surface. This means that substrate through holes, ultra-thin substrate and backside wafer processing were not required, as in conventional Microstrip lines [100] [101]. Therefore, system complexity and cost for the realised MMIC circuits can be effectively reduced with enhanced yield.

Figure 4.1a indicates the cross-sectional view of a Microstrip line. It consists of a signal line with a width of (*W*) located on a grounded substrate with a height of (*h*) and relative permittivity of (ε_r) and a ground shield. The substrate thickness of a microstrip is relatively thin, compared to CPW. The field configurations of a Microstrip line are indicated in Figure 4.1 b.



(a) (b)

Figure 4.1: Microstrip transmission line. (a) Structure. And (b) Electrical and magnetic field lines [98].

Microstrip line analysis and behaviour are relatively sophisticated. This is because of the use of non-homogeneous dielectrics around the signal line, where the area on top of the strip *($y > d$)* is air and uncovered by dielectric. The electromagnetic field lines are totally confined in the dielectric region of a Stripline, while they are partially distributed within the dielectric

(substrate) between the signal line and ground shield plate and the air region upon the substrate of a Microstrip line. Therefore, a pure *transverse electromagnetic* (TEM) wave cannot be considered for Microstrip lines because the phase velocity of TEM fields in the dielectric and air regions are different; ($c/\sqrt{\epsilon_\mathrm{r}}$) and c, respectively. Therefore, the assumption of phase-matching condition at the dielectric–air boundaries are applicable. Practically, extra complicated methods are needed to accurately analyse the electromagnetic field of a Microstrip line, which can be considered as a hybrid *transverse magnetic* (TM) - *transverse electric* (TE) wave. However, since the electrical length of the dielectric substrate is particularly thin ($d \ll \lambda$) in the majority of practical applications, the fields are quasi-TEM. Hence, static, or *quasi-static*, solutions lead to an acceptable estimation for the phase velocity (v_P), propagation constant (β), and characteristic impedance (Z_0). Therefore, the phase velocity (v_P) and propagation constant (β) can be written as:

$$v_\mathrm{P} = \frac{c}{\sqrt{\epsilon_\mathrm{r}}} \tag{4.2}$$

$$\beta = k_0 \sqrt{\epsilon_\mathrm{r}} \tag{4.3}$$

$$k_0 = \frac{2\pi f}{c} \tag{4.4}$$

where ϵ_e is the effective dielectric constant of the Microstrip line, which apply the inequality:

$$1 < \epsilon_\mathrm{e} < \epsilon_\mathrm{r} \tag{4.5}$$

This is as a result of the field lines being partially distributed in both the dielectric and air regions. In addition, ϵ_e depends on the substrate dielectric constant, the substrate thickness, the conductor width, and the frequency.

- ***Effective Dielectric Constant***

An approximate expression of the effective dielectric constant of a Microstrip line can be written as follows:

$$\epsilon_e = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12d/W}} \tag{4.6}$$

It can be seen that an equivalent homogeneous medium to the dielectric and air regions of the Microstrip line is assumed to define the dielectric constant for the effective dielectric constant. Therefore, Equations 4.1 and 4.2 can be employed to obtain the phase velocity and propagation constant.

- ***Characteristic Impedance***

The characteristic impedance approximation depends on the Microstrip lines dimensions as follows:

$$Z_0 = \begin{cases} \dfrac{60}{\sqrt{\epsilon_e}} \ln\left(\dfrac{8d}{W} + \dfrac{W}{4d}\right) & for \dfrac{W}{d} \leq 1 \\ \dfrac{120\pi}{\sqrt{\epsilon_e}\left[\dfrac{W}{d} + 1.393 + 0.667\ln(\dfrac{W}{d} + 1.444)\right]} & for \dfrac{W}{d} \geq 1 \end{cases} \tag{4.7}$$

The ration (W/d) can be written for a known characteristic impedance (Z_0) and dielectric constant (ϵ_r) as follows:

$$\frac{W}{d} = \begin{cases} \dfrac{8e^A}{e^{2A} - 2} & \text{for} \dfrac{W}{d} < 2 \\ \dfrac{2}{\pi}\left[B - 1 - \ln(2B - 1) + \dfrac{\epsilon_r - 1}{2\epsilon_r}\left\{\ln(b - 1) + 0.39 - \dfrac{0.61}{\epsilon_r}\right\}\right] & \text{for} \dfrac{W}{d} > 2 \end{cases} \tag{4.8}$$

where

$$A = \frac{Z_0}{60}\sqrt{\frac{\epsilon_r + 1}{2}} + \frac{\epsilon_r - 1}{\epsilon_r + 1}\left(0.23 + \frac{0.11}{\epsilon_r}\right) \tag{4.9}$$

$$B = \frac{377\pi}{2Z_0\sqrt{\epsilon_r}} \tag{4.10}$$

- ***Attenuation***

The attenuation constant as a result of dielectric loss (α_d) can be evaluated based on the assumption that a Microstrip line is a quasi-TEM line as follows:

$$\alpha_{\mathrm{d}} = \frac{k_0 \epsilon_{\mathrm{r}} (\epsilon_{\mathrm{e}} - 1) \tan \delta}{2\sqrt{\epsilon_{\mathrm{e}}}\, (\epsilon_{\mathrm{r}} - 1)} \; N_{\mathrm{p}}/m \tag{4.11}$$

where $\tan \delta$ is the loss tangent of the dielectric substrate. Therefore, parasitic modes, including surface waves and space modes are the main source of dielectric loss, which is directly proportional to frequency.

The attenuation following the conductor loss (ohmic loss), α_{c} can be determined as a function of surface resistivity and the line inductivity. This is basically affected by the skin depth(σ), resulting in an increase in the effective resistance of the conductor when frequency increases. The skin depth in terms of frequency, resistivity and relative permeability of the conductor, can be expressed as:

$$\sigma = \sqrt{\frac{\rho}{\pi f \mu}} \tag{4.12}$$

where f is the frequency of operation, ρ is the bulk resistivity, and $\mu = \mu_0 \mu_{\mathrm{r}} = 4\pi \times 10^{-7}\ F/m$ is its absolute permeability. As a rule of thumb, this loss can be minimised by having a conductor thickness of 4 to 5 times the skin depth [102].

4.2.2 Metal-Insulator-Metal (MIM) Capacitor

In most RF applications, capacitors are considered as the main passive components. They are widely used in filter circuits, coupling circuits, DC block circuits, RF bypass circuits, impedance matching networks and resonators [103] [104]. Interdigitated capacitors and MIM capacitors are the most commonly used capacitors in MMIC circuits. MIM capacitors have the advantage of producing larger capacitance values over interdigitated capacitors. This means MIM capacitors can be adapted for DC bypass circuits. For example, capacitance values of

only a few pF can be obtained using the interdigitated capacitor, whereas, MIM capacitors can easily introduce a capacitance value as high as 20 pF [102]. Therefore, only MIM capacitors were considered for this work. A MIM capacitor consists of a dielectric layer sandwiched between two metal plates. The layouts of series and shunt MIM capacitors in MMIC design are shown in Figure 4.2.

It can be seen that there is a dielectric layer sandwiched between the input and output signal tracks in the series connection. However, in the parallel connection, the input and output tracks are connected directly above a dielectric layer deposited on a bottom metal plate connected to the ground. Equation 4.12 provides an empirical driven formula of the capacitance value of a MIM structure including fringing term:

$$c = \epsilon_0 \epsilon_r \frac{W_{\mathrm{Cap}} L_{\mathrm{Cap}}}{d_{\mathrm{Cap}}} + 4.8 \times 10^{-5}\, W_{\mathrm{Cap}} L_{\mathrm{Cap}} \tag{4.13}$$

where ϵ_0 is the free space permittivity, ϵ_r is the dielectric permittivity, W_{Cap} and L_{Cap} are the width and length of the plate, respectively, and d_{Cap} is the dielectric thickness or the vertical distance between the top and bottom metal plates.

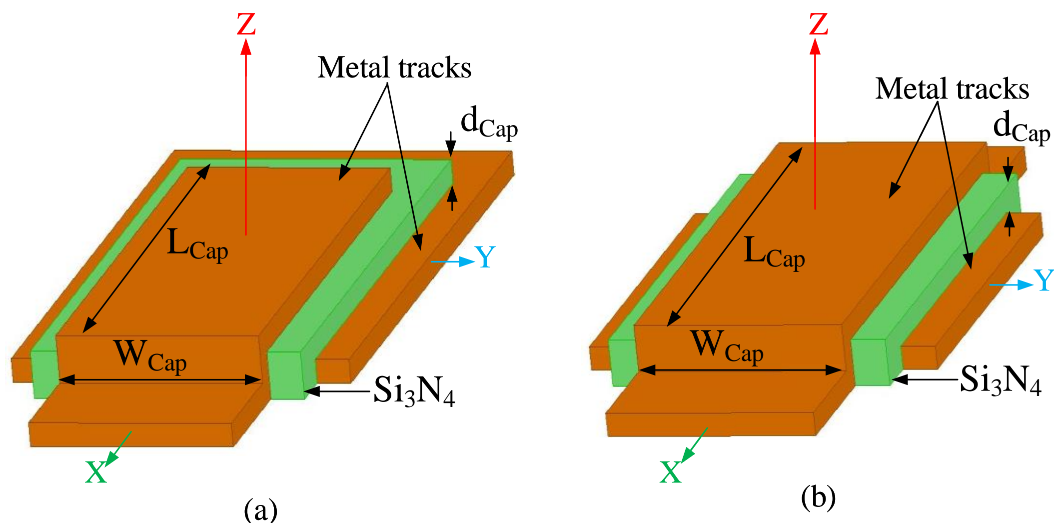


Figure 4.2: Layout of in-line MIM capacitors. (a) Series. And (b) Shunt.

- ***High-Frequency Electrical Model***

Since the dimensions of MIM structure are comparable to those of the employed wavelength at microwave frequencies, the assumption of MIM capacitor as lumped components can be applied [105] [106]. The equivalent circuit model is essentially required for better understanding of the behaviour of a MIM capacitor, particularly at higher frequencies bands. The equivalent-circuit parameters values were extracted based on the measured *S*-parameters [58].

Figure 4.3a shows the equivalent circuit model of the series MIM capacitor. C_{M1} and C_{M2} represent the coupling capacitances between the top and bottom of the substrate. The R_{Cap} and the R_{Series} correspond to the parasitic loss of the capacitor plates. C_{Eff} is the effective capacitance value of the MIM capacitor. The equivalent circuit model of the shunt MIM capacitor (shown in Figure 4.3b) is relatively simple and contains fewer parasitic elements than that of series MIM capacitor. It consists of R_{Cap} and R_{Grad} which correspond to the capacitor plate and through-hole (connection to ground), respectively. The parasitic substrate resistance and capacitance (account for substrate coupling) were not needed in this work due to the use of complete shielding ground planes, where the conductive substrate was fully isolated. However, these parasitics would be essential if the MIM capacitors were employed directly on the substrate. Finally, transmission lines were integrated into the model which accounted for line losses for a specified length.

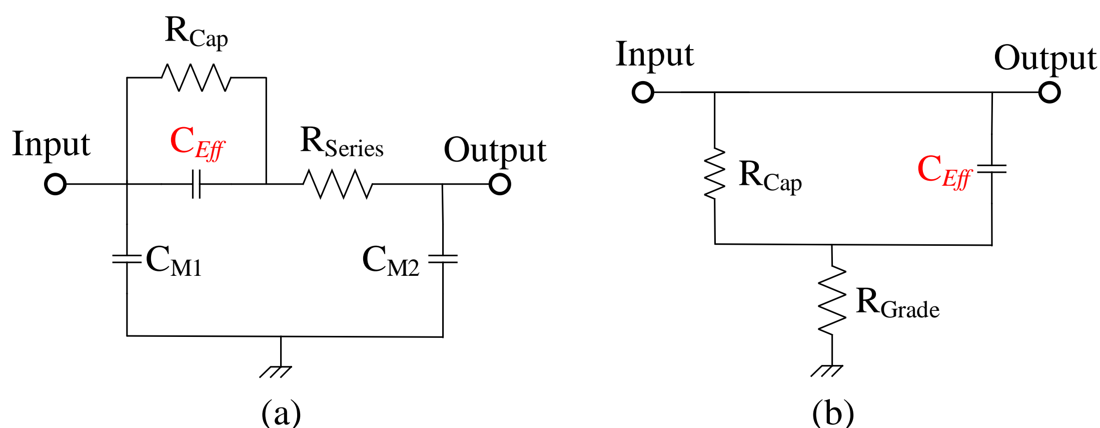


Figure 4.3: Equivalent circuit model of (a) Series MIM capacitor. And (b) Shunt MIM capacitor [58] [107].

4.2.3 On-chip RF Spiral Inductors

The yield of a MMIC circuit and chip cost are noticeably determined by the performance of the on-chip inductors. Therefore, it is considered as a main passive component that can be used in various circuits, such as matching networks, baluns and inductive loads. Obtaining precise inductance value (L), high-self-resonance frequency (SRF), high quality-factors (Q-factor), and small layout areas are of a great importance for the realisation of an on-chip inductor [108].

Among on-chip inductors, spiral inductors are the most widely adopted structures. Generally, they can be designed as rectangular or circular layout structures. The advantage of rectangular spiral inductors is that they can be easily designed and fabricated. However, circular spiral inductors yield higher efficiency and better performance at the cost of complex design layout design and challenging fabrication process [109]. Figure 4.4 shows the general layout of circular and rectangular spiral inductors. The performance of inductors can be effectively affected by different design parameters, such as width of spiral turns (W), separation between the turns (S), number of turns (N), outer and inner diameters of the inductor (D_{in} and D_{out}, respectively) and the thickness of the metal (t_m) [110].

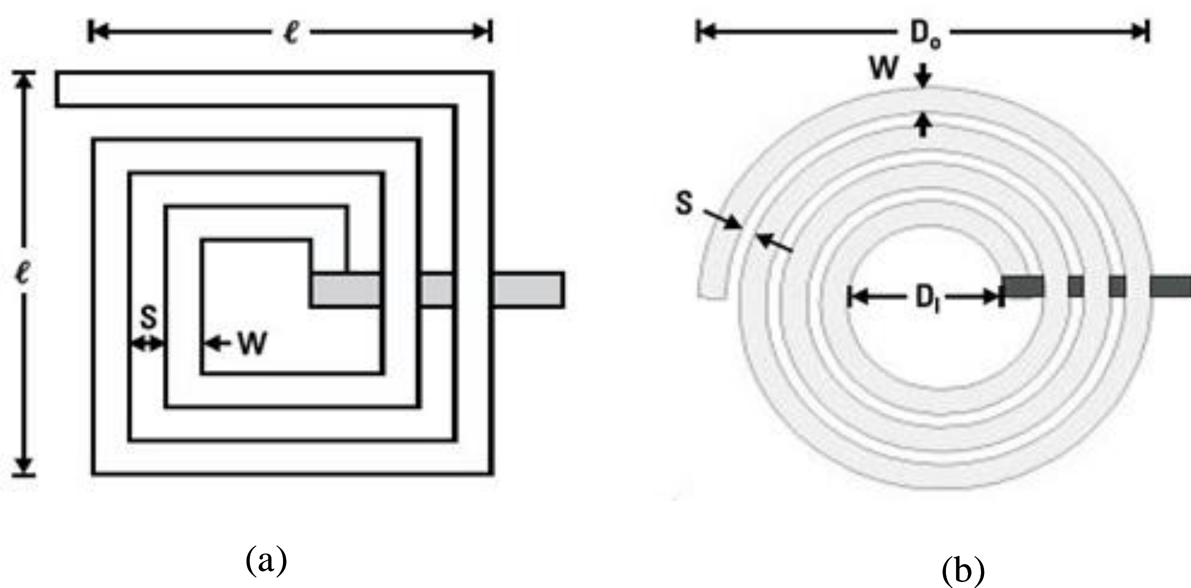


Figure 4.4: Geometry of spiral inductors (a) Rectangular. And (b) Circular [12].

- ***High-Frequency Electrical Model***

An equivalent circuit model is needed to obtain better interpretation of the performance/loss mechanisms of the inductors, particularly at high frequency ranges (beyond X-band). Generally, an inductor model can be quickly developed based on its measured *S*-parameters. This type of inductor modelling has the advantage of providing precise yields but it could be only valid for a specific device measurements. Computer optimization is employed to extract the parameter of the equivalent circuit model [111].

Figure 4.5 indicates the topology of the model employed in this work, which is similar to that proposed in [112] [113]. L_{Prime} is the spiral inductance; R represents the series resistance due to conductor loses; R_S and L_S are the resistance and inductance associated with skin depth, respectively; C_P is mainly due to the overlap between the spiral and the underpass and the capacitive coupling between two adjacent spiral tracks; C_{d1} and C_{d2} represent the total capacitance between the spirals and conductive Si substrate; and R_{Sub1}, C_{Sub1}, R_{Sub2} and C_{Sub2} are substrate parameters.

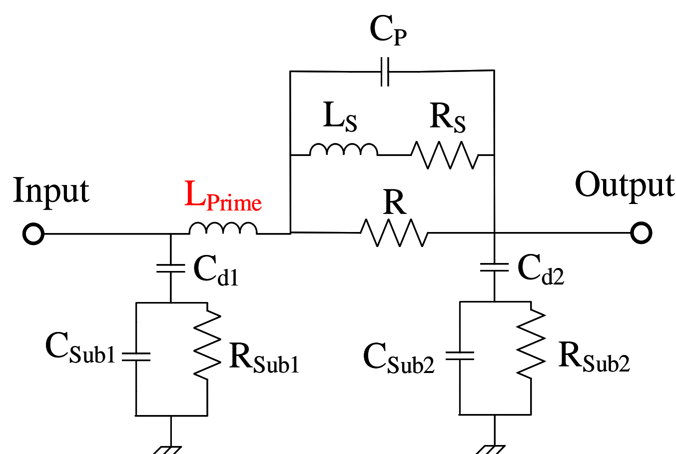


Figure 4.5: Schematic of the equivalent circuit model for a spiral inductor.

- ***Characterisation of Spiral Inductors***

Q-factor, inductance, and Self-Resonance Frequency (SRF) are the most commonly used parameters as figures of merit for spiral inductor characterisation. The inductor performance is then evaluated based on these parameters.

1- Quality-Factor:

Q-factor can be defined in different ways; where the ratio of energy storage to the energy loss per cycle in the device is considered the most common expression [114]. It can be evaluated for a spiral inductor as follows [115]:

$$Q = \frac{Im\left(\frac{1}{Y_{11}}\right)}{Re\left(\frac{1}{Y_{11}}\right)} = -\frac{Im\,(Y_{11})}{Re\,(Y_{11})} \tag{4.14}$$

where Y_{11} is the input admittance that is extracted directly from the measured two port *S*-parameters.

2- Inductance.

The energy stored as function of the inductance is one more critical parameter used for inductor performance characterisation. The inductor can be defined as the ability to store energy in the magnetic field when passing the current through the inductor [110]. The inductance value (L) is inversely proportional to frequency. Because of the current crowding at the edges of the conductors, the inductance value is physically reduced as frequency is increased. This is as a result of the reduction in the internal inductance. On the other hand, the situation is different for on-chip spiral inductors, where the coupling capacitance dramatically increases the effective inductance value. Consequently, inductance L is directly proportional to frequency. Equation 4.14 is used to evaluate the induction value, L [116]:

$$L = \frac{Im\left(\frac{1}{Y_{11}}\right)}{2\pi\, f} \tag{4.15}$$

3- Self-Resonance Frequency.

The distribution characteristics of metal traces and substrate parasitic effects cause resonance at a specific frequency, called SRF. Since the reactance of the inductor becomes negative beyond the SRF, the inductor acts as a capacitor. Therefore, the operational frequency must be

chosen to be smaller than the SRF of the inductor. The inductive reactance is identical to the parasitic capacitive reactance at resonance frequency. The impedance peak value (|Z|) determines the SRF. Alternatively, the SRF can be identified from the Q-factor curve as the frequency at which Q-factor is equal to 0.

4.3 Modelling and Measurements

On-wafer measurements of small-signal *S*-parameter were carried out using an Agilent PNA network analyser (E8361A) over the range 0.1-67 GHz. The system was calibrated using SOLT calibration technique based on an off-chip ISS impedance standard [88]. 50 µm-pitch Picoprobes were used to probe the CPW-transition parts located at either end of the fabricated transmission lines and passive components. The samples were placed on a thick quartz spacer to eliminate any possible parasitic substrate modes caused by the metal chuck.

Simulations were carried out using two different commercial simulators; a 3-D full-wave electromagnetic simulation tool, Ansoft HFSS™ and also Agilent ADS 2016. The prefabricated transmission media and passive components technology were designed and simulated using Ansoft HFSS. Accurate optimisation of the multi-layer structures and layout dimensions were needed during the design for optimum device performance and to ensure the suppression of RF energy dispersion introduced by the conductive substrate. In addition, the equivalent circuit model of the realized MIM capacitors and spiral inductors was extracted using Agilent ADS. This was employed to extract the actual capacitance and inductance values and device parasitics values for additional losses mechanism analysis.

4.4 Novel Transmission Media Technology

In this work, novel shielded and shielded-elevated transmission media technology was introduced for eliminating substrate coupling effect associated with the conductive Si substrate. Two structure designs were realised on GaN-on-LR Si substrate providing almost complete isolation from the conductive substrate, by employing a ground plane, a 5 µm-thick benzocyclobutene (BCB) and elevated line traces on air. The shielded (S)-Microstrip and shielded-elevated (SE)-Microstrip lines developed in this work are illustrated in Figure 4.6.

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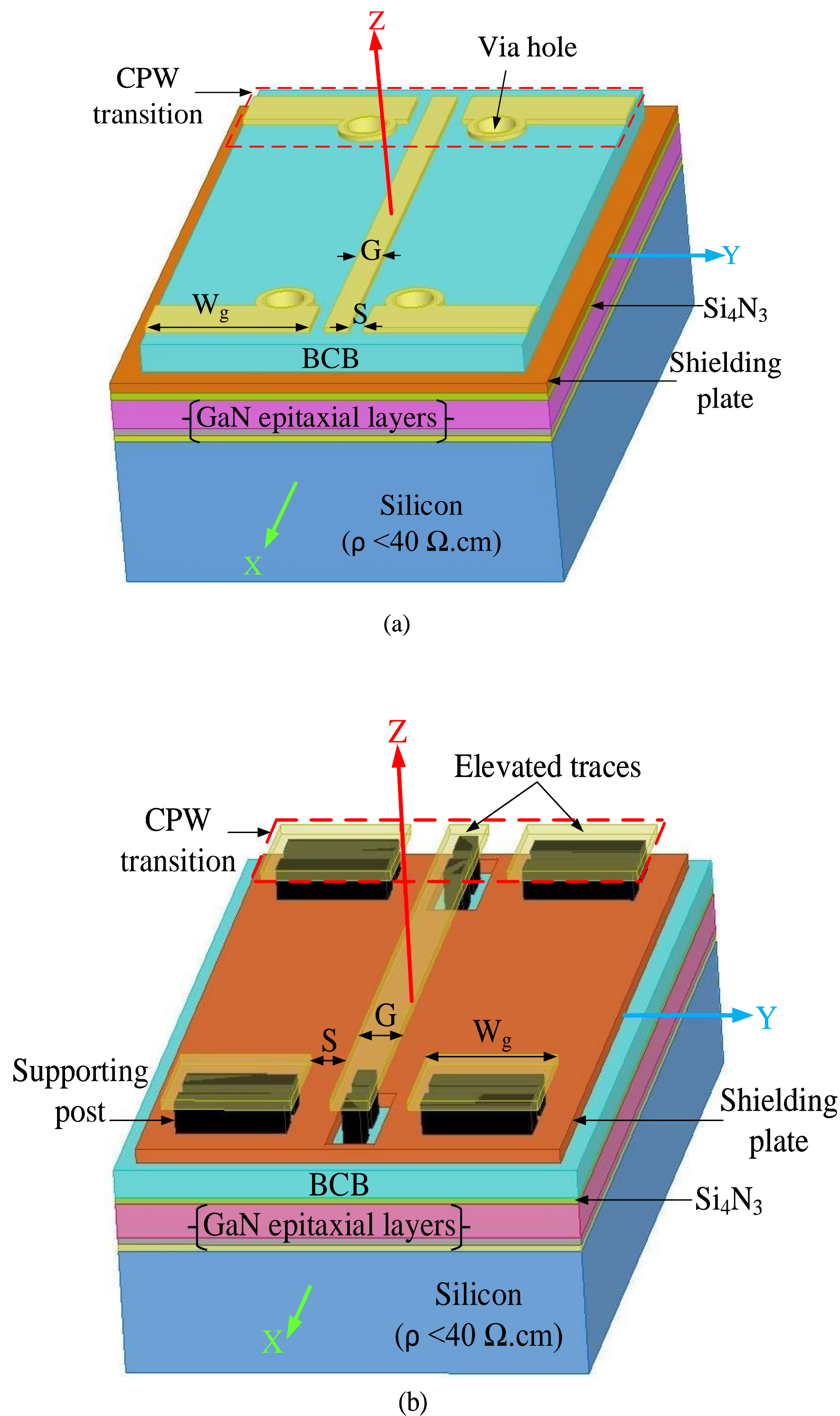
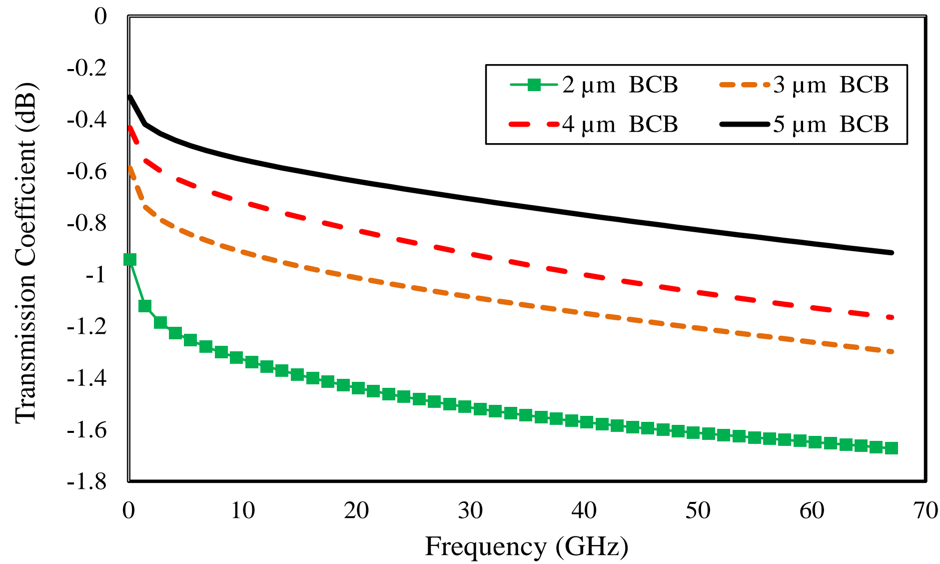


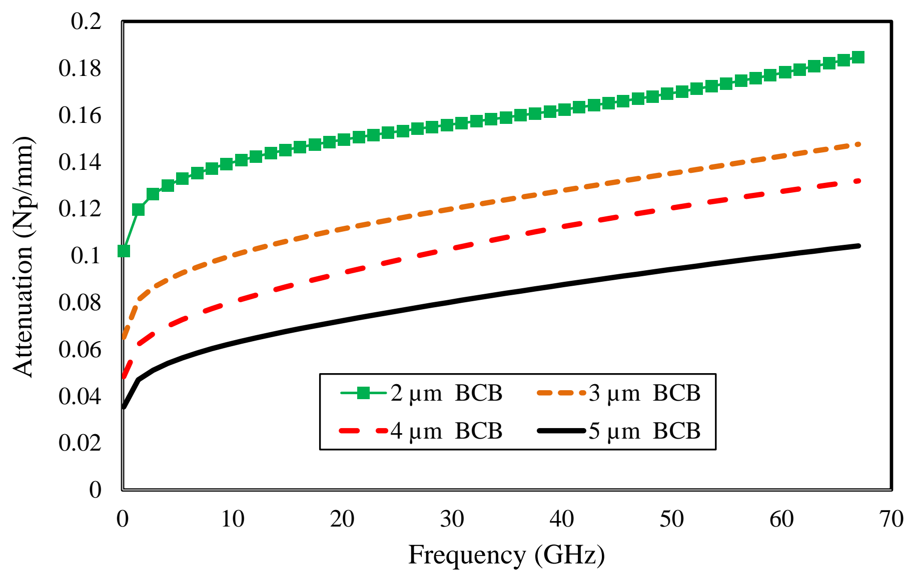
Figure 4.6: Oblique projection of the fabricated 1 mm-length 50 Ω lines (a) S-Microstrip line with $S = 4.5$ µm and $G = 13.2$ µm. And (b) SE-Microstrip lines with $S = 9$ µm, $G = 20$ µm, $Wg = 100$ µm.

4.4.1 Influence of Design Parameters

The effect of the technological parameters including BCB thickness and elevation height was carried out for the prefabricated 1mm-length 50 Ω transmission media technology. The study was done on the Ansoft HFSS simulation, taking into account the fabrication capabilities available for the realisation of reliable MMIC-integration technology.



(a)



(b)

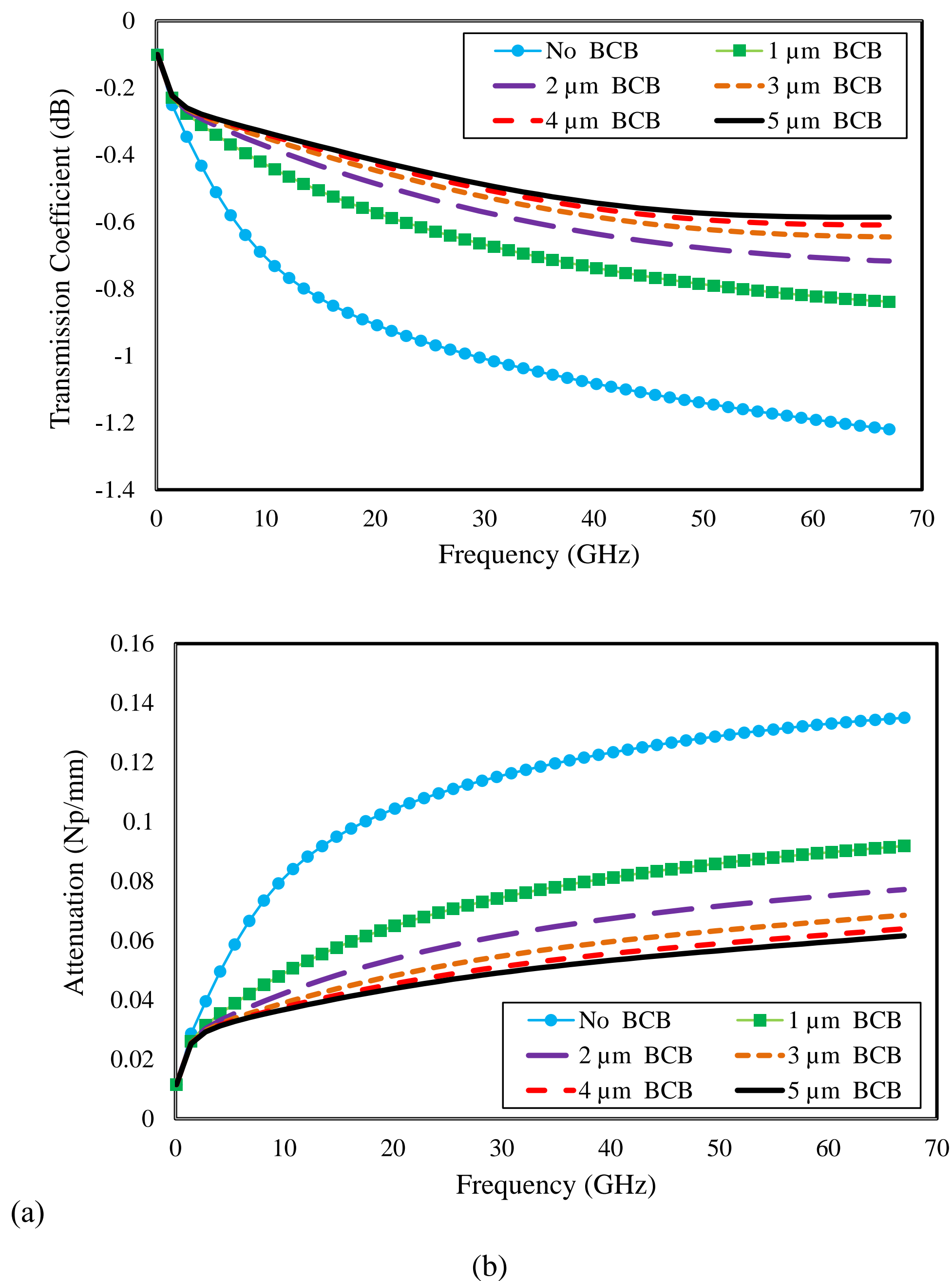
Figure 4.7: Effect of BCB thickness on S-Microstrip lines (a) Transmission coefficient. And (b) Attenuation.

1- Shielded-Microstrip Transmission Media.

Figure 4.7 shows the effect of BCB thickness on the performance of S-Microstrip transmission media. It is clear that losses can be reduced by increasing the BCB thickness over the whole frequency range. A reduction in transmission losses, S_{21} and attenuation, α of nearly 45 % at 67 GHz is obtained when increasing the BCB height from 2 µm to 5 µm, respectively. This increase in losses is attributed to the reduction in parasitic capacitance between the line track and ground plane [117] [118]. However, the maximum applicable BCB thickness is 5 µm, which is limited to fabrication capabilities and yield. This is because thicker BCB layers have poor surface uniformity, as well as possible difficulties in creating successful through-holes connections through the BCB for device integration when considering the realisation of MMIC-circuits, and could cause additional parasitic inductance.

2- Shielded-Elevated Microstrip Transition Media.

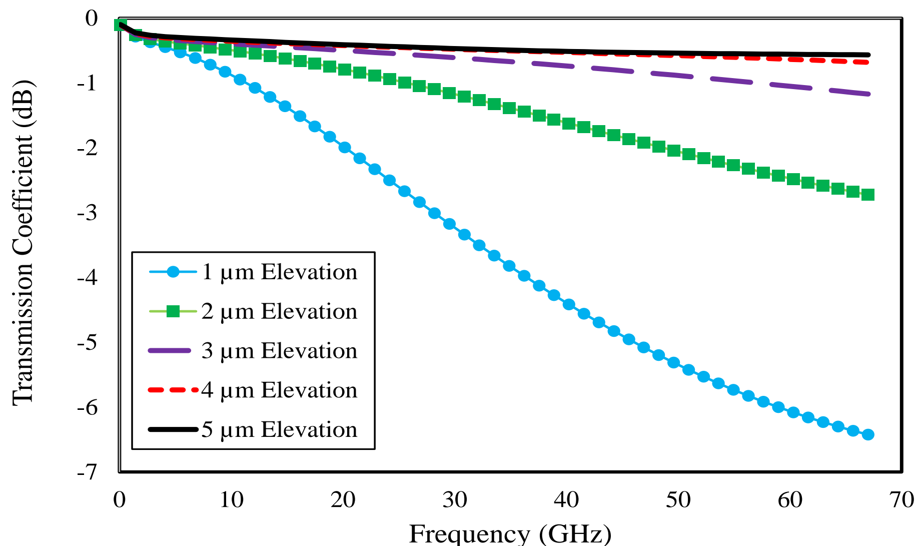
As the SE-Microstrip structure requires the use of ground holes in the shielding plate, there are small areas in the shielding plate in which the Microstrip signal trace is in direct contact with the lossy substrate. Losses depend directly these exposed areas (ground holes) especially at a higher frequency range, where the wavelength dimensions become comparable to the substrate exposed area at the base of the air-bridge support. To overcome this, the SE-Microstrip lines were fabricated on top of a dielectric layer of BCB. The effect of BCB thickness on SE-microstrip lines was initially investigated, as shown in Figure 4.8. An elevation height of 5 µm was fixed during simulation. It can be seen that the loss is dramatically decreased when employing thicker BCB layers up to 4 µm, where S_{21} and α were improved by 55 % and 53 %, respectively. However, losses are slightly reduced when increasing the BCB thickness beyond 4 µm, indicating a complete isolation of the Silicon substrate. A BCB thickness of 5 µm was therefore chosen, not only to ensure a full substrate shielding but also to enable the integration of the SE-Microstrip lines for MMIC circuit applications.



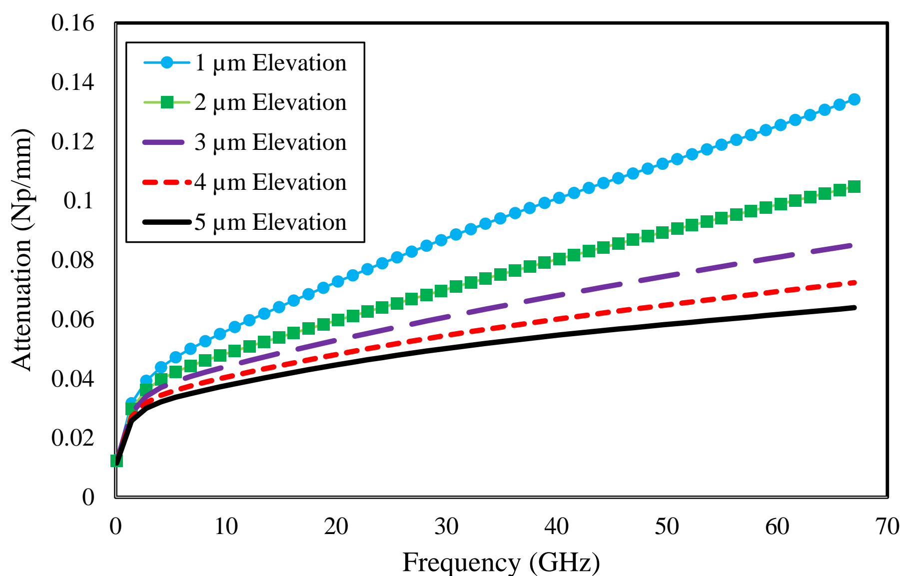
(b)

Figure 4.8: Effect of BCB thickness on SE-Microstrip line (a) Transmission coefficient. And (b) Attenuation.

Elevation height is another critical parameter affecting the performance of the prefabricated SE-Microstrip lines. Figure 4.9 shows the simulation results of SE-Microstrip lines with BCB thickness of 5 µm and varying elevation heights (from 1 to 5 µm). At frequencies beyond 8 GHz, losses are steeply reduced when the elevation height is increased from 1 µm up to 3 µm,



(a)



(b)

Figure 4.9: Effect of elevation height on SE-Microstrip line (a) Transmission coefficient. And (b) Attenuation.

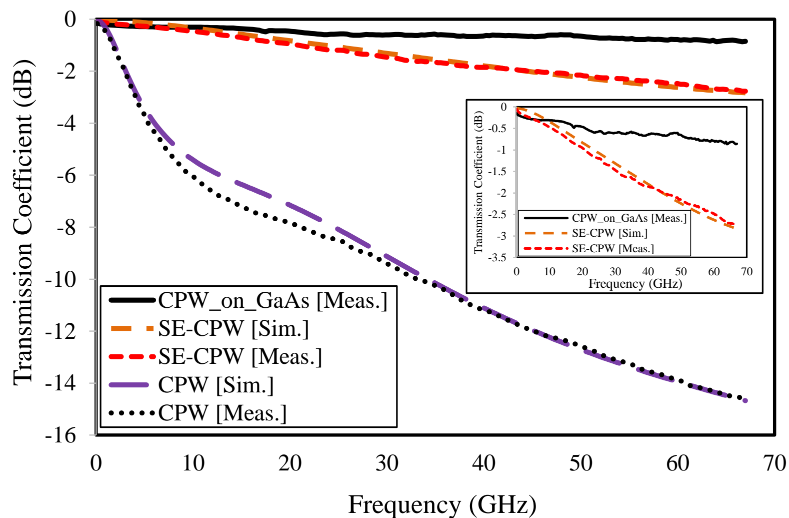
where S_{21} and α were improved by 88 % and 36 %, respectively. This is because of the increased overall parasitic capacitance between the Microstrip line track and ground plane, particularity at the holes located in the ground plane [117]. Moreover, elevation heights of greater than 3 µm were found to be enough to isolate the lines from the conductive Si substrate. Therefore, an elevation height of approximately 5.5 µm was chosen to the developed SE-Microstrip lines during this work.

4.4.2 Results and Discussion.

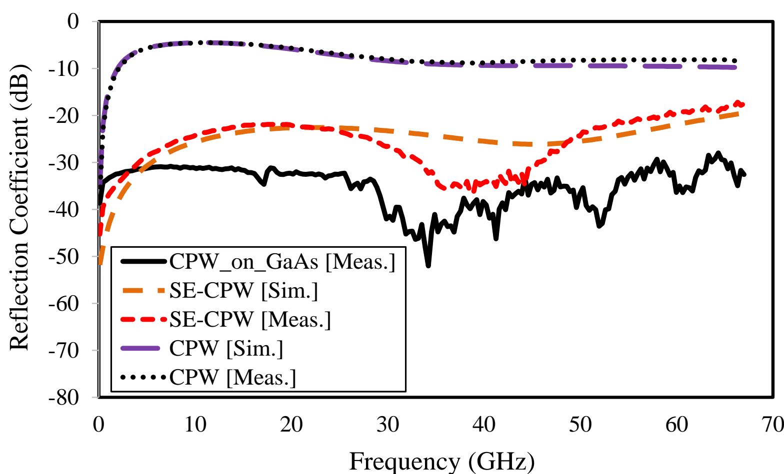
- ***Silicon Substrate Coupling Effect***

The effect of the conductive Si substrate on losses was initially investigated by comparing the measured and simulated data of conventional CPW fabricated directly on the substrate with that of a shielded-elevated (SE)-CPW line between 0.1 GHz and 67 GHz. Measured and simulated *S*-parameters were in very close agreement, as shown in Figure 4.10. It is clearly seen that the effect of the conductive substrate was dominant, even at low frequencies, for conventional CPW lines. As all the CPW traces are in direct physical contact with the substrate, most of the E-field was coupled into the conductive substrate even when employing a thin Si_3N_4 insulating layer and GaN buffer layers. The losses are mainly the result of two phenomena: one is capacitive coupling which allows the flow of conduction current not only through the metal strips but also through the lossy substrate contact areas. The other reason is inductive coupling which induces current loops and associated losses by penetration of the magnetic field through the lossy Si substrate. Losses continued to increase over the whole frequency band, reaching a maximum of more than 14 dB at 67 GHz. On the other hand, by using an SE-CPW structure, improvements of the line performance (up to 12 dB) over a conventional CPW line can be achieved. Losses also increase gradually over the entire band for the SE-CPW line, as shown in Figure 4.10a.

Not only did SE-CPW introduce improvements in terms of transmission losses (S_{21}), but it also provided acceptable matching, with as low as -22 dB/mm return loss, and more than 20 dB/mm reduction over a conventional CPW line. Moreover, the resonant frequency was shifted by nearly 5 GHz using the proposed transmission media. Consequently, SE-CPW lines mitigated the unwanted in-band resonances, as shown in Figure 4.10b. Figure 4.10c clearly shows that the attenuation constant rose steeply to very high values for conventional CPW lines; 1 NB/mm at 76 GHz. However, a reduction in the attenuation constant of more than 0.6 Np/mm was obtained using the SE-CPW structure, as a result of the electrical isolation of the signal trace from the bottom ground plane and the substrate. However, there are small areas in the lower ground where the line is in physical contact with the substrate and the supporting posts are in physical contact with the substrate by exposed rectangular areas in the lower ground plane bond pad layer. This is why the SE-CPW line had a slightly larger attenuation



(a)



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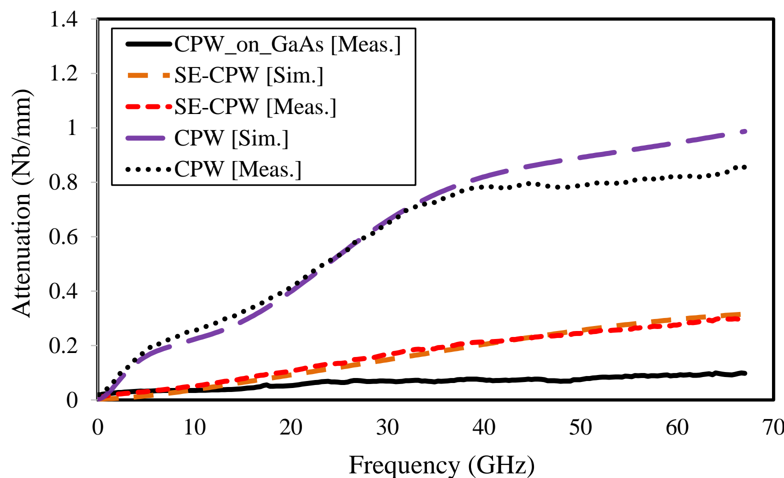


(c)

Figure 4.10: Measured and simulated *S*-parameters results of conventional CPW and SE-CPW lines. (a) Transmission coefficient, S_{21}. (b) Reflection coefficient, S_{11}. (c) Attenuation, α.

constant (about 0.2 NB/mm) compared to that of CPW-on-GaAs line at K-band.

- ***Novel Transmission Media Technology***

Figure 4.11 shows the RF performance of the developed transmission media for RF GaN-on-LR Si substrates MMIC applications. The performance achieved is comparable with that of traditional CPW on SI substrates and better than that of SE-CPW using air as a spacer on LR Si substrates. Clearly from the measured results, shown in Figure 4.11a, the developed technology (S-Microstrip and SE-Microstrip) exhibited an excellent RF performance of transmission loss of better than 0.9 dB/mm and 0.6 dB/mm at 67 GHz, respectively. Furthermore, the measured results obtained have been verified by the very close agreement between measured and simulated *S*-parameters. As shown in Figure 3.11a, the proposed, newly developed SE-Microstrip transmission media, exhibited the least losses - better than that of the standard CPW on SI substrate and SE-CPW lines. This indicates the almost complete isolation of the conductive substrate and, where virtually no conduction current flows, induced current loops or associated losses were allowed through the lossy substrate.

Moreover, it is clearly shown in Figure 4.11a that the effect of the conductive substrate was still noticeable for the SE-CPW lines fabricated on thin Si_3N_4 layer above the lossy substrate. The losses are mainly because the E-field was partially coupled onto the conductive substrate even whilst employing a thin Si_3N_4 insulating layer, which was used to suppress the DC leakage current [119]. This is because of the small areas in the lower ground plane in which the line is in physical contact with the lossy substrate. In Figure 4.11b, a reflection coefficient of less than -18 dB over the full band shows that the fabricated transmission media were well-matched to a characteristic impedance, Z_0, of 50 Ω. The best matched line was the S-Microstrip line, where a reflection coefficient of less than -29 dB was achieved. This is a clear indication of the high-quality fabrication yield with uniform BCB surface and well-controlled thickness, which determines the characteristics impedance, Z_0, of the line [120]. Moreover, the resonant frequency was further shifted when BCB was employed, indicating the mitigation of undesirable in-band resonances and ensure single-mode propagation for the fabricated microstrip lines.

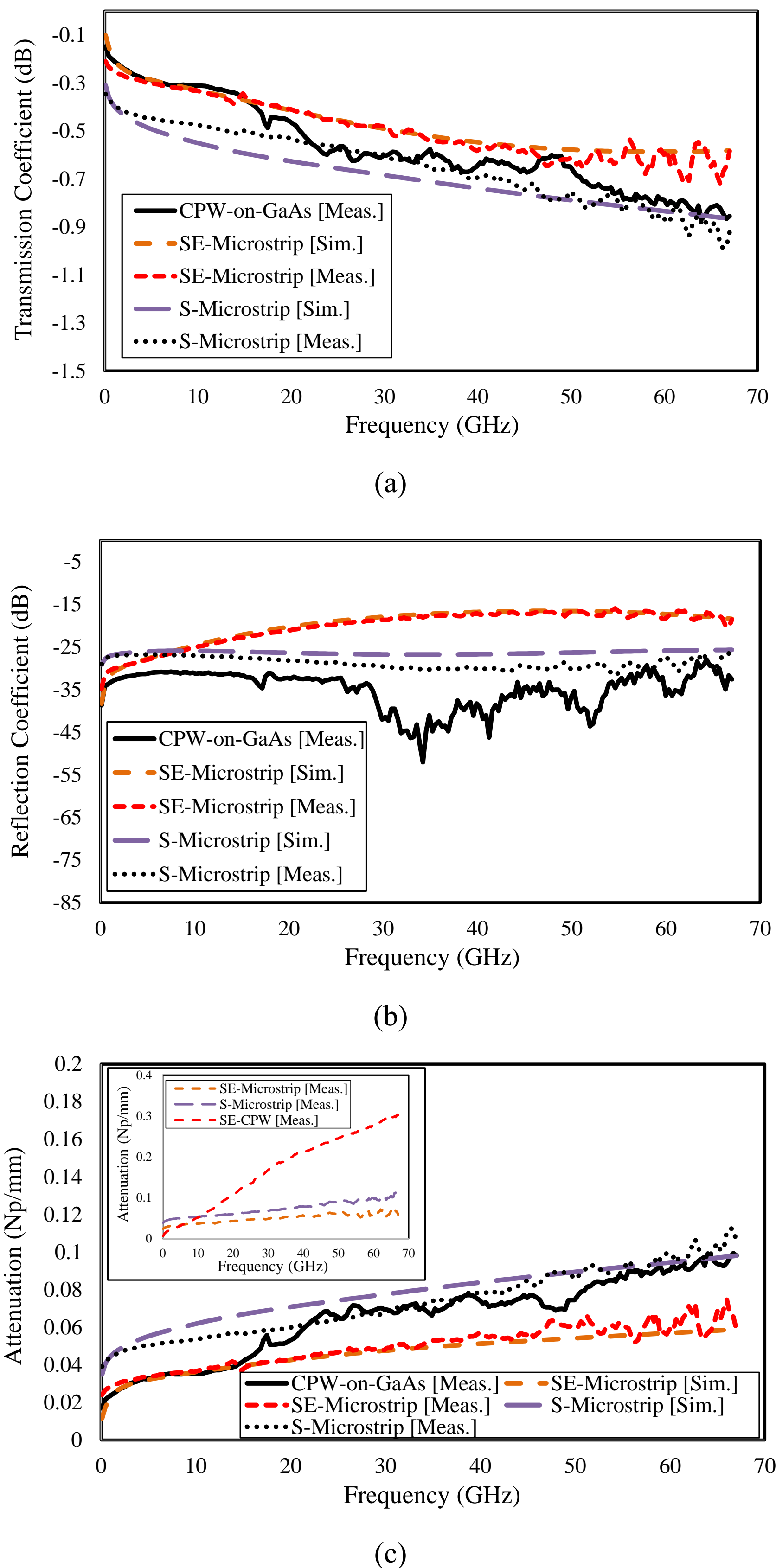


Figure 4.11: Measured and simulated *S*-parameters results of SE-CPW, S-Microstrip, SE Microstrip lines on GaN-on-LR Si and CPW-on-GaAs lines. (a) Transmission coefficient, S_{21}. (b) Reflection coefficient, S_{11}. (c) Attenuation, α

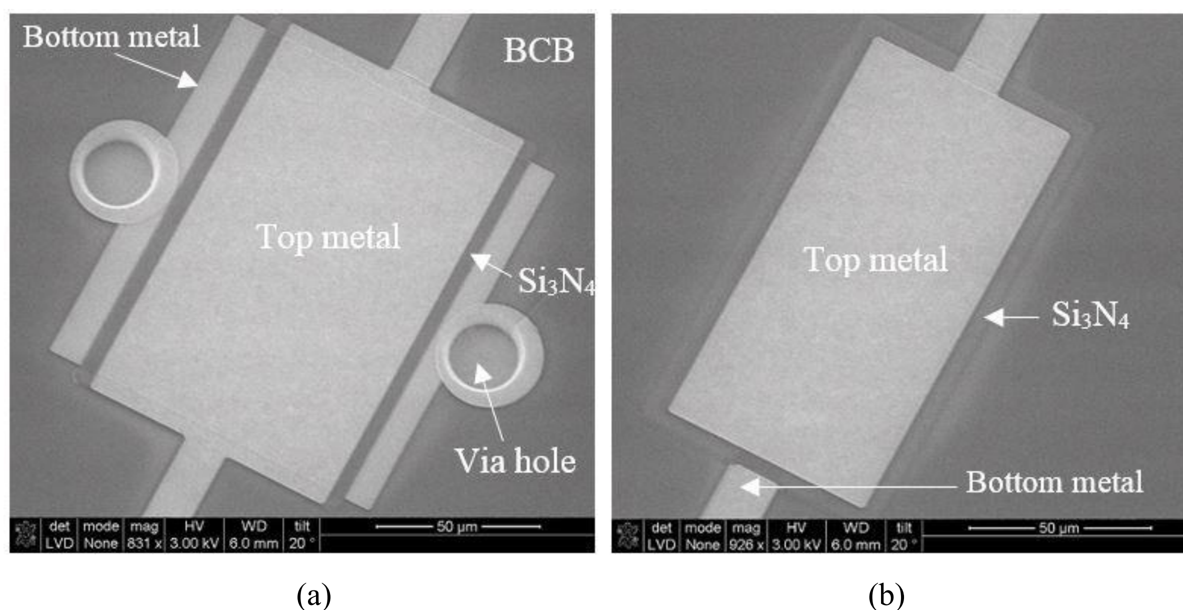
Attenuation constant (α) extracted from the measured *S*-parameters of the developed transmission media technology is shown in Figure 4.11c. It is clearly shown that the attenuation constant rose steeply to 0.3 dB/mm for the SE-CPW at 67 GHz. An improvement of more than 65 % can be obtained using the proposed S-Microstrip lines. However, S-Microstrip lines have a slightly larger attenuation constant of 0.06 Nb/mm up to X-band frequencies, whereas it is comparable to that of SI GaAs substrate over the rest of the frequency range. SE-Microstrip lines achieved the lowest attenuation constant values and almost flat response over the whole frequency band with $\alpha < 0.06$ Nb/mm.

The developed method using BCB significantly enhances the performance of the transmission line especially at high frequencies where the gap dimensions of the ground plane at the CPW signal line posts become comparable to the signal wavelength.

4.5 Low-loss MIM Capacitors

To prove the capabilities and efficiency of the developed transmission media technology, low-loss in-line MIM capacitors were realized using the developed S-Microstrip technology. However, the substrate losses including the magnetic and electric loss were major losses of the RF MIM capacitors at high frequencies as a result of the high conductivity of the Si substrate. The opposing current induced in the substrate because of the variable magnetic field penetrating the substrate causes the magnetic loss of MIM capacitors. The electric loss originates from electric coupling between the electrodes and the conductive substrate depending on the insulator between them and the parasitic electric field in the substrate [105]. Therefore, in-line shunt and series MIM capacitors were realised using the proposed S-Microstrip technology to mitigate these issues.

In this work, all capacitors used a 200 nm Si_3N_4 as a dielectric, which has a relative permittivity of approximately 6.7. SEM images of the fabricated series and shunt MIM inductors are shown in Figure 4.12. The shunt capacitors were connected to ground (shielding plate) using a via-hole through the BCB layer.



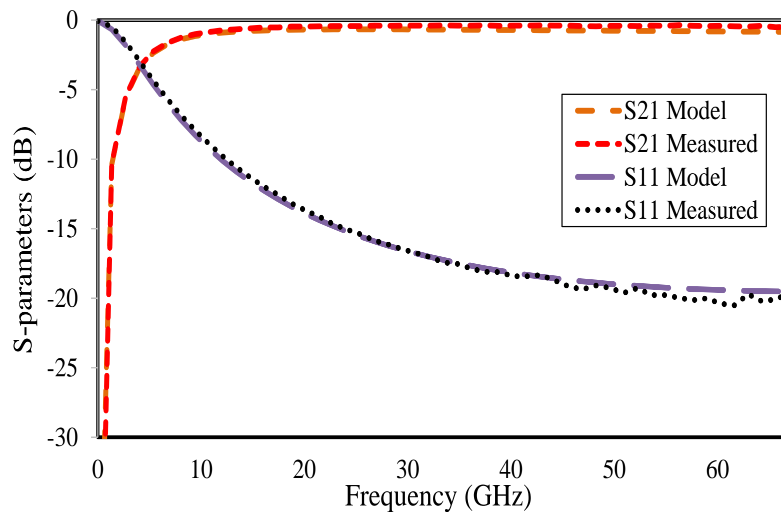
(a) (b)

Figure 4.12: SEM images of the fabricated in-line (a) Series. And (b) Shunt MIM capacitors using S-Microstrip transmission media technology.

4.5.1 Results and Discussion

Measured and modelled *S*-parameter results of the fabricated series and shunt MMIC capacitors are shown in Figure 4.13 and Figure 4.14, respectively. It can be seen that the modelled and measured *S*-parameters are in good agreement, which verifies the utilised equivalent circuit model of the capacitors. The capacitor area is (20×60 μm^2) for both series and shunt capacitors. Line parasitics were not de-embedded from the measured data to avoid over-estimating the losses following the *Z*-parameter de-embedding [121].

As shown in Figure 4.13, using the developed S-Microstrip technology, the coupling between the capacitor and Si substrate for the series capacitor was negligible, where an insertion loss of less than 0.5 dB at 67 GHz was obtained. In addition, an insertion loss of less than 0.8 dB was achieved up to V-band frequencies for the shunt capacitor, as shown in Figure 4.14. Therefore, by using the S-Microstrip technology, the RF performance of the fabricated MIM capacitors was improved together with reliable and simple fabrication processes.



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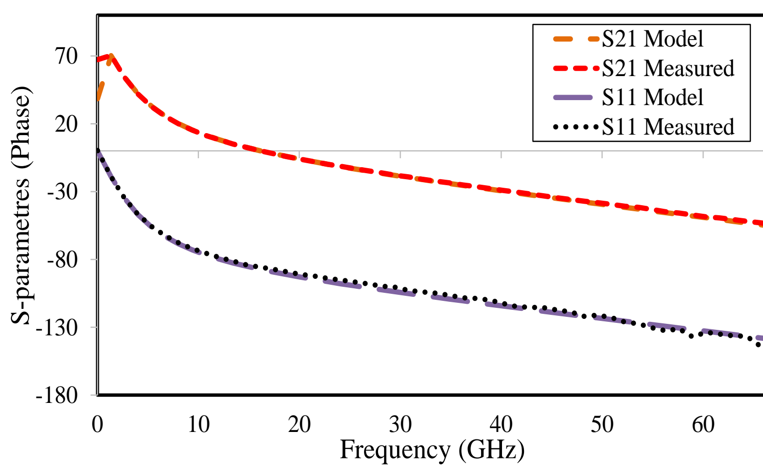
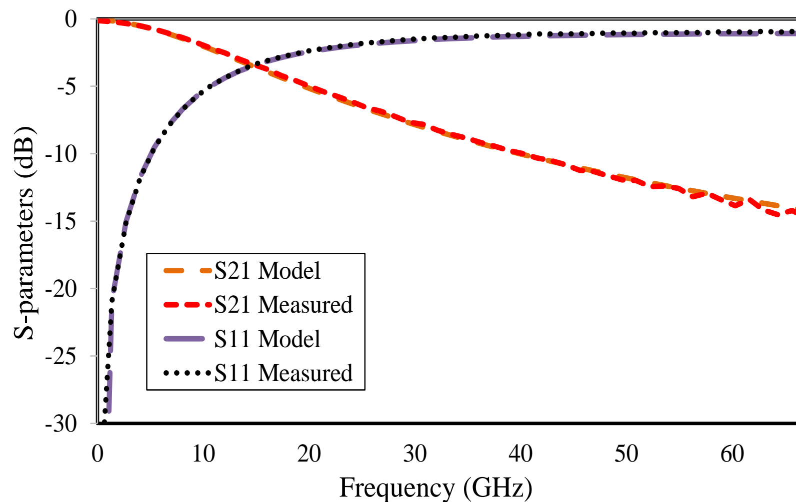
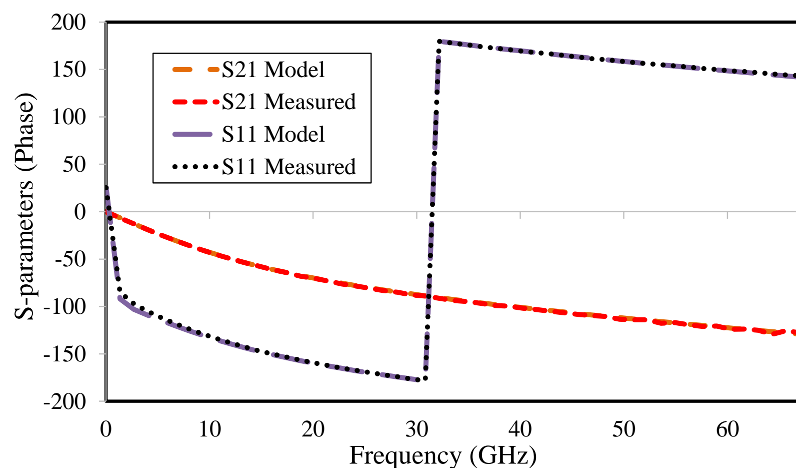


(b)

Figure 4.13: Measured and modelled *S*-parameters results of a 60 × 20 μm^2 series capacitor integrated to 0.19 mm-length S-Microstrip lines, (a) Magnitude (dB). And (b) Phase (degrees).



(a)



(b)

Figure 4.14: Measured and modelled *S*-parameters results of a 60 × 20 μm^2 shunt capacitor integrated to 0.19 mm-length S-Microstrip lines, (a) Magnitude (dB). And (b) Phase (degrees).

Table 4.1 shows the equivalent circuit model elements values of the fabricated capacitors for different areas. It can be seen that the ideal (with having fringing capacitance added) and modelled capacitance values are similar. However, the capacitance values of the measured *S*-parameters, shown in Figure 4.13 and Figure 4.14, are different from the calculated and modelled values, where the line parasitic was included. This was a result of the parasitic resistances of the capacitors. As mentioned, C_{M1} and C_{M2} are considered as coupling capacitors. It can be seen that their values are very sensitive to the capacitance area, as was expected. For a minimum capacitor area of (25 × 25 μm^2), the coupling capacitance parasitics were negligible, while they reached a maximum value of 0.043 pf for a capacitor area of (120 × 120

μm^2). This provided more evidence of the accuracy and viability of the proposed equivalent circuit model

Table 4.1: Derived equivalent circuit model and its coefficients for MIM capacitors.

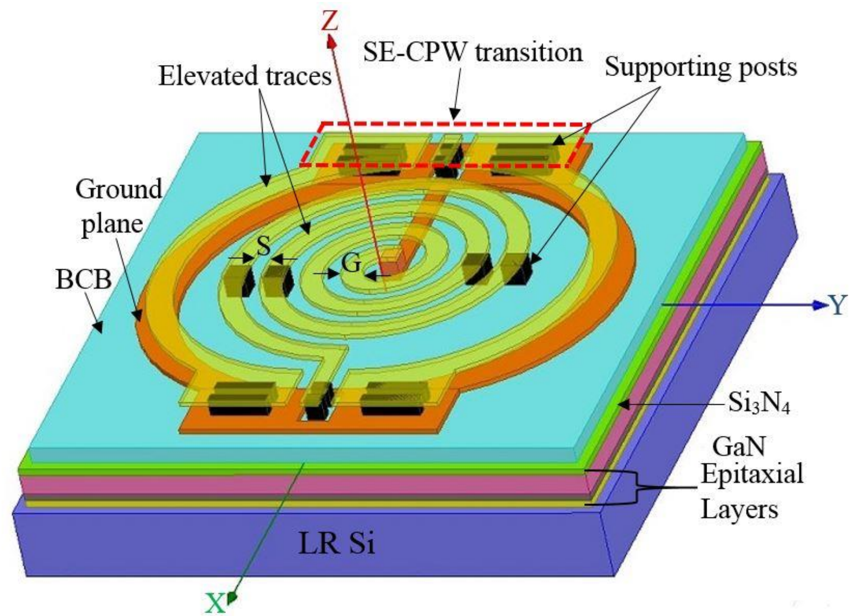
Capacitor size in µm	Calculated capacitor value (p*f*)	Series capacitors					Shunt capacitors		
		Modelled C_{Eff} value (p*f*)	C_{M1} (*pf*)	C_{M2} (*pf*)	R_{Series} (Ω)	R_{Cap} (KΩ)	Modelled C_{Eff} value (pf)	R_{Series} (Ω)	R_{Cap} (KΩ)
25×20	0.18	0.17	0	0	1	>15	0.18	0.12	>15
30×20	0.22	0.21	0.001	0.001			0.23		
60×20	0.45	0.4	0.002	0.002			0.43		
120×20	0.89	0.81	0.005	0.005			0.87		
120×40	1.79	1.67	0.014	0.014			1.69		
120×60	2.69	2.65	0.02	0.02			2.61		
120×100	4.49	4.27	0.034	0.034			4.48		
120×120	5.39	5.01	0.043	0.043			5		

4.6 High-Q Inductors

In this work, high-performance on-chip inductors were realised using a cost-effective MMIC-compatible technology with reduced parasitics using elevated traces on air and a BCB interface layer. Inductors with various inductance values (0.81 to 4.3 nH) were designed, fabricated and characterized based on the extracted inductors' model. Schematic cross-sectional view and SEM images of the fabricated MMIC spiral inductors integrated to 50 Ω SE-CPW on BCB are shown in Figure 4.15. The SE-CPW lines located at the input/output terminals of the inductor were employed as a measurements pads, where they are essentially required when considering the integration to active devices for MMIC circuits application.

4.6.1 Results and Discussion

To show the challenges involved in the design of high-performance inductors using the developed shielded-elevated transmission media technology, three different inductor technologies were realized; shielded-elevated inductors where ground planes were patterned



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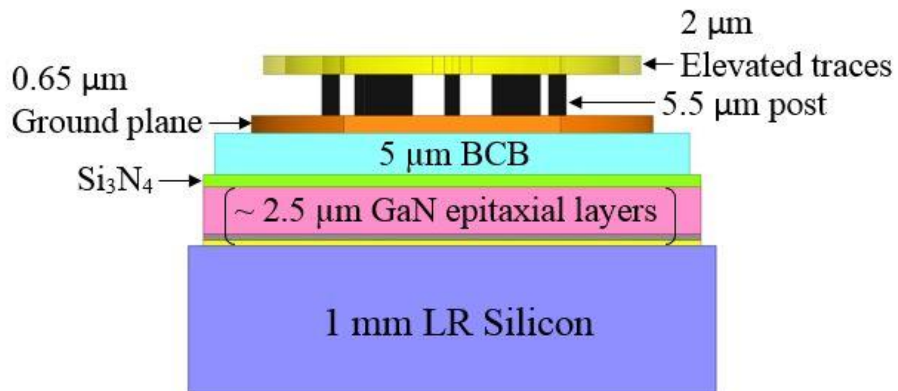

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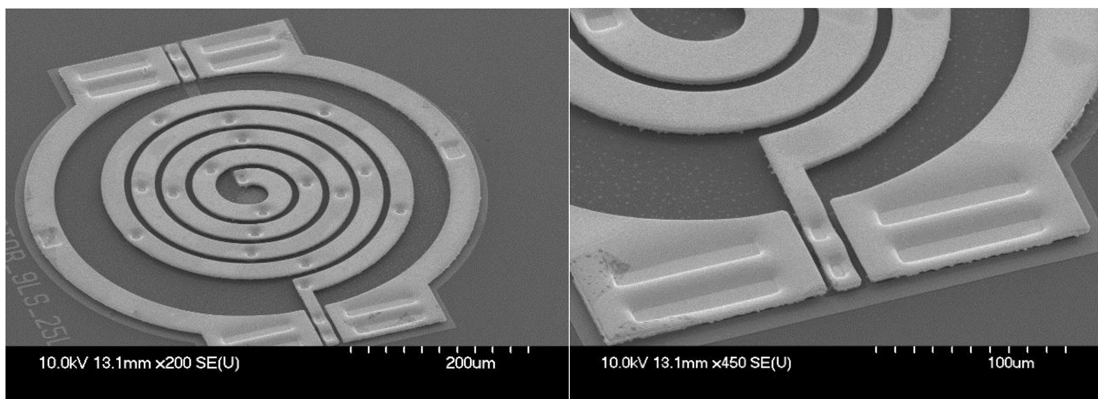


(c)

Figure 4.15: (a) 3-dimentional view. (b) Cross-sectional view. And (c) SEM image of the fabricated MMIC spiral elevated inductor integrated to 50 Ω SE-CPW on BCB.

on BCB underneath the elevated spiral loops, inductors fabricated directly on the BCB, and elevated inductors on BCB.

As shown in Figure 4.16, for the 3-turn inductors, the shielded-elevated inductor achieved the lowest performance, where a Q-factor of as poor as 4 at 17 GHz along with an f_{SRF} of 34 GHz were measured. This could be because the conductive ground plane allows an image current to flow and the negative mutual coupling between the spiral and ground plane reduces the inductance [105]. Using the patterned ground shield instead of solid ground shield can improve

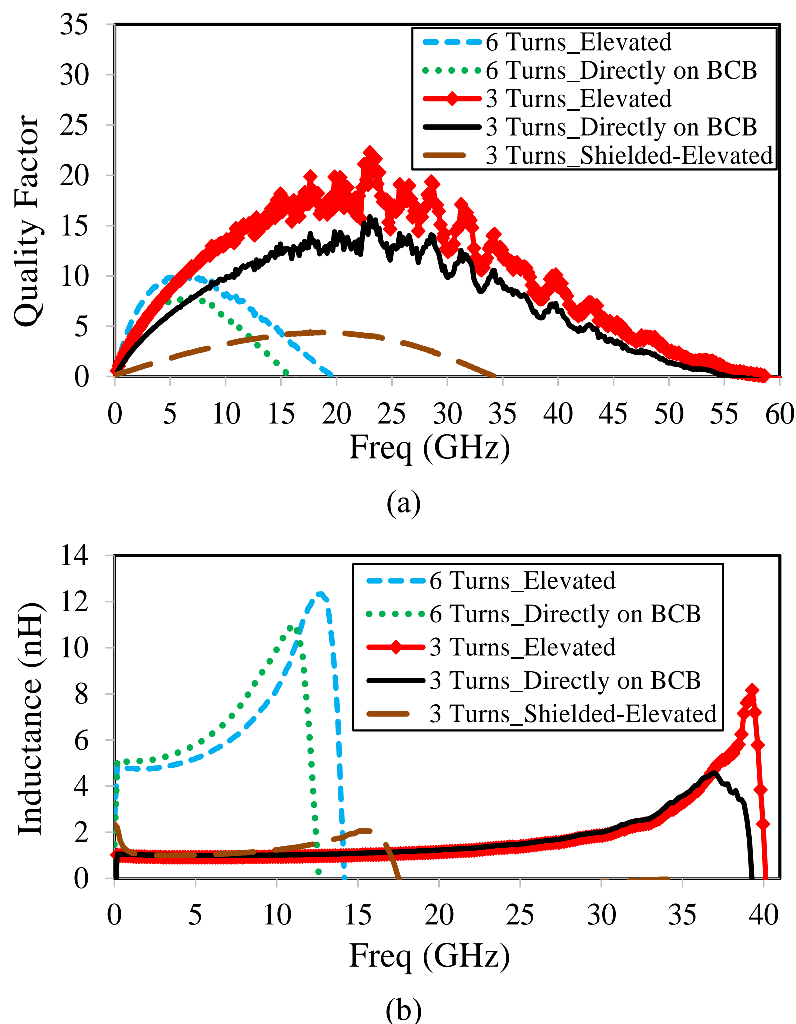


Figure 4.16: Comparison of the measured results of the fabricated MMIC inductors versus frequency: (a) Quality-factor and (b) Inductance.

inductor performance, but it is limited to lower frequency range. This is because the capacitive coupling between the spiral metal and the shield is increased [108]. Q-factor and f_{SRF} were further improved to 15 at 23 GHz and 55 GHz respectively, when fabricating the inductors

directly on the BCB. Having the spiral loops elevated in air increased the Q-factor by 57 % (Q = 22 at 24 GHz and f_{SRF} = 59 GHz) owing to reduced substrate parasitics. However, inductors achieved lower performance at frequencies below X-band due to a finite conductor thickness of 2µm, where conductor losses are dominant [107]. This could be enormously improved by having thicker conductor metals (by increasing electroplating time during fabrication process). However, at higher frequency range, improvement to inductor performance by increasing the physical conductor thickness is limited by the saturation of the series resistance [122]. Therefore, this technique will not be effective in the mm-frequency range.

To further investigate the performance/loss mechanism of the best performing elevated inductors on BCB, inductors with various number of turns (N = 3, 4, 5 and 6) were fabricated and modelled. The circuit model was verified by the excellent agreement between modelled and measured *S*-parameters up to 40 GHz, as indicated in Figure 4.17 . The model parameters (indicated in Table 4.2) are determined using the *S*-parameters fitting technique. As shown in Table 4.2, increasing N results in an increase in self-inductance due to the addition of the new conductors, and corresponding increase in the total mutual inductance of the device, resulting in the increase of the inductance value (L_{Prime}). However, as the inductor periphery increases, C_{d1} and C_{d2} and R will be dramatically increased, resulting in degradation of the Q-factor and f_{SRF} (as shown in the results of the 6-turns inductors indicated in Figure 4.16a)

Table 4.2: Extracted parameters for the equivalent circuit model and measured Q-factor and f_{SRF} of spiral inductors.

Parameter	**N = 3**	**N = 4**	**N = 5**	**N = 6**
L_{Prime} (nH)	0.815	1.517	2.677	4.304
L_s (nH)	0.104	0.464	0.689	1.19
R_s (Ω)	3.73	7.53	9.6	12.5
R (Ω)	7.5	9.1	11.58	16.28
C_{d1} (*fF*)	18	19.5	24.7	30.06
C_{d2} (*fF*)	18.8	20.82	26.02	31.26
C_P (fF)	2	3.4	6.8	14.4
R_{Sub1}/R_{Sub2} (KΩ)	15.8 / 13.3			
C_{Sub1}/C_{Sub2} (fF)	2			
f_{SRF} (GHz)	59	42	28	15
Q-Factor (Peak)	22	18	15	10

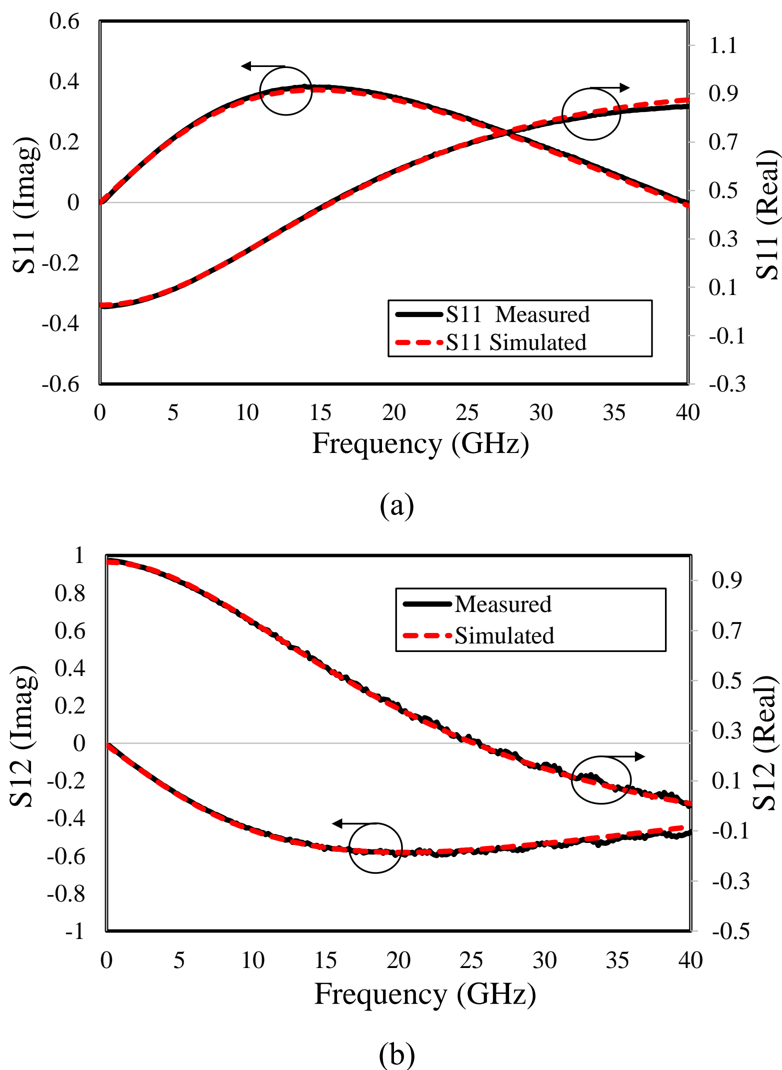


Figure 4.17: Measured versus modelled (a) S_{11} and (b) S_{21} for a 3-turns spiral elevated inductor on BCB for model validation.

4.7 Viability of the Developed Transmission Media Technology for THz Frequencies

THz technology has many applications in imaging and sensing, spectroscopy, astronomy and communications [123] [124]. The short wavelength of THz frequencies makes it a promising technology due to the unique interaction of its spectral regime with matter and the achievable high resolution imaging [125]. This interest in new emerging applications is motivated by the recent advances in high-speed semiconductor devices and nanotechnology; which have enabled the realization of TMIC (THz Monolithic Integrated Circuits) [126]. The advantage of using GaN-Si based material devices in TMIC such as low cost and higher power density and power added efficiency makes it more suitable than other material systems such as GaAs, InP or Si [127]. However, not only losses are dramatically influenced by substrate resistivity and

dielectric constant but they are also extremely sensitive to device layout dimensions which become comparable to wavelength dimensions at THz frequencies. Therefore, extra care is required when considering THz operation. As an example of loss sensitivity to device dimensions when operating at very small wavelengths (λ < 0.6 mm), the effect of CPW-transition via-hole depth of the developed S-Microstrip lines (indicated in Figure 4.6a) on the parasitic loss was studied using Ansoft HFSS simulations. The via-holes can be modelled as an in-series resistance (R_{via}) and inductance (L_{via}). Hence, they behave as a low pass filter to the RF signal. The extracted R_{via} and L_{via} values at 700 GHz (λ = 0.42 mm) are shown in Figure 4.18. It can be seen that the via-hole depth had a great influence on both R_{via} and L_{via}, where their values were noticeably increased from 0.44 Ω and 4.11 pH to 214.43 Ω and 82.77 pH when the depth was increased from 5.5 µm to 50.5 µm, respectively. This increase will lead to a dramatic degradation in transmission media performance. Therefore, the via-hole structure design needs to be carefully considered during simulation.

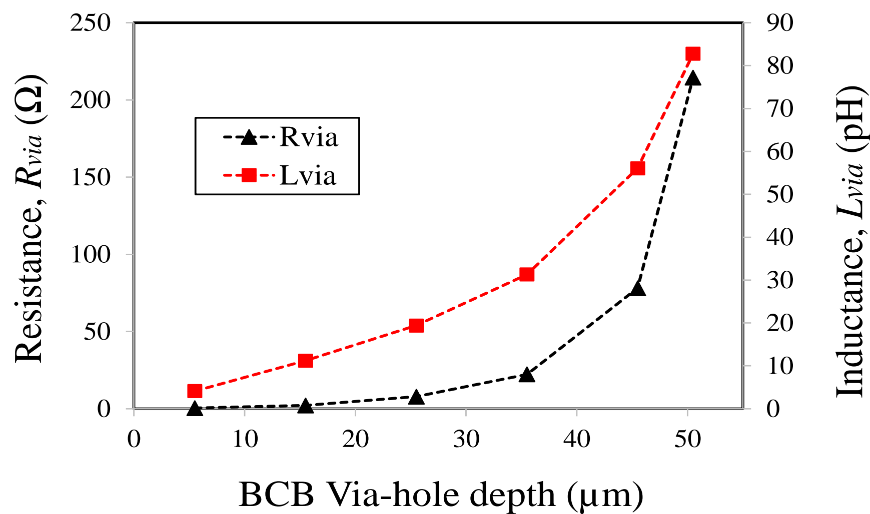
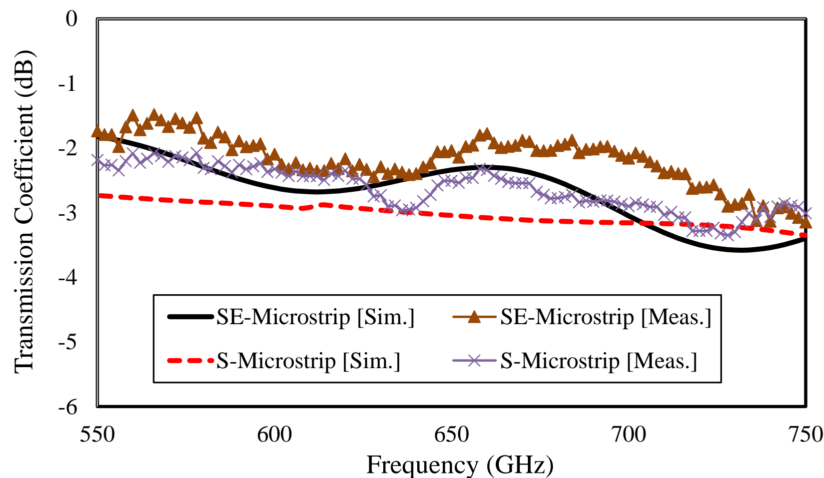


Figure 4.18: Extracted parasitic resistance (R_{via}) and inductance (L_{via}) values versus via-hole depth of the S-Microstrip line.

4.7.1 Results and Discussion

The THz on-wafer measurements were conducted at Fraunhofer Institute for Applied Solid State Physics IAF, Freiburg, Germany. Simulated and measured *S*-parameters results of the developed SE-Microstrip and S-Microstrip lines are shown in Figure 4.19. The simulation results were verified by the good agreement between measured and simulated *S*-parameters. It can be seen that both lines achieved an insertion loss (S_{21}) and attenuation (α) of less than 3.5 dB/mm and 0.5 Np/mm at frequencies up to 750 GHz, respectively. Moreover, better electrical field confinement was observed when employing air as a dielectric material as compared to BCB. Consequently, SE-Microstrip lines achieved less losses (S_{21} and α) than that of S-Microstrip lines. This attributes to the increased parasitic capacitances when the dielectric constant increased from 1 (air) to 2.6 (BCB). In addition, extra dielectric losses presented due to the loss tangent of the BCB. However, S-Microstrip lines performed better matching characteristics than that of SE-Microstrip lines, with a matching of better than 15dB across the whole measured frequency band (550 GHz –750 GHz). The matching characteristics of SE-Microstrip lines can be further improved by modifying the elevation height at THz frequencies.

The obtained results prove the total shielding from the substrate where the electrical field is being confined in the BCB/air between the ground plane and the microstrip signal line, rather than penetrating through the lossy silicon substrate. Therefore, the choice of a dielectric layer with low dielectric constant along with low loss tangent (e.g. BCB and air) is essential, especially in the THz frequency range. The developed transmission media technology not only can be used for conductive substrates, but also could be successfully utilised for SI-substrates, e.g. GaAs and InP. This is because radiation losses is dominant for SI-substrates at THz frequencies, basically owing to the presence of a high dielectric constant material.



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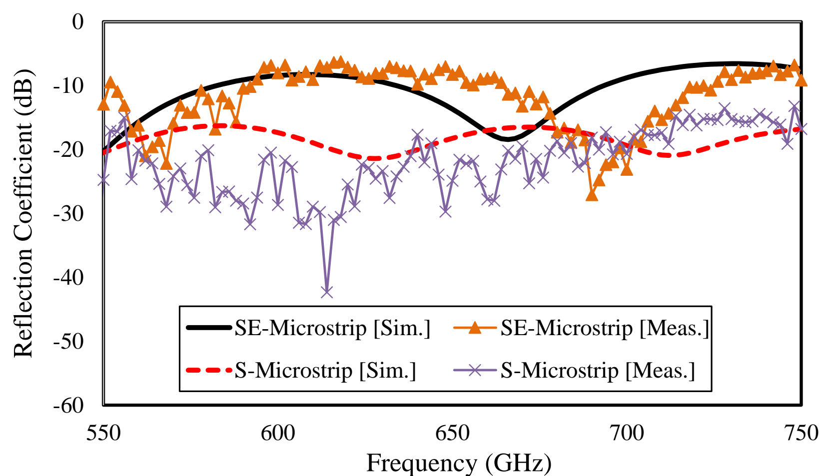

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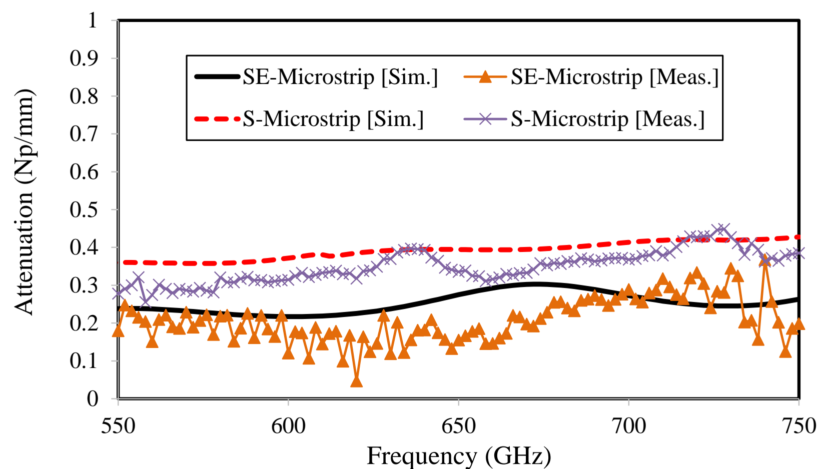

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Figure 4.19: Measured and simulated *S*-parameters results of 1mm-length 50 Ω S-Microstrip and SE-Microstrip lines on GaN-on-LR Si. (a) Transmission coefficient, S_{21}. (b) Reflection coefficient, S_{11}. (c) Attenuation, α.

4.7.2 Short-circuited stub filters

The short-circuited shunt matching network is a key topology for a variety of circuits including band-pass filters, diode detectors and matching / DC return networks [126] [128]. However, in the H-band frequency range, short-circuited matching stubs exhibit low quality factor even for SI GaAs substrates which makes them a non-viable component for TMIC technology [129].

Figure 4.20 shows a 3-D plot of the fabricated SE-CPW on BCB dielectric short-circuited stub filter structure. The short stub characteristic impedance, Z_0 is approximately 36 Ω, and dimensions are; W= 39 µm and S = 19 µm. While the feed line was designed to be Z_0 = 50 Ω, W = 24 µm and S = 30 µm.

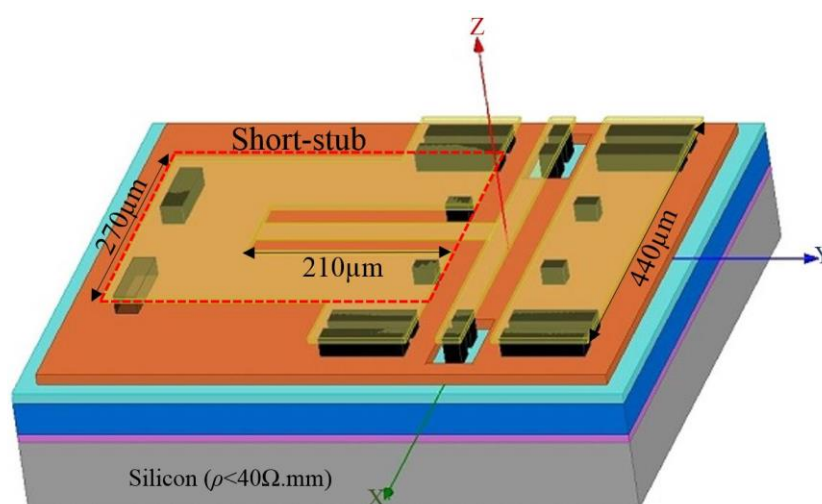
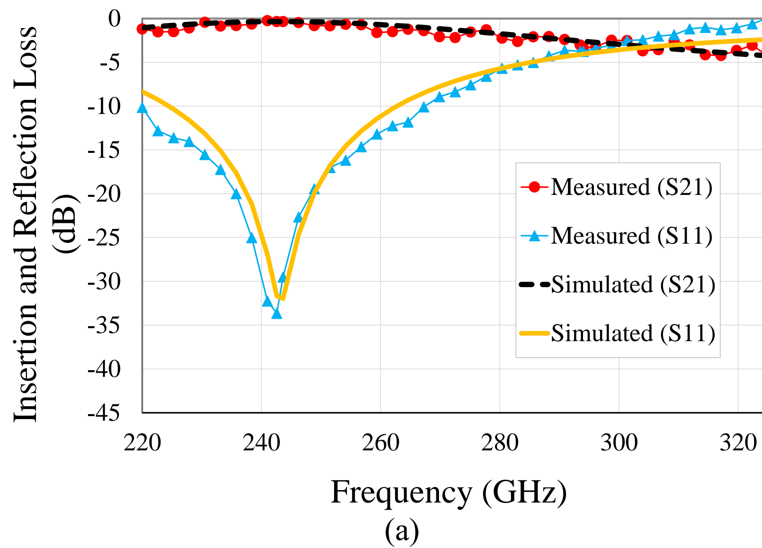


Figure 4.20: Oblique projection of the fabricated SE-CPW short-circuited stub filter with the fabricated dimensions.

Figure 4.21a shows the simulated and measured S-parameters of the SE-CPW short stubs on BCB dielectric insert. It is clear that insertion of an insulating layer of BCB between the GaN-on-LR Si substrate and shielding plate resulted in superior performance and a relatively sharp resonance, with a Q-factor of 28 and return loss of -34 dB and at 244 GHz. In addition, an insertion loss and 3dB-bandwidth of as low as 0.35 dB and 101 GHz were obtained respectively at a resonance frequency of 244 GHz. This improvement in performance is an indication of the complete isolation of the lossy substrate.

Previous work done by other researchers obtained a Q-factor of 21 and insertion loss of -4.1 dB/mm on RF CMOS technology operating at 60 GHz [37] . These results obtained by the

newly developed technology are superior to those of the same structure using shielded elevated CPW on air-bridge supports without the BCB dielectric insert layer as shown in Figure 4.21b. Higher insertion loss was observed in additional to the low quality factor.



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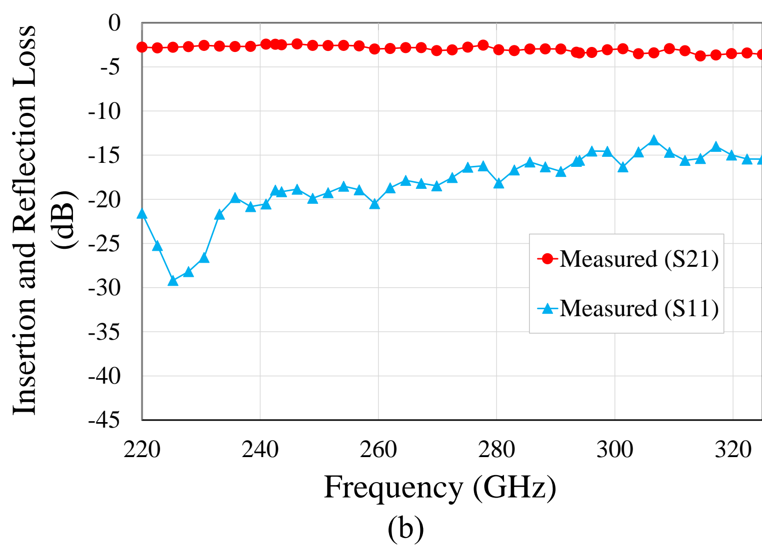

(b)

Figure 4.21: S-parameters results of the fabricated SE-CPW short-circuited stub filter (a) with BCB insert, and (b) without BCB insert.

4.8 Conclusion

The general operational principle of Microstrip lines and passive components, including MIM capacitors and spiral conductors, has been introduced in this chapter. The newly-developed transmission media technology was designed and validated using a 3-D full-wave electromagnetic simulation. The developed passive devices and MMIC interconnect were proven to suppress substrate loss effects, eliminating electromagnetic decoupling of the conductive Si substrate up to THz frequencies. Consequently, a transmission loss, S_{21}, and attenuation, α, of better than 0.6 dB/mm and 0.06 Np/mm were achieved, respectively at frequencies up to 67 GHz. These results were even better than those achieved using MMICs conventional transmission media on a standard SI GaAs substrate. Furthermore, the developed lines were characterised at THz frequencies, where S_{21} and α of less than 3 dB/mm and 0.4 Np/mm were achieved, respectively at frequencies up to 750 GHz; indicating its potential as a viable wideband RF integrated technology. In addition, low-loss in-line MIM capacitors and high-Q inductors were presented to prove the capabilities and efficiency of the developed transmission media. The developed technology in this work offers a promising capability for the integration of high RF performance active devices and low-losses high-Q passive elements for the realization of MMIC circuits at mm-wave and THz frequencies.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

The research study conducted in this thesis has shown GaN-on-LR Si technology as a promising candidate for low-cost high-power, high-frequency MMIC applications. This is mainly due to the superior material properties offered by the wide-bandgap semiconductor material, GaN, and the scale offered by the large Si wafer diameters. GaN HEMTs grown on LR Si are widely used for power management, whereas GaN HEMTs grown on HR Si are leading the technology for RF operations. However, one of the major concerns about GaN-on-HR Si technology is that substrate resistivity is greatly reduced at high temperature operation, causing an increase in substrate loss, and, therefore, dramatic degradation in RF performance. This work focused on the mitigation of the substrate coupling effect associated with the conductive Si substrates for RF operation. As a consequence this will allow a successful demonstration of high-performance MMIC circuits using GaN-based HEMTs on LR Si technology. The following two sections conclude the work undertaken in the course of this thesis:

5.1.1 Demonstration of High DC and RF Performance AlGaN/GaN HEMTs on LR Si.

The AlGaN/GaN HEMTs on LR Si were fabricated in this work using a reliable and MMIC-compatible fabrication process. In addition, the RF performance of the realised devices was analysed based on the extracted small-signal equivalent circuit model to allow better understanding of device RF behaviour, and hence improved RF performance. The gate, drain and source parasitic geometric capacitances were reduced by the optimisation of the device layout. Therefore, the layout of the input and output feeds and pads of the device were designed to accommodate the smallest RF probe tips pitch size (of 50 μm) and RF probing required skating distances. The epitaxial material structure was found to have a great influence on both DC and RF device characteristics. Insertion of 1 nm AlN interlayer between the GaN buffer layer and AlGaN Schottky barrier, and scaling the AlGaN Schottky barrier to 9 nm dramatically

improved the DC and RF performance of the devices. This was attributed to the excellent material growth engineering which was obtained where enhanced electrons, confined in the 2DEG channel, were prevented from overflowing into the buffer and toward the conductive Si substrate. Consequently, a 0.27 µm T-gate AlGaN/GaN HEMTs on LR Si with maximum I_{DS} of 825 mA/mm, V_T of -1.12 V, and a maximum G_m of 369 mS/mm, maximum f_T of 79.75 GHz and f_{MAX} of 82.5 GHz, was obtained. These results were even better than AlGaN/GaN HEMTs grown on SI-SiC substrates [130]. Furthermore, the obtained combinations of DC and RF results were the best reported to date for GaN-on-LR Si technology and indicated the viability of cost-effective mm-wave frequency applications using this technology in addition to further system integration.

5.1.2 Demonstration of Low-loss Transmission Media for GaN-on-LR Si Technology.

The newly proposed transmission media technology was initially simulated using a 3-D full wave electromagnetic simulation tool to ensure best device performance and complete isolation from the conductive Si substrate. Two design structures were realised on GaN-on-LR Si substrates providing almost complete isolation of the conductive substrate, by employing a ground plane, a 5 µm-thick BCB and elevated line traces on air. A transmission loss, S_{21}, and attenuation constant, α, of less than 0.6 dB/mm and 0.06 Np/mm respectively were achieved at frequencies up to 76 GHz. These results were even better than those achieved using conventional MMIC transmission media on a standard SI GaAs substrate. To prove the capabilities and efficiency of the developed transmission media, low-loss in-line series and shunt MIM capacitors with various capacitance values, ranging from 0.18 to 5.39 pf, were presented. In addition, High-Q on-chip inductors employing elevated traces and a BCB interface layer were been realized on GaN-on LR Si in order to reduce substrate coupling effects. Inductors with inductance varying from 0.81 nH to 4.3 nH were designed, fabricated and analysed. A peak Q-factor of 22 at 24 GHz and f_{SRF} of 59 GHz was achieved for 0.81 nH inductors. The realised MIM capacitors and spiral inductors were characterized based on the extracted small-signal model. The developed MMIC transmission media technology offered a promising technology platform and can be integrated with RF GaN-HEMTs on LR Si for the realization of high-performance MMIC circuits for mm-wave applications.

5.2 Future Work

The mm-wave GaN-on-LR Si technology developed in this work is considered as base for additional on-going development process within the research group led by Dr. Khaled Elgaid. In additional to AlGaN/GaN HEMTs on LR Si enhancement by improving layer structure and ohmic contacts; additional future work that currently restricts the performance of the proposed technology will be proposed. The potential future research developments based on this work are presented in the following sections.

5.2.1 Material Optimisation

- As indicated in Table 1.1, to extend the speed (cut-off frequency) of GaN-on-LR Silicon devices, ultrashort gate lengths ($\leq 100\ nm$) are required. This can be realised by employing an ultrathin AlN Schottky barrier ($\leq 6\ nm$) instead of AlGaN, enabling a high aspect ratio and 2DEG density [131]. However, the use of ultrathin barriers results in high gate leakage currents, which have been effectively reduced by using an in-situ Si_3N_4 early passivation to control the strain relaxation and hence strengthen the robustness of the surface. Consequently, outstanding RF and DC characteristics have already been demonstrated on HR Si substrates [29].

- The generation of high electric fields beneath the gate when using short gate lengths resulted in poor electron confinement in the 2DEG, especially at drain voltages of V_{DS} >10 V. Hence, Double-Heterostructures Field Effect Transistor (DHFET) design structure employing an AlGaN back barrier has been widely adapted to improve the electron confinement and the gate modulation efficiency [132].

- With reference to Figure 3.16, the transmission media realised on GaN-on-LR Si showed a remarkable enhancement in RF loss when increasing the GaN buffer thickness from 1.4 µm to 2.6 µm. However, since the fabricated devices in this work were not identically realised (e.g. different gate lengths, source-to-drain separation and material growth conditions), more investigations in this area are required. To the author's knowledge, no such comprehensive study have been conducted (to date) on the effect on Fe-doped GaN buffer thickness on both DC the RF performances of GaN-on-LR Si.

In addition, this study could lead to potential improvements in the DC and RF performance despite the possible challenges involved in the material growth quality of thick GaN buffer layers.

5.2.2 Fabrication Technology

- Device performance can be further improved by reducing the source/drain contact resistance which generally dominates the extrinsic resistance of the device. Hence, a reduction in the contact resistance from 0.6 Ω.mm to less than 0.1 Ω.mm is required to reduce this loss. In addition, low-temperature annealing temperatures (≤ 600 ^{0}C) are essential to obtain smooth edge roughness, and, therefore, to enable the further reduction of source-drain distance for high frequency operations. For example, Si-implantation or recess ohmic contacts have to be incorporated into the existing MMIC fabrication technology, despite the additional cost and complex fabrication process [133] [134].

- As lateral source-drain scaling is desirable to supress drain delay and velocity improvements at frequencies beyond W-band, additional parasitic capacitances between the gate-source pads and gate-drain pads should be considered [9]. These parasitic capacitances can be minimised by increasing the height of the T-gate foot (h_G) using air as a dielectric to ensure minimum parasitic capacitances. In this case,

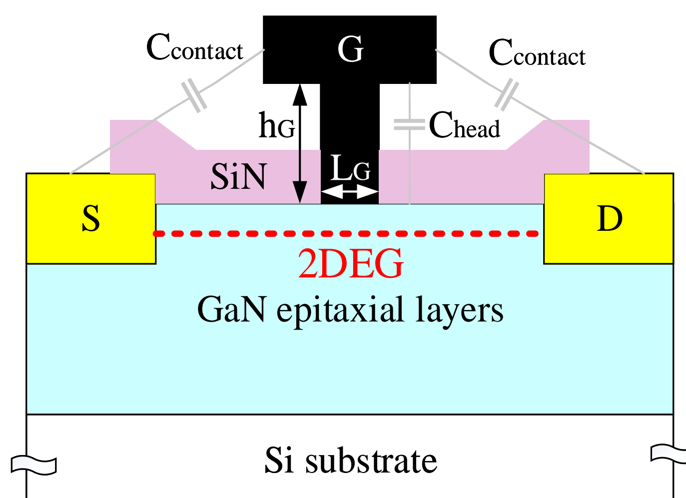

Figure 5.1: Cross-sectional view of two-level T-shaped gate module and associated parasitic capacitances.

the T-gate can be fabricated into two steps; the basic gate foot is initially defined in the Si_3N_4 passivation layer as mentioned in Section 3.6 to ensure low gate leakage currents, and then additional fabrication steps are required to define the extended gate foot height and head simultaneously using chemically amplified DUV resists and PMMA [135]. The fabrication process summary and schematic cross-sectional view of this process are indicated in Figure 5.1.

5.2.3 Thermal Management in GaN-based Heterostructures on LR Si Substrates.

Despite the superior RF performance obtained by GaN-based heterostructures grown on HR Si substrates, the power performance of these devices is still relatively poor and limited to the low thermal conductivity of the Si substrate, as compared to SiC and diamond substrates (Table 1.1). To gain a full advantage of the electrical material properties of GaN semiconductors, it has to be grown on super-thermal conductive substrates for heat dissipation purposes. This will not only allow high power densities at a high frequency range, but will also reduce the cooling complexity and cost when considering system level operation. GaN-on-Diamond devices have already shown over three times higher power densities when compared to GaN-on-SiC devices [6]. This is as a result of the superior thermal conductivity of diamond compared to SiC [5]. However, difficulties are involved in growing high quality GaN-on-diamonds because of the lattice mismatch between diamonds and III-Nitride materials. Nevertheless, the GaN-on-diamond has a limited size substrate availability and is extremely expensive compared to GaN-on-Si substrates. Therefore, to combine the low-cost advantage of GaN-on-LR Si and high thermal conductivity of diamond, backside processing is proposed on GaN-on-Si technology. This includes, Si substrate thinning and then removal beneath the active device area, depositing a AlN adhesion layer prior to the growth of polycrystalline diamonds using a hot filament Chemical Vapour Deposition (CVD) [136].

The proposed future development of a complete AlGaN/GaN HEMTs is indicated in Figure 5.2. Finally, using the fabrication technique and the developed transmission media technology in this work, a full MMIC circuit can be completely performed on the top, where no substrate via are required anymore.

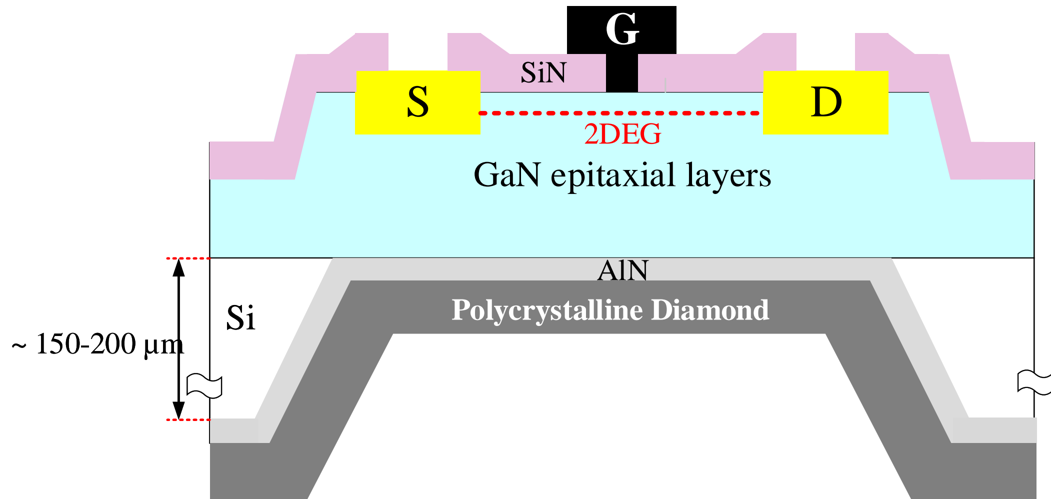

Figure 5.2: Cross-sectional view of GaN-based heterostructure on Si with incorporated backside diamond.

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