A Novel Monolithic Focal Plane Array for Mid-IR Imaging

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Abstract

The use of Mid-infrared (mid-IR) imagers has great potential for a number of applications in gas sensing and medical diagnostics, but so far for many of those non-defence fields it has been significantly limited by their high price tag. One of the reasons behind the great cost of mid-IR imagers is that most of them need to operate at cryogenic temperatures. Thanks to more than half a century of research, state-of-the-art mid-IR photodetectors have finally achieved premium detection performance without the need for cryogenic cooling. Some of them have even demonstrated very promising results, suggesting room temperature operation is on the horizon. As a result, the cost associated with cooling equipment has been significantly suppressed. However, most mid-IR imagers are still based on hybrid technologies needing a great number of die-level process steps and being prone to connection failure during thermal cycles. The high manufacturing cost this entails is also preventing a wider diffusion of mid-IR imagers. Currently, there is still a lack of an effective monolithic approach able to achieve low-cost mass production of mid-IR imagers in the same way as monolithic integration has been widely used for imagers working at visible wavelengths.

This thesis presents a novel monolithic approach for making mid-IR imagers based on co-integration of mid-IR photodetectors with GaAs-based MESFETs on the same chip. The initial focus of the project was the development of the fabrication steps for delivery of prototype devices. In order to achieve monolithic fabrication of pixel devices made in either indium antimonide (InSb) or indium arsenide antimonide (InAsSb) on a gallium arsenide (GaAs) substrate, various highly controllable etch processes, both wet and dry etch based, were established for distinct material layers. Moreover, low temperature annealed Ohmic contacts to both antimonide-based materials and GaAs were used. The processing temperatures used never exceeded 180˚C, preventing degradation of photodetector performance after fabrication of transistors, thus avoiding well-known thermal issues of InSb fabrication. Furthermore, an intermediate step based on polyimide was developed to provide a smoothing section between the lower MESFET and upper photodetector regions of the pixel device. The polyimide planarisation enabled metal interconnects between the fabricated devices regardless of the considerable etch step (> 6 μm) created after multiple mesa etches. Detailed electrical and optical measurements demonstrated that the devices were

sensitive to mid-IR radiation in the 3 to 5 μm range at room temperature, and that each pixel could be isolated from its contacts by switching off the co-integrated MESFET.

Following the newly developed fabrication flow, InSb-based mid-IR imaging arrays (in two sizes, 4×4 and 8×8) are presented here for the first time, with pixel addressing achieved by monolithically integrated GaAs MESFETs. By demonstrating real-time imaging results obtained from these array devices at room temperature, implementation of a new type of monolithic focal plane array for mid-IR imaging has been confirmed. The device is suitable for further scaling(up to 64×64 pixel and beyond)and potential commercialisation. More importantly, the monolithic approach developed in this work is very flexible,as a numberof III-V materials with mid-IR detecting capabilities can be grown on GaAs substrates, meaningalternative semiconductor layer structures could also beinvestigated in the near future.

Declaration

Unless otherwise acknowledged, the content of this Thesis is the result of my own work. None of this material has been submitted for any other degree at the University of Glasgow or any other institution.

Chengzhi Xie

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Publications

Journal Papers

C. Xie, V. Pusino, A. Khalid, M. J. Steer, M. Sorel, I. G. Thayne and D. R. S. Cumming, "Monolithic Integration of an Active InSb-Based Mid-Infrared Photo-Pixel with a GaAs MESFET", *IEEE Transactions on Electron Devices*, 62(12), pp.4069-4075, 2015.

V. Pusino, C. Xie, A. Khalid, I. G. Thayne and D. R. S. Cumming, "Development of InSb dry etch for mid-IR applications", *Microelectronic Engineering*, 153, pp.11-14, 2016.

V. Pusino, C. Xie, A. Khalid, M. Steer, M. Sorel, I. Thayne and D. Cumming, "InSb Photodiodes for Monolithic Active Focal Plane Arrays on GaAs Substrates", *IEEE Transactions on Electron Devices*, vol. 63, no. 8, pp. 3135-3142, 2016.

C. Xie, M. Aziz, V. Pusino, A. Khalid, M. J. Steer, M. Sorel, I. G. Thayne and D. R. S. Cumming, "Single-chip, Mid-infrared Array for Room Temperature Video Rate Imaging", *prepared for submission*.

Conference Papers

C. Xie, V. Pusino, A. Khalid, M. Aziz, M. J. Steer; D. R. S. Cumming, "A new monolithic approach for mid-IR focal plane arrays", *Proc. SPIE 9987, Electro-Optical and Infrared Systems: Technology and Applications XIII*, 99870T, 2016.

Oral Presentations

"A Novel InSb-Based Photo-Pixel with a Monolithically Integrated GaAs MESFET for Video Rate Sampling", *Conference on Lasers and Electro-Optics (CLEO) 2016*.

"Novel Monolithically Integrated Photo-pixels for Mid-IR Imaging", *UK semiconductors 2016*.

"A Novel Monolithic Focal Plane Array Approach for Mid-IR Imaging", *SPIE Defense&Security 2016*.

Posters

"Monolithic Fabrication of InSb-based Photo-Pixel for Mid-IR Imaging", *Compound Semiconductor Week 2016*.

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List of Acronyms

ADC	analog-to-digital conversion
CMOS	complementary metal-oxide-semiconductor
CCD	charge coupled device
CDS	correlated double sampling
CTE	charge transfer efficiency
CTLM	circular transmission line method
CID	charge injection devices
CIM	charge-imaging matrices
DAQ	Data Acquisition
DEC	decoder
DI	deionized
EBL	electron beam lithography
FE	field emission
FTIR	Fourier transform infrared
FPA	focal plane array
HOT	high operating temperature
IPA	isopropyl alcohol
IR	infrared
IMF	interfacial misfit
ICP	inductively coupled plasma
JFET	junction field effect transistor
JWNC	James Watt nanofabrication centre
LCC	leadless chip carrier
LED	light emitting diode

LN_2	liquid nitrogen
LOR	lift off resist
LWIR	long-wavelength infrared
MBE	molecular beam epitaxy
MCT	mercury cadmium telluride
MD	misfit dislocation
MEMS	micro-electro-mechanical systems
MESFET	metal-semiconductor filed effect transistor
MIS	metal-insulator-semiconductor
MU	measurement unit
MUX	multiplexer
MWIR	mid-wavelength infrared
NIR	near infrared
PC	photoconductor
PD	photodetector
PMMA	polymethyl methacrylate
PV	photovoltaic
QCL	quantum cascade laser
QD	quantum dot
QE	quantum efficiency
QWIP	quantum well infrared photodetector
RHEED	reflection high energy electron diffraction
RIE	reactive ion etching
ROIC	read-out integrated circuit
S-I	semi-insulating
SPA	semiconductor parameter analyser
SWIR	short-wavelength infrared

SLS	superlattice structure
SBD	Schottky barrier diode
TD	threading dislocation
TE	thermionic emission
TFE	thermionic field emission
TLM	transmission line method
TMAH	tetra-methyl ammonium hydroxide
TIA	transimpedance amplifier
UV	ultraviolet
VLSI	very-large-scale integration
VRU	variable resolution unit

1. Introduction

1.1 Motivation and Objectives

An effective imaging technology in the Mid-infrared (mid-IR) range can contribute to a wide range of applications in the fields of gas sensing, environmental monitoring, medical diagnostics, security and defence [8-12]. However, compared to standard digital cameras imaging at visible wavelengths, mid-IR imagers have not yet reached such level of technological maturity, thus their use for many non-defence applications is still limited.

In order to make an imaging device, such as a focal plane array (FPA), it is required that the signal generated in each pixel must be individually readable or addressable. For imaging at visible wavelengths, this has been achieved by monolithic integration of silicon photodetectors (PDs) with silicon transistors using the well-established complementary metal oxide semiconductor (CMOS) process to form arrays of switchable pixels [62, 63]. The situation is rather different for imaging in the mid-IR range. Although a number of narrow bandgap semiconductors, such as indium antimonide (InSb) and indium arsenide antimonide (InAsSb), are well-suited for making mid-IR PDs, none of them is adaptive for making transistors with good switching behaviour for pixel addressing [45]. Due to this fundamental difficulty, early attempts for making monolithic mid-IR FPAs based on metal-insulator-semiconductor (MIS) structures were soon abandoned [73, 76].

Most commercially available mid-IR imagers choose to circumvent this problem by hybridising an array of isolated mid-IR PDs with a separate CMOS silicon addressing chip known as a read-out integrated circuit (ROIC). Generally, this is done through a technique known as “flip-chip bonding”. However, as a die level process that requires individual chips to be diced from corresponding wafers before hybridising, this approach presents low yield and high costs. Furthermore, because of the large thermal expansion mismatch between the two hybridised chips (upto 70% under 300K [101]), the resulting bonds and devices may suffer considerable strain stress as their operating or storage temperature changes dramatically. Even after reducing the thermal expansion mismatch by applying complex processes such as substrate thinning, hybrid mid-IR imagers can still be prone to bonds breaking or even chip cracking in the worst case [100-102].

Recently, antimonide-based mid-IR PDs have been grown on a gallium arsenide (GaAs) substrate by molecular beam epitaxy (MBE) and were reported to have comparable performance to the devices grown on more expensive native substrates [121, 145, 202]. In addition to providing a cost-saving substrate, GaAs can be used as a functional material to fabricate transistors and thus realise ROICs [150-153]. Naturally, the great potential of GaAs to provide a novel monolithic platform for mid-IR FPAs is highlighted. Similar to hybridised approaches, this approach allows separate fabrication of PDs and ROICs in different material systems. It will also increase the yield of mid-IR imaging devices, reduce cost by wafer level manufacturing, and not suffer from the problems related to flip-chip bonding.

The main objective of this project is to monolithically integrate state-of-the-art mid-IR PDs with GaAs-based ROICs by heterogeneous growth of high quality antimonide-based semiconductors onto a GaAs substrate consisting of active layers for transistor fabrication. In this thesis, the design, fabrication, and characterisation of the first monolithic FPA based on on-chip integration of InSb PDs and GaAs metal-semiconductor filed effect transistors (MESFETs) are described. Real-time imaging test of the fabricated prototype devices confirm the possibility of realising a compact, cost-effective mid-IR imager based on this newly proposed monolithic approach.

1.2 Organisation of the Thesis

The thesis is divided into eight chapters. Following this brief introduction, **Chapter 2** provides a literature study on the current state of mid-IR imaging technology. The chapter begins with an introduction to mid-IR radiation and its typical applications, followed by a discussion of the state-of-the-art in mid-IR detectors and of the approaches to make imaging devices. The chapter continues with presentation of some main requirements for implementation of next generation mid-IR imagers. The chapter concludes with comparison and discussion of all of the reviewed techniques, highlighting the research topic that thesis will be focused on.

The background theory and operation of a GaAs-based monolithically integrated pixel array device is outlined in **Chapter 3**. The chapter begins with proposing a novel monolithic FPA approach based on heterogeneous integration of mid-IR PDs with GaAs-based readout integrated circuits ROICs. The chapter continues with listing the fundamentals and the figures of merit of GaAs MESFET and mid-IR photodiodes. This helps understanding the operating mechanism of an X-Y addressing strategy based on

pixels integrated with GaAs MESFET switches. A summary of performance requirements to be used as guidance for device fabrication concludes the chapter.

The next two Chapters present the main techniques and methods that have been used in this work to fabricate and characterise the completed prototype devices as presented in the previous chapter. The first section of **Chapter 4** briefly gives an overview of general micro- or nanofabrication techniques followed by the introduction of a series of measurement methods used for monitoring the fabrication and evaluating the performance of fabricated devices.

Afterwards, detailed device fabrication process flow is outlined in **Chapter 5**. The chapter is focused on the main challenges and on the solutions for achieving independent fabrication of mid-IR PDs and GaAs MESFETs side-by-side on the sample surface. This is followed by presenting the process to make interconnections between fabricated pixels so that a complete array circuit can be completed. The chapter ends with demonstration of some promising processes developed for further scaling the devices into small pitches and large array format.

Chapter 6 presents results obtained from the photo-pixels fabricated using the method described in the previous two chapters. The chapter begins with the description of various device layout designs based on InSb and InAsSb PDs. This is followed by the presentation of the DC characterisation of the individual components (PDs, MESFETs) and of the whole interconnected pixel circuit. Besides, results from reported devices with similar PD structures are also included for comparison and evaluation. The final half of the chapter demonstrates and discusses the spectral photoresponse and the transient response of the photo-pixels. A summary of the overall device performance concludes the chapter.

Chapter 7 demonstrates the real-time mid-IR imaging capability of the first prototype array devices fabricated in this work. The first section of the chapter describes the experimental setup data acquisition from a 4×4 or an 8×8 array device in real-time. This is followed by the presentation of some key figures of merit obtained from the fabricated arrays, including responsivity, peak specific detectivity and crosstalk between pixels. The chapter ends by showing the results from a series of imaging tests with various mid-IR sources applied.

Chapter 8 draws conclusions from the results achieved in this work and offers a summary of the future work that could be undertaken as a continuation of this project.

2. Overview of Mid-IR Imaging

This Chapter describes the definition and applications of mid-IRradiation in a wide range of areas, followed bythe presentation ofan overview of the mid-IR imaging technology. After demonstrating thestate-of-the art mid-IR detectors and imaging devices, this chapter will presentthe main candidates for next generation mid-IR imagers. The chapter will conclude with comparison and discussion of all these existingtechniques.

2.1 Mid-IRRadiation and Applications

Next to the visible spectrum and in the longer wavelength side,infrared (IR)radiation is a form of radiated electromagnetic energy that covers the 0.7 to 100 μmregion of the electromagnetic radiation spectrum.As a portion of the IR spectrum,mid-IR radiation spans widely from 3 μm to approximately 30 μm.However, for long-range imaging applications only few portions of the mid-IR spectrum can be used, as most of the wavelengths are strongly absorbed by earth's atmosphere components such as water vapour. Themid-IR radiation that can be efficiently utilized without significant losses isthus limited to twoimportantregions, highlighted in Fig. 2.1. They are the mid-wavelength infrared (MWIR) spectral range, spanningwavelengths from3 to 5 μm, and the long-wavelength infrared (LWIR) range, covering from8 to 12 μm.

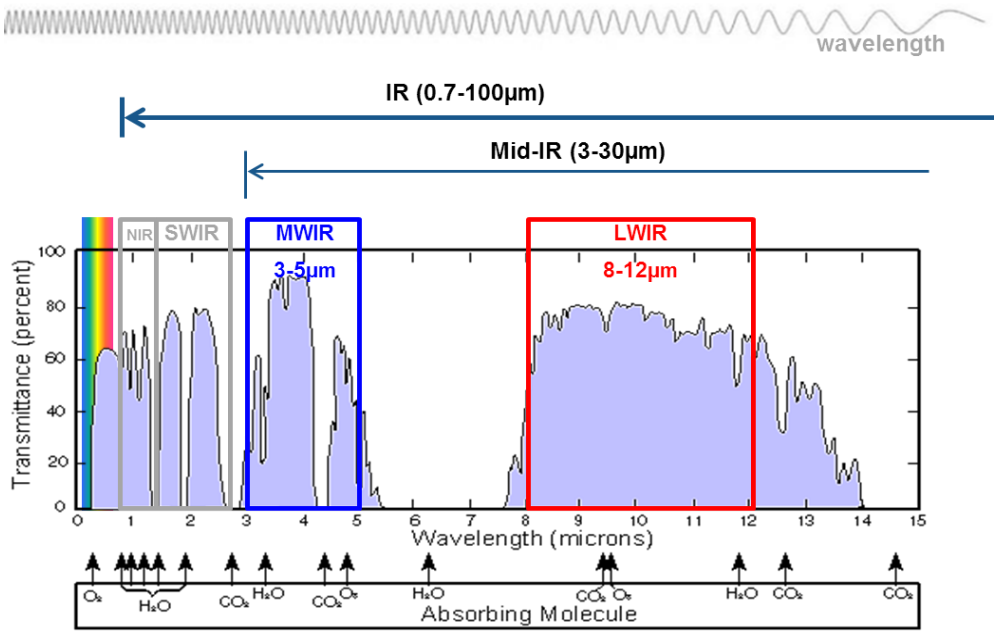


Fig. 2.1. Atmospheric transmittance highlighting windows of good atmospheric absorption [1]

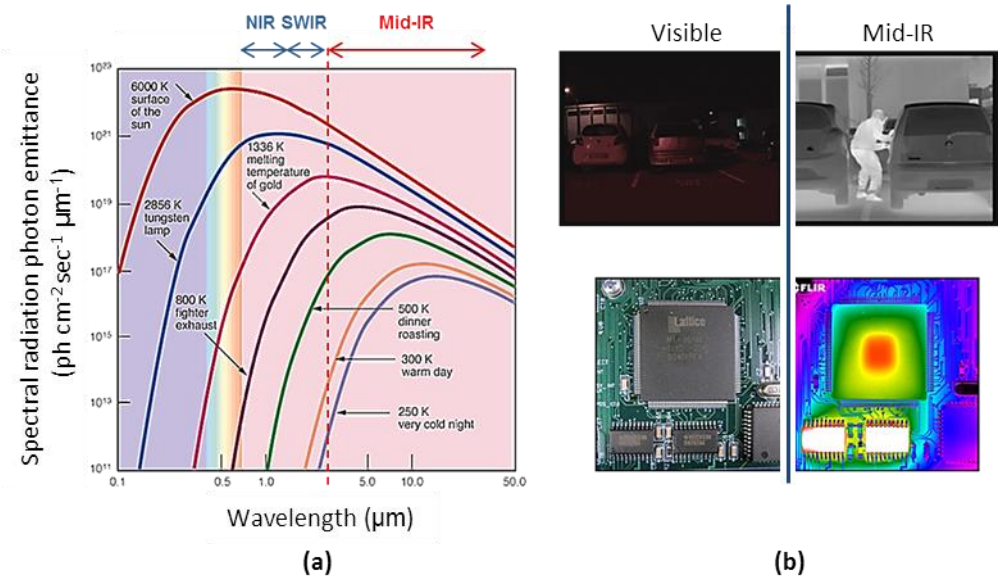


Fig. 2.2. (a) Spectral radiation photon emittanceof a blackbody source as a function of wavelength for different temperatures [2] (b) Images taken in visible and mid-IR range respectively, showing typical applications of mid-IR imagingin security [3] and industry manufacturing [7].

Mid-IR radiation is distinctfrom both short-wavelength infrared (SWIR) and near infrared (NIR) regions.Objects at temperature beyond about 250 K (-23 ^{o} C) can readilyemit considerable amount of mid-IRradiation (see Fig. 2.2 (a)). Mid-IR radiation is thus commonly regarded as radiation that is associated with heat. Asensitiveenough camera in the mid-IR regioncan operate without need for any additional illumination. This concept isknown as passive detection, and it has allowednight vision,an application heavily exploited in the defence and security field [3]. When further combined with proper algorithms, it can also provide functions such as illumination-free face recognition [4], motion detection [5] and night driving assistance [6]. Moreover, since the peak wavelength of theIR radiation energyemittedfrom an object is significantlydependenton its temperature, mid-IR thermal imaging is also commonly applied for non-contact, high sensitivity temperature measurement as shown in Fig. 2.2(b). This is particularly crucial for industrial chip manufacturing and maintenance.

More importantly, mid-IR region is also referred to asa “fingerprint” region since a large number of molecular species exhibit specific spectral bands of absorption, as shown in Fig. 2.3. The molecularcharacteristic optical absorption can be exploited to detectthe presence of a certain gas, and also to measureits concentration [8].When forming images, the abilityof detecting gases such as carbon dioxide (CO_2), carbon

monoxide(CO), and methane(CH_4)can further contribute toareas such as atmospheric chemistrybased on remote sensing[9]and industrialpollution monitoring [10]. Similarly, most chemical bonds, particularly from biomolecules, can interact withidentifiable mid-IR radiationdepending on their exact chemical composition and vibrational motion, providing an accurate method to determine the chemical makeup of an unknown sample(see Fig. 2.4) [11]. As a result, mid-IR spectroscopic imaging has attracted considerable attention in recent years particularly for biochemistry and is highly expected to be a competitive candidate for skin cancer early diagnostic [12].

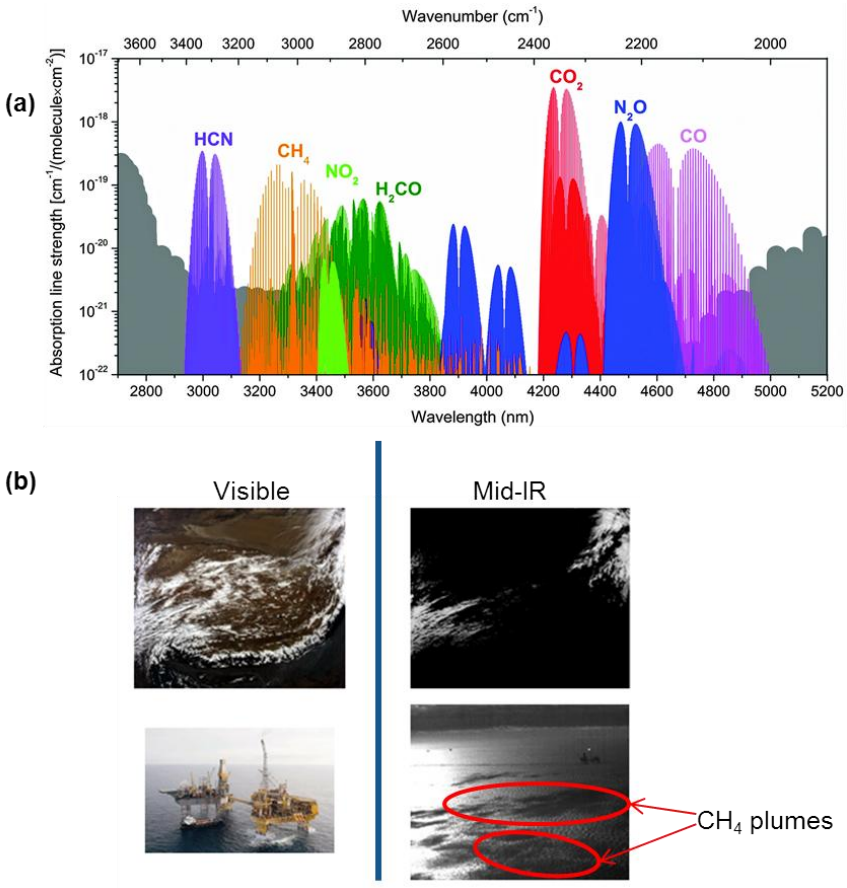


Fig. 2.3. (a)Spectral absorbance of a set of important gases in mid-IR region [8]. (b) Corresponding applications in remote sensing [9] and methane pollution monitoring [10].

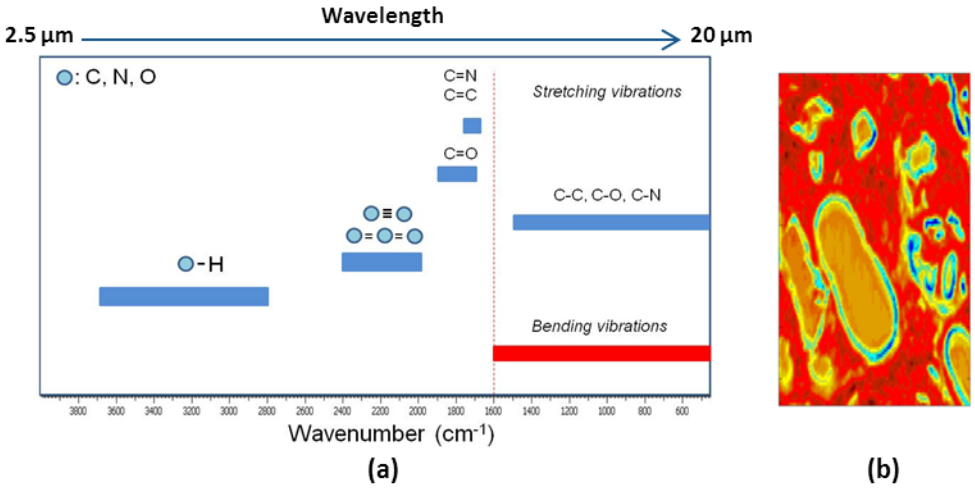


Fig. 2.4. (a) Spectral absorbance ofseveral typical chemical bondsin mid-IR range [11]. (b) Image of prostate tissue in mid-IR range [12].

2.2Mid-IRDetectors to Date

The core component of any infrared imagers is an IR detector. AnIR detector is a device that can absorb the incident IR electromagnetic radiation and convert it into measurable electric signals. According to theiroperation mechanism, mid-IR radiation detectors are mainly divided into two categories: thermal detectors and photon detectors.

In 1800, W. Herschel measured the distribution of energy in sunlight with athermometer,and found that the highest temperature reading was always just beyond the red colour light, what we now know astheIRregion [13]. Since then, early stage detection of IR light was all based on one strategy: first absorbing the energy of IR, transferring it into heat which can change the temperature of probing material, and finally quantifying the change bycertain temperature sensitive physical properties.For example, in a classicthermometer,the change of temperature is indicatedby thevolume expansion of a liquid or gas stored in a tube container. Detectors which base their operation on this energy transfer mechanism are called thermal detectors (Fig. 2.5(a)). Examples of thermal detectors arebolometers, pyroelectric detectors and thermocouples which sense atemperature induced change in resistance orvoltage,respectively[14-16].

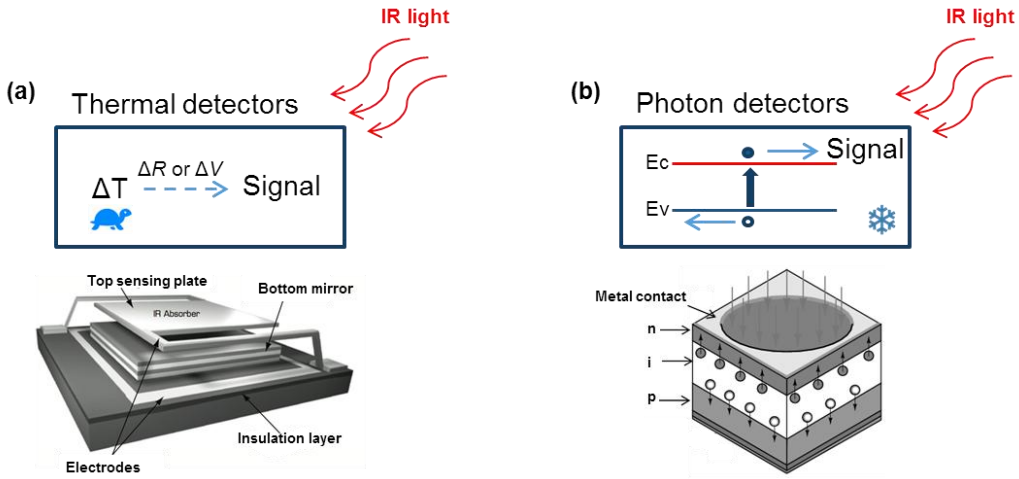


Fig.2.5. Basic operation of (a) a bolometer based thermal detector and (b) a photon detector using p-i-n junction.

Photon detection is a more advanced IRdetection method where the absorption of light, quantized as photon,will instantaneously induce an electrical signal in certain semiconductor materials [17] (Fig.2.5(b)).In a typical IR photon detector, electrons in the lower energy valence band will absorbenergy from the incident IR radiation and be excited into the conduction band. Correspondingly, an equal number of holes will be created in the valence band.These photo-generated electron-and-hole (E-H) pairs willthen be swept out and collected by electrodes when an electric field is applied, inducinga photo current signal.

Evaluating which type of detector is better is not simple. Both types of detectors have different sets of advantages and disadvantages and each hasits own irreplaceable role in state-of-the art IR detection technology.Thanks to the fast development of Micro-Electro-Mechanical Systems (MEMS), fabrication of thermal detectors with micro-size scale is now accessible.Miniaturized from the classic bolometer, amicrobolometer is a device that can be integrated on a CMOS chipon large scale production,hence allowing very low cost. However, since thermal detection relies on an indirect method to transform the energy of the IR light into an electric signal, the fundamental limit of these detectors is their slow response and low detection performance. In contrast, both fast response and extremely high IR detection performance can be achieved with photon detectors [18]. However, many photon detectors cannot work at room temperature.As a result,they are much more expensive due to cost of manufacturing and cooling equipment [19]. In fact, by exploitingnovel designs which will be detailed in a later section, in recent years the cost of photon detectors keptdecreasing. As a result, in the scientific community photon detectorsare

regarded as the dominant option for high-sensitivity sensing applications in the mid-IR "fingerprint" region, and their position is unlikely to be significantly challenged.

2.2.1Intrinsic Photodetectors

Intrinsic photodetectors are semiconductor detectors where an intrinsic (i.e. undoped) region is used as absorbing material to detect the incident light. The most common example of the intrinsic photodetector is the p-i-n photodiode. As shown in Fig.2.6 (a), a p-i-n photodiodeconsists of a wide intrinsic region sandwiched between p-type and n-type doped layers that form a p-n junction. In order to provide enough energy to generate E-H pairsin the p-i-n photodiode, it is required that the incident photon energy must be larger than the semiconductor bandgap. Therefore, the maximum radiation wavelength that an intrinsic detector can sense, referred to as the cut-off wavelength of the detector, significantly depends on the energy bandgap of the bulk semiconductor material. Due to the relatively small energy of the mid-IR radiation (<0.4 eV), only a limited number of bulk semiconductor materials can fulfilthisbandgap requirement. At presentthe most popular bulk materials for mid-IR detection are mercury cadmium telluride (HgCdTe or MCT) and indium antimonide (InSb)or related materials (InAsSb, InAlSb).

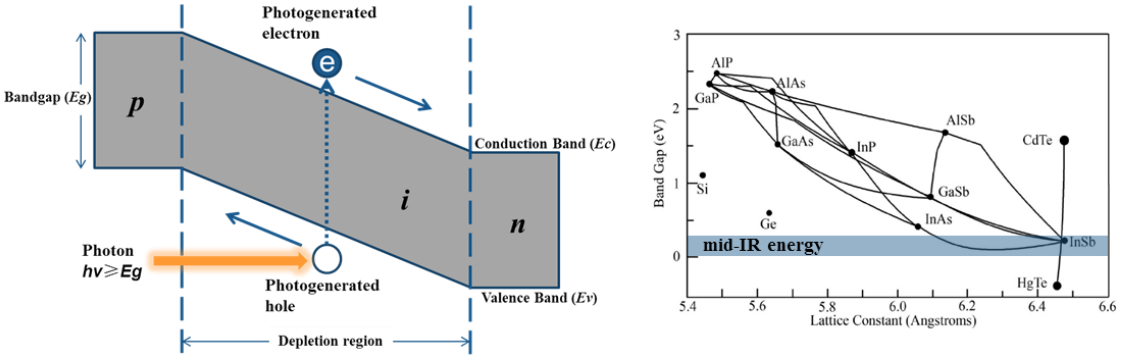


Fig. 2.6. (a) Illustration of generation of electron-hole pairs in a p-i-n photodiode structure.(b) Bandgap energy and lattice constant of various III-V semiconductors [17].

First developed in 1959 [20], MCT-based IR detectors have been extensively studied for half a century and have now become fairly mature for a number of commercial products[21,22].Since the bandgap of MCTvariesdramatically according tothe mole fraction of itselemental components, the cut-off wavelength of MCT detectors can be easily tuned to cover several wavelength spans from 2 to 20 μm,in theSWIR, MWIR and LWIR regions[23-26].More importantly, despite the ability to cover sucha wide range of wavelengths, the change of MCT composition will only introduce very little variation in the value of the lattice constant (see Fig. 2.6 (b)). This

is particularly important for bandgapengineering where MCT layers with various compositionsis required to be grown on the same substrate.However, despite providing unbeatabledetection performancein the LWIR, the MCT technology does have severe limitations.The greatest disadvantage of MCT technology is the fundamental difficulty of growing material with precise composition controldue to a number of problematic crystalline properties [17]. A finely control of thebandgap of MCT across the wafer with good uniformity is thus extremely difficult, especially when trying to achieve the longest detecting wavelengths in the LWIR [23, 27]. In this case, even 0.001 variation of mole composition change can lead to drastic effect on the detector performance [17].These growth related problems have significantly reduced the yield of MCT technology and thus dramatically increased its manufacturingcomplexity andcost.

InSb-based detectors have been commercially manufactured for IR detection also since the 1950s [13].As a binary material with bandgap down to 0.17 eV (~7.3 μm) at 300 Kand 0.23 eV (~5.4 μm) at 80 K, InSb is well matched to the MWIR region detection requirements[28].At present, InSb technology is well established and even more mature than MCT,offeringhigher device stability, lower fragility, and bettergrowth yield as a binary material [29].As in MCT, if additional elements are used to form ternary materials (such as InAsSb and InAlSb), the cut-off wavelength can be tuned also for antimonide detectors. By changing the elemental composition, wavelengths in SWIR, MWIR,anda small part of the LWIR regioncan becovered [30-33]. Moreover, because the difference in bandgaps between InSb and InAs is much less than that between HgTe and CdTe, tuning wavelength with InAsSb provides larger composition tolerance and hence hasbetter growth uniformity across the wafer as compared toMCT technology[17]. Nevertheless, due to the large lattice mismatch between InSb, AlSb and InAs, growth of thick layers of InAsSb or InAlSb with various compositions simultaneously on one substrate is not straightforward so far, limiting wider usability for these materials.

2.2.2 Quantum Well Infrared Photodetectors

First introduced in 1980s, Quantum well infrared photodetectors (QWIPs) are a relatively new technology for IR applications [34, 35]. Different from bulk detectors, the light absorption and interaction in QWIPs rely on periodic repetition of layers of two or more materials with dissimilar bandgaps. In the simplest case,as shown in Fig. 2.7, a single quantum well made of a lower energy bandgap material is sandwiched between two material layers with higher bandgap.The small and high bandgap

materialsare commonly referred to as the well and the barrier layer, respectively. According to quantum mechanical theories, when the well layer is thin enough (less than tens of nanometers), movement of carriers in this layer will be confined by the surrounding energy barriers. As a result, energy states in the well layer will be discrete due to quantum effects,and thelevels of these energy states will befully depending on the width of the well [36].

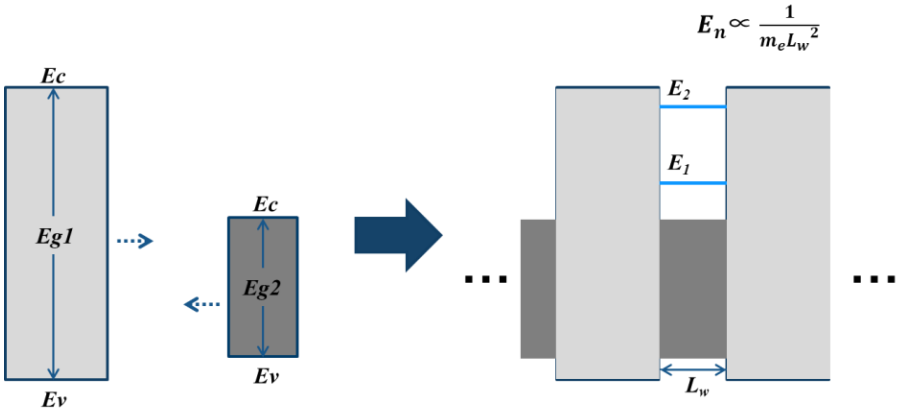


Fig. 2.7. Formationof a quantum well in a QWIP, showing the ground energy state of the well (E_1) and an excited energy state of the well (E_2).

Fig. 2.8 (a)shows the basic operation of a GaAs/AlGaAs QWIP, commonly used for mid-IR detection.Generally, the well layers of the QWIParedoped n-type to provide carriers localized in the first subband (E_1) which is also referred to as the ground state. After absorbing the photon energy, these carriers are then excited to an energy state (E_2) near the barrier energy level,where the applied voltage can sweep the carriers out of the well,forminga photocurrent. As a result, the minimumphoton energy that a QWIP can absorb is limited by the energy difference between E_2 and E_1[29].In practice, thisenergy separation is tuned by controlling the deposited well layer thickness to match the energy of the IR photons to be detected. Therefore, various quantum well structures can be designed to detect distinct wavelengths in both MWIR and LWIR regions[37, 38]. Due to negligible lattice constant mismatch between GaAs and AlGaAs, QWIPs based on these materials can be grown with very high quality and uniformity,on large wafers [39, 40].

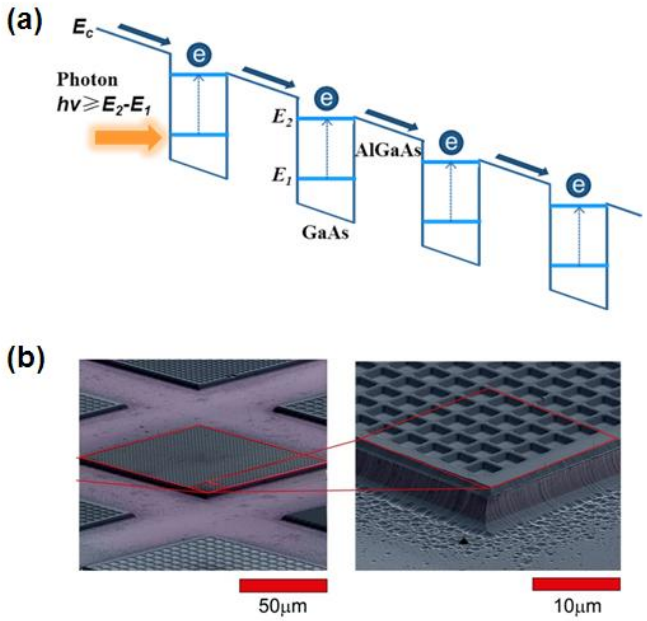


Fig. 2.8. (a) Band diagram of QWIP structures, showing the mechanism of photocurrent generation. (b) Scanning electron microscopy (SEM) image of a QWIP after fabrication of diffraction gratings [43].

However, one major problem with n-type dopedGaAs/AlGaAsQWIPs is that their optical absorption strength is dependent on the direction of the electric field associated with an incident photon. The absorption will be maximised when the field polarisationdirection is normal to thequantum wells. This means that a normal incident light, whose polarization is entirely in the plane of quantum wells, is not going to be absorbed [41]. Although this problem can be eased by introducing a diffraction grating patternon top of the device to angle any normal incident light (Fig. 2.8 (b)),but it results in sacrificed quantum efficiency [42, 43].QWIPs are also very sensitive to operating temperature since carriers can easily be thermally excited between the E1 and E2 states, producing dark current. As a result of these two disadvantages, QWIPs are not able to achieve same levels ofperformance as bulk detectors,even under cooled operation [44].

2.2.3 Type-II SuperlatticePhotodetectors

With lattice constants all closely matched to 6.1 Å, InAs,GaSb and AlSb forma very specialgroupof binary semiconductors. High quality growth of heterostructuresbased on these lattice-matched materials can thus be achieved, providing a great opportunity for quantum physics based bandgap engineering [45].When thin layers of InAs and GaSb stackedperiodically, they form a so called “superlattice” structure (SLS), where a unique staggered (type-II) band edge alignment will be formed. This allows quantum wells for electrons and holes to be formedwith new quantized energy states located in both conduction and valence band as shown in

Fig.2.9. Furthermore,if therepeatedly stacked InAs and GaSb layers are thin enough to allow effective tunnelling in between the wells, these quantized energy states will be able to blur together despite being separated spatially in the different material layers, creatingnew conduction and valence minibands in the superlattice [46].These mini-bands will define theeffective bandgap Eg* (see Fig. 2.9) that determines the absorption wavelength of the final manufactured superlattice detector. Exploiting the type II transition allows to overcome the intrinsic bandgap limitations posed by theconstituent InAs and GaSb layers.

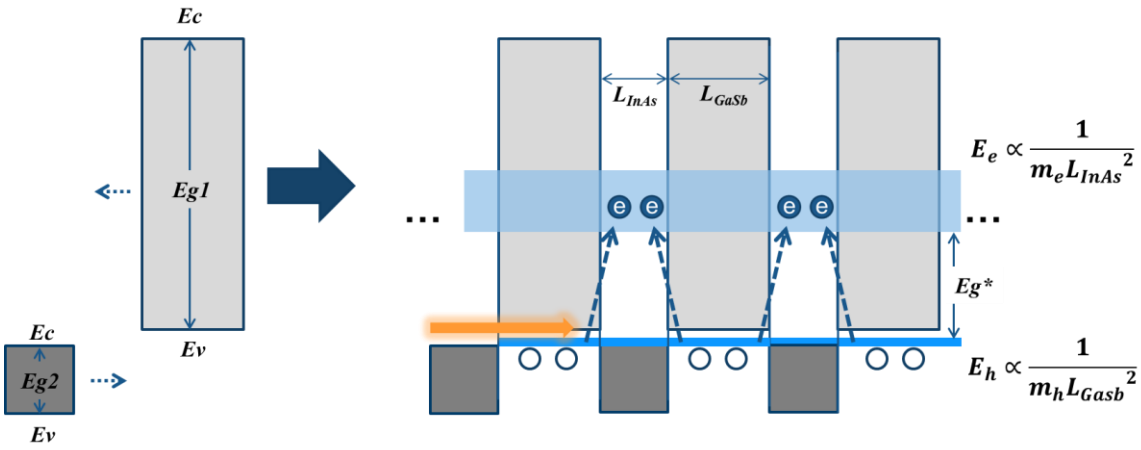


Fig.2.9. Illustration of a type-II superlattice structure, highlighting the formation of mini-bands with effective bandgap Eg*.

Given the quantized energy level in a quantum well depends significantly on the width of well layer, changing the deposited thickness of both the InAs and GaSb layers can lead to efficient tuning of the effective bandgap from 0 to 250meV[47]. As a result, InAs/GaSb superlattice photodetectors have the ability to detect wavelengthsranging from 3to 30μm, covering allregions of the mid-IRas the MCT detectors [48-51].Although relyingon a quantum well structure, optical transitions in the superlattice material occur between spatially different layersand thus high quantum efficiency can be achieved also for normally incident light without need for diffraction gratings [17].

Despite the numerous promising advantages,the theoretically predicted superior detection performance of superlattice detectors has not been realizedyet. When compared with the well-knownRule 07 (a heuristic model to predict performance of the state-of-the-art MCT detectors [46]), the dark current densitiesobtained from InAs/GaSb superlattice detectors are still considerably high especially when layers are engineered for detectionin the MWIR region (Fig.2.10). The main reason for the higher dark current in superlattice detectors is theirshortminority carrier lifetime,caused by the presence of Shockley-Read-Hall (SRH) trap centres [52, 53]. Although over the last few

years great effort has been made to accurately measure and increase minority carrier lifetime in superlattices [53-56], the origins of the SRH centres are still not well understood, hindering a wide adoption of this type of detector.

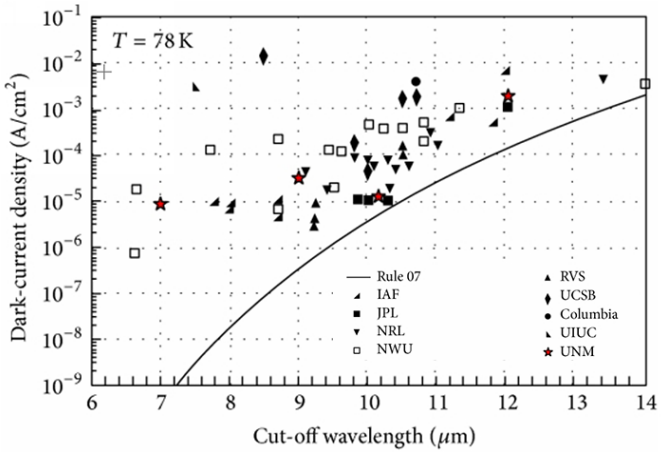


Fig.2.10. Dark-current density of type-II superlattice detectors compared with Rule 07 [46]. Abbreviations for the different institution working on this kind of detectors. These include: Fraunhofer-Institut (IAF), Jet Propulsion Laboratory (JPL), Naval Research Laboratory (NRL), Northwestern University (NWU), Raytheon Vision Systems (RVS), University of California, Santa Barbara (UCSB), Columbia University (Columbia), University of Illinois, Urbana-Champaign (UIUC), and University of New Mexico (UNM).

2.3Focal Plane Arrays

While optimizing the detection performance of various kinds of single detectors for “sensing”, people have never stopped making effort to realize image sensors in order to “see” the mid-IR light. The termfocal plane array (FPA)refers to an arrayof individual detector elements (pixels) located at the focal plane of the optical path, which is the fundamentalcomponent of all digital imaging systems [19].

At the early stage, detectors with electrical contacts were simply assembled together to form a 1-dimentional (1D) multi-element array. As shown in Fig. 2.11(a), in order to obtain an image by a linear array, the given scene has to be scanned by a rotating mechanical scanner.Since the late 1970s, linear scanning arrays employing 60, 120, or180 MCT photoconductive elementshave beensuccessfully commercialised and they arenow commonly referred to as the first-generation FPAs [57， 58].However, these scanning array systemsrequirea massive number ofconnections to read out signals from each detector element.As a result, increasing the detector number beyong few hundreds with this approachwas found to be impractical.

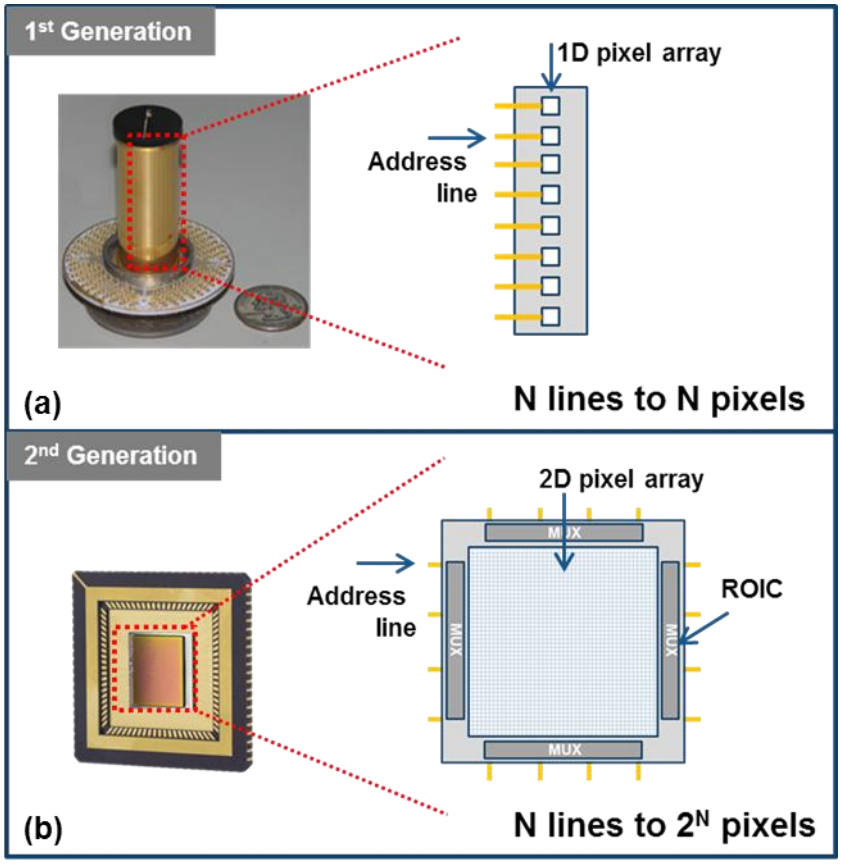


Fig. 2.11. Image and schematic of (a) the first-generation linear array [57] and (b) the second-generation staring array where pixels are configured in 2D format and integrated with ROIC.

Driven by the demand of placing more detectors into the array and thus obtaininga higher image resolution, second-generation FPAs(also known as staring arrays)werethen developed. Fig. 2.11(b)shows a typical structure of the staring arrays, in which individual detectors are configured in2-dimentional (2D) format and scanned electronically by readout integrated circuits(ROIC)[58]. Thanks to thesignal multiplexing functions provided by ROIC,the number of connection wires required for addressing each pixel in a staring array is significantly reduced,meaning thearray sizecould quickly and relatively easily be increased.At present, with the fast upgrading of integratedcircuit design and fabrication technology, IR FPAs with megapixel size can be readily achieved [59-61]. Staring arrays thus achieved a pixel densityat least three orders of magnitude highercompared with first generation systems.

Depending on how the ROICsare implemented and interconnected with the detectors, modern IRFPAs can be classified intoeither monolithic or hybrid designs.

2.3.1 Monolithic Designs

In a monolithic FPA, both the light detectors and signal readout circuits are implemented on the same substrate and can thus be manufactured simultaneously with

identical processes. The most representative examples of monolithic FPAs are the silicon-based charge coupled devices (CCDs) and complementary metal-oxide-semiconductor (CMOS) imagersthat arewidely used in modern digital cameras for photography in the visible range[62，63].

2.3.1.1 Fully SiliconCompatible Designs

Unfortunately, the massively used bulk silicon substrate on its own is not sensitive toinfrared light since its bandgap is much larger than the energy that any infrared radiation can provide. As a result, exploring extrinsic ways to expand the imaging ability of the silicon-based arraysbecame an early approach for making monolithic infrared FPAs.In 1973, *Shepherd* and *Yang*proposed the first infrared sensitive PtSi/Si Schottky barrier detector (SBD) which was fully based onsilicontechnology [64]. As shown in Fig. 2.12, PtSi/Si SBDs generally operate in back illumination mode, with the IR radiation absorbed in the PtSi metal. Instead of crossing the large Si bandgap, the photo-excited hotholesare designed to step over the energy barrier(~0.22 eV) formedat the metal-semiconductor interface,leaving the PtSi charged negatively. Afterwards, these charges can then be readout fully by relying on standard visible digital camera architectures, either CCD or CMOS [65，66].Since fabrication of SBD can utilise well-established silicon very-large-scale integration(VLSI) processes, this technology quickly became maturefor FPAs implementation in the SWIR, MWIR [67, 68] and even in part of the LWIR region, thanks to the development ofan appropriatemetal. IrSi [69].Large-area and high-density arrayswith size up to 1040×1040were readily achieved,showing good thermal imaging quality under 77K cooling [70，71].

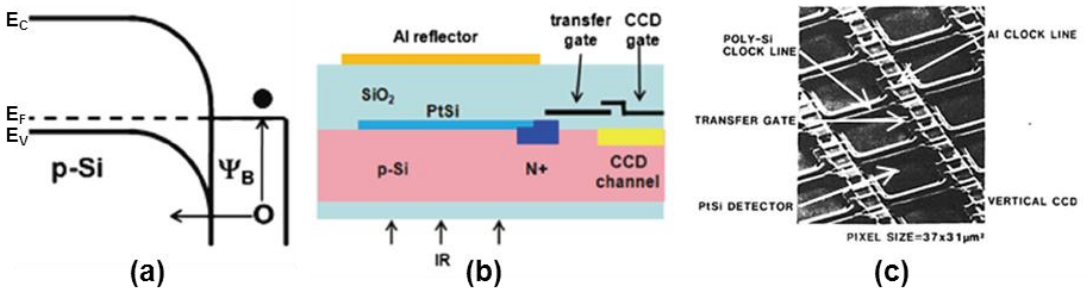


Fig. 2.12. (a) Band diagram and (b) cross-section of a SBD being integrated with Si-based readout (c) SEM image of a fabricated FPA device based on SBD [57, 64].

Although successful to a certain extent,SBD technology still has a number of issues. The most notable one is the relatively large dark current due to the nature of free carrier absorption process. This theoretically prohibits operating these FPAs under higher temperature. Other issues such as poor quantum efficiency (<1%) and poor

photo-response uniformity are also hard to overcome without significant technology breakthroughs [57].

2.3.1.2 MIS-based Structures

Roughly at the same time of SBD technology becoming mature, rapid advances were made in narrow bandgap semiconductor materials and their corresponding processing techniques. Utilizing these IR sensitive bulk materials to imitatesilicon-based device architectures, metal-insulator-semiconductor (MIS) structures (see Fig. 2.13), was of greatresearch interest during 1980s since it was expected torealize new monolithic FPA approaches with better detection performance as compared to SBDs.

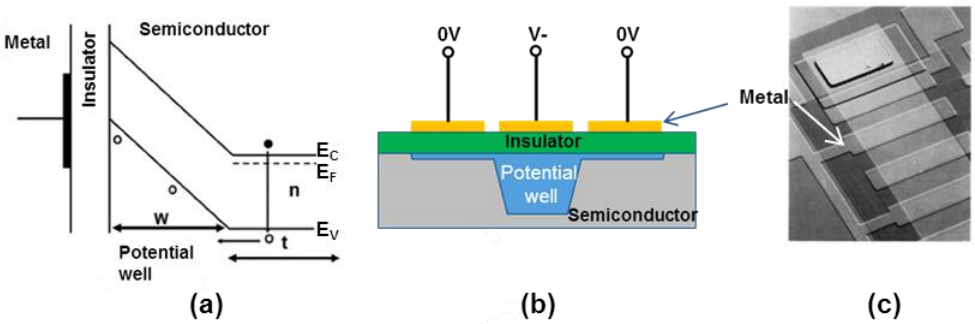


Fig. 2.13. (a) Band diagram and (b) cross-section of theMIS structure (c) SEM image ofa linear MIS CCD array [57, 74].

Previously, the main concerns for making MIS devices on narrow bandgap materialswere due to the lack of a proper passivation method to suppress the leakage current associated with surface states [72]. After years of systematic comparison with many other options including SiO_x, Al_2O_3, SiO_xN_y, TiO_2 and the native oxide, researchers at Santa Barbara Research Centerchose to use low-temperature chemical vapor deposited (LTCVD) SiO_2 as insulating layer and successfully achieved very low InSb-SiO_2surface-state density down to $8x10^{10}$ cm^{-2}under 77K cooling. Withsuch good suppressing characteristics, thestorage timeand capability of theses InSb-based MIS devices wouldonly be limited by bulk rather than by theleakagecurrent introduced by surface states [73].

As an outcome, linear arrays with 20 elements and 4-phase scanning gate approach were then fabricated and tested functional [74].In 1980, MCT-based MIS structureswere also successfully developed and 32 elementsand 4-phase CCD arrays were demonstrated [75]. Despite the successful demonstration of linear CCD arrayswith InSb and MCT, it was not until 1995 that2D infrared CCD arrayswere developed, and only fabrication of a 128x28 test array was achieved onMCT platform [76]. The difficulty in

making 2D arrays lies in the poorcharge transfer efficiency (CTE) of MIS devices. CTE is defined as the fraction of stored charges that can be successfully moved to the next potential well per transfer, and in narrow bandgap materials is very poor (0.978 for InSb and 0.999 for MCT) compared to that of typical silicon-based devices (0.99999). This implies that a large size CCD array, where a huge number of charge transfers are needed for readout cycle, is not achievable with narrow bandgap materials.

Given this intrinsic limitation in IR CCD devices, efforts were then switched to more fault-tolerant charge injection devices(CID)and charge-imaging matrices (CIM). Instead of fully basing the signal readout on shifting the charges in between potential wells, silicon chips are introduced to assist signal multiplexing and pre-amplification.Therefore, these arrays require much less number of transfers per readout as compared to CCD devices. In this case, each unit cell isconnected to silicon scanner chips through a common row line (X) and a common columnline(Y) respectively, andhencean X-Y addressingscheme can be built,as shown in Fig. 2.14.Progress in CID and CIM technology has led to relatively large size (128×128) staring arrayson both InSb [77] and MCT [78].More importantly, based on successful demonstration ofMCT-based MIS field effect transistor (MISFET), digital integrated circuits including amplifiers, shift registers, and correlated double samplers were also reported [79].All these achievements have suggested that making a “CMOS-like” fully monolithic infrared FPA isalso possible.

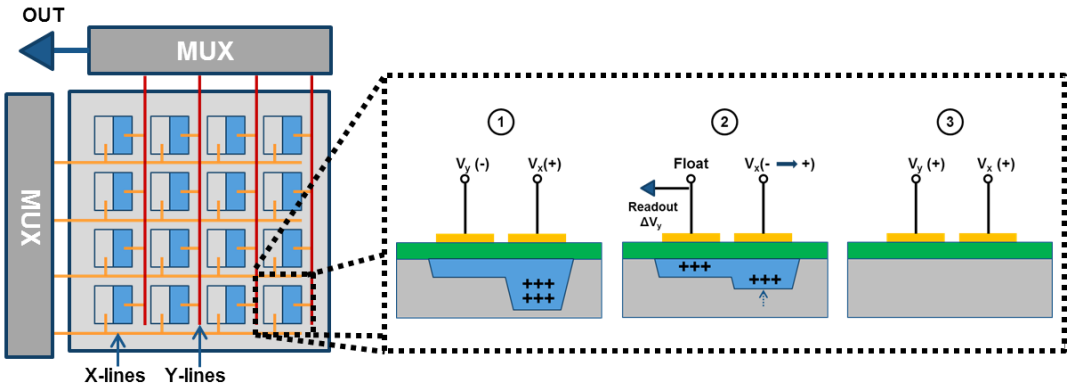


Fig. 2.14. Illustration of the X-Y addressing scheme in a CID based array device, highlighting the charge transfer process: charge generation,signal sensing and potential well reset.

Nevertheless, due to very small bulk breakdown voltage of InSb and MCT (<1/10 of silicon), the amount of charge that can be storedin the wells of MIS devices made onnarrow bandgap materials is notably less than devices made on silicon technology [80]. This inherent issue makes pixel size scaling and long-time integration (used for

better detection performance)inapplicable.Besides, theses MIS devices also suffer problems such as requiring very high material quality, poor signal linearity and unacceptably high magnitude of 1/f noise even under 77K cooling [19, 80]. As a result, development of monolithic designs including CCD, CID and CIM based on narrow bandgap materials has been completely abandoned.

2.3.1.3 Evaporation-based

Modern monolithic integration thoughts are focused on keeping the well-established silicon ROIC chip as the only handling substrate and then depositing infrared sensitive materials on it. This method is particularly popular in thermal detector FPAs [81, 82]. However, finding a material that can be deposited directly to form photon detectors on silicon chips is not trivial. So far, only the lead salt materials such as PbSe and PbScould be used due to their capability of infrared detection even under polycrystalline condition [83].

In late 1970s, although polycrystalline PbSe could be prepared by either chemical bath deposition (CBD) or vapor phase deposition (VPD), the photoresponse uniformity, long term stability and high 1/f noise associated with the poor material quality had halted its further development. The most recent progresses in polycrystalline PbSe thin film deposition have brought attention back to PbSe. *G. Vergaraet al.*reported a newly developed special VPD method which coulddepositIR sensitive polycrystalline PbSeonto Si ROIC chips [84]. As shown in Fig. 18, thin films of PbSe can be directly deposited and patterned by lift-off, then connected to the metal pads on the CMOS chip. Based on this technique, monolithic FPAs with sizesranging from 32x32 to 80x80were demonstrated,providing higher detection performanceby an order of magnitude when compared to FPAs based on thermal detectors at ambient temperature [85-87].

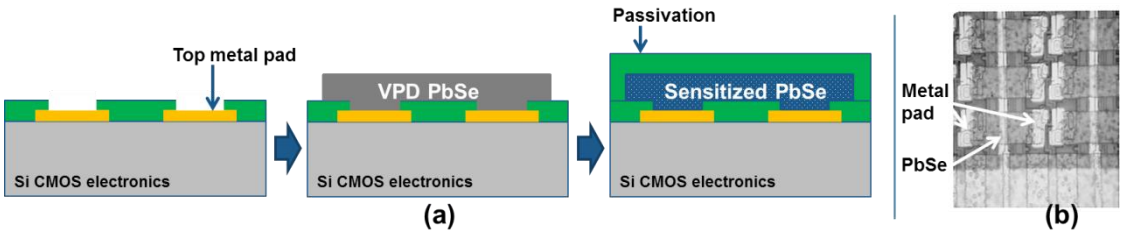


Fig. 2.15. (a) Basic processing stepsformaking a PbSe-based photodetector on a CMOS chip. (b) SEM image of a completed FPA after PbSe evaporation [83].

What remains amajor problemof VPD prepared polycrystallinePbSe thin film is the large 1/f noise caused by the low material quality, making the promised performance only achievable at high chopping frequency (> 600Hz) [88].Furthermore, there is still

lack of a proved physical theory to explain the detection capability of polycrystallinePbSe. The as-grown polycrystalline PbSe film is not sensitive to infrared radiation regardless of deposition techniques until it is sensitized by high temperature annealing (from ~400 ℃ to 600 ℃ [89, 90]) in a certain atmosphere (e.g.I_2 and O_2). Considering the typical ~450 ℃ thermal budget limit of CMOS electronics, further improving the detection performance of polycrystallinelead salt based FPAs by increasing the annealing temperature can be challenging. Additionally, the bandgap of PbSe is not tunable and thus limited to detection inthe MWIR region.

2.3.2 Hybrid Designs

In the case of hybrid FPA technology, arrays of photodetectors and ROICsare realized independently, and these two separately manufacturedcomponents are then assembled together through various interconnection techniques.

2.3.2.1 Flip-Chip Bonding

Firstdemonstrated in thelate 1970s [91], indium bump based flip-chip bonding has been widely applied to makeinterconnections for hybrid FPAs. Fig. 2.16shows the basic processing steps of the flip chip bonding technique. First, infrared sensitive materials are etched into individual mesas to define the active area of each photodetector. The photodetectors are then passivated followed by window opening and formation of Ohmic contacts.Due to the nature of hybrid designs, each detector in the array requires one-to-one interconnection to the readout circuits. Therefore, indium bumps are deposited ontoevery detectormesa by thermal evaporation. Similarly, thesame number of indium bumps is also formed on the multiplexmetal pads of the Si ROIC chip correspondingly. Assisted by flip-chip bonder, the detector chip is then flipped over and aligned to the Si ROIC chip. Afterwards, the two chips are pressed together and the temperature is increased, to fuse the indium bumps together and achieve successful bonding.

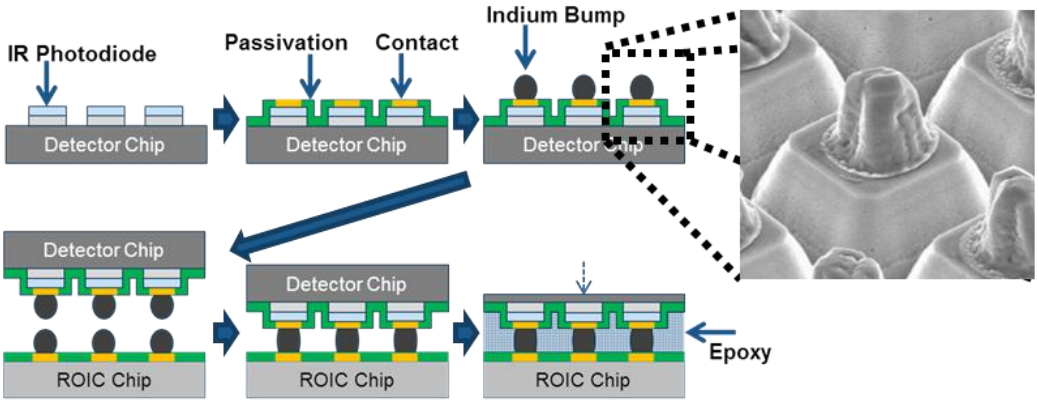


Fig. 2.16. Basic processing steps of hybridization process based on the flip-chip bonding technique, including indium bump formation, chip alignment, bump bonding and epoxy under-filling. The inset figure shows a zoomed-in SEM image of indium bumps formed on top of photodiode mesas.

Themost attractive advantageof this technique is the great ease of design since IR detectors and ROICs can be optimised independently. Moreover,since the silicon platformwill provide robust readout circuits, the high performance photodetectors mentioned in Section 2.3 can be readily adapted for making infrared FPAs without considering their own capability of making electronic circuits [92-95].In the meantime, the development of ROIC chip will also benefit from the fast evolution of CMOS technology where more and more on-chip signal processing functions can be integrated, creating new possibilities for extremely large format FPAs with high spatial resolution [96, 97].Moreover, since all the electronic readout circuits are realized externally, the whole space of the light sensitive semiconductor material can be used to define photodiodes. This approach thus allows achieving a near 100% fill factor which is highly desirable for making a sensitive image sensor for low incident light level.

Despite the great success that the flip-chip based hybrid approach has achieved, there are also clear challenges associated with this technique.The high number of additional steps related to die-level flip-chip bonding technique has dramatically increased the cost of photon detector based infrared FPAs. For example,in order to make tall indium bumps required by standard flip-chip bonding, very thick photoresist (>20um) is required. Therefore, extra attention for resist-coating and patterning such a thick layer onsmall diced detector arraysorROIC chips isrequiredto preventunacceptable edge bead from affecting the lift-off process [98]. In addition, epoxy underfilling ofthe gap between the two chips during bonding is another delicate step which is generally necessary to increase the bonding strength after hybridization [99].

More importantly, due to the coefficient of thermal expansion mismatch between narrow bandgap substrates (e.g. MCT, InSb and GaAs) and Si substrates, the indium bumps are subject to considerable stress during thermal cycles between 300K and 77K, the standard operation temperature for flip-chip bonded FPAs[100]. If not carefully suppressed, fatigue limit of indium bumps willbe reached quickly resulting in possibility of connection failure and even material cracking in the worst cases[101, 102] (see Fig. 2.17). Substrate thinning or removal is a possible method to decrease the thermal mismatch, but at theexpense of further increase in the fabrication complexity.

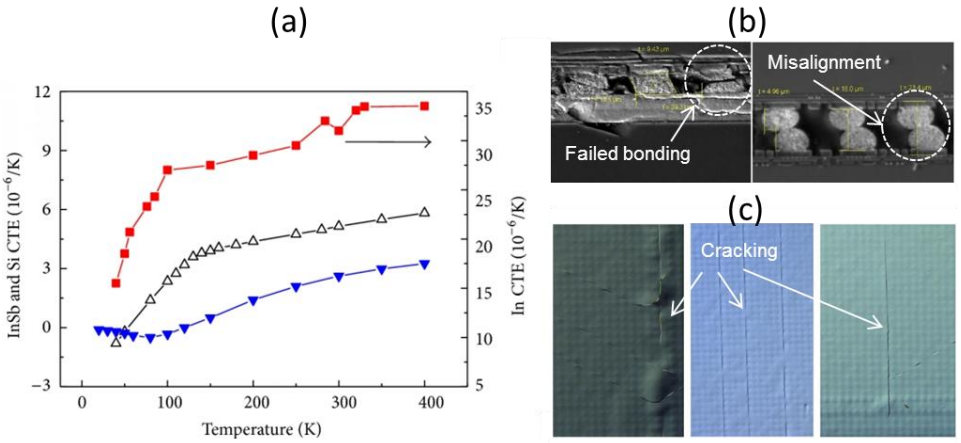


Fig. 2.17. (a) Coefficients of thermal expansion depending on temperature for InSb, indium bumps and silicon ROIC. (b)(c) Some typical fabrication issues associated with flip-chip bonding technique if the thermal expansion mismatch is not fully suppressed [101].

2.3.2.2 Loophole Interconnection

Another way to hybridise detector and ROIC chip is the use of the loophole interconnection technique shown in Fig. 2.18.In this case, p-type detector substrate is directly glued to ROIC substrateusing epoxy to form a single chip before fabrication. Ion beam milling is then applied to drill loopholes on this hybridized chip until stopped by the multiplex metal pads of the ROIC. Similarly to ion implantation, the etchingprocess itself also drivesdopant diffusion into the detector substrate, creating the p-n junction for defininga photovoltaic detector array [103, 104]. Since the drilled loopholes have sloped sidewall shape, electricalinterconnection between each detector and its corresponding multiplex pad can be formed by metallization. The loophole technique provides much more reliable bonding strength and thus greatly simplifies the scaling of the pixels. This technique is now further referred to as VIP(vertically integrated photodiode) and recently it allowed achieving the highest density FPA with

pitch down to 5μm [105, 106].The possibility for VIP of achieving even smaller pixel sizeshas also been predicted [107].

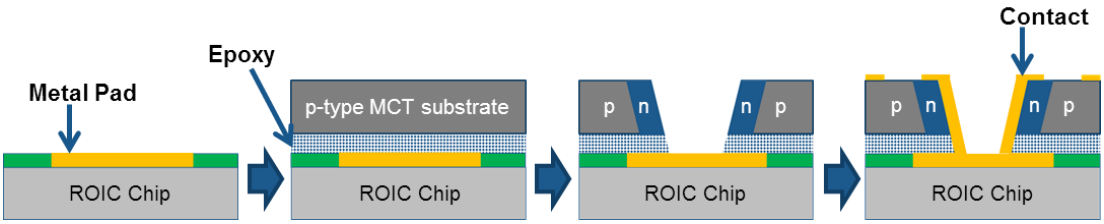


Fig. 2.18. Basic processing steps for making a hybridized FPA by loophole interconnection technique

Although so far there are no reports in the literature pointing out any drawback of this approach, the loophole technique is not commonly applied for makingIR FPAs. This may implysome difficulties were encountered when developing fabrication process steps such as epoxy-based chip bonding, ion beam milling and dopant implantation. Moreover, since photodetectors are formed by high power ion milling and implantation, the materials and device structures that can be adaptedfor VIP are limited. So far, MCT was the only candidate that proved suitable forthe loophole technique.

2.4 New Trends and Concepts

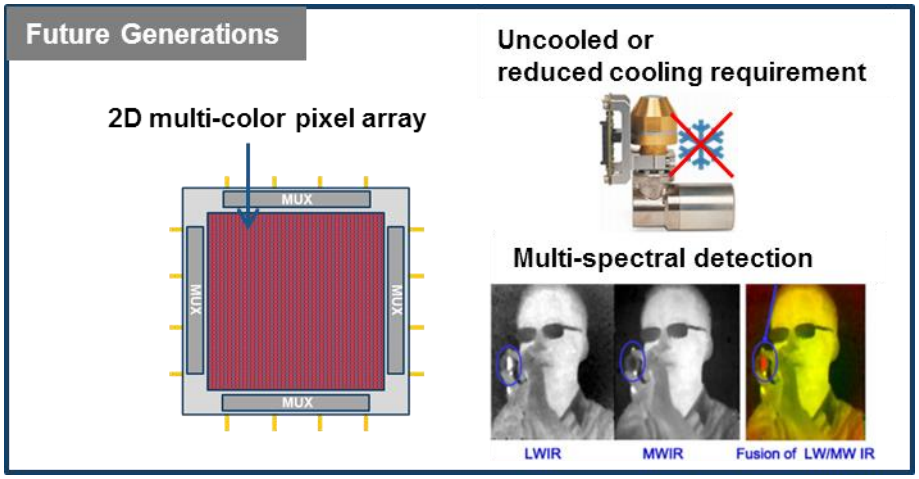


Fig. 2.19. Future developing trends for implementation of IR FPAs: achieving multi-spectral imaging capability and operating at room temperature.

As shownin Fig. 2.19, it is predicted that the future developing trend of high performance mid-IR FPAs will be focused on several key challenges, such as adding new functionalities (e.g. multi-spectral detection) and reducing cost by removing the need for cooling equipmentorby simplifying fabrication[108].

2.4.1 Multi-Colour Function

A colour image can provide not only a better-looking display but also useful information from different wavelength bands and hence enhancethe object discrimination or identification. This is particularly true for the IR radiation, where various wavelength regions/windows present unique capability of sensing temperature changes, gas concentrations and molecule make-ups (Section 2.1). Simultaneous collection of signals fromtwo or threeof the infrared windowsisthus highly appreciated over single band detection and has already become one of the key requirementsof the third generation infrared FPAs [109].

Two main approaches are available to obtain multi-spectral detection: one way is to use of color filters and splitters, at the price of increased imager complexity; another way is to have the absorbing material in each pixel able to absorb and interact with a wide portion of the infrared spectrum.Due to the large wavelength span required, only alimited numberof semiconductor material systems can tune their bandgap for detecting allof the SWIR, MWIR, LWIR windows (1-12μm)simultaneously. Among these materialsystems, MCTand QWIPs have beendeveloped for years and are now commercially availablefor multi-band infrared detection [40, 94,110, 111].However, they both have severe drawbacks, as discussed in Section 2.2.In contrast, the great bandgap tuning flexibility and high detection performance have made the Type-II Superlattice the most attractive material system for developing third generation infrared FPAs with multi-color function.

Type-II superlattice materials allow using asinglematerial system,with two or more photodiodessensitive to various wavelength rangesstacked onto each other to make multi-colour infrared detectors. Generally, thesephotodiodes areplaced in a back-to-back configuration(e.g. p-n-p)and they share common contact layers for minimum device complexity. As shown in Fig.2.20, there are two distinct strategies to activate the multi-colour function.

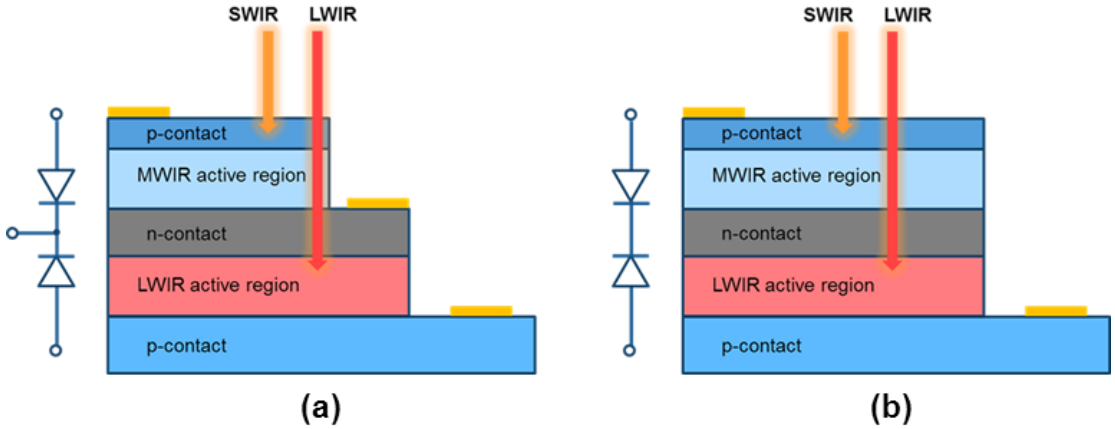


Fig. 2.20. Schematic diagram of a dual color IR detector with (a) three terminal contacts to access each photodiode independently and (b) two terminal contacts to access each photodiode by different biasing condition.

The first approach is accessing each photodiode independently with metal contacts (Fig. 2.20 (a)). Advantages of this approach include ease of design and simultaneous readout of signals generated by different infrared wavelength bands. The increased number of metal pads, however, makesimplementation of indium bump hybridized FPAs very challenging,due to the multiple interconnections required in this case. As a result, only dual-band (MWIR-LWIR) detectionhas been demonstrated so far by addressing the photodiodes independently [112, 113].

Another approach is triggering the readout of signals from various absorption layers selectively by different biasing condition (Fig. 2.20 (b)). The design of this kind of multi-color detectors is slightly more complexas additional care is required to control the electrical field across the whole device when biased [114].However, the relaxed requirements of this approach in terms of number of metal contacts make it suitable for use with well-established one-to-one hybrid technology to fabricate multi-color FPAs. As shown in Fig. 2.21, a three color detector (SWIR, MWIR, LWIR) has been recently demonstrated for the first time, needing only two metal contacts.This demonstration could evolve into the fabrication of FPAs,leading to a future demonstrationof an “RGB” infrared imaging[115].

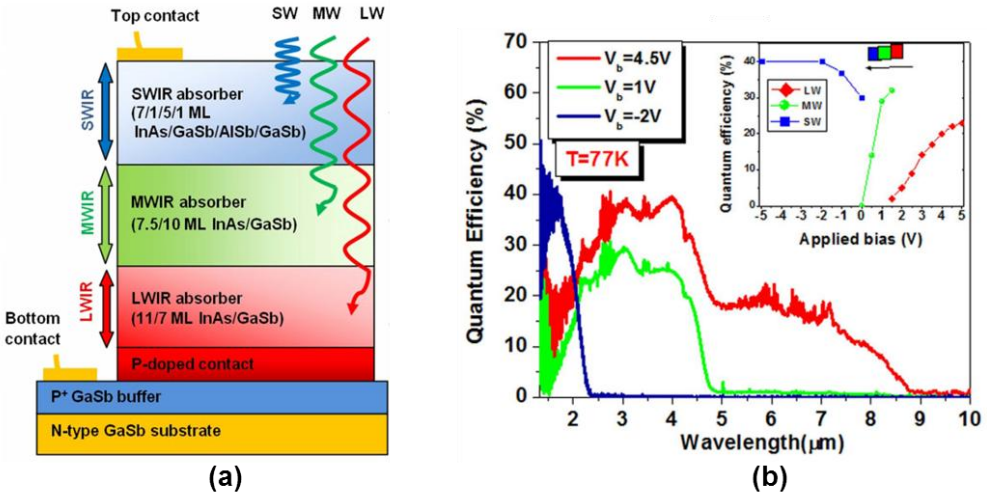


Fig.2.21. (a) Schematic diagram of a triple-band SWIR-MWIR-LWIR photodiode structure with two terminal contacts. (b) Quantum efficiency spectrum of the photodiode as function of applied bias, demonstrating the triple-band detection capability [115].

2.4.2 High Operating Temperature

Cryogenic cooling is currently required by high performance infrared photon detectors to avoid huge thermal generation noise associated with the notably narrow bandgap of absorbing semiconductors [116]. However, this crucial cooling requirement is unlikely to be achieved unless pricy and bulky equipment is attached. In order to reduce the cost and size of current mid-IR imaging systems for portable application, realisinghigh operating temperature (HOT) photon detectors is paramount.Suppressionof the thermallygenerateddark current naturally becomes a main future research direction of mid-IR technology.

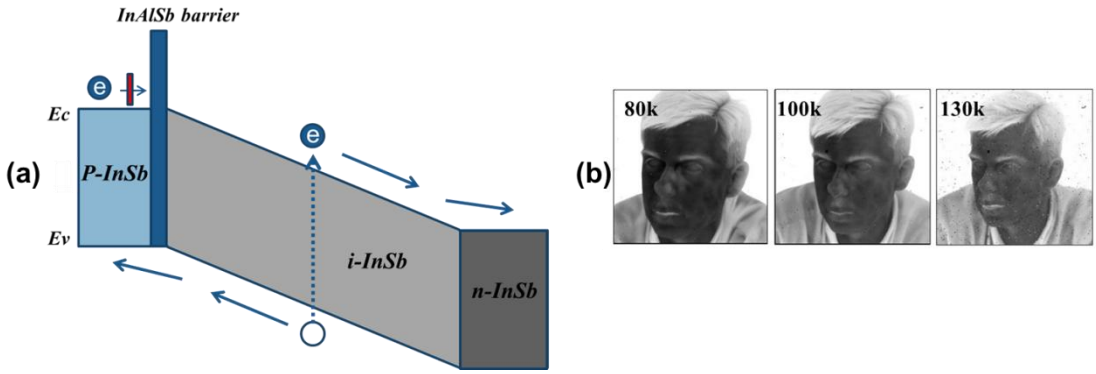


Fig. 2.22. (a) Band diagram of an InSb based nonequilibrium photodiode. (b) Mid-images from a FPA that made by this nonequilibrium photodiodes, highlighting increase of operating temperature for approximately 50K [119].

The first effective way to suppress the thermally induced dark current in infrared photodetectors is the addition into the standard photodiode structures ofa current blocking layer, with a much wider bandgap than the absorbing material. In 1996, *T. Ashley, C. Elliott et al.*proposed anovel InSb detectorstructure which showed feasibility

for near room temperature operation [117,118]. In this approach,an InAlSb “barrier”, providing a conduction band offset with its wider bandgap, is inserted in a standard InSb p-i-n photodiode (see Fig. 2.22(a)).This barrier can effectively block the flow of electronsbetween the p+ contact layer and intrinsic layer, while allowing flow of the holes with a negligible offset in valence band. When this“pBin” photodiode structure is slightly reverse-biased, carriers can be extracted from the intrinsic absorption layer, showing a lower electron concentration value as compared to the equilibrium condition [118]. Accordingly,the dark current associated with Auger generation-recombination, which is proportional to the free carrier concentration, is suppressed and thus the detector maintainsgood performance athigher temperature[119]. This kind of detector is thus named as a nonequilibrium photodiode and it allows an increase in operating temperature of several tens of degrees (from 77K to 130K), as shown inFig. 2.22 (b). For civilian applications such as gas detection and human body detection, where moderate detectivity is acceptable, the nonequilibrium photodiodes can readily operate even under ambient temperature [120, 121].

A breakthrough to further increase the operating temperature was achieved by *Maimon* and *Wicks*who proposed a novel “nBn” detector structure in 2006 [122]. In this design, the suppression of dark current also relies on the barrier. But, differently from the nonequilibrium photodiodes,the barrier is inserted in between then-type doped narrow bandgap absorption layer and the contact layers, as shown in Fig. 2.23.The barrier allows photogenerated electron-hole pairs to be collected by the contacts while blocking the majority carrier dark current. When biased under operating voltage, the electric field profile is concentrated across the thin barrier layer, so that the n-type absorption layeroperates in flatband or with very little depletion. As a result, the dark current induced in the narrow bandgap absorption layer by the Shockley-Reed-Hall (SRH) process is inhibited [123]. Furthermore, surface currents can be suppressed if the barrier layer is not etched in processing, i.e. mesas are defined from the contact layer material only. Given most of the dark current components have been suppressed, nBn detectors are able to operate under really high operating temperatures (200K) which can be readily achieved by low cost thermoelectric coolers [124-126].

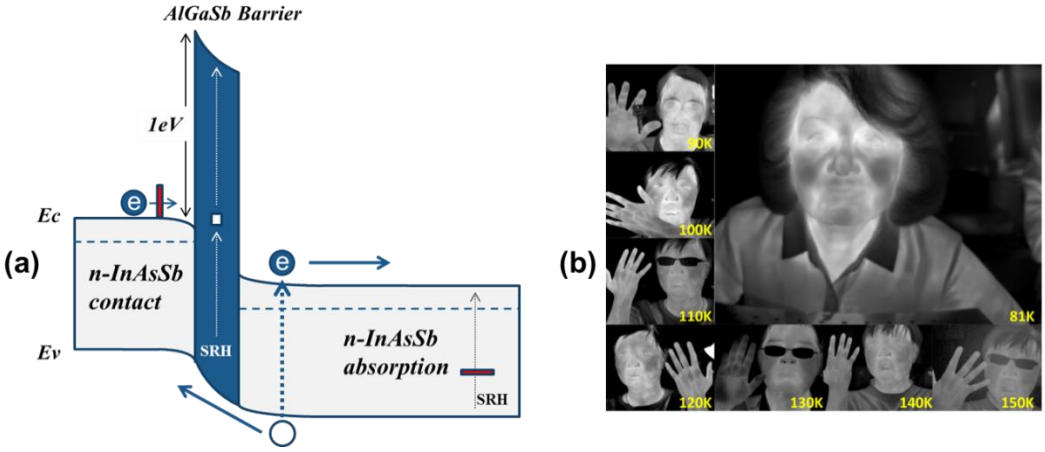


Fig. 2.23. (a) Band diagram of an InAsSb based nBn detector in which the thermally generated current is significantly suppressed. (b) Using a FPA with nbn detectors applied, excellent mid-IR imagescan be obtained, showing human blood veins upto 150 K [124].

Another playground for increasingoperating temperatureof mid-IR photodiodes is offered by photo-signal enhancement used to increase the responsivity or quantum efficiency (QE). For example, fabrication of the photodiodes into photon crystal structures can introduce light trapping processes and demonstrate higher quantum efficiency as compared to standard detectors with the same material volume. In other words, this approach makes further dark current reduction possible in a given detector by using less material, while not sacrificingQE. This concept has been recently demonstratedonboth MCT and InAsSb platforms(see Fig. 2.24) [127, 128]. Finally, plasmonic based techniques are anothervery promising area, since another degree of freedom for designing mid-IR photodiodes can be provided by manipulating the incident light. As described in [129], a “lens-like” metal antenna structure can successfully confinethe incident mid-IR radiation into a small active detection area for detecting, hence further reduced dark current and increased operating temperature can be expected.

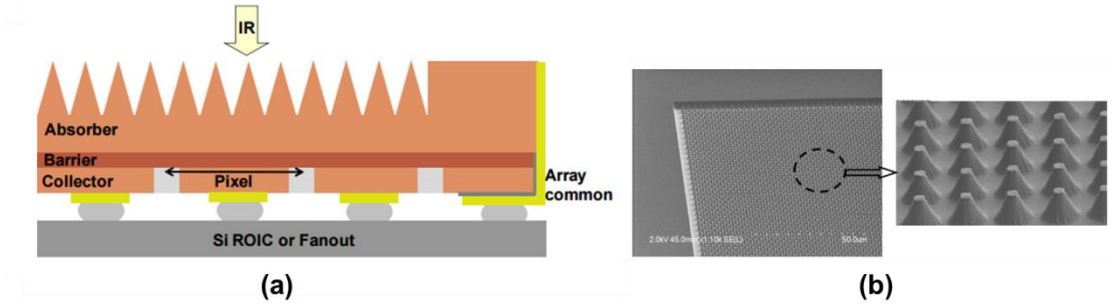
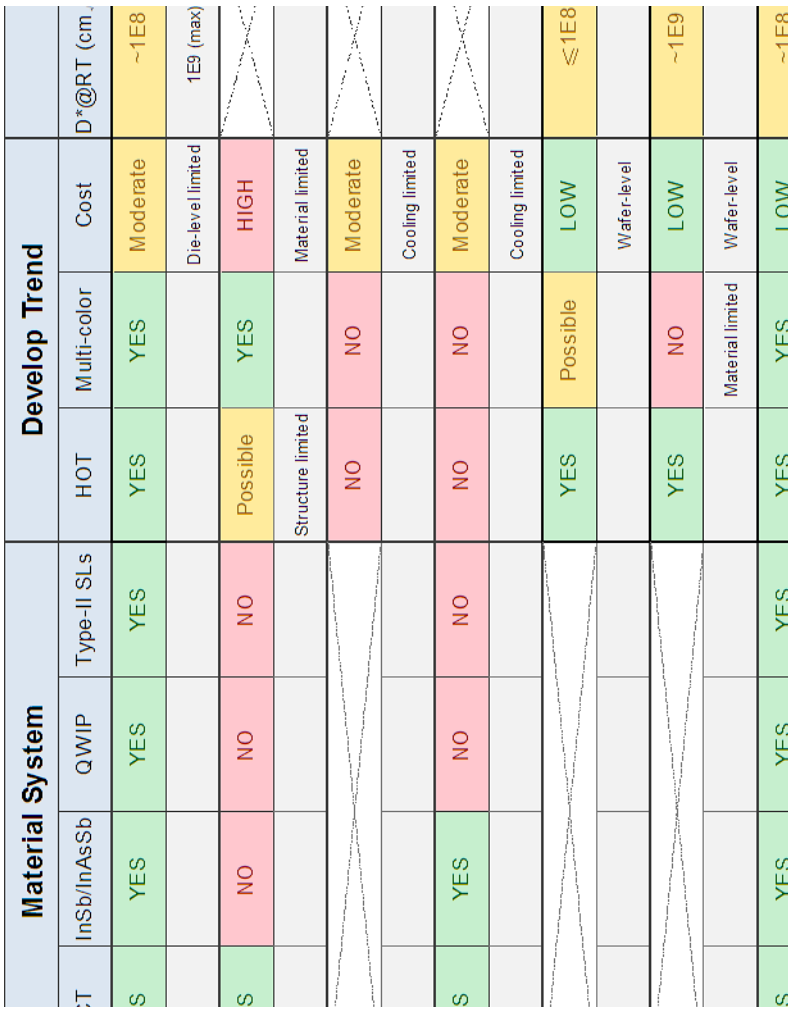


Fig. 2.24. (a) Schematic diagram of the InAsSb nbn detector with pyramid shaped absorber layer to enhance the detection performance. (b) SEM images of the fabricated pyramidal photon trapping absorber [128].

2.5Summary

Mid-IR detection and imaging is of great importance for a number of sensing applications such as gas detection, security, defense and medical diagnostics.State of the art mid-IR photon detector based FPAs require hybridisation of an array of isolated photodetectors, made by narrow bandgap semiconductors, with the CMOS addressing chip. Although this hybrid design has successfully produced very large format and high performance imagers, the commonly used flip-chip bonding technique, as a die level process, will dramatically increase the cost of the manufactured FPAs. On the other hand, monolithic integration of mid-IR photodetectors with readout circuits offersmuch lower cost since the entire device fabrication is achieved at a wafer level. However, as summary in Table.1 shows, there is currently a lack of a monolithic design flexible enoughto satisfyall the future requirementsfrom high performance photon detector basedmid-IR FPAs (HOT, multi-color, and low cost). This constitutesan attractive research topic that this thesis will be focused on.



3. GaAs-based Monolithic Integration

This chapter outlines the operation of a GaAs-based monolithically integrated pixel array device which is suitable for realizing a new type of mid-IR FPA. The first section introduces newly developed epitaxy techniques which support growth of high performance mid-IR photodetectors on GaAs wafers. A brief review of existing GaAs-based technologiesthat use Metal-Semiconductor Field Effect Transistor (MESFET) to form ROIC for FPAs follows.The chapter continues with presenting the background theory and the figures of merit of MESFETs and photodiodes. Understanding the mechanisms ruling the device operation will aid comprehension of an X-Y pixel addressing strategy based on pixels integrated with MESFET switches. Finally, a discussion on device design and a summary of key performance requirements to be used as guidancefor the fabrication of prototype devices concludes the chapter.

3.1 Potential MonolithicApproach

3.1.1 Non-Native Substrate Growth

Previously, antimonide-based mid-IR photodetectors based on either InSb families or type-II superlattice structures (SLS) were grown by lattice matched epitaxy on native substrates such as InSb and GaSb [95, 119], and could thus achieve the best material quality. Although these photodetectors demonstrated satisfactory performance, a fewdisadvantages significantly limit their use. First, native substrates are much more expensive, even though their commercializedwafer size is currently limited to four inches. This is mainly due to the quality of larger substrates currently does not meet the required specifications in terms of flatness and defects to make mass production commercially viable [130]. Secondly, native substrates have a large absorption coefficient in the targeted IRranges, making substrate removal almost compulsory in hybrid designs that need back-side illumination [131]. Because of the aforementioned reasons, most currently available mid-IR FPAs present high manufacture complexity which directly translates to high costs.

In order to avoid the problems associated with native substrates, research attention has recently turned to lattice-mismatched epitaxy of antimonide-based materials on mature substrates, such as GaAs and Si wafers. The main challenge of this approach is due to the lattice mismatch and to the corresponding strain generated between the

epitaxial layers. Mismatch-induced strain limits growth of the infrared-sensing layer to a critical thickness,which is not enough to absorb infrared light (a few monolayers [132]). Although further growth beyond this thickness is achievable, the accumulated strain energy will keep increasing and eventually be relieved by creationof defects inside the grown material, such as misfit dislocations (MDs) and threading dislocations (TDs) [133]. The latter ones are particularly important as they can vertically propagate into the active device layers anddegradedetection performance [134] (See Fig. 3.1).

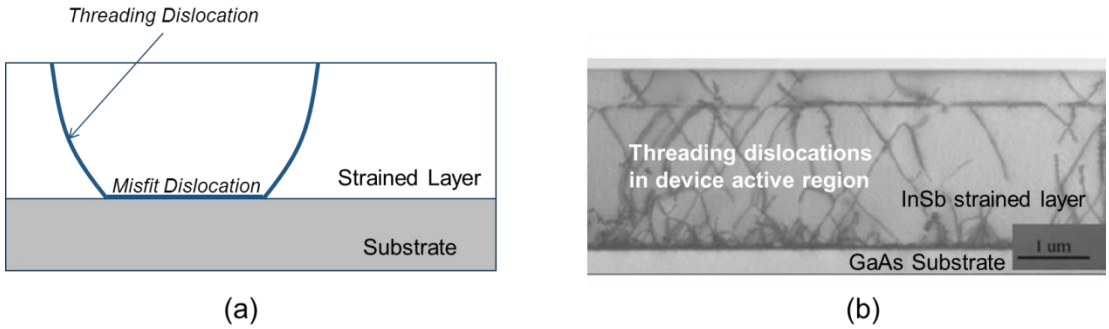


Fig.3.1. (a) Schematic ofdislocations in lattice mismatched epilayers. (b) Typical cross-sectional TEM image showing detrimental TDspropagated into the InSb epilayersifthey are grown on a GaAs substrate directly [134].

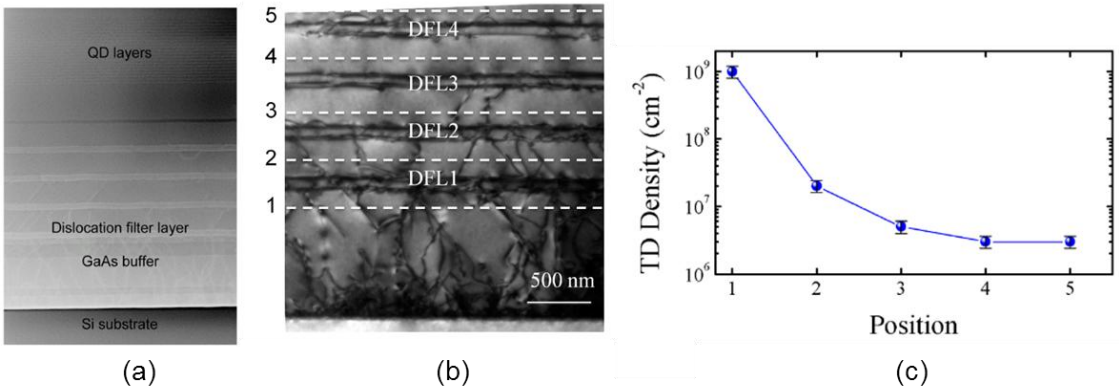


Fig.3.2. (a) TEM InAs/GaAs QD mid-IR photodetector grown on Si substrate with the aid of metamorphic buffer layers. (b) Zoomed in image showing the reduction of TD by InGaAs/GaAs SLS dislocation filter layers (DFL). (c) Estimated TD density from TEM measurements at different positions as indicated in (b) [136].

Growthof metamorphic buffer layers between the substrate and the active region of the device is a practical way to compensate for the lattice mismatch and thus suppress the TD density. This is typically achieved by compositionally grading the epi-layer towards the desired lattice constant [135]. Alternatively, SLS layer structures can be periodically inserted between the substrate and the device active layers to iteratively relieve the strain due to lattice mismatch. In this case, as shown in Fig. 3.2, the vertically propagating TDs are “filtered” after passing through each superlattice structure. As a result, only a small portion of TDs will reach the upper layers, leading to a TD density reduction in the device active region by three orders of magnitude [136].

Although this approach has led to a number of successful device demonstrations including growth of a quantum dot (QD) based mid-IR photodetector on Si substrate [137], the resulting material quality is still considerably lower than thatdelivered by native substrates, unless very thick buffer layers or dislocation filter layers (often>5 μm) are used. Moreover, metamorphic buffer layers are not suitable for electrical conduction due to the large number of non-radiative recombination centrescreated by TDs.

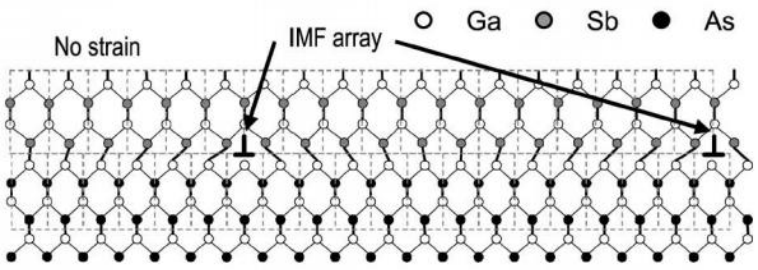


Fig.3.3. Schematic illustration of the interface between GaAs and GaSb using IMF growth mode [138].

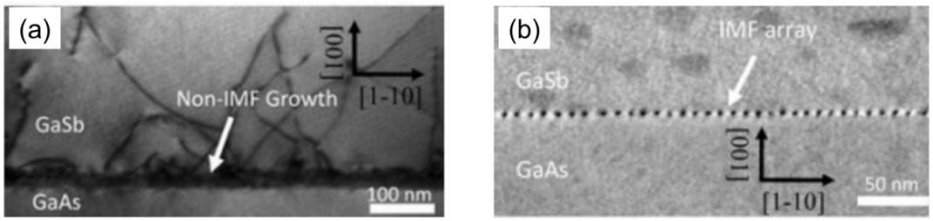


Fig.3.4. (a) TEM image of non-IMF growth of GaSb on GaAs substrate with high TD density. (b) TEM image showing a fully strained relaxed GaSb layer with periodic IMF array at the heterointerface [139].

Another growth mathod relies on a fundamentallydifferentapproach, based oninterfacial misfit (IMF)dislocations.The most representative example of IMF growth is the highly strained GaSb/GaAs system which has approximately 7.8% lattice mismatch. Since the ratio of the lattice constants of GaSb and GaAs is almost exactly 13:14, the growth conditions can be made such that at the GaAs/GaSb interface an Sb-Ga bond is missed every 13 atomic sites (~5.6 nm). As a result a two-dimensional, periodic array of dislocations (i.e. missing Sb-Ga bonds)is formed on the entire surface of the GaAs wafer. Suchdislocationsare also calledege type misfit dislocations and they can be seen in Fig. 3.3,representedby a sign⊥. By bending and stretching the surrounding atomic bonds, the array of dislocationscan relieve the excess strain energyimmediatelyat the heterointerface [138].Hence this approach does not introduceany TDs vertically-propagatingtowardsthe activeregion of the devices.

IMF growth achieved a fully strain-relaxed GaSb layer on GaAs substrate with TD density as low as 10^5 cm^{-2}, as shown by the images in Fig. 3.4 [139, 140]. The nearly defect-free GaSb layer obtained by IMF growth can be used as a template to grow a

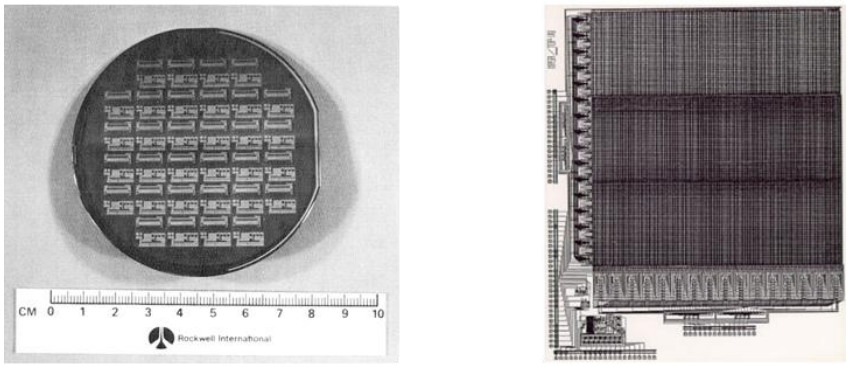
number of lattice-matched materials, such as InAsSb, AlGaSb and InAs/GaSb SLS, with high quality. So far numerousmid-IR devices grown by IMF techniques were demonstrated, including light emitting diodes (LEDs) [141], lasers [142] and photodetectors [143-146]. The latter ones in particularwere reported to have comparabledetection performance to devices grown onmore expensive GaSb substrates. More importantly, since the IMF dislocations are confined at the interface and do not propagate into the active regions, the grown GaSb layer is very suitable for electrical conduction through the corresponding GaAs/GaSb heterojunction [147, 148]. Despite the good results achieved with IMF growth of antimonide-based layers on GaAs, the same on Si delivered wafers of considerably lower quality [138], due to the challenges posed by the larger lattice mismatch (13%) between Si and GaSb.

3.1.2 GaAs-based Readout Circuits

With the great number of advantages offered by VLSI and mass production, the well-established Si CMOS technology isthe preferred platform for implementation of ROICs to be used with IR FPAs. Nevertheless, certain applications require very low noise andmake use of device cooling under deep cryogenic temperatures, which cause the performance of Si ROICsto degrade dramatically because of carrier freeze-out phenomena [149].Even for general imaging purpose beyond 77K, this approach is not without its problem. As discussed in Sec. 2.3.2.1, due to the thermal expansion mismatch between the photodetector substrate and the flip-chip bonded Si ROIC chip, imagers based on hybrid technology are extremely sensitive to storing and operating condition especially when thermal cycles are involved.

For many years, ROICs based on GaAs have been considered as a promising alternative technology. Since GaAshas a relatively small effective conduction band density of states ($\sim 5 \times 10^{17} cm^{-3}$), itcan attain degeneracyat a fairly low doping concentration in which condition the n-type dopants require almost no energy for ionization. As a result, GaAs-based devices are almost immune to carrier freeze-out even when cooled to temperatures below 0.1K, making them ideal for cryogenic applications [150].Moreover, the thermalexpansion coefficient of GaAs is better matched to mid-IR sensitive materials comparedto Si,making hybrid FPAs based on GaAs ROICs theoretically more reliable [151]. Furthermore, GaAs has higher carrier mobility than Si, thus offering the possibility of large format FPAs readout with increased speed. Despite the lack of a truecomplementary solution impeding VLSI of

GaAs circuits, intense research into various kinds of enhancement/depletion mode GaAs transistors has led to a number of successful demonstrations of readout circuits for IR FPAs. As shown in Fig. 3.5, this includes a high speed 2x64 ROIC for hybrid FPAs [152] and a fully addressable 256x256 monolithic array for thermal detector based IR imaging [153], both relying on GaAs MESFET. Other device structures such as GaAs JunctionFiled Effect Transistors (JFET) and GaAs CCD technology [154]can also be used.



(a) (b)

Fig.3.5. (a) Wafer photograph of GaAs 2 x 64 readouts fabricated by Rockwell [152]. (b) Chip layout of a 256 x 256 infrared sensor readout and preprocessing electronics, implemented in Triquint GaAs MESFET QED/A process [153].

3.1.3 Monolithic Integration Design

All of the aforementioned existing techniques have naturally highlighted the great potential of GaAs to realize a novel monolithic platform for mid-IRFPAs. As shown in Fig. 3.6, by heterogeneous growth of high quality antimonide-based materials onto a GaAs substrate integrating active layers for FET fabrication, state-of-the-art mid-IR photodetectors can be monolithically integrated with GaAs-based ROICs. The mid-IR detectors that can be heterogeneously grown on GaAs substrates include newly developed high operating temperature photodetectors, such as InSb non-equilibrium photodiodes and nBn detectors made by either InAsSb or InAs/GaSb SLS (Section 2.4.2). Similar designs, whereInAs photodiodes and InGaAs laser diodes are monolithically integrated with GaAs MESFETs have already been presented [155,156]. However, these devices are only suitable for use in the NIR and SWIR range (<2 μm). Antimonide-basedphotodetectors, which are sensitive in the mid-IR range, havenever been successfully integrated with GaAs MESFETsbefore. Several challenges regardingeither the design or fabricationaspectsmust be overcome to make such adevice system possible.

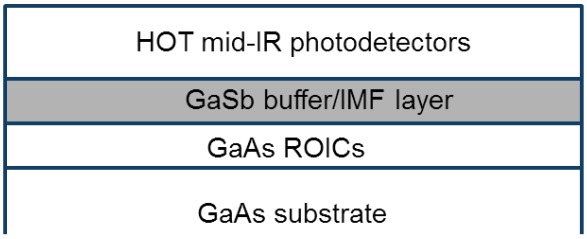


Fig.3.6. Illustration of monolithic integration of high performance mid-IR photodetectors with GaAs ROICs using either metamorphic buffer layer or IMF technique.

3.2 GaAs MESFET Fundamentals

3.2.1 Metal-Semiconductor Contacts

The basic interface for accessing or controlling an electronic device is created when a semiconductor is brought in contact with a metal. Fig. 3.7 (a) shows the energy diagram of a metal and an n-type semiconductor individually. Differently from semiconductors, the Fermi level E_F in a metal is located at the bottom of itsconductionvalley since all electrons are free to move in the crystal. Due to the difference in Fermi level,when a semiconductor and a metal are brought in contact electrons will start diffusingfrom the former to the latter and hence generatea built-in electrical filed. As shown in Fig. 3.7 (b), electron transfer will occur untilthe Fermi level is aligned between the two materials, thus forming anenergy barrier at the interface, with the energy bands bendingon thesemiconductor side. The height of the resulting barrier, known as a Schottky barrier, isdefined as the energy required for transferringan electron from the Fermilevel in the metal to the conduction band of the semiconductor.

In an ideal Schottky model, the height of the energy barrier is given by the difference between the electron affinities of thetwo materials [157]:

$$q\varphi_{Bn} = q(\varphi_m - \chi) \qquad \textbf{Eqn. 3.1}$$

Where$q$is the electron charge,$\varphi_m$is the work function of the metal, definedas the energy required tomove a free electron from the Fermilevel to the vacuum level, and χ is affinity of the semiconductor defined as the required energy tomove a free electron from the conduction band to the vacuum level. The built-in potential that obstructs the transfer ofthe electrons from the semiconductor to the metal is then given by

$$V_{bi} = \varphi_{Bn} - V_n \qquad \textbf{Eqn. 3.2}$$

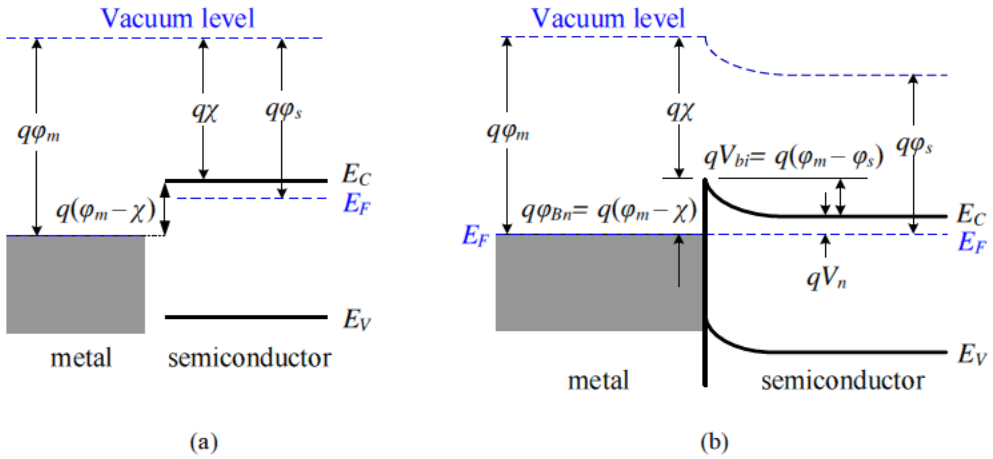


Fig.3.7. (a) The energy diagram of the isolated metal and the n-type semiconductor and (b) theenergy diagram of a metal-semiconductor contact.

In a non-ideal scenario, there will bemid-gap states existing at the semiconductor surface where the periodicity of the crystal lattice is interrupted, andthe position of Fermi levelrelatively to the conduction and valence bands is thus significantly affected.As shown in Fig.3.8, electrons from theconduction band will tend to fill those states which are below the Fermi level, creating a depletion region at the surface region with a positive space charge Q_{sc}. The Fermi level in the semiconductoris then termed "pinned"at aparticular band bending energy level qV_{bb}below the conduction band edge. If the density of surface states is large enough, as at the surface of most III-V compound semiconductors including GaAs, the Fermi level willremain pinned even after being brought in contact with metal. In this case, the resulted barrier height φ_{Bn} and also build-in potential V_{bi} arealmost independent of metal work function but determined by the doping and surface properties of the semiconductor [158].

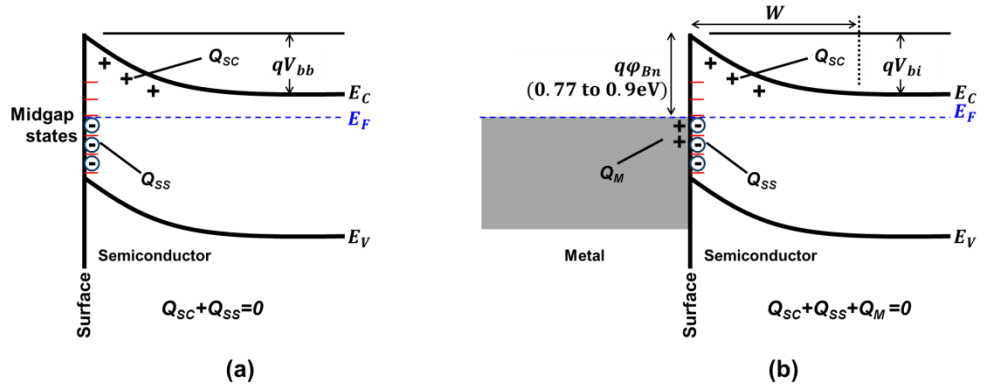


Fig. 3.8. (a) Energy diagram showing the band bending of semiconductor at the surface region and (b) the energy diagram of a typical metal-GaAs contact.

The width of the barrier, also known as the depletion width *W*, is expressed by [157]:

$$W = \sqrt{\frac{2\varepsilon_s(V_{bi} - V)}{qN_D}} \qquad \textbf{Eqn. 3.3}$$

whereε_s is the permittivity of the semiconductor,N_D is the donor concentration, and *V*is the voltage applied to the contact. This equation indicates that applying bias voltage to the metal will significantly change the value of depletion width.

In order to describe the current flowing across the metal-semiconductor interface,three main mechanisms are commonly used: thermionicemission (TE), field emission (FE) and thermionic field emission (TFE) [159].

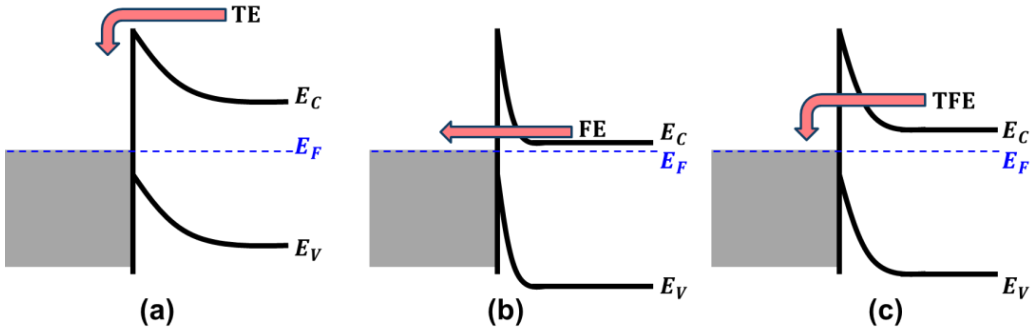


Fig. 3.9. The three main mechanisms for current transport across a metal-semiconductor junction.The arrows indicate theelectron transfer mechanism.

At room temperature, TE is the dominant mechanism for the semiconductor materials with small doping concentration. As shown in Fig. 3.9 (a), the current transport in this caserelies on electrons thermally exited to higher energy level and that are thus able to overcome the height of the energy barrier. This means that more and more electrons can gain enough energy to overcome the barrier height as the temperature increases (or the barrier height reduces). More specifically, as expressed in Eqn. 3.4, the current induced byTEmechanism is exponentially relatedto the temperature T and the energy barrier heightφ_{Bn}.

$$I_{TE} \propto \exp\left(-\frac{q\varphi_{Bn}}{K_b T}\right) \qquad \textbf{Eqn. 3.4}$$

whereK_b is the Boltzmann constant.

FE instead is due to the quantum tunnelling effect and it is more likely when the barrier is narrow, as shown in Fig.3.9 (b). The quantum tunnelling phenomenon derives from electrons having a finite probability to overcome the barrier, even if their energy

level is well below the energy required for TE mechanism. According to Eqn. 3.3, the barrier width is inversely proportional to doping concentration. Therefore, FEwill become the dominant mechanism when the metal material is in contact with a heavily doped semiconductor material.An estimated relation for the FE induced current is given by:

$$I_{FE} \propto \exp\left(-\frac{q\varphi_{Bn}}{E_{00}}\right) \qquad \textbf{Eqn. 3.5}$$

where E_{00} is the characteristic tunnelling energy affected by the doping concentration andthe carrier effective mass $m_e{}^*$. The value of E_{00} is related to the transmission probability of the carrier through the barrier and is given in the following equation:

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{\varepsilon_s m_e{}^*}} \qquad \textbf{Eqn. 3.6}$$

In reality, both TE and FE generally occur simultaneously for metal-semiconductor contacts at room temperature. This type of conduction is thus termed as thermionic field emission and it relies on both thermal excitation and tunnelling effect. TFE can lead to current transport even if the electrons haveinsufficient energy to overcome the barrier height or have little chance to tunnel thorough the barrier directly from the conduction band. As shown in Fig.3.9 (c), since the barrier is thinning towards higher energy states, the thermallyexcited electrons will be able to tunnel from an intermediate energy level higher than Fermi level. As acombination of TE and FE mechanism, temperature,doping concentration and barrier shape all affect the total TFE-induced current.

The relative contributions of TE, FE, TFE can be roughly judged by comparing the thermal energy$K_b T$to E_{00}. TE mechanismdominates when $K_b T \gg E_{00}$. In contrast, FE mechanismdominates when $K_b T \ll E_{00}$. When $K_b T \approx E_{00}$, both TE and FE will contribute to the current flow and hence TFE mechanism dominates.

3.2.1.1 Schottky Contact

A good Schottky contact is formed when the TE mechanism dominates the current transport in between the semiconductor and the metal. As shown in Fig. 3.10 (a), under zero bias condition, the TE induced current flow from metal to semiconductor $J_{M\to S}$ is same as that from metal to semiconductor $J_{S\to M}$ and is given by:

$$J_{M\to S} = J_{S\to M} = J_0 = A^* T^2 \exp\left(-\frac{q\varphi_{Bn}}{K_b T}\right) \qquad \textbf{Eqn.3.7}$$

whereA^* is the Richardson constant.

If a positive bias voltage (V>0) is applied to the metal, the potential barrier at the semiconductor side will be reduced. As a result, more electrons can obtain enough thermal energy to across the barrier and flow into the metal, leading to an exponential increase in$J_{S\to M}$. In the meanwhile, $J_{M\to S}$ remains unchanged. The net current density is thus given by:

$$J = J_{S\to M} - J_{M\to S} = J_0\left[\exp\left(\frac{qV}{nK_b T}\right) - 1\right] \qquad \textbf{Eqn.3.8}$$

where*n* is the diode idealityfactor. In contrast, when a negative bias voltage (V<0) is applied to the metal, the potential barrier at the semiconductor will increase accordingly. The net current density can be expressed by Eqn. 3.8 as well, but the current will flow in the opposite direction as compared to the forward bias condition. With an increased negative bias, the value of current density tends to become constant and reach a value ofJ_0, hence J_0 is also referred to as the reverse bias saturation current density. Finally, a breakdown occurs when the reverse bias is increased beyond the point where the electron transport is no longer dominated by TE but by FE. A typical current-voltage characteristic ofaSchottky contact is shown in Fig. 3.11 (a). It presents a clear current rectifying behaviour, similar to that of a standard p-n junction diode.

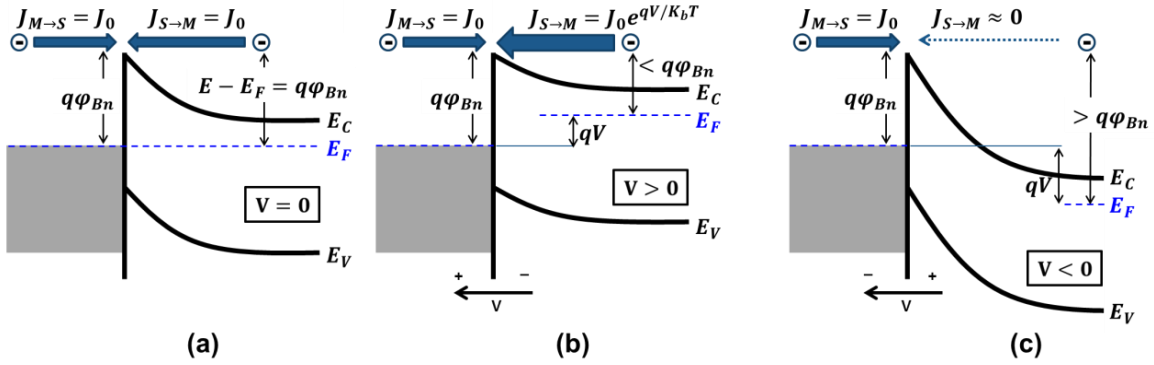


Fig. 3.10. Current transport in a Schottky contact under various bias conditions: (a) zero bias, (b) forward biased, (c) reverse biased.

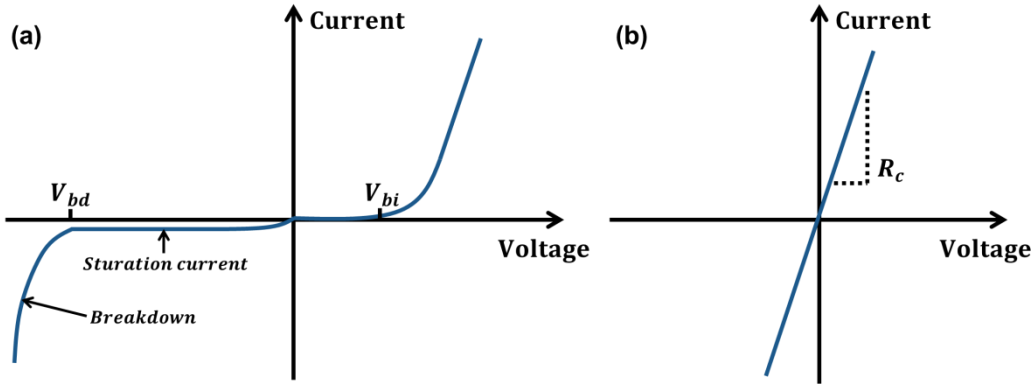


Fig. 3.11. Current-voltage characteristics of (a) Schottky contacts and (b) Ohmic contacts.

3.2.1.2 Ohmic Contact

If FE mechanism dominates the current transport at the metal-semiconductor interface,an Ohmic contacts is formed.This is generally done by heavily dopingthe semiconductor at the interface to make the barrier width as narrow as possible, so that electrons can easily tunnel through. Accordingly, the current-voltage characteristic of the contact will become linear regardless of the bias condition (see Fig. 3.11 (b)). The contact resistance of an Ohmic contact formed on a heavily doped semiconductor is given by [157]

$$R_c = \exp\left(\frac{4\varphi_{Bn}\sqrt{\varepsilon_s m_e{}^*}}{N_D \hbar}\right) \qquad \textbf{Eqn. 3.9}$$

This value can be obtained experimentally from the slope of the linear current-voltage curve. A high quality Ohmic contact is expected to showvery small contact resistance as compared to the series resistance of the semiconductorin order to avoid degradation to the deviceperformance.

3.2.2 MESFET Structure and Operation

Fig. 3.12 illustrates the basic structure of a GaAs MESFET. The device active region is typically n-type doped,and grown on a semi-insulating (S-I) GaAs substrate. The device consists of three metal-semiconductor contacts: one Schottky contact, known as “Gate” electrode, formed on a moderately doped channel layer, and two Ohmic contacts, formed on a heavily doped cap layer, known as “Source” and “Drain” electrodes respectively. The dimension of a GaAs MESFET is mainly described in terms of three important parameters: the gate length *L*, the gate width *Z*, and the channel thickness a. Their effect on device operation and performance will be detailed in this section.

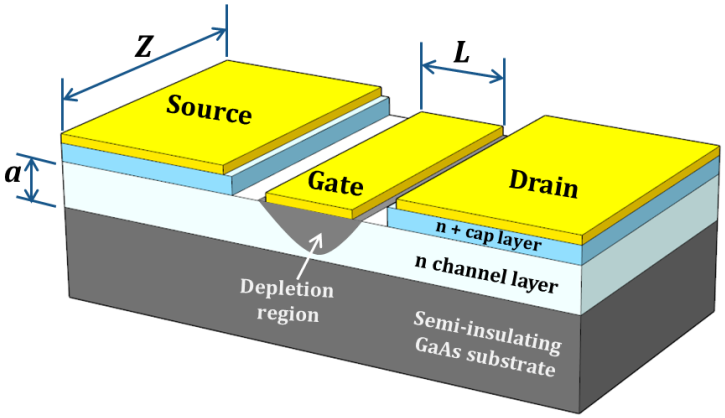


Fig. 3.12. A 3D view of a GaAs MESFET.

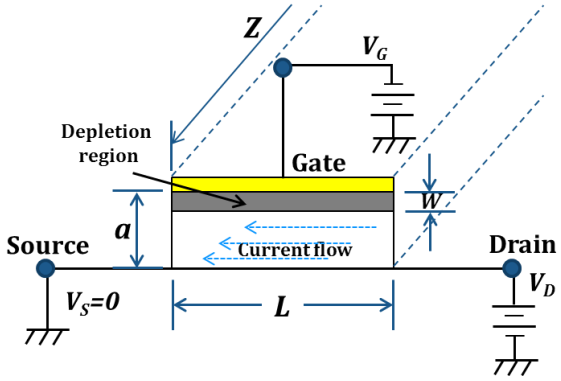


Fig. 3.13. Cross section of the gate region of a GaAs MESFET.

Assuming the parasitic resistances from Source to Gate and Drain to Gate (including Ohmic contact resistances and material series resistances) to be negligible, a simplified cross section view of the device can be drawn as shown in Fig. 3.13 to understand the basic operation of a GaAs MESFET. To drive the device, the Source electrode is grounded (V_S=0 V), and the voltages applied to the Gate and Drain nodes are measured with respect to the source as $V_G$and V_D. As discussed in Sec. 3.2.1, after deposition of the Gate electrode metal onto the GaAs channel, a Schottky barrier is formed at the interface. Accordingly, a depletion region with width value W is created underneath the Gate electrode. Furthermore, with no bias applied, the channel of a MESFET can be regarded as a thin layer of bulk GaAs material whose resistance is given by [157]

$$R_{ch} = \frac{L}{q\mu_n N_D Z(a-W)} \qquad \textbf{Eqn. 3.10}$$

where$\mu_n$is the mobility of n-doped GaAs material.

When V_G=0V, the MESFET is in the ON-state, and if a positiveV_D is applied, current will start flowing in the channel region from Drain to Source. As shown in Fig. 3.14 (a), if V_D is small enough the channel can be treated as a resistor whose resistance

is given by Eqn. 3.10. In this regime,the channel currentvaries linearly with V_D and the MESFET is said to be working in the linear region.The value of the channel current $I_D$willbe given by Ohm's law:

$$I_D = \frac{V_D}{R_{ch}} = \frac{q\mu_n N_D Z(a-W)V_D}{L} \qquad \textbf{Eqn. 3.11}$$

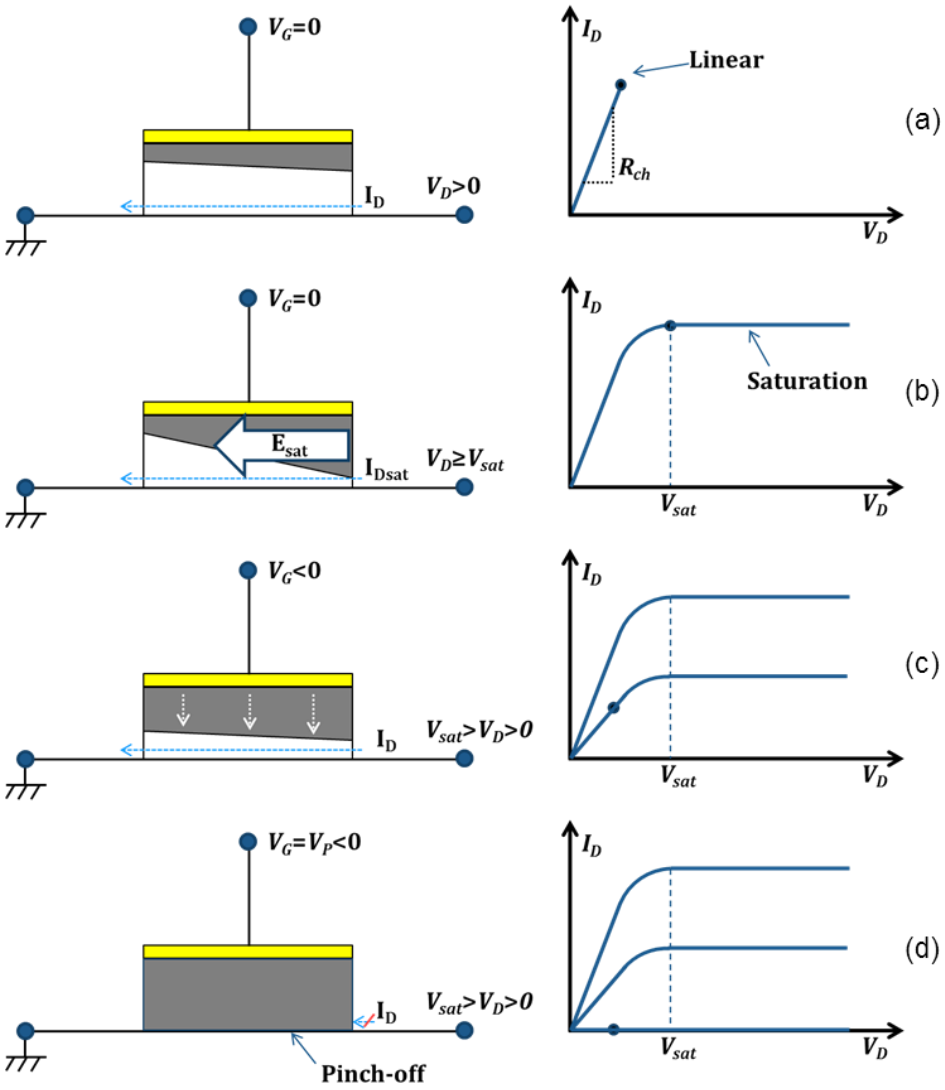


Fig. 3.14. Variation of the depletion region and output characteristics of a MESFET under various biasing conditions. (a) V_G=0, V_D<<V_{sat}(very small), (b)V_G=0, saturation velocity of GaAs is reached with increasing V_D (c) V_G<0, channel is partially pinched off (d) V_G<V_P, channel is fully pinched off.

As $V_D$is increasedfurther, the channel current starts to increase at a slower rate.Eventually, a point where the channel current remains constant despite increasing the value of $V_D$is reached, as shown in Fig 3.14 (b).This behaviour is referred to as channel current saturation, and the corresponding value of V_D is called the saturation voltage. The saturation is due to the drift velocity of the GaAs channel reaching its maximum value v_{sat} when the applied electric field exceedsE_{sat}. For common GaAs

channel doping concentrations, typical values of ν_{sat} are 10^7 cm/s while E_{sat} is generally between 3.5 to 4 kV/cm[160]. Therefore, for a given gate length the saturation voltage can in first approximation be calculated by:

$$V_{sat} \approx E_{sat} L \qquad \textbf{Eqn. 3.12}$$

When the MESFET is working in saturation region, the saturated channel current is given by:

$$I_{Dsat} = qN_D \nu_{sat} Z[a - W] \qquad \textbf{Eqn. 3.13}$$

If instead of keeping it grounded, increasing negative voltages are applied to the schottky gate electrode (i.e. V_G<0), the underlying depletion region will keep expanding due to the increase in the Schottky barrier width (Eqn. 3.3). This will result in thinning of the conductive channel and a further reduction of the channel current under any given V_D (see Fig. 3.14 (c)). Eventually, for a sufficiently largeV_G,the region underneath the Gate electrode willbe fully depleted.When this situation is reached, the channel is said to be "pinched off" and the source and drain nodes are completely separated by the depletion region. The transistor is thus in the OFF-state,andideally no current can flow through the channel. The voltageV_G required to pinch off the channel can be derived from Eqn. 3.3 by using the fact that the width of the depletion region W will have to be equal to the thickness of the channel (i.e.$a = W$).

$$V_P = V_{bi} - \frac{qN_D a^2}{2\varepsilon_s} \qquad \textbf{Eqn. 3.14}$$

As shown in Fig. 3.15, the electrical characteristics of a real GaAs MESFET arevery similar to the ideal ones, but with several importantexceptions. First,depending on the fabrication process, there will be some spacebetween Drain-Gate and Source-Gate electrodes that will introduce series parasitic resistances accordingly. Amore accurate estimate of the resistance across Drain and Source is thus given by:

$$R_{DS} = R_{ch} + R_{SG} + R_{GD} \approx R_{ch} + \frac{L_{SG} + L_{GD}}{q\mu_n N_D Z a} + 2R_c \qquad \textbf{Eqn. 3.15}$$

where$R_c$is the Ohmic contact resistance, and $L_{SG}$and L_{GD} are the source-gate distance and drain-gate distance, respectively. Secondly, the I_D-V_D curves of a real MESFET show a slightly positive slope even after entering the saturation region,even though the carrier velocity should be saturated. This results mainly from chargeinjection into the layers beneath the channel (either the substrate or the buffer layer), creating new paths for current to flow [161]. Besides, sinceV_G<V_D, there will also be a gate leakage current

I_{GL} induced by the reverse biased Schottky barrier which will also contribute to an increased $I_D$in the saturation region. As a result, the real GaAs MESFET will always present a residue current equal to $I_{subs}+I_{GL}$ even if the MESFET is turned OFF. In a worst case scenario, if the voltage applied across Drain and Gate electrode is large enough, the MESFET will be permanently damaged due to the breakdown of the Gate Schottky contact.

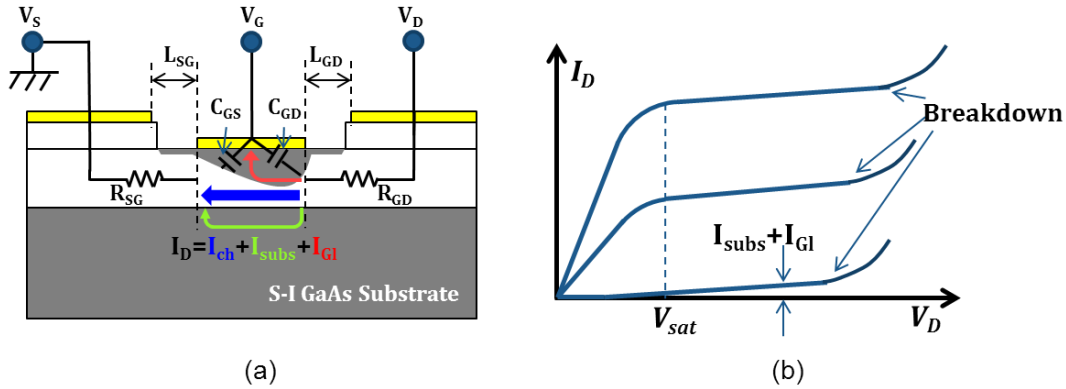


Fig. 3.15. (a) Cross section view of an actual MESFET with series parasitic resistance and leakage current components marked (b) output characteristics of an actual MESFET.

Since a GaAs MESFET operates by modulating the flow of carriers through the channel layer with the application of various bias voltages to the Gate electrode, the modulation efficiencynaturally becomes a vital figure of merit for evaluating. The modulation efficiency canbe effectively described by the intrinsic transconductance (g_m) which quantifies how much the channel current is affected by changes in V_G for a fixed V_D.

$$g_m = \frac{\partial I_D}{\partial V_G}\Big| V_D \qquad \textbf{Eqn. 3.16}$$

when substituting the expressions for I_D in Eqn 3.11 and Eqn 3.13, the following expressions are obtained:

$$g_m = \begin{cases} \dfrac{\varepsilon_s \mu_n V_D Z}{WL} & (linear\ region) \\ \dfrac{\varepsilon_s v_{sat} Z}{W} & (saturation\ region) \end{cases} \qquad \textbf{Eqn. 3.17}$$

It is obvious thatthe value of $g_m$will decrease when V_G is made increasingly negative since the depletion width$W$ increases accordingly. Additionally, $g_m$is also animportantparameter to describe the maximum speed at which a GaAs MESFET can

operate, since it is related to the cut-off frequency f_T where the current gain of device fallsto unity:

$$f_T = \frac{g_m}{2\pi C_G} \approx \frac{v_{sat}}{2\pi L} \quad \textbf{Eqn. 3.18}$$

whereC_G is the Gate capacitance created by the underlying depletion region and equals to $C_{GS} + C_{DG}$.

3.3 Photodiode Fundamentals

3.3.1 Basic Operation

As previously mentioned in Sec. 2.2, photon detection of infrared radiation relies on excitation of free electron-and-hole pairs by absorbing the energy of the incidentlight. In order to sweep out these photo-generated carriers and hence forming a photocurrent signal, there are two classic photodetector structures that commonly applied. They are the photoconductor (PC) detector and the photovoltaic (PV) detector.

A PC detector is the simplest possible structure which only consists of a homogeneous semiconductor absorbing material with two electrodes. The absorption of the photons increases the conductivity of this semiconductor material and the resulted change in the resistance is then measured by applying biasing voltage or current. On the other hand, a PV detector is slightly more complex in which a built-in electric field is formed to cause the photo-generated electrons and holes to move in opposite directions and then collected by cathode and anode respectively. As a result no bias or near zero bias operation can be achieved. The most common example of PV detector is the p-n junction structure made by doping the opposite sides of the detector with n-type and p-type dopant correspondingly. Further, an intrinsic layer can be added in between the p-type and n-type layer to expand the depletion region for efficient light absorption, forming a p-i-n structure.

Generally, PV detectors have advantages such as lower noise and faster response as compared to PC detectors [162]. Therefore, most of the state-of-the-art high performance mid-IR detectors are made usingthe photodiode structure. Note that the newly developed nBn detectors behave more like a PC detector since a small bias voltage is generally required. But its basic operation mechanism is actually very similar to a p-i-n photodiode [163] and hence is discussed together in this thesis.

3.3.2 Current-Voltage characteristics

According to the above-mentioned basic operation mechanism, the total current density in a photodiode can be given as [116]

$$J(V,\phi) = J_d(V) + J_{ph}(\phi) \qquad \textbf{Eqn. 3.19}$$

whereJ_d is the dark current density that depends only on bias voltage V, and J_{ph} is the photocurrent which is decided by the incident photon flux densityϕ.

3.3.2.1 Photocurrent

In a standard photodiode with unity gain, the magnitude of photocurrent can be further written as

$$I_{ph} = \eta q A \phi \qquad \textbf{Eqn. 3.20}$$

where$A$ is active sensing area of the photodiode and η is the quantum efficiency which stands for the number of electron-hole pairs generated per a single photon of incident radiation. Further, the ratio of the photocurrent I_{ph} to the received incident light power$P$ at a given wavelengthλ defines the current responsivity of the photodiode:

$$R_i(\lambda) = \frac{I_{ph}}{P} = \frac{q\lambda}{hc}\eta \qquad \textbf{Eqn. 3.21}$$

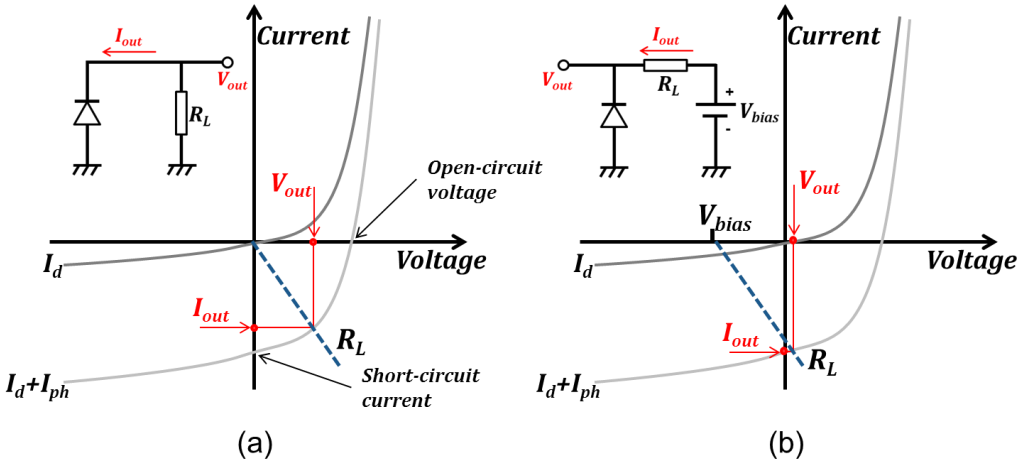


Fig. 3.16. Current-voltage characteristics of a typical photodiode, showing the effect of connecting a load resistance when the photodiode is (a) zero biased (b) slightly reverse biased.

If the photodiode is open-circuited, the photo-generated electrons and holes will be accumulated on the two opposite sides of the junction, producing an open-circuit voltage. On the other hand, a maximum current is obtained when the two electrodes of the photodiode are short-circuited. This is thus named as short-circuited current. When a signal readout circuit is formed by connecting a load resistor R_L in series with the

photodiode, the actual output current and voltage can be extracted from the point where the current-voltage characteristics of the photodiode and the load line slope of R_L cross (see Fig. 3.16(a)). This method is also applicable in case a small reverse bias voltage $V_{bias}$is applied as Fig. 3.16(b) shows.

3.3.2.2 Dark Current

Under the condition where there is no illumination, as shown in Fig. 3.17, the currentflow in the photodiode under zero or reverse bias consists ofa set of components [164, 165]:

$$I_D = I_{dif} + I_{GR} + I_T + I_{SH} + I_{SL} \qquad \textbf{Eqn. 3.22}$$

whereI_D is the dark current, I_{dif} is the diffusion current in an ideal diode, $I_{GR}$and $I_T$are parasitic bulk currents arising from, respectively,carrier generation-recombination and tunnelling, and finally I_{SL} and I_{SH} are leakage currents that induced respectively by surface states anddislocation defects intersecting the junction.Each of the above components has distinct relationship to the bias voltageand the operating temperature.Detailed generation mechanisms and calculation methods of these current components can be found in [116].

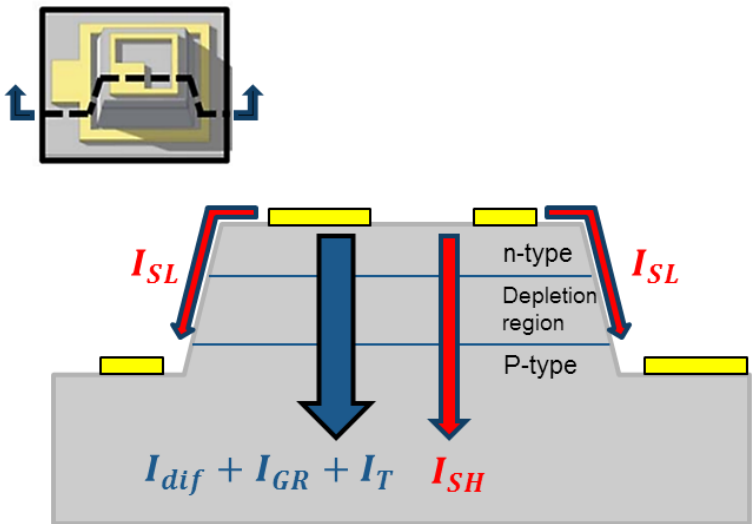


Fig.3.17. Cross section of an InSb PD (inset) highlighting the source of dark current components.

With the dark current being calculated or measured practically, the dynamic resistance of the photodiode can be obtained by taking the reciprocal of the derivative of the equation for the total dark current as a function of voltage. When measured at zero bias, the dynamic resistance is further called R_0 (“R-zero”) and is expressed by:

$$R_0 = \left(\frac{\partial I_d}{\partial V}\right)^{-1}\Bigg|_{V_b = 0} \qquad \textbf{Eqn. 3.23}$$

One of the most frequently used figure of merit for a photodiode is the zero bias "resistance.area" product (R_0A):

$$R_0\mathrm{A} = \left(\frac{\partial J_d}{\partial V}\right)^{-1}\Bigg|\, V_b = 0 \qquad \textbf{Eqn. 3.24}$$

wherethe dark current density $J_d = I_d/A$.

3.3.3 Detection Performance Evaluation

The responsivity, as described in Eqn. 3.21, showshow much photocurrent a photodiode can generate when illuminated by a given power of incident light. However it is not able to evaluate the detection performance of the measured device on its own since higher signal can always be generated by applying an incident light with higher power level. Regarding the practicalapplication of detectors, people are more interested to know the minimum power level that a photodiode can detect without being troubled by the internal noise of the device. As a result, noise equivalent power (NEP) is commonly referred which defined as the incident radiation power that generates an output signal equal to the photodiode internal noise, and it is given by [116, 162]:

$$NEP = \frac{I_n}{R_i} \qquad \textbf{Eqn. 3.25}$$

where I_n is noise current. Generally, thermal noise (Johnson-Nyquist noise) dominates the internal noise of a mid-IR photodiode operating under high operating temperature$T$, and hence the I_n can be further written by:

$${I_n}^2 = \frac{4K_bT\Delta f}{R_0} \qquad \textbf{Eqn. 3.26}$$

where $\Delta f$is the bandwidth under interest. However, NEP is still inconvenient to be applied directly for comparing the performance of photodiodes from various work. Specific detectivity (D*) is thus referred and it can be written by:

$$\mathrm{D}^* = \frac{\sqrt{A\Delta f}}{NEP} \qquad \textbf{Eqn. 3.27}$$

with the capability of comparing the measured results of all photodiodes regardless of their different dimensions and testing bandwidth, D* naturally becomes the most important figure of merit for evaluating the detection performance of all photodiodes. A higher the D* value indicates better performance of a photodiode as compared to others. Furthermore, by combing with Eqn. 3.25 and Eqn. 3.26, Eqn. 3.27 can be expressed by

$$D^* = R_i \sqrt{\frac{R_0 A}{4K_b T}} \qquad \textbf{Eqn. 3.28}$$

It can be seen that, under a given temperature, the responsivity and the R_0A product should be maximized in order to produce a photodiode with high detection performance.

3.4 X-Y Readout with MESFET Switches

3.4.1 Switchable Pixel

A pixel, short for picture element,is the smallest discrete unit for an imaging device such as FPA. In addition to being capable of light sensing, each pixel must be individually addressable or switchable so that the signals generated over the whole FPA can be transferred out in sequence. For imaging at visiblewavelengths this can be readily achieved by integration ofsilicon-based photodiodes with switching MOSFETs through CMOS technology. For implementing the new type of monolithic mid-IR FPA presented in Sec 3.1.3, GaAs MESFETs are required to form a switchable pixel accordingly. As shown in Fig 3.18, each pixel circuit consists of one GaAs MESFET interconnected to an antimonide-based mid-IR photodiode. The P node (or anode) of the photodiode is grounded while the Gate node and Drain node of MESFET are used for switching control and signal output, respectively.

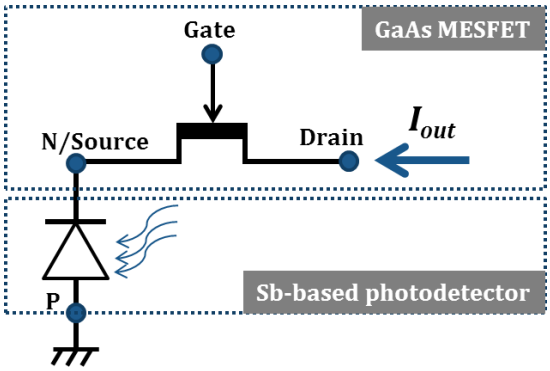


Fig. 3.18. Schematic of the monolithically integrated switchable pixel.

An equivalent circuit is shown in Fig. 3.19 (a) for a better understanding of the pixel operationand signal switching. The photodiode can be represented by two ideal current sourcesI_d and I_{ph}, a junction capacitorC_j and a shunt resistor R_{sh}which are connectedin parallelwith an ideal diode.As mentioned in Sec. 3.3.2,the two current sourcesI_d and I_{ph} stand for the dark currentand photo-generated current respectively whereas R_{sh}approximately equals to the dynamic resistance of the photodiode.As mid-IR photodetectors are commonly operated either at zero bias or with an applied

negative biassmaller than 300mV [114,115,121], the voltage drop between Drain and Source nodeswill be smaller than the saturation voltage of the MESFET (approximately 1V for 1 µm gate length according to Eqn. 3.12), which will thus operate in the linear region. The MESFET conducting channel can therefore be treated as a Gate controlled variable resistorconnected across the Drain and Source nodes. With regard to the Gate electrode, there will be a leakage current from Source to Gate, represented by I_{GL}.

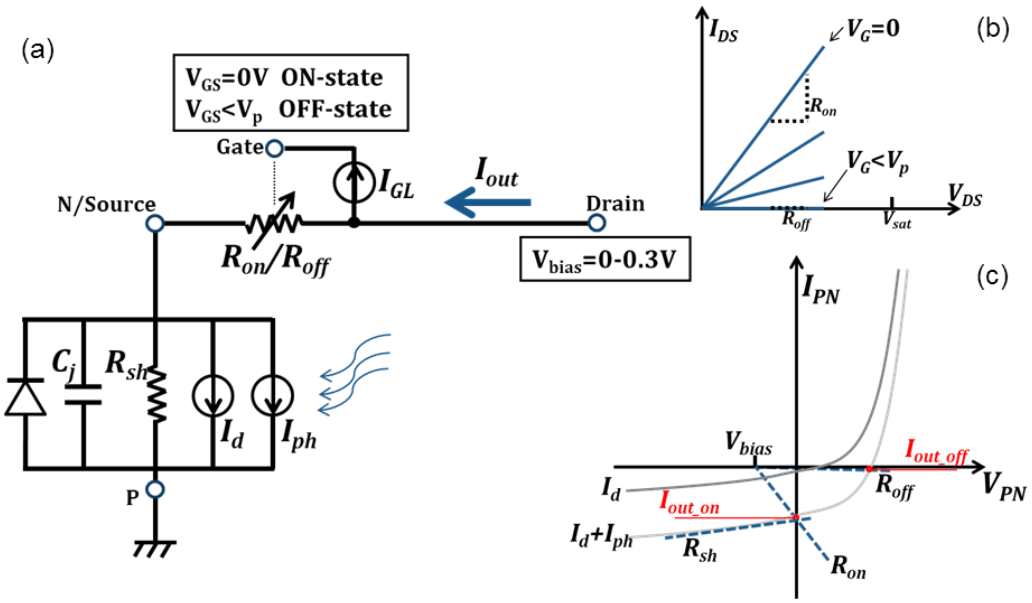


Fig. 3.19. (a) Equivalent circuit of the switchable pixel (b) current-voltage characteristics of the GaAs MESFET when operating in linear region (c) illustration of the switching operation with current-voltage characteristics of the photodiode.

When the switching MESFET is turned ON with V_{GS}=0V, the corresponding Drain-Source resistance is referred to as ON-state resistance R_{on}. The output current obtained at the MESFET Source node can be expressed by

$$I_{out\_on} = \eta_{on}\left(I_d + I_{ph}\right) + I_{GL} \approx \eta_{on}\left(I_d + I_{ph}\right) \qquad \textbf{Eqn. 3.29}$$

whereη_{on} is the ON-state transfer efficiency of the switching MESFET, which is given by

$$\eta_{on} = \frac{R_{sh}}{R_{sh} + R_{on}} \qquad \textbf{Eqn. 3.30}$$

Compared to the transferredphotodiode currents, the Gate leakage is considerably small and thus negligible at ON-state. This equation indicates that in order to maximise the transfer efficiency and obtain maximised output photocurrent, R_{on} has to be small as compared to R_{sh}.

The switching MESFET is turned OFF by applying the required negative bias to fully pinch off the conduction channel. As discussed in Sec 3.2.2, due to the existenceof substrate leakage current, the OFF resistance R_{off} of a MESFET will have a finite value. In this case, the output current is expressed by

$$I_{out\_off} = I_{GL} + I_{subs} \approx I_{GL} + \eta_{off}\left(I_d + I_{ph}\right) \quad \textbf{Eqn. 3.31}$$

Similarlyto Eqn. 3.30, the OFF-state transfer efficiencywill be given by:

$$\eta_{off} = \frac{R_{sh}}{R_{sh} + R_{off}} \quad \textbf{Eqn. 3.32}$$

Therefore, ifR_{off} is sufficiently large as compared to R_{sh}, the output current will only be determined by the gate leakage current from Drain to Gate node and given by Eqn. 3.8.

However, because the Source node of MESFET is connected to the photodiode N node instead of being grounded directly, the photocurrent-induced voltage change at this shared node can significantly affect the switching behaviour of the pixel device. This happens particularly under strong illumination(i.e. incident light with high power) since a large photocurrent is generated in the photodiode. Fig. 3.20 illustrates several possible biasing conditions for a pixel device. The Gate node is biased to a designed pinch off voltage aroundV_P=-3 V to switch the MESFET to OFF-state, while the Drain node voltageV_D is kept at 0.1 V for biasing. With increasing illumination power, the Source node of MESFET, which is also the N node of the photodiode, will be negatively charged by the accumulatedcarriers generated by the incident light. As a result, the photodiode will be forward biased and more importantly the MESFET Gate-Source voltagewill become less than the pinch off voltage ($V_{GS}=V_P+0.3V$). The channel is then no longer fully pinched off andthe OFF resistance is dramatically reduced as aconsequence. According to Eqn. 3.31, significant leakage in the pixel device will be introduced even when it is supposed to be in OFF-state. This leakage is referred to as subthreshold conduction current which indicates the photo-generated signal in a pixel is not fully isolated by the switching transistor from the output node. Fortunately, since the forward voltage of a mid-IR photodiode is relatively small, the Source node voltage V_s will saturate at approximately 0.3V independently of the illumination power. Therefore, the subthresholdleakage can be effectively suppressed by applying a Gate voltage negatively large than V_P-0.3V to ensure fully pinch off the conduction channel.

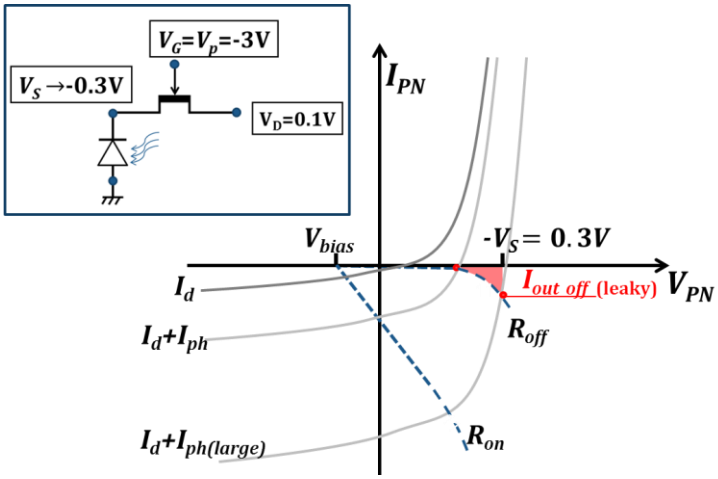


Fig. 3.20. Illustration of the subthreshold conduction leakage that occurs when the incident light power happens to be high.the graph in the inset shows the corresponding bias condition.

An external transimpedance amplifier (TIA) is often used to convert the photocurrent signal to voltage values for readout as shown in Fig. 3.21 (a). The final switching speed of the output voltage is an essentialparameter since it determines how fast the signal can be transferred out. Generally, the switching speed is quantified as the required time to switch the MESFET from ON-state to OFF-state or fromOFF-state to ON-state. Fig. 3.21(b) shows a typical timing diagram of the switching operation. The upper waveform represents the control signal applied to the gate node while the lower onepictures the correspondingtransient response of the pixel device. The switching time can be described in two ways: rise/fall time and ON/OFF time. The rise time is the time it takes for the output node voltage level to raise from 10% to90% of the final value when switching ON the MESFET.In contrast, the fall time is the time it takes for the output voltage level to drop from 90% to 10% when the MESFET is turning OFF. In a slightly different manner, the ON/OFF time is defined as the interval between thetime at which the digital control signal is at 50% of its final valueand the time at which the MESFET output node voltage level reaches its 90% and 10% value, respectively. The differentcebetween ON/OFF time and rise/fall time is known as the propagation delay.

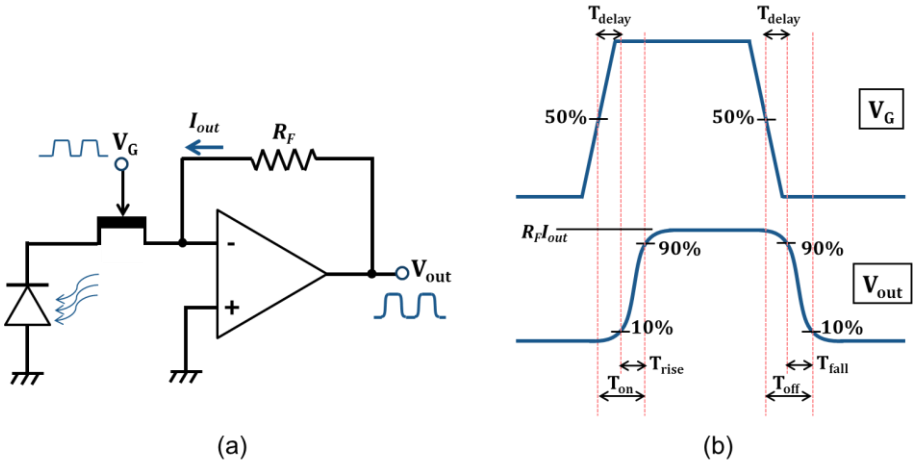


Fig. 3.21. (a) A readout circuit for pixel device with an external transimpedance amplifier to convert current signal into voltage signal (b) Signal waveforms illustrating switching times in a pixel device.

3.4.2 Array Structure and Pixel Addressing

Byreplicating the switchable pixels and aligning them into a 2D (M×N) format, a pixel array is formed. As illustrated in Fig. 3.22, with all P nodes of the photodiodes (anodes) at signal ground, each switchable pixel is connected to a common select line shared by M pixels in row and a common signal output line shared by N pixels in column. In order to complete the readout circuits with a full multiplexing function, external CMOS decoder chips and a TIA are added. For example, an array device with 4×4 switchable pixels will have four select lines controlled by the row decoder and four signal output lines linked to the column multiplexer, respectively. The single output line of the columnmultiplexer is connected to the TIA input for signal conversion and amplification.

The scanning operation of the array device starts by applying a negative voltage V_{off} ($<V_P$-*0.3V*), to each rowselect line to switch off the MESFETs and isolate all pixels from the columnsignal output lines. Then, driven by the row decoder, the voltage applied to the first rowselect line (RS_1) is pulled up to V_{on} (0V), enabling transfer of the photocurrent signal generated in the first row of pixels to their interconnectedsignal output lines in column. In a controlled sequence from CS_1 to CS_M, the signal on each column line is then passed onto the output node of the multiplexer for amplification.The readout of the first row of pixels is completed with pulling down the voltage applied on RS_1 back to V_{off} and applying V_{on} to the next row select line (namely RS_2) for another multiplexing cycle. This process repeats until the photocurrents are transferred out from the last row of pixels (RS_N).In this way, the whole M×N pixel array is scanned and a frame of image can be formed accordingly.

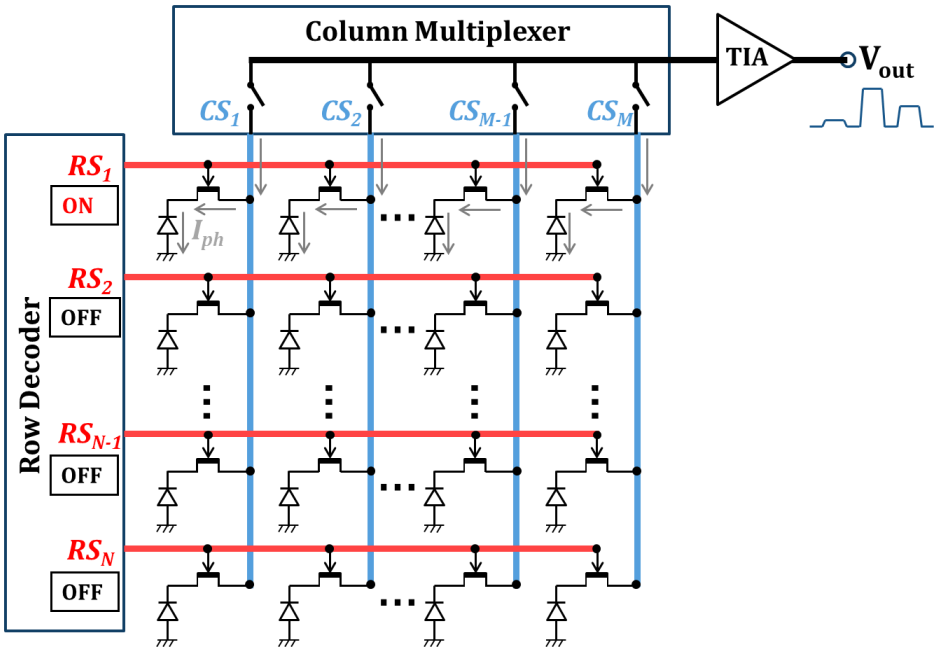


Fig. 3.22. Schematic of an M ×N array architecture demonstrating the selective readout of the first row of pixels.

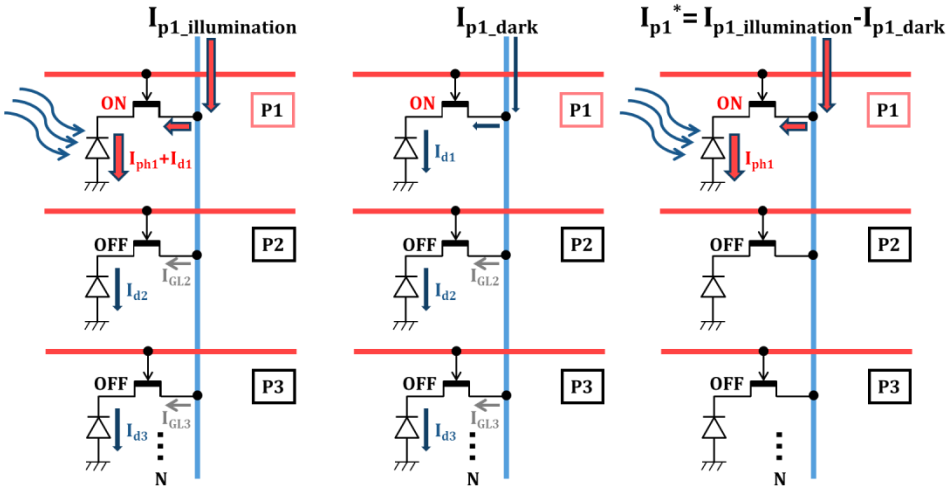


Fig. 3.23. Illustration of excluding the dark current and leakage current components generated by other pixels connected in column by correlated double sampling.

Differently from a single switchable pixel, the output signal lines in an array device are shared by pixels in column. As shown in Fig.3.23, in order to transfer current signal from apixel (P1 in this case) to the column line, the MESFET of the addressed pixel isswitchedON while MESFETs in other N-1 pixels are OFF.Following Eqn 3.29 and 3.31, when only P1 is illuminated and addressed, the total sensed current on the column line is given by:

$$I_{P1\_illumination} = \sum_{x=2}^{N} (I_{GLx} + \eta_{off} I_{dx}) + \eta_{on} (I_{d1} + I_{ph1}) \qquad \textbf{Eqn. 3.33}$$

Therefore, due to existing substrate leakage and Schottky Gate leakage currents in the OFF-state MESFET switches, the current signal sensed from one addressed pixel is always associated with leakage currents from other pixels. One simple way to effectively suppress this problem is measuring the current on the column line again but in absence of illumination, thus obtaining:

$$I_{P1\_dark} = \sum_{x=2}^{N}(I_{GLx} + \eta_{off} I_{dx}) + \eta_{on} I_{d1} \qquad \textbf{Eqn. 3.34}$$

After subtracting the dark sensed current from the sensed current under illumination, a processed column output current can be obtained, where both the dark current of P1 and the contributions from other pixels are excluded:

$$I_{P1}{}^{*} = \eta_{on} I_{ph1} \qquad \textbf{Eqn. 3.35}$$

This processing method is commonly referred to as correlated double sampling (CDS),and is particularly useful to calibrate the difference of output signal level introduced by the random variation of pixel characteristics [166].

Note that this CDSmethod is done by assuming illumination is only applied on the addressed pixel, which is obviously not the case most of the time during actual imaging. As shown in Fig. 3.24 (a), if pixel P2_2 is illuminated but not addressed, the column output current obtained when its adjacent pixel in the same column P1_2 is addressed can then be given by:

$$I_{P1\_2}{}^{*} = \eta_{off} I_{ph2\_2} \qquad \textbf{Eqn. 3.36}$$

It is obvious that there is a falsely sensed currentcomponent introduced by the illuminated pixel P2_2 even after CDS applied. In order to quantify this effect, an electrical crosstalk term is introduced [167], expressed as the ratio of falsely sensed current to the output current of the illuminated pixel:

$$X_{tlk} = \frac{I_{P1\_2}{}^{*}}{I_{P2\_2}{}^{*}} = \frac{\eta_{off} I_{ph2\_2}}{\eta_{on} I_{ph2\_2}} = \frac{R_{sh} + R_{on}}{R_{sh} + R_{off}} \qquad \textbf{Eqn 3.37}$$

Eqn 3.37 is applicable for all pixels sharing the same column output signal line. Therefore, it implies that electrical crosstalk, if present, will affect the whole column with its value dramatically depending on the ON/OFF resistance ratio of the switching MESFETs. Horizontally adjacent pixels such as P2_1 and P2_3 are much less sensitive to this electrical crosstalk since the output nodes of pixels in a same row are connected through CMOS switches inside the multiplexerthat provide excess OFF resistance in addition to that of the MESFET. However, as shown in Fig 3.24 (b), another source of

false detection caused byadjacent pixels is related to substrate backside reflection of angled incident light. This is referred to as optical crosstalk and its value is proportional to the distance between each pixel and the incident light angle. Both electrical and optical crosstalk should be minimised in order to obtain images that are representative of the captured subject both in terms of position, shapes, and colours.

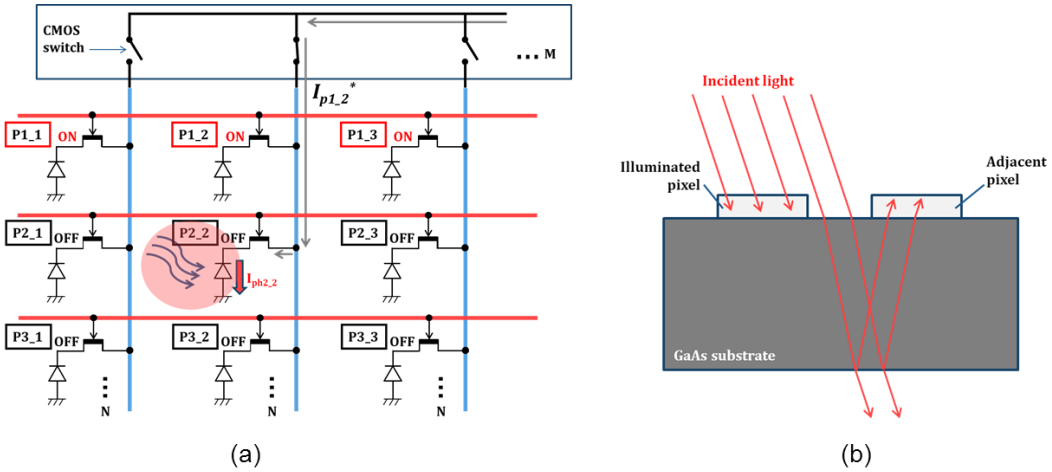


Fig. 3.24. (a) Electrical crosstalk due to OFF-state leakage of the MESFET switches and (b) optical crosstalk due to the reflection of angled incident light at the backside of the GaAs substrate.

With regard to the speed of the scanning process the most important parameter is the frame rate, which describes how many frames of images can be obtained through the array device within a second. For a given array size, increasing scanning speed will dramatically shorten the time slots available for transferring signal out from each pixel. Eventually, once the time allocated for readout is comparable to the ON/OFF time of the switching transistors, the maximum scanning speed achievable without sacrificing signal level will be reached. Because the array is horizontally scanned, the fastest switching occurs during the column multiplexing. Therefore, the maximum frame rate that the array can achieve is determined mainly by the switching time of the CMOS switches inside the column multiplexer rather than by the performance of the GaAs MESFETs in each pixel. Fig. 3.25shows an example of a timing sequence diagram for signal readout in a 64×64 array device which is recording video at 30 frames per second (fps), corresponding to a time slot of 33 ms per frame. In this case, the time allocated to readout a row of pixels is approximately 520 µs (33 ms/64). Given the ON/OFF switching time of a typical CMOS multiplexer is less than 100 ns [168], it is reasonable to set 5 µs for each column multiplexing and hence 320 µs in total for switching all 64

columns in sequence. Therefore, as long as the MESFET of each pixel has atotal ON/OFF time less than 200 μs, this kind of readout strategy can be adopted.

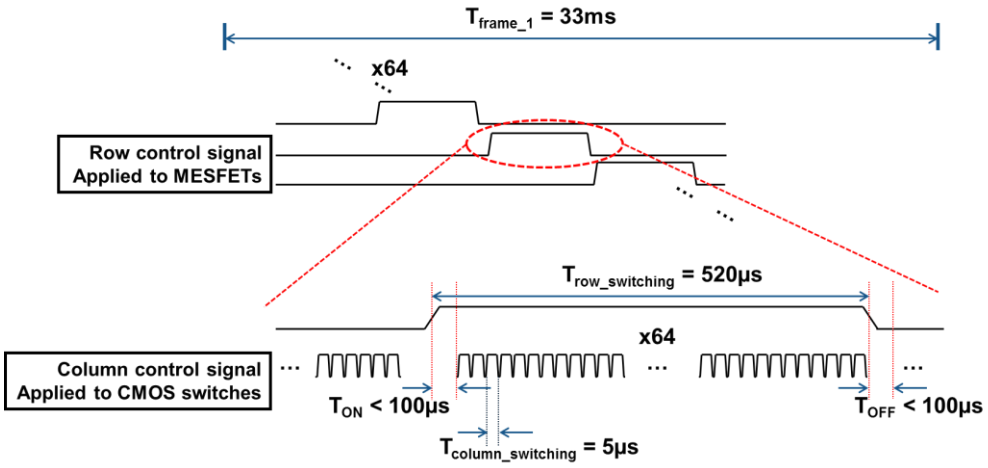


Fig. 3.25. Readout timing sequence of 64×64 array device obtaining video at 30 fps.

3.4.3Implementation Challenges

In order to realize a new type of monolithic mid-IR FPA based on the presented integration approach, a series of performance requirements for the fabricated GaAs MESFET should be met. In particular, according to Eqn. 3.29 and Eqn. 3.30, the ON-state resistance of the MESFET switch has to be as small as possible compared to the shunt resistance of the photodiode for maximized transfer efficiency. Since standard silicon-based photodiodes have a very large shunt resistance ranging from 10's to 1000's of MΩ [169], the effect of ON-state transistor resistance to transfer efficiency is minor. However, it is often not the case for mid-IR photodiodes especially when operating under high temperature. For example, under room temperature, the R_0Aproduct of most mid-IR photodiodes are around $10^{-3}\Omega cm^{-2}$ [119, 121]. This means a mid-IR photodiode with targeted active area of 50 μm × 50 μm will only present approximately 50Ω shunt resistance. Consequently, achieving Ron ≤ 50Ω becomes one of the key requirements of the corresponding pixel design to achieve >50% signal transfer efficiency. Moreover, in order to block out the electrical crosstalk, a high OFF-state resistance is desired. According to Eqn. 3.37, given Ron+Rsh≈100Ω, a >1MΩ OFF-state resistance for each pixel is required to achieve a small electrical crosstalk (Xtlk < 0.01%). The required switching speed of the MESFETs is moderate (μs range) and hence can be readily achieved by standard large dimension MESFET devices without being troubled by scaling the gate length into sub-micrometre range.

3.5 Summary

In this Chapter, the great potential for integration of the combination of mid-IR detectors with GaAs-based ROICswas demonstrated. In addition to providing a cost-saving substrate, GaAs can be used as a functional material to fabricate transistors and hence realize addressing circuits for the monolithically grown high performancemid-IR photodetectors. Among GaAs-based transistors, the MESFET is the most promising candidate for making large-scale integrated ROICs,due to the simplicity of its structure. By applying various biasing voltages to the Gate Schottky node, a GaAs MESFET can be used to modulate the conduction channel between its Drain and Source node, and switch between ON- and OFF-states. Therefore, when integrating MESFET switches with mid-IR photodetectors in series, a switchable pixel device can be created. More importantly, with the aid of external CMOS multiplexers and preamplifiers, these pixel devices are able to be further scaled into fully addressable monolithic FPA for mid-IR imaging.

4. Fabrication and Characterisation Methods

This Chapter briefly describes somekey techniques and methods used in this work to fabricate and characterise the monolithically integrated mid-IR photodetectors thatare presented in the previous chapter. The first section describes all the necessary micro or nanofabricationtechniques which can be accessed in the University ofGlasgow's James Watt Nanofabrication Centre (JWNC). The second and third sections outline a series of electrical and optical measurement methods used for evaluating the performance of the fabricated devices.

4.1 General Fabrication Techniques

Development of the fabrication process isperhaps the most challenging task in this work,since a monolithically integrated FPA device must be fabricated with reliable and repeatable techniques. While the next chapter will outline a detailed device fabrication processflow, this one will give an overview ofgeneral fabrication techniques. These include techniques forepitaxial growth,pattern definition,metallisation, materialetching, cleaning and passivation.

4.1.1 Material growth

Molecular beam epitaxy (MBE) is a commonly used technique to grow compound semiconductormaterials. As shown in Fig. 4.1, MBE growth is performedinside an ultra-high vacuum (~10^{-8}Pa) chamber. Initially, the elemental atoms or molecules (also referred to as effusion cells) are vaporised from high temperature sources. Given the very low pressure, the vaporised elements follow straight paths, forming beams that aresubsequently directedto thesubstrate surface, where the temperature is independently controlled to drive formation of the corresponding epitaxial layers. The delivery of a given effusion cell is physically controlled by a shutter and the growth thickness is monitored by the system usingin-situ analysis techniques such as reflection high energy electron diffraction (RHEED) [170].

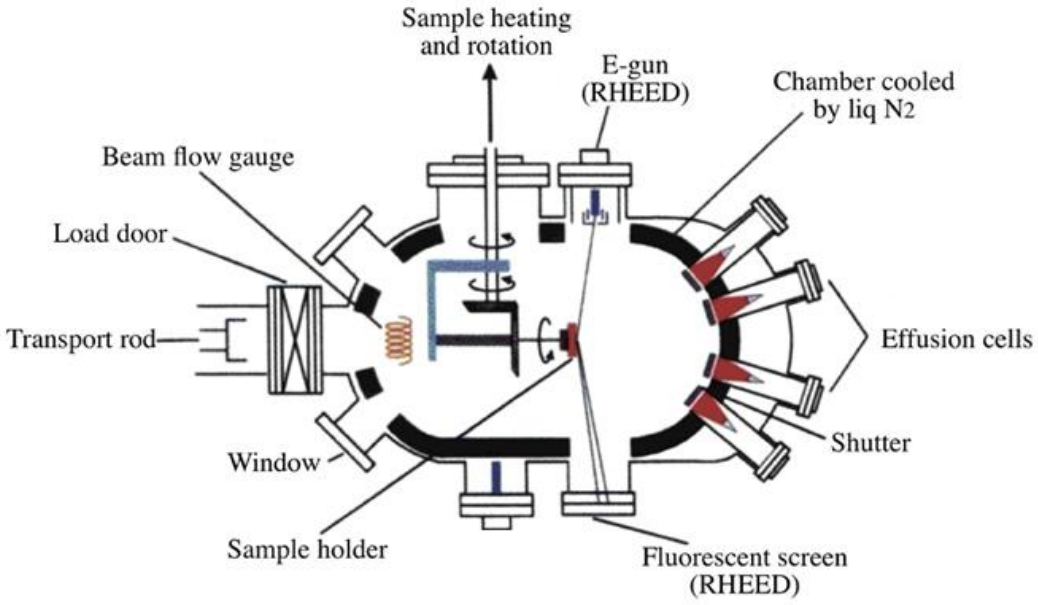


Fig. 4.1. Schematic of a simplified MBE growth system [170].

Compared to other epitaxy methods, MBE provides more highly controllable growth rates and material shutting or switching, leading to thicknesses of active layers precisely defined, and with very sharp interfaces in between [45, 171]. Moreover, MBE offers great flexibility for implementationofheterogeneous structures with various compositionsand dopants. Finally, as discussed in Sec. 3.1, MBE is currently the only technique that can achieve high quality growth of antimonide-based mid-IR sensitive materials onto lattice mismatched GaAs substrates. Because of the advantages described, all the active layer structures used in this works were grown by MBE on S-I GaAs 3-inchwafers.

4.1.2 Lithography

Lithography refers to the method used to define patterns or shapes into a radiation sensitive polymer material, called *resist*.The resist is used tomask certain regions of the sample surface during further processing of the underlying materials. Resists need to be applied onto the sample surface in advance, which usually happens by spin-coating.A dehydration baking follows, either on a hotplate or in a conventional oven.

Different kinds of lithography can be identified based on the mechanism used to define the shapes on the resist mask. The two lithography techniques which have been employed in this workare photolithography and electron beam (E-beam) lithography. The final choice of lithography technique for a certain process step is based on their unique set of advantages and disadvantages with regard to various aspects such as: the resolution, i.e. the minimum size ofthe designed patterns reliably transferred onto the

resist layer; the required alignment accuracybetween different lithographic layers; and finally the throughput, which refers to theproductivity of the device and is considered mainly inindustrial manufacturing in terms of the cost.

4.1.2.1Photolithography

Photolithography involves optical light at ultraviolet (UV) wavelengths, used to expose the underlying light-sensitive resists (photoresists) through a shadow mask placed in between the light source and the sample. The shadow mask, also known as photomask,generally consists of a quartz plate coated with a patterned layer of chrome to form transparent and opaque regions accordingly. As shown in Fig. 4.2, UV light can only pass through the transparent regions and expose the photoresist on the sample surface. This exposure changesthe chemical structure of the resist, and depending on the nature of this change two types of resist can be identified, either *positive* or *negative*. For positive photoresists (e.g. S1818, AZ4562), the interaction with UV light weakens chemical bonds in the resist, making the exposed regions soluble to a solution known as resist developer; the unexposed regions instead are unaffected by the developer. The opposite applies for negative photoresists (e.g. AZ2070), where the UV light causes molecule cross-linking and makes the exposed regions insoluble in the developer, while the unexposed regions remain soluble. In both cases, after resist development, the patternedphotoresist will display a pattern which is a direct and accurate reproduction of the designed photomask, and with corresponding device features.

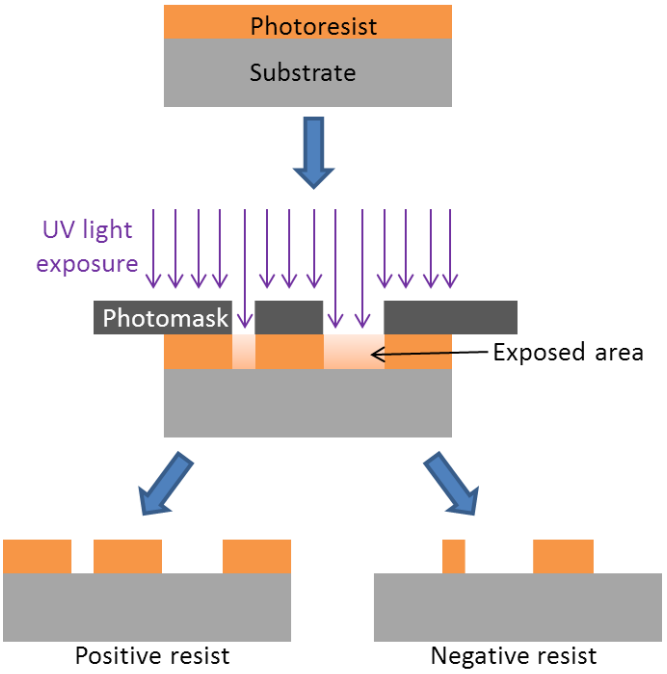


Fig. 4.2. Illustration of pattern definition using photolithography.

Because pattern definition for a largewafer area can be achieved simultaneously after a short-time UV exposure, photolithography naturally is a low cost technology, with high throughput and supporting mass production of semiconductor devices. The main drawback ofphotolithography is its relatively low resolution introduced by the diffraction effectswhenthe UV light is used to expose feature sizes which are close to the wavelength of light used (300-400 nm) [172]. Sincetheminimum feature size and alignment accuracy required in this work are both > 1 μm (see Sec. 3.4), a Suss Microtec Mask Aligner 6 (MA6)tool with a 350 W mercury lamp source (365nm) was employed to perform the photolithographic exposure for most of the process steps developed in this work.

However, although the manufactured photomasks can be reused for various batches of devices,new photomasks are always needed every time the designed pattern changes. This is ratherinconvenient, especially during the developmental stage of the fabrication processes for the novel monolithic integrated devices presented in this work.Sincesome device features neededfrequent tuning according to the outcomes of the fabrication tests, it was often decided to use E-beam lithography, described in the next section.

4.1.2.2 E-beam Lithography

E-beam lithography(EBL) sequentially writes patterns and shapes onto electron sensitive resists(E-beam resists) by using a beam ofelectrons focussed onto the sample surface. As with photolithography, there are positive and negative E-beam resist. In this work, only the positive E-beam resist—polymethyl methacrylate (PMMA) was used. This commonly used E-beam resist will become soluble by the corresponding developer (MIBK:IPAsolution) after exposed to electrons, forming the features according to the design.

A Vistec VB6 E-beam lithography tool housed in a Class 10 cleanroom of the JWNC was thus used in this work to write patterns that required frequent tuning. Fig. 4.3 shows a simplified structure of the VB6 system. Initially, the electron beam is generated inside the electron gun from a heated cathode, made of tungsten and coated inzirconium oxide. Assisted by the suppressor electrode, electrons are emitted only by the cathode tip and then quickly accelerated by the high electric field applied between the cathode and the extractor.Upon leaving the electron gun, this beam of high-energy,accelerated electrons is focussed by the focussing electrode. Two sets of deflection coils are then used to conduct the tilting and shifting alignment of the

beamwith the optical axis. In order to manipulate the focus of the beam on the substrate, a series of lenses are applied. The magneticcondenser lens C2 togetherwith the upper electrostatic lens C1 are used to adjust thespot diameterof the beam without changing the focus and current density. The divergence of the beam is controlled by selectable apertures. Furthermore, blanking plates selectively switch off the beam when desired bydeflecting it away from the optical axis and therefore are able to control the exposure time. Finally, another magnetic condenser lens C3 is applied to focus the beam onto the sample substrate.

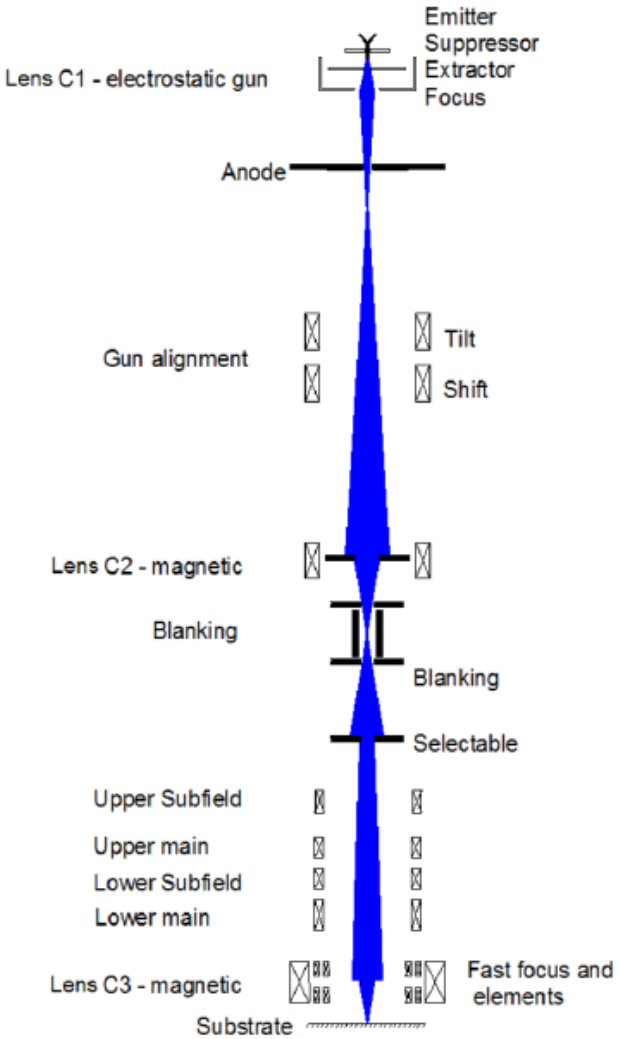


Fig. 4.3. Schematic of the Vistec VB6 electron beam lithography tool [173].

In this work, all patterns written by E-beam lithography were designed in Tanner L-Edit CAD software. The completed design file was exported inGDSII file format and then imported to the GenISys BEAMER software which put the design in a readable format so that it could be written by the VB6. In order to ensure the shapesdefined in the resist were not significantly distorted by the Gaussian profile of the focussed electron beam, or by the back-scattered electrons which cause unexpectedlyincreased

resist exposure (known as proximity effect), the pattern preparation with BEAMER started by adding proximity effect correction function. The E-beam tool in the JWNC can write shapes and patterns sequentially and continuously over a maximum area of 1.3 mm^2, because of the limited span of the deflection plates. Thus, patterning of bigger areas requires the VB6 stage to be moved mechanicallyto complete the patterning over the whole surface. As a result, the pattern preparation work also included fracturing functions to separate the designed pattern into mainfields and subfieldsin order to guide themechanical movements of the stage and of thedeflection coils, respectively.

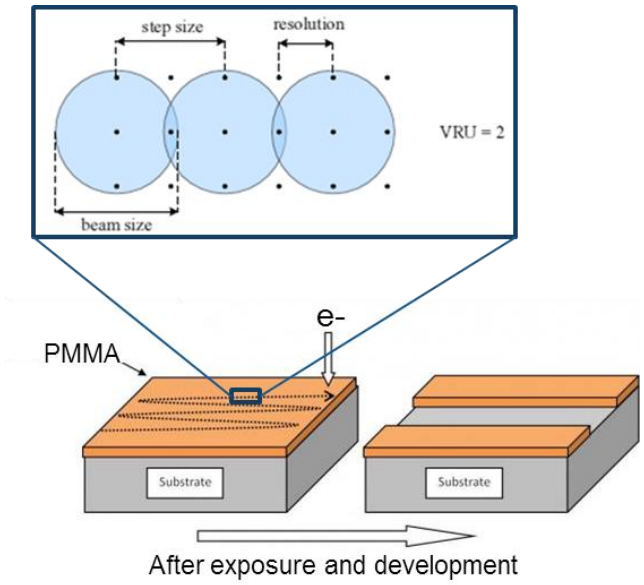


Fig. 4.4. Illustration of pattern writing by stepping the beam spot. The relationship between beam step size and resolution is also shown.

Once the pattern was ready to be written and had been transferred to the computer that controls the VB6, it was then necessary to set a series of other important parameters before proceeding with the lithography. This is done through a software called Belle, which was created in Glasgow to simplify and make E-beam patterning more accessible. The parameters set through Belle include the dose of the electron beam (determined by the currentdensity and the exposure time), the beam spot size, the resolution and thevariable resolution unit (VRU). This last quantity was used to define the step size with which the electron beam exposes the resist point-by-point until completionof the pattern,,and it is given by

$$\text{Beam step size} = \text{VRU} \times \text{resolution} \qquad \textbf{Eqn. 4.1}$$

As the smallest available current is 1nA, corresponding to a spot size of 4 nm in the VB6 system,nanoscale features can be readily created with extremely high alignment accuracy. More importantly, since only digitally created patterns are used,E-

beam lithography providesgreat flexibility in changing pattern designs between test sampleswithout the need for fabricating new photomasks as in photolithography. However, E-beam lithography is significantly more expensive than photolithography considering the much lower throughput caused by a slow point-by-point exposure process. Therefore,in this work E-beam lithography was only applied for process steps where required alignment accuracy was rather difficult to achieve with MA6 tool. Moreover, once a designed pattern was optimised, it was then transferred to photolithography for cost reduction.

4.1.3 Metallisationand Lift-off

After patterning the resists by lithography techniques, metallisation by metal evaporation is one of the most frequently applied process steps to selectively coat the sample surface with thin films ofmetals. Metallisation in this work was achieved using two electron beam evaporation toolsavailablewithin the JWNC:Plassys MEB 450 and Plassys MEB 550. Both tools are quite similar to each other except for the types of metals available, withPlatinum (Pt) loaded in MEB 450, and and Palladium (Pd) in MEB 550, respectively.

An electron beam evaporation tool involves a chamberwith high vacuum(approximately 10^{-6} – 10^{-7}Torr). Initially, a high energy electron beam is used to heat the selected metalcrucible to itsmelting point, thus triggering the evaporation. Due to the highvacuum condition, the evaporated metal will move vertically within the chamber until it reaches the sample that hangs face-downabove the crucible with the melted metal. Once hitting the cold sample surface, the evaporated metal condenses and starts to gradually build up a thin film layer whose thickness is monitored by the machine through a crystal oscillator. The thickness feedbackis used to set the end point of the evaporation cycle once the desired value is reached.

Although the selected metal will be evaporated onto the whole sample, it will be in direct contact withthesubstrate only in the regions which are not masked by resist. On the other hand, metal film deposited on top of the resist will be readily removed when the resist is stripped, normally by means of a warm acetone or SVC-14 soak. In a fabrication flow, this process step is referred to as metal patterning by lift-off. Accordingly, the patterns that wereoriginally defined on the resist mask are transferred to the deposited metal thin film. The patterned metals are then used to form either

Ohmic contacts to semiconductor material or registrationmarkers tofacilitate alignmentbetween different lithographic layers.

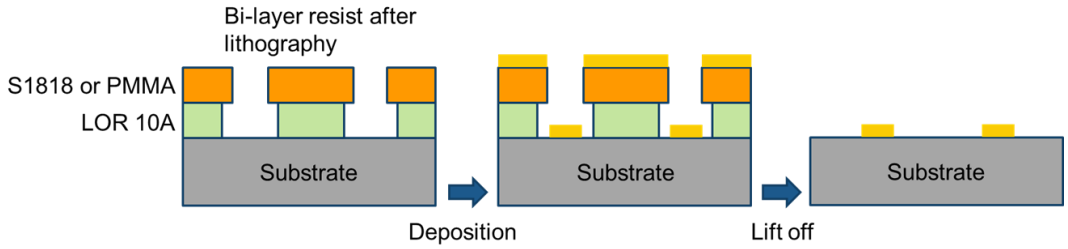


Fig. 4.5. Illustration of the lift off process flow using Bi-layer resists.

In order to successfully perform a lift-off step and forming a perfectly transferred pattern,it is very important to ensure adiscontinuity exists between the metal that is deposited on top of the resist and the metal that is in contact with the substrate. The most common way to achieve this is by applying a bi-layer of resist to create an undercut profile in the developed resist. In this work, MicroChem LOR 10A resist is employed to form bi-layer structures with either S1818 or PMMA. As shown in Fig. 4.5, the LOR 10A resist is specially designed to be solublein MF319 developer solution even without exposure. Therefore, by tuning the developing time, a considerable undercut with controlled overhang size can be achieved [174]. It must be notedthat atwo-stage developmentwas required in case of using E-beam lithography: MIBK:IPA for the PMMA andthen MF-319 for the LOR 10A.

4.1.4 Etching of Material

Etching of material is anothercriticalfabrication process which often takes place after lithography. Particularly in MBE grown structures, etching is required in order to selectively remove epitaxial layers for the implementation of the corresponding devices. Using both dry and wet etching techniques, etching steps incorporated in this work were mainly used to define the active light sensing area of mid-IR photodiodes, expose the channel layer for MESFET Gate formation and isolate each pixel in the array from the surrounding elements.

4.1.4.1Dry Etch

Among dry etching techniques for III-V materials, reactiveion etching (RIE) is perhaps the most popular one since it involves lower-costequipment than other etching techniques and it thus iscommonly available in many clean rooms including JWNC.As shown in Fig. 4.6, a typical RIE system consists of two electrode platesplaced in parallelwithin a vacuum chamber, where the upper electrode is grounded and the lower

electrode is capacitivelycoupled to a radio frequency (RF) signal. Before the start of the etching, the sample is loaded on the lower electrode plate; pumping of the chamber to the chosen pressure follows, then the desired gases are let into the chamber with controlled flow rates. When power is applied to the electrodes, due to their very high mobility electrons will respond to the rapidly varying RF potential and thusbreak the bonds with the parental gas molecules. However, the remaining ions, with much lower mobility, respond only to the time-averagedDC potential and are therefore accelerated towardsthe negatively charged powered electrode, where the sample is sitting.

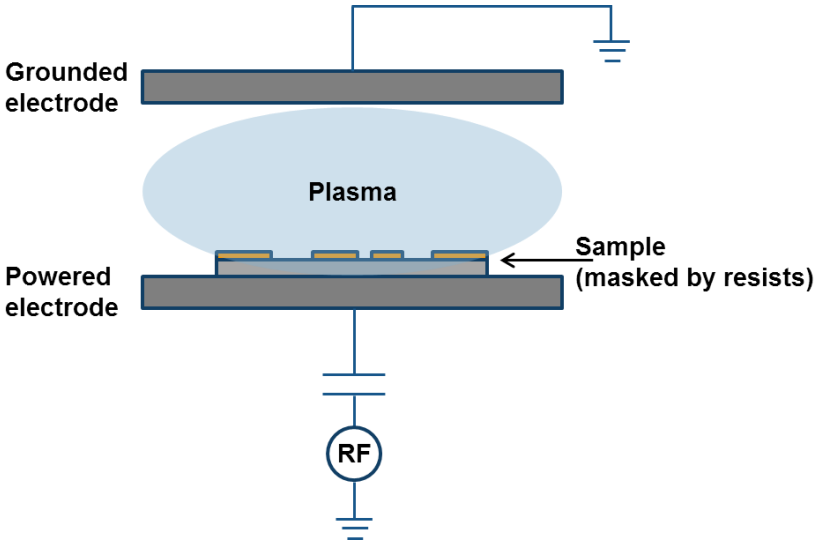


Fig.4.6. Basic structure of a RIE etcher with the sample placed on the powered electrode [158].

The etching in RIE systemsinvolves two mechanisms. One of them is physical sputtering, where the ions accelerated by the DC potential bombard the material surface andphysically knock atoms off the material. The other is chemical etching, where a reactiontakes place between the energetic ionsandthe exposed material surface with the resulting product volatised into the surrounding gas and extracted from the chamber. The prevalence of the physical or chemical mechanism is dependent on processing conditionssuch as the DC potential voltage, the RF power, the chamber pressure and the gas flow rate. The conditions will affect the sidewall profile of the etched material,which will be either isotropic, diagonal or vertical (see Fig. 4.7). The two latter sidewall profiles are obtained when physical mechanisms are dominant, thus they imply strong sputtering or bombardingand possible significant damage to the etched sample surface. Since generation of plasma and acceleration of ions are both accomplished by a single power supply, the ion density and bombarding energy cannot be controlled independently in a conventional RIE system. This means it is very hard to minimize plasma damage to the sample without sacrificing the etch rate or desired sidewall profile.

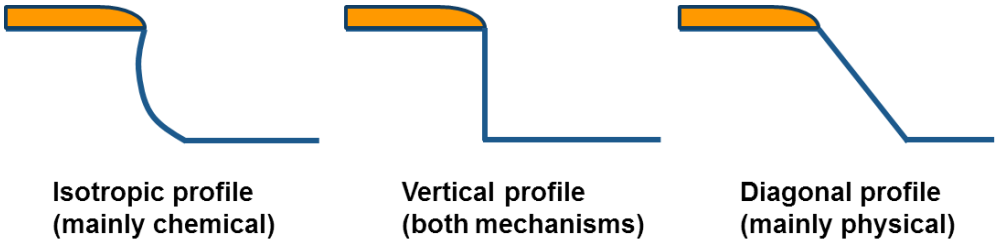


Fig. 4.7. Various possible cross-sectional profiles that can be obtained by dry etching depending on the preponderance of chemical and physicaletching.

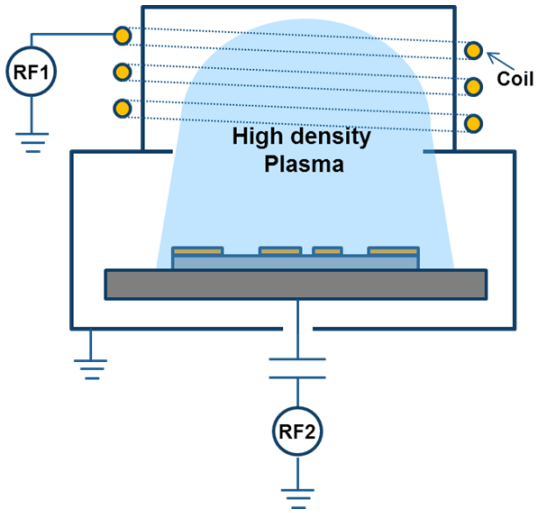


Fig.4.8. Basic structure of aICP-HDPEreactor with separated power supplies for plasma generation and ion accelerating [158].

This problem has been significantly suppressed by introducing high density plasma etching (HDPE) methods such as inductively coupled plasma (ICP). Fig. 4.8 shows a schematic of the ICP-HDPE reactor: it is very similar to a RIE system,but relies on separate power supplies,on to drive plasma formation and one to accelerate the ions. The improved chamber architecture and the extra power supply allow the ICP chamber to operate at much lower pressures (<20 mTorr) and the ion density to be two orders of magnitude greater as compared to RIE methods [158]. More importantly, the incident ion energy can be controlled semi-independently by the capacitively coupled RF power applied at the lower electrode where the sample sits. As a result it is possible to achieve optimized etching conditions, minimising plasma-induced damage while obtaining high etch rates. Furthermore,due tothe low chamber pressure, etching of large areas with good uniformity can be expected [175].

In this work, an OxfordInstruments RIE80+ tool was used to etch thin layers of silicon nitride(SiN_x)with sulfur hexafluoride (SF_6) gas. A dry etch process suitable for antimonide-based III-V materials and offering tuning of the sidewall profile was developed based on a methane (CH_4), hydrogen (H_2) and argon (Ar) mixture in an OxfordInstrumentsICP 180 tool. Moreover, all dry etching processes were monitored

with an interferometer which shone a laser beamonto the exposed sample surface. Due to the phase difference between the light reflected at the sample surface and at the underlying layer interfaces, interference oscillations can be observed when monitoring the intensity of the reflected laser beam. The actual shape of the oscillations is dependent on the refractive indices of the various materials and thus the interferometer trace can be used to determine the endpoint of a dry etch run by detectingthe desired stop material.

4.1.4.2 Wet Etch

In comparison with dry etching, wet etching is a much simpler and lower-cost method for removal of epitaxial layers, requiring only chemical solutions mixed in different stoichiometries.Generally, the mechanism of wet etching is based on the continuous repetition of a two-stage cycle: first oxidisation of the exposedsample surfacetakes place, then removal of the oxidised product follows by means of an acidic ingredient included in the etching solution. Therefore, one of the most notable advantages of wet etching is that it does not cause damage to the underlying active layers,thusavoiding performance degradationinthe fabricated devices. Quite often, a wet etching process step is applied right after dryetching processes in order to remove the damaged surface materials associated with high energy ion bombarding.

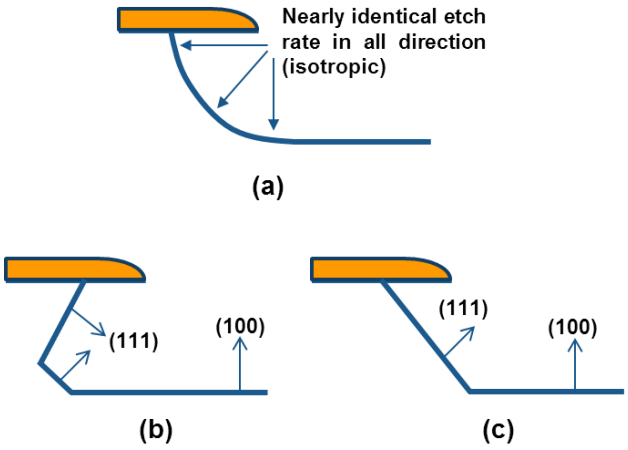


Fig. 4.9. Various cross-sectional profiles that obtained by wet etching: (a) isotropic profile, (b) and (c) crystallographic etch profiles in GaAs for (100) wafer.

However,the cycles of material oxidisation and oxide dissolution always occurin both the vertical and lateral directions, creating a post-etch undercut beneath the resist,shown in Fig. 4.9. As a result, it is difficult to precisely control the dimension of processed devices according to their original design, especially when relatively small features and deep etching are required. Besides, if notable etch rate difference exists for variouscrystallographic planes, the final etched sidewall profile can present

varyingsidewall angles according to the crystallographic orientationof the etched material. Fig. 4.9 (b) and (c) show cross-sections of two typical crystallographic orientation-dependent sidewall profiles obtained after certain GaAs (100) wet etching processes. In the case of a negative undercut in the sidewall profile of the etched material, metal connections crossing the etchedfeatureswill fail after metallisation. Since interconnections between etched isolated devices are crucialin this work, a positive sloped sidewall profile is always desired during the process development.

Despite the advantages, wet chemical etching is unfortunately very sensitive to variations of process conditions such as temperature, pH,aging of the solution and agitation of the sample. It is thus very challenging to develop a reproducible etching recipe that can provide a uniform etch rate across the whole sample. An effective way to suppress this problemis adding etch stop layers into the device structure. Generally, an etch stop layer is an epitaxial layer which is not etched or etched very slowly in the solution used to remove the corresponding unwanted material. This means that, in the area where the etch stop layer is reached first, once this is reached the wet etching process stops or slows down dramatically. As a result, by extending the etching time (over-etching), one can ensure the etch stop layer isuniformly reached across the whole sample. The etch non-uniformity and the advantage of using an etch stop layer is shown in Fig. 4.10. Nevertheless, in some cases, introducing an etch stop layer may not be trivial regarding the growth difficulty. Thus the reproducibility of a wet etching recipe may require equipment such as water baths with stirring options which can supply precise control of temperature and agitation of the etching solution. Moreover, some special precautionsmust be followed with regard to thetermination of a wet etching process. For example, when the sample is removed from the etchant, droplets of etching solution will remain on the surface and keep etching the material. It is thus very important to quickly rinse the etchant from the sample surface with running deionized (DI) water [158].

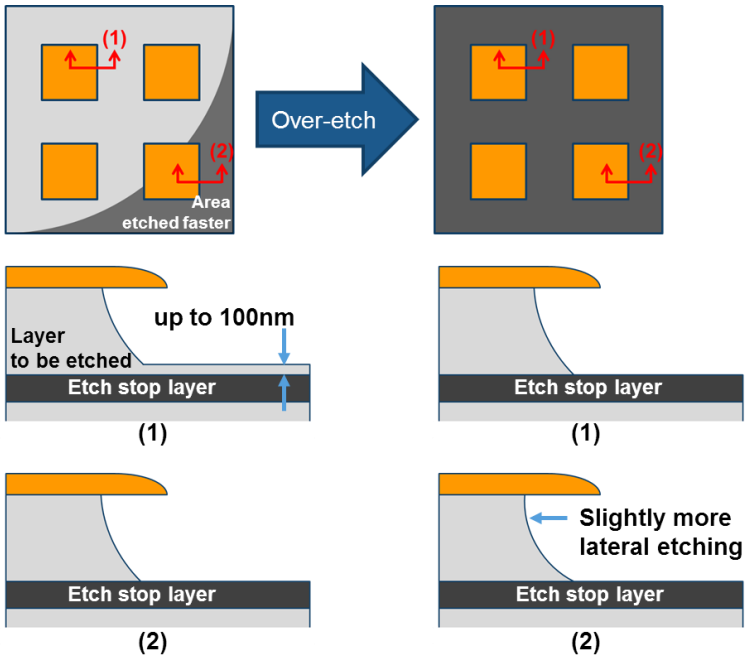


Fig. 4.10. Illustration of etch rate difference on various position of a sample during a wet etching process and using an etch stop layer to improve the uniformity.

In this work, several etching solutions were used, all based on mixtures of acidand hydrogen peroxide (H_2O_2). Citric acid, water and hydrogen peroxide ($(C_6H_8O_7)/H_2O_2/H_2O$) solutions with various stoichiometries were used for removal of un-masked InSb or InAsSb photodiode active layers. Since GaSb or AlGaSb compounds are etched very slowly by these mixture solutions (< 1 nm/min)[176], the buffer layer grown in between the antimonide-based materials and the GaAs layers can readily act as an etch stop layer and therefore make the mesa etching process highly controllable. For device isolation etching of GaAs, an orthophosphoric acid, peroxide and water ($(H_3PO_4)/H_2O_2/H_2O$)solution was used, and presented a positively sloped, crystal-orientation independent sidewall profile after etching. Finally, in the MESFET gate recess etching step, another $(C_6H_8O_7)/H_2O_2/H_2O$ solution was used to remove the heavily doped contact layer and reveal the channel layer without inducing any electronic damage. In case of a long etching (>1hr), a temperature controlled water bath with circular stirring motion was applied in order to achieve reproducible etching results.

4.1.5 Cleaning and Passivation

When processing compound semiconductor materials, the surface qualityplays a significant role in thereproducibility and the performance of the fabricated devices. Therefore, it is necessary to put in place effectivecleaningprocedures to remove any unwanted organic compounds or native oxides from the sample surface and produce asurface condition as close as possible to the as-grown one, beforeembarking on further

processing steps. After device fabrication is accomplished, electronic passivation of the cleaned sample surface with dielectric material is also essential to permanently protect the processed devices from the ambient environment.

Samples processed in this work all underwent the same cleaning procedure consisting of a sequence of soaks in the following order: SVC-14 stripper, acetone, isopropyl alcohol (IPA) soak and DI water rinse.After this cleaning procedure,a short time, low power oxygen (O_2) plasma ash in aET340 Plasmafab Barrel Asherwas conducted, to further ensure the removal of organic residues left on the sample surface prior to the lithography stage. Note that ultrasonic agitation was nevera part of the cleaning procedure, in order to avoid potential physical damage to the material.

III-V compound materials used in this work, GaAs for example, are known to have a layer of 2-3 nm of oxide formed at the sample surface after a long term exposure to the atmospheric air [158]. The existence of this native oxide layer at the metal-semiconductor interface can dramatically degrade the electronic characteristics of the formed contacts, particularly when low resistivity Ohmic behaviour is desired. Hydrochloric acid (HCl)/H_2O deoxidising solutionswerethus applied to dissolve the oxidised layers of the III-V semiconductormaterials prior to metallisation steps. However acid cleaning solutions tend to change the surface stoichiometry of the deoxided surface. In case of using HCl/$H_2O$to remove GaAs native oxide, due to the preferential reaction of acid solution with Ga, an As-rich surface will be created which can be undesirable for formation of Schottky barrier contact [158]. Consequently, before putting metal layers for MESFET gate electrode, ammonia (NH_4OH)/ H_2O solution was used. It is worth to mention that a monolayer of oxide can always grow within a few milliseconds after the dioxidetreatment and is thus unavoidable in actual fabrication, except with the use of in-situ de-oxidisation and metallisation techniques, which were not available.

The HCl/H_2O deoxidising solutionswere also used before sample passivation. Typically right after removing the native oxide, a SiN_x dielectric layerwas used in order to passivate the exposed sidewall of antimonide-based photodiodes and thus suppress the surface leakage current. The SiN_x layers were deposited using an inductively coupled plasma chemical vapour deposition (ICP-CVD) which allows deposition of dielectric materials at lower temperatures than other CVD methods and with improved material quality.

4.2 Electrical Characterisation

Electrical characterisations conductedat intermediate stages of the fabrication flow can provide extremely useful feedback for improving the design of the devices and their fabrication process. Thissection presents the main measurement methods that have been frequently incorporated in thiswork.

4.2.1 General DC measurements

Non-destructive electrical characterisation of partially fabricated devices or testing structures was carried out at room temperature using aCascade probe stationconnected to an Agilent 4155C Semiconductor Parameter Analyser (SPA).As shown in Fig. 4.11, four DC probes are mounted on manipulator arms which allow them to precisely move in three-dimensions.Therefore, assisted by microscope, the probetips can be manually placed on any desired positions where metal pads have been made on the fabricated devices. Controlled by a laptop runningAgilent EasyExpert software, the SPA can realize a series of characterisation functions. For instance, bysweeping voltages in between any two probes and measuring the resulted current flow, current-voltage (I-V) characteristics of the semiconductor materials or devices under test can be obtained. The SPA also allows measurementsof three-terminal devices such as MESFETs, where the current flow from Drain to Source can be monitored with various DC gate bias voltages applied. Additionally, four probe measurements can be done, typically with passing current between two probes and using the other two probes to measure the potential difference. This is particularly useful for accurate measurements of Ohmic contact resistivity where the impact of theprobes series resistance has to be excluded.

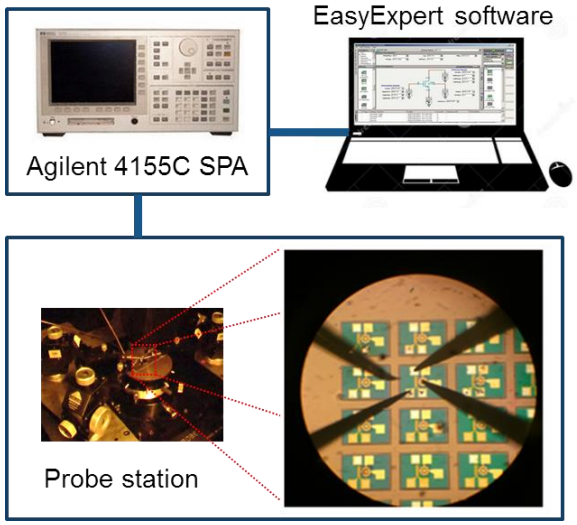


Fig. 4.11. Non-destructive electrical measurement setup based on probe station.

After device completion,characterisation was usually carried out outside the clean room.The samples with the completed devices were initially cleaved into pieces smaller than 6 mm, in order to fit on a 28-pin ceramic leadless chip carrier (LCC).Once mounted on the LCC, a wedge bonder was used to connect the metal pads of the devices to the corresponding output pins. Finally, mounted and bonded devices were loaded into matched PLCC sockets and attached on various testing circuit boards or equipment designed for further measurements.

At room temperature, the DC performance of packaged devices, loaded into a PLCC-DIP adapter, was measured using an Agilent B2902A 2-Channel Measurement Unit (MU). Similar to SPA, the measurement unit can force a bias voltage through the selected channels while sensing the resulting current flow at the same time, and hence the I-V characteristics of the testing device can be obtained. Besides, using an Agilent E4980A Precision LCR meter,capacitance-voltage (C-V) characteristics of the completed devices were also obtained. An illustration of the corresponding measurement setup is shown in Fig 4.12.

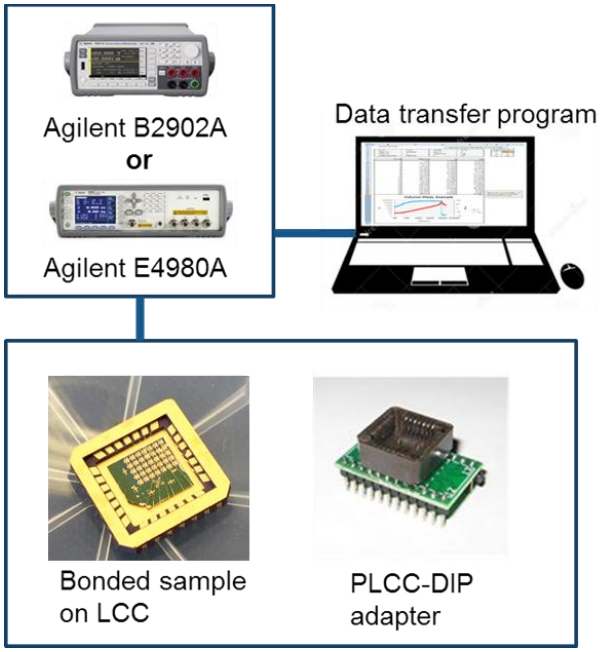


Fig. 4.12. I-V and C-V measurement setup for completed devices with LCC packaging.

Although all of the mid-IR detectors made in this work were targeted for room temperature operation, characterisation with liquid nitrogen (LN_2) cooling was also carried out for a better understanding of the performance of the fabricated devices. Dipping the wire bonded chips directly into LN_2 is the simplest way to achieve the required 77K cooling. For this purpose, a home-madeconnectorequipment, shown in Fig. 4.13, was used. It consists of a chip carrier socket mounted on a >20 cm long copper

rod; a series of electronic connections run between the socket pins and BNC connectors, which are attached to analuminium box at the end of the rod.Thanks to this mount, once the LCC with the mounted devices is loaded, its pins become fully accessible through thecorresponding BNC connectors. At the start of a measurement, LN_2 was poured into a foam bucket. Then, the whole connectorequipment with the sample loaded was turned upside down and carefully placed on top of the bucket. Because the dimensions of the aluminium connector box were much larger than the diameter of the bucket, only the chip carrier was immersed into the LN_2 leaving all the BNC connectors isolated from cooling for other electronic connections. Finally, after leaving the devices time to stably reach 77 K, I-V and C-V characteristics of the LN_2 cooled devices were obtained using Agilent MU and LCR meter respectively.

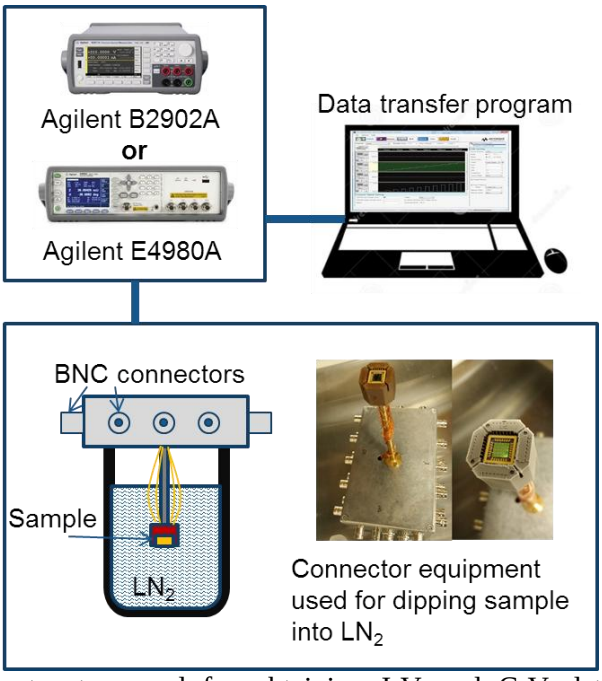


Fig. 4.13. Measurement setup used for obtaining I-V and C-V data at 77K. The LCC packaged sample was mounted on home-made connector equipment in order to be dipped into LN_2 directly.

4.2.2 Measurements for Etching Control

In order to monitor the wet etching processes and thus exposing the desired active layer for further fabrication steps, a simple etch depth control method based on the above mentioned probe station measurement setup was introduced. As shown in Fig 4.14 (a), with a distance of 20-30 μm in between, two probes were manually lowered to touch an open area of freshly etched semiconductor surface. A linearly increasing DC voltage was then applied while the current flowing between the two probes was measured. Since Schottky contacts were formed at the points where the metal probes directly touched the semiconductor material, the resulting circuit can be

treated as sweeping DC voltage on two Schottky diodes placed back-to-back.As a result, at a certain characteristic voltage, depending on the bandgap and doping level of corresponding material, the Schottky diodes would breakdown. As shown in Fig. 4.14 (b), a material with smaller bandgap or higher doping level will present a much larger leakage when biased and hence easier to breakdown at a smaller voltage. Accordingly, the stop point for a wet etching step can be judged based on these measured breakdown voltage if the stop layer is on a different material and has different doping than the layer lying above.

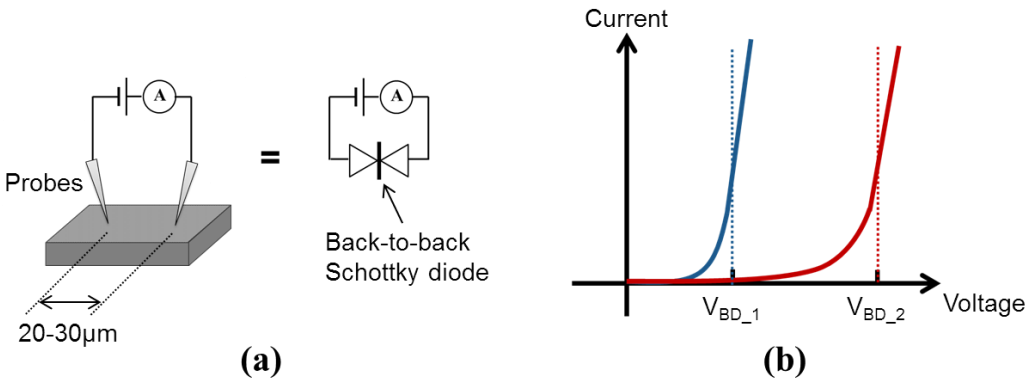


Fig.4.14. (a) Illustration of the two probe breakdown measurement method (b) typical breakdown voltage difference of two exposed device active layerwith different doping level where highly doped material present a smaller breakdown voltage.

4.2.3 Contact Resistivity Measurement

When developing fabrication processes for the implementation of the proposed mid-IR sensitive pixel device, there is always a strong need to form Ohmic contacts with the lowest resistivity possible to both antimonide-based materials and GaAs. As discussed in Sec. 3.2, a possible high contact resistance of the formed Drain and Source electrode can increase the total On-state resistance of the switching MESFET and thus dramatically reduce its signal current transfer efficiency after integration with the mid-IR photodiodes. Therefore, it is essential to have an accurate but simple measurement technique to determine and optimise thecontact resistance of fabricated devices.

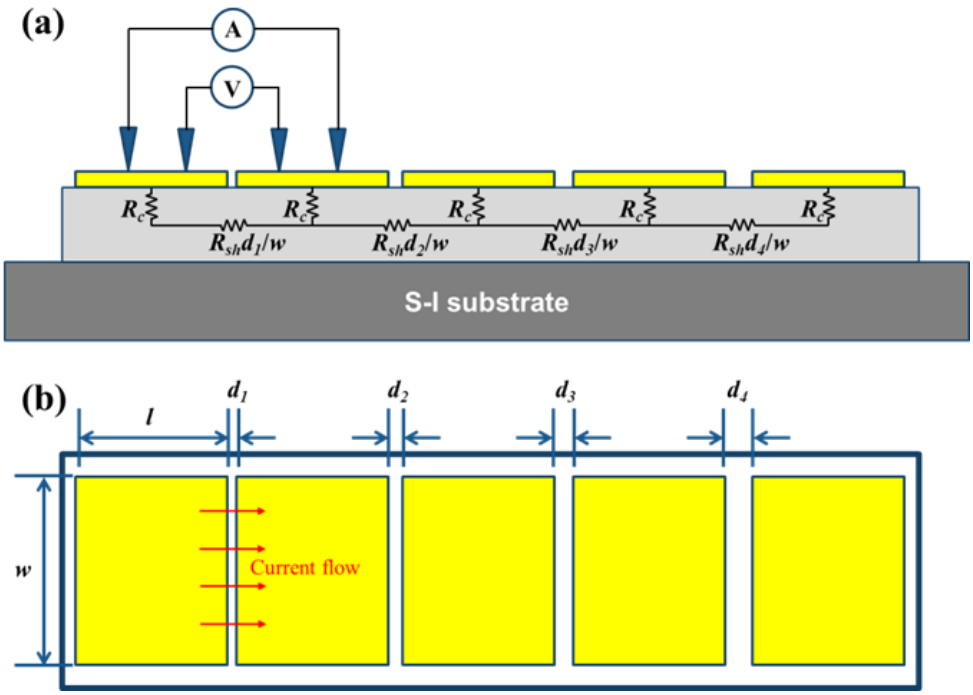


Fig. 4.15. (a) Diagram of four-point probes based resistance measurement (b) The top view of a standard TLM structure wheresquaremetal contacts areseparated by various distances *d*.

The transmission line method (TLM) is the most commonly used contact resistivity measurement technique. A typical TLM structure,asshown in Fig,4.15consists of a series of identical square pads with increasing distances separating them. Due to the increase of sheet resistance R_{sht} of the semiconductor material, when measuring the resistance between various pairs of pads in sequence, the obtainedvalue isexpected to increase linearly with the separation gaplength. At the point where the gap length is zero, the total resistance between two pads should be induced only by the two corresponding metal-semiconductor interfaces. As shown in Fig. 4.16, the contact resistance of a single contact $R_c$can thus be determined by half the value obtained from the intersection of the R-d characteristicwith the R-axis.The voltage under the contact follows anexponential distribution as the distance increases. The transfer length L_t, defined as the distancefrom the edge of the contact to a point where current density decreases by *e* times, can also be obtained from the R-d plot [177].

$$R_{total} = 2R_c + R_{sht}\frac{d}{w}$$

$$L_T = -\frac{R_c}{R_{sht}}w$$

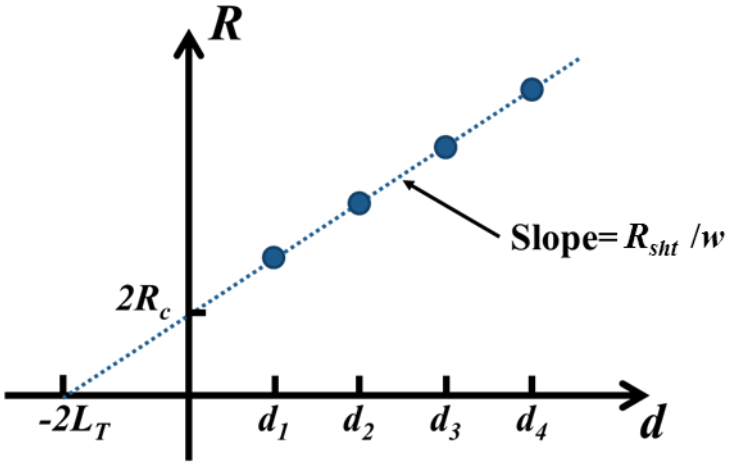


Fig. 4.16. Resistance-distance (R-d) characteristic for the extraction of contactresistance, transfer lenth and sheetresistance by standard TLM method.

However, in a standard TLM structure the current does not flow only along the gap between two metal squares, but presents lateral fringes. For the presented theory to be valid, an excess mesa etching step is thus required in order to ensure current flows between two metal pads only along the gap. This excess step is rather inconvenient, as less fabrication steps and fastcharacterisation are always desired when developing and optimizing process recipes for III-V materials. To simplify the development of Ohmic contacts, theso-called circular transmission line method (CTLM)has therefore been used [178]. Fig. 4.17 shows a typical CTLM structure layout which consists of circular contacts separated from a large common pad by ring-shaped gaps. Since this design allows current flow from every circular contact to the common pad regardless the direction, this approach thus avoids the need of an etchingstep to isolate mesas and can be prepared by a single lithography stage plus a metallisation and lift-off step.

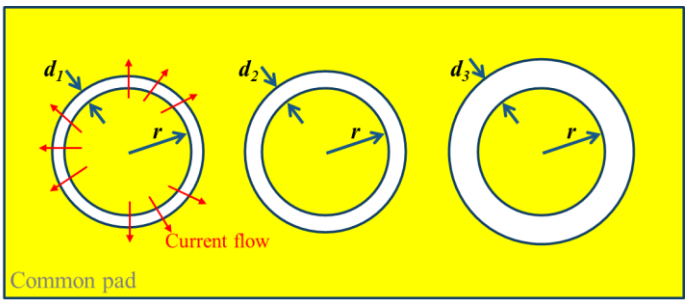


Fig. 4.17. The top view of a CTLM structure, where circular metal contacts are separated from a common pad by various distances *d*.

The CTLM structure designed in this work included 16 different values of gap spacing, varying from 3 µm to 48µm, and implying 16 differentresistance values obtained for one set of measurement. Similarly to standard TLM, the measured resistance increases accordingly with increasing gap spacing. However, the R-d characteristic obtained from the measurements presents a non-linear behaviour due to the nature of the circular structure design. The nonlinearity of the curve can be corrected by applying to each data point its corresponding correction factor C, given by

$$C = \frac{R_1}{s} \ln \frac{[R_1 + s]}{R_1} \qquad \textbf{Eqn 4.2}$$

where$R_1$is the radius of the inner circle metal disc, s is the gap spacing.

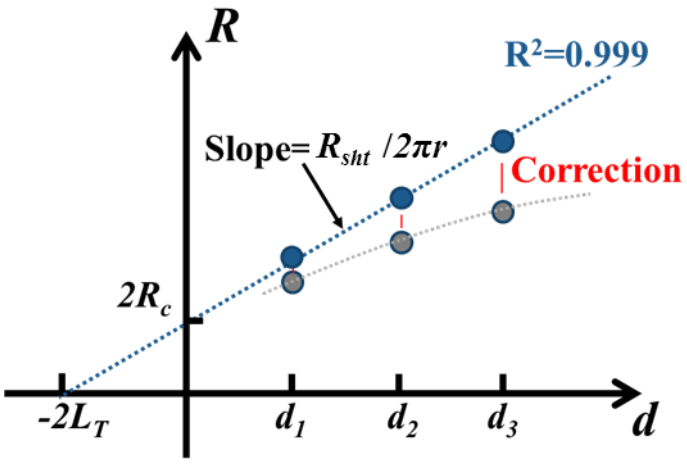


Fig. 4.18. Demonstration of data correction when using CTLM method to extract contact resistance, transfer lenth and sheet resistance from measured R-d characteristic.

As shown in Fig. 4.18, after the correction applied, the resistance values can then be treated as data obtained from standard TLM square pads with width Wc = $2\pi R_1$. The quality of the linear fit is measured by the Pearson product (Regression coefficient, R^2). From a good linear fit of theR-d characteristic ($R^2 \approx 1$),R_c, $R_{sht}$and $L_T$can both be obtained. If the metal contact is not notably alloyed with the underneath semiconductor, one can assume the sheet resistance $R_{sht}$is constant across the whole sample and can be extracted from the slope of the linear fit as well. Finally, the contact resistance is evaluated by the specific resistivity which is given by

$$\rho_c = R_{sht} {L_T}^2 \qquad \textbf{Eqn. 4.3}$$

4.3 Optical Characterisation

Once satisfied with the electrical behaviour, optical characterisation was then carried out using the completed devices mounted on LCCs. This section briefly outlines the main methods used in this work to evaluate the infrared light detection performance of fabricated detectors.

4.3.1 Fourier Transform Infrared Spectroscopy

The simplified structure of a Fourier transform infrared (FTIR) spectrometer is a Michelson interferometer which consists of a broadband IR source, abeamsplitter, a fixed position mirror M1, a movable mirror M2 and a IR detector [179]. As shown in Fig. 4.19,when the collimated IR light from the source is incident at the beamsplitter for the first time, half of the light is reflected to M1 while the other half is transmitted to M2. After reflection by the corresponding mirrors, the two returninglight beamsare recombined at the beamsplitter again. In the end, half of the returning light is directed towards the IR detector for intensity measurement while the other half is transferred back to the source.

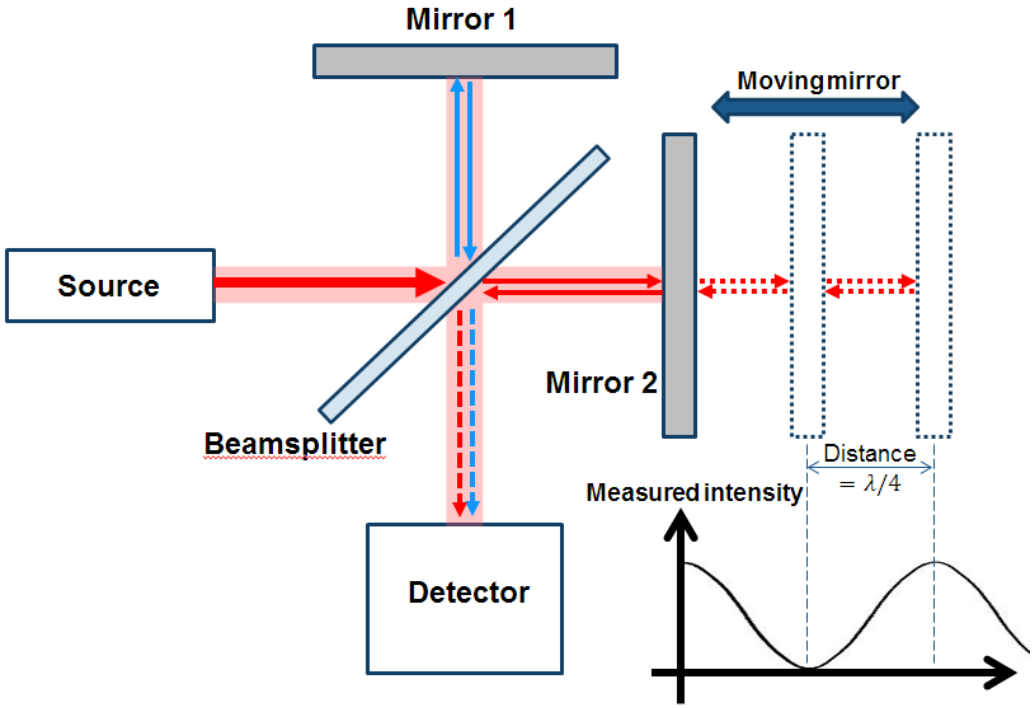


Fig. 4.19. Basic operation of a Michelson interferometer, which is the main partof aFTIR spectrometer.

At the beginning, when the distance between the centre point of the beamsplitter and each of the mirrors is the same, the light reflected from each mirror have the same optical path length resulting in constructive interference and hence measuring peak

intensity at the detector. Then, by moving M2 with a distance *x*, the path length of thelight that is transmitted to M2 is changed accordingly creating a difference of path length between the two returning lights. As a result of their phase difference, the two returning lights interfere with each other and create adeconstructive or constructive interference pattern with increasing *x*. Measuredby the detector, the resulting intensity change of the recombined light as a function of mirror positionis known as the interferogram. Finally, a Fourier transform is performed on the interferogram to produce a plot of the recombined light intensity as a function of thewavenumber, a unit that can easily be convertedto wavelength for a better understanding.

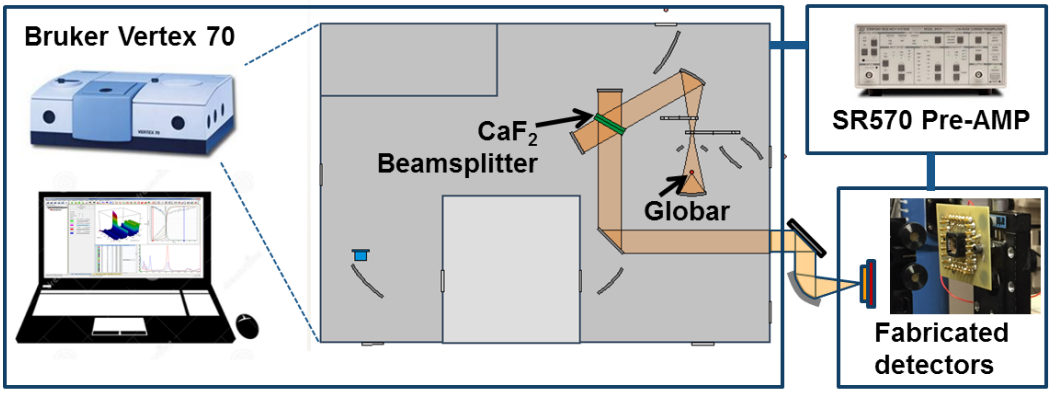


Fig.4.20. Measurement setup used for obtaining spectral photo-response of the mid-IR detectors fabricated in this work.

In order to measure the relativephoto-response of the fabricatedmid-IR photodetectors, a Bruker Vertex70 FTIR was used. It consists of aglobar source, the emission of whichpeaks at a wavelength of 2.4 μm, a calcium fluoride beamsplitter, a series of remotely controlled mirrors and multiple light input/output ports. As shown in Fig.4.20, characterisation was performed by firstly setting the optical path so that the recombined light after passing through thebeamsplitter could be coupled out of the FTIR system and hence focussed externally onto one of the devices fabricated in this work. The photo-generated current signal, which represents the measured light intensity, was then amplified by the SR570 transimpedance current preamplifier and fed back to the FTIR system for further Fourier transformation and data plotting.

4.3.2Laser Based Responsivity Measurement

The absolutephoto-response or responsivity of fabricated photodetectors to the infrared light wavelengths of interest was characterised by corresponding laser-based measurement systems.Fig. 4.21shows the two laser-based setups used in this work for characterisation of the devices. In order to measure the photocurrent responsivity of the devices under mid-IR illumination, a Hamamatsu Quantum Cascade Laser (QCL)

source, with a fixed 4.57 µm wavelength continuous wave output, was employed. Besides, photocurrent responsivity under a short wavelength infrared (SWIR) illumination (1.61 µm) was obtained as well using an Agilent 81940Atunable laser mounted on an Agilent 8164A Lightwave Measurement System.

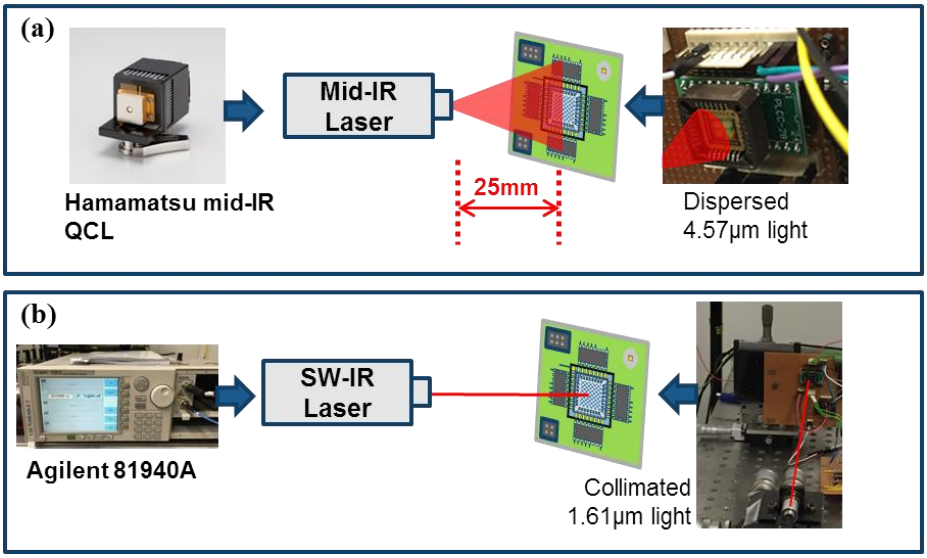


Fig. 4.21. Illustration of the two laser systems used to measure the current responsivity of fabricated photodetectors to (a) mid-IR light (b) SWIR light.

In both laser based measurement systems, since the laser spot is larger than the active sensing area of the photodetector A_{det}, the incident light power P_{det} received by the photodetector is estimated by

$$P_{det} = \frac{A_{det}}{A_{beam}} P_{tot} \qquad \textbf{Eqn. 4.4}$$

whereP_{tot} is the total power emitted bycorresponding laser, A_{beam} is the area of the incident laser beam spot illuminating the photodetector under test. Because of the low availability and difficulty to find the right optics for mid-IR,the output laser beam of the Hamamatsu QCL mid-IR was not collimated. The laser output consisted of an extremely divergent elliptical beam (30 ° vertical, 70 ° horizontal). During the measurements, the photodetector was placed approximately 25 mm away from the QCL source, thus an elliptical beam spot with area of 368 mm^2 was estimated accordingly (see Fig. 4.22). In case of using the Agilent tunableshort wavelength IR laser, which could be collimated much more easily by standard borosilicate lenses, a much smaller spot area of approximately 0.1 mm^2 was obtained.

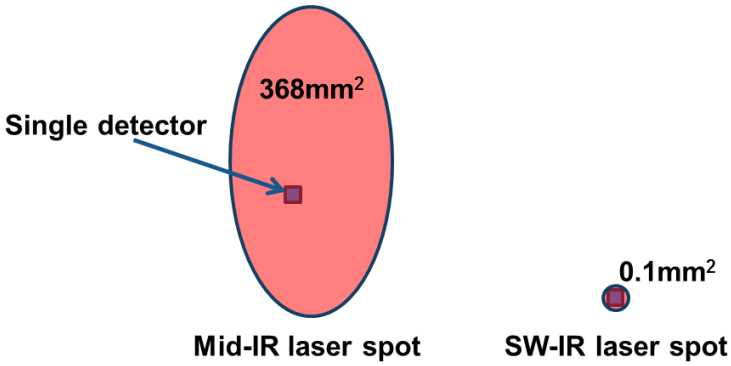


Fig. 4.22. Estimated laser beam spot size emitted from mid-IR and SWIR laser system used in this work.

Afterwards, the photo-generated current signal was amplified by the SR570 preamplifier and the transferred output voltage signal $V_{ph}$was measuredfora series of P_{det} values.Finally, through the linear fit of the V_{ph}-P_{det} characteristic, the measured current responsivity to a given light wavelength could thus be calculated by

$$R_i(4.57\mu m \text{ or } 1.61\mu m) = \frac{\Delta I_{ph}}{\Delta P_{det}} = G\frac{\Delta V_{ph}}{\Delta P_{det}} \qquad \textbf{Eqn. 4.5}$$

where G is the Gain (or sensitivity) of the SR570 preamplifier.

4.4 Summary

In this chapter,an overview of the main fabrication techniquesused in this work was presented. After a brief outline of the MBE material growth, both the concepts of photo-lithography and E-beam lithography were described and compared for different fabrication stages. With regard to design flexibility, e-beam lithography was initially used while nearly all of the developed processes would be finally transferred to be photolithography-based for cost reduction. Metallisation was then described, followed by illustration of a lift off process using a bi-layer of resist.As another critical process step, various material etching techniques based on both dry etching and wet etching were presented. Moreover, since the performance of devices which are going to be fabricated in this work is significantlydepending on the corresponding surface condition, appropriate cleaning and passivation of the sample surface throughout the fabrication is required. More details of using these techniques for actual device fabrication would be given in the subsequent chapter.

The chapter continued by describing characterisationmethods used in this work, based on either electrical or optical measurements. In order to non-destructively monitor the electrical performance of devices during the fabrication processes, a 4-channel probe station based measurement setup was used. A simplified material characterisation

method was developed particularly for monitoring the etching steps while the CTLMtechnique was employed to evaluate of the quality of the Ohmic contacts formed on the devices.The final section described two characterisation methods used to test both relative and absolute photoresponse of the fabricated mid-IR detectors,with an FTIR spectrometer and laser-basedsetups, respectively.

5. Fabrication Process Development

While the previous Chapter gave a general overview of the fabrication processes used in this work, this Chapter will focus onthose fabrication processesspecifically aimed at achieving monolithic integration of mid-IR photodetectors with GaAs MESFETs that is the core of both the proposed photo-pixel and FPA devices. The Chapter begins by describingdifferent MBE-grown layer structures used to fabricatedifferent batches of devices. The following sections detail thedevelopment of all the critical process steps, following the device fabrication flow. The developed processes include fabrication of photodetectors (both InSb- and InAsSb-based), etching of buffer layers, fabrication of GaAs MESFETs and interconnection between devices. Additionally, an InSb dry etching process, necessary for the fabrication of large area FPAs, is outlined. The Chapter ends by summarising the device fabrication flow, highlightingwhen the newly developed processes take place.

5.1 Growth of Layer Structures

In order to realise the novel monolithic approach discussed in Sec 3.1, the layer structures used in this work are designed to contain those well-established HOT mid-IR photodetector structures. More importantly, the corresponding narrow bandgap materials, either InSb or InAsSb, must be grown onto GaAs substrates which contain active layers for MESFETs fabrication.

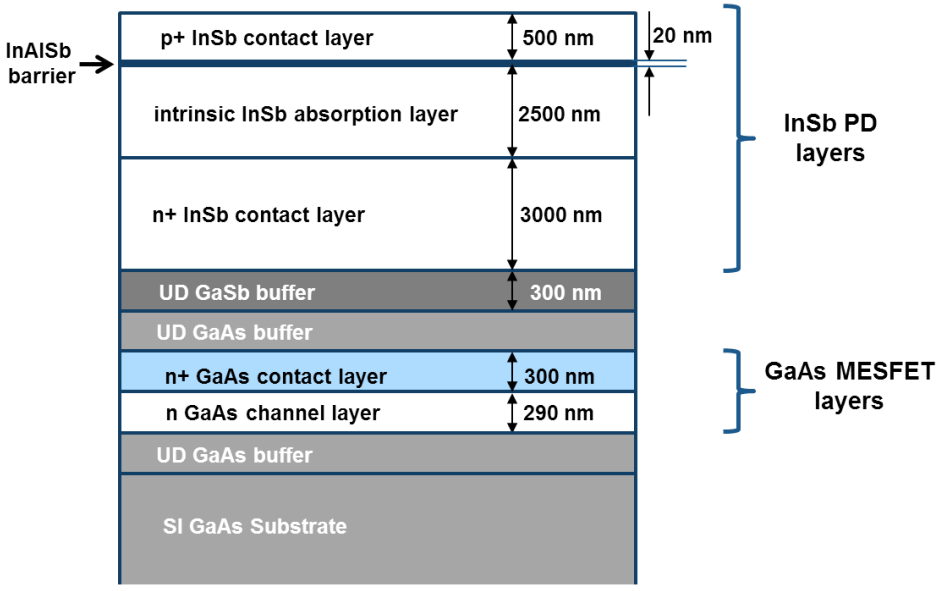


Fig.5.1. Diagram of the material layer structure used, highlighting the heterogeneous growth of GaAs and InSb device layers on aS-I GaAs substrate.

Fig. 5.1 shows the main layer structure investigated in this work. Growth was carried out on a 3-inch S-IGaAs substrate, and it started witha 500 nm thick undoped GaAs buffer layer. A200 nm thick Si doped GaAs channel layer was subsequently grown, with a donor density (N_d) of 1×10^{17} cm^{-3}, and a 300 nm thick contact layer of GaAs with $N_d = 2\times10^{18}$ cm^{-3} followed, completing the GaAs MESFET.A further 500 nm thick undoped GaAs buffer layer was then grown to separate the MESFET active layers from the antimonide-based materials. In order to allow relaxation of the strain introduced by the large lattice mismatch (14.6 %) between GaAs and InSb, a 300 nm undoped GaSb buffer layer wasgrown. Finally, as shown in Fig. 5.1., a non-equilibrium InSb photodiode with p-B-i-n structure [118, 119] was grown, including a 3 μm thick Te doped n+ contact layer ($N_d = 7\times10^{17}$ cm^{-3}), a 2.5 μm thick non-intentionally doped absorption layer ($N_d = 1\times10^{16}$ cm^{-3}), a 20 nm $In_{0.15}Al_{0.85}Sb$ barrier layer, and a 500 nm thick Be doped p+ contact layer ($N_d = 1\times10^{18}$ cm^{-3}).It must be noted that, although an intermediate GaSb buffer layer was grown, the following n-contact layer of the InSb photodiode was chosen to be particularly thickin order to further reduce the number of defects and threading dislocations, to the density of which is much higher next to the interface between the GaSb buffer and the InSb [180].

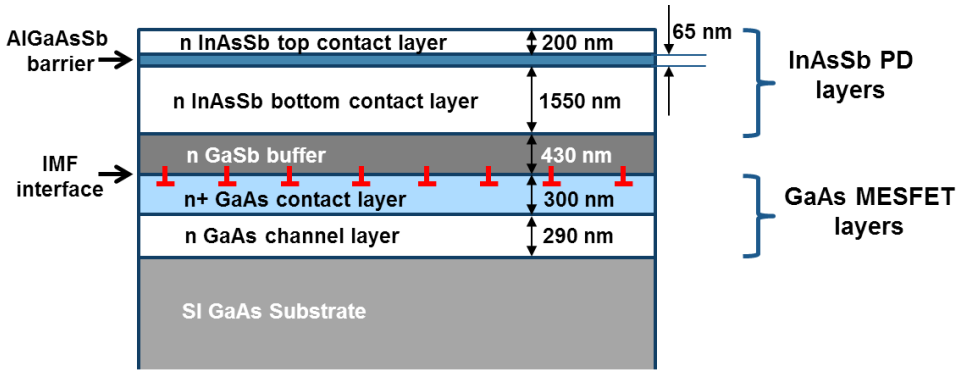


Fig. 5.2. Diagram of the material layer structure with InAsSb nBn photodetector being grown using IMF technique.

With the aim of proving the migration flexibility of this monolithic integration approach and achieve higher detection performance, a newly established nBn photodetector architecture was also tested. As shown in Fig.5.2, the InAsSb-based nBn structure was also grown on a S-I GaAs substrate. This wafer was grown in a different MBE system and provided by researchers from University of Lancaster [144, 146]. Therefore, the doping levels of MESFET active layers were slightly amended according to their suggestions in order to conduct IMF growth properly. In this case, MESFET active layers were made by a 290 nmthick Si doped channel layer ($N_d = 2\times10^{17}$ cm^{-3}) followed by a 300 nm thick contact layer of GaAs with $N_d = 1\times10^{18}$ cm^{-3}. The IMF

interface was then initiatedby growing a 430 nm thick high quality buffer GaSb layer (Sec. 3.1.1). Finally, using this GaSb layer as a thin “virtual substrate”, a lattice matched InAsSb nBn photodetector was grown, including a non-intentionally doped 65 nm AlGaAsSbbarrier layer sandwiched between a 1.55 μm thick absorption layer and a 200 nm contact layer, both n-type doped with $N_d = 5 \times 10^{17}$ cm^{-3}.

5.2 Fabrication of mid-IR photodetectors

After growth, wafers were cleaved into 12mm × 12mm square samples for fabrication of the photo-pixels and the FPA devices as described in Sec. 3.3. In both cases, fabrication of the mid-IR sensitive photodetectors is the first main stage. This section will outline the optimised processes used for fabricating photodetectors based on InSb and InAsSb respectively.

5.2.1 Fabrication of InSb Photodiodes

5.2.1.1 Formation of Registration Markers and P Contacts

Registration markers help aligning a pattern to features previously defined on the sample, and are essentialfor fabrication of devices comprising more than one stage of lithography. In this work, metal markers for both photo-lithography and E-beamlithography were formed as the first process step for each sample. After undergoing the cleaning process, the sample was coated by approximately 900 nm thick LOR 10A resist followed by pre-baking in a 180 ℃ oven for 1hr.A bi-layer of PMMA resist (15%+4%) was then spun on to the sample, baking each layer on a 180 ℃ hot plate for 5mins after spinning. Afterwards, the sample was patterned by the VB6 EBL system. Finally, after resist development, the markers were defined by evaporating Ti 50nm and Au 150nm onto the sample, followed by lift-off.

Due to the very small bandgap ofInSb and to the high doping level ($>1 \times 10^{18}$ cm^{-3}) of the P contact layer, the Ti/Au metal system can readily serve as Ohmic contact without the need for thermal annealing. As a result, formation of the metal markers and the photodiode P contacts were done simultaneously by defining thecorresponding patterns onto the resist in a single lithography andmetallisation stage (see Fig. 5.3). Compared to processes where both the P and the N contact of the photodiodes are realised in the same metallization step, formation of the P contact together with the metal markers prior to wet etch is preferable. The reason is the excellent planarity of the sample at this stage: after carrying out the following deep mesa etchess it would

beextremely challenging to form those small ring-shaped features with the process described.

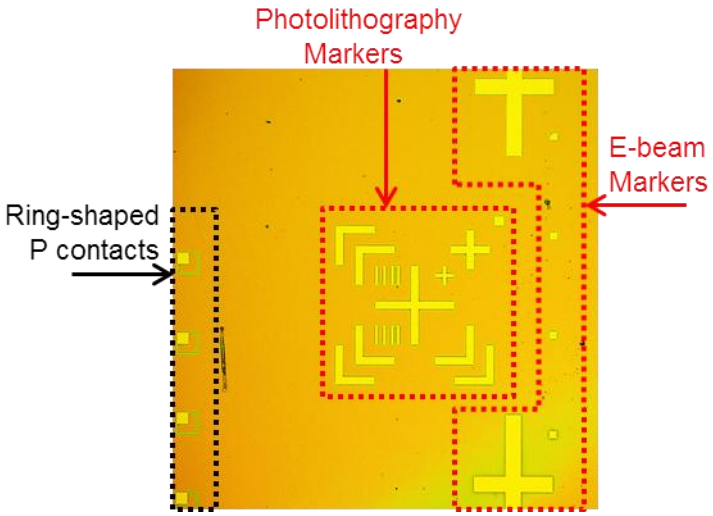


Fig. 5.3. An optical micrograph of a sample showing patterns defined in the LOR 10A+PMMA resist bi-layer for making both markers and photodiode P contacts simultaneously.

5.2.1.2First Mesa Etching and Formation of N Contacts

In order to define the active sensing area of the InSb photodiodes and reach the underlying n-doped layer onto which N contacts will be defined, a 1st mesa etching step was conducted after formation of metal marks and p contacts. As discussed in Sec. 4.1.4, to avoid exposing the sidewall of the photodiodes and the surface of the n-doped layer to possible plasma damage, a wet chemical etching process was preferred to dry etch.

The process started by patterning the etch mask for the 1st mesa etching. Two different masks can be used for this step: a hard SiN_x mask patterned through EBL, used during the developmental stages of the fabrication process; or a photoresist mask, used once the fabrication flow was established.

In case EBL was used, PMMA could not be used directly as etching mask. Due to its poor adhesion to the InSb samples,the outcome of the etching was very poor and the mesa shape poorly defined. A SiNx hard mask was thus required, and it was formed by coating the sample with the dieletric, which was subsequently patterned through EBL and dry etch. The sample was firstlyprepared for SiN_x deposition by dipping into a HCl:H_2O (1:2 by volume) solution for 1 min to remove the native oxide. This step was particularly necessary to improve the adhesion of the mask to the InSb material during mesa etching. Afterwards, a 400nm SiN_x layer was deposited onto the sample surface using a low temperature ICP-deposition process. A bi-layer PMMA (15%+2.5%) was

then spun on the deposited dielectric, followed by definition of the 1st mesa etching pattern with EBL. After resist development, SiN_x removal in the developed areas was achieved by dry etching using low damage SF_6 plasma in a RIE machine. As shown in Fig. 5.4, upon finishing, the pattern of mesa etching was transferred from the PMMA resist to the SiN_x hard mask and hence the sample was ready for the InSb to be etched.

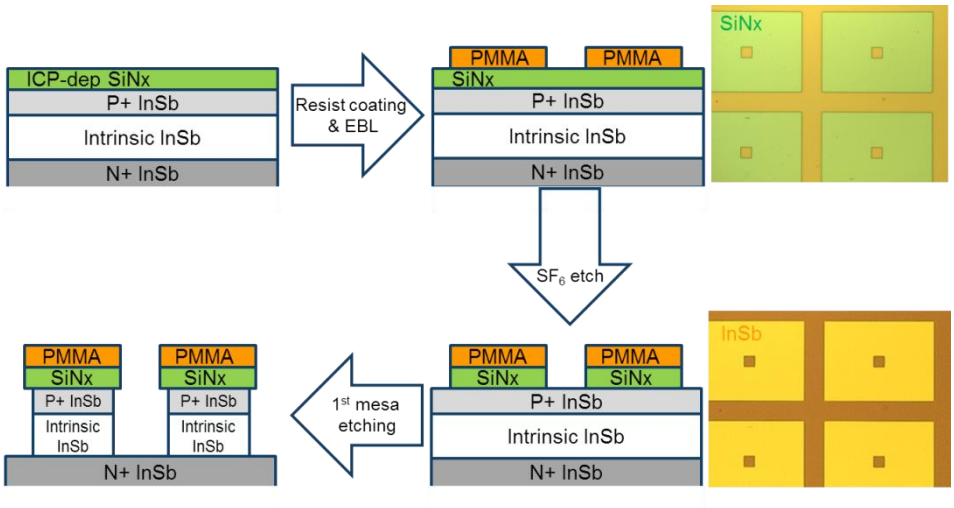


Fig. 5.4. Illustration of hard mask preparation process and mesa etching usingEBL. Inset micrographs demonstrate the pattern transferring from PMMA to ICP-dep SiNx correspondingly.

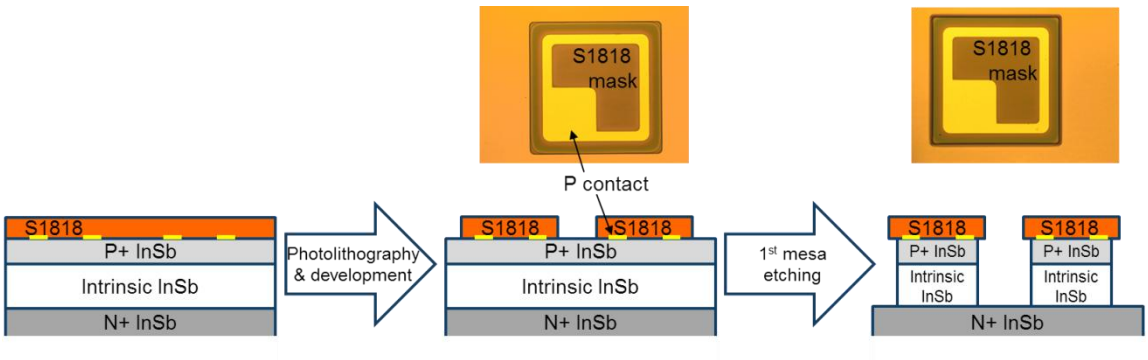


Fig. 5.5. Illustration of the simplified mask preparation process using photolithography. The inset micrograph shows the defined S1818 mask covering the P contacts of corresponding InSb photodiodes which were evaporated during formation of markers.

If resolution and alignment requirementsare moderate, a much simpler process can be realised with the use ofphotolithography to define the etch mask. Definition of the mask for the 1stmesa etch by photolithography was the method of choice in this work once the full fabrication flow had been established. Removal of native oxide using a HCl:H_2O solution (1:2 by volume) was carried out also in this case, then (see Fig. 5.5) a1.8 μm-thick film of S1818 photoresist was spun onto the sample and prepared for exposure. The sample was subsequently exposed by UV light using the MA6 system,

with a photomask containing the 1st mesa etching pattern loaded and aligned to the photolithography markers. Once developed, the sample was ready for the following etching.

A citric acid – hydrogen peroxide etchant mixture (110: 10: 70 $C_6H_8O_7$:H_2O_2:H_2O by volume) was then used to etch the InSb-based materials with a room temperature etch rate varyingbetween 15 and 20 nm/min. According to the layer structure, atotal etch depth of approximately 3.5 μm was targeted to reach well into the underlying N+ contact layer. Given the etch rate of the solution used, the 1st mesa etching can easily last up to 4 hours. As a result, in order to precisely control etching conditions the beaker with the etchant and the sample was kept in the water bath equipment at a constant temperature and with the circular stirring function always applied.

The obtained etch results are shown in Fig.5.6 (a) and (b). Despite its slow etch rate, the citric acid based etchant used can produce a very smooth InSb surface after etching. The resulting sidewall profile confirms that this wet etching process is highly isotropic, and with no obvious dependence on thecrystallographic orientations. The size of lateral undercut created beneath the photoresist etch mask is approximately 3 μm (close to the actual etch depth). With these properties, a set of photodiode mesas with different dimensions and shapes can be defined, as Fig. 5.6 (c) and (d) show.

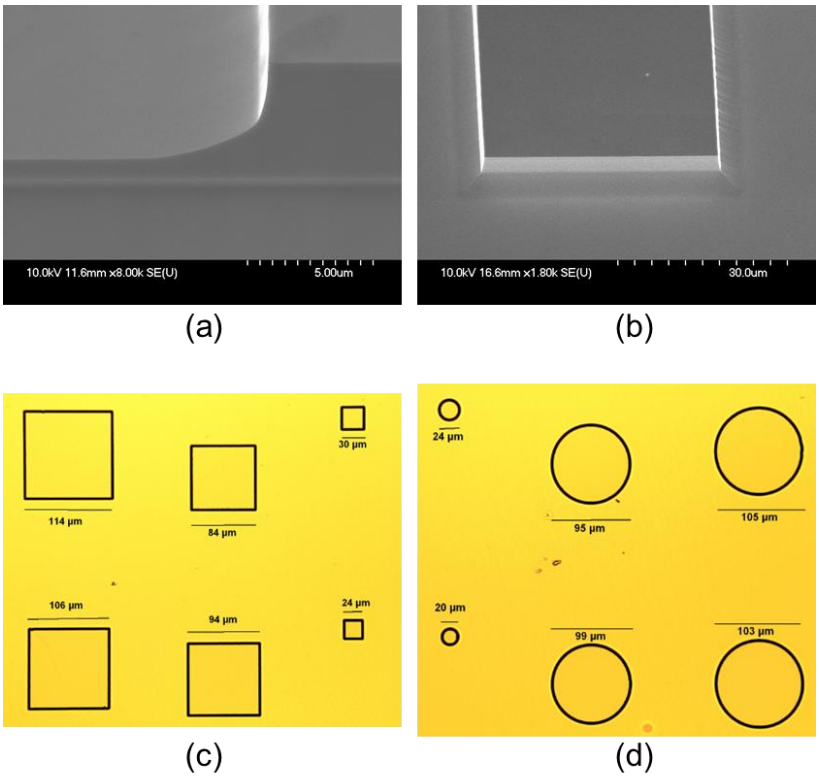


Fig. 5.6. SEM images (a) (b) and micrographs (c) (d) of the wet etched photodiode mesas with various dimensions and shapes for mid-IR light sensing.

Once the InSb N+ layer was reached, the etch masks were stripped off. This was done by low-damage SiN_x etch for samples processed by EBL, or simply by a warm soak in SVC-14 for photolithographic processing. The next step was the definition of the mask for the N contacts, achieved with a bi-layer of LOR 10A+PMMA resist written through EBL.Following resist development, a Ti 50nm/Au 150nm metal stack was evaporated, creating the N contact of the photodiode accordingly. Due to the varying resist thickness across the etched mesa steps, lift-off of small ring-shaped contact features done after etching on top of the photodiode mesas could be problematic. Instead, formation of P and N contacts separately, as used in this work, can avoid making small metal features simultaneously on top and at the bottom of the mesas. As a result, Ohmic contacts to photodiodes with active area down to 1.6×10^{-3} mm^2 (40 µm x 40 µm square mesas) can be readily fabricated (see Fig. 5.7).

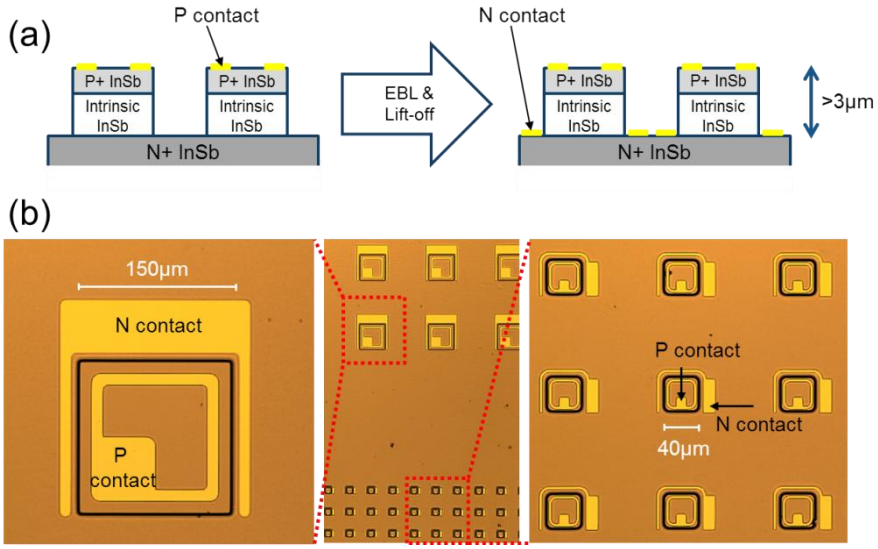


Fig.5.7. (a) A diagram shows the separated formation of P and N contacts of the InSb photodiodes. (b) Micrographs of a sample that have just defined small ring-shaped contact features to photodiodes with mesa dimensions as small as 40 µm×40 µm.

5.2.1.3Second MesaEtching and passivation

Next, a 2nd mesa etching step was performed to remove the unwanted InSb N+ layerand expose the buffer layers beneath it. Despite thedifference in pattern designs, this etching step is identical to the 1st mesa etching since exactly the same mask preparation processes and etchant mixture were used.

As discussed in Sec. 4.1.4.2, having a etch stop layer in the layer structure is always desired,particularly when uniform etching over a large area of the sample is required. During the2ndmesa etching, the citric acid based etchant offered over

30:1selectivity: theetch rate of InSb was ~20nm/min, while that of GaSb was only ~0.6 nm/min. The GaSb buffer layer could therefore act as an etch stop layer to terminate the etch process with great uniformity, as Fig. 5.8 shows.

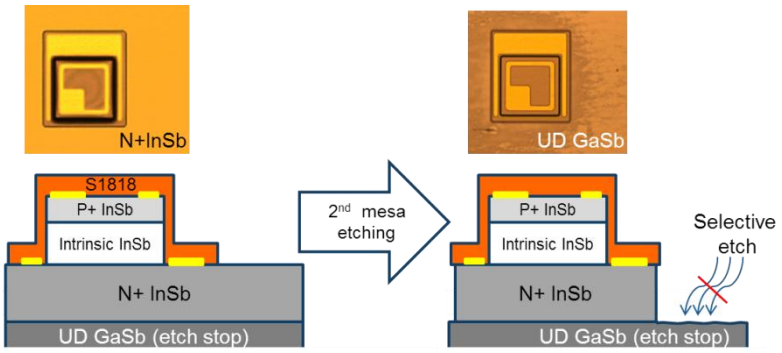


Fig. 5.8. Illustration of the 2nd mesa etching process, terminated by the underlying GaSb buffer layer. The inset micrographs shows the clear surface roughness change once hitting the etch stop layer.

However, since the etch rate of the citric acid-based wet etching process was slightly different every time, it was very hard to judge the time required to fully remove the unmasked N+ InSb contact layer. An estimate of the required etch time was thus initially used, after which the sample was observed under a microscope. As the surface of the GaSb buffer layer showed obvious increase of surface roughness after exposure to the citric acid etchant (seethe inset micrograph in Fig.5.8), this resulted in a colour change of the etched sample surface. The observed colour change was one of the important indications of etching termination once the GaSb buffer layer was exposed.

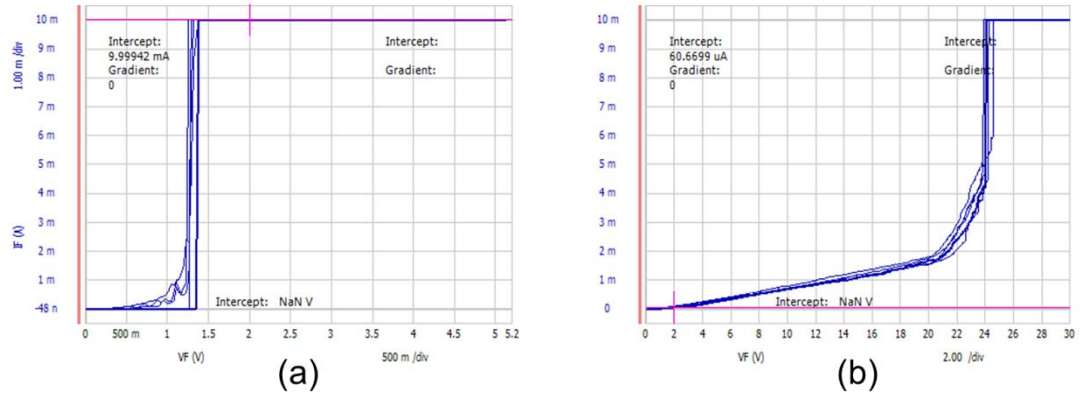


Fig. 5.9. Breakdown characteristics of (a) N+ InSb layer surface and (b) undoped GaSb buffer layer surface, obtained at various position of the sample using the simplified probe-station based material characterization method.

Besides, as discussed in Sec. 4.2.2, the simplified probe-station based material characterisation method was then conducted. As shown in Fig. 5.9, the breakdown

characteristics in various areas of the sample were subject to alinearly increasing bias voltage using two probes. In case there was any InSb material from the N+ layer left, the corresponding breakdown voltage could be as small as ~1.5 V due to the heavy doping. The sample would then be placed back into the etchant for a short additional etching time, followed by the same two-probe breakdown measurement again. These etching and measuring cycles were repeated until the measured breakdown voltages of all unmasked regions showed a value of ~24V, meaning the undoped GaSb buffer layer had been reached and hence that the 2nd mesa etching process was concluded.

As shown in Fig. 5.10, fabrication of the InSb photodiode was completed by deposition of a 400nm thick SiN_x layer. Other than for surface passivation, the deposited SiN_x layer was also patterned to be used as a hard mask for the following etching of the GaSb buffer layer. Moreover, during the dry etching of the SiN_x, via windows were also opened on top of both P and N metal pads of the photodiodes. Patterning of the SiN_x hard mask completed the fabrication of the InSb PDs.

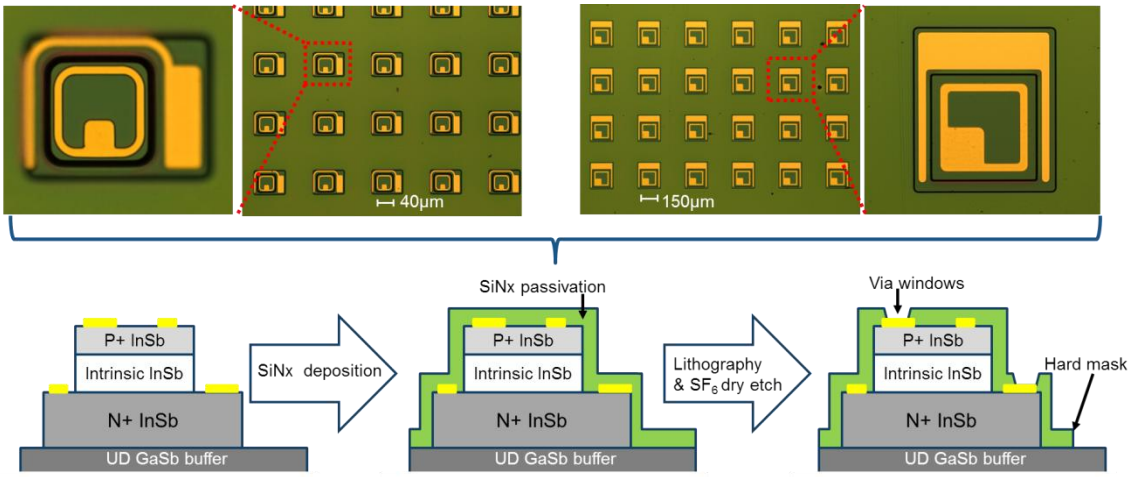


Fig. 5.10. Completion of photodiode fabrication by SiN_xpassivation followed by via windows opening and mask patterning for the following buffer etches.

5.2.2 Fabrication of InAsSb Photodetectors

Similar to the processes used to fabricate InSb photodiodes, fabrication of the InAsSb-based nBn photodetectors was also started by conducting the mesa etching steps. As shown in Fig. 5.11, S1818 photoresist mask was firstly patterned onto the sample followed by etching the top n-type InAsSb layer using a 2:1, by volume, citric acid:H_2O_2 etchant. Similarly to GaSb and AlSb, the quaternarymaterial $Ga_{0.9}Al_{0.1}Sb_{0.85}As_{0.15}$ reacts very slowly with the citric acid etchant. Therefore, the first mesa etching was suspended once hitting the barrier layer. The same photoresist mask used for the first wet etching was then hard baked, before a standard resist

developer(Microposit MF319) solution was applied to etch the unmasked GaAlSbAs barrier layer and thus expose the bottom contact layer for further processes. More details about etching of the GaSb-based materials will be provided in the next section. After etching through the GaAlSbAs barrier, the 2:1 citric acid:H_2O_2 etchant could be used again to complete the first mesa etching after approximately 1 µm of the InAsSb material had been removed. Thanks to the material growth exploiting the IMF layer, the etched mesa height was much smaller compared to that obtained for the InSb photodiodes, leading to a much smaller sample non-planarity. As a result, both the Top and the Bottom Ohmic N contacts of the nBn photodetectors could be formed simultaneously by metallisation and lift-off through a bi-layer of LOR10A+PMMA. The metal stack chosen for the nBn devices consisted of Ti 50 nm/Au 150 nm.Another photolithography stage was used to define the pattern for the second mesa etching, carried out using the 2:1 citric acid:H_2O_2etchantuntil the GaSb buffer was eventually reached. The fabricated nBn photodetectors were also passivated with a 400nm thick ICP-deposited SiN_x layer, and also had via windows opened through low damage SiN_x dry etchingon top of the P and N contacts metal pads, which completed the InAsSb diodes fabrication.

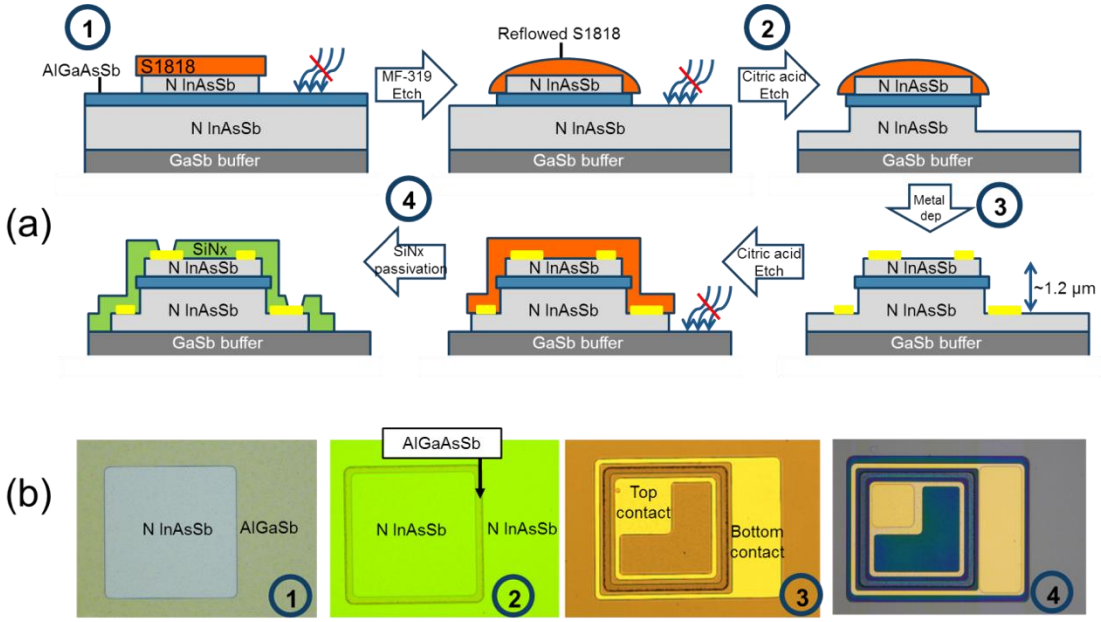


Fig. 5.11. (a) Main process flow for fabrication of InAsSb nBn photodetector and (b) micrographs of a 200 µm×200 µm device took after corresponding steps applied.

5.3 Etching of Buffer Layers

After completion of the photodetectors fabrication (either InSb- or InAsSb-based), the exposed buffer layers have to be removed in order to reach the underlying GaAs active layers and start the fabrication of the MESFETs. Depending on small changes in the layer structure between the wafers used in this project, buffer layers made by combination of undoped GaSb and undoped GaAs or n-type doped GaSb were etched in this step.

5.3.1 Etchingof GaSb Buffer Layers

Although designed to be safe on most semiconductormaterials (e.g. Si, GaAs), the most common photoresist developers such as Microposit MF-319are based on tetra-methyl ammonium hydroxide (TMAH),which etches some antimonide materials such as GaSb, AlSb and their ternary or quaternary compounds [181]. This implies that it is possible to achieve selective removal of GaSb buffer layers without chemically attacking the underlying GaAs active layers.

Using the previously patterned SiN_x passivation layer as a mask,the sample with photodiodes fabricated was immersed in a beaker of MF-319. The beaker was then placed into the water bath equipment since mechanicalagitation of the solution was found to benecessary for activating the etching. An etch rate of approximately 5-10nm/min was obtained when etching GaSb at room temperature. More importantly, with negligible attack to GaAs, etching of the GaSb buffer layer could be terminated automatically with perfect uniformity and hence result in an extremely smooth etched surface as shown in Fig. 5.12. Following etch of the GaSb layers, fabrication of the MESFETs couldstart with an as-grown GaAs surface condition which has never been reported in any other similar III-V material based monolithic integration attempts before [155, 156].

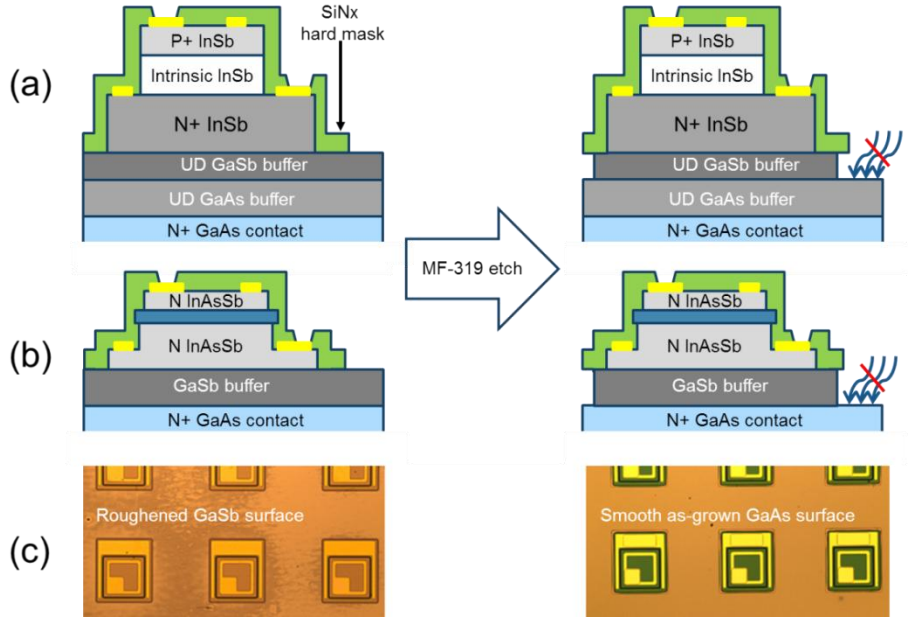


Fig.5.12. Selective wet etching of GaSb buffer layer using MF-319 in (a) InSb based layer structure (b) InAsSb based layer structure. (c) Corresponding micrographs which showthe uniform exposure of underlying GaAs layers with as-grown surface smoothness.

5.3.2 Etchingof GaAs Buffer Layers

In the InSb based layer structures, there was also a 500 nm thick undoped GaAs layer between the GaSb buffer layer and the GaAs N+ contact layer, requiring removal. For this purpose, anorthophosphoric acid:H_2O_2:H_2Osolution (3:1:50 by volume) was used.The reason for choosing this etchant will be detailed in a subsequent section. Since GaAs etch rates for this etchant varied widely (from 80 nm/min to 120 nm/min) in different tests, an iterative approach was needed. As shown in Fig. 5.13, after each etch etching cycle, the two-probe breakdown check method was usedat various positions on the sample. Due to different doping levels between the bufferand the N+ contact layer, adecrease in breakdown voltage was observed as the etch approached the target stop layer. The etching and breakdown checks cyclecontinued until a breakdown voltage between 5 and 8 V was measured at all positions, indicating that the GaAs contact layer with $N_D = 2 \times 10^{18}$ cm^{-3}had been reached.

Despite the possibility of controlling the GaAs buffer etch in order to precisely land on the N+ contact layer, ensuring a good uniformity with such a number of etch cycles could become very challenging especially when a big array of pixel devices covering a wide area of the sample is targeted. The undoped GaAs buffer layer will be deleted from future layer structure designs, as it has been done in the InAsSb based

layer structures. The absence of the GaAs buffer simplifies the fabrication flow as the N+ contact layer can be uniformly exposed right after etching the GaSb buffer layer.

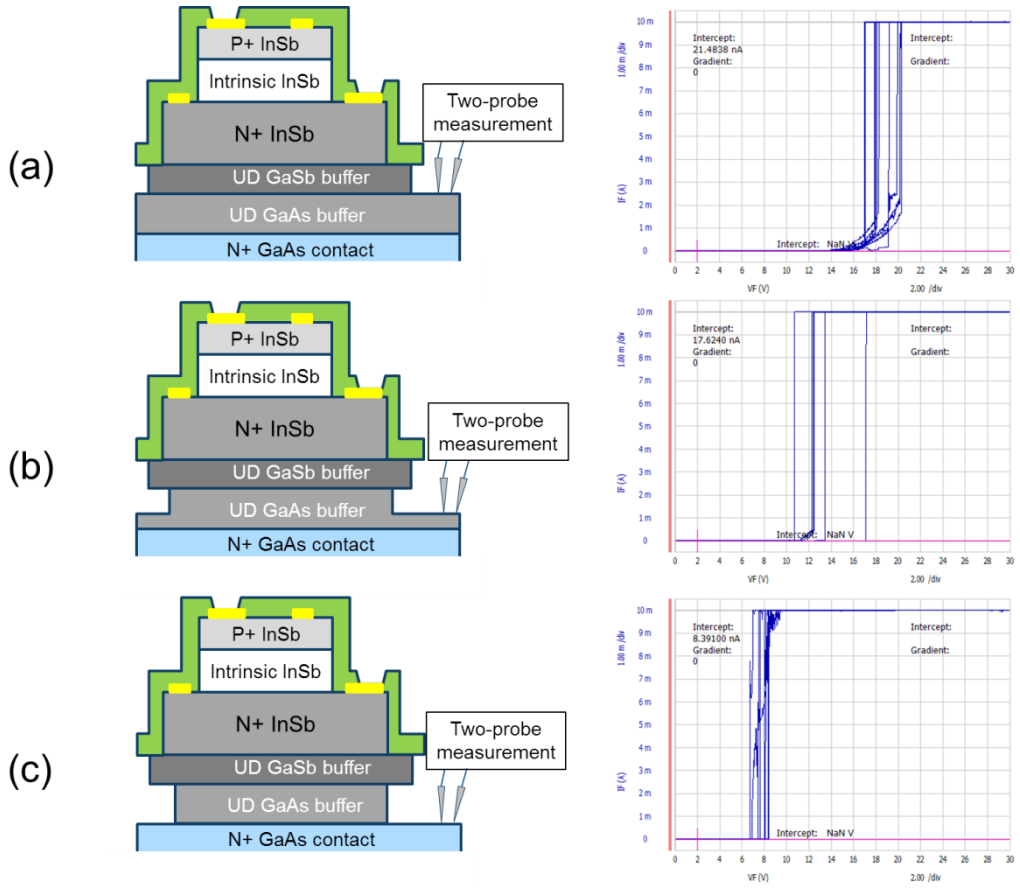


Fig. 5.13. Iterative etching of the un-doped GaAs buffer layer with the aid of the simplified material characterisation method.

5.4 Fabrication of the GaAs MESFET

Fabrication of MESFETs was conducted once exposure of the GaAs active layers was achieved through buffer layer etching. Currently, there are no existing reports of fabrication of GaAs MESFETs andAntimonide-based photodetectors side-by-side. Several challengesmust be overcome to make such a device system possible, with challenges arising from various aspects,e.g. material etching and Ohmic contact formation. This section will detail the special processes developed in this work to solve these integration challenges.

5.4.1 Isolation Etching

Isolation etching is the first step of MESFETs fabrication, in which the unmasked GaAs active layerswere etched until reaching the S-I GaAs substrate. After conducting this etching, electrical isolation of individual devices from each other can be realized accordingly as shown in Fig. 5.14.

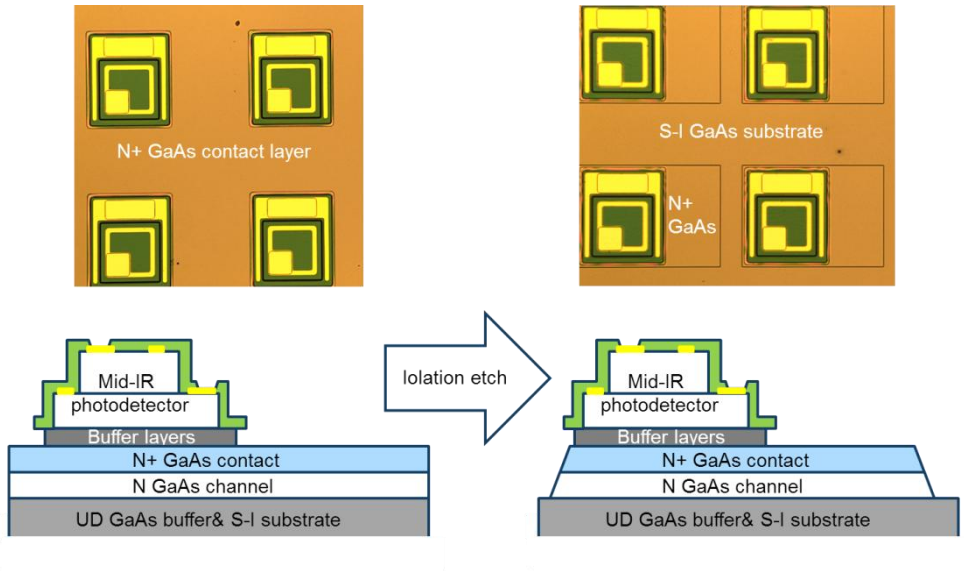


Fig. 5.14. Isolation etching process applied to separate individual devices from each other. The inset micrographs show the top-view of the devices at the corresponding step

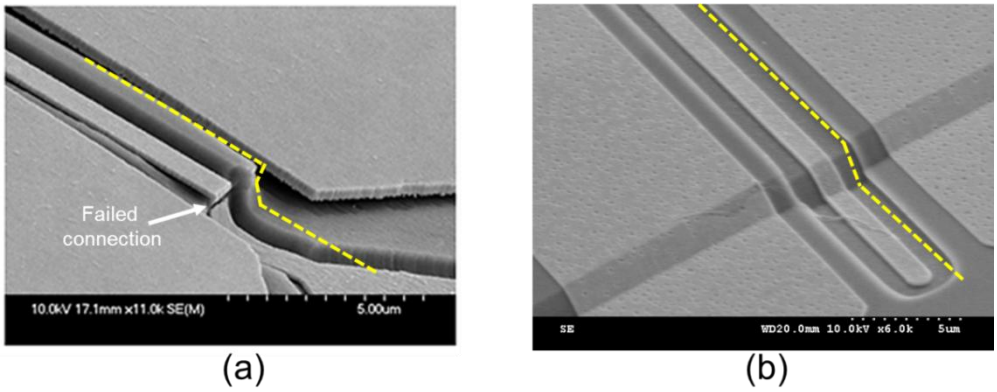


Fig. 5.15. Evaporated Gate pad on top of isolation mesas with (a) undercut sidewall profile and (b) positively sloped sidewall profile.

Especially for this work, a GaAs etching process which can produce positively sloped sidewall profile and present no obviouscrystallographic dependence is highly desirable. The main reason is that a thin layer of metal on top of the etched GaAs surface will form the Schottky gate electrode, and it will have to cover the mesa steps without breaking. As shown in Fig. 5.15, if etching of the isolation layer created a sidewall with vertical or undercut profile, the deposited gate metal pad could easily crack when brought across the corresponding mesa edges. This would result in losing gate control of the MESFET at the end of the fabrication. Also if the obtained etching profile varied greatly according to the crystal direction, the designed devices layout would be significantly restricted to guarantee the gate metal would only cover mesa edges where sloped sidewall profiles can be created.

In order to etch GaAs layers, there are a number of existing wet chemicaletchants with various mixture ratios available for use. These includesulphuric acid,citric acid,phosphoric acid, ammonia hydroxide and so on. Among them, the phosphoric acid

based etchants are especially usefulwith the advantage of producing very smooth surfaces and highly controlled etch depth down to the angstrom level [158]. Furthermore, with proper mixture ratio applied, theH_3PO_4:H_2O_2:H_2Oetchant system has been reported to produce almost identical etching rate for most of the GaAs crystal directions [182] which is a fundamental requirement for achieving crystallographic independent etching. Based on this etchant system, an isolation etching process was successfully developed. For device fabrication, the sample was firstly masked using S1818 photoresist patterned by photolithography. The sample was then placed into abeaker of freshly prepared H_3PO_4:H_2O_2:H_2Oetchant (3:1:50 in volume) without agitation until the estimated etching time to reach the S-I substrate elapsed. As shown in Fig. 5.16, this process resulted in a sloped sidewall profile independent of the crystal orioentation. The reason for obtaining a profile with sloped sidewalls is still unsure and needs further investigation. However, a test sample etched in the same etchant with manual agitation showed a very obvious lateral undercut of the sidewall profile, indicating that minimising agitation or stirring is critical to this etching step.

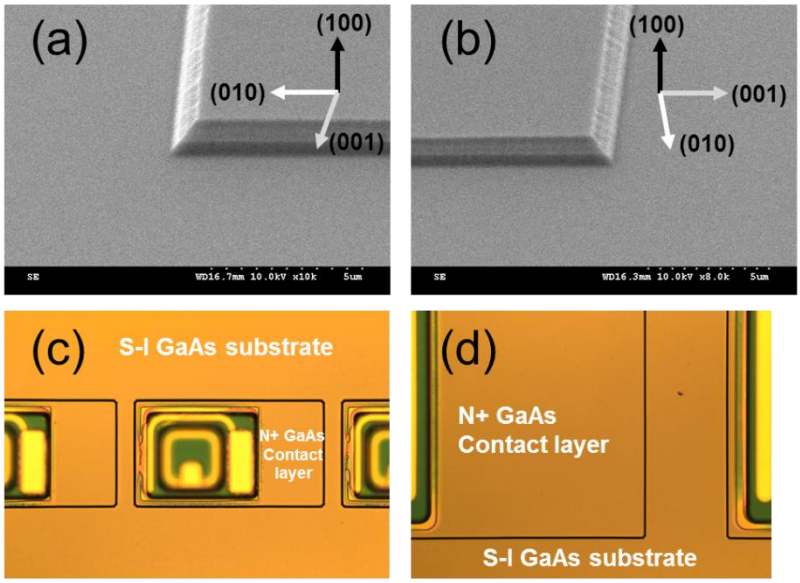


Fig. 5.16. (a) (b) Positively sloped sidewall profile obtained independentlyof the GaAs crystal direction. (c) (d) Zoomed-in micrographs showing the etched mesa edges.

5.4.2 Low Temperature Annealed Ohmic Contact

Having achieved the device isolation, it was then necessary to form Ohmic contacts onto the etched GaAs mesas. As summarised in Table 5.1, most of the metallisation systems used to form Ohmic contacts on GaAs require high temperature annealing (up to ~400 ˚C) to produce good contact resistivity for making electronic circuits. However, since the photodiodes have already been fabricated on the sample surface at this stage, it is crucial to conduct all of the following process steps without

exceeding a temperature of approximately 200 ˚C, point at which antimony desorption begins to happen [183, 184]. If the sample is subject to higher temperatures, elemental antimony will surface on the sidewalls of the photodiodes and act as a low-resistance path for leakage current, leading to a degraded detection performance.

Table5.1. Summary of Ohmic Contact Data

Metallization	Anneal Temp (℃)	Resistivity (Ω cm^2)	Ref
Ni/AuGe	>360	$<1 \times 10^{-6}$	[185]
Ge/Ni/Al	500	1.4×10^{-6}	[186]
Cu/Ge	400	6.5×10^{-7}	[187]
Pd/Ge	250-325	0.8×10^{-6}	[188]
Pd/Ge/Au	150-175	1×10^{-6}	[189]

5.4.2.1 Pd/Ge/Au Metallisation system

So far, Pd/Ge/Au is the only metallisation system reportedly being able to achieve good Ohmic behaviourwith an annealing temperature below 200℃. As shown in Fig. 5.17, rather than alloying, the key mechanism for this metal system to form Ohmic contacts is the so called solid phase regrowth at the contact interface of a heavily Ge-doped GaAs layer with N_d>2×10^{19} cm^{-3} [189]. With such a high doping level, the deposited metal can readily form Ohmic contact by the tunnelling mechanism as mentioned in Sec. 3.2.1. Interdiffusion of Ge and Au layers is another important mechanism that accrodingly contributes to the overall reduction in resistance. As a result, the success of this low annealing temperature process dramatically relies on the GaAs surface condition prepared before deposition, and on the thicknesses of each metal layer.

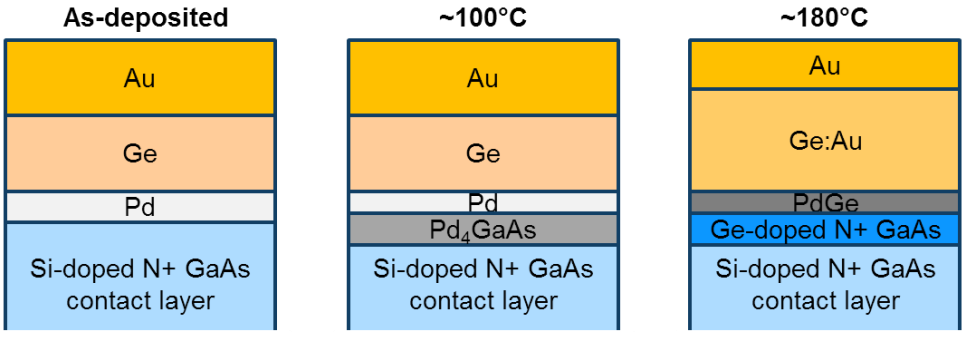


Fig. 5.17. Low temperature Ohmic contact formation mechanism using the Pd/Ge/Au metallisation system.

A set of GaAs samples with highly n-type doped cap layer (N_d=~2×10^{18} cm^{-3}) wasthen prepared for testing. They were all initially cleaned using SVC-14 pre-warmed at 50 ℃, followed by acetone, IPA, and a final rinse under running DI water.After the CTLM patterns were defined bylithography and lift-off processes, the samples were annealed in a 180 ℃conventional oven and in standard atmosphere for 1hr followed by specific resistivity measurements with the probe-station (see Sec. 4.2.3 for more details on the characterisation technique).The results obtained from the testing samples were used to identify the optimised surface preparation steps prior to metal evaporation, that include: (1) a short time,low power O_2 plasma ash, (2) removal of native oxide by dipping the samples into HCl: H_2O solution(1:1 by volume), (3) load the sample in to the evaporation chamber as quick as possible after de-oxide. As for the optimised metallisation thickness, thePd(10 nm)/Ge(40 nm)/ Au(100 nm) stack presented a good Ohmic behaviour with the lowest contact resistivity(~2×10^{-6} Ω cm^2), the value of which is in good agreement with the results obtained in other work [189, 190], and thus confirms the effectiveness of the process.

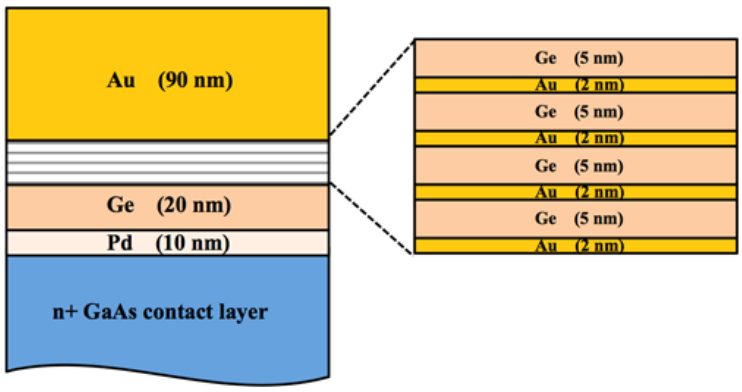


Fig. 5.18. A schematic diagram of the metallisation system used for Ohmic contact formation. The diagram on the right is an expanded view of the Au/Ge stack that was incorporated.

In order to further reduce the contact resistivity and annealing temperature, a superlattice-like Au/Ge layer structure was introduced in place ofthe standard Ge/Au metal stack following Pd in the evaporation (see Fig. 5.18). In this new metal contact structure, the interdiffusion of Au and Ge can be controlled more precisely by assigning a certain thickness of Ge layer especially for regrowth of the heavily doped GaAs while using other multiple Ge thin layers for reacting with Au. When comparing standard Pd/Ge/Au contacts with the ones based on the superlattice-like layers for the same total metal thickness and using the same evaporator, an improvement in contact resistivity with factor of 1.5 to 2 can be observed. With the optimised metal thickness, as shown in Fig. 5.18, a resistivityvalue as small as 1.2×10^{-6} Ω cm^2 was achieved. Furthermore, even

bringing the annealing temperature down to 120 ℃ was stillfound to produce good Ohmic behaviour with resistivityin the order of $10^{-6}\ \Omega\ cm^2$, although with a much longer annealing time required (up to 50hrs). Again, the resistivity of contacts based on superlattice-like layers was found to be smaller as compared to standard stack after such long annealing time.

5.4.2.1 Contact Formation on Actual Devices

In actual device fabrication, as shown in Fig. 5.19, the patterns for the Source and Drain of the MESFET devices were firstly defined onto the sample using a bi-layer of LOR+PMMA resists. After conducting the above-mentioned surface preparation steps,the superlattice-like Ohmic contact structure was depositedand the source and drain contacts to the MESFET were then formed by lift-off. However, differently from the testing samples, in the actual device fabrication flow annealing was not required immediately after metallisation, as it could be incorporated into the later resist preparation steps used for making the Schottky gate. This process will be detailed in the subsequent section.

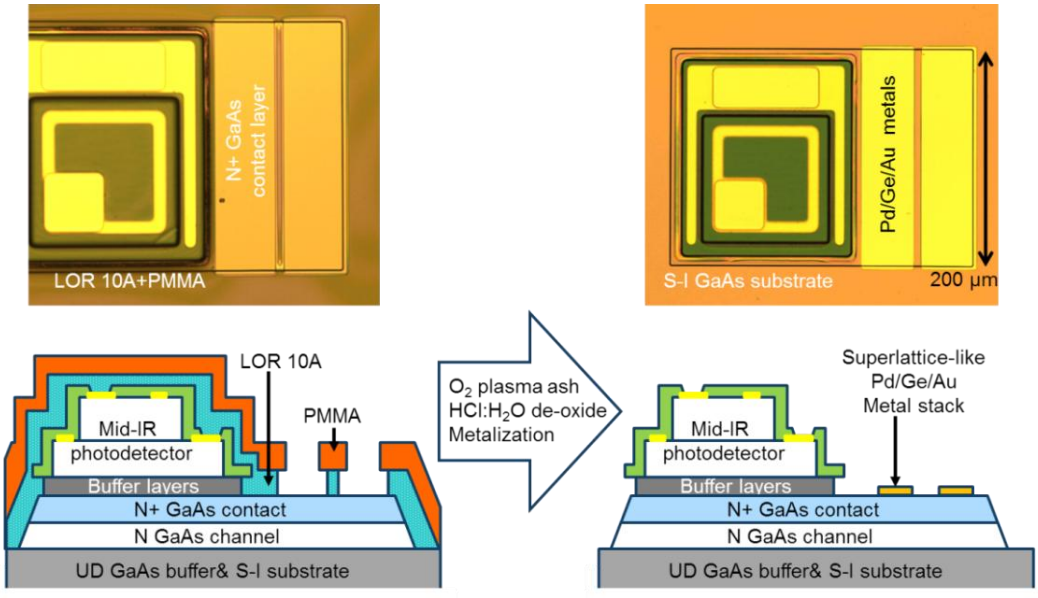


Fig. 5.19. Pd/Ge/Au based Ohmic contact deposition to form the Drain and Source contacts of the MESFET devices.

5.4.3 Schottky Gate Formation

Gate formation is commonly regarded as the most critical step and also the last step for making a GaAs MESFET device. Once the gate is formed on top of the channel layer, the MESFET device will be ready to be tested. As discussed in Sec. 3.2.2, the behaviour of the gate Schottky contact will directly decide the performance of

fabricated MESFET by affecting the ON/OFF resistance, leakagecurrent and switching speed of the devices. This section will present the optimised gate formation process steps used in this work to achieve the desired MESFET characteristics with high yield and high uniformity.

When fabricating MESFET based on MBE grown active layers, in which the n-type channel layer is capped by the highly doped contact layer, a recess etching process is thus needed prior to Gate metal deposition. As shown in Fig. 5.20, the etch mask consisted ofa bi-layer of LOR 10A+PMMA resists. While preparing the mask, the pre-baking of the LOR 10A resist also served the purpose of annealing the above-mentioned Pd/Ge/Au Ohmic contacts, since both processes required180 ℃ oven baking for more than 1hr. The MESFET gate pattern was then written usingEBL followed bytwo development stages: standard MIBK:IPA for the PMMA and then MF-319 for the LOR 10A. Afterwards, recess etching was carried outusing a 20:1, by volume, $C_6H_8O_7$: H_2O_2etchant.

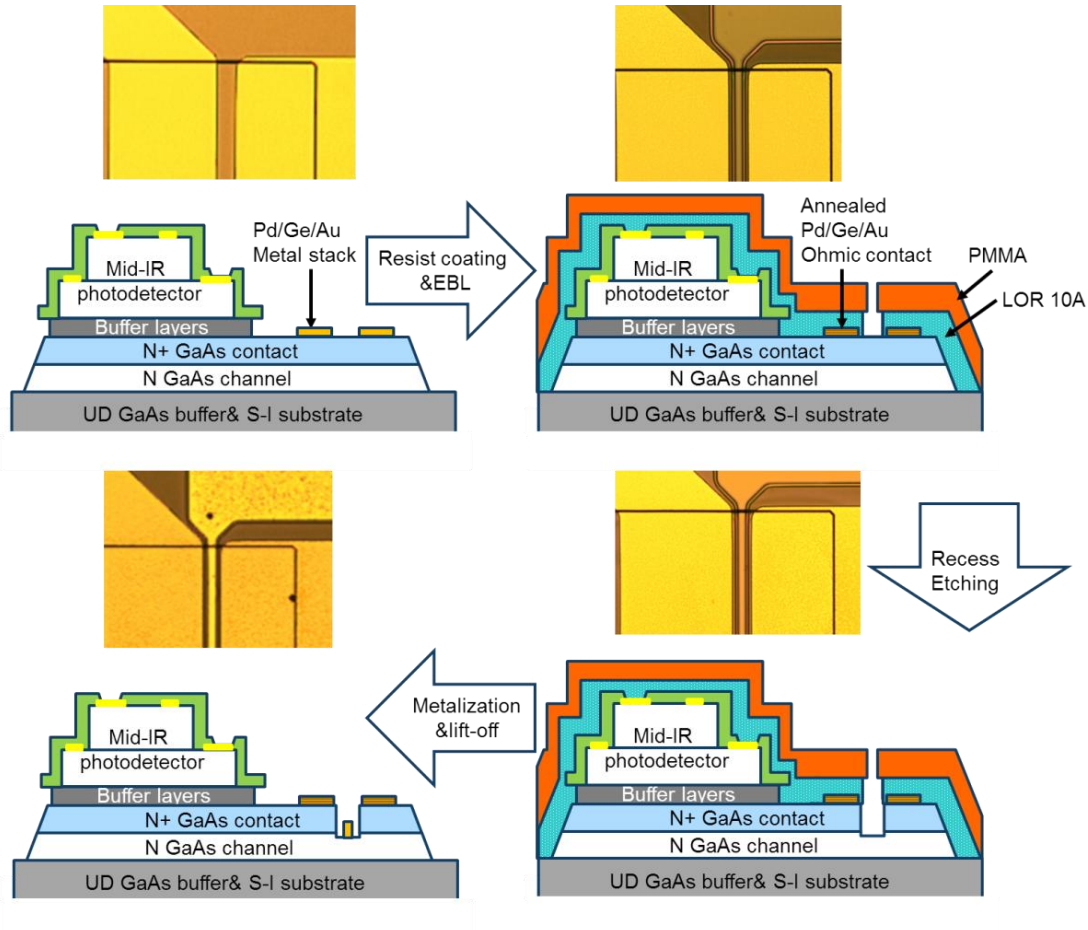


Fig. 5.20. Illustration of the LOR/PMMA gate recess resist, etch and self-aligned metallization technology.

Since the recess etch requires precision in order to land on the channel layer without excess over-etching, an iterative etchingapproach was used which gives an etch rate of 80 to 100nm/min. After each etching iteration, the current flow through drain and source pads was monitored using a probe station. As shown in Fig.5.21, if there was still considerable amount of highly doped contact layer capping on the channel layer, the obtained I-V characteristicsshowed no obvious saturation behaviour. When approaching the channel layer, currentsaturation started to be observed. Then, etching iteration was continued but with gradually reduced etching time until the measured saturation current reached 30-40 mA at drain-source bias V_{ds} = 3 V (Eqn. 3.13), at whichit was determined that the contact layer was removed totally. This value also implies the resistance of the obtained transistor devices would have a ~50ΩON-state resistance accordingly.

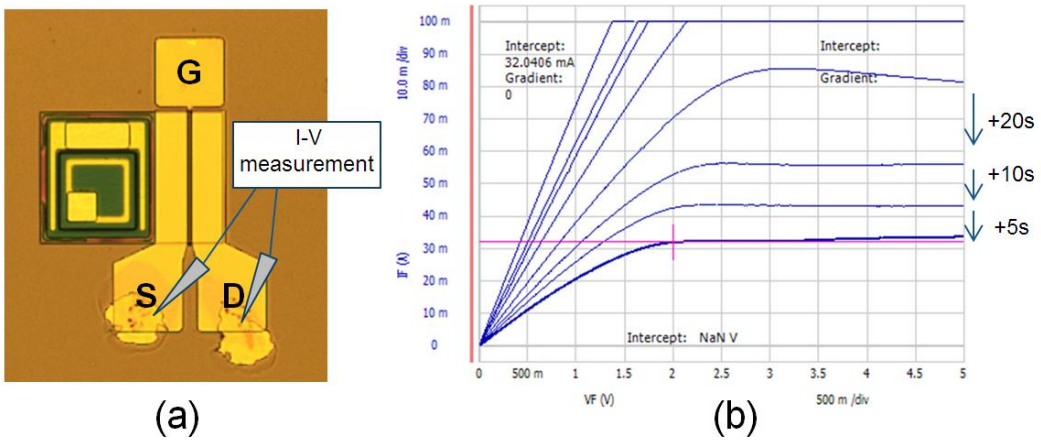


Fig. 5.21. (a) A micrograph of a test device with expanded Drain and Source pads for monitoring saturation current during recess etching. (b) Measured Drain-Source I-V characteristics using the iterative etching approach.

Finally, since the bi-layer LOR/PMMA mask can also be used for lift-off, a self-aligned gate pad can be realised without the need for another lithography stage.20 nm of Ti, 30 nmPt and 150 nm Au werethen evaporated on the sample, followed by lift-off in warm SVC-14solvent to form the Schottky gate of the MESFET. Fig. 5.22 shows the SEM pictures of the fabricated MESFET part in a typical pixel device used in this work. The MESFET gate dimensions were 3 µm long by 100 µm wide.

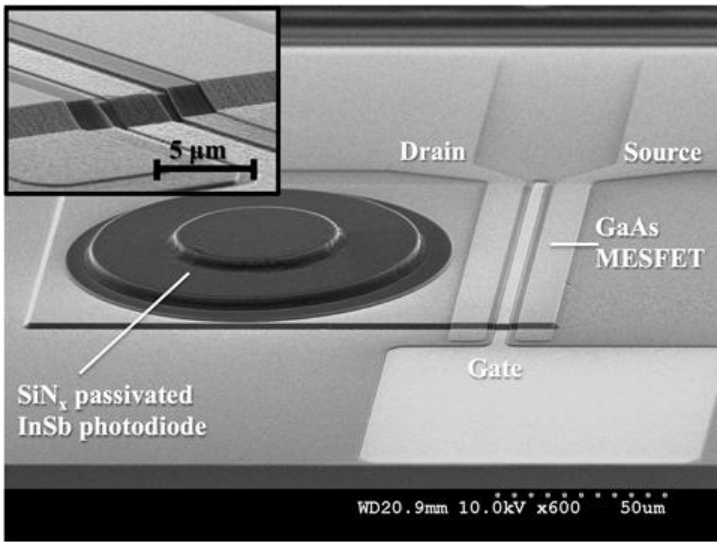


Fig. 5.22. A scanning electron micrograph of the fabricated MESFET with 3 μm gate length and 100 μm gate width.

A good etch depth uniformity is always desired when recess etching is carried out, so that a large number of MESFET devices with high yield and nearly identical characteristics can be produced. This is especially important when fabricating FPA devices, in which all pixelsshould ideally have identical photoresponse. To achieve a uniform etch depth, the most common method is to ensure etching of the unmasked area is selectively terminated by an etch stop layer once the desired depth is reached.However, in a standard MESFET layer structure which only contains GaAs active layers, selective etching is not applicable. As a result, a special surface activation process based on a surface wetting agent (DECON-90) was developed to ensure the etching process would start simultaneously in various regions of the sample, thus improving uniformity. A set of solutions was prepared in advance: (1) a beaker of DI water (100ml) with a drop (0.1 ml) of DECON-90added; (2) a beaker of citric acid: H_2O de-oxide solution (100ml) with a drop (0.1ml) of DECON-90 added; (3) a beaker of 20:1, by volume, citric acid:H_2O_2 etchant;and (4) a beaker of DI water. The sample was then dipped into the solutions in turns without exposing the surface to air. The beakers, in the numbered order, served the purposed of: (1)surface activation; (2) native oxide removal; (3) material etching; and (4) rinsing. In case aniterative etching was applied, the same soaking sequence was repeated for each cycle before the desired saturation current was reached. As shown in Fig. 5.23, an obviously improved etching uniformity was confirmed by measurements of the saturation current of several test devices right after the recess etching process.

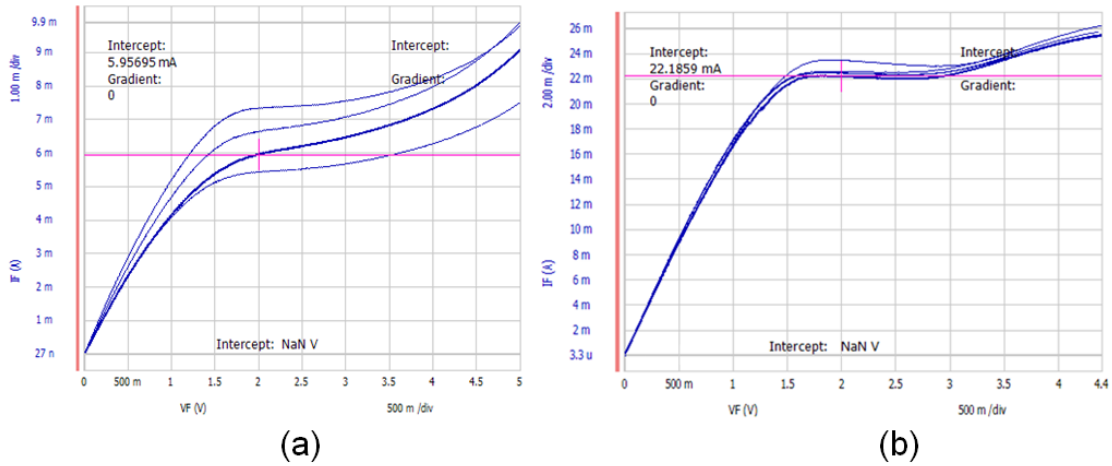


Fig. 5.23. Saturation Drain-Source current measured from five test devices positioned at various regions of the sample, without (a) and with (b) surface activation process applied.

5.5 Interconnections

With both the MESFET and photodiode completed, the final fabrication stage was formation of interconnects between these two componentstorealisethe switchable photo-pixeldescribed in Sec. 3.4. Given the extreme nonplanarity created afterthe numerous mesa etching steps previously mentioned, the interconnection metal could easily break if direct deposition is attempted. As shown in Fig. 5.24, even with more than 600 nm metal evaporated on to the sample surface, interconnectionsbetween devices still failed at the mesa edge due to the near vertical sidewall profile and the step height, in total up to 6 µm. This problem will escalatewhen alarge format array of devices is targeted, given the large number of interconnections and the multiple metal layers needed.

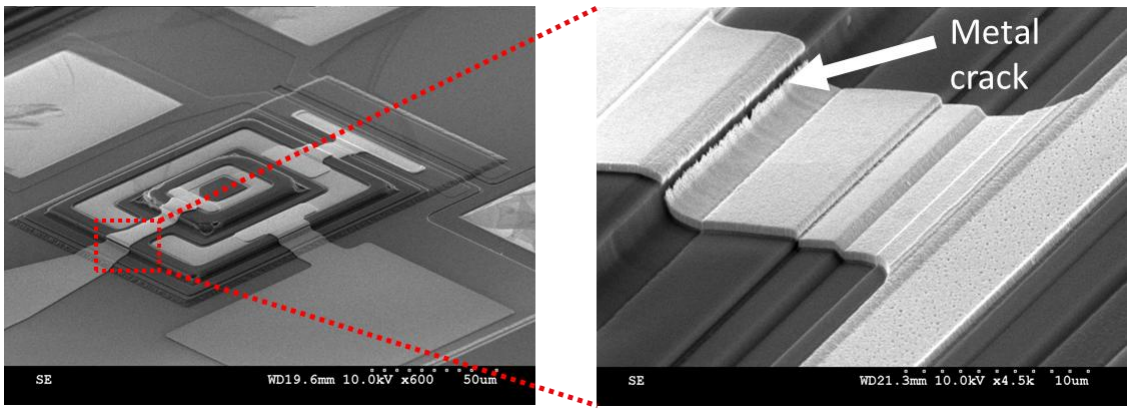


Fig. 5.24. Failed metal interconnection due to etch step height up to 6 µm

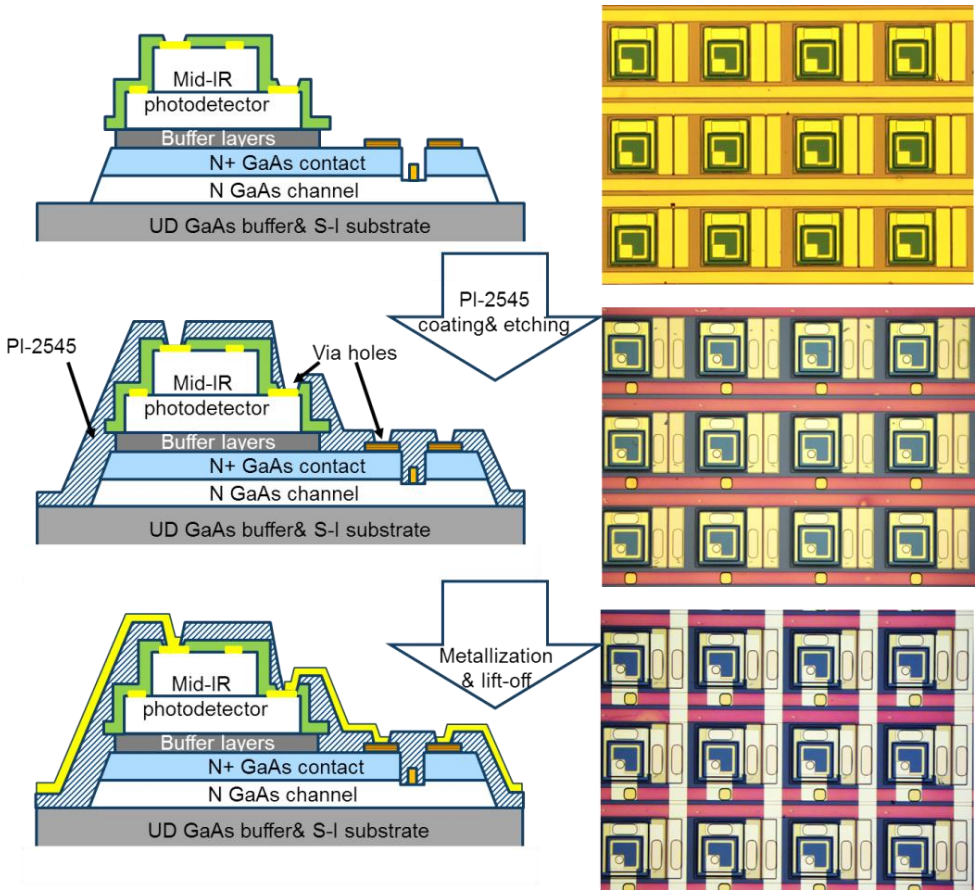


Fig. 5.25. Illustration of the polyimide based planarization process flow.

As shown in Fig. 5.25, an intermediate step based on polyimide was developed to solve this problem, since it could provide a planarising section between the lower MESFET and upper photodiode regions of the device so that the interconnection metals can cross the mesa steps without cracking.Firstly, a 2 μm thick film of Dupont PI-2545 polyimide was spin-cast on to the sample, followed by baking for 6 minutes on a hotplate set at 150˚C. This temperature was chosen to partially cure the polyimide layer and provide a continuous gentle ramping region at the etch mesa step edges. A bi-layer of PMMA (15%+2.5%) was then coated and each layer was baked for 7 minutes on the 150˚C hotplate as well, which also contributes to curing of the underlying polyimide. Then, a pattern was defined in the PMMA resist, to be used as a mask for opening via holes through the polyimide where interconnections were required. Since the polyimide was only partially cured with 150˚C baking, standard photoresist developer MF-319 could readily be used as an etchant to remove unmasked polyimide layer [191]. By carefully controlling the etching time, via holes with sizes as small as 10 μm diameters were successfully opened. More importantly, the etched via holes have positively sloped sidewall profile in all directionswhich is ideal for interconnection metals to straggle. After stripping the PMMA resist, the sample was further oven-baked at 180 ˚C for 2 hours in order to fully cure the polyimide and further smooth the etched via hole edges.

Once this planarization process was applied, a 200nm thick Ti/Au metal can easily be used to form the interconnections in between devices without breaking (see Fig. 5.26).

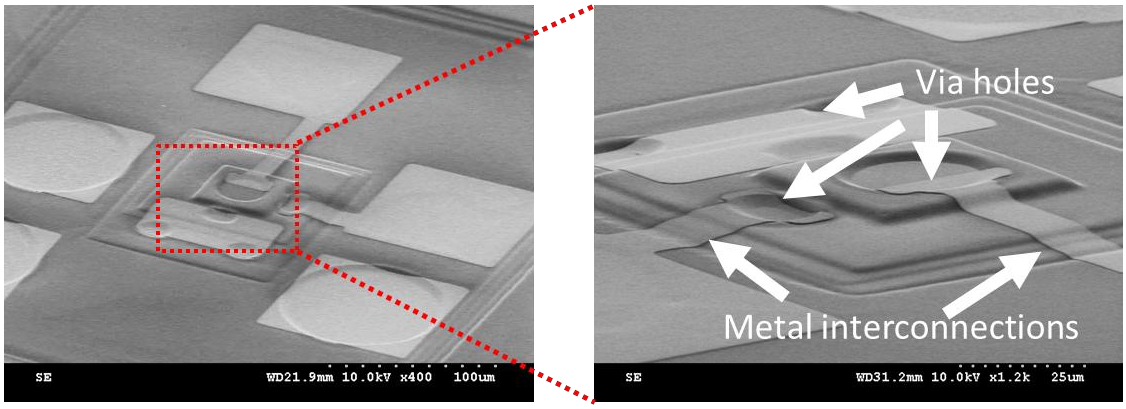


Fig. 5.26 **.** Interconnected devices with polyimide smoothing section applied

5.6 Dry Etch Processes for Scaling

Besides the aforementioned processes, dry etch processes were also developed, aiming to eliminate well-known wet etching problems such aspoor reproducibility due to the variation of sample surface conditionand galvanic corrosion issues [192]. A switch to more consistent and reliable dry etch processes for steps such as photodetector mesa etching and polyimide via holes opening, will simplify fabrication of scaled FPAs with much larger format and smaller pixel pitch than the prototype devices.

5.6.1 Dry Etch of InSb-based materials

Although the citric acid based InSb mesa etching has provided very smooth etched surface and demonstrated automatic etch termination once reaching the GaSb buffer layer, it is still imperfect especially for fabricating large format FPA devices. As shown in Fig. 5.27 (a), this wet solution based isotropic etching process requires very good adhesion of the etching mask to the InSb sample surface, otherwise notching defects will be created in the etched mesas, limiting the minimum achievablepixel pitch.Moreover, the very long etchesrequired in this work can lead to the unexpected exposure of the underlying GaSb layer to the etchant at the position where large threading dislocation defects have been created during MBE growth. As shown in Fig. 5.27 (b), in the worst case, penetration of the GaSb layer will happen which can further create deep trenches into the GaAs active layers and hence hinder MESFET fabrication.

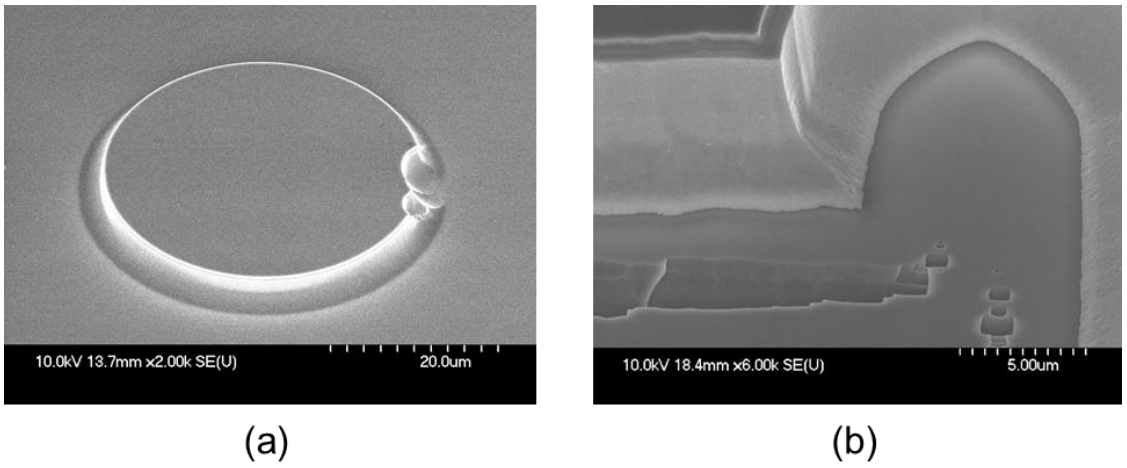


Fig. 5.27. Disadvantages of currently developed citric acid based InSb wet etching process: (a) notching defects created due to partially failed resist adhesion; (b) failed etch stop by GaSb buffer layer which resulted in deep trenches inside GaAs active layers.

In contrast, a dry etching process with balanced physical and chemical reactions can give anisotropic profiles. It can thus be much faster than the citric acid based wet etching and less sensitive to the defect areas on the sample. Dry etching of InSb was previously reported in several publications [193, 194]. In most cases, chlorine-containing compounds such as BCl_3 and Cl_2wereused in an ICP dry etch machine to enhance the chemical reaction and provide maximised etch rate accordingly. However, this will create a large amount of non-volatile indium chloride ($InCl_3$) by-products, which require temperatures in excess of 200 ℃ to be successfully purged. The materials grown in this work cannot withstand such a high temperature due to the potential performance degradation of fabricated devices induced by the antimony desorption phenomena. As a result, a chlorine free gas mixture, $CH_4/H_2/Ar$,was used and a low temperature, low damage dry etch process was developed. Furthermore, two different etch profiles were obtained depending on the type of mask used.

Etch test samples were firstly patterned with two types of masks: (1) photoresist masks based on combination of post-baked Shipley AZ4562 resist and LOR 10A; and (2) hard masks, based on either ICP-depositeded SiN_x or Hydrogen silsesquioxane (HSQ). The samples were then mounted on a 6 inch silicon carrier wafer by thermal grease to ensure a good thermal contact. Irreversible temperature indicators were also placed on the carrier wafer for monitoring the maximum actual temperature reached during the etching process. After loading the sample into the chamber of the ICP 180 tool, a $CH_4/H_2/Ar$ plasma was carried out, withthe followingoptimised parameters: ICP power of 600 W; RF power of 150 W; chamber pressure of 15 mT; and table

temperature of 110 ℃.The DC bias wasapproximately −300 V.Detailed optimization of parameters can be found in Appendix I.

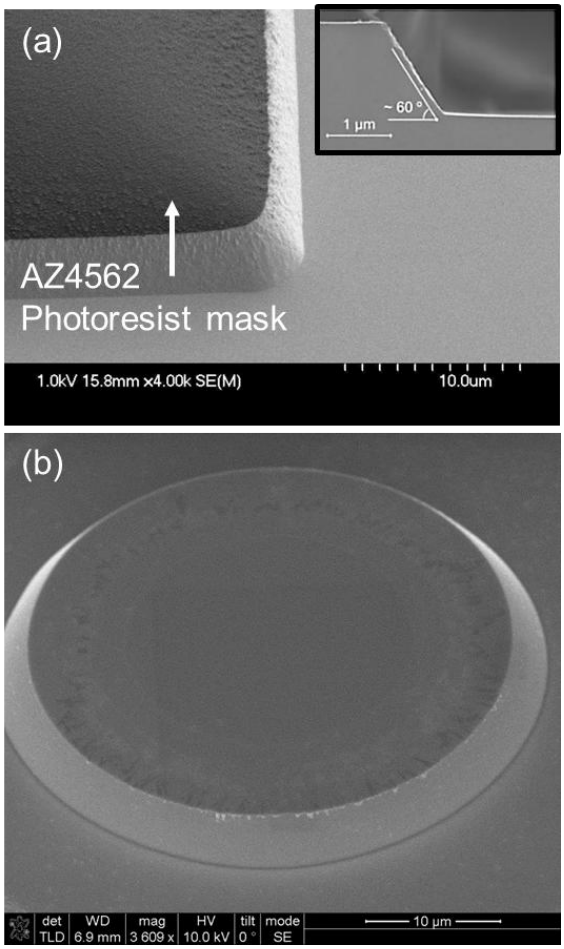


Fig. 5.28. (a) SEM images showing the results of a 90 minsInSb dry etching test using the optimised CH4/H2/Ar gas flow and with AZ4562 mask.(b)A defined photodiode mesa after corresponding process applied.

In case the sample was masked by the post-baked AZ4562 photoresist and a CH_4/H_2/Ar gas flow ratio of 15/50/5 was used, an 80 nm/min average etch rate on InSb was achieved with a selectivity of 2:1.Due to reflow of the photoresist during the post development baking, the AZ4562mask acquired a dome-shaped profile and was gradually eroded by the RF plasma. The erosion of the mask translated into a sloped etch of the InSb as shown in Fig. 5.28. Different from the obtained smooth surface,the maximum sidewall roughness can be as large as 50 nm when estimated from SEM. This isprobably due to a direct transfer of the edge roughness of the photoresist mask used. Fortunately it was found to be avoidable when applied to define circular mesas as shown in Fig.5.28 (b).

After 90 minutes long etching, the temperature indicators showed a temperature of approximately 145 ℃ by the end of the run which is still well tolerated by the material. Nevertheless, since this temperature is close to the glass transition of AZ4562 [195], the

dry etch process is equivalent to a long hard bake process which made the photoresist cross-linked and become extremely difficult to be fully removed after etching. As a result, the mask process was slightly amended to insert a LOR 10A layer between the sample surface and the AZ4562. With a much higher glass transition temperature, the additional LOR 10A layer can effectively help removal of the cross-linked AZ4562 mask even after etching the sample for a long time (see Fig. 5.29).

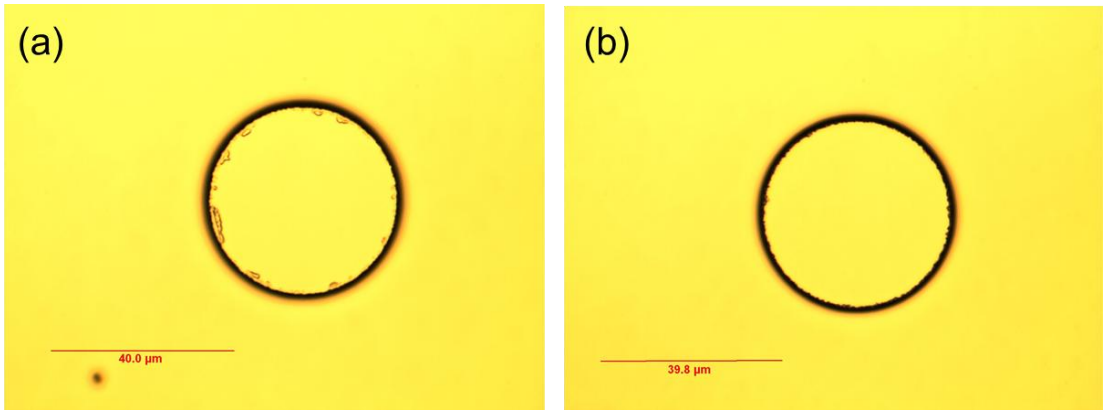


Fig. 5.29. Micrographs comparing resist residues for a (a) AZ4562 only mask and (b) a dual layer of LOR 10A and AZ4562.

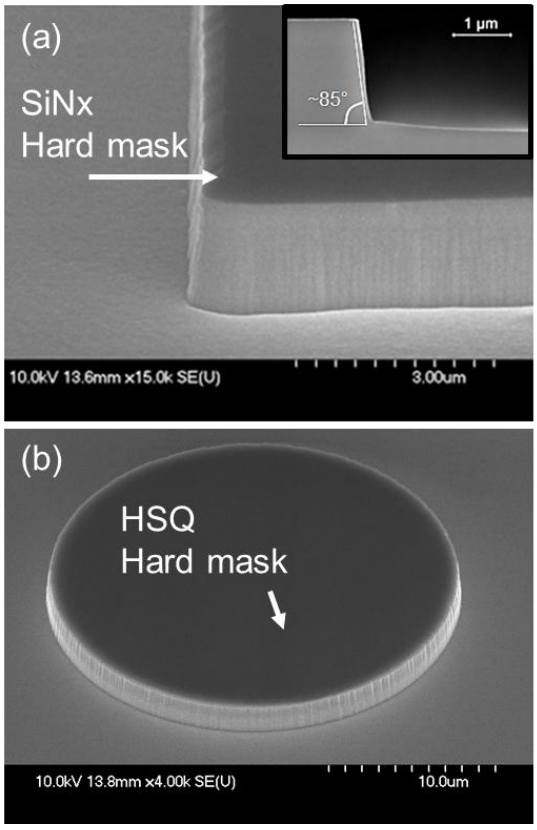


Fig. 5.30. (a) SEM images of test samples etched with a SiN_x hard mask.(b) A defined photodiode mesa after corresponding process applied.

The dry etch showed different results when hard masks were used.In this case, adilutedCH$_4$/H$_2$/Ar gas flow ratio of 9/36/3 was found to yield the best results. Using this chemistry on samples with a SiN$_x$ hard mask,the etch rate was significantly reduced to approximately 50nm/min while the selectivity was approximately 5:1. The process, however, provideda nearly vertical sidewall profile (approximately 85 degrees) and hence anisotropic etching of InSb could be achieved. More importantly, as shown in Fig. 5.30, the use of hard mask resulted in very smooth sidewall profile which further suggested that that the etch roughness observed for the AZ4562 resist was due to the mask roughness.Additionally, hard baked HSQ resist can also demonstrate very similar etching results and has the advantage of very high pattern resolution. After etching the hard masks can be removed easily with one of the well-established RIE dry etching recipes available in JWNC (e.g. SF$_6$ for SiN$_x$).

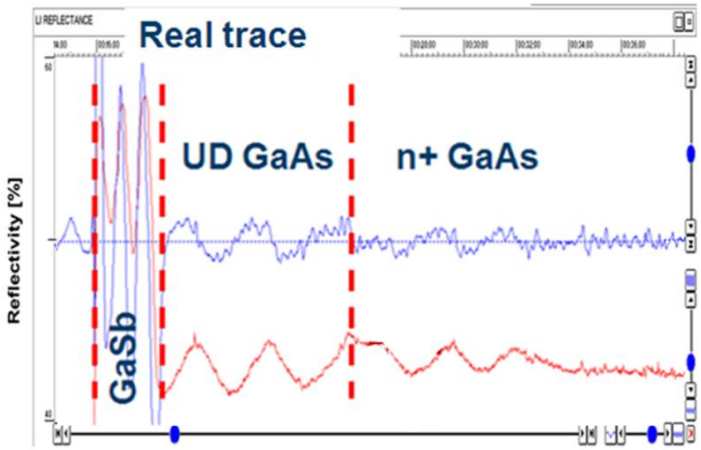


Fig. 5.31. Screenshot of the interferometer traces obtained during the actual etching foretch depth control.

The developed dry etching process was then applied in the second mesa etching for fabricating InSb photodiodes. Despite the process etching nonselectively through InSb and GaAs, changes in the interferometer trace can be clearly mapped to corresponding epi-layers, and the etching process can be terminated precisely when hitting the GaSb buffer layer. Furthermore, the developed dry etch does not display a different behaviour at threading dislocations or defect areas, hence providing increased yield of MESFET fabrication.

5.6.2 Dry Etch of Polyimide Via Holes

In order to form interconnections between the fabricated devices, via holes have to be opened through the spin-cast polyimide layer after the surface planarisation process. However, the current MF-319 based wet etching of polyimide becomes problematic

especially when scaling down the active sensing area of each pixel. The much longer etching time needed to create via holes to access the lower MESFETs can lead to significant over-etching of the polyimide layer coated on top of the upper photodiode mesas. Fig. 5.32 shows the first attempt to open via holes when fabricating a 16x8 array device with 45 μm×45 μm sensing area for each photodiode. After the bottom via holes were created, the mesa edges of the photodiode were already exposed and thus could no longer provide the smoothing section for making interconnections.

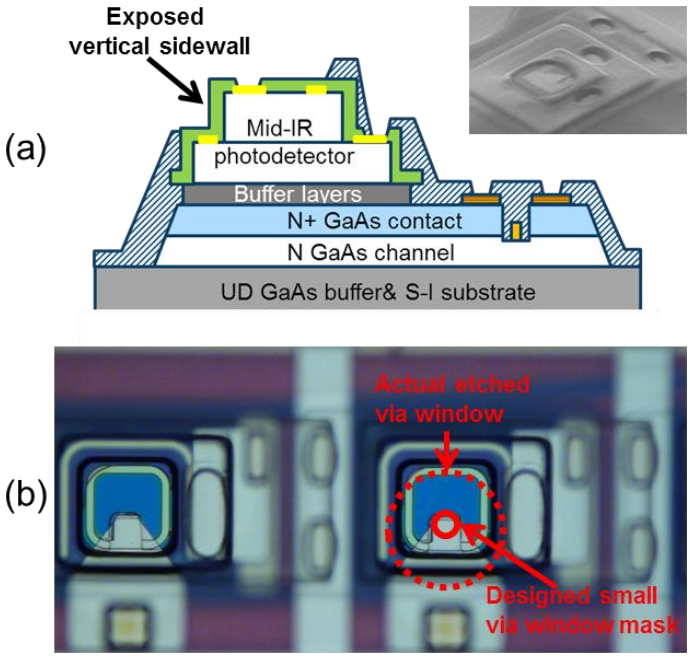


Fig. 5.32. (a) Cross-section and (b) micrograph showing the exposed vertical sidewall when using MF-319 to wet etch the polyimide layer simultaneously on top and at bottom of a 40 μm×40 μm photodiode mesa.

Opening via windows separately may be applicable to solve this problem,but at the expense of fabrication complexity. A polyimide dry etch process was then tested. The sample coated with polyimide was first fully cured at 180 ℃ for 2hrs, followed by definition of the via holes pattern into a bi-layer of S1818 using photolithography. Following development, the S1818 mask was reflowed through a hard bake at 120 ℃ in a conventional oven for 15 minutes. Finally the sample was etched by CF_4/O_2 plasma inside a RIE machine which gave an etch rate of approximately 240 nm/min. As shown in Fig. 5.33, via holes as small as 8 μm diameter could be opened on top of a circular photodiode with 40 μm diameter. Furthermore, the etched via holes present perfectly sloped side wall profilesextremely suitable for evaporating metals to form interconnections.

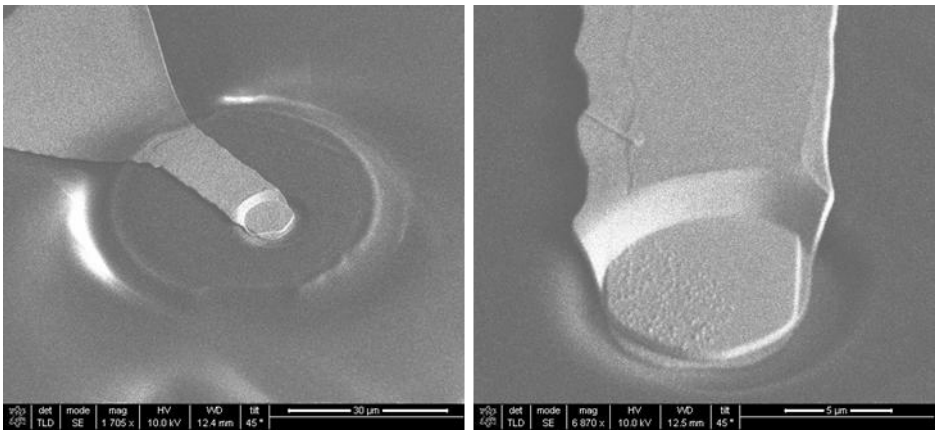


Fig. 5.33. SEM images of a dry etch defined polyimide via window on top of a circular photodiode with 40 μm diameter.

5.7 Summary

In this chapter, after detailing the MBE grown layer structures used in this work, the entire process flow for fabricating both the switchable pixels and FPA devices has been described. The whole fabrication process involves four main stages, to make mid-IR photodetectors and GaAs MESFETs side-by-side on the sample surface, and their interconnections to further form electronic circuits. These main stages and their corresponding detailed practical process steps can be found in Appendix.III.

A set of highly controllable etch processes was established for distinct material layersso that two kinds of mid-IR photodetectors based on InSb and InAsSb could be fabricated, respectively. More importantly, by using standard photoresist developer to remove the GaSb buffer layer, the underlying GaAs active layers could be exposed with extremely high uniformity and as-grown surface condition. Furthermore, in order to avoid thermally-induced damage to the fabricated InSb photodiodes, a low temperature annealed Ohmic contact was used during fabrication of the GaAs MESFET, and the processing temperature never exceeded 180 ˚C. Finally, an intermediate step was developed where polyimide was applied to provide a smoothing section between the lower MESFET and upper photodiode regions for the interconnection metal to straddle. In addition, dry etch processes for mesa etching and polyimide etching were also investigated, paving the way towards FPA devices with much larger format and smaller pixel pitch.

6. Monolithically Integrated Mid-IR Photo-pixels

By connecting a mid-IR sensitive photodetector to a GaAs switching MESFET side-by-side on the sample surface, a photo-pixel device can be readily formed. This chapter begins with describing the layout designs of several batches of photo-pixel devices fabricated in this work. It then continues with the presentation and discussion of the results obtained from both electrical and optical characterisations, followed by the demonstration of photo-generated signal sampling in the time domain. Finally, a summary of the key achievements obtained with the photo-pixel devices concludes the chapter.

6.1 Fabricated Photo-pixels

As shown in Fig. 6.1, several batches of photo-pixel devices based on either InSb or InAsSb photodetectors have been fabricated adopting various layout designs. The completed photo-pixel devices were then wire-bonded to a leadless chip carrier for further characterisation. An InSb based photo-pixel with the smallest dimensions was fabricated first, and consisted of a 45 µm diameter circular photodiode connected to a MESFET with 100 µm gate width. The following batch was composed of larger devices, where a 150 µm ×150 µm square photodiode was interconnected to a MESFET with 250 µm gate width. Finally, in order to test the flexibility of transferring this technology to other III-V material systems, an InAsSb based photo-pixel that integrated a 200 µm diameter circular nBn photodetector with a 300 µm wide MESFET was fabricated. All batches of photo-pixel devices have switching MESFETs with a 3 µm gate length.

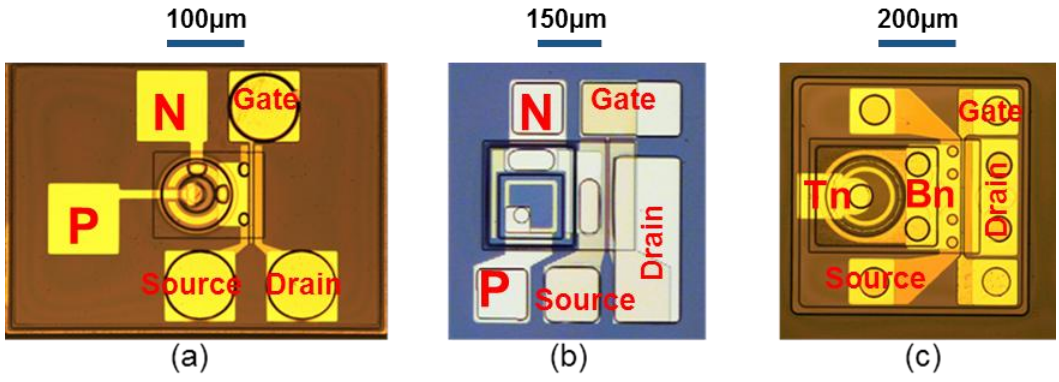


Fig. 6.1. Micrographs of (a) the smallest and (b) a larger pitch of photo-pixel device based on InSb photodiodes. (c) Micrograph of a photo-pixel device based on InAsSb nBn photodetector.

Each pixel has several test-point pads so that the corresponding photodetectors and the MESFET components could be independently probed during the measurement. In each InSb based photo-pixel, there are five metal pads: P, N, Gate, Drain and Source. The metal pads in InAsSb photo-pixels have basically the same functions except two of them are named as Tn and Bn, which are the two Ohmic contacts of nBn photodetector. The node Source and N (or Bn) are short-circuited by the metal interconnection in the complete circuit.

6.2 DC Characteristics

6.2.1 MESFETs

As discussed in Sec. 4.2.1, an Agilent 4155C semiconductor analyser together with the probe-station was used to characterise the DC behaviour of the MESFET. Measurements started by biasing the MESFET with a series of negative voltages applied between the Gate and Source pads(V_{gs}). For each value of MESFET bias voltage V_{gs}, the voltage between the Drain and Source pads (V_{ds}) was swept, and the corresponding current flow $I_{ds}$was measured accordingly. Fig. 6.2 (a) shows the obtained I-V characteristics of a typical fabricated switching MESFET with 3 μm gate length and 100 μm width. Under room temperature operation, the transistor shows a maximum saturation current of approximately 18 mA for V_{ds}> 1.5 V with a gate bias V_{gs} = 0 V. As V_{gs} decreases, the saturation current drops accordingly. Eventually, V_{gs} = -3.5 V is required to pinch-off the channel and thus turn off the transistor. The calculated transconductance as a function of applied V_{gs} is plotted in Fig. 6.2 (b), for several values of voltage applied between drain and source V_{ds}. A maximum g_m value of 100 mS/mm was measured with V_{gs} = 0 V when the device was in saturation region. These results are comparable to previously published GaAs MESFET results with similar gate length and channel doping level [160, 196].

Since the mid-IR photodetectors used in this work are generally zero biased or reverse biased with a small voltage, normally less than 500 mV, the MESFET will operate in the linear region when integrated with the photodiode. As discussed in Sec. 3.3, the ON/OFF resistance ratio plays a key role in the switching behaviour of the MESFET and thus should be maximised. Fig. 6.2 (b) also shows the Drain-Source resistance of the fabricated MESFET as a function of V_{gs} with V_{ds} = 0.1 V. The transistor shows an ON/OFF resistance ratio up to 10^6 with a resistance that varies from 50 Ω in the ON-state to a maximum of approximately 50 MΩ in the OFF-state. This

large variation in transistor output resistance is sufficient for the purposes of this work and these findings are consistent with a reported GaAs MESFET switching device used for an InGaAs detector array [197].

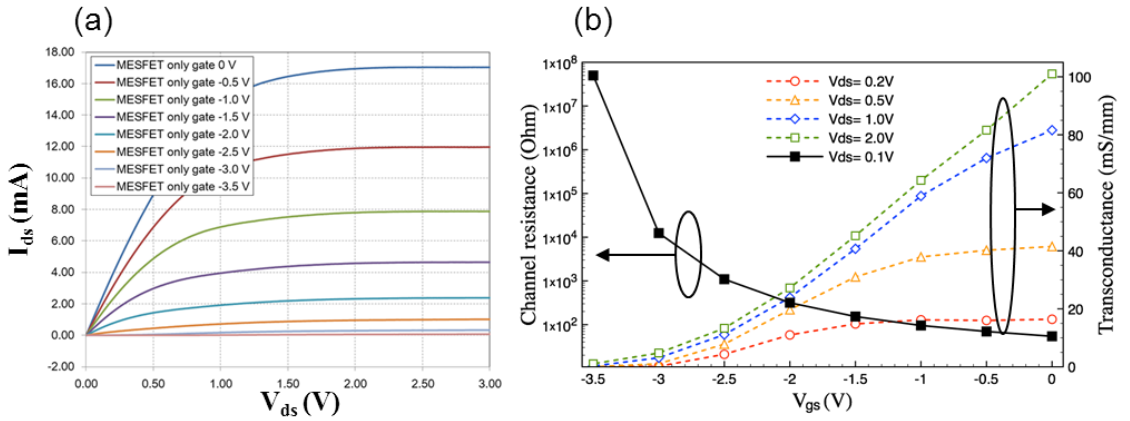


Fig. 6.2. (a) The current–voltage (I_{ds} –V_{ds}) characteristics of the fabricated MESFET and (b) the MESFET drain-source resistance and transconductance as a function of V_{gs}, both at 300K.

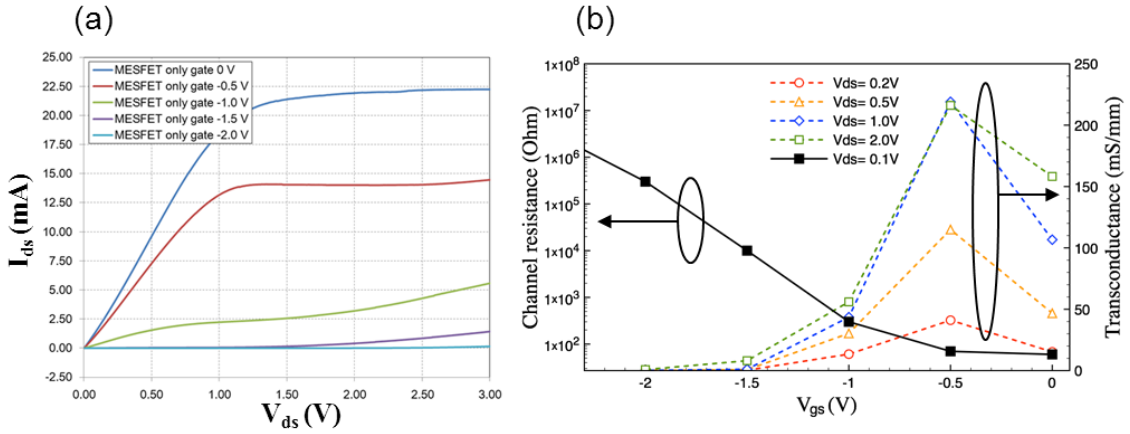


Fig. 6.3. (a) The current–voltage (Ids –Vds) characteristics of the fabricated MESFET and (b) the MESFET drain-source resistance and transconductance as a function of Vgs, both at 77K.

I-V characteristics of the same MESFET device under LN_2 cooling condition was also measured in order to test if good switching performance can be maintained even when a much lower photodiode operating temperature is used. As shown in Fig. 6.3(a), as compared to the results obtained under room temperature, the cooled MESFET shows an increase of saturation current to approximately 23 mA for V_{ds}> 1.5 V with V_{gs} = 0 V. In the meanwhile, the pinch-off voltage reduces to approximately -2 V. When plotting the calculated transconductance as a function of applied V_{gs},the maximum g_m value also increases under all V_{ds} biasing conditions, in some cases showing a 100% increase, as Fig. 6.3 (b) shows. These changes in characteristics are most likely due to

the growth in charge carrier mobility and drift velocity of the active channel layer when the transistor is operated under cryogenic cooling [198, 199].

The On-state channel resistance, which still remains at approximately 50 Ω, confirms that the low temperature annealed Ohmic contact formed is based on the tunnelling mechanism rather than on thermal excitation. More importantly, the OFF-state resistance remaining in the MΩ range also implies that the fabricated MESFET device is able to act as a switch even at 77K. In fact, since the shunt resistance of the mid-IR photodiode increases at such a low temperature, the signal transfer efficiency can be improved dramatically once LN_2 cooling is applied.

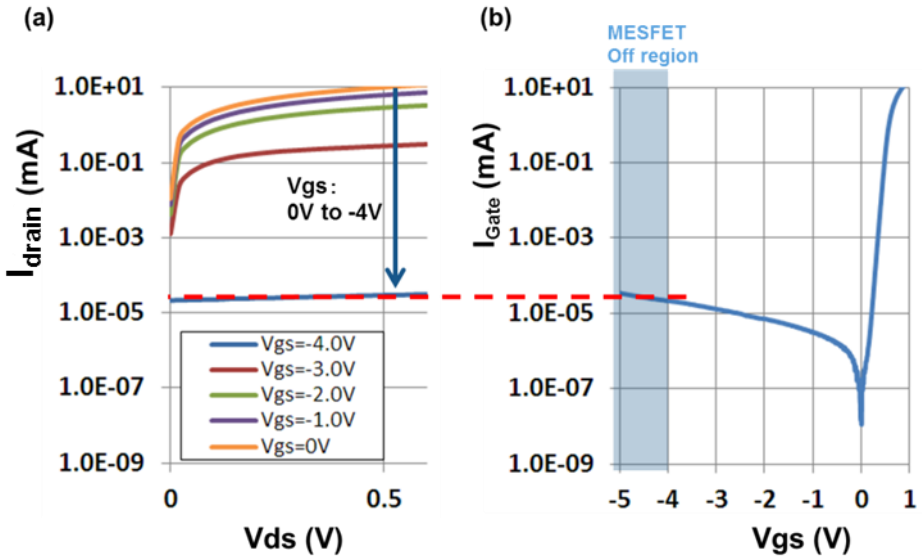


Fig. 6.4. (a) Logarithmic plot of I-V characteristics of a fabricated MESFET, and (b) I-V curve of the Gate Schottky diode in the same device, highlighting that the residue current in the MESFET OFF-state equals to the Gate leakage current at the corresponding biasing conditions.

In order to gain a better understanding of the OFF-state behaviour of the fabricated switching MESFETs, the current flowing through the Gate and the Source nodes was also measured. As shown in Fig. 6.4 (a), when the pinch-off voltage V_{gs} = -4V is applied, the I-V characteristic of the MESFET shows a residue current of approximately 20nA, which appears to be nearly independent from V_{ds}. Moreover, as shown in Fig. 6.4 (b), the OFF-state residue current matches very well with the current flowing between the Gate and Source under the same biasing condition. This further confirms that the MESFET OFF-state residue current is mainly arising from the reverse leakage current of the Gate Schottky diode rather than from the substrate leakage (Sec. 3.2.2).

6.2.2 Mid-IR Photodetectors

The I-V curve for the InSb non-equilibrium photodiode on its own was obtained by measuring the current through the two pads labelled P and N. As shown in Fig. 6.5, under room temperature, a typical fabricated circular InSb photodiode with 45 μm diameter active sensing area shows an obvious rectifying behaviour when reverse biased. Although a high reverse leakage current (order of mA) is observed with V_{PN}< -20mV, it is also commonly reported in other InSb based photodetectors regarding the large number of thermally excited carriers across the band gap that is only 0.17 eV [121, 200]. As a result, when being used to detect mid-IR light under room temperature, all InSb based photodiodes have to be zero biased in order to minimize the dark current to the order of μA.

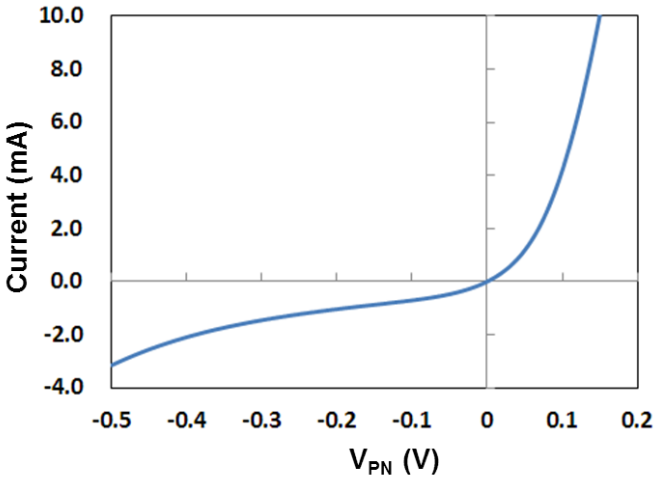


Fig. 6.5. The I-V characteristics of a 45 μm diameter circular InSb photodiode fabricated in a photo-pixel device.

As discussed in Sec. 3.3.2, the zero bias "resistance.area" product (R_0A) is a known figure of merit for evaluating the DC behaviour of the photodiodes, with a higher value indicating a better device. Initially, using samples from a single wafer, a series of circular InSb photodiodes was fabricated and tested without applying any further MESFET processes. The measured R_0A values for these photodiode-only devices are plotted as red squares in Fig. 6.6 as a function of perimeter to area ratio (P/A). The obtained R_0A product results have an average value of approximately $1.3\times10^{-3}\ \Omega\ cm^2$, and are almost independent with scaling of the mesa sizes. This property confirms a good device passivation is performed when using the fabrication processes developed in this work, which has significantly suppressed the surface leakage current [201].

Then, the photodiodes integrated in various batches of photo-pixel devices were tested. These devices have either square mesas with dimensions from 45 µm × 45 µm to 150 µm × 150 µm or circular mesas with 45 µm diameter. The obtained R_0A product results are displayed in Fig. 6.6by the blue diamond symbols. It can be seen that the R_0A results of the photo-pixel devices compare favourably with those obtained from the photodiode-only devices, proving that the low thermal budget fabrication of the MESFET used in this work does not introduce obvious performance degradation to the InSb photodiodes. Moreover, the higher R_0A value displayed by some of the photo-pixel devices can be explained either by a better quality of the growth in the sample used (although from a single wafer), or by the effect of the different contact shape between various batches (see the inset micrograph images).

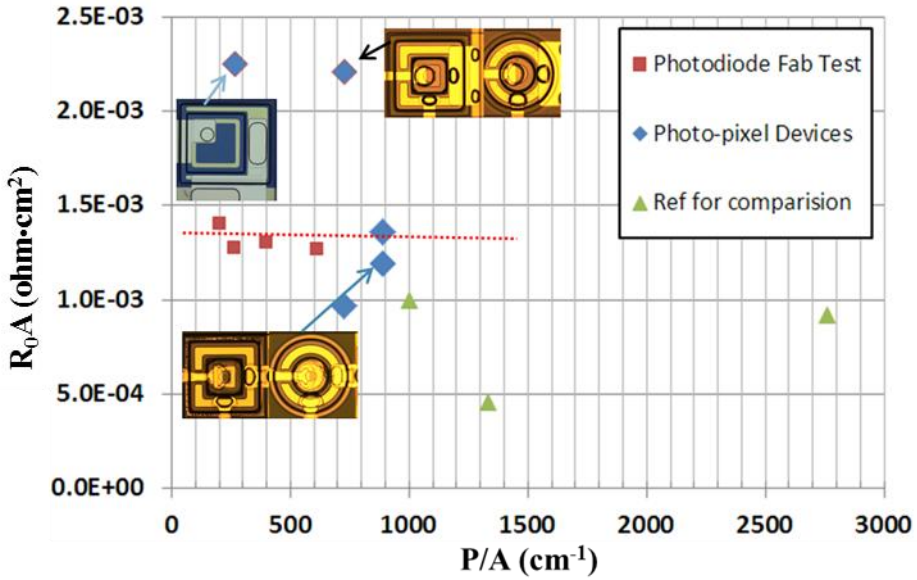


Fig. 6.6. Summary of measured R_0A product as a function of P/A value, at 300K.

Results from previous research have also been plotted in Fig. 6.6 for comparison. Previously published work showed InSb circular photodiodes with a diameter of 30 µm (P/A 1333 cm^{-1}) yielded R_0A values of 0.46×10^{-3} Ω cm^2 [200]. Note that these photodiodes were grown on GaAs substrates and fabricated on an epi-structure that did not include a p+ barrier between the contact layer and the absorption layer. When the barrier was introduced to form a InSb non-equilibrium photodiode, a higher value of 0.92×10^{-3} Ω cm^2 could be obtained for a square diode the side of which was 14.5 µm (P/A ~2760 cm^{-1}) [121]. The same photodiode structure grown on InSb (100) substrate produced R_0A values, at room temperature of approximately 1×10^{-3} Ω cm^2 [119]. It can thus be concluded that the performance of the InSb photodiodes fabricated in this work is comparable with results obtained from previously reported InSb photodiodes grown

on either GaAs or InSb substrates. Also, the obtained data confirms that the introduction of a barrier in the layer structure can obviously increase R_0A value and hence improve the photodiode detection performance.

Measurements were also performed under LN_2 cooling (~77K) which is a common operating condition for mid-IR photodiodes to achieve their best performance. Fig. 6.7 shows the I-V curves of a fabricated 45μm × 45μm sqaure InSb photodiode measured at 77 K and 300 K for a side-by-side comparison. As previously stated, thermally generated carriers dramatically contribute to the reverse leakage current because of the small energy bandgap of InSb, whereas their contribution is much less at 77K. A dramatic drop in dark current can thus be observed. The leakage current near 0 V decreased from 1.14 μA at 300 K to 150 nA at 77 K. A similar reduction was also observed for a small reverse bias of -50 mV, for which the dark current decreased from ∼520 μA at room temperature to ∼3 μA. In forward bias, the I-V characeteritic of the photodiode shows two regions in which the current flowing through the photodiode p-n junction is dominated by two distinct components respectively. At higher bias ($0.1V < V_{PN} < 0.2V$), the current increase exponentially with the bias voltage and an ideality factor of 0.95 can be caclutated from linear fit of the I-V curve. In this case, because the value of ideality factor is close to one, the current flow is dominated by the drift-diffusion component. An ideality factor of approximately 2.4 is obtained at lower bias (V_{PN} = ~ 50mV), suggesting that the remobination current within the jiunction depletion region starts dominating. Similarly, in reverse bias, the photodiode I-V characteristic is decided by different comoponents including SRH generation, Ohmic leakage and avalanche breakdown. In order to understand which component is dominating the current flow particularly in very low reverse bias, the R_0A value of photodiodes fabricated in this work is compared with that obtained in literatures.

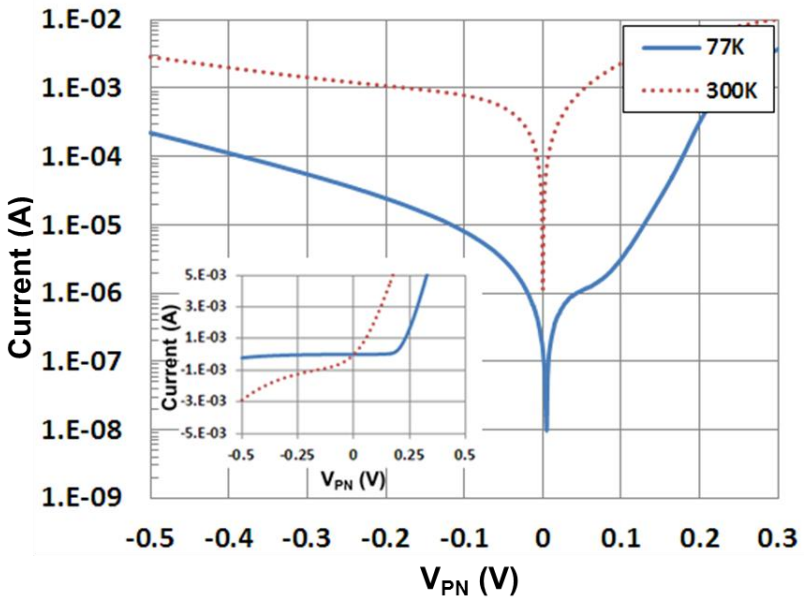


Fig. 6.7. The I-V characteristics of a 45 μm × 45 μm square InSb photodiode fabricated in a photo-pixel device, at 77K.

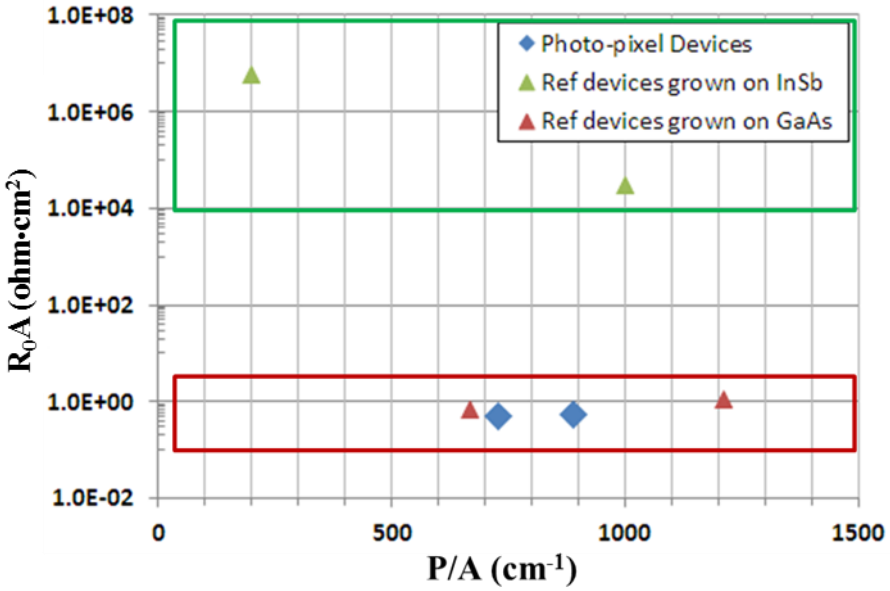


Fig. 6.8. Summary of measured R_0A product as a function of P/A value, at 77K.

As shown in Fig. 6.8, by applying LN_2 cooling to reduce the dark current, the R_0A of the fabricated photodiodes can display an increase by 2 orders of magnitude. At 77K, the photo-pixel devices can yield an R_0A value of approximately 0.54 Ω cm^2, in good agreement with results reported from similar structures also grown on non-native substrates such as GaAs [200] and Si [165]. However, this value is still much smaller (by approximately 5-7 orders of magnitude) than the 77K R_0A results reported in previously published works reporting on photodiodes grown on native InSb substrates [119]. Thus, the results obtained in this work support that the 77K R_0A value of InSb photodiodes grown on non-native substrates is mainly limited by the Ohmic leakage, and that this in turn is related to the density of thread dislocations created in the

photodiode active layers during the MBE growth. Moreover, the results also show that the inserted p+ barrier layer will no longer show any observable improvement of the R_0A value if the devices are operated at cryogenic temperatures.

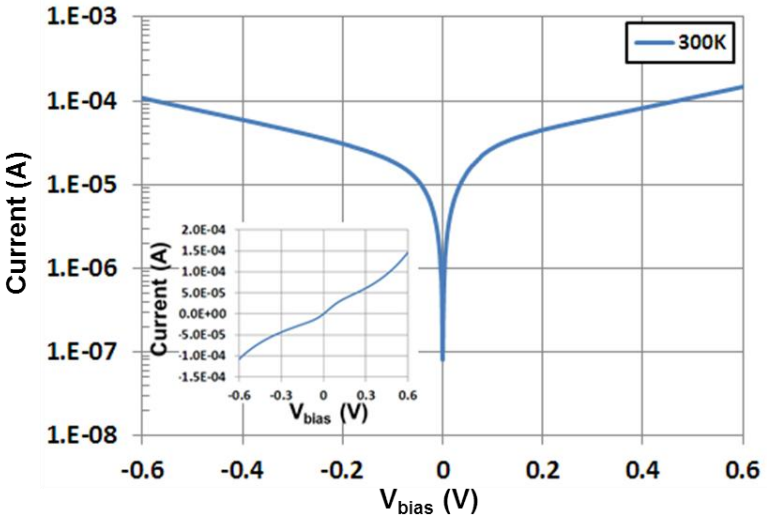


Fig. 6.9. The I-V characteristics of an InAsSb photodetector fabricated in a photo-pixel device, at 300K.

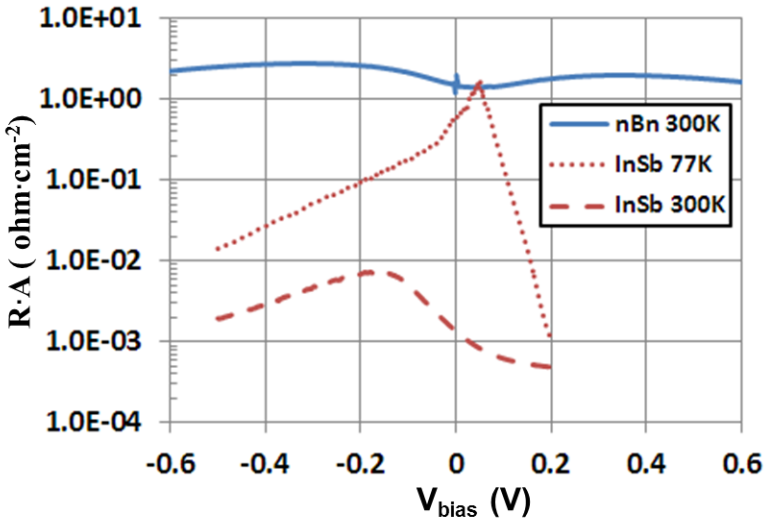


Fig. 6.10. Measured R_0A product of the nBn photodetector as a function of bias voltage.value, at 300K.

I-V curves of InAsSb nBn photodetectors were also obtained, by measuring the current through the two pads labelled Tn and Bn. As shown in Fig. 6.9, at room temperature the I-V curve of a fabricated 200 µm × 200 µm square nBn photodetector displays a very small dark current (on the order of µA) which shows only a moderate increase when few hundred mV of reverse bias are applied. Since the underlying operating principle of an nBn photodetector is similar to that of a bulk photoconductor device, the I-V curve shows a resistor-like behaviour instead of a rectifying one. Generally, nBn photodetectors do not operate near zero bias like the Insb ones, therefore their R_0A product is normally plotted as a function of voltage bias conditions. As shown

in Fig. 6.10, an average R_0A value of ~2 Ω cm^2 is obtained under all bias conditions and at room temperature. By comparing these results with those obtained from InSb photodiodes, it is obvious that InAsSb nBn photodetectors are a promising HOT detector structure that can provide significantly improved R_0A value and potentially improve the detection performance of the photo-pixel devices.

6.2.3 Complete Photo-pixels

The complete photo-pixel, containing both the photodetector and the MESFET, was characterised by measuring the current flow inside the device as a function of the gate bias voltage. During the actual measurements, the pad P (or Tn in thenBn devices) of the photo-pixel was connected to signal ground which was 0 V. In the meanwhile, the Drain node voltage labelled V_d was swept from 0.5 V to -0.5 V, with various values of gate bias V_g applied.

The I-V characteristics of the photo-pixel devices have been found to be dependent on the sizes of the InSb diodes, with different behaviour observed for small (i.e. 45x45 μm) and big (i.e. 150x150 μm) ones. For InSb based photo-pixels with 150 μm square-shaped photodiodes, as can be seen in Fig. 6.11 (a), the MESFET component dominates the I-V characteristic since the resistance of the photodiode, in either forward or reverse bias, is much smaller than the transistor ON-state resistance, which is 40-50 Ω. In comparison, as shown in Fig. 6.11 (b), since 45 μm diameter circular photodiodes have resistance greater than the MESFET ON-state resistance, the pixel I-V characteristic starts to follow the photodiode I-V curve when reverse biased, thus showing a rectifying behaviour. When V_g is decreased so that the MESFET switches off, the pixel I-V characteristics show a drop in the current as $V_d$is swept. A V_g value of ~ -4 V is required to switch off the photo-pixel circuit, which matches well the pinch-off voltage derived from the aforementioned characterisation of the MESFET alone. Similar switching behaviour is also obtained when the device is cooled at 77K, as shown in Fig. 6.11 (c). Due to the dramatic increase in photodiode resistance at such a low temperature, the I-V curve of the photo-pixel with V_g= 0V and $-V_d < 0$ overlaps with the photodiode-only curve. Additionally, when the pixel is switched to the OFF-state, a residual current ranging from a few tens of nA to a few hundreds of nA is generally measured, which corresponds to the reverse leakage current of the MESFET Schottky Gate.

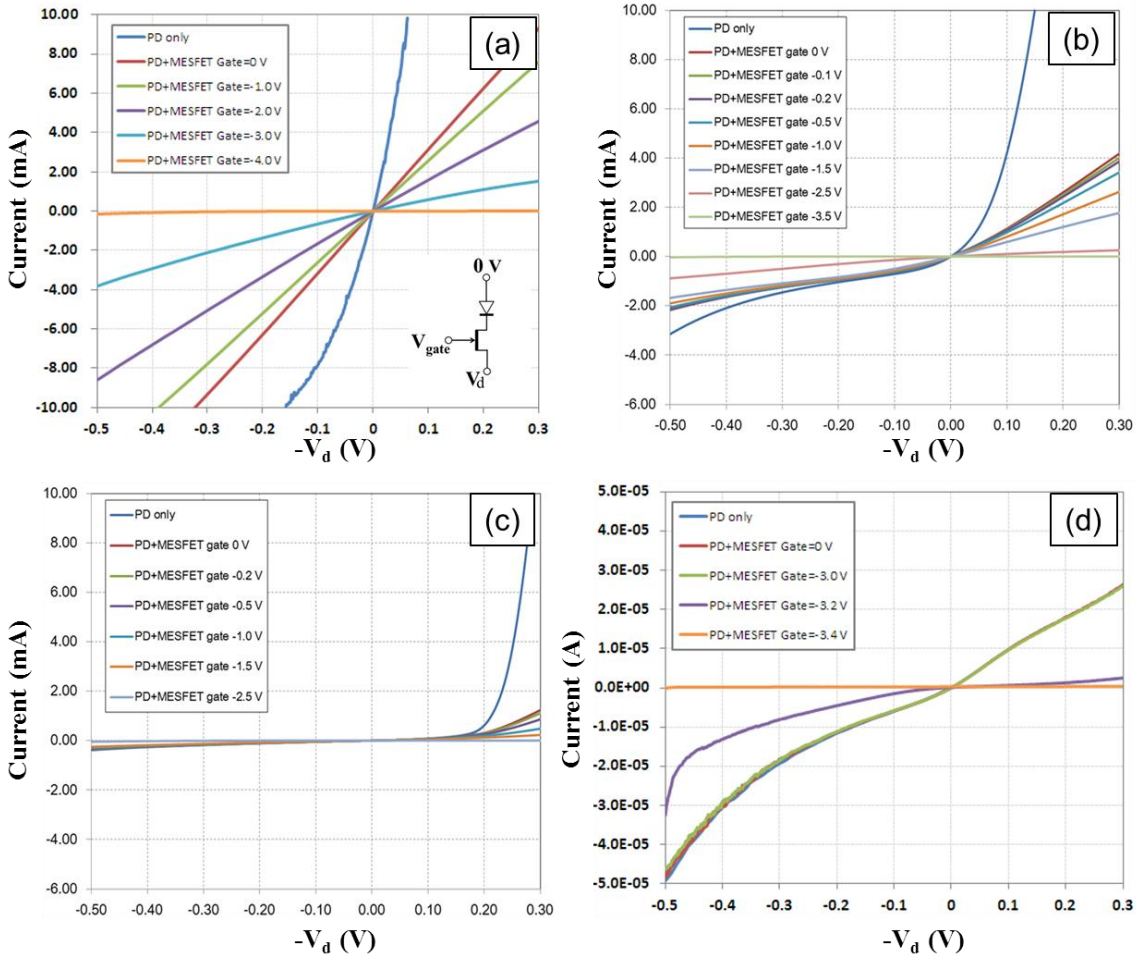


Fig. 6.11. The current–voltage characteristics of photo-pixel devices with (a) a 150 μm square shaped InSb photodiode (b) a 45 μm diameter circular InSb photodiode at 300K (c) a 45 μm diameter circular InSb photodiode at 77K (d) a 200 μm square shaped InAsSb nBn photodetector at 300 K.

The I-V curves of an InAsSb based photo-pixel device with 200 μm square-shaped nBn photodetector are shown in Fig. 6.11 (d). At room temperature, the pixel I-V characteristics of the InAsSb based photo-pixel duplicates the nBn photodetector-only curve with 0V $>V_g>$ -3V regardless of V_d. This is because the nBn photodetector has much larger resistance (~5 KΩ) as compared the MESFET ON-state resistance and thus a near 100% current transfer efficiency can be obtained according to Eqn 3.30. In other words, this implies that the photocurrent generated in the nBn detector can pass though the switching transistor without obvious signal loss, which is highly desirable in terms of the resulted detection performance of the integrated photo-pixel. The current flow will be eliminated when the transistor is at the pinched off point where the MESFET OFF-state resistance dominates.

6.3 Photo-response and Signal Switching

6.3.1 InSb photo-pixels

Having satisfied with the electrical characteristics that the MESFET was capable of turning off the photo-pixel, optical characterisation was then carried out to measure the detected photo-response of the completed circuit under illumination. As described in Sec. 4.3.1, a Bruker Vertex 70 FTIR spectrometer was used to measure the relative photo-response of the photo-pixel device. All measurements were done at room temperature and in standard atmosphere. For measuring the InSb based devices, no bias voltage was applied between node P and node Drain of the MESFET (zero bias). A small bias voltage was instead applied between node Tn and node Drain when testing the InAsSb based devices, as this is normally the way nBn devices are tested [202]. A SR570 current preamplifier was connected to the node Drain of the photo-pixel devices and its output was fed to FTIR system for measuring the response.

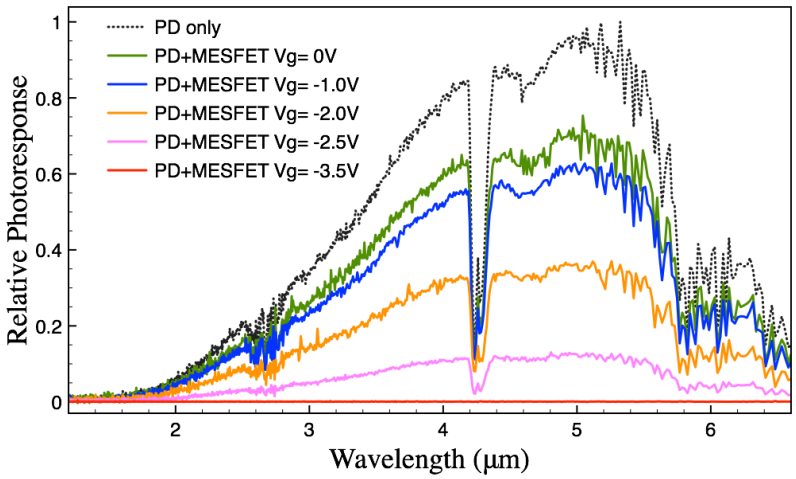


Fig. 6.12. The relative spectral response of the InSb based photo-pixel device under various gate bias conditions [203].

Fig. 6.12 shows the spectral scan results obtained from the same InSb-based photo-pixel device with a 45 μm diameter photodiode for various values of V_g. The obtained spectra covered the wavelength range from 1.3 μm to 6.7 μm with a peak in the response existing at 5.1 μm. A half width at half maximum (HWHM) of 1.1 μm is achieved, which is consistent with results from similar InSb photodiodes operating at room temperature [121]. Due to absorption by CO_2 molecules present in the atmosphere, a sudden drop in photoresponse at approximately 4.2 μm is observed. There are also two less well-defined signal drops at 2.6 μm and 5.8 μm, which can be attributed to absorption by water vapour. More importantly, by reducing the V_g applied to the switching MESFET component of the photo-pixel, the measured photo-response

displays an obvious decrease in amplitude. Eventually, when V_g reached the pinch-off point of the MESFET (~ -3.5V), the photo-response was totally eliminated. As a result, the entire pixel was turned off and isolated from the readout line. Additionally, the photo-response of the InSb photodiode component, by itself, was also measured, shown by the black dotted line in Fig. 6.12. By comparing the spectral amplitude data of the photodiode alone with that obtained from the integrated photo-pixel device, a signal transfer efficiency of approximately 70% was achieved. This value is in good agreement with that predicted by Eqn 3.20, if the resistances of the photodiode and of the MESFET in ON-state are substituted into the equation.

6.3.2 InAsSb photo-pixels

The photo-response of an InAsSb based photo-pixel device with 200 µm square-shaped nBn photodetector is shown in Fig. 6.13. Due to the larger bandgap of the absorption material, the obtained spectra have a cut-off wavelength of 4.5 µm and a peak response at approximately 3.2 µm. Similarly, by applying negative Gate bias voltages to the photo-pixel, the flow of photo-generated carriers (i.e the photocurrent) can be controlled accordingly. More importantly, the results confirm that a near 100% MESFET transfer efficiency can be achieved which agrees very well with the DC electrical measurement. However, it can also be seem that the obtained spectra traces got somewhat noisier as the applied V_g approached the pinch-off point of the corresponding MESFET component. The source of this noise still needs further investigation. It is unlikely to be introduced by the gate leakage of the MESFET component since a clean spectral data can be recovered when the pixel is fully turned off.

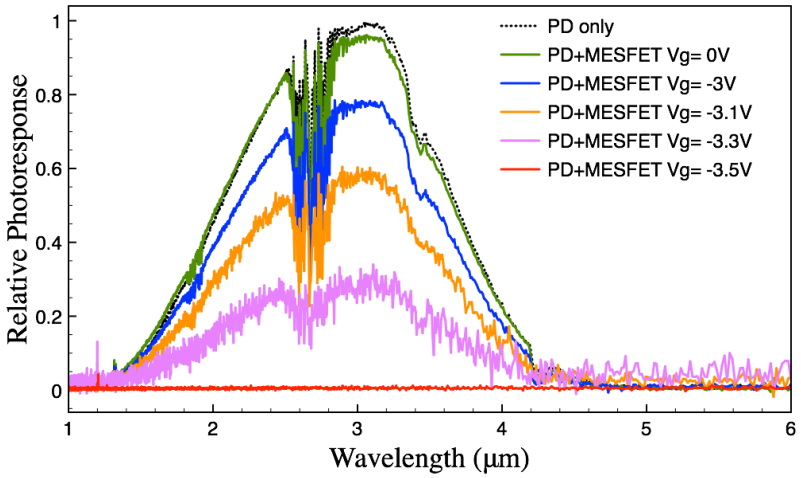


Fig. 6.13. The relative spectral response of the InAsSb based photo-pixel device under various gate bias conditions.

Unexpectedly, the fabricated InAsSb nBn photodetectors were found to be extremely unstable and thus delicate. During prolonged photo-response measurements an obvious increase of noise was observed for most devices under test, sometimes leading to degradation and disappearance of the photo-response signal.

The deterioration of the InAsSb nbn photodetectors was present both if they were fabricated and tested independently, or as a component inside an integrated photo-pixel, proving that the problem was not caused by introducing the MESFET. The matter is thought to be linked to chemical reactions taking place on the sidewall surface, particularly between the passivation layer and the barrier layer which has very high aluminum composition and thus could easily be oxidized [204]. This hypothesis is supported by the fact that similar photodetectors that were previously reported did not suffer from performance degradation [144, 202]. In those reported devices, the mesa etching was stopped once arriving the barrier layer, whereas the sidewall of all active layers had to be exposed and passivated in this work in order to further fabricate the MESFET. It can be concluded that the fabrication process currently in place for nBn photodetectors still needs further investigation and optimisation.

6.4 Video Rate Sampling

In order to test the switching speed, transient response of the fabricated InSb based photo-pixel was measured using a waveform generator and the SR570 pre-amplifier. With the node P grounded, the Drain node of the photo-pixel was connected to the SR570 for converting the current into a voltage signal with a pre-set gain. Again, no bias voltage was applied between pad P and the pad Source during the measurement to avoid overloading the amplifier with an excessive current. The experimental set-up is shown in Fig. 6.14. A logic square waveform was generated and applied to the Gate node to control the switching MESFET. In the meanwhile, the output signal of the amplifier together with the synchronisation signal from the waveform generator was monitored by the oscilloscope and saved for further measurement of the switching time. Moreover, except for testing under the dark environment, the Hamamatsu mid-IR QCL laser as mentioned in Sec. 4.3.2 was used to generate carriers inside the InSb photodiode. As a result, the sampling behaviour of the photocurrent using the corresponding transistor could be also monitored during the experiments.

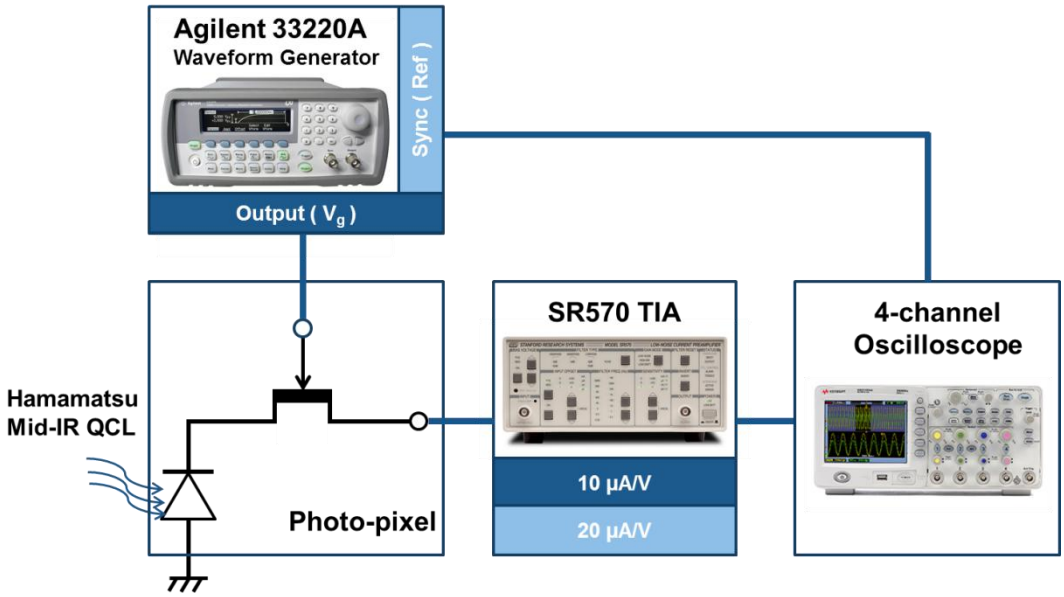


Fig. 6.14. Schematic of the experimental set-up used to measure the transient response of the photo-pixel device.

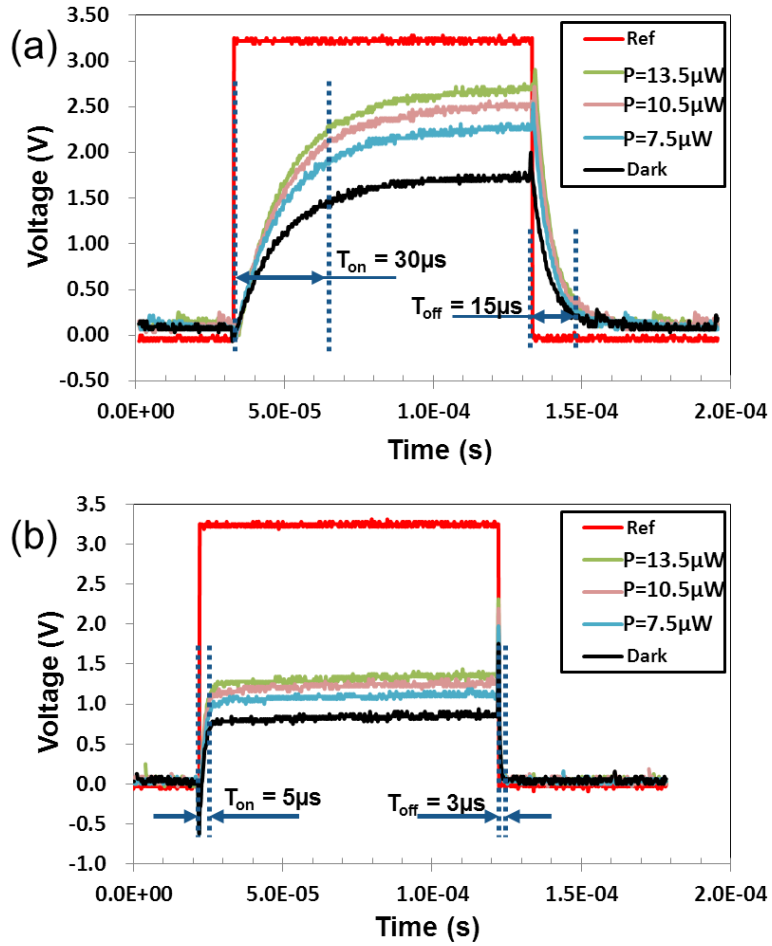


Fig. 6.15. Transient response of the fabricated InSb photo-pixels, measured with (a) 10 µA/V and (b) 20 µA/V sensitivity of the SR570 amplifier being set.

Fig. 6.15 shows a signal sampling cycle in the time domain obtained with a typical photo-pixel device in which a 150 µm×150 µm square photodiode was connected to a switching MESFET with 250 µm gate width and 3 µm length. A set of laser bias current

values, from 750mA to 850mA, are referred which represents various incident power levels applied to the photodiode correspondingly. Switching of the photo-pixel is triggered by applying a 5 KHz digital signal to the Gate node, where 0V is “High” and -4V is “Low”. Sampling of the photo-generated voltage signal begins when the device is turned ON by applying a “High” level voltage whereas the photo-generated signal is excluded from the output voltage if a “Low” level voltage comes.

With sensitivity (or gain) of the SR570 amplifier being set to 10 μA/V, as shown in Fig.6.15 (a), an ON/OFF switching time of T_{on}= ~30 μs and T_{off}= ~15 μs respectively is achieved, which is independent of the power level of the applied illumination. A significant improvement of the switching speed was observed when the amplifier sensitivity was changed to 20 μA/V, with T_{on} and T_{off} reduced to approximately 5 μs and 3 μs. The 3-dB cutoff frequency defined bandwidth is approximately 10 KHz at 10 μA/V amplifier sensitivity and 100 KHz at 20 μA/V. As discussed in Sec. 3.3.2, under both amplifier settings, the measured switching speed meets the requirement of implementing a monolithic mid-IR FPA device with 64×64 pixels and standard video rate (30 fps) scanning.

According to the manual of SR570, the amplifier itself is not band-limiting the measurement under both sensitivity settings, as its bandwidth should be 200 kHz [205] in both cases. In order to find the actual limitation of the maximum switching speed, the capacitance of both the MESFET Gate and the InSb photodiodes were measured by a LCR meter. The measured Gate capacitance shows a value of approximately 10 pF which is comparable to reported values for GaAs devices of similar dimensions [160]. According to Eqn.3.18, the fabricated MESFETs should present a maximum speed at least in the order of MHz, and thus should not limit the bandwidth of the measurement as well. On the other hand, a 45 μm diameter InSb photodiode shows a rather large capacitance of 136.5 nF, approximately corresponding to a 170 KHz bandwidth. With larger active sensing area, bandwidth can even further drop to 20 KHz [164]. Therefore, the actual switching speed of the photo-pixel is most likely limited by the photodiode bandwidth rather than by the MESFET. The reason for obtaining a large photodiode capacitance under room temperature needs further investigation. It may be due to the presence lattice defects in large number, or to impurities and surface states that can act as charge trapping centers and introduce charge latency [206].

6.5 Summary

In this chapter, the electrical characterisation results of the single photo-pixel devices fabricated were presented. By probing the test-pads of the photo-pixel correspondingly, the MESFET and the photodetector component could be characterised independently. Under room temperature, the MESFET showed excellent switching behaviour with an ON-state resistance of as little as 50 Ω and an ON/OFF resistance ratio of 10^6. The InSb photodiode showed a clear rectifying behaviour with R_0A value comparable to devices previously reported in the literature, whereas the InAsSb nBn photodetector presented some issues needing further investigation to improve its performance. After proving that the two components fabricated side-by-side individually functioned as-designed, DC characterisation of the completed photo-pixel was carried out. Similarly to a single MESFET device, in which the Schottky Gate can be used to control the Drain-Source current, the current flow in either the InSb-based or InAsSb-based photo-pixel was also found to be switchable by applying biasing voltages to the Gate node.

The chapter continued by presenting the optical characterisation results of the photo-pixels. Using the FTIR system, isolation of the photo-generated current from the readout line was observed when the device was biased to be turned off. Finally, the switching speed of the InSb based photo-pixel was measured through transient response experiments. An ON/OFF switching time with T_{on}= ~30 µs and T_{off}= ~15 µs respectively was achieved when the sensitivity of SR570 was set to 10 µA/V. The results meet the requirement of implementing prototype array devices for mid-IR imaging purposes.

7. Monolithic Focal Plane Arrays for Mid-IR Imaging

A new type of monolithic focal plane array was created by replicating the single photo-pixel discussed in the previous chapter and by arranging the devices into a two-dimensional array format. To complete the readout circuit, the P nodes of all the pixels are connected to a common ground line, whereas the Drain and Gate nodes were connected to common row and column lines, respectively. Through corresponding metal pads placed around the sensing area of the array device, these common lines could then be accessed by the driving circuits, and hence an X-Y addressing architecture could be achieved.

This chapter begins by discussing the completed array devices together with the driving circuits and programmes that were used to control the switching of pixels in the array and hence to capture images in real-time. The chapter continues with the presentation of the most important characterisation results obtained with the imaging system. After demonstrating the imaging capability of the fabricated prototype arrays by a series of real-time imaging experiments, the chapter ends by summarising the performance of the device.

7.1 Imaging System Setup

7.1.1 Fabricated Devices and Driving Circuits

As proof of concept, two batches of prototype array devices with either 4×4 or 8×8 format were fabricated in this work. As shown in Fig. 7.1, these devices have a 400 μm × 400 μm pixel pitch, whereas the active sensing area in each pixel consists of a 150 μm × 150 μm InSb photodiode, leading to a fill factor of approximately 14%. The completed array devices were mounted and bonded to ceramic leadless chip carriers, and then loaded into a driving circuit board. A set of input/output pins and off-the-shelf CMOS logic components were included in the circuit board in order control the switching of the pixels and thus to implement the readout of the photo-generated signal. As shown in Fig. 7.2, the main logic components for driving the array devices are a column multiplexer (MUX) and a row decoder (DEC). Standard CMOS based decoders could only output positive voltages, which would have been unsuitable for switching the GaAs MESFETs inside the pixels. A simple voltage reversing circuit based on standard

operational amplifiers was therefore added to the circuit, in order to convert the positive output voltages of the DEC into negative values.

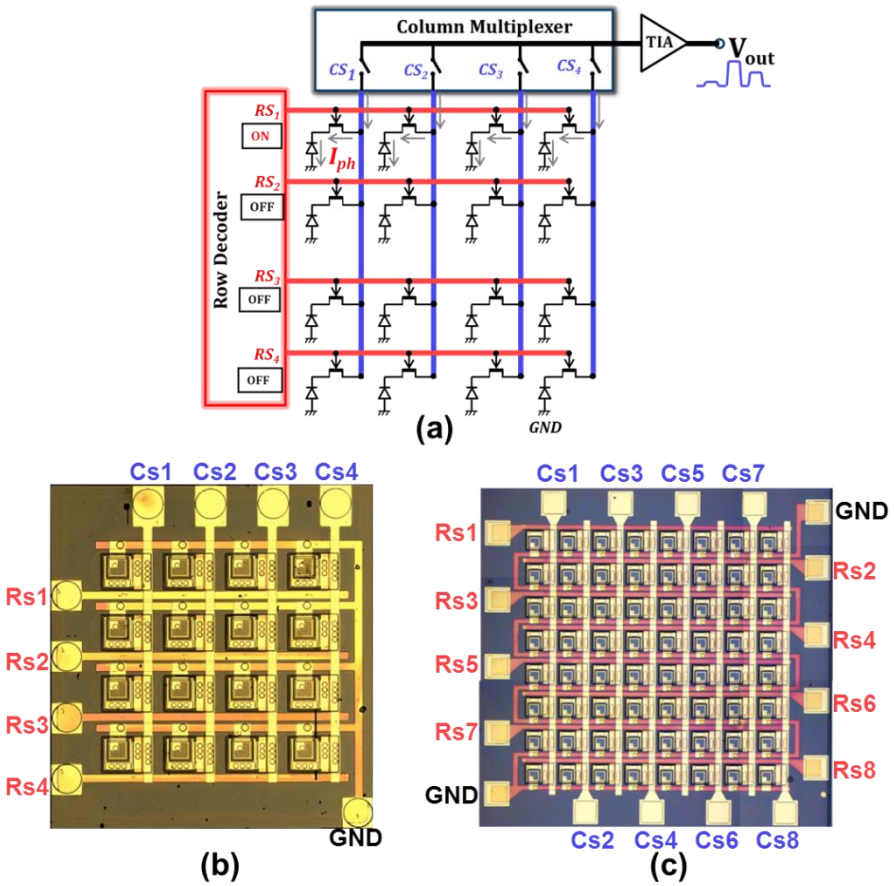


Fig. 7.1. (a) Schematic of the 4×4 array architecture followed by micrographs of the fabricated prototype focal plane array devices with (b) 4×4 and (c) 8×8 pixels format.

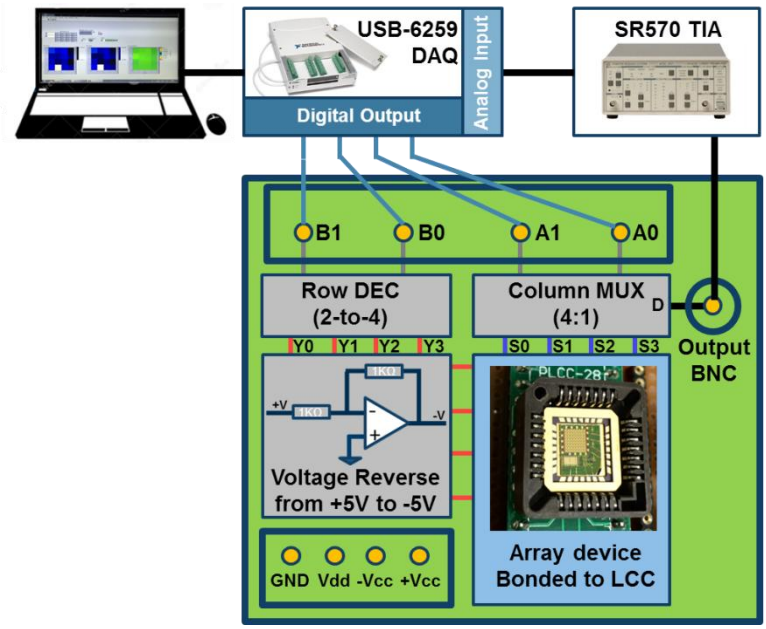


Fig. 7.2. Illustration of the imaging system setup with a 4×4 array loaded, demonstrating the wire connections between the array device, the driving circuit, and the data acquisition unit.

When driving the 4×4 array, the four common column lines of the device were first connected to the input nodes, S0 to S3, of a 4:1 MUX. After reversing the voltage through the inverting amplifiers, the output nodes of a 2-to-4 DEC, Y0 to Y3, were connected to the four common row lines. The switching of the MUX was controlled through two digital pins: A0 and A1, whereas another two digital pins B0 and B1 were used for controlling the output of the DEC. The pins Vdd, +Vcc,-Vcc and GND on the driving circuit were used to connect the voltage supplies required by the CMOS components. The common node D of the MUX was used as output of the driving circuit board.

In order to simultaneously control the switching of pixels in the array device and acquiring the photo-generated signal, a National Instrument USB-6259 Data Acquisition (DAQ) unit was used. After connecting the output node of the driving circuit to the SR570 pre-amplifier, the signal was fed to one of the analog input nodes on the DAQ for sampling and analog-to-digital conversion (ADC). Finally, the four digital output nodes of the DAQ were connected to the four digital pins (A0, A1, B0 and B1) for generating the digital waveforms used to drive the switching of the pixels.

7.1.2 Programme for Data Acquisition

Having satisfied that all the wire were properly connected, a Labview programme developed in this work was used to perform the data acquisition and monitor the obtained data on a laptop in real-time. The main function of this programme was to create a synchronised sampling cycle so that the signal from the array device could be read into the DAQ after a certain set of digital output voltages had been dumped to the digital pins of the driving circuit.

Fig. 7.3 shows the basic flow of the programme created for driving the 4×4 array. Initially, sixteen digital address strings (from “0000” to “1111”) were created. Each address represents a set of digital output voltages that can be used to selectively turn on a certain pixel in the array through the driving circuit. These digital voltages were then dumped to the driving circuit board in sequence with a certain rate f_{scan}. After a certain address was dumped for a period of $1/2f_{scan}$ seconds, the signal from the array device was sampled into the DAQ. Finally, depending on which row and column the selected pixel belonged to in the 4×4 array, the obtained data was plotted at the corresponding position in a 4×4 intensity graph. A real time image could thus be acquired during the experiments.

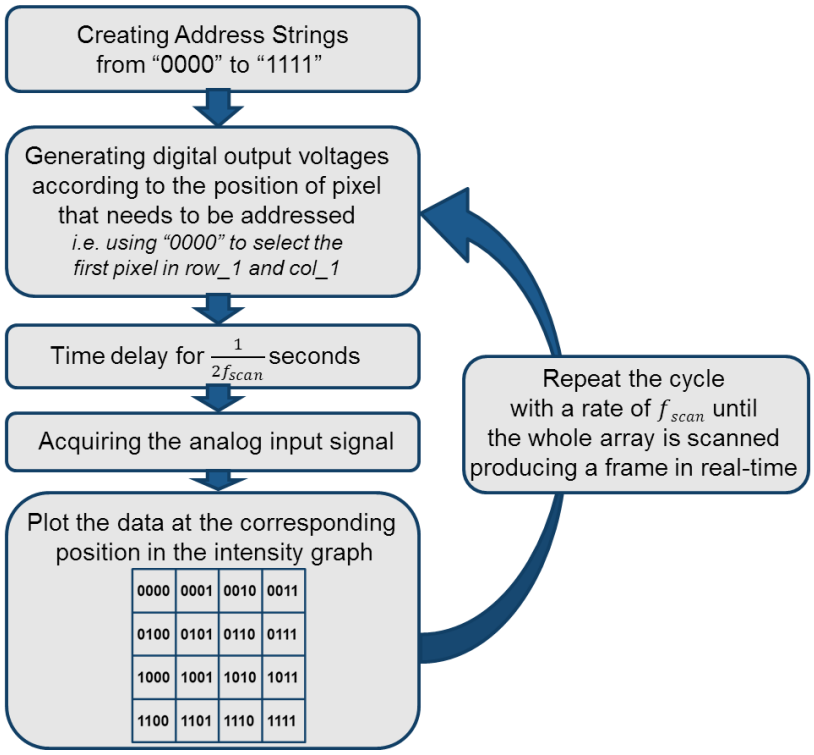


Fig. 7.3. Flow diagram of the programme used to acquire images from a 4×4 array in real-time.

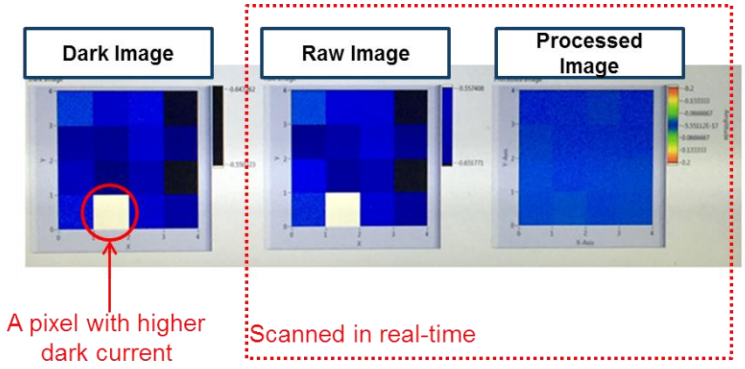


Fig. 7.4. Illustration of the basic programme interface, demonstrating dark level subtraction in real-time.

At the beginning of the experiments, a dark image was first captured without illumination, saving the data obtained from each pixel in the first intensity graph, dubbed "Dark image" in Fig. 7.4. It can be seen that a pixel in this 4×4 array showed a slightly higher dark level. In order to exclude the effect of dark level difference caused by the devices non-uniformity, a software based CDS method (see Sec. 3.4.2) was then used. During the acquisition, the program kept subtracting in real-time the previously saved dark levels from the actual image captured (labelled "Raw Image" in Fig. 7.4). In this way, an image where the non-uniform dark level was excluded and only the photo-generated signal contributed could be formed (shown as "Processed image" in the third intensity graph).

7.2 Characterisation Results

7.2.1 FTIR Spectral Response

In order to check the spectral response of the fabricated array devices, it is necessary to manually readout the signal from each pixel in sequence. Using the above-mentioned DAQ, a certain set of DC addressing voltages was generated to control the driving circuit and only switch on one pixel at a time. The photo-generated signal from each selected pixel was then fed into the FTIR spectrometer system for measurement. After obtaining the spectral response of one selected pixel, another set of DC addressing voltages was applied to readout the next pixel. The same measurement was repeated until the spectral photoresponses of all pixels in the array were obtained.

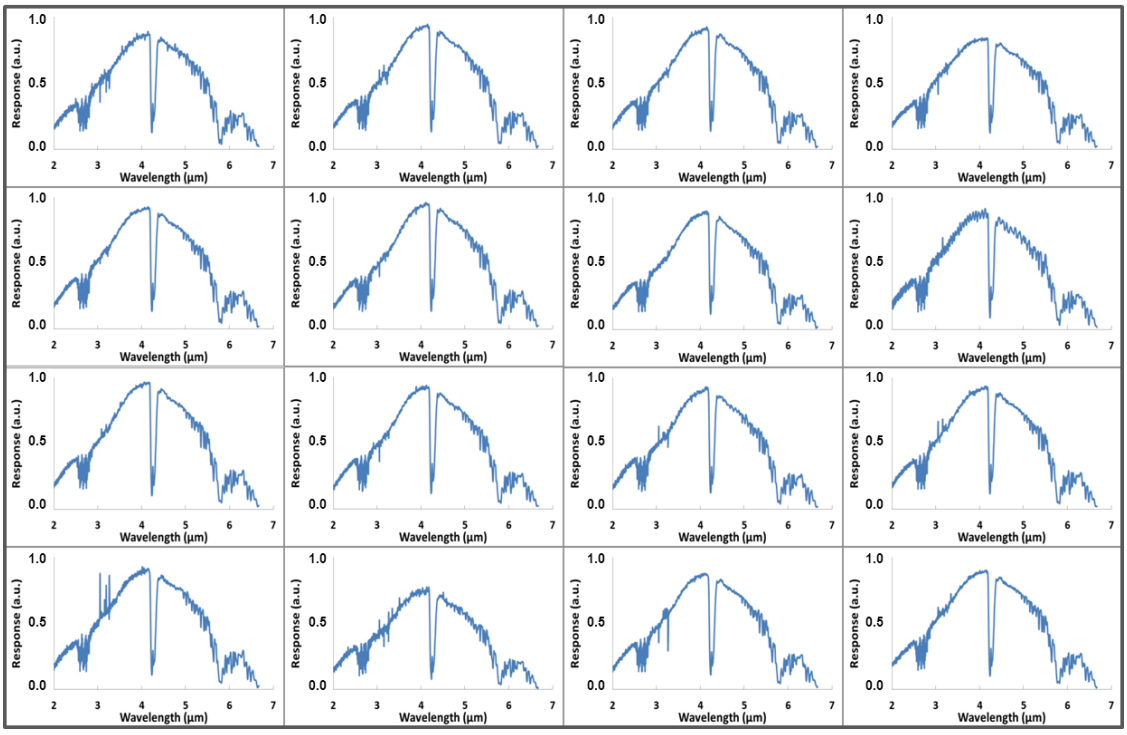


Fig. 7.5. The relative spectral response of every pixel addressed from a 4×4 array device.

Fig. 7.5 shows the measured spectral photoresponse of every pixel addressed from a fabricated 4×4 array device. Note that all of the spectral data was obtained with the FTIR light spot well aligned to the pixel being addressed. The results show a peak in the response existing at 4 μm and a cut-off wavelength at approximately 6.7 μm, similarly to the spectral data obtained from the single pixel device. The sudden signal drop in the curve induced by CO_2 gas and water vapours can be observed in each pixel at approximately 4.2 μm and 5.7 μm. More importantly, the peak signal values of all pixels are very close to each other. A histogram showing the peak response of all pixels

at 4 μm is plotted in Fig. 7.6 for a better view on the excellent uniformity of the 4×4array.

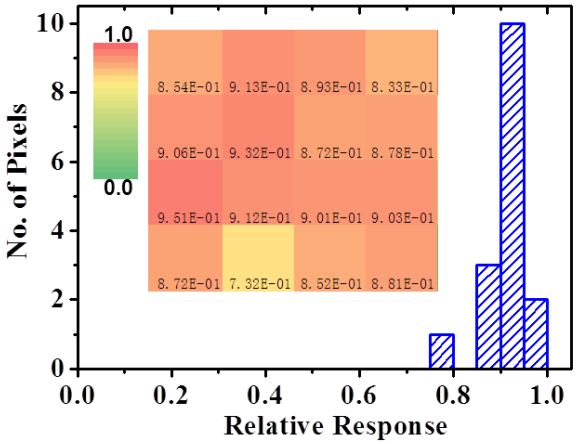


Fig.7.6. A histogram of the number of pixels in the 4×4 array showing their variation in peak photoresponse at 4μm. The inset figure shows a 4×4 heatmap plotting of the measured peak values.

Similarly, spectral photoresponse curves of all pixels in the 8×8 array device were also obtained. As shown in Fig. 7.7, the peak photoresponse of pixels in the 8×8 array spans a wide range in the histogram, indicating existence of non-uniformity and insensitive pixels. When using a response value of 0.4 as threshold, the yield of the 8×8 array is about 65% which still allowed imaging tests to be carried out. The lower yield in the 8x8 array was due to problems encountered during fabrication, which affected an entire row of the array, which had to be disconnected during the characterisation. As only one 8×8 array device was completed and tested, a significantly improved performance and yield can be expected in future batches.

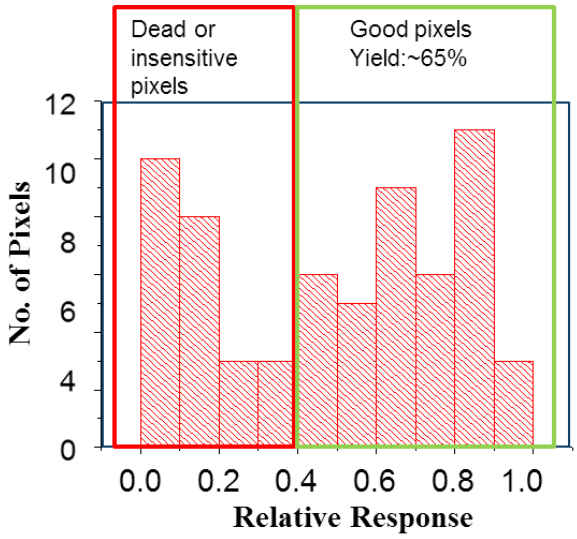


Fig.7.7. A histogram of the number of pixels in the 8×8 array device showing their variation in the peak photoresponse at 4μm.

7.2.2 Responsivity & Detectivity

As described in Sec. 4.3.2, the responsivity of the fabricated arrays to the 4.57μm mid-IR light was measured using a Hamamatsu QCL laser system. Initially, the emitted laser power levels under various biasing conditions were measured by a commercial power meter based on a thermal IR detector (S401C from Thorlabs). Due to the high beam divergence of the QCL, the power meter was placed as close as possible to the output window of the laser in order to measure as accurately as possible the total power of the emitted mid-IR light. Then, the input current was gradually increased while recording the power value read from the power meter. As a result, the power-current characteristics of the mid-IR QCL source with different cooling temperature applied could be obtained, as Fig. 7.8 shows. These data were particularly useful for extracting the value of incident power received by photodetectors fabricated in this work using Eqn. 4.4.

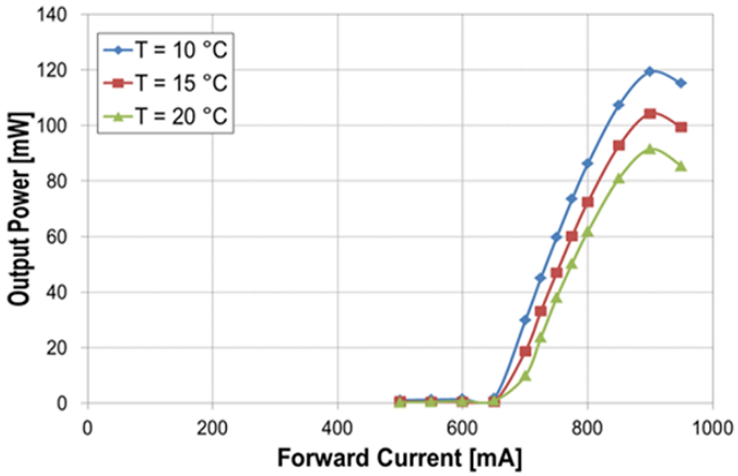


Fig. 7.8. Output power versus input current curve of the Hamamatsu mid-IR QCL.

Having a method to extract the incident power according to the applied input current, responsivity of the 4 × 4 array was then measured. Throughout the measurements the temperature of the QCL was maintained at 10 ℃, while the sensitivity of SR570 pre-amplifier was set to 10μA/V. A series of 4×4 images was then captured, each corresponding to a value laser input current, with values ranging from 650mA to 850mA. Each of the images consisted of the signal voltage values of all the sixteen pixels. As a result, the average of acquired signal voltages of all 16 pixels in the array could thus be plotted as a function of the incident light power (see Fig. 7.9(a)). From the slope of the curve a responsivity of approximately 5000 V/W or 50mA/W at 4.57 μm was extracted. The corresponding value of effective quantum efficiency was calculated to be approximately 1.5 %. It is worth to mention that, the effective quantum efficiency

calculated here arises from the whole circuit that takes into account signal drop due to co-integrated switching transistors and the multiplexers. The intrinsic de-embedded quantum efficiency of the photodiode is approximately 30%. Such a value is consistent with previously reported InSb photodiodes. More details regarding the signal loss due to the readout circuit are given in Appendix IV.

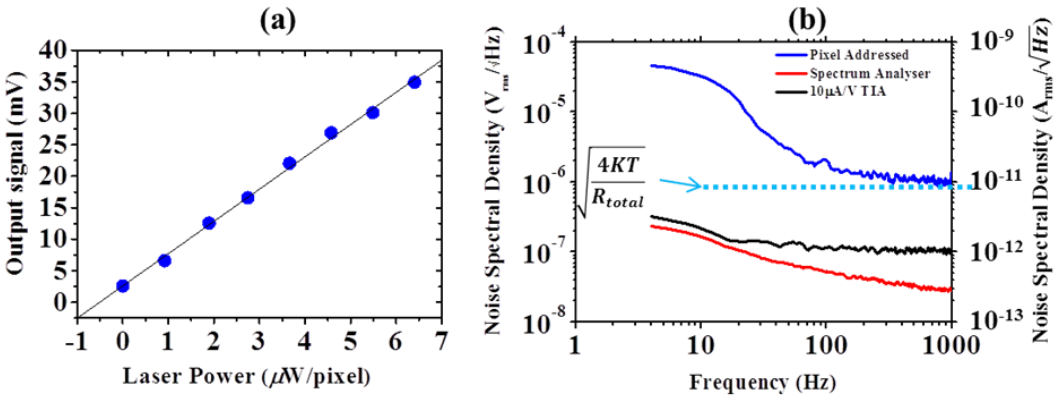


Fig. 7.9. (a) Averaged responsivity of all 16 pixels in the 4×4 array, with laser illumination at 4.57 μm. (b) Noise spectrum, measured with the spectrum analyser without input signal (red), with only the SR570 pre-amplifier connected to the analyser (black), and finally with the amplified signal from the pixel being fed to the analyser (blue).

Noise measurements were also performed, by feeding the SR570 amplifier output to an Agilent 4440A spectrum analyser. First the noise density of the spectrum analyser and of the SR570 pre-amplifier were both measured individually so that the noise contribution coming from the pixels themselves could be extracted. The noise spectral density of a selected pixel from the 4×4 array was subsequently measured. Fig. 7.9(b) shows all the curves obtained from the noise characterisation. It can be seen that the 1/f component dominates as source of noise in the pixel at low frequencies. The noise plateaus at frequencies greater than 100 Hz, where a noise density of 1.2×10^{-6} V/Hz$^{1/2}$ can be achieved. According to Eqn. 3.26, this yields a NEP value of 2.4×10^{-10} W/Hz$^{1/2}$. As a result, specific detectivity (D*) of the pixel at the illumination wavelength of 4.57 μm is calculated as 6.25×10^{7} cmHz$^{1/2}$W^{-1} using Eqn. 3.27, with the active area of the pixel equal to 150×150 μm^2 (2.25×10^{-8} m^2). Again, this value is an effective value that takes into account the signal loss introduced by the whole readout circuit which includes the ON resistance of the multiplexer and the input impedance of the TIA. After de-embedding the data from the circuit, the D* of the InSb photodiode itself is found to be approximately 2.7×10^{8} cmHz$^{1/2}$W^{-1}, which is comparable to the best results previously reported [120, 121] (details are also given in Appendix IV).

7.2.3 Crosstalk & Scanning Speed

In order to measure the crosstalk of a FPA device, a highly collimated light source with a spot size smaller than the pixel pitch was required, so that only one pixel at a time would be illuminated. Due to the lack of appropriate collimation and focusing optics for the Hamamatsu QCL source, a 1.61 μm laser (Agilent 81940A) system was used instead. At this shorter wavelength widely available borosilicate optics could be used and a spot size as small as $0.1mm^2$ could be readly achieved, which is well below the 400 μm ×400 μm pixel pitch. As shown in Fig.7.10, when 5 mW of continuous wave (CW) laser emission at 1.61 μm was collimated and shone upon the array devices, the real-time scanned intensity graph showed a bright white pixel, indicating the relative position of the focused laser spot. By maximising the signal level, the laser spot could be finely aligned to the sensing area of any pixel of interest. Finally, the voltage levels acquired from all neighbouring pixels were used for calculating the crosstalk.

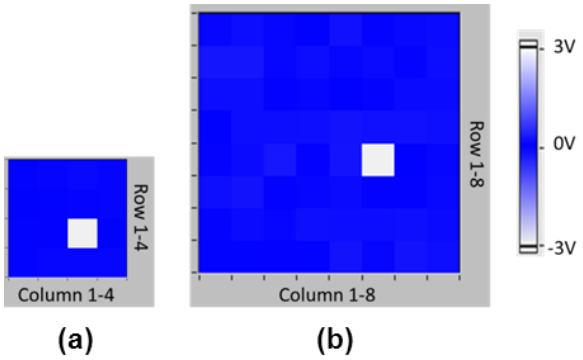


Fig. 7.10. Real-time scanned intensity graphs (images) taken from the (a) 4×4 array and the (b) 8×8 array when illuminated by a highly focused and collimated1.61 μm laser light.

Fig. 7.11 shows the voltage levels readout from all pixels in the 4×4 array in the absence of illumination (Fig. 7.11(a)), and when the laser light is shining on two distinct positions (Fig. 7.11(b) and (c)). The crosstalk is calculated by dividing the voltage level obtained from the neighbouring pixels by the voltage level obtained from the illuminated pixel. For a clearer view, a 3D bar chart plot of the calculated crosstalk is also shown in Fig. 7.11. As apparent from the charts, only a very small crosstalk, with a value <1%, was observed for the pixels in immediate proximity of the illuminated pixel. Such a value is rather small compared to the dark noise level, from which it can be indistinguishable at times. The results support the discussion given in Sec.3.3.2, that the electrical crosstalk can be significantly suppressed if a large ON/OFF resistance ratio of the switching MESFETs is achieved after the device fabrication. The residual crosstalk

is most likely to be introduced by backside reflection of the incident light from the substrate.

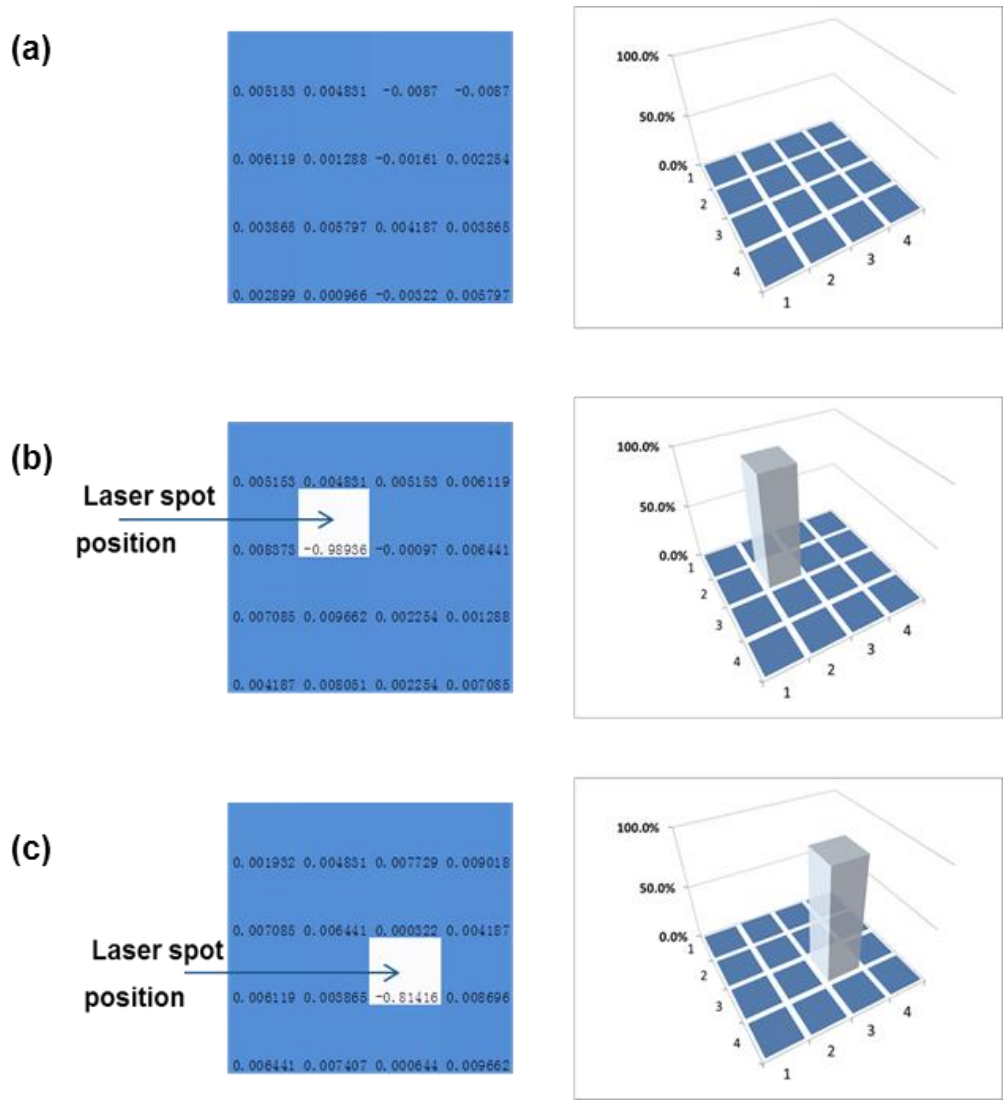


Fig. 7.11. The measured signal level and calculated crosstalk of the 4×4 array with (a) no illumination (b) laser spot focused at 2nd row and 2nd column and (c) laser spot focused at 3rd row and 3rd column.

The characterisation at 1.61 μm also looked at the signal dependence on the image scanning rate. Fig. 7.12 shows the obtained signal voltage value of an illuminated pixel when scanning the 4×4 array with various frame rates. The results showed a small drop in signal voltage when the scanning rate was increased from 10fps to 40fps, whereas negligible signal loss was observed once the scanning rate increased beyond 40 fps to 80 fps. This implies that the current scanning speed is still far from the maximum limit of the current imaging system setup. However, higher scanning rates were not applied in order to avoid potential damage to this 4×4 array device, in order to use it for the following imaging tests. Additionally, as shown in Fig. 7.13, it can be seen that the

scanning speed did not obviously affect the measured crosstalk in between pixels, further proving good suppression of the electrical crosstalk in the fabricated arrays.

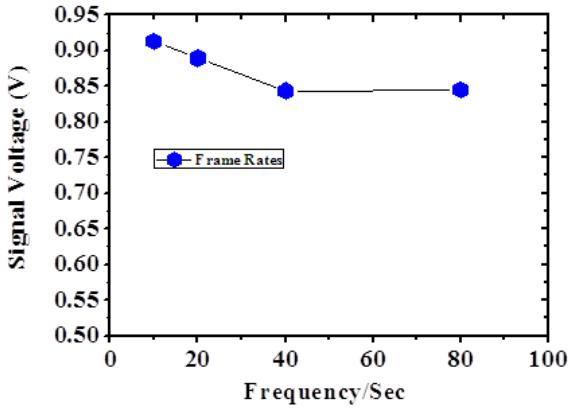


Fig. 7.12. Signal voltage dependence on the scanning speed of a 4×4 array, showing that an increase in the frame rate from 10 to 80 frames per second causes only a little bit signal loss and thus the maximum speed limit of the device is not yet arrived.

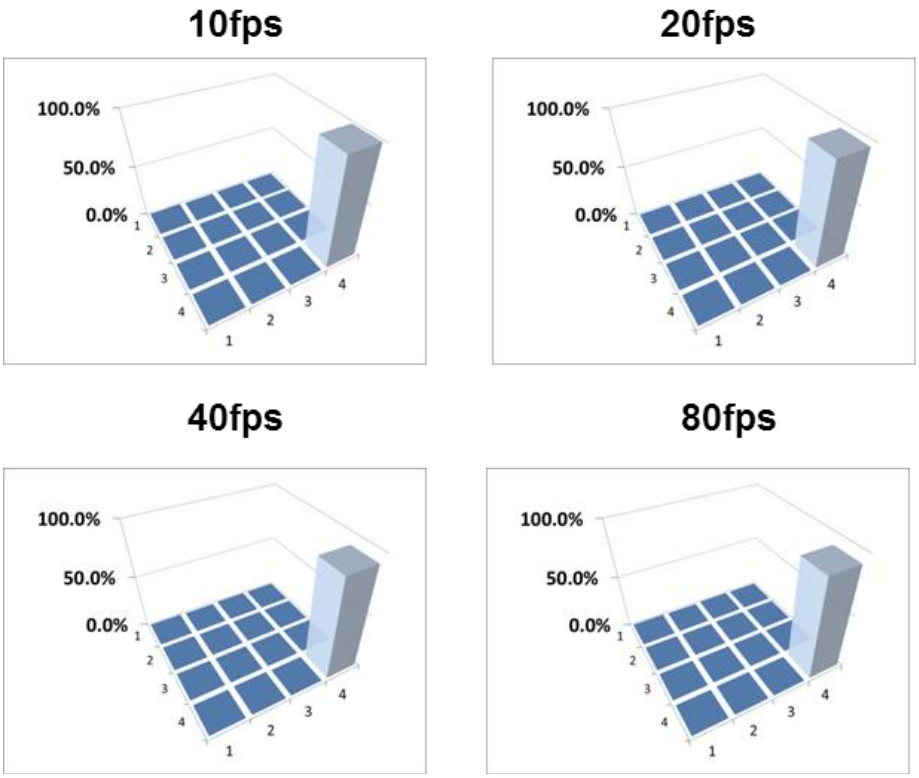


Fig. 7.13. Calsulated crosstalk of the 4×4 array with various scanning speed applied.

7.3 Real-time Mid-IR Imaging

7.3.1 Mid-IR Shadow mask Imaging

After obtaining the most important figures of merit for the fabricated arrays, imaging experiments were carried out, as obtaining images of an object was the most direct way to demonstrate that the monolithically integrated GaAs-based readout circuits were scanning and extracting the photo-generated carriers from each pixel in the

right sequence. For this purpose, the QCL system that was used to characterise the responsivity of the devices was used as a mid-IR source, aimed at obtaining projected images of a shadow mask.

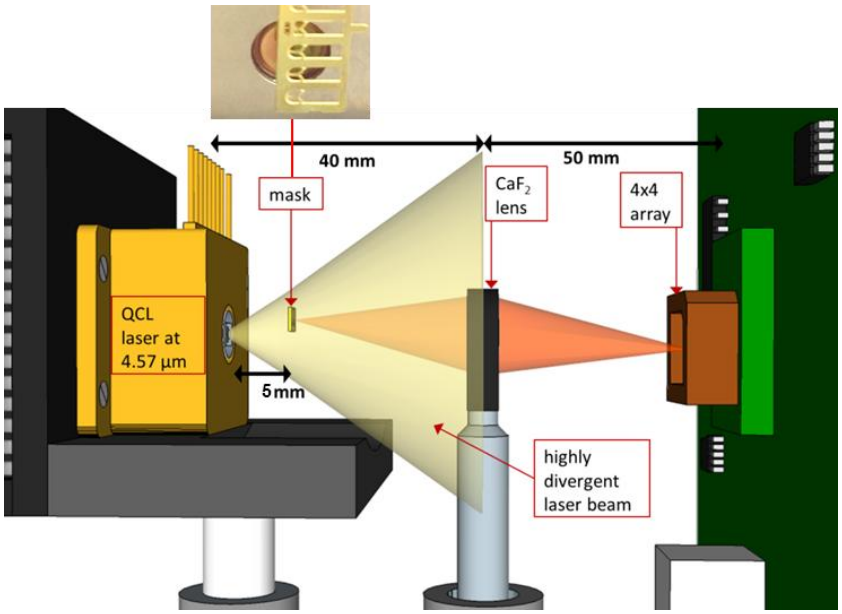


Fig. 7.14. Schematic of the experimental set-up used to carry out the shadow mask imaging experiments.

Fig. 7.14 illustrates the experimental set-up used for shadow mask imaging. As previously mentioned (see Sec. 4.3.2), the QCL source was not collimated, and its highly divergent emission meant that the laser light could be treated as a single point mid-IR light source. However, in order to at least partially focus the widely dispersed mid-IR light and carry out projection imaging, a CaF_2 lens (1/2 inch diameter, focal length f=20mm) was aligned and placed 40mm away from the QCL source. A shadow mask object— a piece of thin metal presenting a Y-shaped pattern, was placed 5mm away from the QCL source and thus at a distance u=35mm before the CaF_2 lens. Note that, although not shown in Fig.7.14 for simplicity, the shadow mask object was attached to a XY translation stage so that its position could be precisely controlled. The 4×4 array, mounted in the previously mentioned driving circuit board, was placed beyond the lens at a distance v=50 mm. This position approximately corresponded to the plane where the image of the shadow mask would be formed according to the thin lens equation (1/u+1/v=1/f).

As the pixel number of the prototype arrays is limited, to 4×4 in this case, only a small part of the shadow mask shape could be imaged with a single image capture. In order to form a more informative image with higher resolution, the shadow mask was mechanically scanned: every image capture with the 4×4 array was followed by a precise movement of the shadow mask along either the X or Y direction before

capturing a new image. Each scanning step of the shadow mask was chosen to produce a shift of the projected image corresponding to the size of the array sensing area along the direction of movement. For the 4×4 array device, which had a pixel pitch of 400 μm, the required shift was 1.6mm corresponding to a mask scanning step of 0.8 mm. As a result, each of the captured 4×4 images represented unique imaging information from a distinct part of the object without overlapping in between. By using this scanning method, a 32×28 pixel image was obtained by combining 56 individually captured 4×4 images, and it is shown in Fig. 7.15, which also exemplifies the process of image combination. It can be seen that the composite image shows a clear Y-shaped pattern matching very well the profile of the shadow mask used.

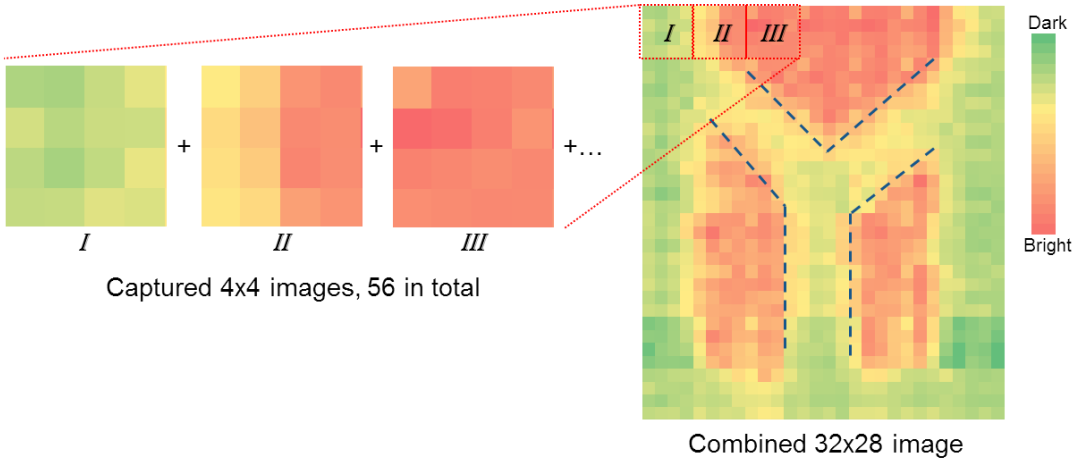


Fig. 7.15. A combined 32×28 image of the shadow mask obtained by scanning multiple images captured by the 4×4 array. Images I, II and III illustrate the image combination process.

7.3.2 FTIR Spot Imaging

As described in Sec. 4.3.1, the Bruker FTIR measurement system used in this work is equipped with a mid-IR globar source (peaked at 2.4 μm) and several reflective optic components to manipulate and reshape the emitted mid-IR beam. Therefore, direct imaging of the glow bar spot of the FTIR system was also carried out. During the experiment, the array device was placed at the focal point of the beam, where the spot size was at its smallest. In order to have a larger sensing area, this experiment was carried out using the 8x8 array which was mounted onto a XYZ translation stage to allow its precise positioning.

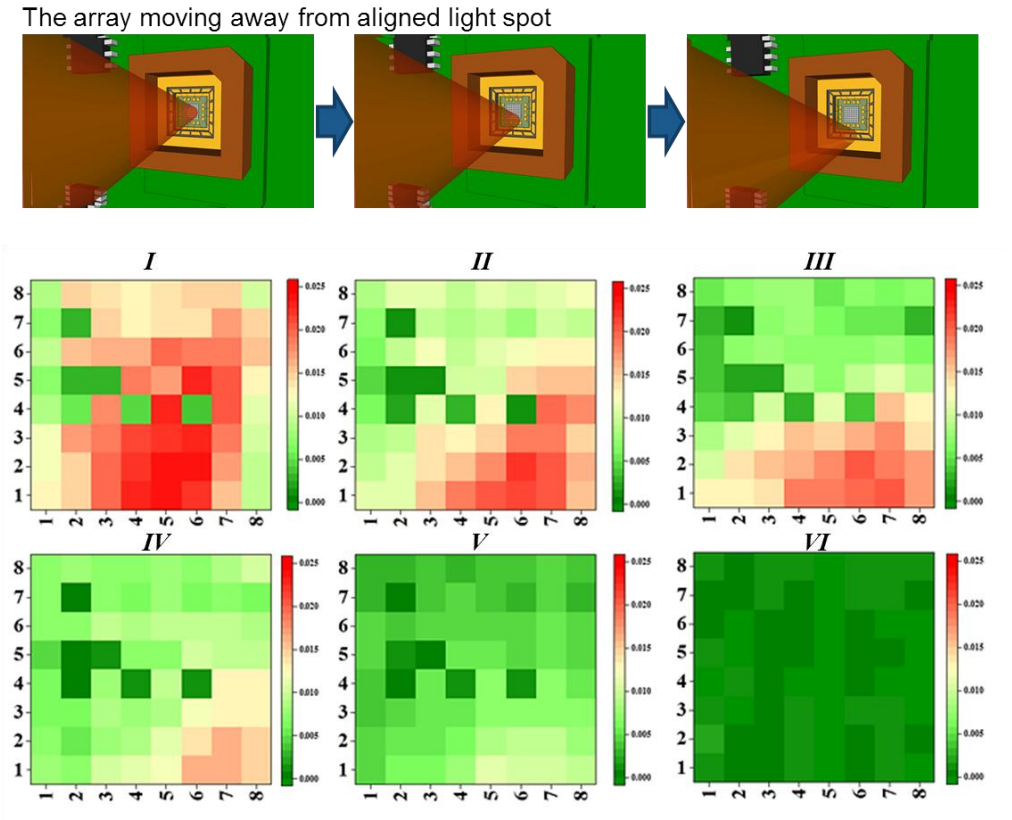


Fig. 7.16. Images of the FTIR glow bar source captured with the 8×8 pixel array. The images are taken in sequence, moving the array laterally away from the glow bar spot.

An image of the focused light spot could thus be obtained once the device was well-aligned to the focal point. Again, given the limited number of pixels and the low resolution, it is hard to illustrate the imaging capability with a single image capture. Therefore, while the array was kept in the focal plane of the beam, a set of images were taken: after obtaining the image of the aligned light spot, they array device was moved away from the spot, each time by 0.5 mm. As shown in Fig.7.16, the spot of mid-IR light was indicated in the obtained images by red pixels. As the spot gradually leaves the sensing area of the device, the red pixels can be seen shifting position and moving towards the bottom right area of the array. Eventually, when the mid-IR light spot is not illuminating the device any more, the array displays a dark scene, showing as dark green in the corresponding image.

7.3.3 Real-time CO_2 Plume Detection

Finally, in order to demonstrate the potential gas plume imaging application of the fabricated array devices, a simple test involving CO_2 gas was conducted. As the experimental set-up is shown in Fig. 7.17, and it includes a SiC blackbody source the emission of which spanned wavelengths from 500nm to 9000nm. In order to match the specific absorption peak of the CO_2 gas in the mid-IR region, a narrow (200 nm FWHM)

pass-band optical filter centred at 4.25 μm was applied to the blackbody source. Finally, the filtered light was shone upon the 4×4 array based imaging system, while the developed LabView program was used to monitor the photo-generated signal levels in real-time.

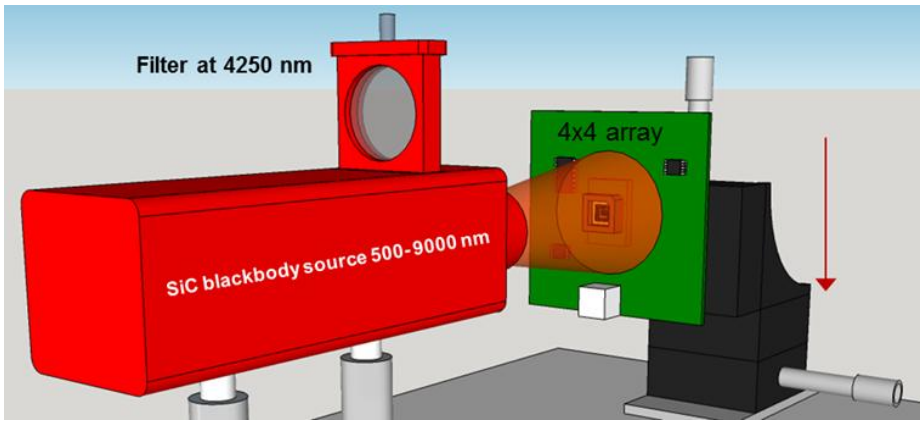


Fig. 7.17. Schematic of the experimental set-up used to carry out the real-time CO_2 spray detection experiments.

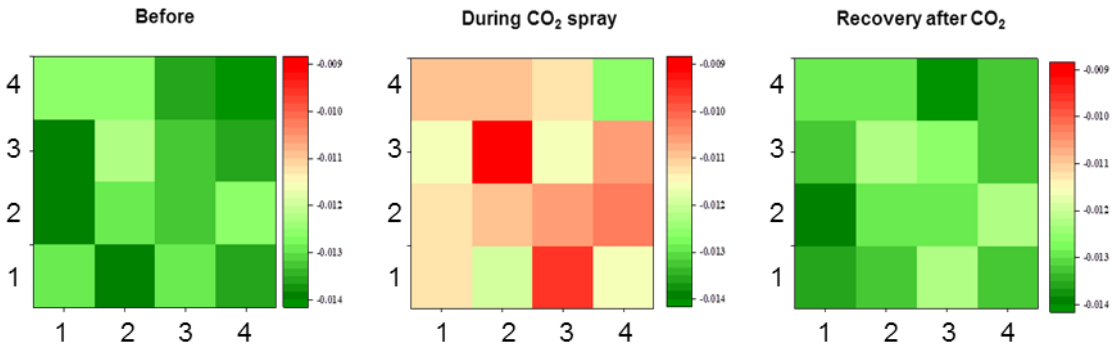


Fig. 7.18. Obtained 4×4 image captures showing the clear signal change once the valve of CO_2 gas is turned on.

As shown in Fig. 7.18, despite most of the emitted power from the SiC light bulb being blocked by the 4.25 μm filter, the 4x4 array was sensitive enough to detect the filtered mid-IR light. The gas plume imaging test was carried out by using a small disposable bottle of CO_2 to spray concentrated gas between the blackbody source and the array. As the colour in the corresponding images indicates, once the gas valve on the CO_2 disposable bottle was opened, a clear drop of the signal level in all pixels can be captured. More importantly, once thevalve was closed and the CO_2 concentration gradually returned to standard atmospheric levels, the obtained image showed a recovery in the level of the signal recorded.

7.4 Summary

In this chapter, real-time mid-IR imaging systems based on the fabricated 4×4 and 8×8 prototype array devices were presented. First the developed real-time data acquisition method was described. On a circuit board, standard off-the-shelf multiplexers and decoders were grouped together with the wire-bonded array devices to implement the X-Y addressing strategy. Labview programmes, running on a laptop, were also developed to control the addressing and readout photo-generated signals through a DAQ product.

The chapter continued with a discussion of the most important figures of merit of the array devices. By obtaining spectral response of every single pixel in the array, the 4×4 array device was found to have excellent response uniformity to the mid-IR light. The uniformity of 8×8 array device was not as good due to fabrication issues, however it still proved suitable for imaging tests. According to the measurements carried out with a mid-IR QCL light source, the average responsiviyy of a pixel in the 4×4 array yielded a value of approximately 5000 V/W (or 50mA/W) at 4.57 μm. Together with the measured noise density at frequencies greater than 100 Hz, specific detectivity (D*) of the pixel was calculated as 6.25×10^7 $cmHz^{1/2}W^{-1}$. De-embedding the data from the readout circuit, the D* of the InSb photodiode itself is found to be approximately 2.7×10^8 $cmHz^{1/2}W^{-1}$. Such value is comparable to the best results reported in earlier works. Additionally, the crosstalk in between the illuminated pixel and the neighbouring pixels was also assessed, and found to be minimal and independent of the scanning speed. Up to 80 fps scanning rate was readily achieved, and it is believed to be still far from the maximum limit of the fabricated switching transistors in the array.

The imaging capability of the arrays was finally proved by a series of imaging tests. First, projection imaging of a Y-shaped shadow mask was demonstrated. By applying a mechanical scanning method, a composite image with increased pixel number and resolution was obtained with the 4×4 array, displaying a clear Y-shaped profile matching the mask well. A similar imaging experiment was also carried out using the 8×8 array, used to capture the shifting position of glow bar source in the FTIR system. Finally, the imaging system based 4×4 array demonstrated the capability of CO_2 gas plume imaging in real-time, which further confirmed the potential applications of the devices developed in this work.

8. Conclusions and Future Work

8.1 Conclusions

This work has been focused on the implementation of a compact, cost-effective focal plane array of active pixels for imaging in the mid-IR range without the need for flip-chip bonding to a CMOS readout chip. Upon finishing, a novel monolithic integration approach has been designed, realised and demonstrated for the first time.

This approach is based on the heterogeneous growth of GaAs MESFET and mid-IR photodetector active layers on a S-I GaAs substrate, so that the light detection and the signal readout functions can be realised independently in the fabricated devices. This means that, differently from all the previously reported monolithic mid-IR imagers, this newly developed approach supports optimisation of detector structures and ROICs separately. Almost all state-of-the-art mid-IR photodetectors with room temperature operating capability can therefore be integrated using this approach, without the need to implement transistors on a narrow bandgap material.

With optimised MBE, growth of either an InSb non-equilibrium photodiode structure or an InAsSb nBn photodetector structure on top of the GaAs active layers were both proved to be achievable. A sequence of successful process steps was developed in order to achieve independent fabrication of a mid-IR sensitive photodetector and a GaAs MESFET side-by-side on the surface of the sample. This included highly controllable etching processes which allow selective exposure of the underlying GaAs active layers with great uniformity. Also, by developing a low thermal budget GaAs MESFET fabrication process based on the Pd/Ge/Au Ohmic contact system, device fabrication was achieved without exceeding 180 ˚C and thus no thermally induced performance degradation was observed. Furthermore, metal interconnections between devices were realised by applying a polyimide based planarisation process, necessary for the formation of a complete readout circuit to overcome the extreme non-planarity of the sample.

The above mentioned processes were first used to fabricate and test single photo-pixel devices which included mid-IR photodetectors interconnected to the GaAs MESFET. The InSb-based photo-pixel showed typical sensitivity in the 1.3 μm to 6.7 μm wavelength range, whereas the InAsSb device presented comparable photoresponse in the 1.1 μm to 4.5 μm wavelength range. In both case, the absorption

lines for atmospheric CO_2 and H_2O were clearly visible at room temperature. More importantly, in a complete photo-pixel device the photocurrent was proved to be switchable by switching off the co-integrated MESFET. A switching time with T_{on} = ~30 μs and T_{off} = ~15 μs, respectively, was achieved, meeting the timing requirements for realisation of a 64×64 array device with >30fps scanning rate.

For proof of concept, monolithically integrated InSb-based arrays with 4×4 and 8×8 pixels were fabricated. Based on these prototype array devices, a mid-IR imaging system was then realised, which included driving circuits and programmes to conduct real-time data acquisition. The optical characterisation results obtained with the imaging system confirmed that the InSb-based array devices were sensitive to mid-IR photons at room temperature, and that the photoresponse of the 4×4 array presented excellent uniformity. Further measurements of the responsivity and the noise density of the most responsive pixel addressed from the 4×4 array yielded aneffective D* value of 6.25×10^7 $cmHz^{1/2}W^{-1}$ at frequency >100Hz, whereas the corresponding intrinsic de-embedded D* value is 2.7×10^8 $cmHz^{1/2}W^{-1}$. Such value is comparable with the best reported performance of InSb-based detector-only devices working at room temperature. Also, the crosstalk in between an illuminated pixel with its neighbouring pixels was found to be minimal and independent of the scanning rate. Finally, a series of real-time mid-IR imaging tests, which included shadow mask projection imaging, globar spot imaging, and CO_2 gas plume imaging, were successfully demonstrated, proving the great imaging capability of these monolithically integrated antimonide-based arrays.

8.2 Future Work

Having confirmed that the fabricated prototype devices are suitable for imaging at mid-IR wavelengths, a large number of further developments could be conducted in the future which are listed in the following:

1. Implementation of larger format arrays with the developed processes

As described in Chapter 7, the pixel number in the current prototype pixel arrays is too small to obtain a high resolution, informative image without complicate mechanical scanning and data reconstruction. Given all of the characterisation results obtained from the single photo-pixel devices support realisation of much larger arrays, the first future development efforts can be focused towards fabrication of a device with 64×64 pixels (common entry-level for a commercial IR imager). In order to achieve this, the main

task is scaling the current pixel pitch from 400 μm to ~100 μm, so that such a large number of pixels can be fabricated within a reasonably small sample area, highly desirable in terms of material cost. In fact, as mentioned in Chapter 5, scaling of the pixel pitch has been proved achievable with the developed processes. As a result, the 64×64 array device is now under development in our research group.

2. Further optimisation of the design and fabrication processes of the transistors

Despite their excellent switching behaviour, there is still room for improving the performance of current GaAs MESFETs. First of all, efforts could be made to find out optimal values of Gate length and width for the transistors in terms of ON/OFF resistance ratio, switching speed and fabrication yield. Moreover, one can also develop highly controlled dry etch-based gate recess etching processes to replace the current iterative wet etching approach, thus significantly reducing the fabrication complexity. Furthermore, other than MESFETs, it is also worth investigating ways to integrate with many other GaAs based transistors such as MOSFET [207], and heterostructure FET [208]. Both can contribute to a significantly suppressed gate leakage current, and potentially have the ability for implementation of circuits with more functions such as multiplexing and pre-amplifying.

3. Investigating alternate detector structures for better performance and multi-colour imaging capability

Similar to the flip-chip bonding based hybrid design, the monolithic approach developed in this work allows separate optimisation of transistors and detectors. Therefore, alternative photodetector layer structures can be easily applied, improving the detection performance at high operating temperatures. In this work, the InAsSb-based nBn photodetector grown by the IMF technique presented very promising results at room temperature. Further integration of this detector with a GaAs MESFET has led to successful demonstration of a switchable pixel device. A dramatically improved detection performance can be expected once the current fabrication process is slightly amended to deliver a working array device based on this nBn structure. Type II InAs/GaSb superlattices, the growth of which has being recently proved with high quality on GaAs substrates, can also be investigated [145]. As described in Chapter 2, with the capability of tuning the bandgap by changing the corresponding layer thickness, multi-colour function could also be included in this newly developed monolithic approach.

4. Enhancement by integration with photonic techniques

Additionally, photonic techniques have offered another playground for improving the detection performance of fabricated arrays. For example, current monolithic design yields a relatively low fill factor, which can be improved by forming a micro-lens on top of each photodiode in the array to help concentrate the incident light to the active sensing area and hence increase the responsivity. Moreover, by fabricating the photodiodes into photon crystal structures, light trapping process can be triggered resulting in higher quantum efficiency as compared to standard detectors with same material volume [128]. Finally, surface plasmonic filters, as developed in our group [209], could also be integrated to provide a filtering function in the mid-IR range.

Appendix I

Additional Information on Wet Chemical Etcthing Processes

InSb Mesa Etching

Fig.A1.1 illustratesthe great improvement of the mask adhesion by introducing the HCl:H_2O based de-oxide process right beforeresist spinning steps.It is clear that, without applying this surface preparation process, the citric acid based wet etching process does not support definition of mesa sizes smaller than ~40 μm. In contrast, after applying the de-oxide process, very small mesas down to ~15 μm can be readily defined without unexpected lateral erosion.

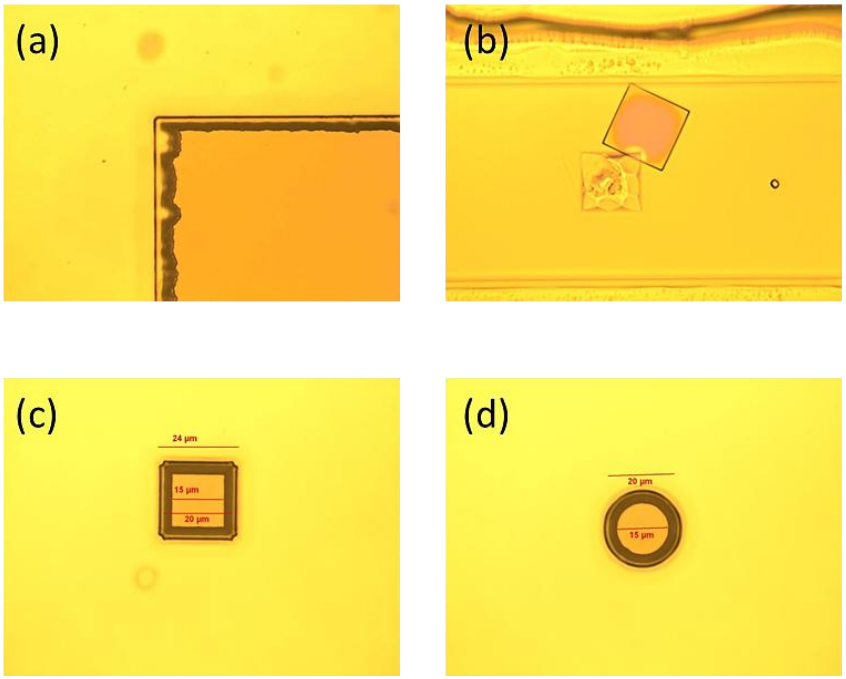


Fig. A1.1. Micrograohs of (a) (b) InSb mesas etched with standard resist preparation process.(c)(d) Micrograohs of small mesas with size down to 15μm, both were defined using the amended mask preparation process as described in Sec. 5.2.1.2.

GaAs Mesa Etching

Various kinds of chemical etching solutions weretestedin this work to achieve the device isolation etch as described in Sec 5.4.1. As shown in Fig. A1.2 and A1.3, these include H_2SO_4-based, citric acid-based and H_3PO_4-based etching solutions. Sloped sidewall profile indepent of the crystal orientation can only be achieved when using H3PO4:H2O2:H2O (3:1:50)etchant. It thus allows metal pads covering the etched mesa

edges without breaking. Fig. A1.4 indicates that minimising the agitation or stirring during this wet etching process is critical.

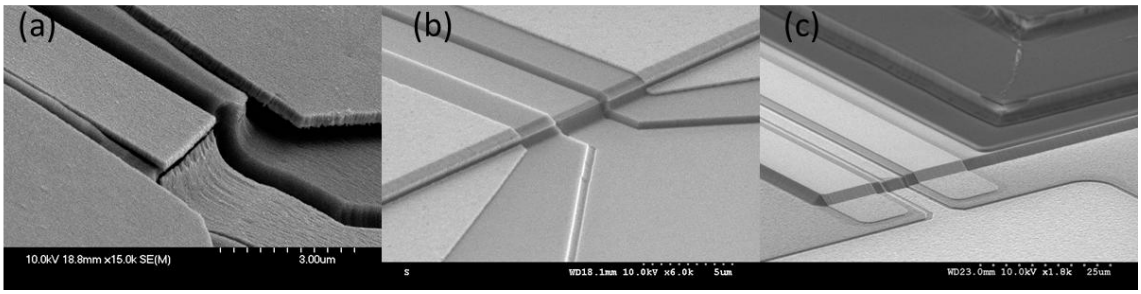


Fig.A1.2.SEM pictures of GaAs mesas etched with (a) H_2SO_4:H_2O_2:H_2O=1:1:10 (b) Citric acid:H_2O_2= 50:1 (c) H_3PO_4:H_2O_2:H_2O=3:1:50 etching solutions.

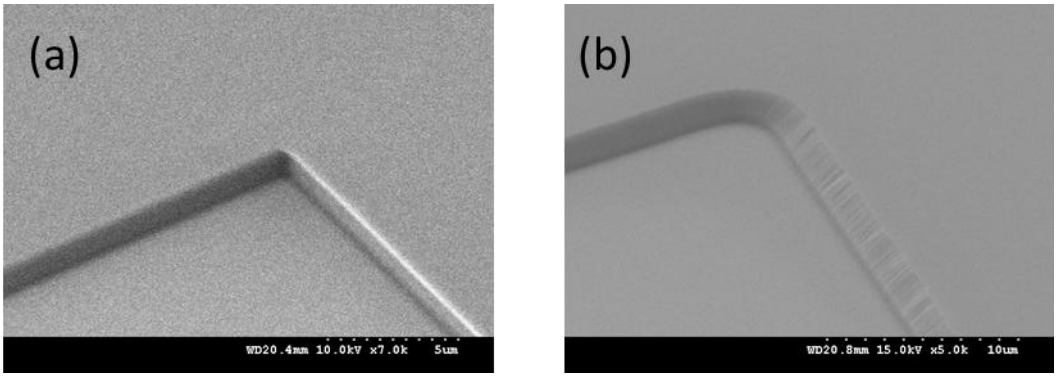


Fig.A1.3. GaAs mesa sidewall profile etched with (a) H_3PO_4:H_2O_2:H_2O=1:4:45 and (b) H_3PO_4:H_2O_2:H_2O=3:1:50 etching solutions.

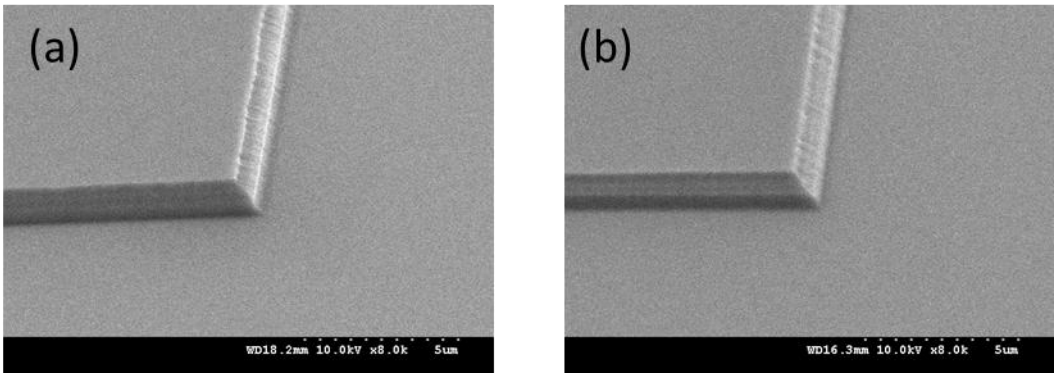


Fig.A1.4. GaAs mesa sidewall profile etched with H_3PO_4:H_2O_2:H_2O=3:1:50 solution, (a) with and (b) without agitation/stirring.

Optimization of InSb Dry Etch for Device Scaling

Summary of Tested Parameters

Etch test ID	Mask material	$CH_4/H_2/Ar$ sccm	Pressure mT	Table Temperature ℃
D01	ICP-deposited SiNx	15/50/5	7.5	100
D02		15/50/5	7.5	110
D03		15/50/5	7.5	120
D04		12/40/4	7.5	110
D05		12/40/4	12	110
D06		12/40/4	15	110
D07		9/36/3	7.5	110
D08		9/36/3	12	110
D09		9/36/3	7.5	No cooling
D10	Hard baked HSQ	9/36/3	7.5	110
D11	Hard baked AZ4562	9/36/3	7.5	110
D12		12/40/4	7.5	110
D13		12/40/4	15	110
D14		15/50/5	15	110
D15		15/50/5/0.1(N_2)	15	110

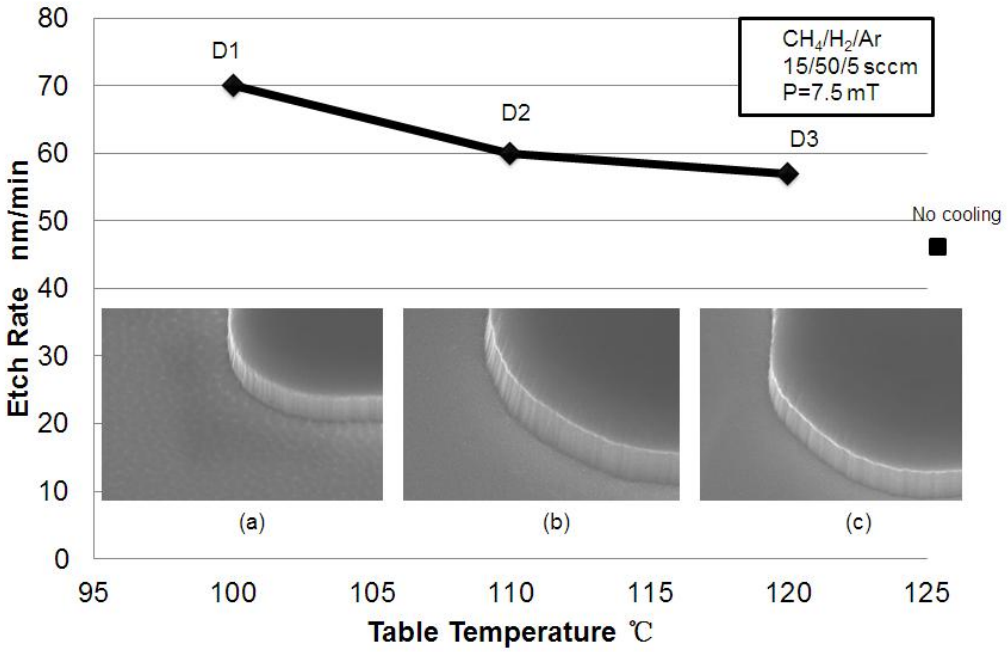


Fig.A1.5. Effect of table temperature on the etch rate and surface condition (a) 100 ℃,(b) 110 ℃,(c) 120 ℃

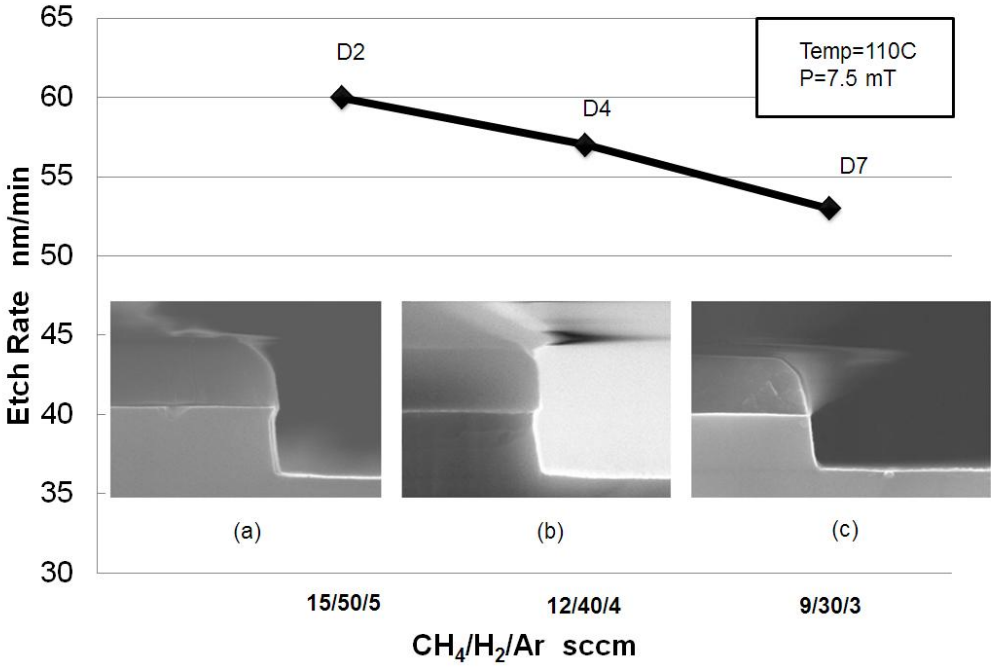


Fig.A1.6. Effect of gas dilution on the etch rate and sidewall profile (a) 15/50/5 sccm,(b) 12/40/4 sccm,(c) 9/36/3 sccm

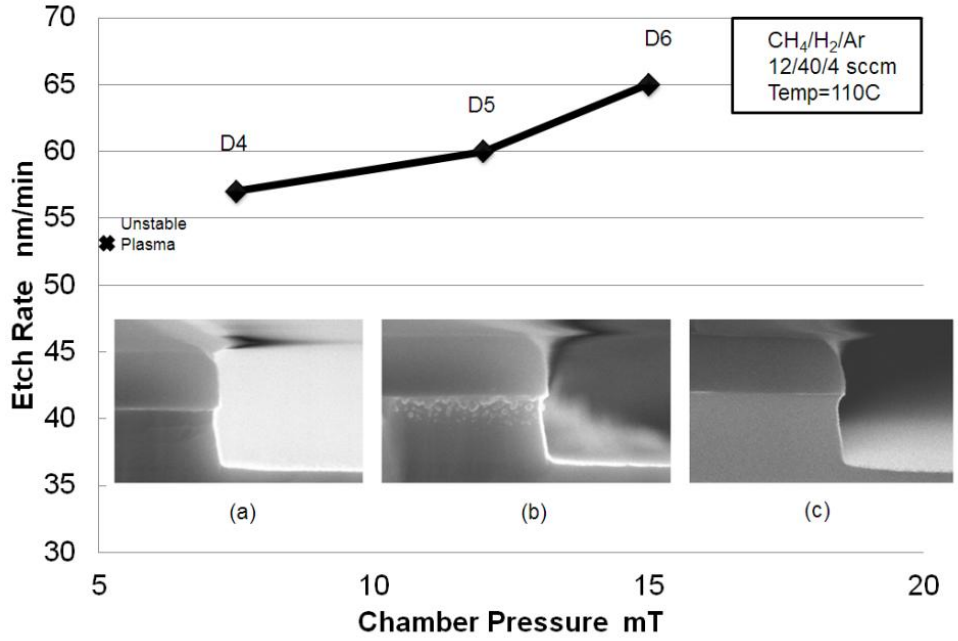


Fig.A1.7. Effect of chamber pressure on the etch rate and sidewall profile (a) 7.5 mT,(b) 12 mT,(c) 15 mT

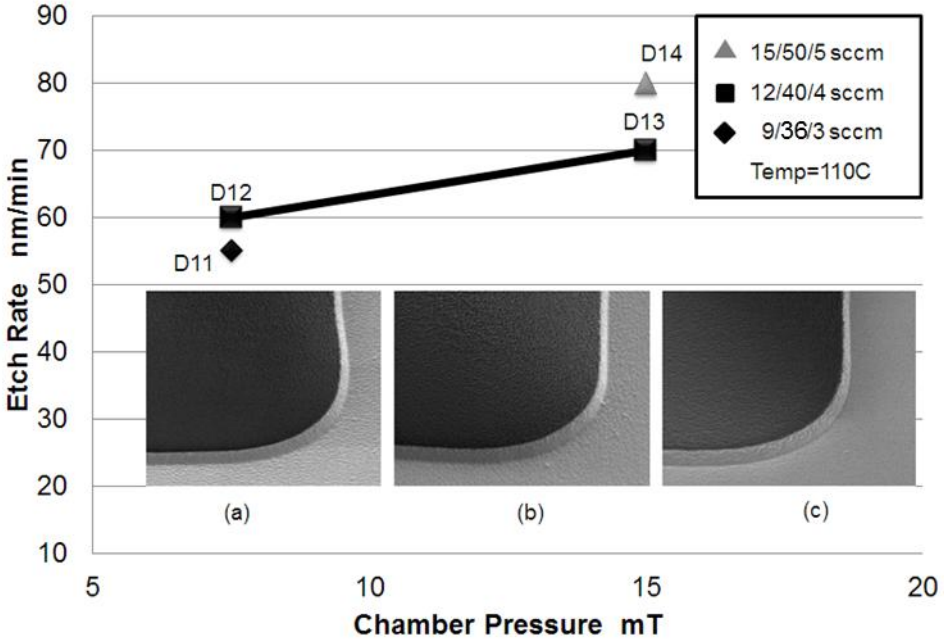


Fig.A1.8. Etch results of photoresist masked samples

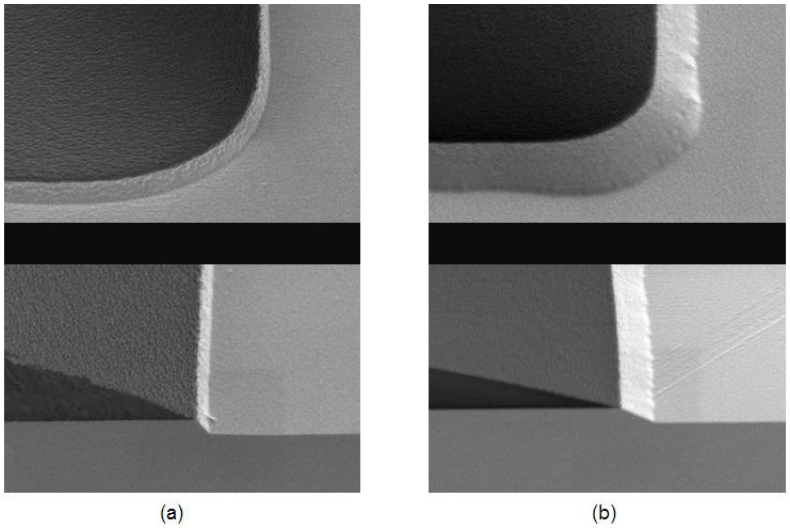


Fig.A1.9.SEM pictures of samples etched in (a) $CH_4/H_2/Ar$ chemistry (D14), (b) $CH_4/H_2/Ar/N_2$ chemistry (D15)

Appendix II

Low Temperature Annealed Ohmic Contact to n-type GaAs

As shown in the table below,CTLM sturctures were fabricated with a series of metal layer structures. These samples were all annealed in the 180℃ oven for 1hr followed by measuring the resistivity with methods decribed in Sec. 4.2.3. An optimized thickness of Pd/Ge/Au is found to be approximately equal to 10nm/40nm/100nm, which agrees well with the reported results [189]. Fig.A2.1 shows diffustion of the top Au layer into the underlying Ge layerwhich leads to reduction oftotal contact resistane after annealing. Therefore, a better control of this diffusion process can contribute to a lower Ohmic resistivity. This is proved by introducing the "superlattice like" structure in this work. The results demonstrate great potential to further improve the resistivity of Pd/Ge/Au based low temperature annealed Ohmic contacts.

Summary of Tested Metal Layer Structures

	Pd	Ge	Au	Ge	Au	Ge	Au	Ge	Au	Ge	Au	Type	Ar Clean	Total (nm)	Resistivity (Ohm cm2)
M1	5	30									100	Normal	N	5/30/100	2.65E-06
M2	5	50									100	Normal	N	5/50/100	6.67E-06
M3	5	10	2	5	2	5	2	5	2	5	120	SL	N	5/30/128	3.63E-06
M4	5	10	2	5	2	5	2	5	2	5	90	SL	N	5/30/98	2.41E-06
M5	10	40									100	Normal	Y	10/40/100	9.34E-05
M6	10	40									100	Normal	N	10/40/100	1.86E-06
M7	10	20	2	5	2	5	2	5	2	5	90	SL	N	10/40/98	1.24E-06
M8	10	15	2	5	2	5	2	5	2	5	90	SL	N	10/35/98	4.86E-06
M9	10	30	2	5	2	5	2	5	2	5	90	SL	N	10/50/98	3.81E-06
M10	2	5	2	5	2	5	2	5	2	5	90	SL	N	2/25/98	4.30E-05
M11	2	5	2	5	2	5	2	5	2	5	90	SL	N	2/25/98	4.70E-05

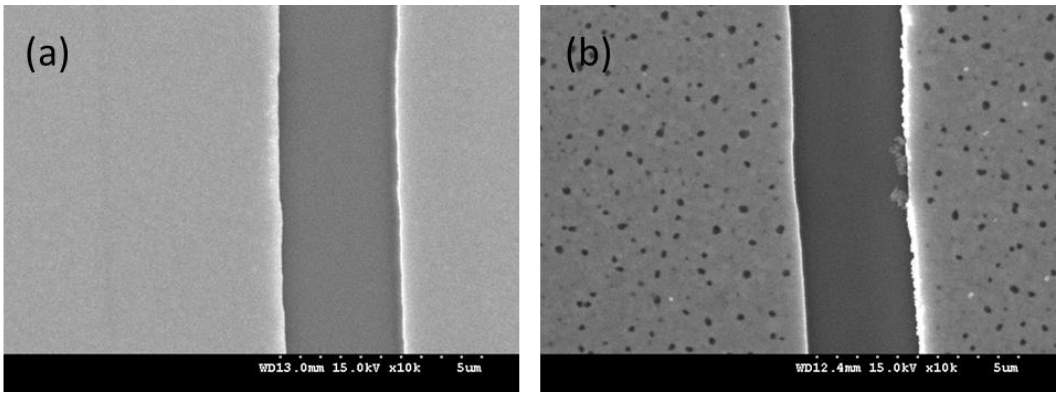


Fig.A2.1. Pd/Ge/Au based Ohmic contact metal stack (a) before and (b) after annealing in 180℃ oven for 1hr.

Appendix III

Detialed Fabrication Steps

- Sample Cleaning or Resist Stripping

-2hr SVC-14 → 5mins Acetone → 5mins IPA → 5mins RO water → N_2 dry

-O_2 ash for 1min30s @80W

- LOR+PMMA Resist Coating & Patterning

Spin coat:

-5mins oven bake @180^oC

-Spin LOR10A @5000rpm for 60s

-1hr oven bake @180^oC

-Spin PMMA 15% @5000rpm for 60s

-5mins hotplate bake @180^oC

-Spin PMMA 4% @ 5000rpm for 60s

-5mins hotplate bake @180^oC

Exposure:

-600 $\mu C/cm^2$, 64nA beam, VRU 33

Development:

-48s in 1:1 MIBK (23.3 ^oC) → 1min IPA rinse

-O_2 ash for 3mins @80W

-1min15s in MF319 → 5mins RO water rinse

-O_2 ash for 1min30s @80W

- S1818 Resist Coating & Patterning

Spin Coat:

-5mins hoteplate bake @ 118^oC

-Spin S1818 @4000rpm for 30s

-2mins hoteplate bake @ 118^oC

Exposure:

-13.5s MA6, Hard contact, Gap 40um

Development:

-90s in MF319 → 5mins RO water rinse

-O_2 ash for 1min 30s @80W

-Ti/AuAlignment Markers & Photodiode Ohmic Contacts

-Sample Cleaning

-LOR+PMMA coating& patterning

-1mins de-oxide in HCl:H_2O 1:4 → 5mins RO water rinse

-Ti 50nm/ Au 150nm evaporation in Plassys II or IV

-2hr in pre-warmed SVC-14 → lift-off

- InSb Mesa Etching

-Sample Cleaning

-1min de-oxide in HCl:H_2O 1:2 → 5mins RO water rinse

-S1818 coating& patterning

-Etching in Citric acid:H_2O_2:H_2O 11:1:7

(etch depth monitored by Dektek profiler or by colour changing of the surface)

-Resist Stripping

- ICP SiNx Deposition & Patterning

-Sample Cleaning

-1mins de-oxide in HCl:H_2O 1:4 → 5mins RO water rinse

-400nm SiNx deposited in ICP-CVD machine

-S1818 coating and patterning

-SiNx etch in RIE 80+ (monitored by interferometer)

- GaSb Buffer Layer Etching

-Sample Cleaning

-1mins de-oxide in HCl:H_2O 1:2 → 5mins RO water rinse

-1hr in MF319 with stirring

-Add over-etching in MF319 with hand stirring

- GaAs Device Isolation Etching

-Sample Cleaning

-S1818 coating and patterning

-8mins soak in H_3PO_4:H_2O_2:H_2O 3:1:50 without agitation

(monitored by Dektak profiler)

-Resist Stripping

- Formation GaAs Ohmic Contact

-Sample Cleaning

-LOR+PMMA coating and patterning

-1mins de-oxide in HCl:H_2O 1:1 → 5mins RO water rinse

-Pd10nm /Ge 40nm /Au 98nm (superlattice stack) evaporation in Plassys IV

-2hr in pre-warmed SVC-14 → lift off

-Sample cleaning

Annealing: (optional can be done during subsequent processes)

-Spin LOR 10A @5000rpm for 60s

(to isolate the sample from the air environment during annealing)

-1hr oven bake @180^oC

- GaAs Recess Etching

-Sample Cleaning

-LOR+PMMA coating and patterning

-Dip the sample in RO water (1drop DECON 90) → Citric Acid:H_2O solution (1 drop DECON 90) → Citric acid: H_2O_2 20:1 etchant → RO water rinse

-30s De-oxide in NH_4OH:H_2O 1:20 solution → 5mins RO water rinse

-Ti 20nm/Pt 30nm/Au 150nm evaporation in Plassys II

-2hr in pre-warmed SVC-14 → lift off

- Polyimide Planarization & Interconnection

Spin Coating:

-Sample cleaning

-VM651 Primer coating @500rmp for 5s

-1min hotplate bake @115^{o}C

-Spin PI2545 with ramped speed

@500rmp for 5s with 100 ramp

@4000rmp for 30s with 1000 ramp

Stop spinning with 1000 ramp down

-16mins hotplate bake @150^{o}C

Via hole etching (wet):

-Spin PMMA 15% @5000rpm for 60s

-7mins hotplate bake @150^{o}C

-Spin PMMA 2.5% @5000rpm for 60s

-7mins hotplate bake @150^{o}C

-Exposure with 600μC/cm^{2} , 64nA beam, VRU 33

-48s development in MIBK:IPA 1:1 solution → 3mins O_2 ash @80W

-2-4mins soaking in MF319 without agitation

-15mins Acetone soaking to remove PMMA → 5mins IPA→ RO water rinse

-1hr hard baking PI2545

Interconnection metal:

-LOR+PMMA coating and patterning

-Ti 50nm/Au 250nm in Plassys II or IV

-2hr in pre-warmed SVC-14→ lift off

Appendix IV

Explanation of Signal Loss

Fig. A.4.1 shows the whole readout circuit when measuring the photoresponse of the fabricated array device. Excepet for the ON-resistance of the co-integrated MESFET (R_{FET}), the ON-resistance of the external MUX (R_{MUX}) and input impedance of the TIA (R_{in}) are also included.

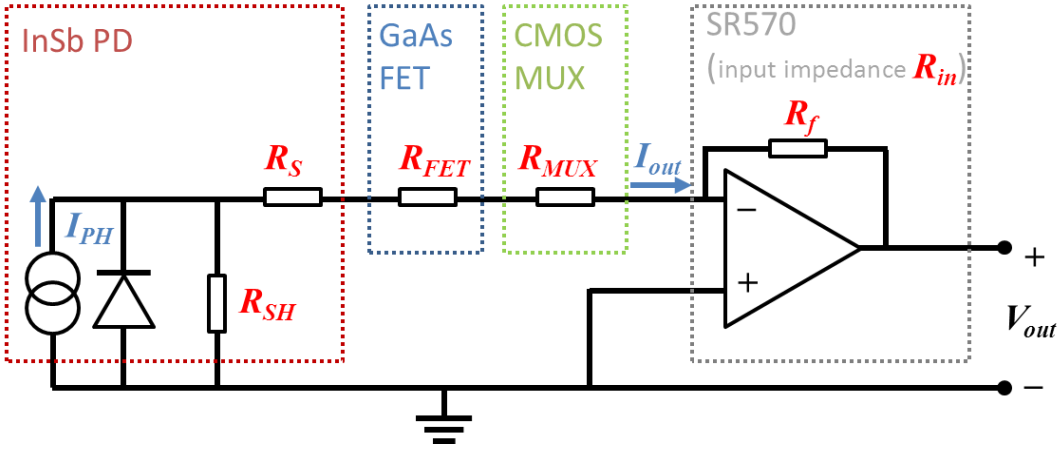


Fig.A.4.1. Equivalent circuit of the responsivity measurement.

The output voltage is then given by:

$$V_{out} = I_{out} \times R_f$$

$$I_{out} = \frac{R_{SH}}{R_{total}} \times I_{PH}$$

where

$$R_{total} = R_s + R_{SH} + R_{FET} + R_{MUX} + R_{in}$$

Therefore, the effective quantum efficiency is given by:

$$\eta' = \frac{h\upsilon}{q} \times \frac{I_{out}}{P_{det}} = \frac{R_{SH}}{R_{total}} \times \eta$$

whereη is the quantum efficiency as described in Sec.3.3.2.1. The effective specific detectivity (thermal noise limited) is then given by:

$$D^{*'} = \sqrt{A} \times \frac{q\eta^*}{h\upsilon} \times \left(\frac{4KT}{R_{total}}\right)^{-\frac{1}{2}} = \sqrt{\frac{R_{SH}}{R_{total}}} \times D^*$$

In this work, the contact resistacne R_s is negligible (<1 ohm), the shunt resistance of the InSb photodiode R_{sh} = ~10 ohm, R_{FET} = ~30 ohm, R_{MUX} = ~60 ohm, R_{in} =100 ohm,hence the quantum efficiency is reduced by a factor of 20 whereas D* is reduced by a factor

of$\sqrt{20}$. Therefore the intrinsic de-embedded quantum efficiency of the photodiode is 30% andD* is approximately 2.7 $\times 10^8$ cmHz$^{1/2}$W^{-1}.

Both the effective quantum efficiency and detectivity values can be recovered when the photodiode shunt resistance is 10 times larger than the series connected resistance. This can be achieved by scaling down the pixel sensing area, replacing the current column MUX with a low ON-resistance device or using cooling.

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