The development of silicon compatible processes for HEMT realisation

By

Menglin Cao

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This thesis is dedicated to my parents *Shufang Wu* & *Guohua Cao*.

Abstract

Compound semiconductor (III-V) devices are crucially important in a range of RF/microwave applications. High Electron Mobility Transistors (HEMTs), as the best low noise high frequency compound semiconductor devices, have been utilised in various applications at microwave and mm-wave frequencies such as communications, imaging, sensing and power. However, silicon based manufacturing will always be the heart of the semiconductor industry. III-V devices are conventionally fabricated using gold-based metallisation and lift off processes, which are incompatible with silicon manufacturing processes based on blanket metal or dielectric deposition and subtractive patterning by dry etching techniques. Therefore, the challenge is to develop silicon compatible processes for the realisation of compound semiconductor devices, whilst not compromising the device performance.

In this work, silicon compatible processes for HEMT realisation have been developed, including the demonstration of a copper-based T-gate with the normalised DC resistance of 42 Ω/mm, and the presentation of a gate-first process flow which can incorporate the copper-based T-gate. The copper electroplating process for fabricating T-gate head with the maximum width of 2.5 μm, low damage inductively coupled plasma molybdenum etching process for realising T-gate foot with the minimum footprint of 30 nm, and the full gate-first process flow with non-annealed ohmic contact are described in detail. In addition, this thesis also describes the fabrication and characterisation of a 60 nm footprint gold-based T-gate HEMT realised by conventional III-V processes, yielding a cutoff frequency f_T of 183GHz and maximum oscillation frequency f_{max} of 156GHz. In the comparison between these two types of HEMT, it is anticipated that a HEMT with the copper-based T-gate would not only have a larger maximum frequency of oscillation f_{max}, but also an easier incorporation into a silicon based manufacturing fab in terms of process technologies, than a HEMT with the gold-based T-gate.

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Publications

- M. Cao, X. Li, M. Missous, I. G. Thayne, "Nanoscale molybdenum gates fabricated by low damage inductively coupled plasma SF_6/C_4F_8 etching suitable for high performance compound semiconductor transistors", *Microelectronic Engineering*, vol. 140, pp. 56-59, 2015.

- M. Cao, X. Li, S. Ferguson, S. Thoms, D. MacIntyre, I. G. Thayne, "A simple silicon compatible 40 nm electroplated copper T-gate process", *Microelectronic* Engineering, vol. 121, pp. 153-155, 2014.

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- M. Cao, X. Li, I. G. Thayne, "A low damage inductively coupled plasma etch process of molybdenum with critical dimension of 30 nm suitable for compound semiconductor devices", in UK semiconductor 2014, 9-10 July 2014, Sheffield, UK.

- M. Cao, X. Li, I. G. Thayne, "An anisotropic low power, low DC bias, SF_6/C_4F_8 inductively coupled plasma etch process of molybdenum with critical dimension of 30 nm suitable for compound semiconductor devices", in 58th International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication (EIPBN 2014), 27-30 May 2014, Washington DC, USA.

Author Declaration

“I declare that the results presented in this thesis are my own work except where stated and they have not been submitted for any other degree”.

Menglin Cao

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Chapter 1

Introduction

Compound semiconductor transistors offer significant performance gains over silicon based devices, due to the superior intrinsic properties of III-V materials such as higher electron mobility and velocity resulting from the low electron effective mass [1.1]. For instance, high electron mobility transistors (HEMTs) are the best low noise high frequency devices [1.2-1.3] for communications, imaging, sensing and power applications at microwave and mm-wave frequencies [1.4-1.9]. However, silicon-based manufacturing is still the mainstream of the semiconductor industry.

Recently, a number of activities have begun to emerge where there is a need to combine the economies of scale and volume manufacture offered by silicon-based approaches with the performance enhancements offered by compound semiconductor materials and devices [1.10-1.11]. These solutions require that compound semiconductor devices can be manufactured using contemporary silicon approaches in a silicon fabrication facility, without compromising either the fabrication line due to the use of incompatible materials, or the device performance due to the process flows being used. This requires a step change in the way compound semiconductor devices are produced. Typically, gold-based metallisations are used in III-V device realisation, which is incompatible with silicon manufacturing as gold is an unwanted impurity in silicon [1.12]. In addition, III-V device process flows are traditionally based around "lift off" approaches, which also are not compatible with mass production silicon fabs.

Silicon manufacturing is based around blanket metal or dielectric deposition and subtractive patterning usually by dry etching techniques, which can introduce damage into the underlying semiconductor materials and reduce device performance. The challenge therefore, is to develop silicon compatible processes for the realisation of III-V compound semiconductor devices, whilst not compromising the transistor performance.

In this work, a key outcome is the demonstration of a silicon compatible process to realise a copper T-gate for a HEMT, and which can be integrated into a gate-first process flow for HEMT fabrication. In comparison with a conventional gold-based T-gate, the copper T-gate

developed in this work is predicted to increase the maximum frequency of oscillation f_{max} of the HEMT due to reduced gate resistance.

Following this brief introduction, **Chapter 2** describes the basic device theory, which lays out the fundamental theoretical aspects of this work. The fabrication techniques utilised in the project are introduced in **Chapter 3,** which provides knowledge on the practical implementation of a HEMT. The characterisation techniques and methods for both semiconductor materials and transistors are included in **Chapter 4**, providing insight into the evaluation of device performance. A brief review of HEMT technology evolution and current state of the art are given in **Chapter 5**. **Chapter 6** and **Chapter 7** present experimental details and relevant results in this research work. Finally, a conclusion of the research work and a discussion of possible future work are given in **Chapter 8**.

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Chapter 2

The High Electron Mobility Transistor

2.1 Introduction

The High Electron Mobility Transistor (HEMT) is a field effect device, whose operation relies on modulating the current flowing through the channel between the source and drain by applying a voltage to the gate contact which is placed between them.

The advantage of the HEMT over other field effect transistors is the large concentration of high mobility electrons in the channel which can be located in close proximity to the gate. The former results in high carrier velocity and reduced access resistance, whilst the latter facilitates good electrostatic control to short channel lengths. These factors in combination, are key to the realisation of an optimised energy efficient, high frequency transistor. The high electron mobility in the device channel results from the heterojunction formed at the interface between two layers of semiconductor material with different bandgaps, which creates a two dimensional electron gas (2DEG) and which can be used to spatially separate the channel carriers from the donor atoms that produced them.

A HEMT consist of epitaxial material layers and metallic contacts fabricated on the material by particular processes, as shown in **Figure 2.1.1**.

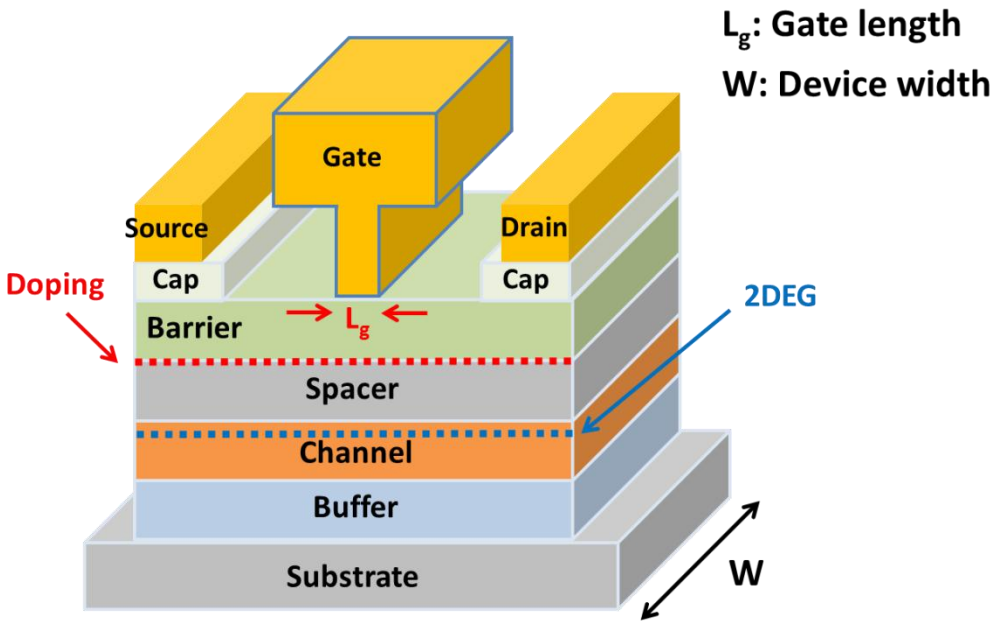


Figure 2.1.1 – A generic layout of the HEMT structure

The material layers include substrate, buffer, channel, spacer, barrier and cap layer from bottom to the top, which are formed during wafer growth. The cap layer is highly doped and enables the formation of source and drain contacts of the device with low contact resistance. The channel is a narrow bandgap and undoped high mobility material. Doping is introduced in the barrier layer, which is a large bandgap material. Generally, there is a spacer layer of the same material as the barrier layer, between the barrier and the channel. It spatially separates the electrons in the channel from the ionised donors in the barrier layer.

The metallic contacts of the HEMT are the ohmic source and drain and the Schottky gate, which are defined on the cap layer and barrier layer respectively. The ohmic contact, facilitate low resistance access to the underlying semiconductor, whilst the Schottky contact is rectifying and can be used to modulate the channel current. A T-gate strategy is normally utilised for the gate contact, for reasons which will be discussed in **Section 2.5**.

In this chapter, the relevant aspects underlying the operation of a HEMT are described, including heterostructure formation, metal-semiconductor contacts, and device operation at both DC and RF frequencies.

2.2 Heterostructure formation

When two dissimilar semiconductor materials are brought into contact, a heterostructure is formed. The heterojunction at the interface between the materials is extremely important to create the high electron mobility channel in a HEMT. To understand the heterojunction formation, the example of an $In_{0.52}Al_{0.48}As$/ $In_{0.53}Ga_{0.47}As$ heterostructure is introduced. In this configuration, the key layers of the HEMT are shown in **Figure 2.1.1**. InGaAs is the layer in which the channel is formed and is undoped, while the InAlAs is the barrier layer and n-doped.

The energy band diagrams of n-doped $In_{0.52}Al_{0.48}As$ and undoped $In_{0.53}Ga_{0.47}As$ material respectively are presented in **Figure 2.2.1**.

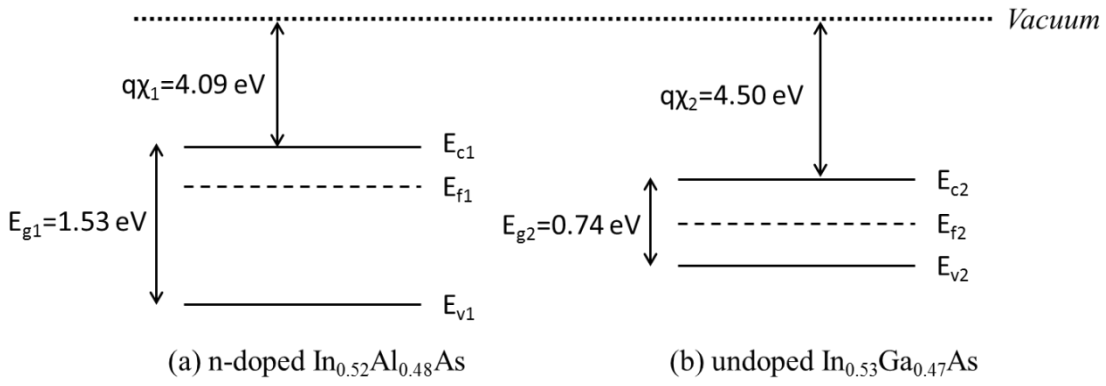


Figure 2.2.1 – Energy band diagrams of n-doped $In_{0.52}Al_{0.48}As$ and undoped $In_{0.53}Ga_{0.47}As$ separately

E_c and E_v are the lower conduction band edge and upper valance band edge of the materials respectively, which are separated by the bandgap energy E_g. The InAlAs is the wider bandgap material and InGaAs is narrower bandgap material ($E_{g1} > E_{g2}$). The electron affinity $q\chi$ is defined as the energy required to move a free electron at the conduction band edge E_c to the vacuum level. From the Fermi-Dirac distribution function, which describes the probability of a state being filled, the Fermi level E_f is defined as the energy at which the probability of a state being filled is one half [2.1]. In undoped semiconductors, the Fermi level E_f can be

related to the conduction and valence band energies, the density of states in each band and the material temperature [2.1]:

$$E_f = \frac{E_c + E_v}{2} + \frac{k_B T}{2} \ln \frac{N_v}{N_c} \qquad \textbf{Eqn 2.2.1}$$

where k_B is the Boltzmann constant, T is the material temperature, N_V and N_C are the effective densities of states in the valence and conduction bands respectively.

If a semiconductor is doped n-type, such as in the system under consideration in **Figure 2.2.1**, the energy of the Fermi level is related to the conduction band energy by [2.1]:

$$E_f = E_c - k_B T \ln \frac{N_c}{N_D} \qquad \textbf{Eqn 2.2.2}$$

where N_D is the donor concentration.

From **Eqn 2.2.2**, the energy difference between the Fermi level and the conduction band edge is reduced with increasing donor concentration N_D, which means the Fermi level E_f is located close to the conduction band edge E_c.

Therefore, for the materials in **Figure 2.2.1**, the Fermi level is close to the conduction band edge E_{c1} in n-doped InAlAs and close to the middle of bandgap E_{g2} in nominally undoped InGaAs.

When n-doped InAlAs and undoped InGaAs material are brought into contact, the heterojunction is formed and the Fermi level E_f is continuous across the interface between n^+ InAlAs and InGaAs. The vacuum level is continuous and must bend to keep the values of $q\chi_1$ and $q\chi_2$ constant throughout the structure. Higher energy electrons diffuse from the highly doped InAlAs into the undoped InGaAs, which depletes the n^+ InAlAs layer over a region of thickness *D* and leaves ionised donors in it. The electrons accumulate at the interface within the InGaAs layer, which generates an electric field across the interface between the ionised donors in n^+ InAlAs and the accumulated electrons in InGaAs layer. An equilibrium state will be reached finally when the electric field is large enough to prevent electrons diffusing from

n^+ InAlAs to InGaAs. The n-doped InAlAs and undoped InGaAs heterostructure formation is illustrated in **Figure 2.2.2**.

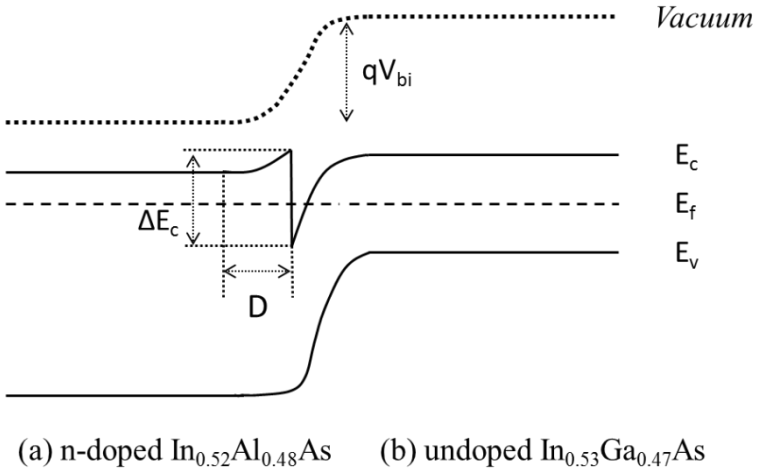


Figure 2.2.2 – Heterostructure formation between n-doped $In_{0.52}Al_{0.48}As$ and undoped $In_{0.53}Ga_{0.47}As$

In **Figure 2.2.2**, the conduction band offset ΔE_c is the magnitude of the discontinuity between two conduction band edges of two semiconductor materials at the interface. The discontinuity ΔE_c is independent of doping and can be expressed by the difference of electron affinities of two material ($\Delta E_c = q\chi_2 - q\chi_1$), since both InAlAs and InGaAs are non-degenerate semiconductors [2.2]. The electric field generated between the ionised donors in the InAlAs layer and accumulated electrons in the InGaAs layer across the heterojunction is governed by the built-in voltage V_{bi}, which causes the conduction band and valence band bending near the interface. The electric field across the heterojunction causes the diffused electrons in the InGaAs layer to be confined into a quasi-triangular potential well in the conduction band close to the interface, which is described by the Poisson equation and Gauss's Law [2.3].

The width of the triangular potential well formed in the InGaAs is similar to the wavelength of the electrons, resulting in the formation of discrete quantised energy levels, as shown in **Figure 2.2.3**.

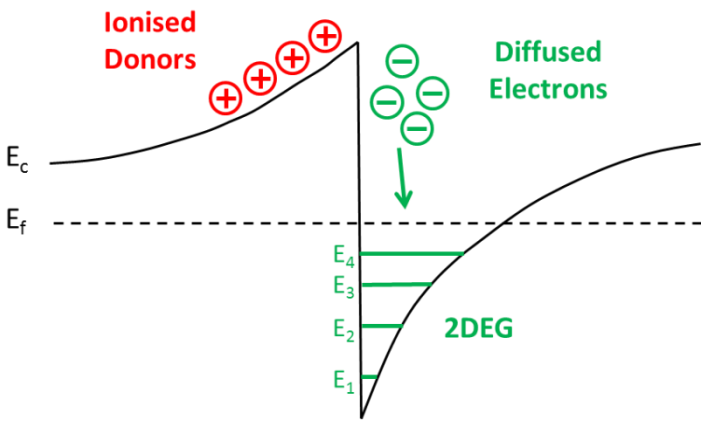


Figure 2.2.3 – Formation of two dimensional electron gas (2DEG)

In these discrete energy levels, electrons are free to move in only two dimensions and in the direction parallel to the interface (between source and drain of HEMT), which is known as a two dimensional electron gas (2DEG). As a result of the spatial separation between the electrons in 2DEG in InGaAs (channel layer of HEMT in **Figure 2.1.1**) and ionised donors in InAlAs (barrier layer of HEMT in **Figure 2.1.1**), the electron mobility of a 2DEG is increased as a consequence of a reduction in ionised impurity scattering, which results from the coulombic interactions of electrons with the electric field of ionised dopants. This concept is known as modulation doping, and was first presented by Dingle, *et al.* [2.4].

Various representative charge concentration and mobility in modulation-doped heterostructures are presented in **Table 2.2.1** [2.5].

Heterojunction	Two-Dimensional Charge (cm^{-2})	Mobility (cm^2/Vs)
$Al_{0.3}Ga_{0.7}As/GaAs$	1×10^{12}	7000
$Al_{0.3}Ga_{0.7}As/ In_{0.2}Ga_{0.8}As$	2.5×10^{12}	7000
$In_{0.52}Al_{0.48}As/ In_{0.53}Ga_{0.47}As$	3.0×10^{12}	10000
AlGaSb/InAs	2×10^{12}	20000

Table 2.2.1 – Electron concentration and mobility of 2DEG in various heterostructures

By self-consistently solving the Poisson and Schrödinger equations [2.6], the conduction band profile and charge distribution in the quantum well can be determined.

The Poisson equation is [2.7]:

$$\nabla\big(k(z)\nabla\phi(z)\big) = -q[N_d(z) - N_a(z) + p(z) - n(z)] \qquad \textbf{Eqn 2.2.3}$$

The Schrödinger equation is [2.7]:

$$\left[-\frac{\hbar^2}{2m_e}\Delta + E_c(z) + V_{xc}(z)\right]\xi_i(z) = \epsilon_i\xi_i(z) \qquad \textbf{Eqn 2.2.4}$$

Where $k(z)$ is the dielectric constant at a given position z, $\phi(z)$ is electrostatic potential, $N_d(z)$ and $N_a(z)$ are donor and acceptor densities respectively, $n(z)$ and $p(z)$ are electron and hole concentrations respectively, $\hbar$ is Planck's constant, m_e is the electron effective mass, $V_{xc}(z)$ is the local exchange-correlation potential, which accounts for the effects of electron-electron interaction, ϵ_i is the eigen energy for the ith (i=1, 2…) subband (solution to the wave function $\xi_i(z)$ at a given position).

Therefore, the electron concentration of the 2DEG can be expressed as [2.7]:

$$n(z) = \sum_i \frac{m_e k_B T}{\pi\hbar^2} \ln\left[1 + exp\frac{E_f - \epsilon_i}{k_B T}\right]|\xi_i(z)| \qquad \textbf{Eqn 2.2.5}$$

Figure 2.2.4 shows the n^+ InAlAs/ InGaAs heterojunction conduction band profile with 1D co-ordinate system z perpendicular to the interface of two semiconductors. The origin of the system is at the interface.

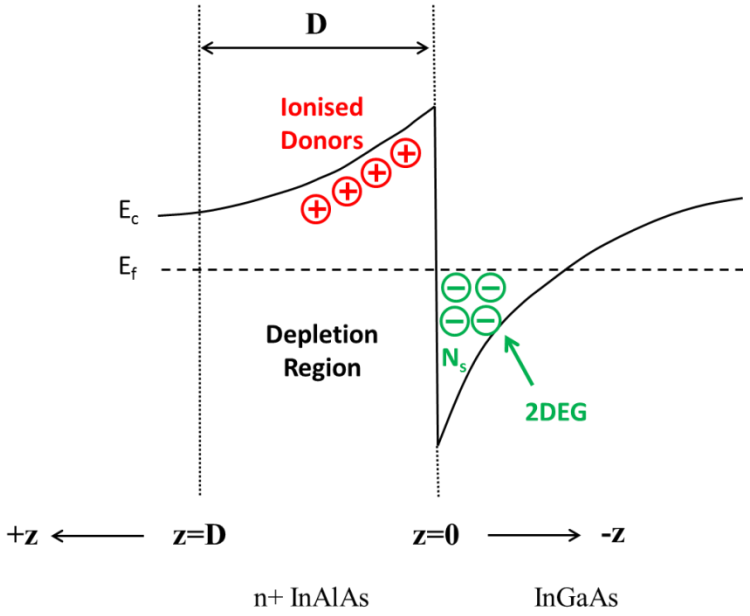


Figure 2.2.4 – Conduction band profile of n^+ InAlAs/ InGaAs heterojunction

According to Gauss's law, the electric field $E_{interface}$ at the interface $z=0$ in the InGaAs can be related to the electron concentration of the 2DEG N_s, and the permittivity of the InGaAs ε_{InGaAs} [2.8]:

$$E_{interface} = \frac{-qN_s}{\varepsilon_{InGaAs}} \qquad \textbf{Eqn 2.2.6}$$

The electric field in the depletion region in n^+ InAlAs will decrease from the maximum value at the interface $z=0$ to zero at $z=D$. According to Poisson's equation:

$$\frac{dE}{dz} = \frac{qN_d}{\varepsilon_{InAlAs}} \qquad \textbf{Eqn 2.2.7}$$

Where N_d is the doping concentration of InAlAs and ε_{InAlAs} is the permittivity of InAlAs.

As a consequence,

$$E(z) = \frac{qN_d z}{\varepsilon_{InAlAs}} + Constant \qquad \textbf{Eqn 2.2.8}$$

Considering **Eqn 2.2.6** and as a result,

$$E_{interface} = E(0) = Constant = \frac{-qN_s}{\varepsilon_{InGaAs}} \qquad \textbf{Eqn 2.2.9}$$

If the permittivities of two semiconductors are assumed to be equal, i.e. $\varepsilon_{InAlAs} = \varepsilon_{InGaAs} = \varepsilon$, then **Eqn 2.2.8** becomes:

$$E(z) = \frac{q}{\varepsilon}(N_d z - N_s) \qquad \textbf{Eqn 2.2.10}$$

At $z=D$, the electric field is zero. Therefore,

$$N_d D = N_s \qquad \textbf{Eqn 2.2.11}$$

From **Eqn 2.2.11**, the depletion width is related to the ratio of the electron concentration of the 2DEG in InGaAs and the doping concentration of InAlAs.

2.3 Metal – semiconductor contacts

Following the achievement of the high mobility 2DEG channel of the device by forming a heterojunction between the wide bandgap highly doped semiconductor and narrow bandgap intrinsic semiconductor, it is important to build the metallic contacts of the device to drive and modulate the channel current.

The formation of a metal-semiconductor junction is, in some ways similar to the situation of heterojunction formation between two dissimilar semiconductors. The energy band diagram of a metal and an n-doped semiconductor is shown in **Figure 2.3.1**.

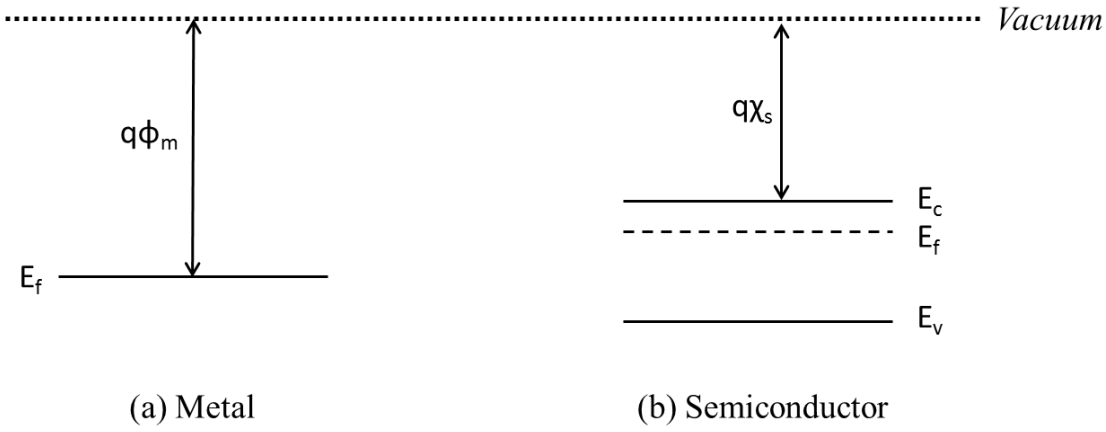


Figure 2.3.1 – Energy band diagrams of metal and n-doped semiconductor

The Fermi level E_f, electron affinity of the semiconductor $q\chi_s$ (defined as the energy required to move a free electron in the conduction band edge E_c to the vacuum level) and work function of the metal $q\phi_m$ (defined as the energy required to move a free electron at the Fermi level E_f to the vacuum level) are illustrated in **Figure 2.3.1**. When the metal and n-doped semiconductor are brought into contact, the Fermi levels align, and electrons diffuse from semiconductor layer to metal layer, which generates a built-in electric field V_{bi} across the interface between the accumulated electrons in the metal and the ionised donors in the semiconductor. The resulting band bending in the semiconductor forms an energy barrier at the interface, which is known as a Schottky barrier, as presented in **Figure 2.3.2**. The Schottky barrier is with a barrier height of $q\phi_b$ above the Fermi level, and a barrier width of *D*

into the semiconductor, which is also the width (depth) of the depletion region in the semiconductor.

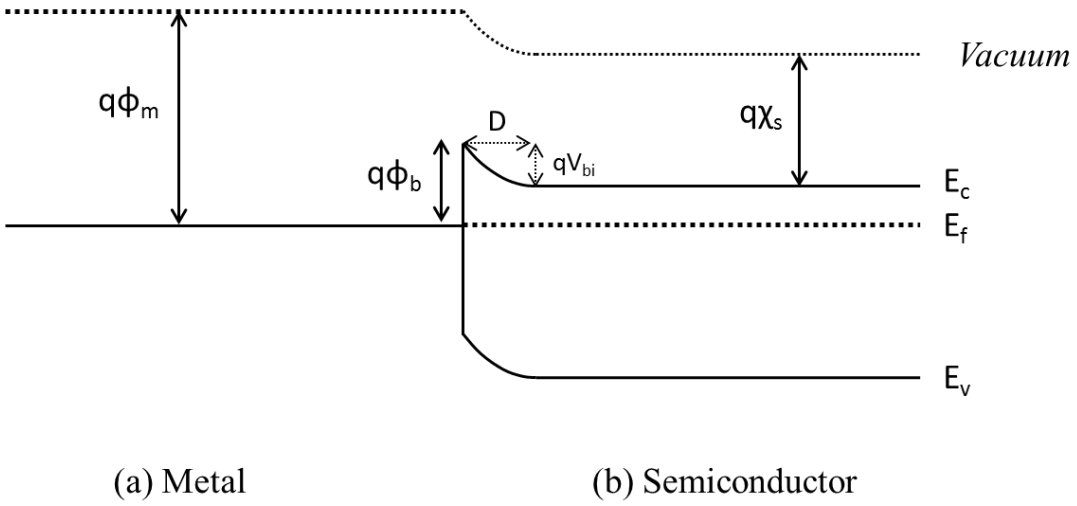


Figure 2.3.2 – Schottky barrier formation

The Schottky barrier height $q\phi_b$ is defined as the energy required for an electron at the Fermi level in the metal to transfer to the conduction band of the semiconductor. In the ideal situation, the Schottky barrier height ϕ_B can be described by the Schottky model [2.9] and expressed as:

$$q\phi_B = q(\phi_m - \chi_s) \qquad \textbf{Eqn 2.3.1}$$

In the Schottky model, the Schottky barrier height is simply the difference between work function of metal and electron affinity of the semiconductor. This is not, however reflected in experimental observation.

The Bardeen model, which considers the surface states at the interface between the metal and semiconductor, describes the Schottky barrier between metal-semiconductor contacts better in reality [2.10]. There are surface states existing in a thin region at the interface between the metal and semiconductor, since the periodicity of the crystal lattice of a semiconductor and metal is interrupted at the contact interface. The surface states density is determined by

various factors including the crystal orientation of the two materials, the quality of the interface between them, and the semiconductor doping situation [2.11].

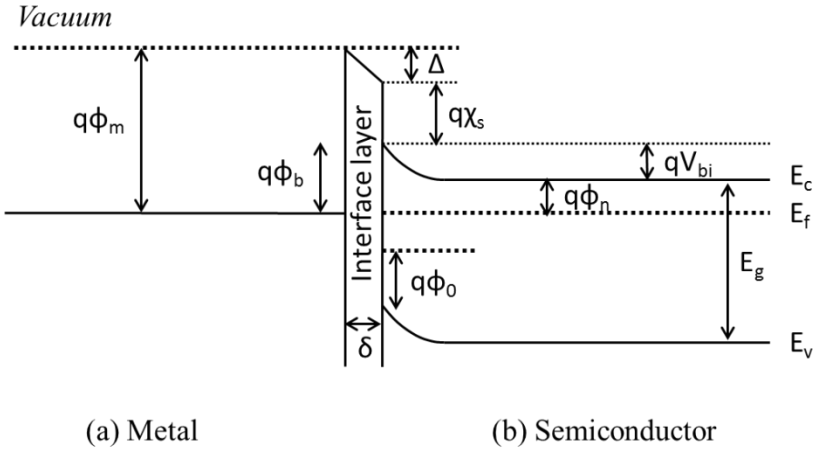


Figure 2.3.3 – The band diagram of metal-semiconductor contact in the Bardeen model

Figure 2.3.3 shows the band diagram metal-semiconductor contact in the Bardeen model. The interface layer between the metal and semiconductor has thickness δ, which is defined by the surface state density supporting a potential difference of Δ. $q\phi_0$ is the energy required to fill in the surface states and make them charge neutral. $q\phi_n$ is the energy offset between the Fermi level and conduction band edge in the semiconductor.

When the surface states density is large enough that the difference between the work function of the metal and the electron affinity of the semiconductor $q(\phi_m-\chi_s)$ can be completely compensated by the surface states, there will be no electron diffusion from the semiconductor to the metal. As illustrated in **Figure 2.3.3**, the Schottky barrier height can be expressed as:

$$q\phi_b = E_g - q\phi_0 - q\phi_n \qquad \textbf{Eqn 2.3.2}$$

Therefore, the Schottky barrier height is independent of metal work function and related to bandgap of the semiconductor and surface state density. The Fermi level will be pinned at a particular energy level below the conduction band edge, which has been experimentally verified in III-V semiconductor materials [2.12-2.13].

The width of the Schottky barrier D can be derived from Poisson equation:

$$D = \sqrt{\frac{2\epsilon_s}{qN_d}(q\phi_b - V)} \qquad \textbf{Eqn 2.3.3}$$

Where N_d is the donor concentration, ϵ_s is the dielectric constant of the semiconductor, and V is the voltage applied to the contact.

From **Eqn 2.3.3**, D will be reduced as N_d increases, which means that higher doped semiconductor material will have a Schottky barrier with shallower depletion depth.

There are three main mechanisms existing for current flowing across the energy barrier between the metallic contacts of the device and the semiconductor material: thermionic emission, field emission and thermionic field emission [2.14]. The dominant mechanism of electron transport through metal-semiconductor contacts is determined by the height of the Schottky barrier and the width of its associated depletion region, as shown in **Eqn 2.3.2** and **Eqn 2.3.3**, which are dependent on the doping level and the properties of the semiconductor material.

In thermionic emission, electrons are excited by thermal energy to cross the energy barrier. The current density J_{TE} in thermionic emission is exponentially dependent on the magnitude of the energy barrier E_B and on the material temperature T.

$$J_{TE} \propto exp\left(-\frac{E_B}{k_B T}\right) \qquad \textbf{Eqn 2.3.4}$$

The thermionic emission current density will be enhanced when material temperature is increased and the magnitude of the energy barrier is reduced.

The field emission mechanism relies on the quantum mechanical tunnelling of electrons through the energy barrier for current to flow [2.15]. The tunnelling current density J_{FE} in

field emission is determined by the probability of electrons tunnelling through the energy barrier, which is dependent on the magnitude and width of the energy barrier.

$$J_{FE} \propto exp\left(-\frac{E_B}{E_{00}}\right) \qquad \textbf{Eqn 2.3.5}$$

Where E_{00} is the tunnelling parameter:

$$E_{00} \equiv \frac{q\hbar}{2}\sqrt{\frac{N_d}{\epsilon_s m_e}} \qquad \textbf{Eqn 2.3.6}$$

From **Eqn 2.3.5** and **Eqn 2.3.6**, the tunnelling current increases as the magnitude of energy barrier decreasing and dopant density increasing, which means that it is easier for electrons to tunnel when the barrier width is thinner.

Thermionic field emission is a combination of thermal excitation and tunnelling transport. In thermionic field emission, electrons have insufficient energy to cross the barrier by thermal excitation entirely, and the width of energy barrier is too wide for electrons to directly tunnel through. However, electrons with a degree of thermal excitation energy might be able to tunnel through the barrier, since the width of the barrier decreases with its height. This results in the thermionic field emission current flowing through the energy barrier, which can be expressed as [2.16]:

$$J_{TFE} \propto exp\left(\frac{E_B}{E_{00}\coth\frac{E_{00}}{k_B T}}\right) \qquad \textbf{Eqn 2.3.7}$$

Three mechanisms of electrons transporting across the energy barrier are illustrated in **Figure 2.3.4**.

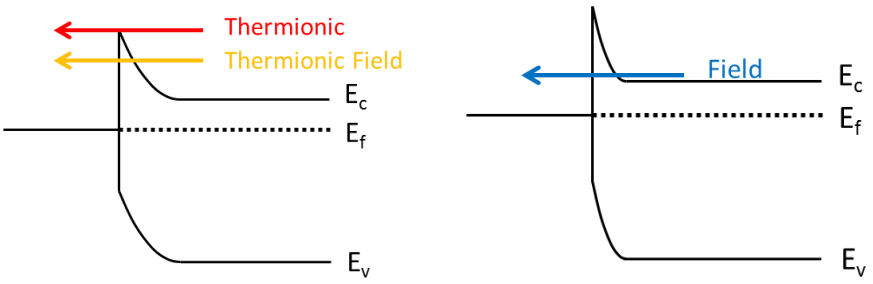


Figure 2.3.4 – Illustration of thermionic emission, thermionic field emission and field emission mechanisms of electron transporting across the energy barrier

As mentioned above, there is a Schottky barrier formed at the interface when a metal and semiconductor are brought into contact, and there are two types of metal-semiconductor contacts: Schottky contact and ohmic contact.

When the electron transport across the energy barrier is dominated by thermionic emission, a Schottky contact is formed.

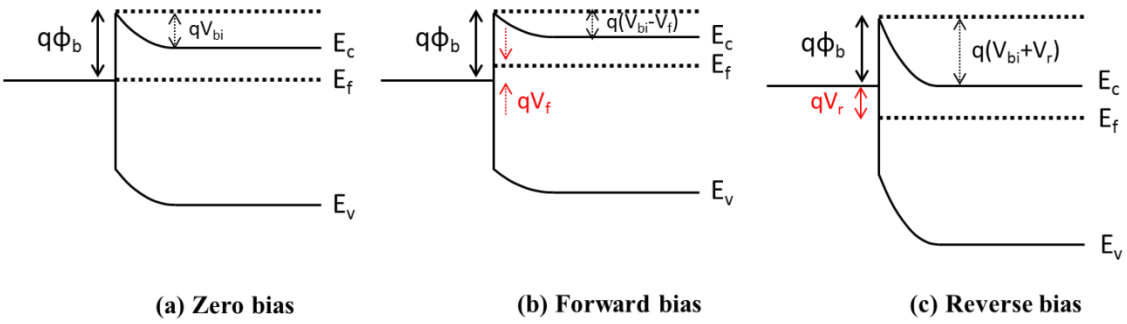


Figure 2.3.5 – Energy band diagram of Schottky contact under various biases

As illustrated in **Figure 2.3.5**, when forward bias V_f is applied on the metal-semiconductor contact, the barrier height impeding electron transport from the semiconductor to the metal is decreased to $q(V_{bi}-V_f)$, which increases the probability of electrons in semiconductor with sufficient thermal energy to cross the barrier into the metal to create a current flow. The current will increase when the forward bias V_f is as large as the built in voltage V_{bi}, since the energy barrier impeding electrons transport from the semiconductor to the metal is eliminated. When the metal-semiconductor contact is reverse biased, the barrier height between semiconductor and metal is increased to $q(V_{bi}+V_r)$. It is unlikely for electrons in the semiconductor to acquire enough thermal energy to cross the barrier and get into metal. If the

Schottky barrier height $q\phi_B$ between metal and semiconductor is large, caused by using wide bandgap semiconductor material, it is also difficult for electron in the metal to cross the barrier into the semiconductor by thermionic emission. Therefore, a metal-semiconductor contact with rectifying characteristics is formed. The current-voltage (I-V) characteristics of Schottky contact is shown in **Figure 2.3.6**.

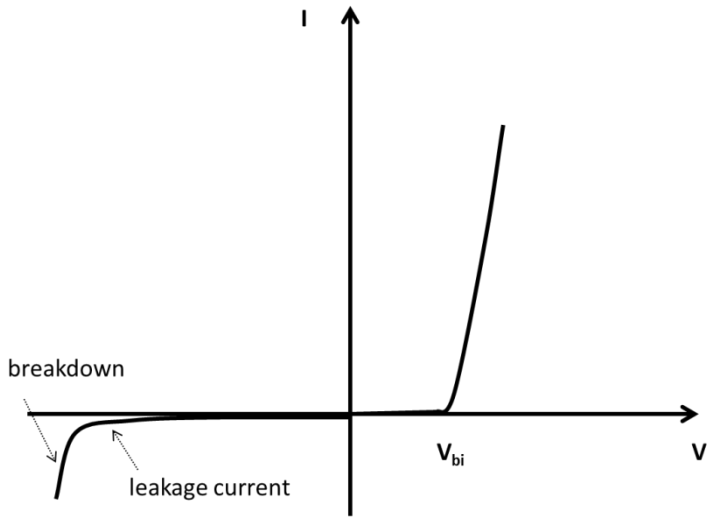


Figure 2.3.6 – Rectifying characteristics of Schottky contact's I-V

There will be small leakage current flow in reverse bias resulting from the electron transport by field emission. The breakdown current occurs finally when the reverse bias is increased beyond a certain value, since the electron transport is dominated by field emission.

When the electron transport across the energy barrier is dominated by field emission, in which the barrier width is very thin resulting from very high doping concentration in semiconductor, the metal-semiconductor contact is ohmic. In ohmic contacts, the current-voltage response is linear for both forward and reverse bias.

In HEMT design and fabrication, different strategies are chosen to form ohmic contacts for source and drain of the device and Schottky contacts for gate of the device. As shown in **Eqn**

2.3.3 and **Eqn 2.3.2**, the width of the Schottky barrier will be reduced when doping density of the semiconductor is high, and the height of the Schottky barrier will be decreased when the bandgap of the semiconductor is small. As a consequence, ohmic contacts are usually built on a highly doped cap layer (as shown in **Figure 2.1.1**) with narrow bandgap such as n-doped $In_{0.53}Ga_{0.47}As$, minimising both height and width of the Schottky barrier to enable large current flowing through the barrier by field emission, and obtaining low contact resistance for source and drain driving the current in the channel of the device. On the contrary, the Schottky contact is usually formed on an undoped barrier layer (as shown in **Figure 2.1.1**) with relatively wide bandgap such as $In_{0.52}Al_{0.48}As$, to achieve rectifying characteristics as discussed above for gate modulating the channel current in the device, which will be described in **Section 2.4.1**.

2.4 HEMT DC characteristics

2.4.1 2DEG concentration modulation

Similar to the operation of other field effect transistors, current flowing through the channel from the source to the drain in a HEMT is modulated by gate voltage. For increasingly negative applied gate voltages, the magnitude of the Schottky barrier between the gate metal and the barrier layer is increased as shown in **Figure 2.3.5**, depleting the electron concentration in the 2DEG. This continues until at a particular threshold voltage, V_{th}, applied to the gate, the electron concentration in the region below gate is reduced to zero. There is no current flowing through the channel between source and drain, and the channel becomes completely depleted. In this condition, the channel is said to be "pinched-off".

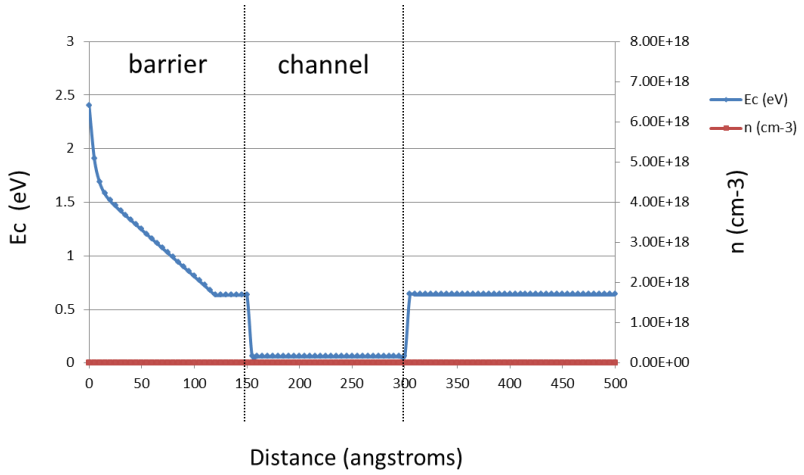
This process can be compared to the charging and discharging process of a parallel plate capacitor, with the metal gate as one plate and the channel as the other, between which the gate voltage applied. The dielectric of the semiconductors between gate and channel can be regarded as the dielectric in the capacitor. As a result, the current flowing through the channel from source to drain will be decreased due to the reduction of the electron concentration in the gate region.

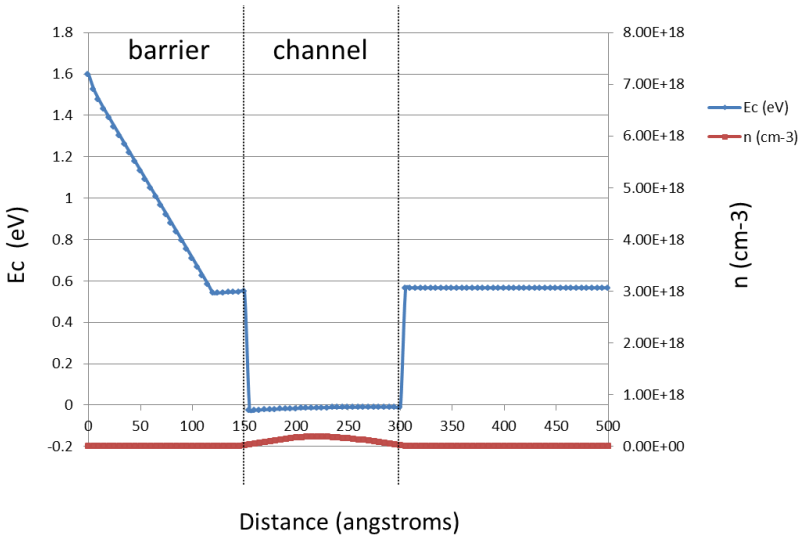
When the threshold voltage is negative, a HEMT is said to work in "depletion mode", at which the transistor is normally in an "ON" state at zero gate voltage. This device type is considered in the subsequent discussion. To the contrary, a HEMT is said to work in "enhancement mode" when the threshold voltage is positive. And the transistor is normally in an "OFF" state at zero gate voltage.

Although the majority of the electron population is confined in the channel layer, it is possible that electron accumulation occurs outside the channel and contributes to the current flow between source and drain. In this case, a parallel conduction channel is formed, which is undesirable. The parallel conduction channel underneath the gate will degrade the device

performance, since the advantages of high mobility 2DEG channel are diluted by electron transport in the parallel conduction path with much lower electron mobility. This effect can be minimised by designing the appropriate layer structure to ensure that the layers above the channel are completely depleted under zero gate bias, whilst the electron concentration in the channel is still large.

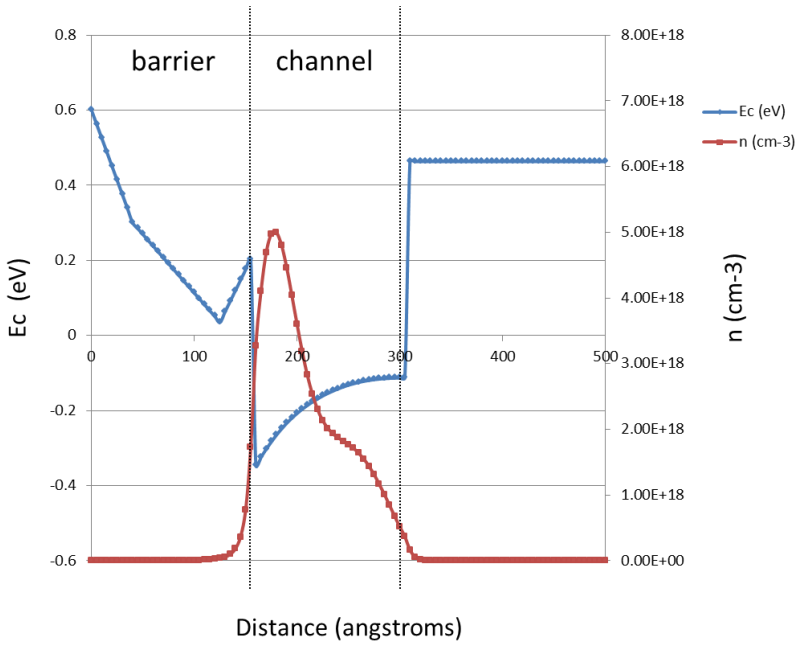
To better understand the 2DEG concentration modulation process, conduction band profiles and carriers concentration distributions through the HEMT structure under various gate voltages were simulated by a Poisson/ Schrödinger solver [2.6] and are presented in **Table 2.4.1**.

Conduction band profiles & carrier concentration distributions	**Gate voltage V_g (V)**
 The channel is completely depleted.	-1.8 V



Charge starts to accumulate in the channel.

-1 V



More charge accumulates in the channel.

0 V

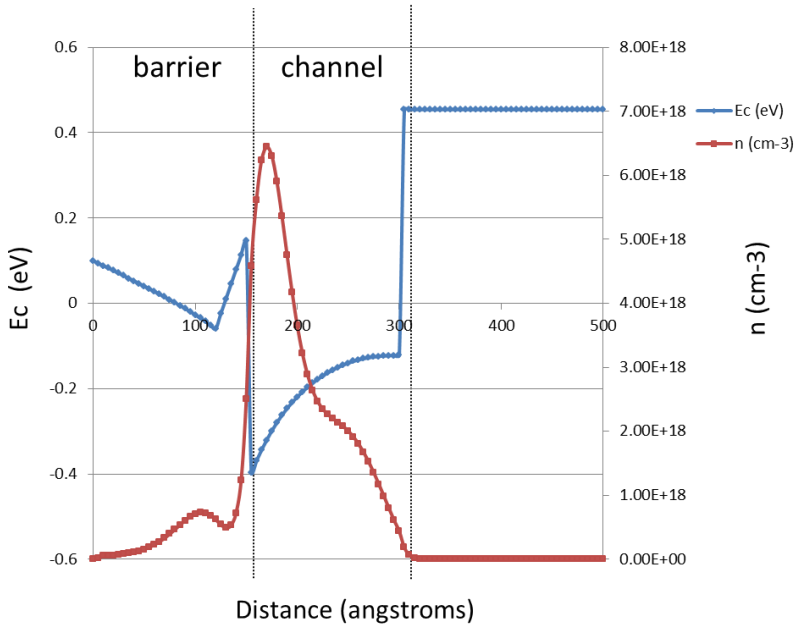
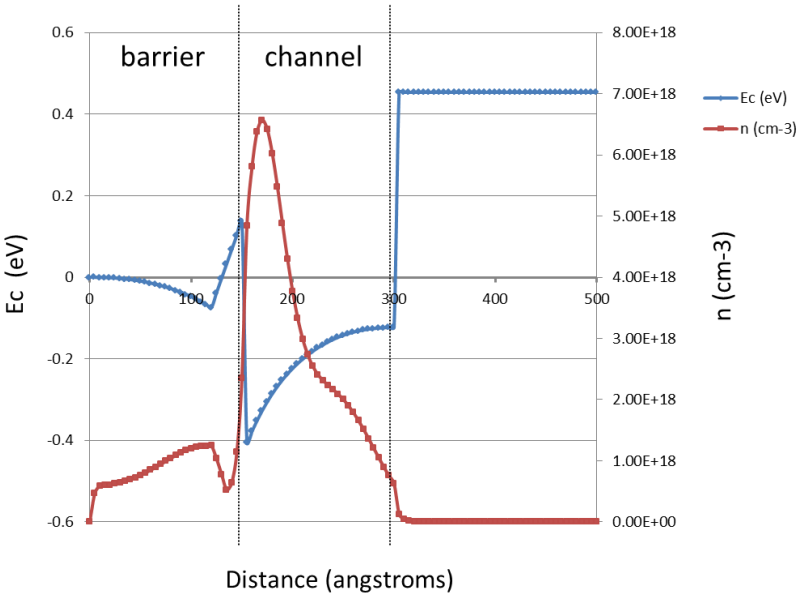
 The parallel conduction channel forms in the barrier.	0.5 V
 The parallel conduction channel concentration increases.	0.6 V

Table 2.4.1 – The change of conduction band profiles and carrier concentration distributions through the HEMT structure when various gate voltages are applied

From **Table 2.4.1**, the carrier concentration of the channel is reduced to zero when gate voltage is -1.8 V, which means that the channel is completely depleted at the threshold voltage of -1.8 V. When the gate voltage moves towards positive, more and more charge accumulates in the channel. However, as the gate voltage increasingly positive till 0.5 V, electron accumulation occurs outside the channel and the parallel conduction channel is formed. When gate voltage is getting more positive, the carrier concentration of the parallel conduction channel increases and the carrier concentration of the real channel will be saturated eventually.

2.4.2 Source-Drain current voltage response

When a voltage is applied between the source and drain of a HEMT, a current will flow between them through the device channel via the ohmic contacts. In HEMT operation, the source contact is usually grounded and a positive voltage is applied to the drain.

When the drain voltage is small, and hence at low electric field, the relationship between channel current I_d and drain voltage V_{ds} is linear. As the drain voltage V_{ds} is increased and hence at high electric field, the channel current saturates, since the electron velocity is saturated at high electric field [2.17]. When drain voltage is increased to a critical value, which is referred to as breakdown voltage, the electric field will be large enough to incur impact ionisation [2.18] in the channel. In this process, an electron with enough energy can knock an electron out of its bound state in the valance band and promote it into the conduction band, generating an electron hole pair. The increase in carrier concentration in the channel causes an increase of channel current, which is referred to as “breakdown”. In **Figure 2.4.1**, three regions of $I_d - V_{ds}$ response curve at zero gate bias are presented for a normally “ON” HEMT.

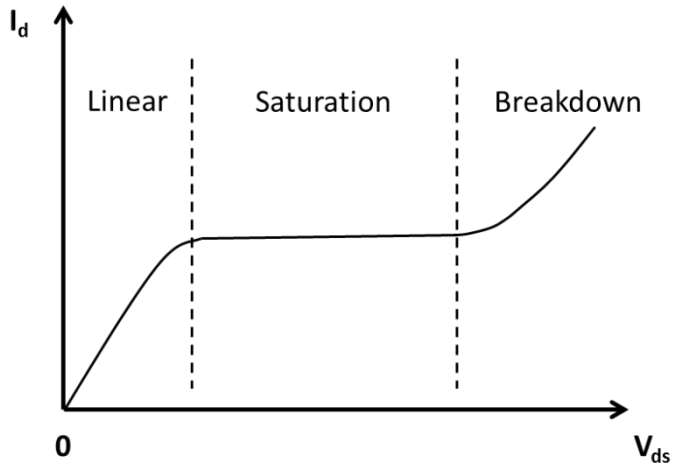


Figure 2.4.1 – Typical normally "ON" HEMT I_d –V_{ds} response with zero gate voltage

2.4.3 Source-Drain current modulation

By the application of a negative voltage on the Schottky gate contact, the electron concentration of the channel can be reduced as a result of channel depletion. Therefore, the current flow from source to drain can be modulated by depleting the channel in the gate region.

For increasingly negative gate voltages, the channel will be increasingly depleted and there will be less current flowing through the channel between source and drain, as presented in **Figure 2.4.2**.

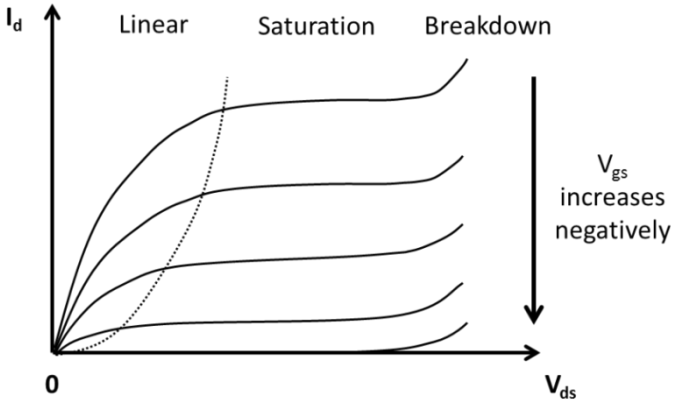


Figure 2.4.2 – Typical HEMT I_d –V_{ds} response with varied gate voltage

It can be seen from **Figure 2.4.2** that channel current I_{ds} saturation occurs at lower drain voltage when gate bias is more negative. It results from a high electric field region formed on the drain side of the gate due to the larger potential difference between the gate and the drain. It will also cause earlier breakdown at more negative gate voltage due to the same reason. The increased potential difference between gate and drain enlarges the effective depletion region of the gate on the drain side, as illustrated in **Figure 2.4.3**, which results in a non-uniform electron concentration through the channel between source and drain.

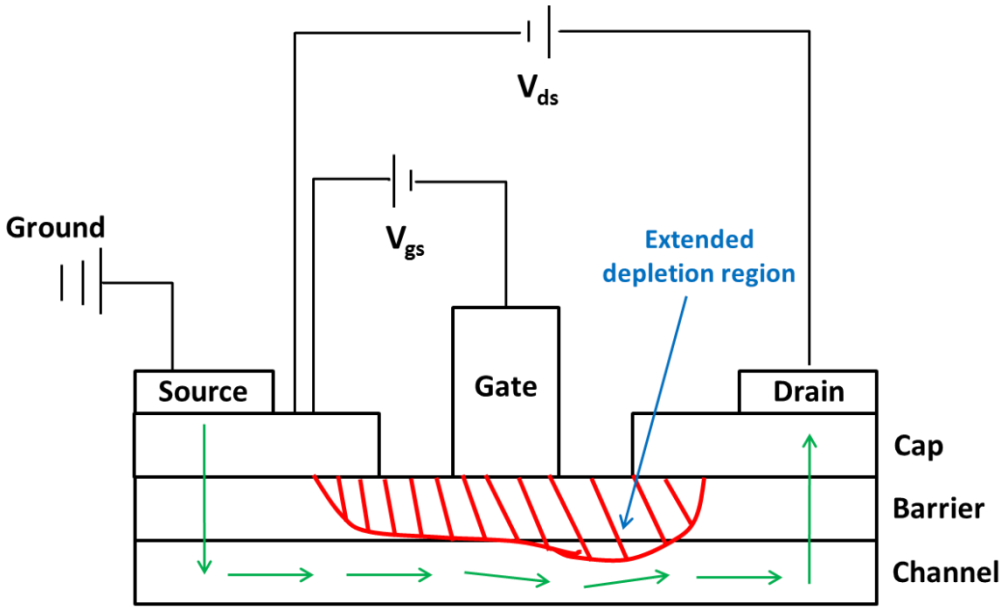


Figure 2.4.3 – Extended depletion region on the drain side of the gate

2.4.4 Intrinsic and extrinsic models

In reality, the complete device performance relies on both intrinsic and extrinsic properties, which includes behaviour in gate region and also in access regions. In the following discussions, the intrinsic properties of the device are extracted from a model, in which only the gate region is considered. Whilst, the extrinsic properties of the device are extracted from a model, in which the overall device region including source and drain access regions are

considered which represents the completed device more accurately. This is illustrated in **Figure 2.4.4**.

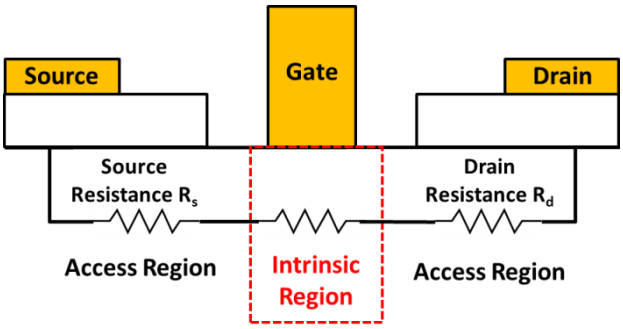


Figure 2.4.4 – Illustration of intrinsic region and access regions

2.4.5 DC figures of merit

Some important figures of merit in the DC characteristics of a HEMT can be extracted. The drain current flowing through the channel from source to drain can be presented as:

$$I_d = qnvW \qquad \textbf{Eqn 2.4.1}$$

Where q is the electron charge, n is the 2DEG carrier sheet density in the channel, v is the effective electron velocity in the channel, and W is the width of the device, as shown in **Figure 2.1.1**.

As discussed in **Section 2.4.1**, in a HEMT, the carrier density in the channel and the metal gate can be regarded as a parallel plate capacitor. If the relative permittivity of the material between gate and channel is constant and the layers between gate and channel are completely depleted, the gate voltage can then be expressed as:

$$V_{gs} = \frac{nqh}{\varepsilon} \qquad \textbf{Eqn 2.4.2}$$

Where h is the separation between gate and channel, ε is the relative permittivity of the semiconductor material layers between gate and channel.

The transconductance g_m of the device is defined as the rate of change of drain current with the voltage applied on gate at a constant drain voltage [2.19]:

$$g_m = \left(\frac{\partial I_d}{\partial V_{gs}}\right)_{V_{ds}} \qquad \textbf{Eqn 2.4.3}$$

Therefore, transconductance g_m can be extracted by calculating the derivative of the drain current I_d with respect to the gate voltage V_{gs}:

$$g_m = \frac{\varepsilon v W}{h} \qquad \textbf{Eqn 2.4.4}$$

As a consequence, the transconductance will be increased when the electron velocity is high in the channel or by reducing the gate-channel separation.

The transconductance given in **Eqn 2.4.4** is based on the assumption that all the gate voltage is applied across the channel in the gate region. In reality, however, the gate voltage also drops across the source resistance R_s [2.20]. Therefore, the actual gate voltage between the gate and channel V_{gs0} is:

$$V_{gs0} = V_{gs} - I_d R_s \qquad \textbf{Eqn 2.4.5}$$

And hence the extrinsic transconductance g_m can be expressed as:

$$g_m = \frac{g_{m0}}{1 + g_{m0} R_s} \qquad \textbf{Eqn 2.4.6}$$

Where g_{m0} is the intrinsic transconductance.

From **Eqn 2.4.6**, the extrinsic transconductance and intrinsic transconductance will be equal when source resistance is zero, and considerably different when source resistance is large.

In addition to the transconductance, the output conductance of the device, g_{ds}, is defined as [2.21]:

$$g_{ds} = \left(\frac{\partial I_d}{\partial V_{ds}}\right)_{V_{gs}} \qquad \textbf{Eqn 2.4.7}$$

which is the inverse of the output resistance defined between source and drain, i.e. $1/R_{ds}$, at a fixed gate voltage.

2.5 HEMT frequency response and equivalent circuit

The HEMT is usually in common-source configuration, and the source terminal is grounded. The input port of a HEMT is between gate and source, whilst the output port is between drain and source. When a HEMT is operated at high frequencies, the small signal equivalent circuit model can be constructed, which allows the operation of the device to be characterised in terms of lumped circuit elements. The intrinsic device model, which represents the equivalent circuit elements in the region below the gate, is shown in **Figure 2.5.1** [2.22-2.23].

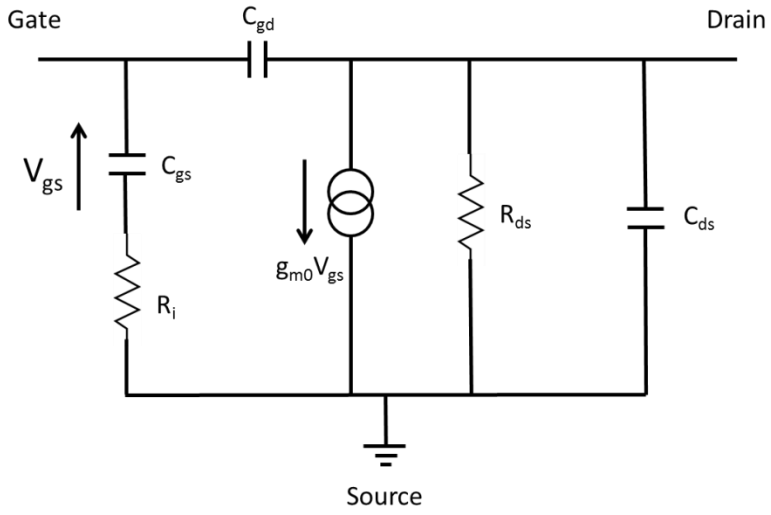


Figure 2.5.1 – Equivalent circuit of the intrinsic device model

The modulation of the current in the channel between source and drain is represented by a current generator, generating the current equal to the intrinsic transconductance multiplied by the voltage across gate capacitance, i.e. $g_{m0}V_{gs}$, which is in parallel with the resistor R_{ds} representing the effective output resistance of the device. The gate capacitance represents the capacitive coupling of the gate to the channel, comprises two elements: C_{gs} and C_{gd}, which represent the capacitances across the depletion region of the gate to the source side or the wider depletion region to the drain side respectively, and depend on the exact depletion region geometries. The resistor R_i in series with C_{gs} represent the resistance of the intrinsic section of the channel. There is also a capacitance, C_{ds}, between the source and drain side of the intrinsic

region, resulting from their different electron densities. These elements representing the intrinsic device model are listed in **Table 2.5.1**.

Element	Symbol	Description
Current source	$g_{m0}V_{gs}$	Channel current modulation
Output resistance	R_{ds}	Inverse of output conductance
Source-end gate capacitance	C_{gs}	Capacitance across the gate depletion region to the source side
Drain-end gate capacitance	C_{gd}	Capacitance across the gate depletion region to the drain side
Intrinsic channel resistance	R_i	Models the finite conductance of the channel
Source-drain capacitance	C_{ds}	Across depletion region from drain to source

Table 2.5.1 – Intrinsic equivalent circuit elements

There are additional parasitic elements in the extrinsic region of the device, which can be collected together in the full equivalent circuit model of the HEMT presented in **Figure 2.5.2**.

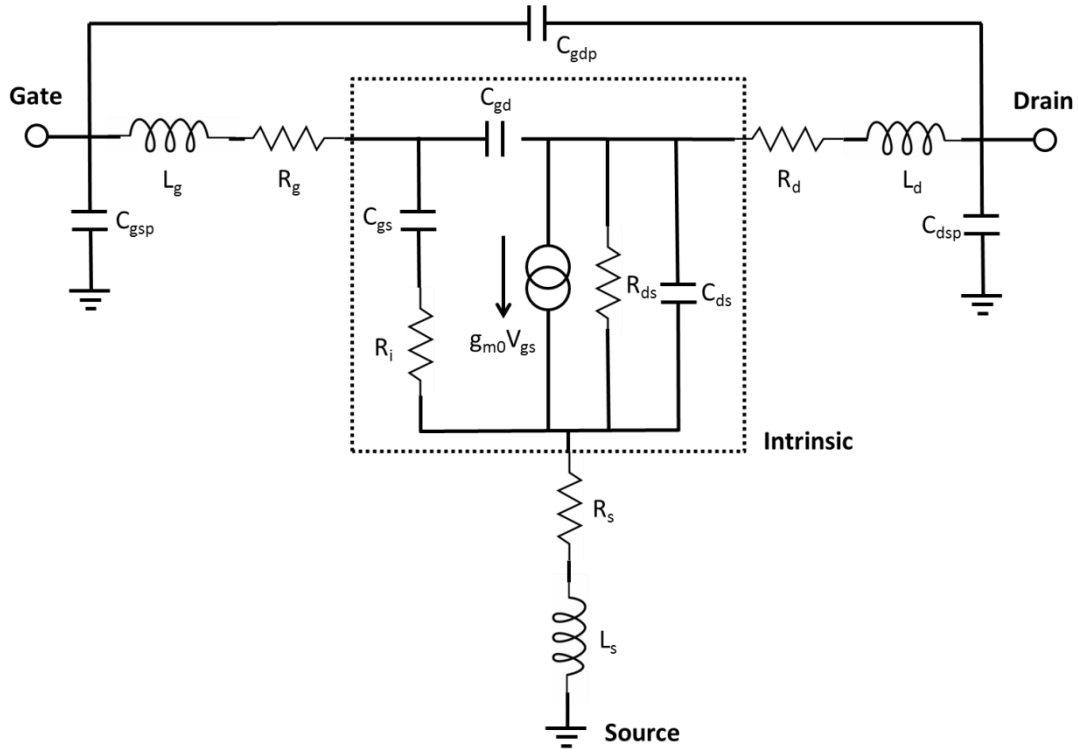


Figure 2.5.2 – Complete equivalent circuit model of HEMT including intrinsic (dotted box) and extrinsic elements (outside dotted box)

The parasitic source and drain resistances R_s and R_d (also shown in **Figure 2.4.4**) include the contact resistances: R_{sc} and R_{dc}, which represent the resistance of the contact through the ohmic region to the channel, and the parallel access resistances: R_{sp} and R_{dp}, representing the resistance from the ohmic contact region to the gate region through the channel. The parasitic capacitances C_{gsp} and C_{gdp} result from the electric field distribution between metallic contacts. The gate, source and drain parasitic inductances L_g, L_s, L_d arise from feed pads of the electrodes. The resistor R_g represents the resistance of the gate metal.

The HEMT device can be regarded as a two-port network in RF characterisation, with the gate at port 1 as input and drain at port 2 as output. The source of the device is grounded.

An important figure of merit in RF performance of HEMT is cutoff frequency f_T [2.24], which is defined as the frequency at which short circuit current gain falls into unity, i.e. the current flowing into gate equals to the current flowing from drain when the output is short circuited.

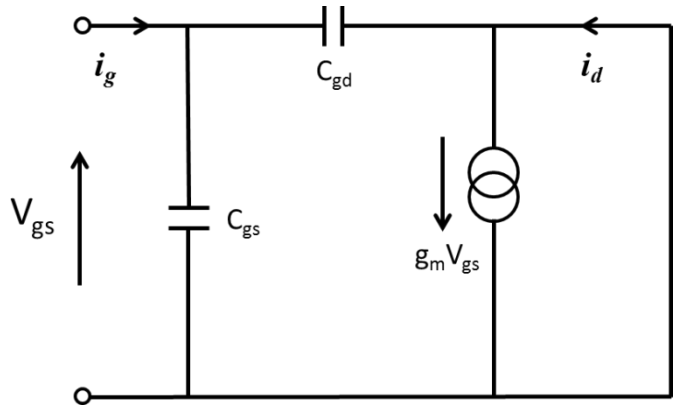


Figure 2.5.3 – Intrinsic gate-channel model for extracting f_T

From the circuit in **Figure 2.5.3**, the input current i_g and output current i_d can be expressed respectively as:

$$i_g = \frac{V_{gs}}{\left(\frac{1}{jw(C_{gs}+C_{gd})}\right)} = jw(C_{gs}+C_{gd})V_{gs} \qquad \textbf{Eqn 2.5.1}$$

$$i_d = g_m V_{gs} \qquad \textbf{Eqn 2.5.2}$$

The short circuit current gain is:

$$A_i = \frac{i_d}{i_g} = \frac{g_m}{jw(C_{gs} + C_{gd})} \qquad \textbf{Eqn 2.5.3}$$

$$|A_i| = \frac{g_m}{2\pi f(C_{gs} + C_{gd})} \qquad \textbf{Eqn 2.5.4}$$

The intrinsic cutoff frequency f_T can be extracted when $|A_i| = 1$:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \qquad \textbf{Eqn 2.5.5}$$

As a consequence, the intrinsic f_T can be increased by reducing the total gate capacitance and enlarging the transconductance.

The gate-channel capacitance C_g can be regarded as a parallel plate capacitor, and can be expressed as:

$$C_g = \frac{\varepsilon L_g W}{h} \qquad \textbf{Eqn 2.5.6}$$

Where L_g is the gate length as shown in **Figure 2.1.1**, W is the device width and h is the gate-channel separation.

Considering **Eqn 2.4.4** for the transconductance and **Eqn 2.5.6** for total gate capacitance, the intrinsic cutoff frequency f_T can be expressed as:

$$f_T = \frac{v}{2\pi L_g} \qquad \textbf{Eqn 2.5.7}$$

Therefore, the intrinsic cutoff frequency can be maximised by increasing the carrier velocity in the channel to enlarge the transconductance and reducing the gate length to decrease the gate capacitance.

When extrinsic parasitic resistances R_s, R_d and R_{ds} are considered into the analysis, the output current will not be the current generated by the current generator $g_m V_{gs}$, and the extrinsic cutoff frequency is [2.25]:

$$Extrinsic\ f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)\left(1+\frac{R_s+R_d}{R_{ds}}\right)+C_{gd}g_m(R_s+R_d)} \qquad \textbf{Eqn 2.5.8}$$

Another important figure of merit in RF operation of HEMT is the maximum frequency of oscillation f_{max} [2.24], which is defined as the frequency at which the device has unity power gain, i.e. when the product of the voltage and current gains of the device equal one. The equivalent circuit of HEMT with a load resistance at output is presented in **Figure 2.5.4**.

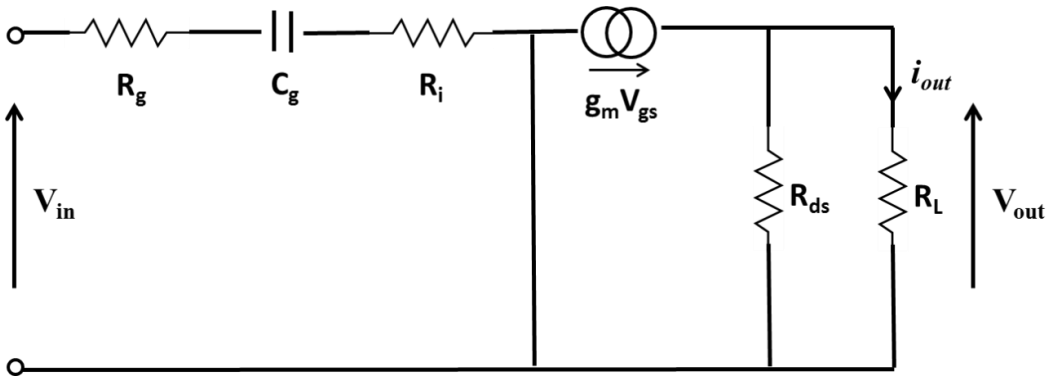


Figure 2.5.4 – Intrinsic Power amplification HEMT model with output load

According to the circuit shown in **Figure 2.5.4**, the maximum power gain across the load resistance will be achieved when the load resistance is equal to the output resistance of the device, i.e. R_{ds}=R_L.

The voltage gain of the circuit is [2.26]:

$$|A_v| = \left|\frac{V_{out}}{V_{in}}\right| = \frac{g_m R_o}{\sqrt{1+4\pi^2 f^2 {C_g}^2\left(R_g+R_i\right)^2}} \approx \frac{g_m R_o}{2\pi f C_g\left(R_g+R_i\right)} \qquad \textbf{Eqn 2.5.9}$$

Where R_o is the output resistance of the circuit, which is the total resistance of the parallel R_{ds} and R_L.

Since the load resistance is equal to the output resistance of the device, i.e. R_{ds}=R_L, hence $R_o = \frac{1}{2}R_{ds}$, $i_{out} = \frac{1}{2}i_d$. Therefore,

$$|A_v| = \frac{g_m R_{ds}}{4\pi f C_g\left(R_g + R_i\right)} = \frac{f_T R_{ds}}{2f\left(R_g + R_i\right)} \qquad \textbf{Eqn 2.5.10}$$

Similar to the previous discussion about **Eqn 2.5.4**, and considering the total output resistance of the circuit is half of R_{ds}, the current gain of the circuit is:

$$|A_i| = \frac{i_{out}}{i_{in}} = \frac{g_m}{4\pi f C_g} = \frac{f_T}{2f} \qquad \textbf{Eqn 2.5.11}$$

The power gain can then be expressed as:

$$G_p = |A_i||A_v| = \left(\frac{f_T}{f}\right)^2 \frac{R_{ds}}{4\left(R_g + R_i\right)} \qquad \textbf{Eqn 2.5.12}$$

Therefore, the intrinsic maximum frequency of oscillation can be extracted by applying G_p=1:

$$Intrinsic\ f_{max} = \frac{f_T}{2}\sqrt{\frac{R_{ds}}{R_g + R_i}} \qquad \textbf{Eqn 2.5.13}$$

Therefore, the intrinsic maximum frequency of oscillation can be increased by maximising the cutoff frequency and output resistance, reducing the intrinsic resistance and gate resistance.

Similarly, if extrinsic parasitic elements are considered, the extrinsic maximum frequency of oscillation can be expressed as [2.27]:

$$Extrinsic\ f_{max} = \frac{f_T}{2\sqrt{\frac{R_g + R_i + R_s}{R_{ds}} + 2\pi f_T R_g C_{gd}}} \qquad \textbf{Eqn 2.5.14}$$

According to **Eqn 2.5.8** and **Eqn 2.5.14**, decreased gate length and hence the reduced gate capacitance results in the increased f_T and f_{max}. However, gate resistance will increase linearly as gate length decreasing, as **Eqn 2.5.15** shows, which leads to a low f_{max}.

$$R_g = \rho \frac{W}{L_g T} \qquad \textbf{Eqn 2.5.15}$$

where W is the device width, L_g is the gate length, T is the height of the gate.

To satisfy the requirements of both small gate length and low gate resistance, a T-gate structure of a short gate foot topped by a large gate head is utilised in gate formation of HEMT, as shown in **Figure 2.5.5**.

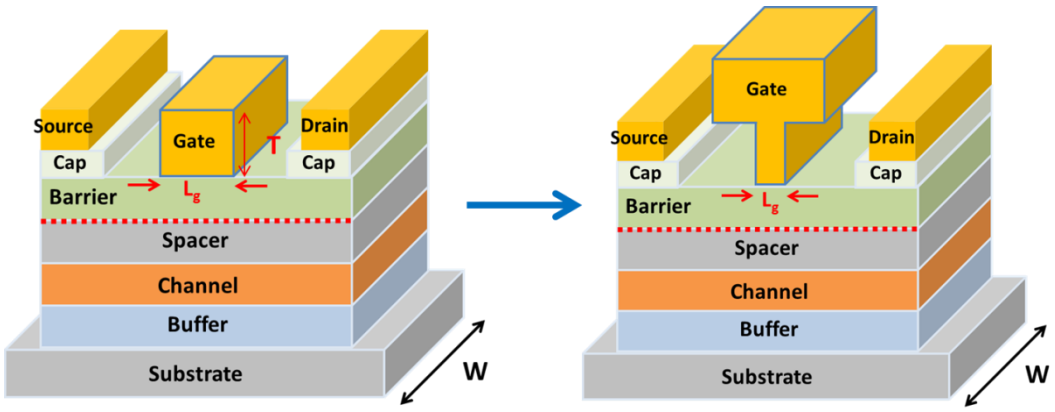


Figure 2.5.5 – HEMT layout of normal gate and T-gate

2.6 Summary

To better understand HEMT operation, several aspects are introduced in this chapter, including:

- 2DEG formation relies on the heterostructure formation between two semiconductors with different bandgaps, which is the key advantage of high mobility of HEMT.
- Schottky and ohmic contacts for gate and source/drain of the device, which are the basis of controlling the device by applying external voltages.
- The working theory of the HEMT at both DC and high frequencies. Important figures of merit are derived for the evaluation of device performance. The properties of semiconductor material and structure of the device, which influence the figure of merit of the device performance, are also included.

With the understanding of the operation theory of a HEMT, the practical fabrication process of the HEMT will be discussed in the next chapter.

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Chapter 3

Fabrication techniques

In this chapter, various fabrication techniques for semiconductor device realisation in particular HEMT fabrication are described, including lithography, metallisation, lift off and etching processes. A standard HEMT fabrication process flow based on these generic fabrication techniques is then presented. All of these fabrication techniques were used extensively in the work presented in **Chapter 6** & **Chapter 7**.

3.1 Electron beam lithography

In HEMT fabrication, electron beam lithography is the essential process technology to form key functional parts of the device, in particular nanoscale gates and source/drain contacts. Although highly advanced photolithography technology is successfully used in industry due to the shorter writing time for mass production compared to electron beam lithography, electron beam lithography is widely used in research labs for nanoscale pattern realisation due to the flexibility offered by software masks.

The approach to defining structures on semiconductor materials by electron beam lithography and photolithography is similar. The patterns are transferred onto the semiconductor material using a layer or layers of resist, which are spin coated and subsequently baked to remove the casting solvent prior to exposure. After the lithography step, the resist is developed to define the required structure. In the development step, the sample is immersed in a developer solution and the exposed (unexposed) area of resist will be removed for positive (negative) resists. The sample is then ready for subsequent processing, which typically is either an etching or metal deposition step.

The exposure process for electron beam lithography and photolithography is very different. In photolithography, the source is UV light; a mask plate is placed between this and the substrate, which allows the transmission of light through the transparent pattern on the mask onto the corresponding area of the resist. In electron beam lithography, the exposure of the resist is from the bombardment of a focussed electron beam and the desirable patterns are written directly onto the resist with no need for a hard mask plate as in photolithography. The patterns to be written on the resist are designed in software and transferred to a computer controlled electron beam lithography system which generates a focussed electron beam which is scanned across the sample to form the desired patterns.

3.1.1 Electron beam lithography tool

The electron beam lithography tool utilised in this work was a Vistec VB6 UHR EWF housed in a Class 10 cleanroom in the James Watt Nanofabrication Centre at University of Glasgow. A schematic of Vistec VB6 electron beam lithography tool is shown in **Figure 3.1.1** [3.1].

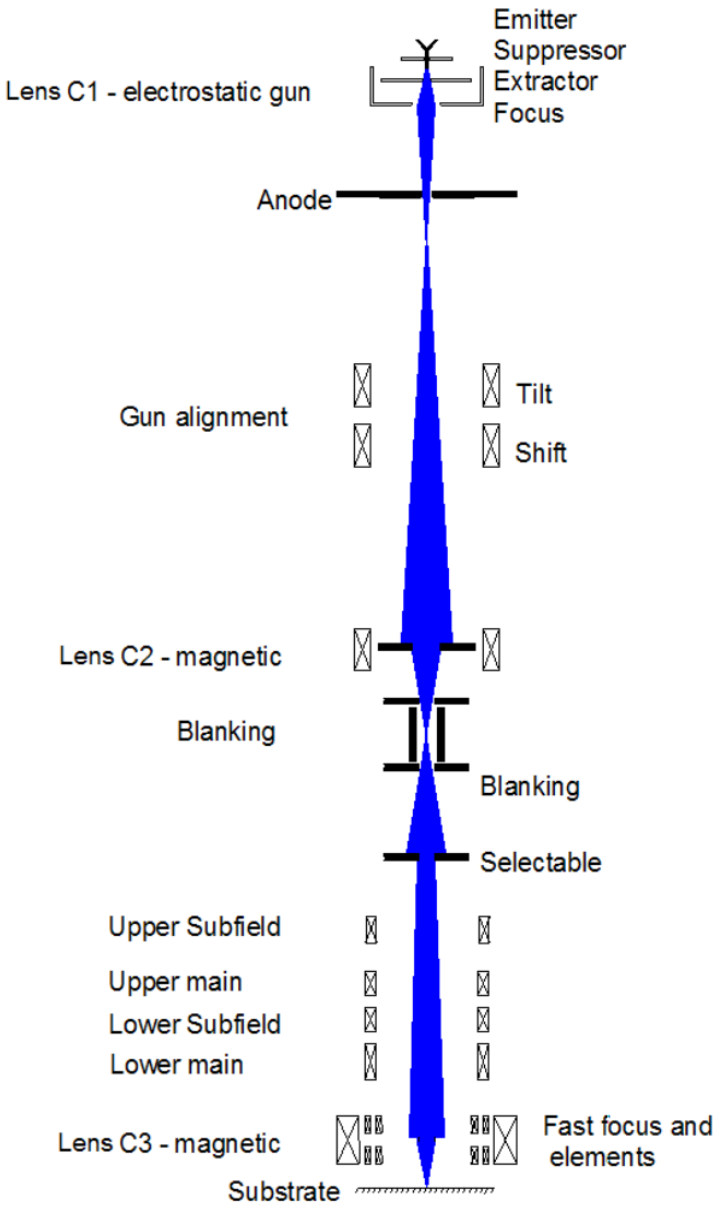

Figure 3.1.1 – Basic layout of Vistec VB6 electron beam lithography system [3.1]

As presented in **Figure 3.1.1**, there are a series of magnetic and electrostatic lenses in the electron beam lithography system to generate and confine the electron beam. The electrostatic lens C1 is at the source in the system. The electron beam is sourced from a Schottky field emission gun using a zirconium oxide coated tungsten cathode, which is heated up to 1800 K. The cathode is usually biased up to accelerating voltage of 100 kV by the column high voltage (HT) source. The "Suppressor" electrode ensures that electrons are only emitted from the cathode tip. The "Extractor" electrode creates a high electric field between it and the cathode, which controls the thermal field emission from the source and the electron acceleration to the "Extractor" electrode. The "Focus" electrode focuses the electron beam before electrons reach the "Anode". The "Gun alignment coils" are used to align the electron beam to the optical axis of the column. Several apertures are used in the system at various positions in the column to reduce the divergence of the electron beam for generating a given spot size of the electron beam. A further condenser magnetic lens C2 allows adjustment of the spot size without changing the focus and beam current. The final magnetic lens C3 focuses the electron beam onto the substrate at a given working distance. The electron beam can be electrostatic deflected into an aperture by using the beam blanker. There are a series of magnetic coils in the system above the final lens C3, which deflect the beam to scan in the x and y axes. There are two types of deflectors in the deflection unit, located between the lenses C2 and C3. The main deflectors are for large scale movements of the beam and the subfield deflectors are for fine controlling of the beam. The stage holding the substrate is moved during exposure when the pattern area of the substrate is greater than 1.3 mm in either x or y, which is the maximum area covered by the deflectors unit. The apertures in the system can be used to adjust the beam size and current in the pattern writing process. The largest current and spot size are 131 nA and 45 nm respectively, which can be used to write large pattern areas in short time. The smallest current and spot size are 1 nA and 4 nm respectively, which can be used to precisely form nanoscale features.

3.1.2 Pattern design and definition

The desired patterns to be written on the substrate by electron beam lithography are designed in a CAD package. In this work, the Tanner EDA tool L-Edit was used. The designed patterns are exported in the GDSII file format which is then fractured by Layout Beamer software from GenISYS Gmbh, which generates vep files. Several parameters of the vep file of each layer of the desired pattern can be set up in the "Belle" software, which was created by Dr. Stephen Thoms of the University of Glasgow. The parameters set up in Belle software include exposure dose value, spot size, beam current, the relative position of the pattern to the substrate, and even the detailed information of alignment markers if needed. The output file from Belle is subsequently read by a computer which controls the electron beam lithography system. This processes all the necessary information of the patterns needs to be written on the substrate.

3.1.3 Resists

Resists used in electron beam lithography play an important role in the formation of the final desired pattern. They are usually chosen to be written depends on different applications. The molecular weight of the resist determines the resist sensitivity [3.2], which will be reduced when molecular weight of the resist is increased. The resist sensitivity needs to be considered as a key factor impacting the formed pattern in electron beam lithography, since more sensitive resist requires lower exposure dose or shorter development time for a given pattern. In addition, several layers of resists with different sensitivities can be combined to be used in various fabrication processing such as lift off and T-gate formation, which will be described in **Section 3.2** and **Section 3.4.4** respectively.

Various types of resist were used for the fabrication in this work, which are outlined in **Table 3.1.1**.

Resist	Type	Application
PMMA	Positive	General Electron beam lithography
LOR	Positive	Undercutting for T-gates (Better lift off)
UVIII	Positive	T-gates
HSQ	Negative	Dry etch mask

Table 3.1.1 – Resists used in this work for various applications

Poly-methyl methacrylate (PMMA) is a positive tone electron beam resist of various molecular weights and can be used in a wide range of fabrication processing [3.3]. There are two types PMMA with different molecular weights available in James Watt Nanofabrication Centre of the University of Glasgow: PMMA 2010 and PMMA 2041, which were used in this work. PMMA 2010 is more sensitive than PMMA 2041 due to the smaller molecular weight. PMMA are usually dissolved in solvents typically ethyl lactate, with different concentrations. PMMA resists are generally developed in methyl isobutyl ketone (MIBK) diluted with isopropyl alcohol (IPA).

Lift off resist (LOR) is based on polydimethyglutarimide (PGMI) and can provide undercut profile for lift off processes, without intermixing with other resists. In this work, LOR is utilised in lift off process, together with PMMA and UVIII, for T-gate formation.

The Shipley Ultra Violet III (UVIII) is a positive tone chemically amplified resist. The incident electrons result in the formation of acids in the chemically amplified resist, which can catalyse reactions in the exposed areas during the development process [3.4]. UVIII is a copolymer of styrene and t-butyl acrylate, and was originally designed for deep ultra violet (DUV) optical lithography but has also been used in electron beam lithography [3.5]. UVIII is generally developed in MICROPOSIT MF CD-26 developer.

Hydrogen silsesquioxane (HSQ) is a negative tone electron beam resist, and is based on silicon dioxide with available Si-H bonds. Electron beam exposure can break Si-H bonds and

cause crosslinking [3.6]. HSQ is generally developed in diluted tetramethylammonium hydroxide (TMAH).

3.2 Metallisation and lift off

After the desired patterns have been defined in the resist on the semiconductor material by electron beam lithography, one of the following process steps is metallisation to form metal contacts of the device including source/drain, gate and bondpads, or alignment markers to facilitate layer to layer registration.

All metallisation throughout this work was performed on electron beam evaporation tools: Plassys MEB 450 and Plassys MEB 550. Electron beam evaporation uses an electron beam to locally heat up the surface of a metal target until a temperature at which the metal vaporises is reached. The metal atoms move to the sample, hit the surface, cool down and finally adhere to the sample surface. The evaporation processes occur in a vacuum chamber with pressure in the order of 10^{-6} – 10^{-7} Torr. A non-conformal metal layer with little or no sidewall coverage is produced by the electron beam evaporation metallisation, which will be beneficial for the following lift off processes.

In the metallisation process step, the desired metal is deposited onto the whole sample surface but only the metal deposited in the exposed area of the resist forms the metallic contacts to the semiconductor material. The rest of the metal film deposited on the resist coated sample can be “lifted off” when removing the resist by rinsing the sample in a solvent such as acetone. Therefore, the original pattern defined on the resists layers is now transferred onto the metal deposition layer on the substrate by the process of metallisation and lift off, as illustrated in **Figure 3.2.1**.

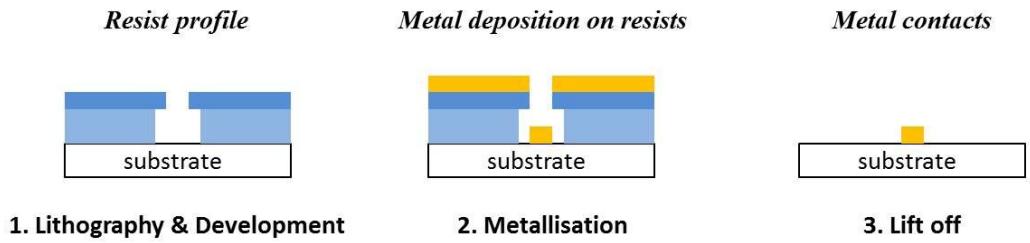

Figure 3.2.1 – Metallisation and lift off process

One thing of note is that a bi-layer of resists with different sensitivities is usually utilised in the lift off process. In the electron beam lithography process, as discussed in **Section 3.1.3**, the top resist layer with lower sensitivity is less exposed than the bottom resist layer with higher sensitivity when same exposure dose applied on both resist layers, which produces an undercut in the resist profile, as shown in **Figure 3.2.1**. It reduces the metal deposited on the sidewall of the resist profile, generates a discontinuity between the metal deposited on the surface of resist and in the exposed area on the substrate, and provides a route for the acetone solvent to access the resist; all of which facilitate the lift-off process.

There are two essential steps after electron beam lithography and development and before metallisation in metal contacts formation; i) ashing and ii) de-oxidation treatment. The ashing step is preformed after the resist development and is a low power oxygen plasma etching process to remove any organic resist residues remaining the exposed area on the substrate. The de-oxidation treatment is subsequently performed immediately before the metallisation process to remove any native oxide formed on the surface of exposed semiconductor material by rinsing the sample in a dilute acid solution for a very short while and then in the de-ionised water.

3.3 Etching

After electron beam lithography definition of the desired resist pattern, wet chemical, plasma or reactive ion etching processes can be used to selectively remove material on the substrate using resist as a mask.

The wet etching process relies on a chemical reaction between the material to be etched and the chemicals in the etchant solution, and the process is influenced by several factors including solution composition, concentration, pH value, temperature of the etchant solution, and duration of the process. The choice of etching solution can enable selective remove of material due to the particular chemical reaction occurring in process. For instance, in InAlAs/ InGaAs HEMT structure, the succinic or citric acid and hydrogen peroxide mixture etchant reacts with gallium-contained layers not aluminium-contained layers. This can be used in a recess etch step prior to the gate metallisation in HEMT fabrication to selectively remove the InGaAs cap layer stopping at the InAlAs barrier layer [3.7]. An orthophosphoric acid and hydrogen peroxide mixture etchant reacts with both gallium-contained and aluminium-contained layers, which therefore can be used in a mesa isolation step of HEMT fabrication to etch down to the buffer layer and remove all the active layers. The gate recess etch and mesa isolation approaches will be described in detail in **Section 3.4**. The concentration, pH value and the temperature of the etchant solution influence the etching rate and hence the roughness of the etched surface, since the higher etching rate may cause rapid gas evolution leading to a rougher etched surface [3.8]. The final etching depth is mainly controlled by the duration of etching. The advantages of wet etching are that it is a simple process, it is low cost and damage free. However, it is difficult to control the wet etching process precisely and the uniformity of the wet etching processes is also an issue.

Dry etching processes are usually used in the definition of high aspect ratio features and/or when precise etching depth is required. In the dry etching system, chemical etching, chemical passivation and physical bombardment are used to make anisotropic etching possible and

produce high aspect ratio etching profiles, whilst the etching depth can be monitored by laser interferometric techniques [3.9]. In a dry etch process, many parameters can affect the final etching profile including etching gas composition, gas ratio, chamber pressure, power levels and also temperature of the sample to be etched. The main disadvantage of dry etching processes is that the etching process may introduce damage which has the potential to significantly decrease the carrier mobility of the active layer and therefore compromise the device performance, particularly in III-V compound semiconductor devices [3.10-3.12]. Some low damage dry etching processes achieved by adjusting various parameters in particular power levels, have been reported for III-V device fabrication [3.13- 3.16].

3.4 Standard HEMT fabrication process flow

The generic process flow of HEMT realisation using the process techniques introduced above includes the following five fabrication steps:

1. Alignment markers

2. Mesa Isolation

3. Ohmic Contacts

4. Gates

5. Bondpads

The sequence of these five fabrication steps is usually as listed above, although it may change depending on a specific device configuration. For instance, in a self-aligned gate process, gates are defined prior to ohmic contacts formation, in order to minimise the separation of source and drain and hence to reduce source and drain parasitic resistances.

These five main components of HEMT fabrication will be discussed in the following sections.

3.4.1 Alignment markers

The first step is usually to define registration markers on a blank substrate to enable alignment of the multiple levels required to realise a completed device. For example, the gate has to be accurately placed between the source and drain contacts. In this work, the alignment markers consist of "global" markers and "cell" markers. The choice of which will be determined by the level of registration accuracy required between various levels. The use of "penrose" patterns as cell markers can facilitate alignment accuracy of better than 5 nm, although it does increase the complexity of the alignment process [3.17-3.18]. The basic layout of markers is illustrated in **Figure 3.4.1**.

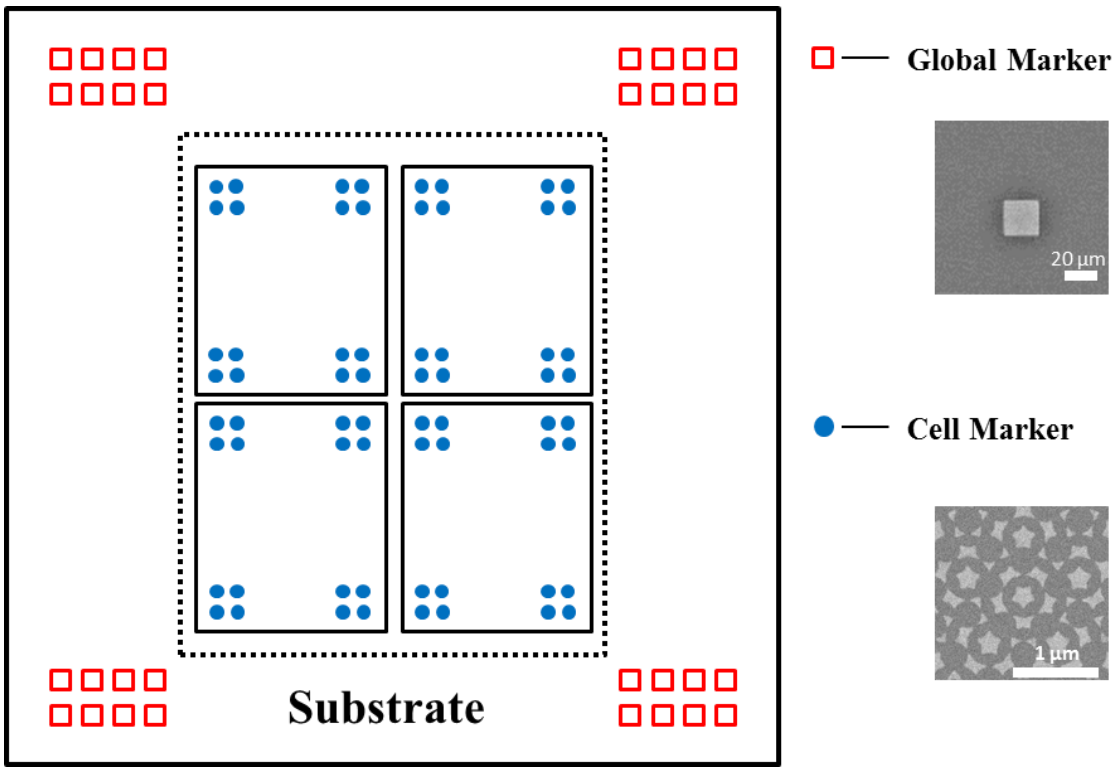

Figure 3.4.1 – The schematic layout of markers (global & cell) on the substrate

The markers are fabricated by electron beam lithography, metallisation and lift off process as introduced above. Two layers of resists with different sensitivities containing 4% PMMA 2010 and 2.5% PMMA 2041, as discussed in **Section 3.1.3**, are used for electron beam lithography and 10nm Ti/70nm Au are electron beam evaporated and then lifted off to form markers. The thickness and the composition of metals of markers are chosen to generate enough contrast to make them distinguishable by the electron beam lithography tool in subsequent lithography step. The contrast is related to the thickness of markers and atomic number difference between the substrate material and the metal of marker.

3.4.2 Mesa isolation

The mesa isolation step is to isolate individual devices from each other by removing the active layers (cap, barrier, and channel layers in **Figure 2.1.1**) completely and down to buffer

layer which is underneath the channel, as shown in **Figure 3.4.2**. This step is aligned to the alignment markers defined in the previous processing step.

Figure 3.4.2 – Mesa Isolation process

In this work, a wet etching process is used to remove all active layers including the InGaAs cap layer, InAlAs barrier layer, InGaAs channel, and part of the InAlAs buffer layer. A non-selective orthophosphoric acid/hydrogen peroxide etchant with a concentration ratio of 1:1:100 H_3PO_4 : H_2O_2 : H_2O was used to remove these III-V material layers, since both gallium and aluminium are contained in these layers. This produces a controllable and repeatable etch rate of 0.7 nm/s.

The etched depth was measured by Atomic Force Microscopy (AFM) to confirm that all the active layers and part of buffer layer below the channel are removed. The minimum possible etch depth is targeted sufficient to achieve electrical isolation, to minimise the chance of having discontinuity of gate metal which will ultimately have to cross the height step between the active "mesa" and isolated material in subsequent processing steps. The target etch depth is dependent on the thickness of the material layers as well as the height of the metal gate of the device.

3.4.3 Ohmic contacts

The ohmic contacts are aligned to the device mesa by registering to the alignment marks defined previously. As discussed in **Section 2.3**, ohmic contacts are generally defined on a

highly doped cap layer to obtain low contact resistance in a HEMT. In the InAlAs/ InGaAs material system, the cap is a heavily n-doped layer of InGaAs. Most ohmic contacts are formed by metallisation and a following annealing process to produce an alloyed metal contact, which reduces the magnitude of the Schottky barrier. A gold/germanium based metallisation is commonly used in annealed ohmic contact formation for III-V HEMTs [3.19], as annealing causes germanium to diffuse into the InGaAs cap layer to form a highly doped region which promotes electron tunnelling between the contact metal and the semiconductor with a low resistance. Gold is included to provide high conductivity. Non-annealed ohmic contacts can also be achieved by introducing additional doping plane in the barrier layer close to the cap layer [3.20].

Figure 3.4.3 shows a Scanning Electron Microscope (SEM) top view of typical ohmic contacts. It can be seen from **Figure 3.4.3** that source and drain are aligned to the device mesa.

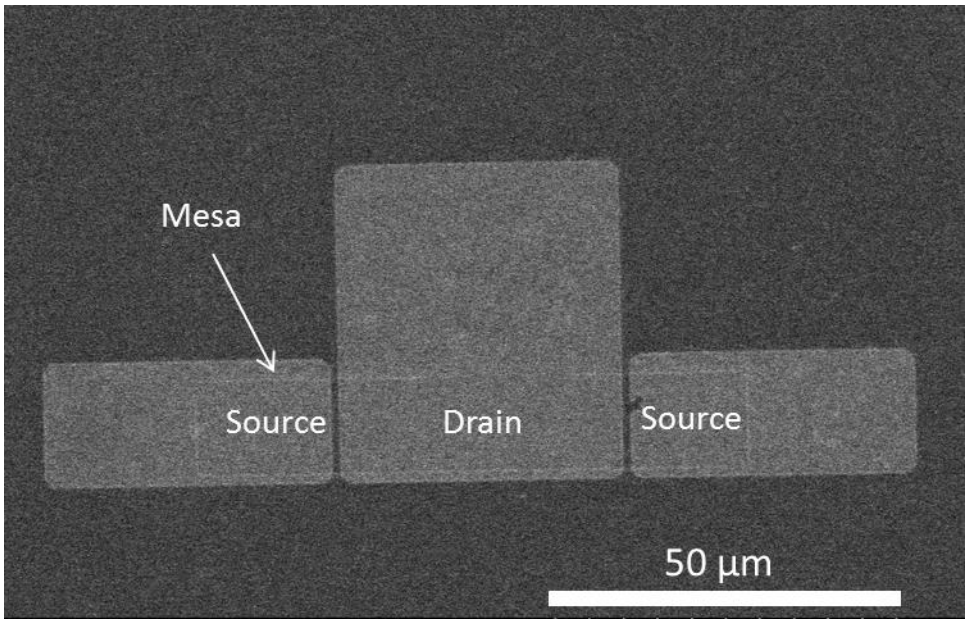

Figure 3.4.3 – Top view of typical ohmic contacts

3.4.4 Gates

As will be discussed in **Chapter 5**, there are a number of processes to fabricate T-gates [3.21-3.22]. In this work, the general method is to use three layers of resists consist of UVIII, PMMA and a very thin layer of LOR between them which enable a single step electron beam lithography strategy for T-gate fabrication, as shown in **Figure 3.4.4**.

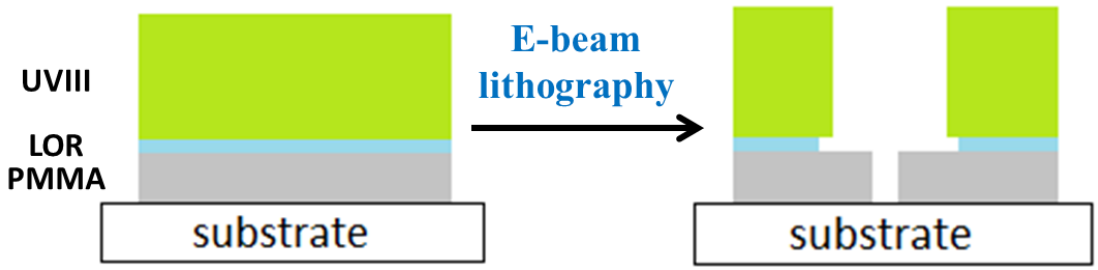

Figure 3.4.4 – T-gate formation using three layers of resists: UVIII, LOR, PMMA

There is an essential recess etch process following the T-gate resist profile formation by electron beam lithography and prior to the gate metallisation. A selective wet etching process is used to remove the highly doped cap layer of HEMT. The gate therefore is deposited on the undoped, large bandgap InAlAs barrier layer. This minimises the gate leakage current. In this work, a succinic acid/ hydrogen peroxide based etch with pH of 5.5 was used to selectively remove the InGaAs cap layer, stopping on the InAlAs barrier layer.

Following the recess etch step, gates are formed by a metallisation and lift off process. An electron beam evaporated 15nm Ti/15nm Pt/160nm Au metal stack was used as titanium provides good adhesion to the semiconductor, high conductivity gold forms the bulk of the gate to minimise resistance and platinum acts as a barrier layer to prevent gold diffusion into the InAlAs layer, which would result in a poor Schottky contact.

3.4.5 Bondpads

Bondpads are required to connect the source, drain and gate of a HEMT to the outside world to enable the measurements of the device from DC to RF frequencies. The bondpads are designed as ground-signal-ground coplanar waveguide topology. The geometry of the bondpads is determined to make the impedance of the bondpads match with that of the measurement system. The bondpad generally consists of a 50 nm NiCr as the adhesion layer and a 1.2 µm Au metal layer to minimise the access resistances to the three terminals of the device. The realisation of bondpads requires lithography, metallisation and lift off processes. A bi-layer resist stack of 15% PMMA 2010 and 4% PMMA 2041 is used to generate 1.5 µm resist profile, which is thick enough to lift off the 1.2 µm NiCr/Au metal layer which deposited by electron beam evaporation.

The complete HEMT device geometry is shown in **Figure 3.4.5**.

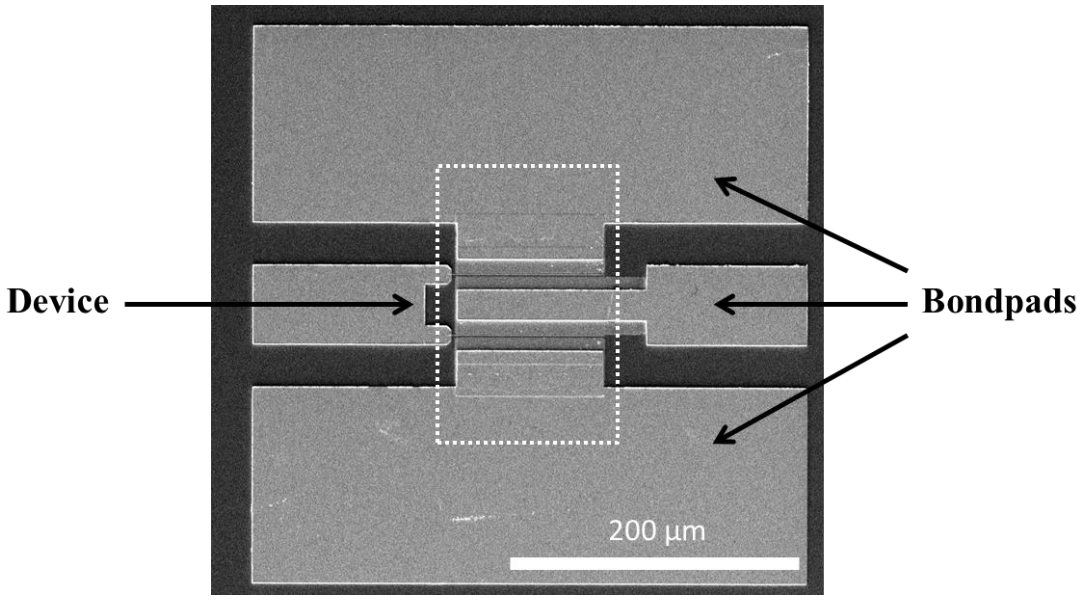

Figure 3.4.5 – Complete HEMT device geometry

3.5 Summary

This chapter describes a standard HEMT fabrication process flow including five steps: alignment markers definition, ohmic contact formation, gate fabrication and bondpad realisation. Fabrication process techniques are also introduced in this chapter, including lithography, metallisation, lift off and etching, which can be used to realise the five steps mentioned above. In the following chapters, the application of these process technologies in device fabrication will be presented.

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Chapter 4

Characterisation and Metrology

In **Chapter 3**, various process techniques to fabricate HEMTs have been introduced. It is important to evaluate whether the desired device realised by those fabrication techniques is achieved. Therefore, it is crucial to characterise the performance not only of the final realised transistors, but also of various test structures during the device process flow which provide information on individual process steps.

In this chapter, various characterisation methods are presented, including the Van der Pauw method for evaluating the properties of material structure, the Transmission Line Method for understanding the resistance behaviour of metal-semiconductor contacts after the source/drain ohmic contacts formation, and also the method of measuring the final device at both DC and RF frequencies.

4.1 Material characterisation and the Van der Pauw method

The quality and structure of the epitaxial material for HEMT fabrication determines the performance of the final device to a great extent. The carrier concentration and carrier mobility of the active layers affect the drain current of the device. The effective scaling of the material layer structure is beneficial for achieving a large transconductance device. Therefore, it is crucial to characterise the properties of material grown for HEMT fabrication and hence understand the possible performance that the device can achieve.

The Van der Pauw method [4.1] can be used to measure the carrier concentration, carrier mobility and sheet resistance of the material. It relies on the Hall Effect as applied to a symmetric four point structure, as shown in **Figure 4.1.1**.

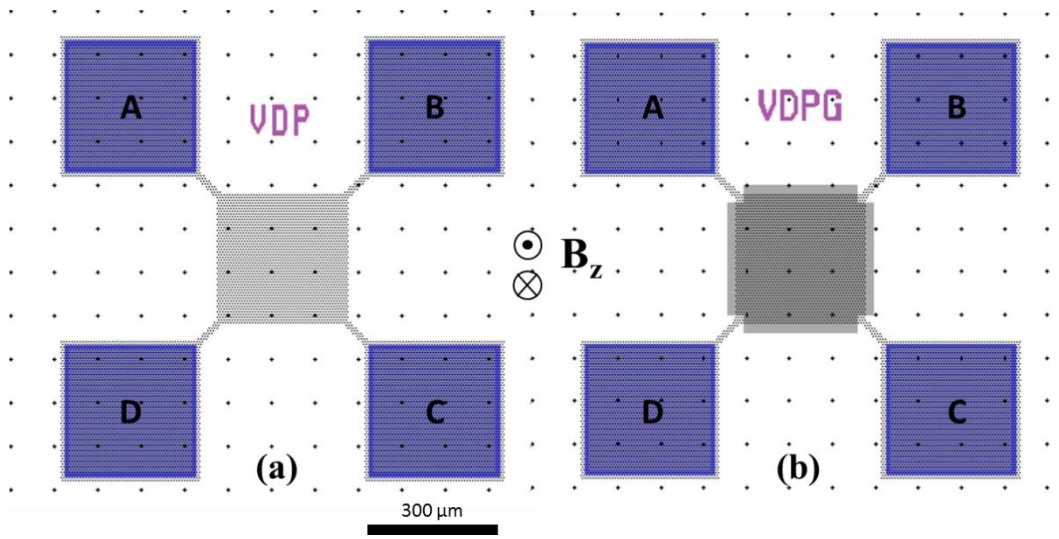

Figure 4.1.1 – Van der Pauw structures with and without cap layer

The Van der Pauw structure includes an isolated square of the active material to be characterised, which is contacted by four large metallic ohmic pads at the corners by narrow lines of active material. The four metallic pads are fabricated by metal evaporation of an AuGe metallisation and then annealed to form low resistance ohmic contacts to the square of active material at the centre of the test structure. The difference between structure (a) and structure (b) in **Figure 4.1.1** is that an additional recess etch step to remove the doped cap layer of the material in the centre area is applied on the sample (b) by selective etching.

Therefore, the material properties extracted by Van der Pauw method in structure (b) are of the channel layer alone.

When currents are applied between various pairs of the contact pads of the Van der Pauw structure, eg I_{DA} is a current driven between contacts D and A, the potential difference between adjacent pads can be measured, eg V_{AB}, where V_{AB} is the voltage difference measured between pads A and B. The following relation is demonstrated in [4.1]:

$$exp\left(-\pi\frac{t}{\rho}R_{AB,CD}\right)+exp\left(-\pi\frac{t}{\rho}R_{BC,DA}\right)=1 \qquad \textbf{Eqn 4.1.1}$$

Where t is the thickness of material sample, ρ is the resistivity of the material, and $R_{AB,CD}$ = V_{AB}/ I_{CD}, $R_{BC,DA}$ = V_{BC}/ I_{DA}, i.e. ratio of the voltage between one pair of adjacent probes to the current between another pair of adjacent probes. Because the Van der Pauw structure is symmetric, $R_{AB,CD} = R_{BC,DA}$, and **Eqn 4.1.1** simplifies to:

$$2exp\left(-\pi\frac{t}{\rho}R\right)=1 \qquad \textbf{Eqn 4.1.2}$$

Where $R_{AB,CD} = R_{BC,DA}=R$, and therefore:

$$\rho=\frac{\pi t}{ln2}R \qquad \textbf{Eqn 4.1.3}$$

Then the sheet resistance R_{sh} of the material defined as:

$$R_{sh}=\frac{\rho}{t} \qquad \textbf{Eqn 4.1.4}$$

can be extracted from **Eqn 4.1.3**:

$$R_{sh}=\frac{\rho}{t}=\frac{\pi R}{ln2} \qquad \textbf{Eqn 4.1.5}$$

The mobility and density of carriers in the material can be characterised by applying a magnetic field onto the sample.

If a magnetic field is introduced into the measurement environment, which is perpendicular to the surface plane of the material sample as labelled as $\mathbf{B_z}$ in **Figure 4.1.1**, and a voltage V_{AC} is

applied between contacts A and C, there will be a Lorentz force on carriers flowing in the material perpendicular to both the magnetic field and the electric field E_{AC}, according to the Hall Effect. Therefore, the direction of carriers movement is between contacts B and D. In the case where the majority carriers are electrons, these are moved by the Lorentz force along the direction between contacts B and D, which generates an electric field E_{BD} between contacts B and D with the electric field force direction opposite to that of Lorentz force. When the magnitude of the electric force increases to be same as the Lorentz force, an equilibrium state is reached. According to the equilibrium conditions:

$$qE_{BD} = qv_{AC}B_z \qquad \textbf{Eqn 4.1.6}$$

where v_{AC} is the velocity of carriers flowing between contacts A and C.

Hence the velocity of the carriers flowing between contacts A and C can be presented as the ratio of the magnitude of electric field between contacts B and D to the magnitude of magnetic field:

$$v_{AC} = \frac{E_{BD}}{B_z} \qquad \textbf{Eqn 4.1.7}$$

Therefore, the low-field carrier mobility μ can be expressed as:

$$\mu = \frac{v_{AC}}{E_{AC}} = \frac{E_{BD}}{E_{AC}B_z} \qquad \textbf{Eqn 4.1.8}$$

Besides, the current density $\boldsymbol{J_{AC}}$ between contacts A and C is related to the conductivity of the material σ (which is the reciprocal of resistivity ρ) and the electric field E_{AC} between contacts A and C, and can be expressed as an equation including carrier concentration *n*:

$$J_{AC} = \sigma E_{AC} = \frac{E_{AC}}{\rho} = nqv_{AC} \qquad \textbf{Eqn 4.1.9}$$

As a consequence, the carrier concentration of the material can be determined.

4.2 Contact resistance and the Transmission Line Method

The performance of a HEMT is influenced by not only the quality and structure of the epitaxial material, but also the quality of contacts of the device to the material layers. The quality of ohmic contacts formed between source/drain of the device and the channel affects the overall parasitic resistances of the device, which will degrade its performance, according to **Eqn 2.5.8** discussed in **Section 2.5**. Therefore, it is crucial to evaluate the quality of the ohmic contacts to ensure low contact resistances between source/drain and the channel for optimal device performance.

The Transmission Line Method (TLM) is usually utilised to characterise the contact resistances [4.2]. In the standard TLM structure, several ohmic contacts are deposited on the material with various separations. **Figure 4.2.1** shows a typical TLM structure with separations of 1.5, 2.5, 3.5, and 4.5 μm.

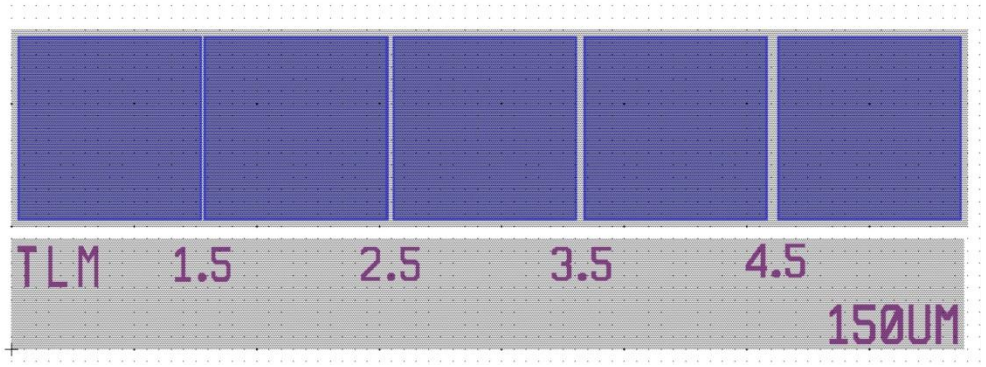

Figure 4.2.1 – Typical Transmission Line Method (TLM) structure with separations of 1.5, 2.5, 3.5, and 4.5 μm. The blue squares are metal contacts with the width of 150 μm, and the grey area underneath the blue squares is active material

The contact resistance can be extracted by measuring the total resistance between two adjacent contacts and generating a plot of resistance versus contacts separation. The resistance extracted from two adjacent contacts with a specified separation, **d**, comprises the resistance of the metal/semiconductor contact for each pad together with the resistance due to the

semiconductor material between the contacts which is related to the sheet resistance, scaled by the contact separation and the width of the contacts, as presented in **Figure 4.2.2**.

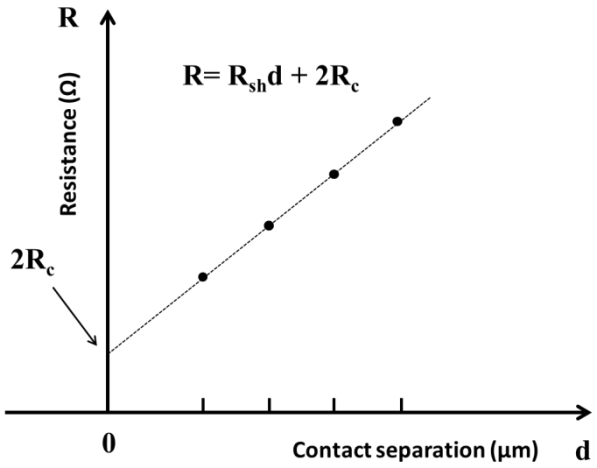

Figure 4.2.2 – Contact resistance extraction from Transmission Line Method (TLM)

The sheet resistance of the material $\mathbf{R_{sh}}$ can be determined from the gradient of the line and the contact resistance $\mathbf{R_c}$ from the Y-axis intercept.

The four-probe measurements technique is used in the Transmission Line Method. Currents are driven through two separate contacts, whilst the voltage between two separate contacts is measured by another two probes, which eliminates the effect of resistance of probes and cables on the measurements.

4.3 Device characterisation

Electrical characterisation of a HEMT includes measurements at both DC and RF frequencies. A general measurement system set up includes a probe station for conducting device measurements, a Semiconductor Parameter Analyser (SPA) and a Vector Network Analyser (VNA).

As described in **Section 3.4.5**, the fabricated HEMT is in a coplanar waveguide layout. Therefore, the three-signal probes in a ground-signal-ground configuration are used in both DC and RF measurements to match with the device layout, as presented in **Figure 4.3.1**.

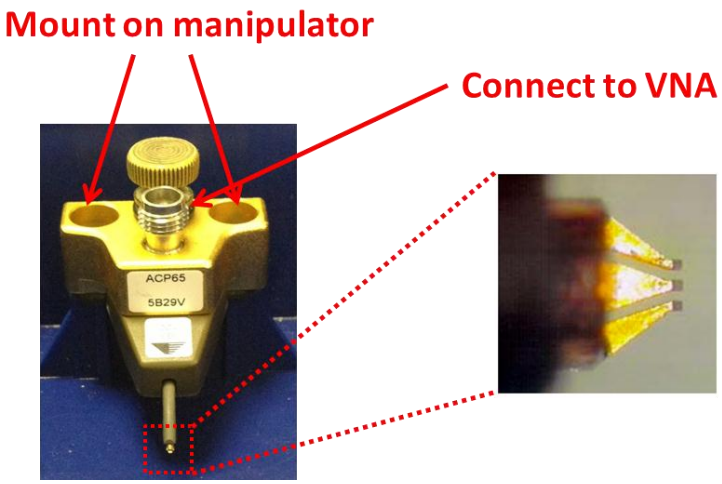

Figure 4.3.1 – Cascade ACP65 probe

The probes are mounted on precision manipulator arms, which allows their movement in three-dimensions and hence to be placed in the desired positions on the wafer during the measurement. The manipulators are mounted on a Cascade Microtech Summit 12000 semi-automatic probe station, which is controlled by Cascade Microtech Nucleus software. The SPA an Agilent B1500 is required to provide DC bias in RF measurements and the specified voltage conditions in DC measurements. This is controlled by Agilent EasyExpert software to set up appropriate DC bias conditions. The VNA an Agilent E8361A is required to measure frequency dependent S-parameters of the HEMTs. This is controlled by Cascade Microtech WinCal software. The complete measurement system set up is presented in **Figure 4.3.2**.

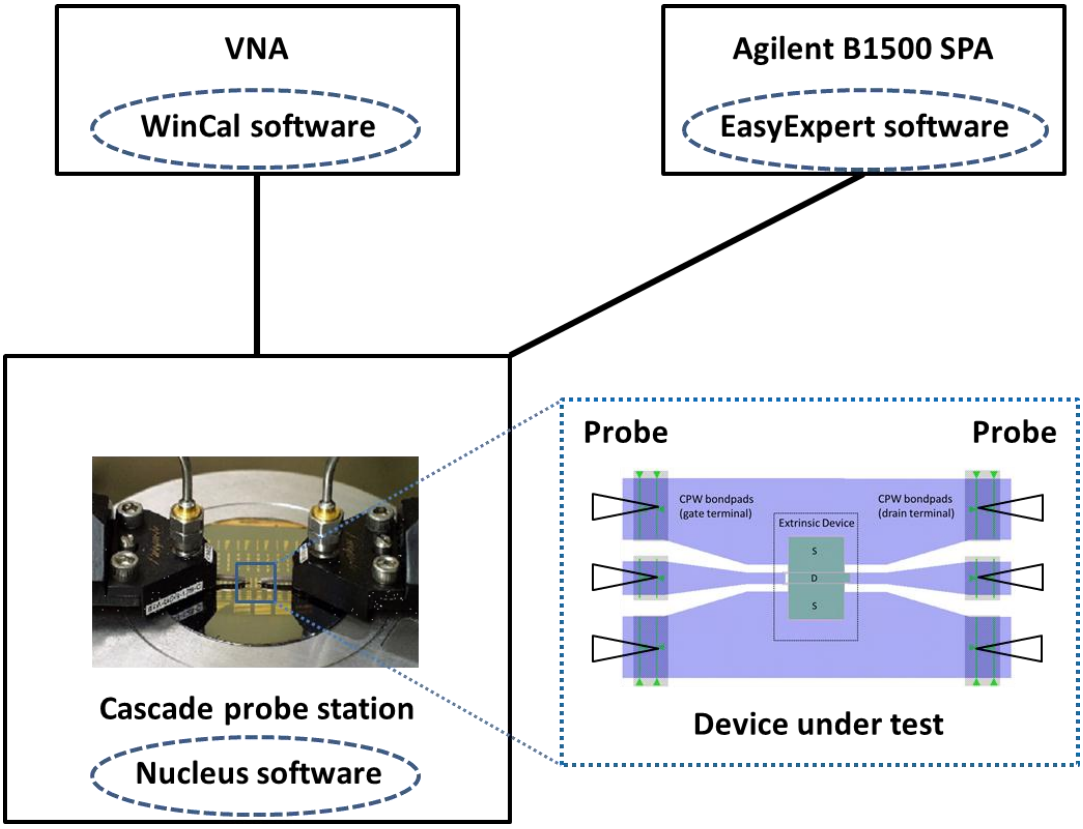

Figure 4.3.2 – DC and RF measurement set up

4.3.1 DC measurements

The DC characterisation of a HEMT is determined by the application of a range of variable biases to the drain and gate terminals of the device, with the source contact grounded.

The SPA provides a method of characterising the current under the condition of sweeping voltage applied on one terminal of the device whilst the bias of another terminal varies step by step. By utilising this method, the drain source current flowing through the channel and the gate current in the Schottky contact between gate and the barrier layer can be measured. The transconductance of the device can be extracted by calculating the derivative of the drain current with respect to the gate voltage.

Figure 4.3.3 shows typical characteristics plots of the drain current of a HEMT with the gate voltage varied from -1.7V to 0.1 V, and the transconductance of a HEMT with the drain voltage varied from 0 V to 1.0 V.

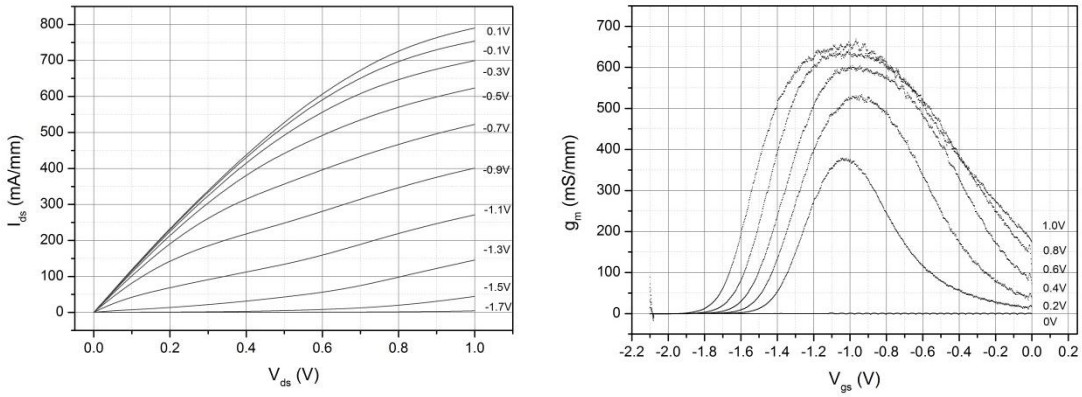

Figure 4.3.3 – Typical characterisation of a HEMT: I_{ds}-V_{ds} & g_m-V_{gs}

4.3.2 RF measurements

In RF measurements, the HEMT can be regarded as a two-port network, with the drain and gate of the device as output and input ports respectively, and the source of the device as ground, as illustrated in **Figure 4.3.4**.

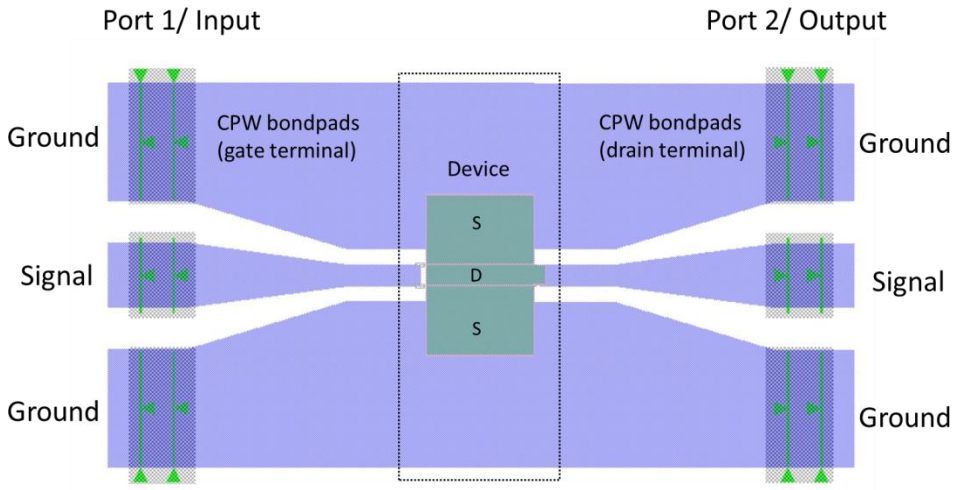

Figure 4.3.4 – A layout of HEMT with coplanar waveguide (CPW) (two-port network)

The measurements are performed in a range of specified frequencies and under various bias conditions applied to the terminals of the device. The small signal behaviour of the device is

usually characterised by Scattering parameters (S-parameters), which can also be transformed to other parameters (Z-, Y-, H-parameters) for particular figures of merit extraction.

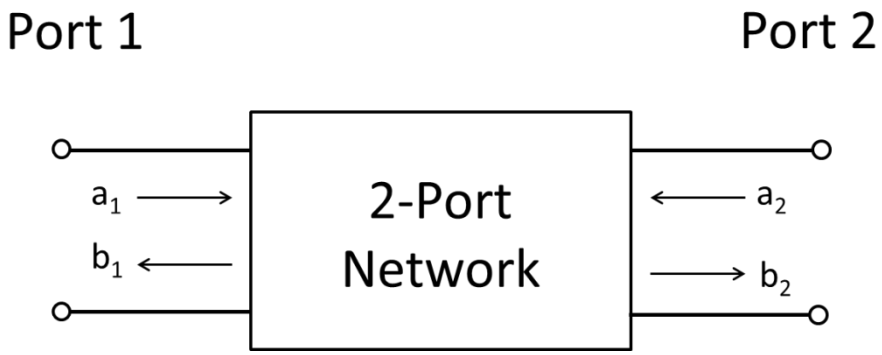

Figure 4.3.5 – A schematic of a two-port network with four transmission/ reflection signals

As shown in **Figure 4.3.5**, the four signals at the two ports of the network are related to the corresponding S-parameters, which can be expressed as following [4.3]:

$$b_1 = S_{11}a_1 + S_{12}a_2 \qquad \textbf{Eqn 4.3.1}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \qquad \textbf{Eqn 4.3.2}$$

Four S-parameters can be extracted by applying a matched load of 50 Ω at each port of the network to eliminate reflection signal in a particular direction, which means a_1 is zero when 50 Ω load is applied at port 2 and a_2 is zero when 50 Ω load is applied at port 1. Hence,

$$S_{11} = \frac{b_1}{a_1} \qquad (a_2 = 0) \qquad \textbf{Eqn 4.3.3}$$

$$S_{21} = \frac{b_2}{a_1} \qquad (a_2 = 0) \qquad \textbf{Eqn 4.3.4}$$

$$S_{12} = \frac{b_1}{a_2} \qquad (a_1 = 0) \qquad \textbf{Eqn 4.3.5}$$

$$S_{22} = \frac{b_2}{a_2} \qquad (a_1 = 0) \qquad \textbf{Eqn 4.3.6}$$

The RF performance of the device across a range of frequencies at a given bias condition can then be characterised by measuring both the magnitude and phase of each of these four S-parameters.

In order to achieve accurate device S-parameters, it is required to conduct a calibration of the measurement system before its use. The "Impedance Standard Substrate" (ISS) is used in the calibration to determine the influence of the measurement system by characterising structures of known S-parameters.

Several methods can be used for calibration, including SOLT (Short, Open, Load, Thru), LRM (Line, Reflect, Match), LRRM (Line, Reflect, Reflect, Match) [4.4-4.5]. In SOLT method, which is used in this work, four structures short, open, load, thru are used, as shown in **Figure 4.3.6**.

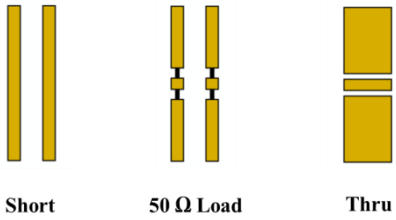

Figure 4.3.6 – Standard structures in SOLT calibration method include Short, Load, Thru

The "short" structure is a metal line to short the three tips (ground-signal-ground) of each probe. The "open" circuit is provided simply by lifting the probe in the air above the substrate. There is a 50 Ω matched load at each port in the "load" structure. In "thru" structure, the three tips of one probe are connected to those of another probe by three metal lines of a known length. The device can then be measured at RF frequencies after the successful calibration on ISS.

The measured S-parameters of a HEMT contain not only the response of the extrinsic device including gate and source/ drain ohmic contacts, but also the unwanted contribution of the coplanar waveguide bondpads for probing in measurements, as shown in **Figure 4.3.4**.

The de-embedding process is used to remove the contribution of bondpads in the characterisation of S-parameters. The basic idea of de-embedding is to evaluate the performance of bondpads by either direct measurement or modelling in software, and then the bondpads performance can be subtracted from the total measured S-parameters.

There is an issue in direct measurement of bondpads S-parameters, which is that it is difficult to control the precise location when placing the probe on the bondpads of each device with good contact for measurements, although alignment markers can be added onto the bondpads in fabrication.

A more useful method is to simulate the S-parameters of the coplanar waveguide bondpads in software, the Agilent Advanced Design System (ADS) was used in this work. A model of the extrinsic device together with the bondpads can be built in the software by constructing an equivalent circuit of the extrinsic device and placing two transmission line (coplanar waveguide) modules at the input and output ports to simulate the real measurement situation. In the transmission line module, various parameters can be set up such as the width, gap, length of the coplanar waveguide, and the physical properties of the substrate. The real performance of the device can then be extracted by removing two waveguide modules and the parasitic elements caused from bondpads, but keeping all parasitic elements caused from the device itself.

The figures of merit of the device can be extracted after the de-embedded S-parameters are obtained. As shown previously in **Section 2.5**, the cutoff frequency f_T, a significant figure of merit of device RF performance, is defined as the frequency when the short circuit current

gain falls to unity. The short circuit current gain H_{21} can be determined by converting the de-embedded S-parameters to H-parameters [4.3]:

$$H_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \qquad \textbf{Eqn 4.3.7}$$

As a consequence, the cutoff frequency of the device can be extracted by extrapolating the H_{21} plot, which decays at a rate of 20 dB/decade of frequency, to its intercept with the frequency axis.

The maximum frequency of oscillation f_{max}, is defined as the frequency when the Maximum Available Gain (MAG) falls to unity, which can be expressed as [4.6]:

$$MAG = \frac{S_{21}}{S_{12}}\left(K + \sqrt{K^2 - 1}\right) \qquad \textbf{Eqn 4.3.8}$$

where K is the stability factor and defined as [4.7]:

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}S_{12}|} \qquad \textbf{Eqn 4.3.9}$$

When K<1, the device is conditionally stable and could potentially oscillate when certain load impedances applied. Then the Maximum Stable Gain (MSG) is defined as:

$$MSG = \frac{|S_{21}|}{|S_{12}|} \qquad \textbf{Eqn 4.3.10}$$

When K>1, the device is unconditionally stable. Therefore, the MSG/MAG-frequency response can be divided into two parts of conditionally stable (MSG) and unconditionally stable (MAG).

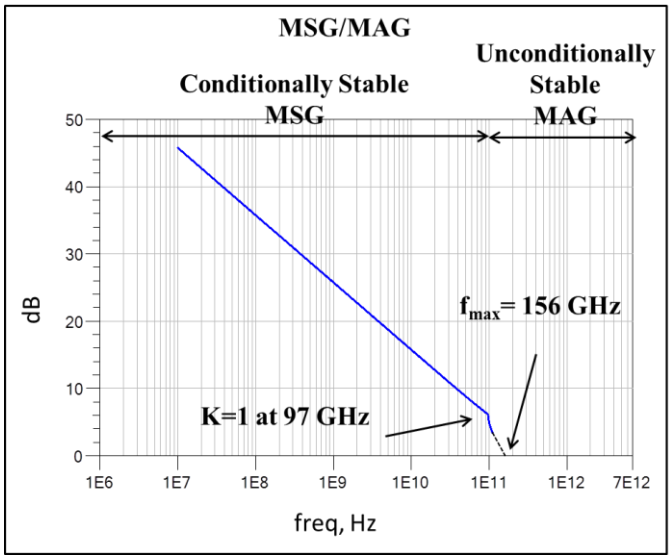

Figure 4.3.7 – An example of f_{max} extraction. The device is conditionally stable when working at frequency less than 97 GHz and unconditionally stable when the frequency larger than 97 GHz

The maximum frequency of oscillation can be extracted in a similar way by extrapolating the MAG plot, which also decays at a rate of 20 dB/decade of frequency, to its intercept with frequency axis. An example is given in **Figure 4.3.7** to show the extraction of f_{max} of a HEMT. **Figure 4.3.8** shows the plot of the stability factor K as a function of frequency. K=1 at 97 GHz.

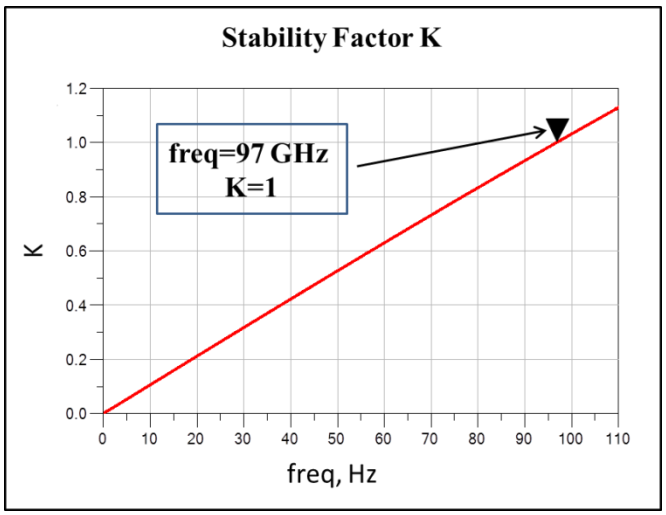

Figure 4.3.8 – Stability factor K=1 at 97 GHz

4.4 Summary

This chapter outlines several characterisation techniques, which can be used for measuring both the epitaxial material structure and evaluating both key elements of the HEMT and the overall device performance, at DC and RF frequencies.

- The Van der Pauw method, which is based on the Hall Effect, can be utilised to characterise carrier mobility, carrier concentration, and sheet resistance of the material.
- The Transmission Line Method can be used to measure the contact resistance of source/drain ohmic contacts.
- The measurement system set up and methods of measurements for device characterisation are described. In particular, calibration and de-embedding process for more accurate RF measurements of the device are introduced. The methods of extracting figures of merit of the device in DC and RF measurements are also presented, including drain current, gate leakage current, transconductance, cutoff frequency and the maximum frequency of oscillation.

Reference

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Chapter 5

Current technology review

In this chapter, a brief overview of HEMT technology development is described, including device performance improvement over the years along with the current state of the art. As the crucial part in the HEMT device, T-gate fabrication process technologies are also reviewed in this chapter.

The High Electron Mobility Transistor (HEMT), an important device for high frequency circuit applications, was first demonstrated by Mimura *et al.* at Fujitsu Labs in 1980 [5.1]. The HEMT device structure is based on the concept of modulation doping, which was first demonstrated by Dingle *et al.* at Bell Labs in 1978 [5.2]. The modulation doped structure in the HEMT device was first demonstrated in the AlGaAs/GaAs material system, which creates a two dimensional electron gas (2DEG) in an undoped GaAs layer at the interface between this layer and a doped AlGaAs layer [5.1].

After the first successful demonstration of the HEMT, the material system has evolved to an InAlAs/InGaAs platform. Higher indium concentration materials are preferred due to their lower effective mass as well as the increased Γ and L valley energy separation which enhances the opportunity for exploiting velocity overshoot effects [5.3].

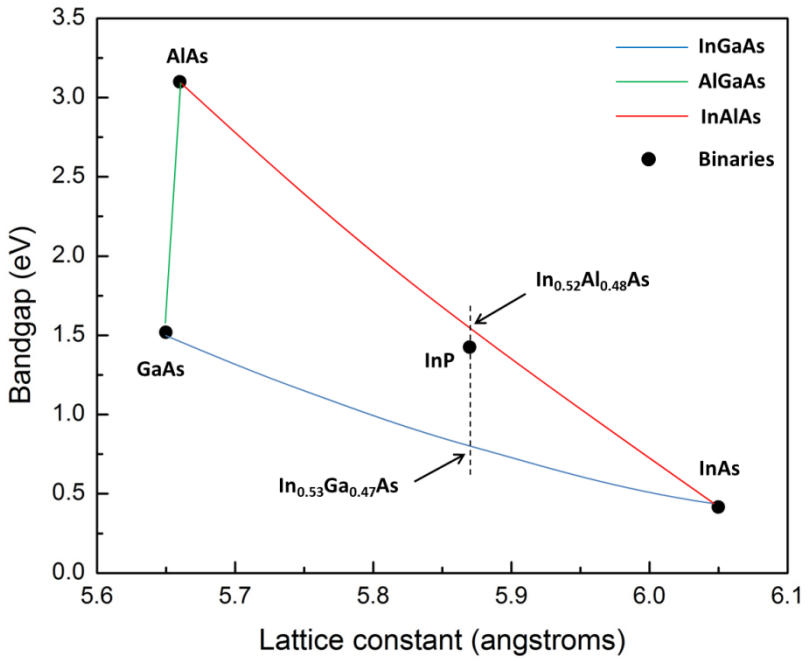

Figure 5.1 – Bandgap and lattice constant for III-V materials

GaAs was the first to be used as the substrate in the development of HEMT. However, as the indium content increases in the channel of the InAlAs/InGaAs material system, the bandgap decreases whilst lattice constant increases, as shown in **Figure 5.1**, leading to a large lattice mismatch between the channel material and the GaAs substrate.

To overcome the lattice mismatch between the high indium channel and underlying layers, InP was then included into the substrate material of HEMT, due to its larger lattice constant. Three solutions have been developed: lattice matched HEMT [5.4], pseudomorphic HEMT (pHEMT) [5.5], and metamorphic HEMT (mHEMT) [5.6].

As presented in **Figure 5.1**, InP substrate has a larger lattice constant than that of GaAs and hence has been utilised in high indium channel HEMT realisation to reduce the lattice mismatch between the channel and the substrate. $In_{0.53}Ga_{0.47}As$, $In_{0.52}Al_{0.48}As$, and InP have the same lattice constant, though with different bandgaps, and therefore can be used in the material system for lattice matched HEMT realisation. The pHEMT utilises a strained channel slightly lattice-mismatched to the underlying buffer layer and InP substrate. InGaAs material with indium concentration higher than 53% is usually used in the channel. The mHEMT utilises a graded buffer which gradually varies in lattice constant to accommodate the strain induced by growing a channel layer with larger lattice constant (such as high indium concentration InGaAs) on a substrate with smaller lattice constant (such as GaAs). Although InP has a closer lattice constant to the InGaAs, it is more expensive and brittle compared to GaAs, resulting in a reduced yield. In addition, GaAs material growth and processing technology is more mature. Both of which make GaAs still preferred to be as the substrate material for HEMT realisation [5.7].

The material evolution in the HEMT fabrication technologies is illustrated in **Figure 5.2**. $In_{0.7}Ga_{0.3}As$ and $In_{0.75}Ga_{0.25}As$ are taken as examples for channel material in pHEMT and mHEMT respectively.

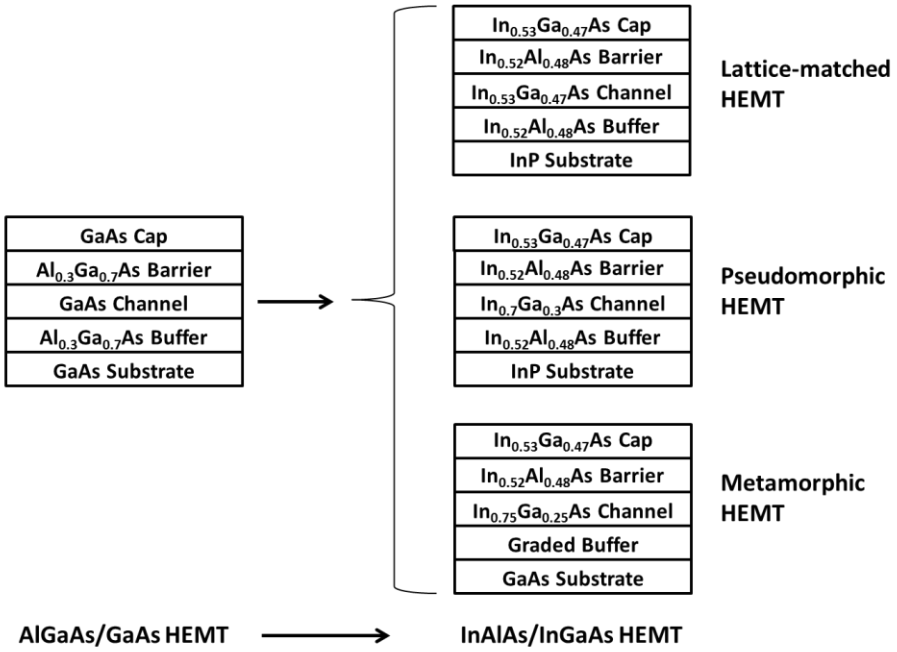

Figure 5.2 – The evolution of HEMT material system from AlGaAs/GaAs to InAlAs/InGaAs

The InAlAs/ InGaAs HEMT has presented record device performance both on GaAs and InP substrates. The current record cutoff frequency f_T is 644 GHz and 688 GHz respectively for InAlAs/ InGaAs PHEMT on InP and InAlAs/ InGaAs Metamorphic HEMT (MHEMT) on GaAs [5.8-5.9]. The record maximum frequency of oscillation f_{max} of an InAlAs/ InGaAs HEMT is above 1 THz both on GaAs [5.10] and InP substrates [5.11], which led to the first demonstration of amplification in a transistor based circuit at 1 THz [5.12]

As well as the progress made in AlGaAs/GaAs and InAlAs/InGaAs HEMT technology development, HEMTs and modulation doping were also demonstrated in the AlGaN/GaN material system. Modulation doping in the AlGaN/GaN material system was first demonstrated in 1992 [5.13] and the first AlGaN/GaN HEMT was then presented in 1993 [5.14]. There has been increasing research interest in AlGaN/GaN HEMTs in particular for power amplification at millimetre-wave frequencies [5.15-5.16], due to the high voltage operation of the device resulting from the wide bandgap of GaN.

To simultaneously satisfy the requirements of short gate length and reduced gate resistance of a HEMT, the T-gate was introduced in the 1980s. T-gates were initially fabricated by various approaches, including angled evaporation [5.17], X-ray lithography [5.18], optical lithography [5.19], and electron beam lithography [5.20]. T-gates fabricated by hybrid processes combining photolithography for head exposure and electron beam lithography for foot formation were also reported [5.21-5.23].

To decrease the complexity of the fabrication process, approaches to realising T-gates using a one-step electron beam lithography utilising multilayer resists with different sensitivities were developed. A tri-layer resist system of a copolymer (PMMA–MAA) layer between bilayers of polymethylmethacrylate (PMMA) had been commonly utilised in one-step electron beam lithography T-gate fabrication due to the simple and reproducible process, since there was no mixing of resist layers during preparation and hence no barrier layer was needed between resist layers [5.24].

To improve the sensitivity contrast between PMMA and PMMA-MAA resist layers, higher sensitivity chemically-amplified resists such as UVIII were then applied to T-gate fabrication for the head formation to replace the copolymer resist [5.25-5.26]. To further reduce the gate length, two-step lithography approaches were developed to decouple the writing of the gate foot and the head. Record device performance demonstrated at the time was the result of these approaches [5.27-5.29]. The smallest footprint T-gate with a gate length of 10 nm, was produced by S. Bentley *et al*. at University of Glasgow in 2009 [5.30].

Copper has been considered as a gate metal of choice in III-V compound semiconductor devices particularly GaN HEMT [5.31-5.33], because of its advantages in low gate leakage current, thermal stability, low resistivity and low cost. A copper T-gate fabricated by electroplating process, compatible with silicon based manufacturing was reported by R. Oxland *et al* [5.34]. Based on this work, a novel fabrication process has been developed for

copper T-gate formation, which is silicon compatible and can be integrated into a full HEMT realisation process flow. This work will be described in detail in **Chapter 6**.

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Chapter 6

Development of silicon compatible HEMT process flow

6.1 Introduction

This chapter reports the main work of this project, the development of a silicon compatible process flow for HEMT fabrication.

The details including nanoscale copper electroplating and low damage inductively coupled plasma etching of nanoscale molybdenum gate lines are described. A viable route to integrating these two technologies into the final copper-based T-gate fabrication process flow is demonstrated. Additionally, a gate-first HEMT process flow which can incorporate the copper-based T-gate is introduced.

6.2 Silicon compatible Cu-based T-gates

Finding routes to the introduction of copper as part of the backend of line in Ultra Large Scale Integration (ULSI) interconnect applications, due to its reduced resistance and improved electromigration properties compared to aluminium [6.1], opened the way to considering copper as a gate metal choice in III-V compound semiconductor devices, because of the merits of low cost, thermal stability, low resistivity and low gate leakage current [6.2-6.5]. In addition, more effort has been invested in recent times on growing III-V compound semiconductors on silicon wafers to benefit from the technological advantages and cost reduction [6.6]. However, the conventional processes of III-V compound semiconductor device realisation are heavily dependent on gold based metallisation and lift off approaches which are not compatible with mass production in silicon fabs. Therefore, it is essential to develop silicon compatible processes to fully exploit III-V devices on a silicon platform for applications where III-V materials have considerable performance advantages over silicon.

In this section, a copper electroplating process for T-gate head formation and low damage inductively coupled plasma dry etching of nanoscale molybdenum for T-gate foot realisation are introduced.

6.2.1 Copper electroplating process

The copper electroplating process has been utilised in high volume manufacturing of interconnects in ULSI since the late 1990s, using the Damascene Process invented by IBM [6.1]. The advantages of electroplated deposition of copper over other approaches including Physical Vapour Deposition (PVD) and Chemical Vapour Deposition (CVD), are void-free and seamless filling of trenches and in particular vias of high aspect ratio [6.1].

In this section, the influence of additives in the electrolyte to electroplated copper morphology both on planar samples and in nanoscale features has been investigated.

6.2.1.1 Copper electroplating on planar samples

An electroplating cell consists of a cathode (working electrode), an anode (counter electrode), and usually a reference electrode, which has a stable and standard potential against which the potential of the working electrode is determined. The basic set up of the electroplating cell used in this work is shown in **Figure 6.2.1**. The working electrode is the sample to be electroplated, and the counter electrode is a copper plate. The reference electrode is a silver/silver chloride (Ag/AgCl) reference electrode manufactured by Koslow scientific testing instruments. It consists of an Ag metal wire coated with AgCl immersed in a saturated chloride ion solution such as potassium chloride (KCl), all of which is enclosed in a glass tube.

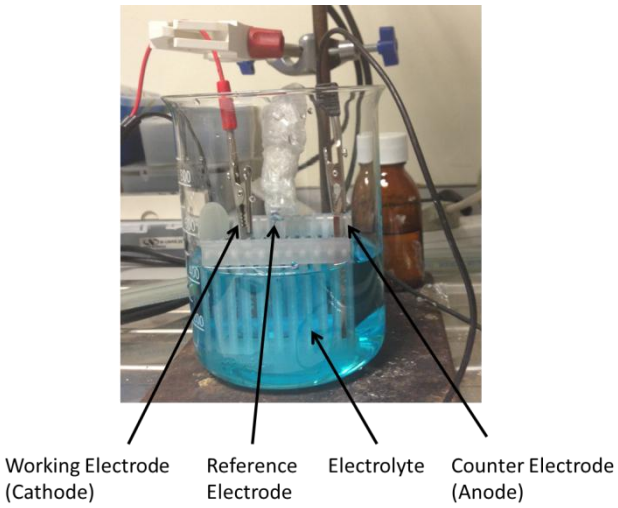


Figure 6.2.1 – Electroplating cell used in this work

The power supply to drive the electroplating process is a Princeton Applied Research Potentiostat/Galvanostat Model 273A. The reference electrode is used as a fixed reference for the potentiostat. When the potential of the working electrode is higher than the reduction potential of the metal ions (Cu^{2+}) in the copper sulphate based electrolyte, the following reactions occur at the cathode and anode respectively:

Reaction occurring at the cathode (sample to be electroplated):

Reduction: $Cu^{2+} + 2e^{-} \rightarrow Cu$

Reaction occurring at the anode (copper plate):

Oxidation: $Cu - 2e^- \rightarrow Cu^{2+}$

To establish baseline copper electroplating conditions, a planar glass substrate was first coated with 15nm Ti/15nm Pt by electron beam evaporation, which acts as a seed layer during the electroplating process. The sample was then patterned by photo-lithography to expose a 1 cm^2 (1 cm×1 cm) electroplating area. During the electroplating procedure, an external constant potential of +0.25V was applied to the working electrode with respect to the reference electrode as illustrated in **Figure 6.2.2**, and the electrolyte was stirred at 100 rpm. The reduction potential of copper ions (Cu^{2+}) is +0.34V with respect to the standard hydrogen electrode (electrode potential is zero), and is +0.143V with respect to the Ag/AgCl reference electrode (electrode potential is +0.197V). Therefore, the applied potential of +0.25V on the working electrode is higher than the reduction potential of copper ions (+0.143V), both with respect to the Ag/AgCl reference electrode, which makes the reduction reaction occur at the cathode and hence copper deposition on the sample.

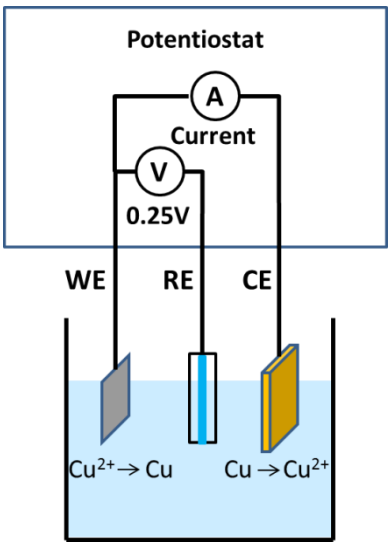


Figure 6.2.2 – Illustration of electroplating potential conditions. WE stands for working electrode; RE stands for reference electrode; CE stands for counter electrode. Copper reduction occurs at working electrode, when 0.25V is applied to working electrode with respect to the reference electrode

Initially, copper sulphate, sulphuric acid and sodium chloride were included in the electrolyte, with relative concentrations shown in **Table 6.2.1**. For an electroplating time of 120 seconds, the root mean square (rms) roughness of the copper surface electroplated in this electrolyte was 24.5nm as shown in **Figure 6.2.3**.

Solute	Conc. (g/l)
Sulphuric Acid	150
Copper Sulphate	30
Sodium Chloride	0.1

Table 6.2.1 – Composition of the initial electrolyte

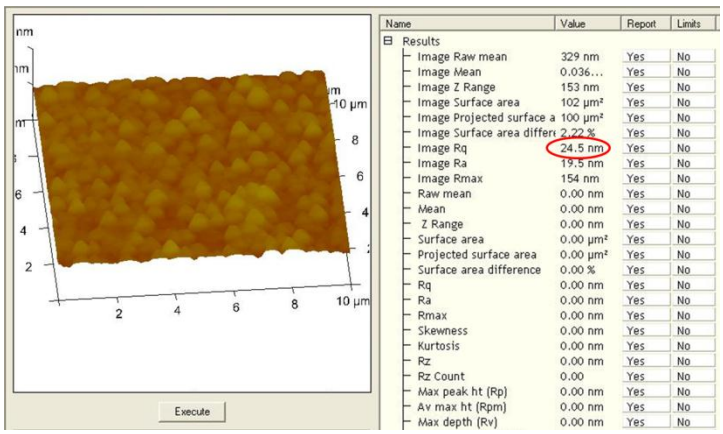


Figure 6.2.3 – The rms roughness of copper film electroplated in the electrolyte shown in **Table 6.2.1** is 24.5nm as determined by a Vecco DI 3600 atomic force microscope (AFM). Scan area is 10 µm×10 µm

To reduce the surface roughness of the electrodeposited copper film, Thiourea was added to the electrolyte, which acts as a brightener to reduce the metal grain size and therefore surface roughness [6.7]. Polyethylene glycol (PEG) was also added, which acts as a suppressor, which, as will be shown shortly, is the key element to electroplating copper into nanoscale features [6.8]. Finally, 3-mercapto-1-propanesulphoic acid (MPS) was included as it is an accelerator and catalyst [6.9]. It adheres to copper surfaces and can locally accelerate current flow during electroplating. These additives were included in the relative concentrations shown in **Table 6.2.2** [6.10].

Solute	Conc. (g/l)
Sulphuric Acid	150
Copper Sulphate	30
Polyethylene Glycol (PEG)	0.5
Sodium Chloride	0.1
Thiourea	0.01
3-mercapto-1-propanesulphoic acid (MPS)	0.01

Table 6.2.2 – Composition of the electrolyte with additives

With the sample electroplating conditions as above, the root mean square (rms) roughness of the copper surface electroplated in the electrolyte with additives was reduced to 15.3 nm as shown in **Figure 6.2.4**.

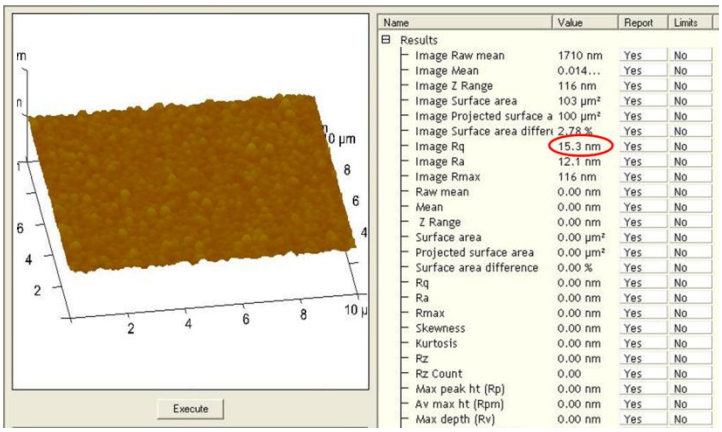
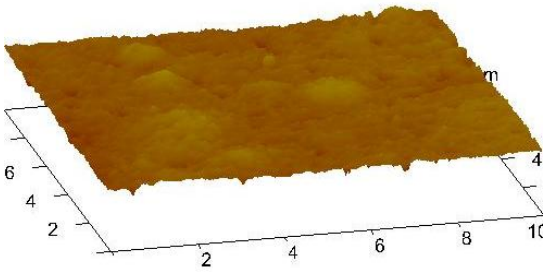
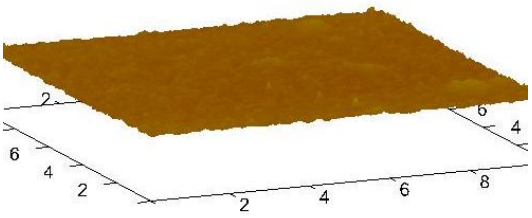
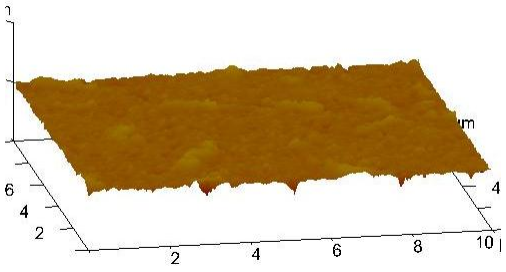
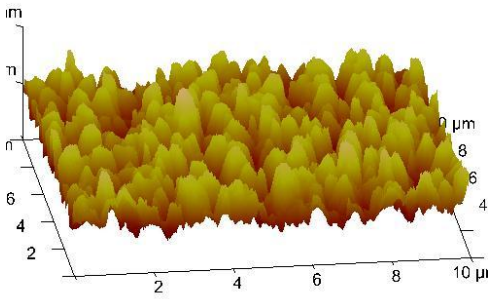
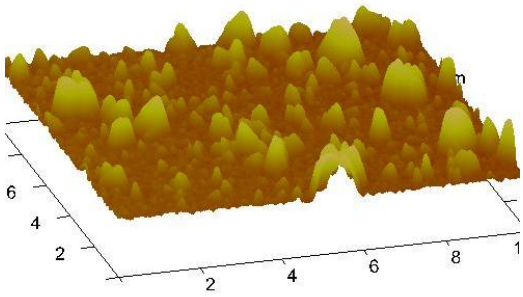
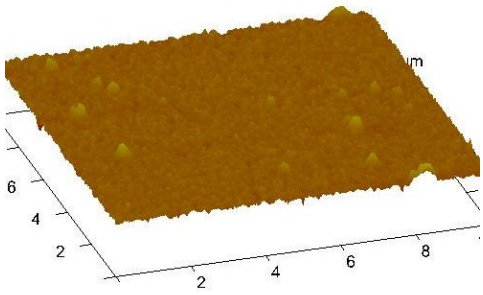


Figure 6.2.4 – The rms roughness of copper film electroplated in the electrolyte with additives is 15.3nm as determined by a Vecco DI 3600 atomic force microscope (AFM). Scan area is 10 µm ×10 µm

The influence of the concentration of copper sulphate ($CuSO_4$) and sulphuric acid (H_2SO_4), two of the fundamental chemicals in the electrolyte, on the roughness and sheet resistance of the electroplated copper film, which were characterised by AFM and Van der Pauw method respectively, were also investigated, as presented in **Table 6.2.3**. The concentrations of other chemicals in the electrolyte were identical to those shown in **Table 6.2.2**. The potential applied on the working electrode was constant at +0.25V.

H_2SO_4 Conc.(g/l)	$CuSO_4$ Conc.(g/l)	3D image of copper film	Sheet resistance of copper film (Ω/□)
150	30	 The rms roughness is 22.1nm.	0.397
250	30	 The rms roughness is 10.7nm.	0.37
200	38.66	 The rms roughness is 16.5nm.	0.266

50	30	 The rms roughness is 111nm.	0.584
100	21.34	 The rms roughness is 96.7nm.	0.452
200	21.34	 The rms roughness is 7.41nm.	0.574

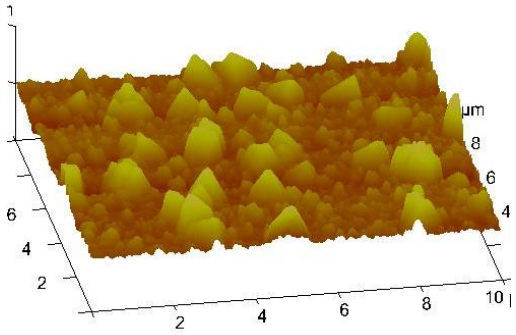
100	38.66	 The rms roughness is 99.4nm.	0.282

Table 6.2.3 – The rms roughness and sheet resistance of copper film electroplated in the electrolyte with different concentrations of $CuSO_4$ and H_2SO_4. The rms roughness was determined by a Vecco DI 3600 atomic force microscope (AFM). Scan area is 10 µm×10 µm. The sheet resistance was measured by Van der Pauw technique

As shown in **Table 6.2.3**, the higher concentration of sulphuric acid contributes to the smaller rms roughness of copper film, and the lower sheet resistance of copper film is mainly resulting from the higher concentration of copper sulphate, therefore there is a trade-off in terms of surface roughness and sheet resistance of the electroplated films.

6.2.1.2 Copper electroplating in nanoscale features

The copper electroplating techniques described above were applied to a sample with patterned nanoscale features, using electrolytes without and with additives in the same concentrations as those shown in **Tables 6.2.1** and **6.2.2** respectively.

15nm Ti/15nm Pt was first evaporated on a GaAs substrate to act as the seed layer of electroplating process. The sample was then coated in 300 nm thick PMMA and patterned by electron beam lithography to form features of 150nm, 250nm and 350nm. **Figure 6.2.5** shows the PMMA resist profile with the feature size of 150nm.

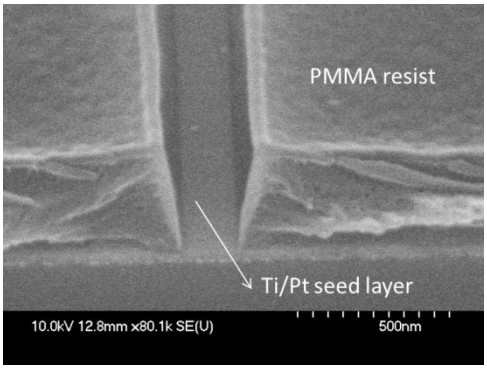


Figure 6.2.5 – PMMA resist profile with the feature size of 150nm ready for copper electroplating

Copper cannot be electroplated into the nanoscale features unless Polyethylene glycol (PEG), Thiourea, and 3-mercapto-1-propanesulphonic acid (MPS) were added into the electrolyte, as shown in **Figure 6.2.6a** and **Figure 6.2.6b**.

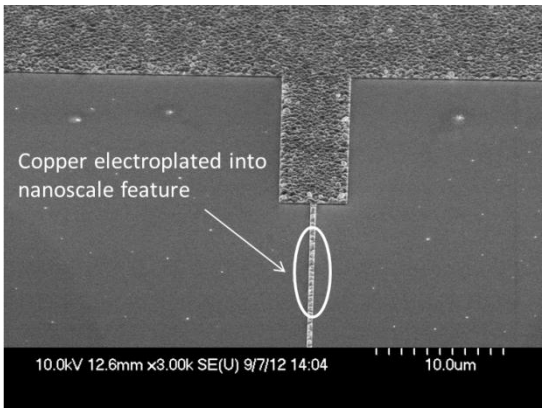


Figure 6.2.6a – Cu electroplating using the electrolyte with the additives (PEG, Thiourea, MPS) as shown in **Table 6.2.2**

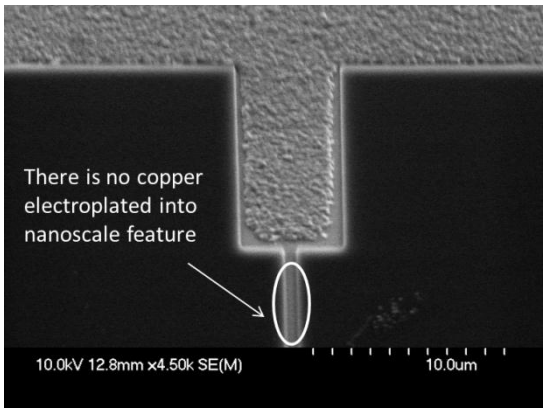


Figure 6.2.6b – Cu electroplating using the electrolyte with no additives as shown in **Table 6.2.1**

Figure 6.2.7a and **Figure 6.2.7b** present 150nm and 500nm copper lines respectively, which were formed by removing the PMMA resist after electroplating copper into 150nm and 500nm resist patterns using the electrolyte shown in **Table 6.2.2** and with a working electrode potential of +0.25V.

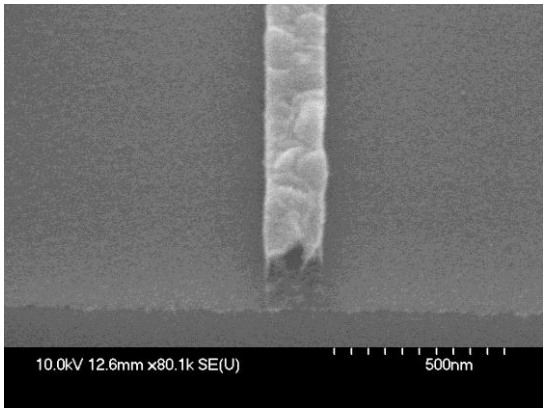


Figure 6.2.7a – 150nm copper line after the removal of PMMA resist

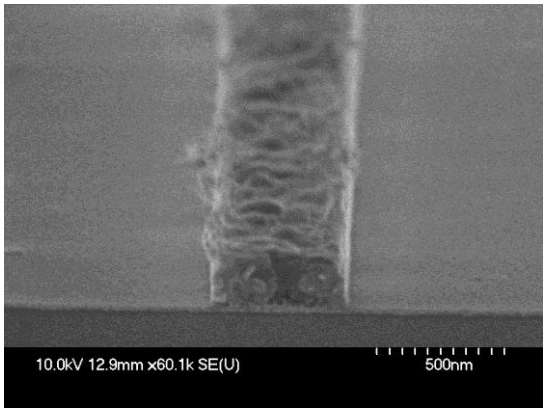


Figure 6.2.7b – 500nm copper line after the removal of PMMA resist

These experiments show that the additives in the electrolyte play a very important role in reducing the roughness of copper film and enabling copper to be electroplated into nanoscale features.

6.2.1.3 Discussion

There are some detailed issues in the experiments and electroplating process worthy of discussion:

Some improvements resulted in the copper electroplating process being more stable and repeatable.

- The electrolyte was used repeatedly in the copper electroplating experiments initially, which led, on certain occasions, to no metal film being electrodeposited. This is because the pH value of the electrolyte increases after several runs since the hydrogen ions are reduced to hydrogen during the copper electroplating procedure. If the electrolyte is not acidic, it prevents dissolution of surface oxides on the seed layer, which further prevents copper electroplating on the sample. Using fresh electrolyte in every copper electroplating run mitigated this effect.

- The Ag/AgCl reference electrode was a handmade one initially, which was coarse and not stored correctly in a saturated potassium chloride solution. The inner filling solution of the Ag/AgCl reference electrode diffused outside the electrode into the copper electroplating electrolyte, resulting in the potential of the reference electrode not being fixed. As a consequence, the potential of the working electrode was not well controlled, which caused unrepeatable results and large grains at the copper surface. The original handmade reference electrode was replaced by a commercial Ag/AgCl reference electrode manufactured by Koslow scientific testing instruments. In addition, the decision was made to stop stirring the electrolyte solution during the electroplating procedure to decrease the reaction rate and reduce the grain size of the copper film. **Figure 6.2.8a** and **Figure 6.2.8b** clearly show that the roughness of the electroplated copper film improved significantly after the changes of process details described above were implemented.

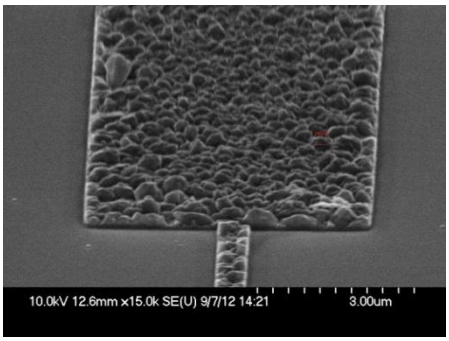


Figure 6.2.8a – Before changes of process details described above were implemented: The diameter of an individual grain is up to 245nm

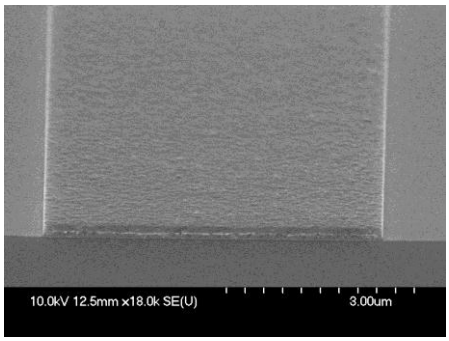


Figure 6.2.8b – After changes of process details described above were implemented: The rms roughness of the copper film is 4.47nm

6.2.2 Simple electroplated copper-based T-gate

The conventional gold-based T-gate fabrication process based on electron beam lithography of multiple resist layers followed by Ti/Pt/Au metallisation and lift off has been described in **Chapter 3**. To be silicon compatible, a significant modification to T-gate manufacture is

required. As copper can be electroplated into nanoscale features as shown in **Figure 6.2.7**, an experiment was performed to see if it is possible to fabricate a copper T-gate using a single-step copper electroplating process.

The process flow developed in this experiment is shown in **Figure 6.2.9**. First, a 15 nm Ti/15 nm Pt seed layer was uniformly deposited on a GaAs substrate by electron beam evaporation. The sample was then spin coated with an 80 nm PMMA bilayer (2.5% 2041/2.5% 2010). A range of feature sizes from 40 nm to 500 nm were then defined by electron beam lithography. Following development in 2:1 IPA: MIBK developer for 30 seconds at 23 ℃, the sample was electroplated in the electrolyte with additives described in **Section 6.2.1.1** and shown in **Table 6.2.2** for 10 minutes at a constant working electrode potential of +0.25V. Thereafter, the sample was placed in warm acetone (50 ℃) to remove unwanted resist.

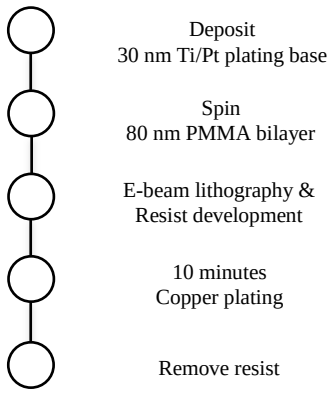


Figure 6.2.9 – Simple electroplated copper T-gate process flow

When the electrodeposition initially starts, the gap in the PMMA will be gradually filled with copper. After a sufficiently long electroplating time, the thickness of the copper will be greater than that of the resist. The copper then starts to grow in three dimensions and forms the T-gate head. As shown in **Figure 6.2.10a-c**, obtained from a single sample electroplated using the conditions described above, the specific T-gate "head" geometry depends on the starting gate foot as for a given electroplating time, a constant volume of copper will be electrodeposited.

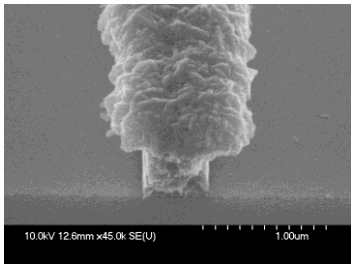


Figure 6.2.10a – 500nm foot copper T-gate on Ti/Pt seed layer

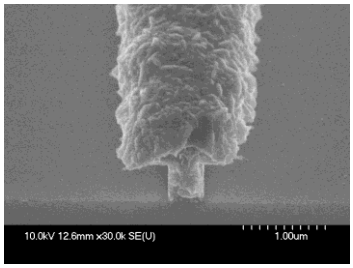


Figure 6.2.10b – 400nm foot copper T-gate on Ti/Pt seed layer

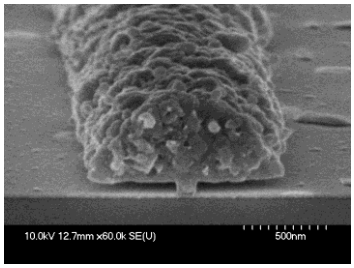


Figure 6.2.10c – 100nm foot copper T-gate on Ti/Pt seed layer

As shown in the image of **Figure 6.2.11a** and **Figure 6.2.11b**, the smallest footprint copper T-gate structure fabricated using this simple and silicon compatible process is 40 nm.

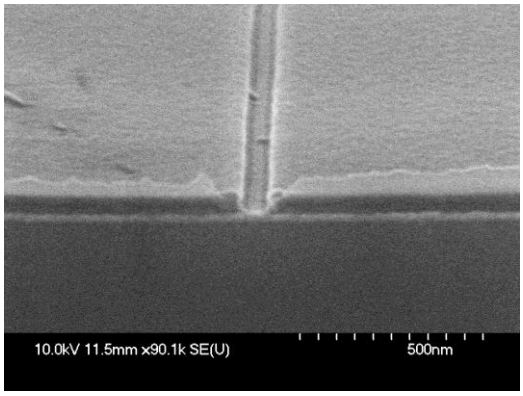


Figure 6.2.11a – 40nm resist profile

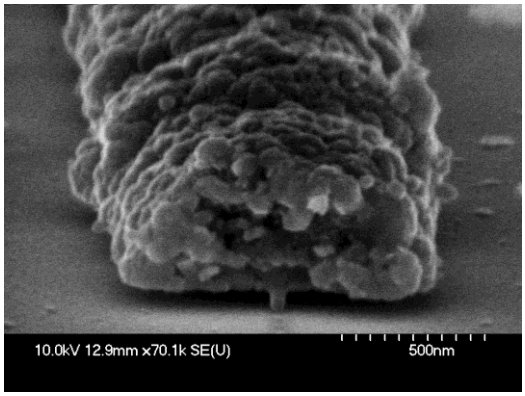


Figure 6.2.11b – 40nm foot copper T-gate

However, the challenge here is how to remove the unwanted seed layer of Ti/Pt underneath the copper T-gate head. A dry etch process is not an effective strategy since the copper T-gate head would be a mask to protect the unwanted seed layer underneath it. An isotropic wet etch process is also an impossible method, since Pt can only be dissolved in aqua regia. The very strong acid will remove all the metal including copper. Electrochemical dissolution of Pt was considered, but the experiment showed that Cu dissolved prior to Pt, when both Cu and Pt were on the anode of the electroplating cell. This is because of the relative reactivity of platinum and copper. As a consequence, the copper on the anode is oxidised and dissolved into the solution prior to the platinum oxidisation. **Figure 6.2.12** shows that the copper film had dissolved into the solution with little change to the platinum film, when the sample (with

both Cu film and Pt film on it) was used as the anode during the electrochemical dissolution procedure.

Therefore, it is essential to develop some other process techniques to make this simple electroplated copper T-gate integrable into a full HEMT process flow.

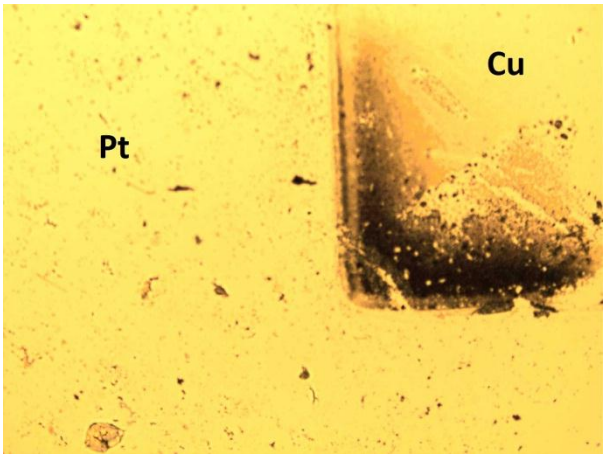


Figure 6.2.12 – Cu film dissolved a lot while Pt film unchanged

6.2.3 Low damage inductively coupled plasma etching molybdenum

To mitigate the issue of having a plating base seed layer below the T-gate head as described above, the use of a patterned seed layer for selectively copper electroplating has been explored.

To be silicon compatible, the seed layer should be blanket deposited on the whole sample, then patterned by dry etching. The nanoscale patterned seed layer would form the T-gate foot, which would also be suitable for selectively copper electroplating to form the T-gate head. Molybdenum (Mo) was selected as the seed layer metal of choice, due to its high thermal stability, good electrical conductivity, high work function and ease of dry etching. In addition, molybdenum is also a good metal of choice as a diffusion barrier between copper and semiconductors [6.11].

Molybdenum has been used as a gate metal of choice in planar and FinFET CMOS fabrication [6.12-6.13], and also in MEMS device realisation [6.14]. In these areas, numerous dry etch processes to pattern molybdenum based on a range of gas chemistries including NF_3 [6.15], Cl_2 [6.16], Cl_2/O_2 [6.13], $SF_6/BCl_3/Ar$ [6.14], and $O_2/Cl_2/Ar$ [6.17] have been described. In III-V MOSFETs, nanoscale gates have been defined by evaporation of molybdenum through a gap etched in a SiO_2 film [6.18]. To date however, there has been no report of dry etching molybdenum with low damage to directly form gates suitable for the realisation of III-V compound semiconductor transistors, where etch process induced damage can significantly compromise device performance [6.19-6.21] in particular in the access regions between the source/drain and gate of the device.

In this section, a low damage inductively coupled plasma dry etching process for nanoscale molybdenum gate lines is described, which is a crucial step in the establishment of a silicon compatible copper-based T-gate process.

To optimise the etching conditions, a 100 nm molybdenum film was deposited by electron beam evaporation on a GaAs substrate, which was then spin coated with 250 nm HSQ resist and subsequently baked for 2 minutes at 90℃ on a hotplate. The substrate was then exposed to define gate line patterns in the range 30 to 50 nm, written by 100 keV electron beam lithography. Following development and a further 90℃ hotplate bake for 2 minutes, HSQ features with critical dimensions to 30 nm as shown in **Figure 6.2.13**, suitable to act as a mask to the SF_6/C_4F_8 etch chemistry used in this study, were obtained. The optimisation of the SF_6/C_4F_8 ICP etch process was performed in a dual RF source etch system where the coil and platen powers can be independently controlled. The sample temperature was maintained at 20℃ by using helium backside cooling [6.22].

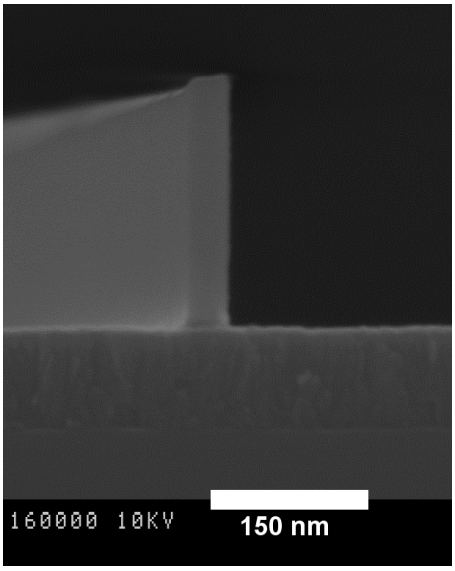


Figure 6.2.13 – HSQ feature with critical dimension of 30 nm and thickness of 250 nm

The parametric investigation consisted of studying the impact of gas ratio, etch chamber pressure, coil power and platen power on the etch rate and profile of molybdenum etched using the HSQ mask. The HSQ mask should be thick enough to protect the molybdenum underneath it, since HSQ is also etched in SF_6 chemistries. It is also very important to make sure that the HSQ mask will adhere to the molybdenum during the etch process. As will be shown below, the profile of the etched molybdenum lines is vital to ensuring that the HSQ mask adheres well. An interferometer was used for monitoring the end point of the molybdenum etch process. Based on the time taken to fully remove the molybdenum, a 20% over-etch time was included for each experiment.

A SF_6 and C_4F_8 gas mixture was utilised in the ICP etching system. Chemically active fluorine species mainly from SF_6 etches molybdenum by generating volatile molybdenum fluorides, whilst carbon species from C_4F_8 passivate the etched metal sidewalls to enable high resolution, anisotropic etching at low power and DC bias, which is important to minimise any process induced damage [6.23-6.24]. The optimisation procedure commenced with a study of the impact of gas ratio on both vertical etch rate and etched molybdenum profile.

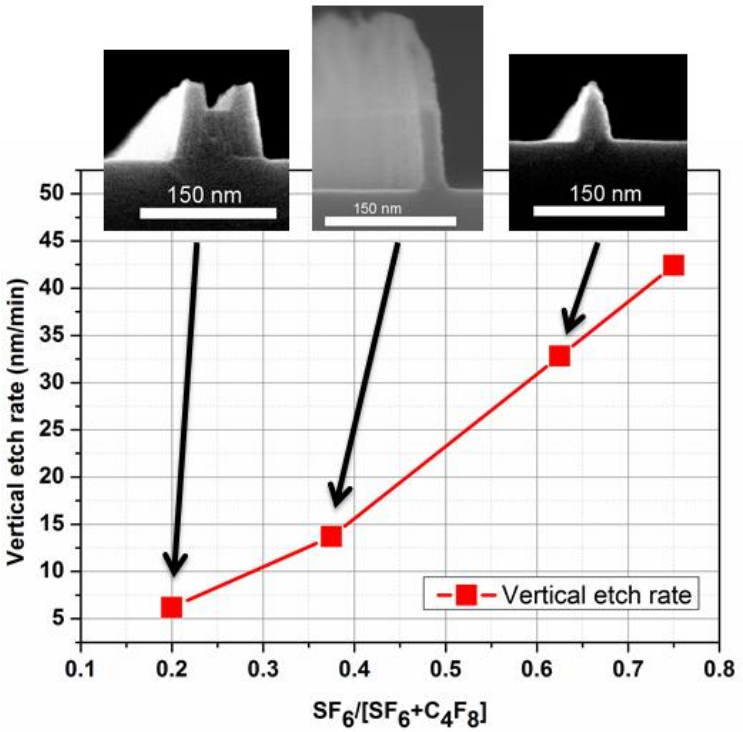


Figure 6.2.14 – Influence of gas ratio on vertical etching rate of molybdenum with chamber pressure 5 mTorr, platen power 2 W, coil power 200 W

As shown in **Figure 6.2.14**, increasing the concentration of SF_6 in the etch gas mixture results in an increase in etch rate. At low SF_6 concentrations, there is excessive polymer deposition on the etched molybdenum, as shown in the micrograph to the left side of **Figure 6.2.14** ($SF_6/[SF_6+C_4F_8]=0.2$). For high SF_6 concentrations, the micrograph to the right side of **Figure 6.2.14** ($SF_6/[SF_6+C_4F_8]=0.625$) shows that there is insufficient polymeric deposition to protect the etched molybdenum, resulting in a 73 ° etch profile. The remaining feature height of 68 nm shows that the HSQ mask has been dislodged prior to completion of the etch process as determined by end point detection. From the micrograph in the middle of **Figure 6.2.14**, a gas ratio of $SF_6/ [SF_6+ C_4F_8] =0.375$ produces a near vertical (85 °) molybdenum etch profile of 100 nm height and with 100 nm thick HSQ etch mask in place.

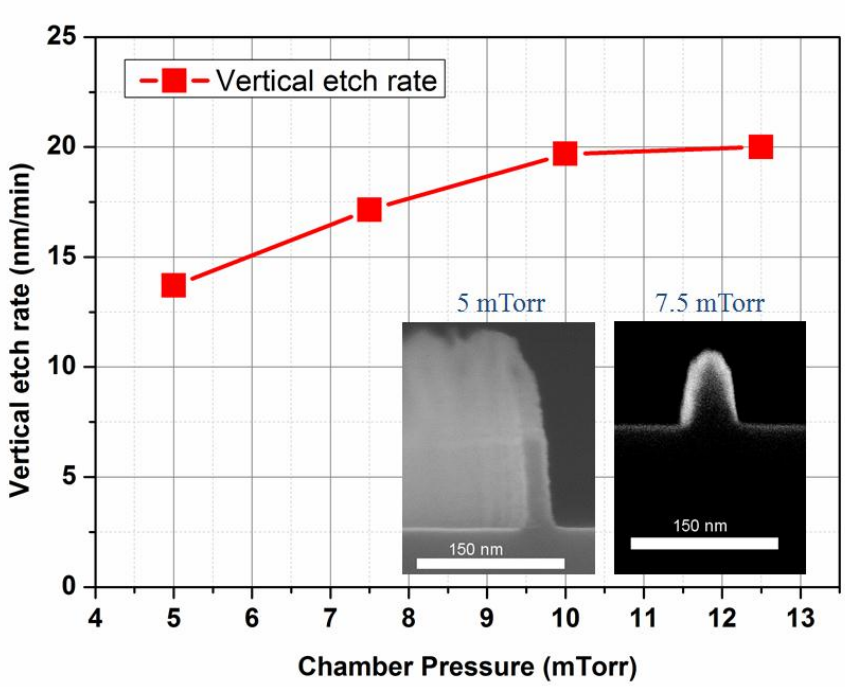


Figure 6.2.15 – Influence of chamber pressure on vertical etching rate of molybdenum with platen power 2 W, coil power 200 W, SF_6/C_4F_8= 15 sccm/25 sccm

Having established a suitable gas ratio, an investigation of the impact of chamber pressure on molybdenum etch rate was undertaken. As shown in **Figure 6.2.15**, increasing the chamber pressure for the fixed, and previously optimised gas ratio of SF_6/C_4F_8=15 sccm/25 sccm increases vertical etch rate for pressures to 10 mTorr, and saturates beyond. This suggests that up to 10 mTorr, increasing the chamber pressure results in a longer residence time for etching species, while for pressures greater than this, the etch products are not being removed quickly enough. Besides, increased pressure results in a reduction of mean free path of active species and higher probability of collision among ions in the plasma, which further leads to a lower probability of reaction between active fluorides and molybdenum. From the insets of **Figure 6.2.15**, for chamber pressures of 5 mTorr and 7.5 mTorr, it is clear that only at the lowest chamber pressure is the etch rate and resulting profile such that the HSQ etch mask adheres for the time required to fully remove the molybdenum. For 7.5 mTorr chamber pressure, the remaining feature with non- vertical profile is 73 nm tall. For 10 mTorr chamber pressure, only 48 nm of the originally masked molybdenum film remained.

The influence of coil power on vertical etch rate and DC bias in the etch chamber is shown in **Figure 6.2.16**. Higher coil power dissociates more of the etch gases and therefore increases the density of etching species while the higher ion density and conductivity of the plasma reduce the DC bias, which can influence the damage introduced into the semiconductor substrate from the etch process. The platen power controls the bias voltage between the electrode and the plasma, and thus bombardment energy of the ions. It can be seen from **Figure 6.2.17** that the vertical etch rate is enhanced as the platen power increases as the molybdenum etch mechanism becomes more physical. **Figure 6.2.17** also shows a vertical etch rate of 4 nm/ min at zero platen power, which indicates the contribution of the purely chemical mechanism to the overall etch process.

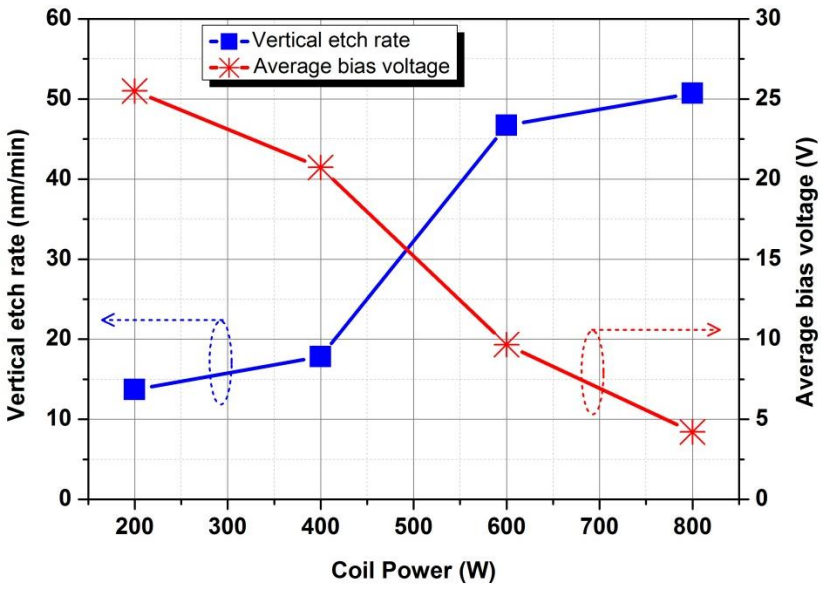


Figure 6.2.16 – Influence of coil power on vertical etching rate of molybdenum with platen power 2 W, chamber pressure 5 mTorr, SF_6/C_4F_8= 15 sccm/25 sccm

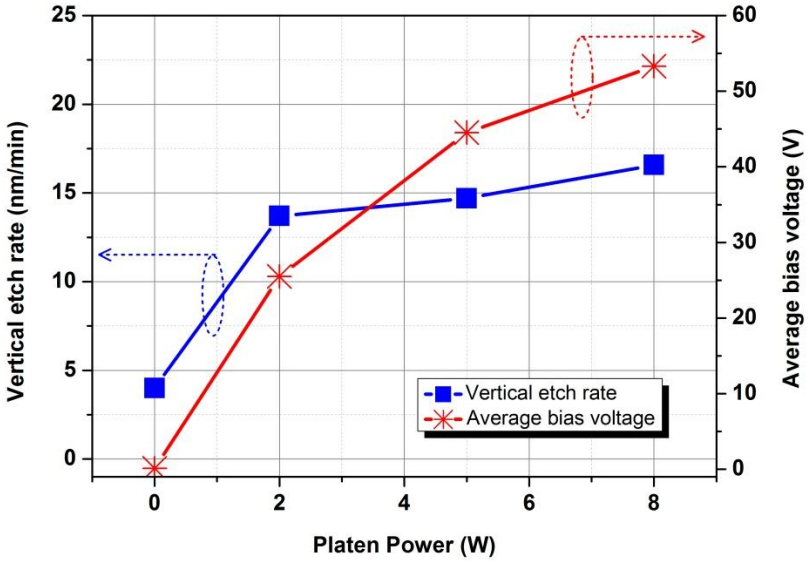


Figure 6.2.17 – Influence of platen power on vertical etching rate of molybdenum with chamber pressure 5 mTorr, coil power 200 W, SF_6/C_4F_8= 15 sccm/25 sccm

A key requirement of any metal gate etch process for high mobility III-V transistor realisation is that it does not introduce damage into the underlying semiconductor material. The source of damage is from bombardment by high energy ions and the presence of reactive species in the plasma [6.19]. To determine the degree of plasma etch induced damage, Van der Pauw structures formed from the HEMT structure shown in **Figure 6.2.18** where the $In_{0.53}Ga_{0.47}As$ cap layer has been removed by selective wet etching [6.25] were exposed for 60 seconds to the etch process with SF_6:C_4F_8=15 sccm:25 sccm, coil power of 200 W, chamber pressure of 5 mTorr and platen powers in the range 0 - 8 W. 60 seconds was chosen as this was the typical 20% over-etch time determined from the vertical etch rate studies, and therefore representative of the duration of plasma exposure that the semiconductor would experience. Before plasma exposure, the room temperature sheet resistance, channel mobility and electron concentration of the 2DEG InP HEMT structure were 330 Ω/□, 10,000 cm^2/ V s and 1.87×10^{12} cm^{-2} respectively.

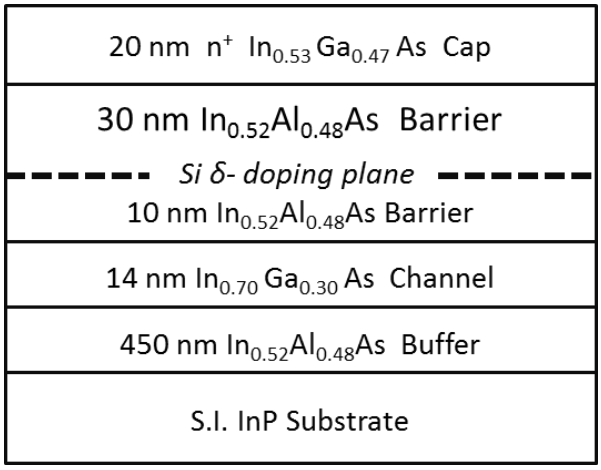


Figure 6.2.18 – 2DEG InP based HEMT layer structure

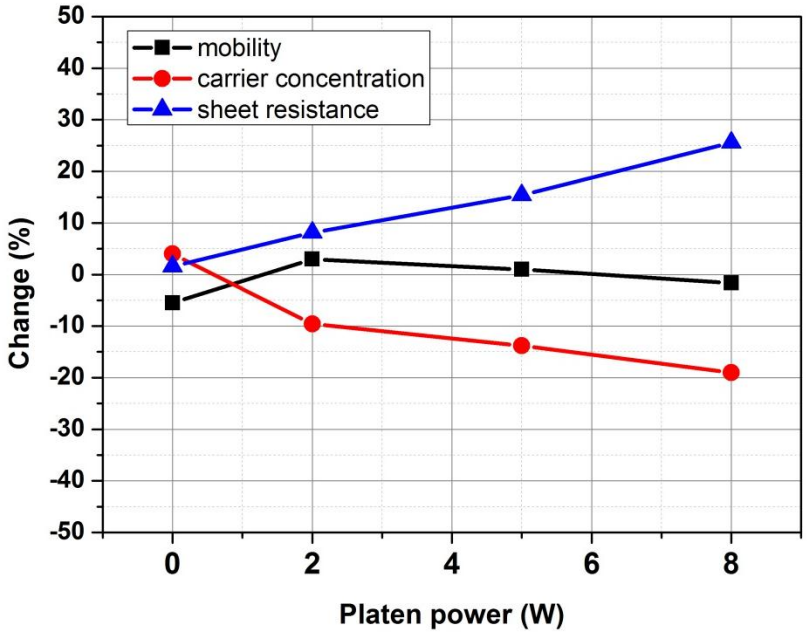


Figure 6.2.19 – Dependence of sheet resistance, channel electron concentration and mobility as a function of exposure of the Van der Pauw structures to the etching processes before and after ICP etching

Figure 6.2.19 shows the dependence of sheet resistance, channel electron concentration and mobility as a function of exposure of the Van der Pauw structures to the etching processes. For platen power of up to 2 W, there is an 8% increase in sheet resistance, primarily arising from a reduction in channel electron concentration, which may be due to a modification of the surface potential of the $In_{0.52}Al_{0.48}As$ barrier layer as a consequence of the surface exposure to

the plasma etch. However, there is no observable mobility degradation. The impact of plasma dry etch process on electron mobility and concentration in the channel may extend into the gate region, however as this is protected by molybdenum gate line, it is unlikely to be a significant issue.

After considering all factors including a practical vertical etch rate for efficient tool utilisation, the optimised conditions for low damage inductively coupled plasma etching of molybdenum with nanoscale critical dimensions are shown in **Table 6.2.4**. The etch rate selectivity of molybdenum and HSQ mask is 1:1.5.

Minimum Mo linewidth	30 nm
Vertical etch rate	13.7 nm/ min
Average bias voltage	25.5 V
Gas ratio	SF_6:C_4F_8=15 sccm:25 sccm
Platen power	2 W
Coil power	200 W
Chamber pressure	5 mTorr
Selective ratio Mo: HSQ	1:1.5

Table 6.2.4 – Optimised conditions of ICP etch process to define molybdenum nanoscale lines

The HSQ etch mask was then removed by 1.82% diluted HF solution treatment. **Figure 6.2.20a-f** show the molybdenum gate lines of vertical profile with nanoscale feature sizes of 50nm, 40nm and 30nm before and after HSQ removal.

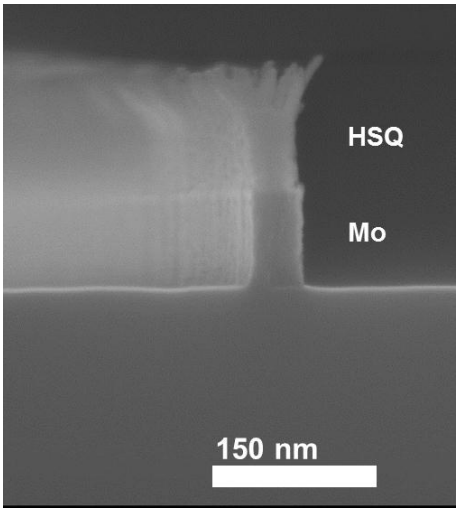


Figure 6.2.20a – 50nm Mo gate line before HSQ removal

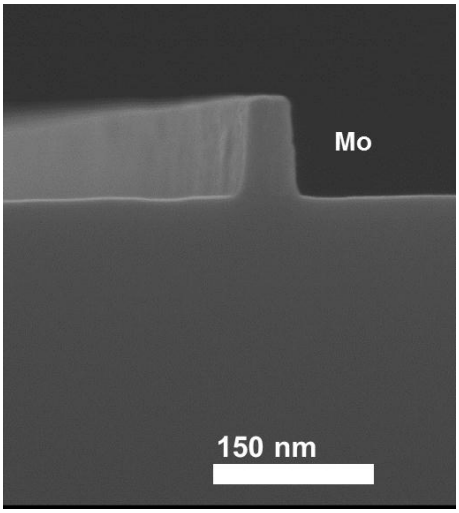


Figure 6.2.20b – 50nm Mo gate line after HSQ removal

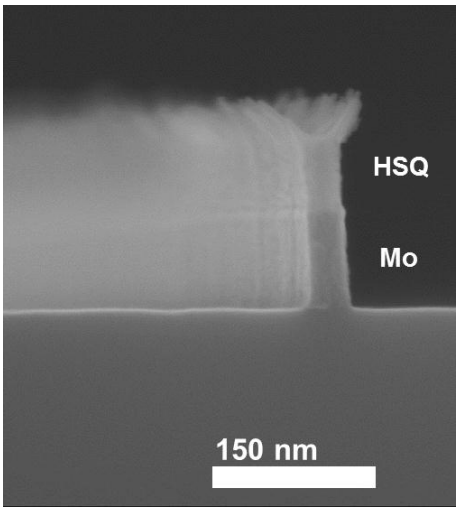


Figure 6.2.20c – 40nm Mo gate line before HSQ removal

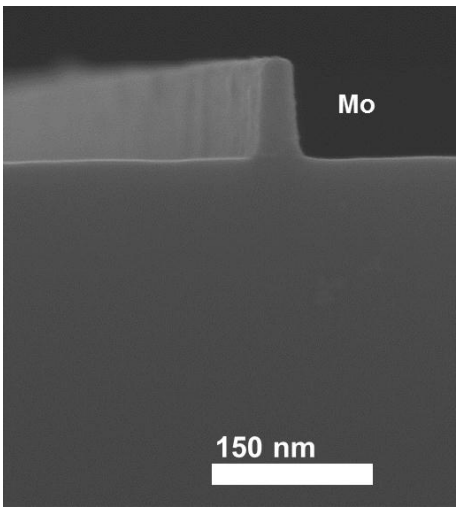


Figure 6.2.20d – 40nm Mo gate line after HSQ removal

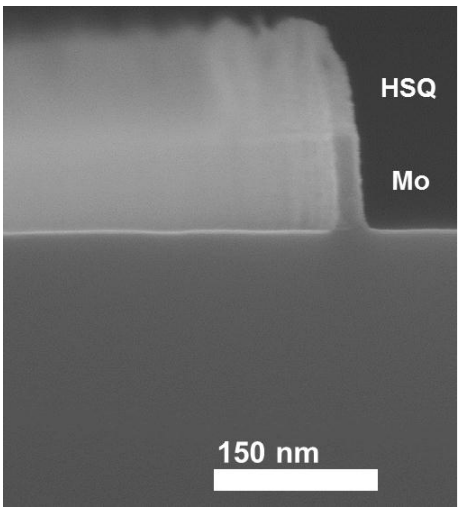


Figure 6.2.20e – 30nm Mo gate line before HSQ removal

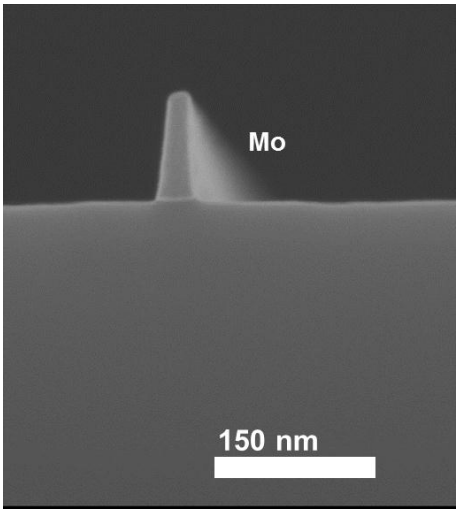


Figure 6.2.20f – 30nm Mo gate line after HSQ removal

The molybdenum gate lines patterned by the low damage inductively coupled plasma SF_6/C_4F_8 etching, with the highest resolution of 30nm critical dimension, are suitable for copper-based T-gate fabrication, which will be introduced in the **Section 6.2.4**.

6.2.4 Silicon compatible copper-based T-gate

In **Section 6.2.2**, the copper T-gate including T-gate foot and T-gate head fabricated by a single step copper electroplating process was presented. Whilst an encouraging development, the process described in **Section 6.2.2** cannot be obviously integrated in a full HEMT process flow due to having a metal seed layer covering the whole wafer which would be challenging to fully remove particularly in the region underneath the T-gate head. To overcome this limitation, a low damage inductively coupled plasma etching process to define molybdenum features with critical dimensions of 30 nm has been developed, which is described in **Section 6.2.3**. The patterned molybdenum lines would be the seed layer for the subsequent selective copper electroplating to form the T-gate head, with the molybdenum lines act as the T-gate foot. The main challenge at this stage is how to combine these two separate processes to

fabricate a copper-based T-gate, and in a way that the combined process can be incorporated into a full process flow for HEMT realisation.

In this section, the fabrication of copper-based T-gates using inductively coupled plasma etching of molybdenum and copper electroplating is introduced. The full process details are summarised in **Figure 6.2.21**.

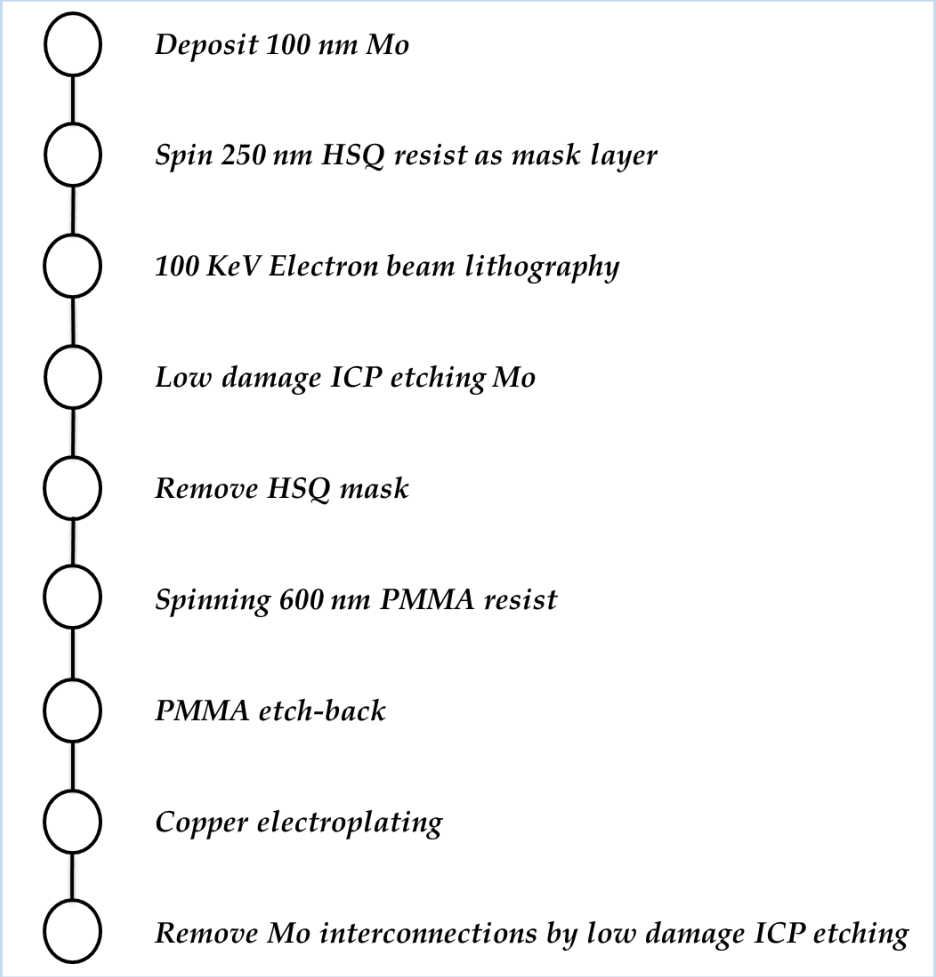


Figure 6.2.21 – Complete process flow of T-gate fabrication, including low damage inductively coupled plasma etched molybdenum gate foot & copper electroplated gate head

Firstly 100 nm molybdenum was blanket deposited on the whole sample by electron beam evaporation. The sample was then spin coated with 250 nm HSQ and patterned as illustrated in **Figure 6.2.22** by 100 keV electron beam lithography and subsequently developed to define the molybdenum etch mask.

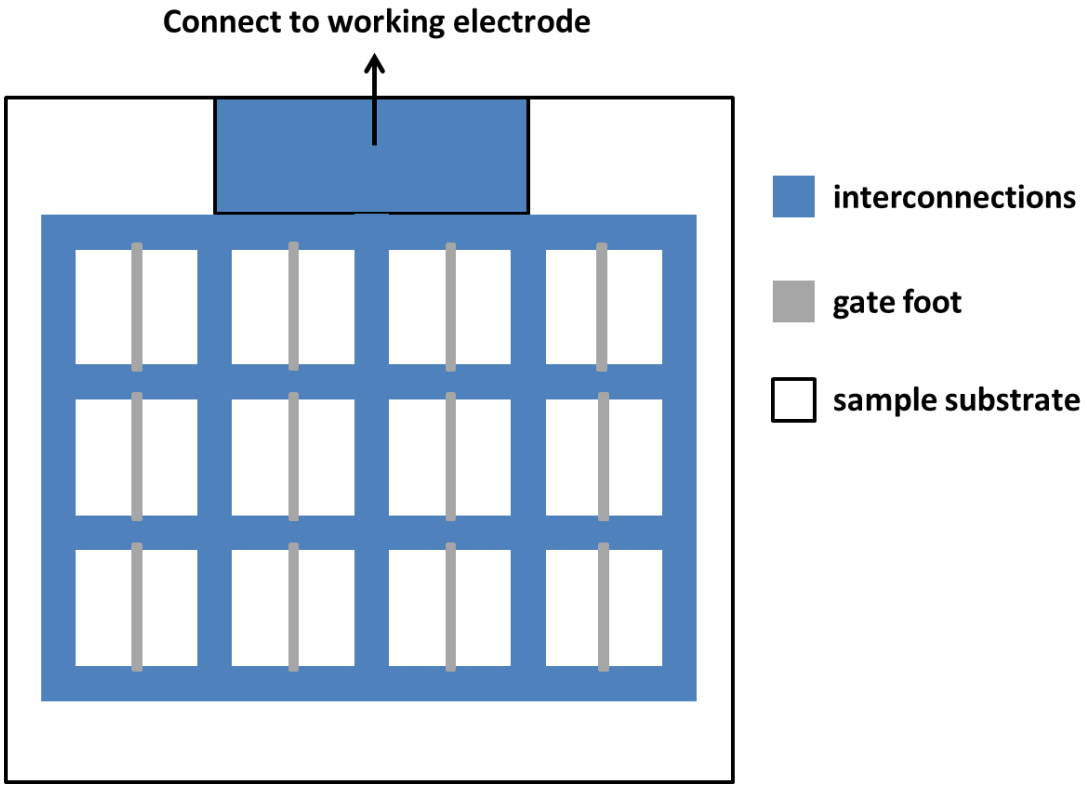


Figure 6.2.22 – Illustration of the pattern of molybdenum gate foot lines and molybdenum micron-scale interconnections

The optimised low damage inductively coupled plasma etch process described in **Section 6.2.3** was then implemented to transfer the pattern from the HSQ to the molybdenum. As shown in **Figure 6.2.22**, the molybdenum pattern includes the 50 nm gate foot lines (grey area in the pattern) and micron-scale "interconnect" structures (blue area in the pattern) joining each of the gate foot features. This can be thought of as a uniform plating base with areas removed, but because the molybdenum pattern is electrically continuous, all exposed areas of molybdenum will plate with copper. To enable selective electroplating of only the gate foot features, the interconnect structures have to be masked in some way. Then following copper electroplating, the interconnect structures can be selectively removed using the low damage etch process described in **Section 6.2.3**, leaving the electrically isolated electroplated copper T-gate features. The process flow is shown schematically in **Figure 6.2.23**.

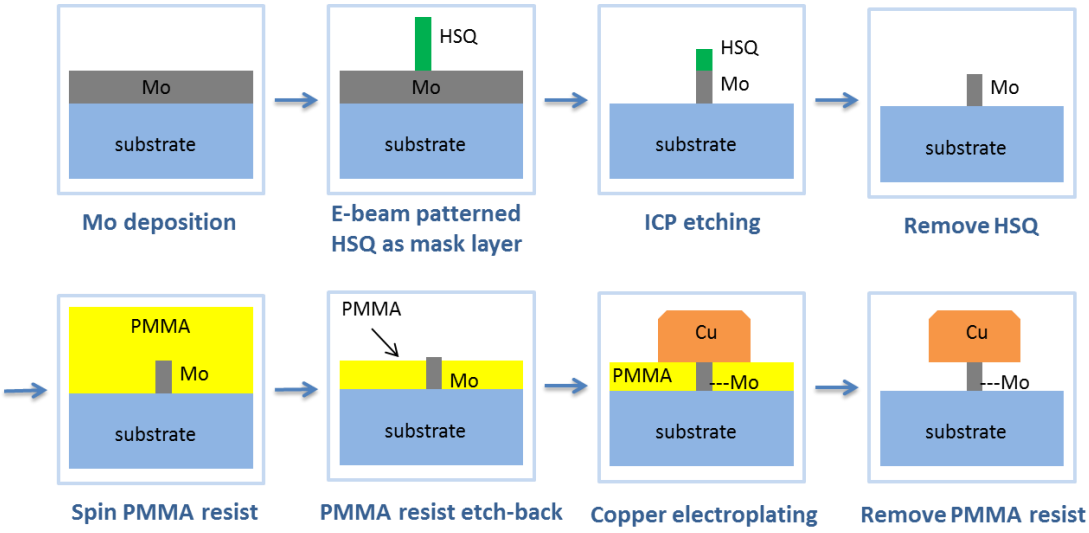


Figure 6.2.23 – The cross sectional view of the formation of a copper-based T-gate with a molybdenum "foot" and an electroplated copper "head"

A PMMA etch back process was used to enable the selective electroplating [6.26]. 600 nm 12% PMMA 2010 resist was spun on the sample covering the molybdenum patterns. The thickness of PMMA is different when it spun on nanoscale metal lines and metal pads with micron-scale features, as illustrated in **Figure 6.2.24**. As a result, the thickness of PMMA on the top of micron-scale molybdenum interconnections is larger than that on the 50 nm molybdenum gate foot lines.

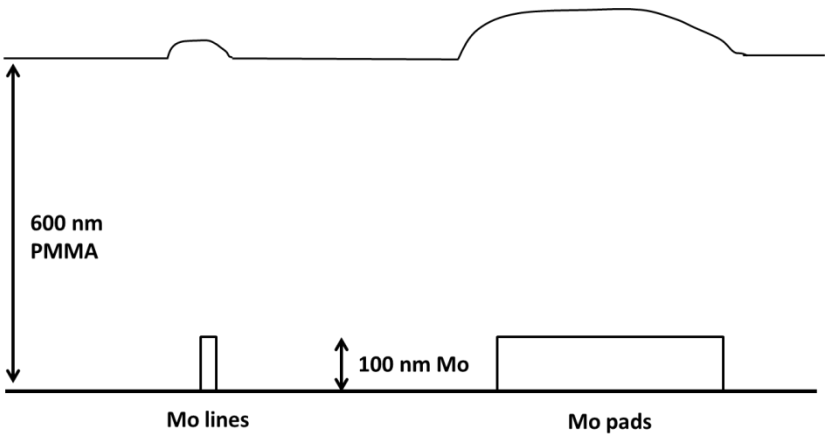


Figure 6.2.24 – Illustration of the situation of 600 nm PMMA spinning on molybdenum gate foot lines and molybdenum micron-scale interconnections, both of which are 100 nm high

When appropriate etch-back conditions are applied to remove PMMA on the sample, the situation can be achieved that the top of 50 nm molybdenum gate foot lines are exposed whilst the top of micron-scale molybdenum interconnections are still covered by PMMA, which acts as a mask in the subsequent copper electroplating process to prevent the micron-scale molybdenum interconnections from being electroplated. The PMMA etch-back is an oxygen-based reactive ion etching (RIE) process [6.26]. The etching time is determined by the thickness of PMMA resist left on the sample, which is monitored by an interferometer during the RIE process.

When the thickness of PMMA resist left on the sample is 70nm, in other words 530nm of PMMA resist has been etched off during the RIE etch back process, the top of the 50 nm molybdenum gate foot lines will be exposed whilst the top of the micron-scale molybdenum interconnections will not be exposed, as shown schematically in **Figure 6.2.25** and in a sample in **Figure 6.2.26**.

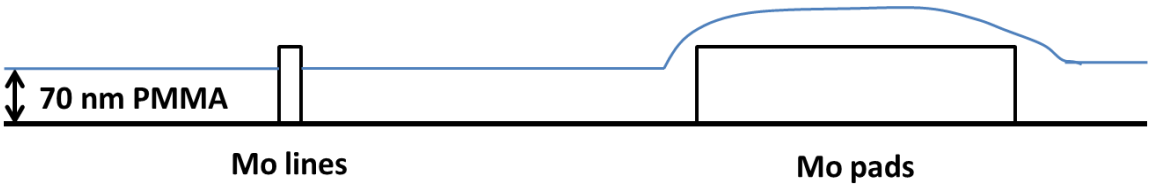


Figure 6.2.25 – Illustration of the PMMA etch-back process. 530 nm PMMA is etched off during the process and 70 nm PMMA is left on the sample, which exposes the top of molybdenum gate lines whilst the top of molybdenum interconnects are still covered by PMMA

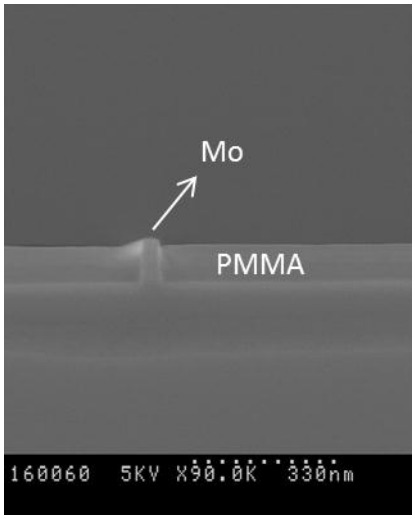


Figure 6.2.26 – 50 nm molybdenum gate foot lines exposed after PMMA resist etch-back process under appropriate conditions

Figure 6.2.27 presents a top view of a selective electroplated sample after the copper electroplating process, which clearly shows that the molybdenum gate foot lines were electroplated whilst the molybdenum interconnects were covered by the PMMA resist and not electroplated.

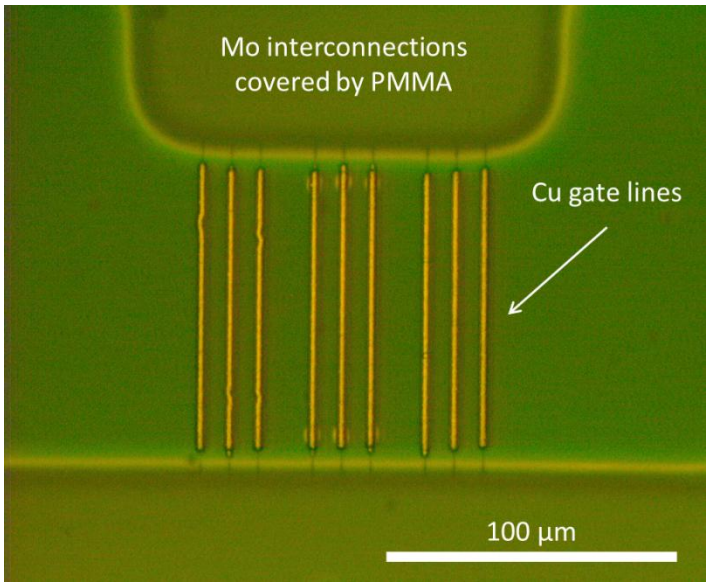


Figure 6.2.27 – Optical microscopy image of an electroplated sample. The molybdenum gate foot lines were electroplated by copper whilst the molybdenum interconnects were covered by PMMA

In the copper electroplating process step, the composition of the electrolyte is shown in **Table 6.2.5**.

Solute	**Conc. (g/l)**
Sulphuric Acid	200
Copper Sulphate	38.66
Polyethylene Glycol (PEG)	0.5
Sodium Chloride	0.1
Thiourea	0.01
3-mercapto-1-propanesulphoic acid (MPS)	0.01

Table 6.2.5 – Composition of the electrolyte for copper electroplating process for silicon compatible copper T-gate fabrication

The concentration of copper sulphate (38.66 g/L) and sulphuric acid (200 g/L) chosen balances the small roughness and low sheet resistance of the copper film, based on the experimental results presented in **Table 6.2.3** mentioned in **Section 6.2.1.1**.

For an electroplating time of 600 seconds, a T-gate with 50 nm molybdenum gate foot and 2.5 µm copper gate head using the process described above was achieved, as presented in **Figure 6.2.28**. The approach is fully silicon compatible, and most importantly, can be integrated with a full HEMT process flow.

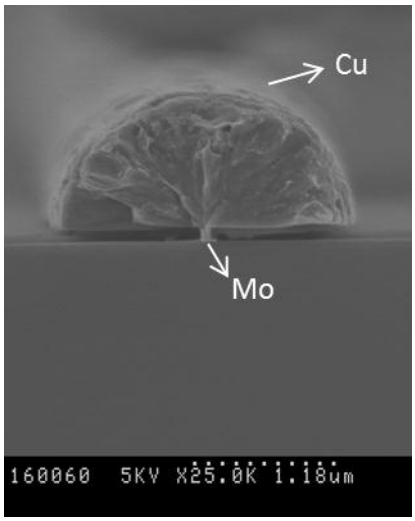


Figure 6.2.28 – Completed T-gate with 50 nm molybdenum gate foot and 2.5 µm copper gate head

The electrical performance of the T-gate fabricated using the process described above was then investigated.

The DC resistance of the copper-based T-gate was measured by using four-point probe method and the test structure is shown in **Figure 6.2.29**. The current applied on the T-gate was swept from 10 mA to 30 mA and two Kelvin probes were placed on the two terminals of the T-gate test structure to monitor the resulting voltage drop.

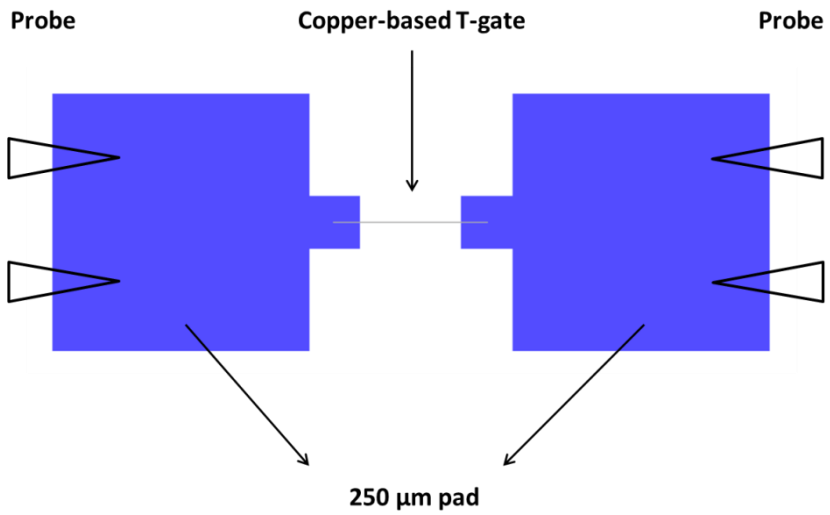


Figure 6.2.29 – The test structure of T-gate DC resistance measurement

Figure 6.2.30 shows the normalised DC resistance of a T-gate comprising 60 nm molybdenum gate foot and 1.2 µm copper gate head produced by reducing the electroplating time to 300 seconds.

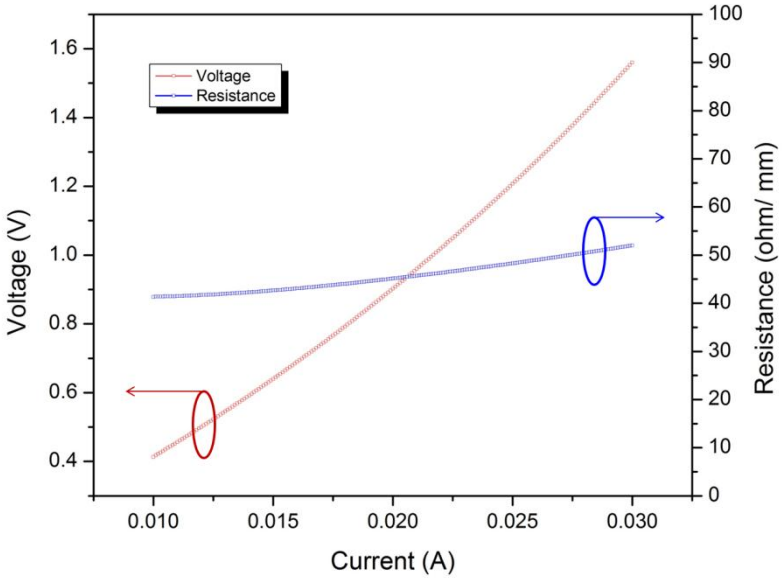


Figure 6.2.30 – Normalised I-V curve from a T-gate comprising 60 nm molybdenum gate foot and 1.2 μm copper gate head

At lower current levels, the normalised DC resistance of the T-gate is 42 Ω/mm. Higher resistance can be seen at the larger currents due to current crowding effects [6.27].

To validate the resistance of the Cu T-gate, consider a 1 mm wide structure with 60 nm molybdenum gate foot and 1.2 μm copper gate head. This can be regarded as two resistors one representing the molybdenum gate foot and the other the copper gate head, in parallel. The resistances of the molybdenum foot and copper head can be calculated based on the respective textbook resistivities of these materials. As a result, the theoretical value of the resistance of the T-gate with the geometry described above is 30 Ω. The reason that the experimentally obtained value is higher than that determined theoretically may be due to the fact that the copper head formed by the electroplating process is not uniform and has a porous structure, which increases its resistance. The porous structure may result from a non-optimised rate of growth of the electroplated copper, which can be addressed in future by adjusting the composition of the electrolyte and electroplating conditions.

6.3 Non-annealed ohmic contacts and material design

To incorporate the silicon compatible copper-based T-gate described in **Section 6.2** into a full HEMT fabrication flow, a "gate-first" approach is required to allow the array of interconnected molybdenum gate foot structures to be realised on a planar substrate, thereby overcoming any issues with unwanted connections to previously defined source and drain contacts. This constrains the overall process flow as a Schottky gate will not withstand the anneal step usually required for low resistance ohmic contact formation, and therefore a method to form low resistance, non-annealed source and drain contacts such as that described in [6.28] is required.

As described in **Section 2.1.1**, a typical HEMT layer structure consists of a highly doped cap layer for low resistance ohmic contacts formation, and a barrier layer which contains a single layer of delta doping, followed by a thin spacer layer to separate donors from the channel. In standard ohmic contact fabrication, an annealing process is implemented after the metallisation to diffuse the contact metal into the semiconductor material, which minimises the height of the potential barriers formed at the interfaces between the various materials in the overall heterostructure. If there is no annealing process, there will be no metal diffusion and therefore the magnitude of the potential barriers will be determined by the electron affinities of the various materials.

To reduce the magnitude of the potential barriers from the source/drain to the channel, an additional delta doping is introduced into the layers structure [6.28].

The key issue here is to ensure that the double delta doping in the barrier layer are of suitable concentrations and at the appropriate positions, which provides low potential barriers from the ohmic contacts to the channel whilst there is no parallel conduction channel in the recessed region underneath the gate.

To find suitable concentrations and positions of the delta doping planes, a Poisson/Schroedinger solver [6.29] was utilised to simulate conduction band profiles and

carrier concentration distributions for various doping plane concentrations and positions within the overall device layer structure. An optimal double delta doping layer structure for an InP-based HEMT was finally achieved, as shown in **Figure 6.3.1**.

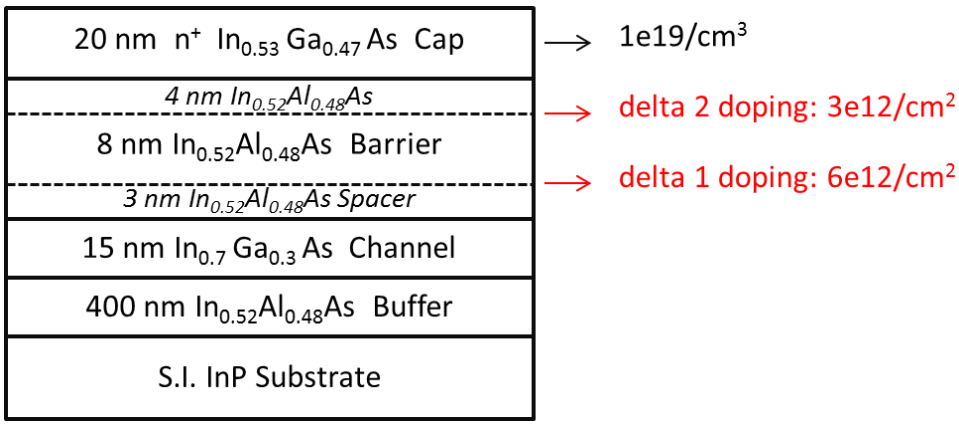


Figure 6.3.1 – Double delta doping layers structure of InP HEMT

In this optimal layer structure, there is no significant potential barrier to carrier transport from ohmic contacts to the channel, and at the same time no parallel conduction channel occurring in the recessed region where the cap layer is removed, as shown in **Figure 6.3.2** and **Figure 6.3.3**, which demonstrate the conduction band profile (blue) and carrier concentration distribution (red) through the cap/barrier/spacer/channel layers in the cases of capped and cap removed situations respectively.

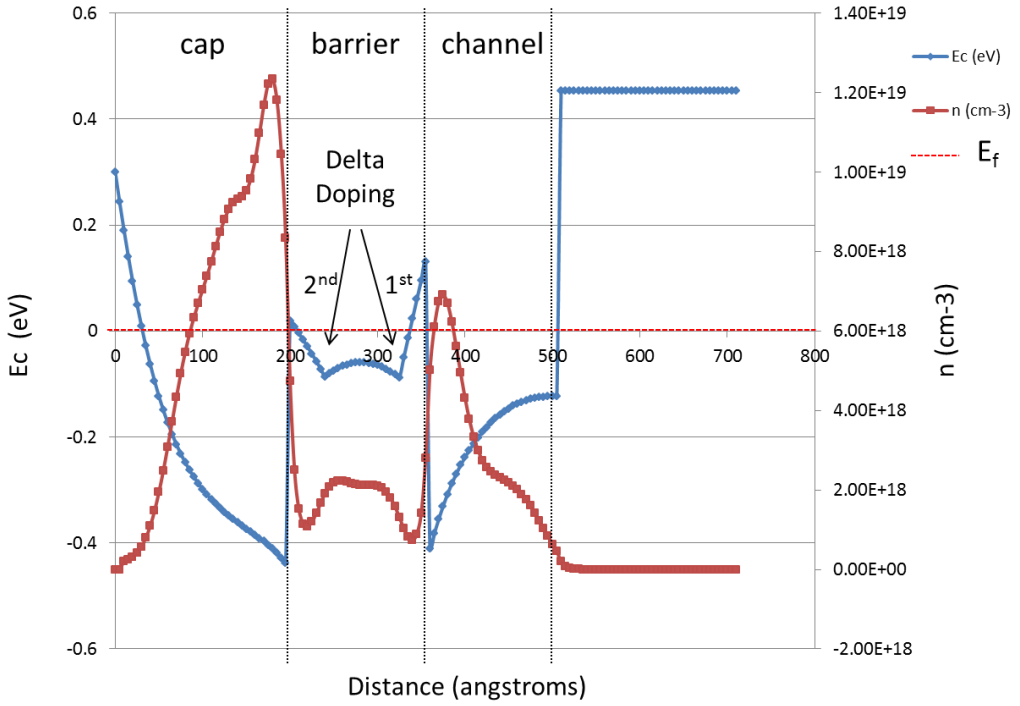


Figure 6.3.2 – Conduction band profile (blue) and carrier concentration distribution (red) in capped double delta doped InP HEMT

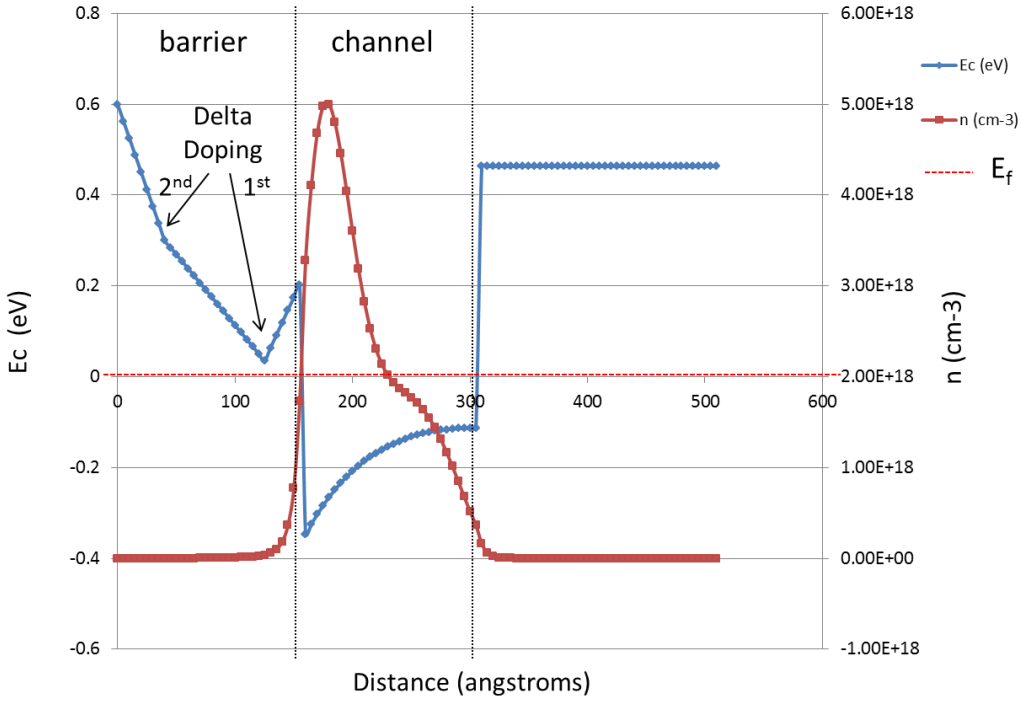


Figure 6.3.3 – Conduction band profile (blue) and carrier concentration distribution (red) in double delta doped InP HEMT without cap layer

The material with layer structure shown in **Figure 6.3.1** was grown by molecular beam epitaxy (MBE) in Glasgow. To establish the properties of the non-annealed ohmic contacts and determine the channel transport properties, TLM and Van der Pauw test structures were realised on the material. The ohmic contacts were formed from 100 nm electron beam evaporated Au which without an annealing process, yielded a contact resistance of 0.211 Ω.mm. The contact resistance might be further reduced by using Au/Ge/Ni metallisation as the ohmic metal [6.30].

In addition, Van der Pauw characterisation of this structure yielded the sheet resistance, mobility and carrier concentration with and without the cap layer as shown in **Table 6.3.1**.

	Capped	**Cap removed**
Sheet Resistance (Ω/□)	98	148
Mobility (cm^2 / Vs)	4674	6007
Carrier Concentration (cm^{-2})	1.356×10^{13}	7.021×10^{12}

Table 6.3.1 – VDP measurements of double delta doped InP HEMT structure shown in **Figure 6.3.1**

The value of carrier mobility is lower than that of typical single delta doped InP HEMT material which commonly has a carrier mobility around 10000 cm^2/Vs when cap layer removed [6.31]. It may be due to the thinner spacer layer of 3 nm in the designed structure mentioned above than a typical value, as well as the peak carrier concentration occurring very close to the channel-spacer interface as shown in **Figure 6.3.3**. Therefore, the carriers in the channel may suffer greater ionised impurity scattering and hence lower mobility.

6.4 Gate-first process flow for HEMT realisation

The gate-first process flow for HEMT realisation including silicon compatible copper-based T-gate process and non-annealing ohmic contact formation is presented in **Figure 6.4.1**.

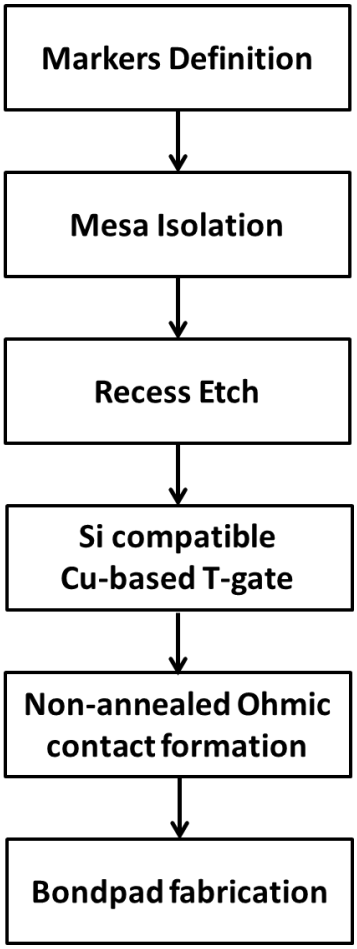


Figure 6.4.1 – Gate first process flow for HEMT fabrication

The process starts with markers definition and mesa isolation, which are similar to the standard HEMT fabrication process described in **Section 3.4**. However, the subsequent process steps are different.

A recess etch step prior to the gate formation is required in this process flow, since the gate formation is different from the standard T-gate fabrication approach. In standard T-gate fabrication, a T-gate resist profile is defined first for the subsequent metallisation and lift off. The recess etch step is performed prior to the metallisation and after the T-gate resist profile

definition, since the gate length has been defined in the T-gate profile formation step. In silicon compatible copper-based T-gate formation, as described in **Section 6.2**, the gate foot is defined by dry etching molybdenum using patterned HSQ as a mask, instead of lifting off gold-based metallisation. Therefore, in the gate-first process, the recess etch step needs to be implemented before the gate formation. In addition, a double recess etch is required to remove the cap layer and also part of the barrier layer, since there is an additional delta doping plane in the barrier and close to the cap layer. As a result, both succinic acid etch and orthophosphoric acid etch are used in the double recess etch, as illustrated in **Figure 6.4.2**.

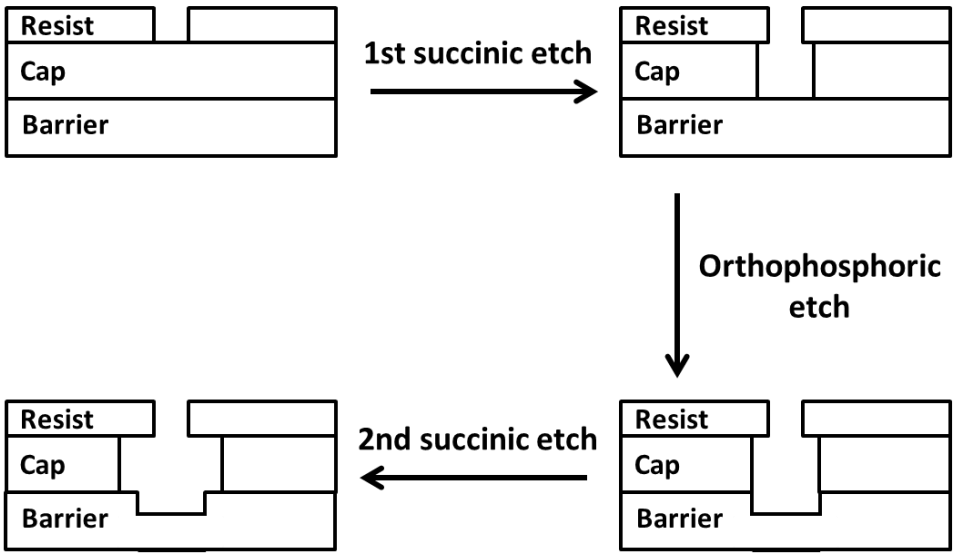


Figure 6.4.2 – Illustration of double recess etch

As shown in **Figure 6.4.2**, a layer of PMMA resist is spun on the sample and patterned by electron beam lithography to form the gate foot trench, in which the double recess etch will be implemented subsequently. A succinic acid etch is firstly used to remove the cap layer and followed by a non-selective orthophosphoric acid etch to remove the additional doping layer in the barrier to minimise the gate leakage current, finally a second succinic acid etch is used to enlarge the cap layer etch ensuring gate metal not contacting with the conductive cap layer [6.28].

After the double recess etch, the copper-based T-gate can be fabricated using the silicon compatible process presented in **Figure 6.2.21** described in **Section 6.2**, as illustrated in **Figure 6.4.3**.

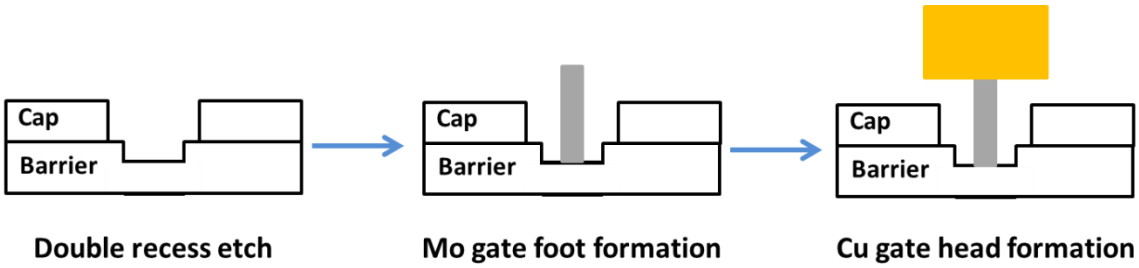


Figure 6.4.3 – Illustration of molybdenum gate foot and copper gate head formation in recess region formed by double recess etch

An alignment is required between these two steps to ensure gate foot locating in the middle of the recess region. This approach, using the Penrose marker strategy [6.32] has previously been successfully implemented in HEMT realisation.

In non-annealed ohmic contact formation, electron beam lithography and metallisation are needed similar to the standard process, but without annealing. Bondpad fabrication is similar to the standard approach. The complete gate-first process flow for HEMT realisation is detailed in **Appendix I**. Due to time constraints, the fabrication of this final device was not completed. However, this proposed solution for the realisation of a silicon compatible Cu-based T-gate HEMT device is promising for future work mentioned in **Chapter 8**.

6.5 Summary

In this chapter, a copper electroplating process and the development of low damage inductively coupled plasma etching nanoscale molybdenum with the smallest feature of 30 nm are described, which are fundamental to the realisation of a silicon compatible copper-based T-gate comprising a 50 nm molybdenum gate foot and a 2.5 μm copper gate head, which is also described. In addition, the design of a double delta doped InP HEMT layer structure for non-annealing ohmic contact formation as required for the copper-based T-gate process integration was presented, and shown to produce ohmic contacts with acceptable levels of performance. Further, a gate-first process flow for HEMT realisation incorporating the copper-based T-gate is presented.

In summary, in this chapter, a viable route to the realisation of III-V HEMTs using a silicon compatible T-gate module has been proposed and all key enabling modules validated.

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Chapter 7

60nm Au-based T-gate HEMT

7.1 Introduction

Following the achievement of the copper-based T-gate fabricated by silicon compatible processes described in **Chapter 6**, a sample of gold-based T-gate HEMTs was realised by the conventional fabrication process flow to establish a baseline to compare the conventional gold-based T-gates with those fabricated by a copper-based silicon compatible process.

This chapter mainly describes utilising the standard fabrication process outlined in **Chapter 3** to realise functional gold-based T-gate HEMT with gate length of 60 nm. In addition, the comparison between the gold-based T-gate and the copper-based T-gate, specifically in relation to process technologies and electrical performance, is also presented in this chapter.

7.2 Fabrication of 60 nm Au-based T-gate HEMT

The complete process flow for fabricating 60nm Au-based T-gate HEMTs includes mesa isolation, ohmic contact fabrication, T-gate realisation in a gate recess and bondpad formation. In the devices described in this chapter, mesa and ohmic contacts were realised by the University of Manchester by photolithography as part of a collaboration to evaluate the performance of their micron-scale critical dimension device flow with sub-100 nm T-gates produced in Glasgow, so there was a requirement to establish registration strategies to allow successful alignment of the electron beam written T-gates to previously photolithographically defined source and drain contacts. Manchester also provided the epitaxial material from which the HEMTs were realised, a schematic of which is shown in **Figure 7.2.1**. The cap layer is 20nm $In_{0.53}Ga_{0.47}As$ silicon doped at 2×10^{19} cm^{-3}; the undoped barrier layer is 15nm $In_{0.52}Al_{0.48}As$; below which is placed a silicon delta-doping layer. A 10 nm spacer layer of undoped $In_{0.52}Al_{0.48}As$ separates the delta doping layer from the 14nm undoped $In_{0.7}Ga_{0.3}As$ channel. An additional delta-doping plane is introduced into the $In_{0.52}Al_{0.48}As$ back barrier 10 nm below the device channel.

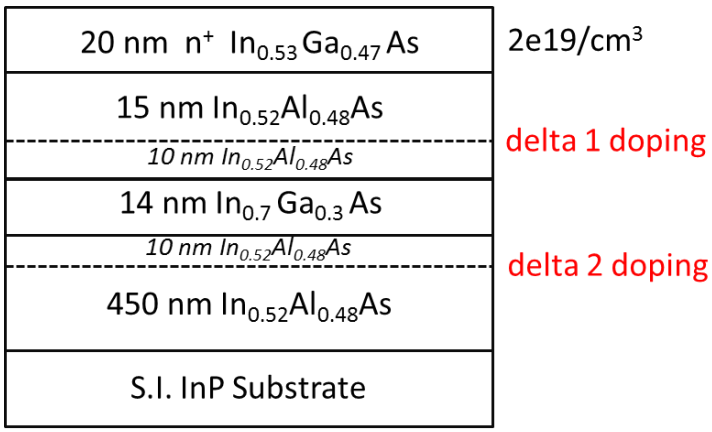


Figure 7.2.1 - HEMT structure material

The mesa was etched by orthophosphoric acid/hydrogen peroxide mixture with a concentration ratio of 3:1:50 H_3PO_4 : H_2O_2 : H_2O, and a mesa height of 150 nm was achieved.

The source-drain contacts were separated by 2 μm. A 150 nm thick AuGe/Au metallisation was used, and using TLM test structures, yielded a contact resistance of 0.053 Ω.mm, as characterised by the University of Manchester, with the cap layer in place between the ohmic contacts. 20 μm×20 μm registration markers were defined at the same time as the ohmic contacts.

The standard fabrication method of T-gate realisation in HEMTs includes the formation of a suitable resist profile using a combination of resists of different sensitivities and an appropriate electron beam writing strategy, a wet chemical gate recess etch in which both the etch depth and the length of the recess compared to the gate foot is controlled, and gate metallisation by a lift off process.

The first step in this process flow is to define a T-gate profile of appropriate dimensions in resist. Electron beam lithography is used to define T-gates with nanoscale critical dimensions. The standard process technology involves using several layers of resists with different sensitivities in a single step electron beam lithography, as discussed in **Chapter 3**. As the sub-100 nm single step electron beam lithography process had not been run in Glasgow for a number of years, there was a need to re-establish it on the Vistec VB6 electron beam tool, and to determine the resolution limits of the process on this machine. A previously developed T-gate process based on UVIII and PMMA resists separated by a thin layer of LOR was explored [7.1]. In this process, a 70 nm 2.5% PMMA 2041 is first spun on the sample at 3500 rpm for 60 seconds, and subsequently baked at 180℃ in an oven for 120 minutes. It is in this layer of resist that the gate foot will ultimately be defined. A 40 nm layer of LOR is then spun at 5000 rpm for 60 seconds, and the sample baked at 180℃ in an oven for 15 minutes. This layer prevents the subsequent UVIII layer from intermixing with the PMMA. Finally, a 300 nm UVIII layer is spun on the sample at 3500 rpm for 60 seconds and baked at 120℃ on a hotplate for 60 seconds. This resist stack was chosen as it had previously enabled the lift off of 200 nm thick T-gates with footprint size of 50 nm in a Leica Cambridge EPBG5 electron

beam tool [7.1]. The challenge was to transfer this process to the Vistec VB6 electron beam lithography tool.

The writing strategy for T-gate definition involves writing a high dose "central" line which exposes each of the resist layers – this ultimately defines the gate foot. To increase the size of the gate head, two features are defined either side of the central line with a dose which is sufficient to expose the higher sensitivity UVIII, but not the PMMA. Identifying the appropriate doses and feature sizes for the gate foot and head exposures was the first aspect to be performed in establishing the T-gate process.

The pattern designed for writing T-gates by electron beam lithography is shown in **Figure 7.2.2**, including a narrow central line for gate foot definition and a large area for gate head exposure. The feature size of the gate foot is usually designed smaller than the desired gate length, since this central line is written by a high dose electron beam through a thick resist stack, and so the transferred pattern will be larger than designed.

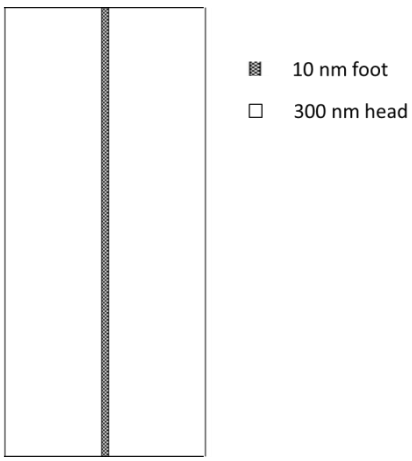
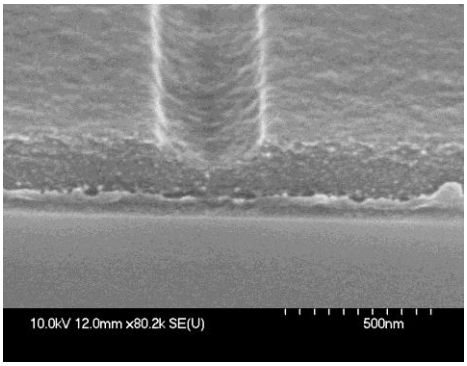
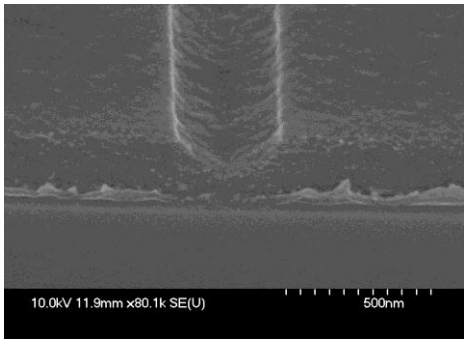
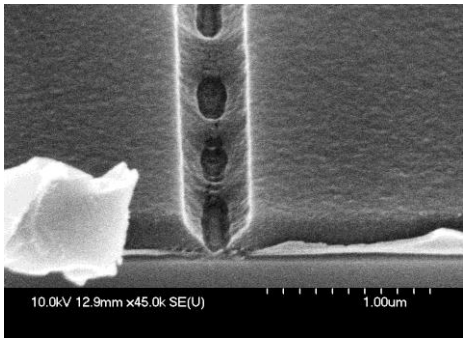
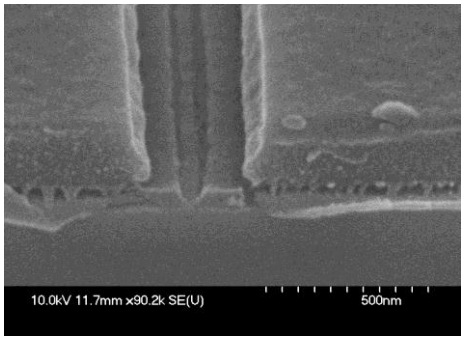
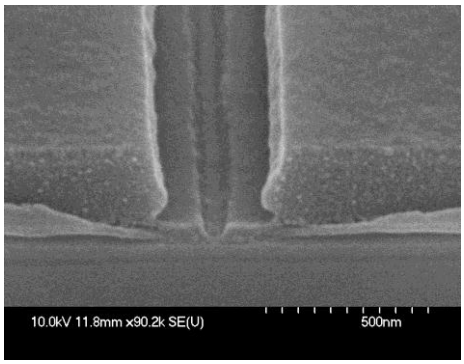
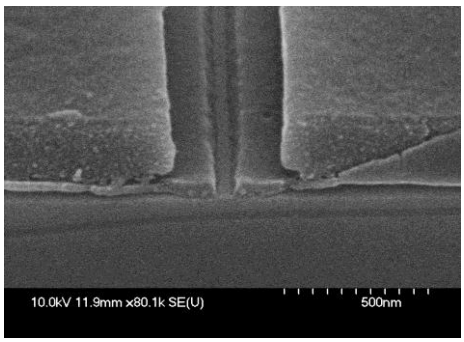
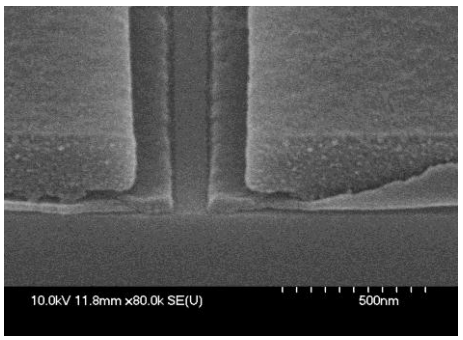


Figure 7.2.2 – Design pattern for T-gate exposure

A dose-test experiment was implemented to determine the best values of exposure for both foot and head layers. This experiment was conducted on an unpatterned, planar GaAs substrate with the first layer resist of PMMA spinning at the speed of 3500 rpm. Dose values of the foot ranged from 750 $\mu C/cm^2$ to 4000 $\mu C/cm^2$ with dose values of the head from 67 $\mu C/cm^2$ to 250 $\mu C/cm^2$. The test results are summarised in **Table 7.2.1**.

SEM	Foot dose ($\mu C/cm^2$)	Head dose ($\mu C/cm^2$)	Foot feature (nm)	Head feature (nm)
	787	70	Not exposed	Not completely exposed
	866	75	Not exposed	Not completely exposed
	1270	101	Not completely exposed	Not completely exposed

	1397	109	Not completely exposed	270
	1465	113	Not completely exposed	290
	1691	127	60	365
	3303	215	118	383

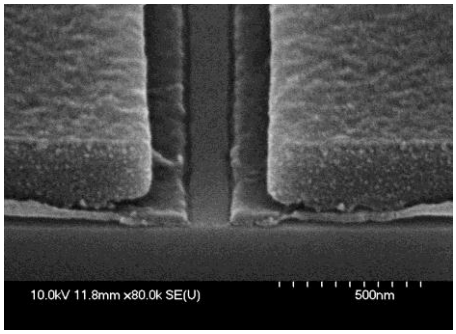
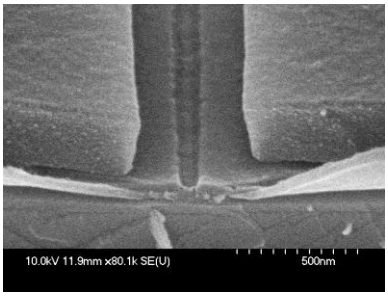
	4000	250	140	408

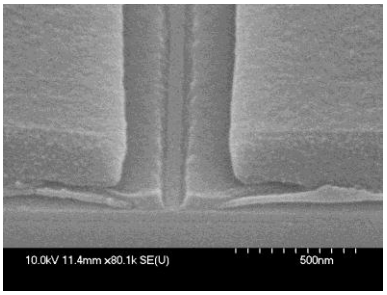
Table 7.2.1 – T-gate dose-test results

From **Table 7.2.1**, it can be seen that a suitable T-gate resist profile is obtained for the dose values of 1691 $\mu C/cm^2$ and 127 $\mu C/cm^2$ for the foot and head layers respectively, which are the dose values applied into the electron beam lithography writing strategy in this work. When dose values are smaller than that, the gate foot is not completely exposed. When larger dose values are used, the feature size of the gate foot increases resulting from over exposing the resist.

This optimised writing strategy was then applied to HEMT devices with 150nm thick ohmic contacts as mentioned above. The topography introduced by the ohmic contacts results in an increase in resist thickness in the 2 μm gap between the source and drain contacts. To mitigate this, the spin speed when coating the sample with PMMA was modified. An experiment was conducted with various spin speeds of PMMA on samples with 150 nm ohmic contacts and using the optimal exposure conditions established on the planar substrate as mentioned above. At a PMMA spin speed of 3700 rpm, the foot was underexposed as showed in **Figure 7.2.3 (a)**. However, increasing the PMMA spin speed to 3900 rpm, resulted in correct exposure, as showed in **Figure 7.2.3 (b)**.



a) – 3700 rpm PMMA



b) – 3900 rpm PMMA

Figure 7.2.3 – T-gate resist profiles in a 2 μm source-drain gap for PMMA spinning speeds of 3700 rpm and 3900 rpm

As highlighted in **Chapter 3**, after gate lithography, and prior to gate metallisation, a recess etch step is used to remove the cap layer in the gate region. In the case of the InP based HEMT material utilised in this work, a succinic acid/hydrogen peroxide chemistry with controlled pH was used as it selectively etches the InGaAs cap layer, while terminating on the InAlAs barrier layer [7.2]. Therefore, the vertical etch reaction will terminate on removal of the 20nm InGaAs cap layer, though the etching reaction will still continue laterally. It is critically important to control the lateral etching size, as it impacts the access resistance and thereby the transconductance of the device.

Following the recess etching and prior to the gate metallisation, a 30s rinse in dilute hydrochloric acid with a concentration of 1:4 HCl: H_2O followed by another 30s DI water rinse de-oxidation treatment was used to remove any surface oxide layers that may have formed on the InAlAs barrier layer following the gate recess etch process. This de-oxidation step was included to improve the performance of the Schottky gate contacts. The gate metal was a stack of 15 nm Ti, 15 nm Pt and 160 nm Au, deposited by electron beam evaporation, and lifted off in warm acetone. As shown in **Figure 7.2.4**, a 60nm footprint Au-based T-gate with a 130nm laterally etched recess was realised, in source-drain gaps, as required for device realisation.

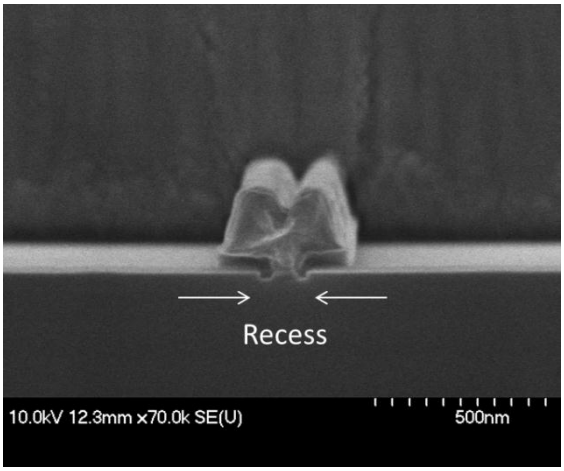


Figure 7.2.4 – SEM cross-sectional view of a 60nm T-gate with gate recess of 130nm lateral width and 20nm vertical depth

In the full HEMT device flow, after the optimised 60 nm T-gate had been formed, coplanar waveguide (CPW) bondpads in a ground-signal-ground configuration with signal width of 54 μm and signal to ground separation of 29.25 μm designed by the University of Manchester, were defined by e-beam lithography. Simulation predicts that these geometries will result in a characteristic impedance of 47.26 Ω, which is somewhat mismatched to the RF measurement system used for the device evaluation. The bondpad metallisation, defined by electron beam evaporation and lift off, comprised 50nm NiCr for good adhesion and 1200nm Au to reduce RF losses.

A top view of a completed 60 nm Au-based T-gate InP HEMT and detail of the gate-gate feed region are shown in **Figure 7.2.5**. Full details of the device process flow are presented in **Appendix II**.

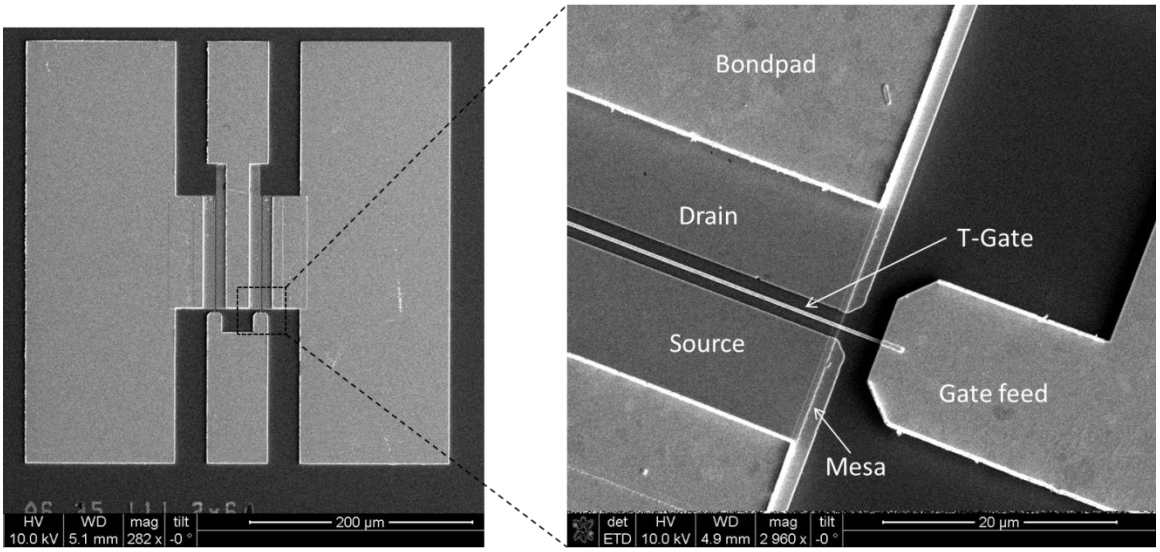


Figure 7.2.5 – SEM top view of a 60nm Au-based T-gate InP HEMT and detail of gate-gate feed region

7.3 DC and RF characterisation of the device

The normalised DC output characteristics for a 2×15μm device, which has two gate fingers with the device width of 15 μm, is shown in **Figure 7.3.1**.

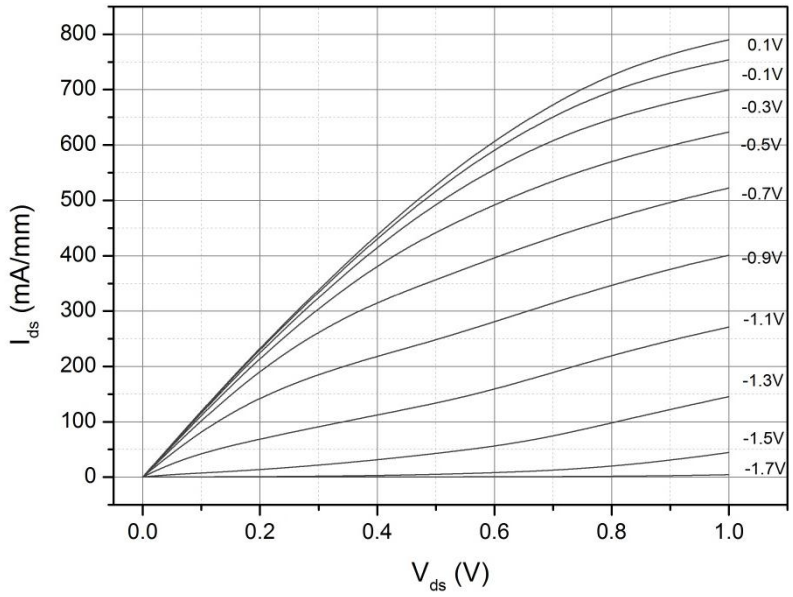


Figure 7.3.1 – Normalised output I_{ds}-V_{ds} characterisation from a 60nm Au-based T-gate InP HEMT

In this figure, the drain voltage is swept from 0 to 1 V in steps of 200 mV, and the gate voltage from -1.7V to +0.1V in steps of 0.2V. Beyond 1 V drain bias, the device began to breakdown. The drain current achieved is around 800 mA/mm.

The transfer characteristics are presented in **Figure 7.3.2**. The voltage applied on the gate is swept from -2.1V to 0V, while the drain voltage is varied from 0V to 1.0V in steps of 0.2V.

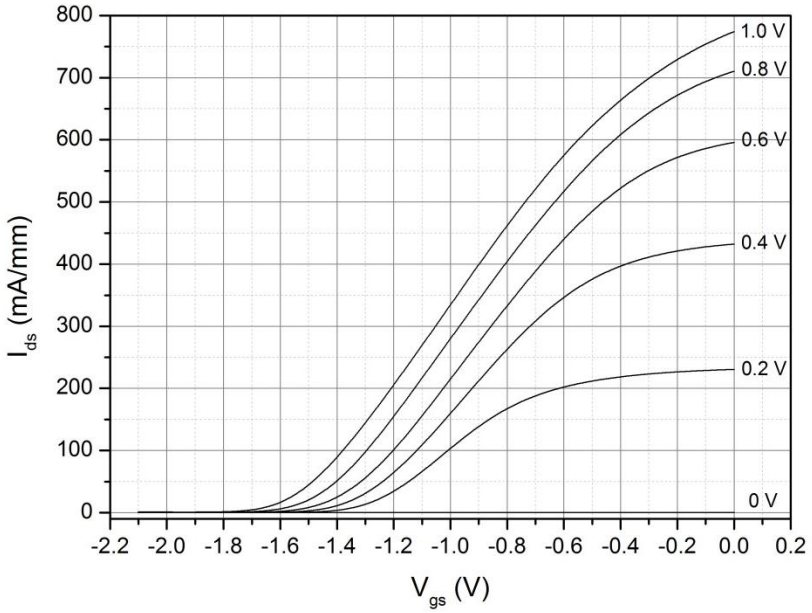


Figure 7.3.2 – Normalised transfer I_{ds}-V_{gs} characterisation from a 60nm Au-based T-gate InP HEMT

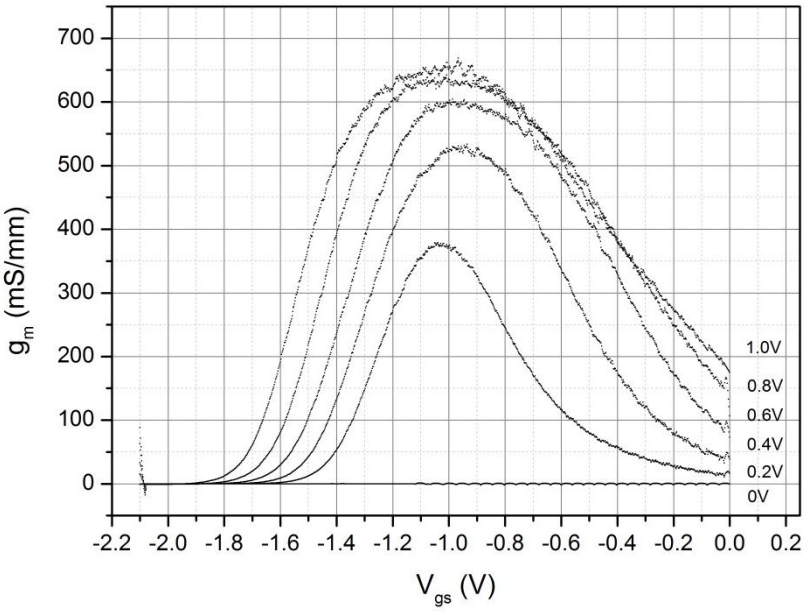


Figure 7.3.3 – Normalised transconductance g_m-V_{gs} characterisation from a 60nm Au-based T-gate InP HEMT

The transconductance plots for a range of drain voltages are shown in **Figure 7.3.3**. The maximum transconductance is 650 mS/mm at gate and drain voltages of -1.0V and 1.0V

respectively. The transconductance could be increased by reducing the gate-2DEG separation, which around 30nm in the material utilised in this work (the 2DEG plane is usually formed around 5nm below the interface between the spacer layer and channel).

Determining the bias conditions for peak transconductance is important as it is usually at around these that a HEMT will display the highest values of f_T and f_{max} which are determined from on-wafer frequency dependent S-parameter measurement. As described in **Chapter 4**, the RF measurement system was calibrated using the SOLT technique to place the reference planes for the on-wafer measurement at the wafer probe tips. S-parameters were obtained in the frequency range 10 MHz to 67 GHz at the bias condition for peak transconductance.

The equivalent circuit model described in **Chapter 2** was constructed in Agilent Advanced Design System (ADS) software to represent the HEMT, and by fitting the measured S-parameters to those from the equivalent circuit model, the intrinsic and extrinsic circuit elements of the device can be established.

In **Figure 7.3.4**, simulated and measured S-parameters are presented. S_{11} & S_{22} are displayed in Smith charts and S_{12} & S_{21} are displayed by magnitude and phase in linear plots separately. The measured S-parameters (blue) are compared with those generated by simulating the equivalent circuit model in ADS (red). Good agreement is found between the experimental and simulated S-parameters in S_{11}, S_{22}, S_{12} and the phase of S_{21}. It was not possible to accurately fit the magnitude of S_{21}, which might result from the mismatch between the characteristic impedance of the bondpad and that of the RF measurement system. However within range of the frequency below 10 GHz or above 60 GHz, the measured S_{21} matches with the modelled S_{21} in magnitude.

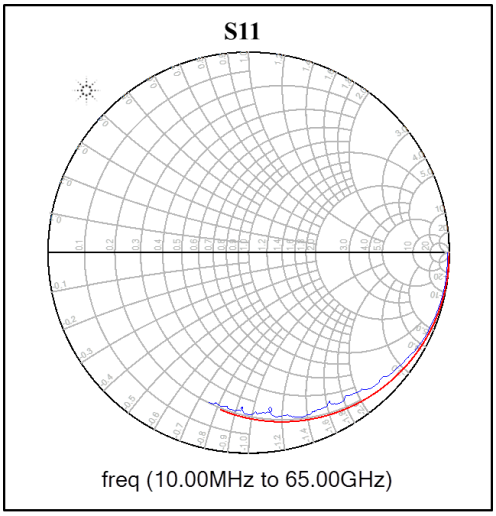


Figure 7.3.4a – Smith plot of S_{11}

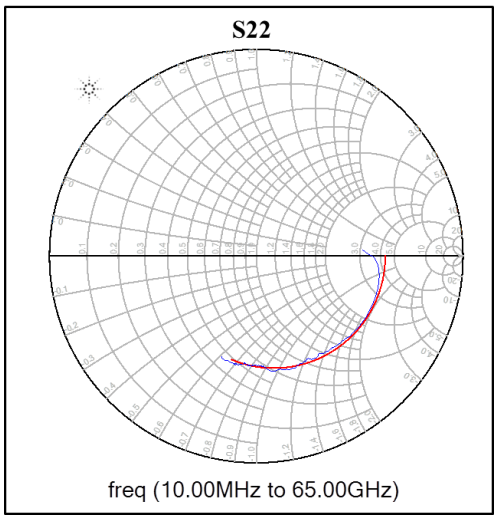


Figure 7.3.4b – Smith plot of S_{22}

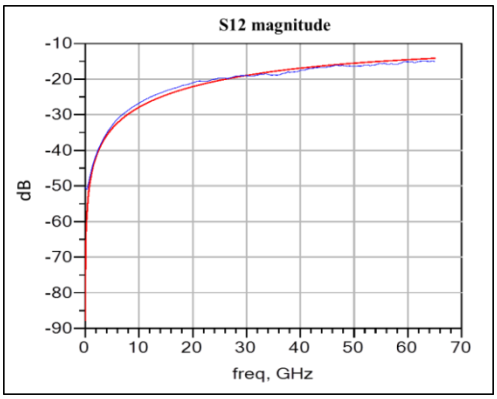


Figure 7.3.4c – S_{12} magnitude

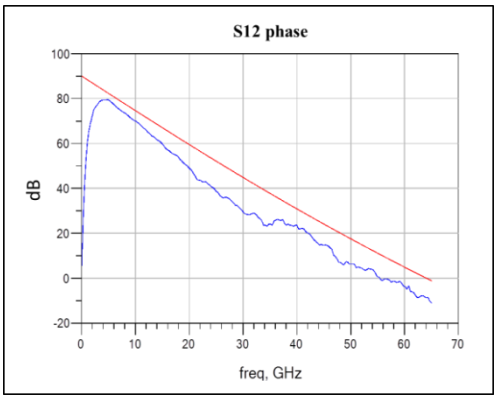


Figure 7.3.4d – S_{12} phase

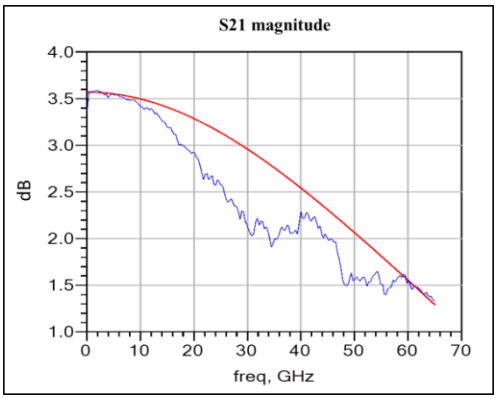


Figure 7.3.4e – S_{21} magnitude

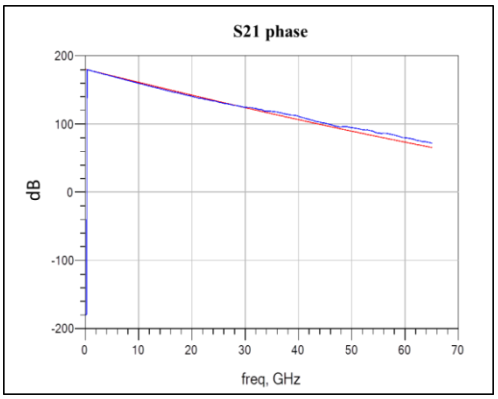


Figure 7.3.4f – S_{21} phase

Figure 7.3.4 – Measured (blue) and simulated (red) S-parameters

The de-embedded equivalent circuit elements determined from the simulation model are presented in **Figure 7.3.5**.

Parameter	Value	Parameter	Value
C_{gs}	15.6 fF	R_i	2.3 Ω
C_{gd}	7.3 fF	C_{gsp}	0.4 fF
C_{ds}	16.5 fF	C_{gdp}	0.1 fF
g_m	30.1 mS	C_{dsp}	0.3 fF
R_{ds}	133 Ω	L_g	1.0 pH
R_d	12.8 Ω	L_s	1.5 pH
R_s	13.9 Ω	L_d	0.2 pH
R_g	8.6 Ω		

Figure 7.3.5 – Equivalent circuit elements for a $2\times15\,\mu m$ device

The cutoff frequency, f_T, defined as the frequency at which short circuit current gain falls to unity, was extracted by extrapolating the H_{21} parameter to its intercept with the frequency axis. The maximum frequency of oscillation, f_{max}, is defined as the frequency at which the maximum available gain falls into unity, and can be extracted in similar way. As shown in **Figure 7.3.6** and **Figure 7.3.7**, 183GHz and 156GHz for f_T and f_{max} respectively for $2\times15\,\mu m$ device were extracted from H_{21} and maximum available gain, which were generated by the de-embedded equivalent circuit model.

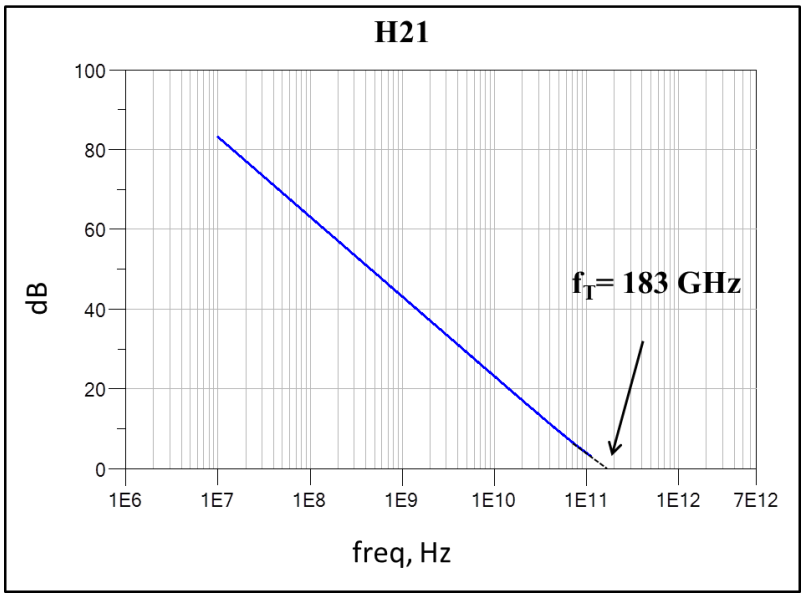


Figure 7.3.6 – H_{21} plot for 2 ×15 µm device

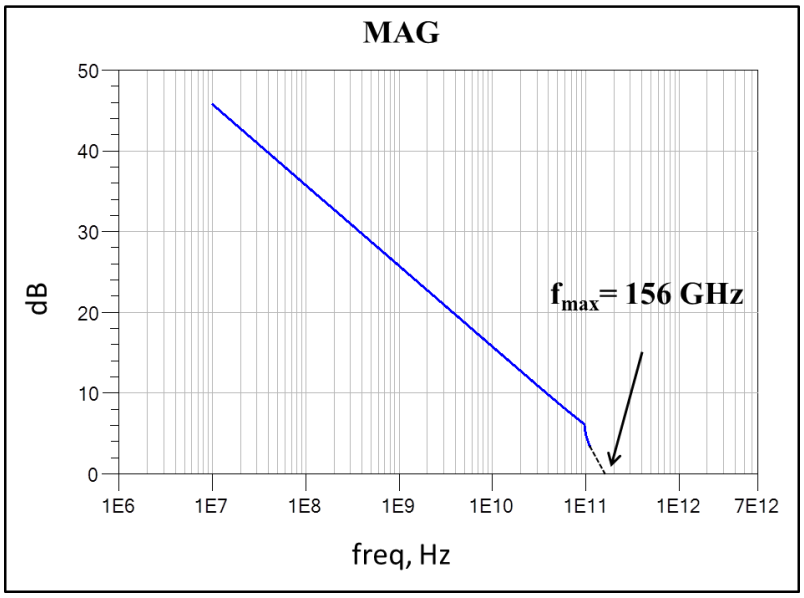


Figure 7.3.7 –Maximum available gain (MAG) plot for 2 ×15 µm device

7.4 Discussion

From **Figure 7.3.5**, the total gate capacitance C_g combining C_{gs} and C_{gd} is 22.9 fF in total. According to **Eqn 2.5.6**, however, the calculated gate capacitance C_g is 6 fF. The increase gate capacitance might result from the fact that the effective gate length is larger than the physical gate length (60 nm footprint) used in the calculation using **Eqn 2.5.6**. As described previously, the gate is formed on the barrier layer in the recess region which is larger than the gate footprint. Therefore, the barrier layer is exposed on both sides of the gate and surface states will be present on this exposed surface. The surface states cause charge trapped in the regions adjacent to the gate, which can be modulated by the fringing fields of the gate and causes the extension of the gate region. The variable charge present at the surface will influence the channel carrier concentration, resulting in an increased effective gate length [7.3]. The increased gate capacitance may also result from the capacitance from the head of the T-gate to the channel.

The intrinsic transconductance is 30.1 mS from **Figure 7.3.5**. According to **Eqn 2.4.4**, the electron velocity in the channel can be derived and is 3.1×10^7 cm/s, which is the typical value for an $In_{0.7}Ga_{0.3}As$ HEMT verified by [7.4]. This suggests velocity overshoot is occurring in the device channel.

The extrinsic transconductance can be extracted based on **Eqn 2.4.6** and 13.9 Ω source resistance from **Figure 7.3.5**. The calculated normalised extrinsic transconductance is 700 mS/mm, which is larger than 650 mS/mm determined by DC evaluation as shown in **Figure 7.3.3**. The carrier concentration of the channel is 2.4×10^{12} /cm^2, information supplied by the University of Manchester. According to **Eqn 2.4.1** and the electron velocity derived above, the channel current from source to drain is expected as 1190 mA/mm, and larger than the characterised I_{ds} presented in **Figure 7.3.1**. The reason for the decrease of extrinsic transconductance and the source-drain current compared to the expected values might be related to the recess region. The ideal size of the recess region on each side of the gate is

usually half of the gate length, which is 30 nm in this case. However, the actual recess etch size is 130 nm in total, i.e. 35 nm on each side of the gate. The wider recess region will lead to a larger source resistance, which results in a reduction of the transconductance. In addition, it is more possible for larger exposed barrier surface to get damaged. The damage surface might impact the carriers in the channel and influence the surface potential, which might contribute to the decrease of the source-drain current.

The source resistance comprises the ohmic contact resistance R_1, the resistance in the cap region R_2, and the resistance in the recess region R_3, as shown in **Figure 7.4.1**.

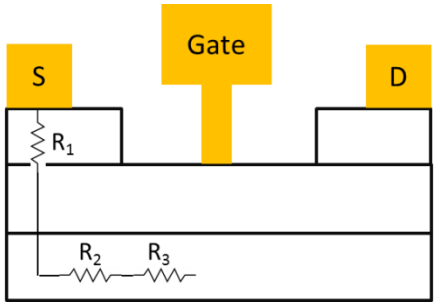


Figure 7.4.1 – Illustration of source resistance: R_1, R_2, R_3

From the data provided by the University of Manchester, the ohmic contact resistance R_c is 0.053 Ω.mm, and the sheet resistance R_{sh} is 80 Ω/□. As a consequence, R_1 = 1.77 Ω, R_2 = 2.67 Ω. The source resistance is much larger than the sum of R_1 and R_2, considering the values extracted from the RF model. Therefore, the resistance in the recess region may contribute significantly to the total source resistance and likely play an important role in degrading the device performance.

In addition, the gate-channel separation (30 nm) is rather large for a 60 nm gate device (1/5 L_g is ideal [7.5]) and there may be parallel conduction in the barrier layer, both of which might contribute to the degradation of the device performance. Although the f_T of this 60 nm Au-based T-gate HEMT could be improved, it still provides a reasonable benchmark for comparison to a silicon compatible Cu-based T-gate HEMT device.

7.5 Comparison between conventional Au-based T-gate and silicon compatible Cu-based T-gate

A comparison of the gold-based and copper-based T-gates presented above and in **Chapter 6** taking into consideration both process technologies and electrical performance, is presented in this section.

Firstly in aspect of process technologies, as discussed previously, copper-based T-gate fabrication processes can be incorporated into silicon foundries using compatible materials and processing approaches.

In addition, a copper-based T-gate should result in improved HEMT device performance as copper has a lower resistivity than gold and gate resistance strongly impacts the maximum frequency of oscillation f_{max} of HEMT. In **Section 7.3**, a de-embedded equivalent circuit model of a $2\times15\,\mu m$ HEMT with 60 nm gold-based T-gate has been constructed and the de-embedded equivalent circuit elements used in this simulation model were extracted. To compare with a copper-based T-gate, the gate resistance (R_g) of 8.6 Ω in the model shown in **Figure 7.3.5** will be replaced by the gate resistance of the copper-based T-gate, which can be deduced from normalised DC resistance presented in **Section 6.2.4**, to observe the change of f_{max}.

When a HEMT is operated at high frequencies, the gate resistance of the T-gate is one-third of the DC gate resistance due to the distributed R-C nature of the structure [7.6]. Therefore, the RF gate resistance of the copper T-gate described in **Section 6.2.4** in a $2\times15\,\mu m$ HEMT would be 0.11 Ω. The f_{max} extracted respectively from the de-embedded equivalent circuit models of gold-based T-gate HEMT and copper-based T-gate HEMT are presented in **Figure 7.5.1**.

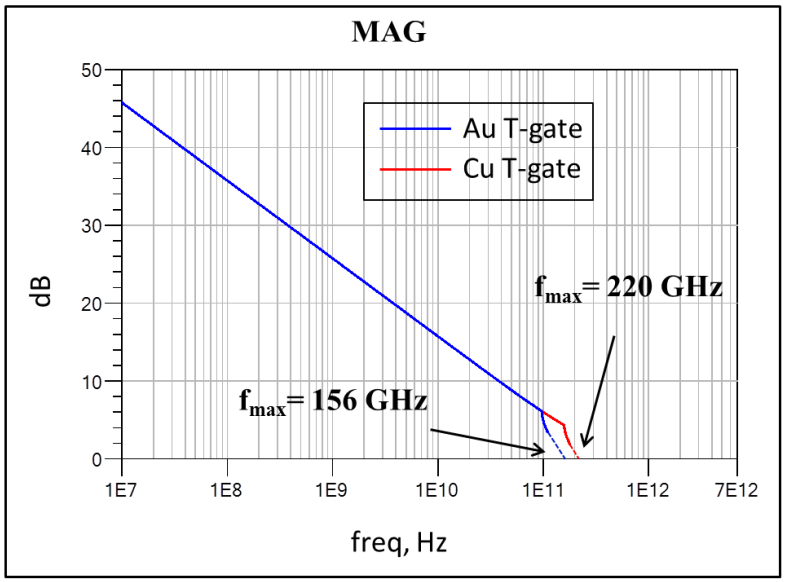


Figure 7.5.1 – f_{max} extracted from the de-embedded equivalent circuit models of gold T-gate HEMT (blue) and copper T-gate HEMT (red)

As shown in **Figure 7.5.1**, the f_{max} extracted from the de-embedded equivalent circuit model including the copper-based T-gate is predicted to be 220 GHz, compared to 156 GHz for the gold-based T-gate as expected and resulting from the lower resistivity of copper.

The copper T-gate used in the comparison mentioned above is with the dimensions of 60 nm molybdenum foot and 1.2 μm copper head. The micron-scale T-gate head may lead to larger parasitic capacitance, which will degrade device performance. In HEMT fabrication, the dimensions of the T-gate head can be decreased by reducing the copper electroplating time.

7.6 Summary

This chapter has described the optimised fabrication of a 60 nm Au-based T-gate InP HEMT, including:

- Establish acceptable 60 nm T-gate resist profile on planar GaAs substrates using the Vistec VB6 electron beam lithography tool by choosing appropriate resist layers and running tests of dose values variation in electron beam lithography technology.
- Transfer the optimised stable process of realising 60 nm T-gate profile from planar GaAs substrates to real HEMT material structure with ohmic contacts by modifying the spinning speed of the first resist layer.

In addition, DC and RF characterisation of the devices are also included in this chapter. The output and transfer characteristics of the device were established from DC characterisation. Maximum drain current of 800 mA/mm and peak transconductance of 650 mS/mm are obtained. RF measurement of the device was conducted with bias of -1.0V on the gate terminal and 1.0V on the drain terminal, the condition of the maximum transconductance. Following RF characterisation, an equivalent circuit model was constructed and de-embedded equivalent circuit parameters were extracted, yielding a cutoff frequency of 183GHz and maximum oscillation frequency of 156GHz.

Further, in the comparison between the silicon compatible copper-based T-gate introduced in **Chapter 6** and the gold-based T-gate fabricated by the conventional process presented in this chapter, an increase in the f_{max} of the copper-based T-gate HEMT is predicted.

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Chapter 8

Conclusions and Future work

A suitably engineered III-V High Electron Mobility Transistor (HEMT) is the best low noise high frequency transistor available and as a result has been utilised in various applications such as imaging, sensing and wireless communication [8.1-8.4]. The typical fabrication processes for III-V compound semiconductor devices include gold based metallisation and lift off process, which are not compatible with mass production silicon based manufacturing, which will always be the mainstream approach to low cost, high volume semiconductor component production. Therefore, this research work aims to develop silicon compatible process for III-V HEMT realisation, without compromising device performance.

In this thesis, progress towards this objective has been presented and is summarised as follows:

- A silicon compatible process to fabricate Cu-based T-gate of HEMT has been developed, including copper electroplating process for T-gate head formation [8.5] and low damage inductively coupled plasma molybdenum etching process for T-gate foot realisation [8.6]. The normalised DC resistance of a T-gate with 60 nm molybdenum foot and 1.2 μm copper head is 42 Ω/mm. Based on an equivalent circuit model prediction, it is anticipated that the maximum frequency of oscillation f_{max} of a HEMT with the copper-based T-gate would outperform that of an identical device with a gold-based T-gate. In addition, this silicon compatible copper-based T-gate fabrication process can be integrated into a full process flow for HEMT realisation. A gate-first approach utilising non-annealed ohmic contacts which have been demonstrated is described.

- The fabrication and characterisation of a 60 nm Au-based T-gate InP HEMT realised by conventional III-V processes was achieved. This established a baseline in terms of fabrication techniques and device performance, which can be compared with those of a HEMT fabricated by silicon compatible processes.

Some potential work could be done in future including:

- Further improvement of the properties of the copper head of the T-gate by adjusting electrolyte concentration and other electroplating parameters such as plating potential.
- To realise a complete HEMT device with the silicon compatible copper T-gate using the gate-first HEMT fabrication process flow described in **Chapter 6** and presented in **Appendix I**.
- To compare the performance of a Cu-based T-gate HEMT fabricated by the silicon compatible process and Au-based T-gate HEMT realised by conventional process.

References

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Appendix I

Gate-first Cu-based T-gate HEMT process flow

1. **Markers**

Clean substrate –5min ultrasonic Acetone + 5min ultrasonic IPA

Spin resist – 4% PMMA 2010 5k rpm 60s, 2 min 137℃ hotplate bake. 2.5% PMMA 2041 5k rpm 60s, 2 min 137℃ hotplate bake

Exposure – VB6 e-beam lithography. Penrose cell marker: dose 800 μC/cm^2, 1nA beam, VRU4; Global marker: dose 400 μC/cm^2, 64nA beam, VRU20

Develop – 30s 2.5:1 IPA: MIBK at 23℃, IPA rinse

Ash – 40W O_2 30s

Metallise – 30s 4:1 H_2O: HCl de-oxidise, 30s water rinse, 10nm Ti/70nm Au evaporation

Lift off – 2hr 55℃ acetone, pipette clean, IPA rinse

2. **Mesa**

Clean substrate – 5min Acetone rinse + 5min IPA rinse

Spin resist – 12% PMMA 2010 5k rpm 60s, 1hr 180℃ oven bake

Exposure – VB6 e-beam lithography. Dose 300 μC/cm^2, 64nA beam, VRU20

Develop – 60s 2:1 IPA: MIBK at 23℃, IPA rinse

Ash – 40W O_2 60s

Orthophosphoric etch – 30s 4:1 H_2O:HCl de-oxidise, 30s water rinse, 1:1:100 H_3PO_4: H_2O_2: H_2O 140s at room temperature, water rinse

Resist removal - 2hr 55℃ acetone, IPA rinse

3. **Recess etch**

Clean substrate – 5min Acetone rinse + 5min IPA rinse

Spin resist – 2.5% PMMA 2041 5000 rpm 60s, 2 min 137℃ hotplate bake.

Exposure – VB6 e-beam lithography. Dose 320 μC/cm^2, 1nA beam, VRU10

Develop – 60s 2:1 IPA: MIBK at 23℃, IPA rinse

Ash – 40W O_2 60s

Postbake – 2 min 90℃ oven bake

Wet etch – 30s 4:1 H_2O: HCl de-oxidise, 30s water rinse. Succinic etch (Succinic acid/hydrogen peroxide pH=5.5) 60s, Orthophosphoric etch (1:1:100 H_3PO_4: H_2O_2: H_2O) 7s, Succinic etch (Succinic acid/hydrogen peroxide pH=5.5) 10s, water rinse

Resist removal - 2hr 55℃ acetone, IPA rinse

4. **T-gate foot**

Clean substrate – 5min Acetone rinse + 5min IPA rinse

Metallise – 100nm Mo/2nm Ti, water rinse 10s, 10min 140℃ hotplate bake

Spin resist – 1:3 HSQ: MIBK 1k rpm 60s, 2 min 90℃ hotplate bake

Exposure – VB6 e-beam lithography. Gate foot: dose 4000 μC/cm^2, 1nA beam, VRU2; Interconnections: dose 350 μC/cm^2, 64nA beam, VRU20

Develop – 60s 1:3 25% TMAH: H_2O at 23℃, 30s DI water, 30s DI water, 15s IPA

Postbake – 2min 90℃ hotplate bake

Dry etch – STS-ICP etching: 15 sccm/25 sccm SF_6/ C_4F_8, platen power 2W, coil power 600W, 5 mTorr, 20% over-etch time

Resist removal – 10s 50ml 1/10 HF: 200ml H_2O

5. T-gate head

Spin resist – 12% PMMA 2010 5k rpm 60s, 1hr 180℃ oven bake

Etch back – "T-gate" tool, oxygen RIE, 50 sccm O_2, 25W, 100 mTorr, 70nm PMMA left

Cu electroplating – 0.25V, 5min

Interconnections removal – STS-ICP etching

6. Ohmic Contacts

Spin resist – 4% PMMA 2010 5k rpm 60s, 2 min 137℃ hotplate bake. 2.5% PMMA 2041 5k rpm 60s, 2 min 137℃ hotplate bake

Exposure – VB6 e-beam lithography. Dose 400 μC/cm^2, 64nA beam, VRU20

Develop – 30s 2.5:1 IPA: MIBK at 23℃, IPA rinse

Ash – 40W O_2 30s

Metallise – 30s 4:1 H_2O: HCl de-oxidise, 30s water rinse, 100nm Au evaporation

Lift off – 2hr 55℃ acetone, pipette clean, IPA rinse

7. Bondpads

Spin resist – 15% PMMA 2010 3k rpm 60s, 2 min 137℃ hotplate bake. 4% PMMA 2041 5k rpm 60s, 2 min 137℃ hotplate bake

Exposure – VB6 e-beam lithography. Dose 305 μC/cm^2, 64nA beam, VRU40

Develop – 60s 1:1 IPA: MIBK at 23℃, IPA rinse

Ash – 40W O_2 60s

Metallise – 30s 4:1 H_2O:HCl de-oxidise, 30s water rinse, Ar etch 10s, 50nm NICr/1200nm Au evaporation

Lift off – 2hr 55℃ acetone, pipette clean, IPA rinse

Appendix II

60 nm Au-based T-gate HEMT process flow

The "Mesa" and "Ohmic Contacts" were fabricated by the University of Manchester, the "Gate" and "Bondpads" were fabricated in this work at University of Glasgow.

1. **Mesa**

   Clean substrate – 5min ultrasonic 1165 + 5min ultrasonic Acetone + 5min ultrasonic IPA

   Prebake – 1 min hotplate 115℃ bake

   Spin resist – Photoresist S1805 4k rpm 30s. 1 min hotplate 115℃ bake

   Exposure – MA4 photolithography expose 20s

   Develop – MIF319 60s. Water rinse

   Postbake – 30min oven 120℃ bake

   Orthophosphoric etch – 3:1:50 H_3PO_4: H_2O_2: H_2O 60s at room temperature

   Sidewall etch – Succinic acid powder 10g, H_2O 50ml, Ammonia (~10 ml to pH of 5.5), H_2O_2 5 ml, 5 min at room temperature

2. **Ohmic Contacts**

   Clean substrate – 5min ultrasonic Acetone + 5min ultrasonic IPA

   Prebake – 1 min hotplate 100℃ bake

   Spin resist – Photoresist AZnLOF2070 3k rpm 30s. 1 min hotplate 110℃ bake

   Exposure – MA4 photolithography expose 5.5s

   Post exposure bake – 1 min hotplate 110℃ bake

   Develop – MIF326 60s. Water rinse

   Metallise – O_2 plasma etch 20s, 1:1 HCl:H_2O de-oxidise 30s, 50nm AuGe/100nm Au evaporation

   Lift off – 30 min 85℃ 1165

   Anneal – 90s 280℃

3. **Gates**

   Clean substrate – 5min Acetone rinse + 5min IPA rinse

   Spin resist – 2.5% PMMA 2041 3900 rpm 60s, 2hr 180^{o}C oven bake. 4:1 LOR 10A 5k rpm 60s, 15 min 180℃ oven bake. 66% UVIII 3500 rpm 60s, 60s 120℃ hotplate bake

   Exposure – VB6 e-beam lithography. Gate foot: dose 1691 μC/cm^2, 1nA beam, VRU5; Gate head: dose 127 μC/cm^2, 4nA beam, VRU22.

   Develop – CD26 60s at room temperature, water rinse 180s; o-xylene 90s at 23℃, water rinse 60s

   Ash – 40W O_2 30s

   Recess etch – Succinic acid/hydrogen peroxide pH=5.5 45s

   Metallise – 30s 4:1 H_2O:HCl de-oxidise, 30s water rinse, 15nm Ti/15nm Pt/160nm Au evaporation

Lift off – 2hr 55℃ acetone, pipette clean, IPA rinse

4. <u>Bondpads</u>

Clean substrate – 5min Acetone rinse + 5min IPA rinse

Spin resist – 15% PMMA 2010 3k rpm 60s, 2 min 137℃ hotplate bake. 4% PMMA 2041 5k rpm 60s, 2 min 137℃ hotplate bake

Exposure – VB6 e-beam lithography. Dose 305 $\mu C/cm^2$, 64nA beam, VRU40

Develop – 60s 1:1 IPA:MIBK at 23℃, IPA rinse

Ash – 40W O_2 60s

Metallise – 30s 4:1 H_2O:HCl de-oxidise, 30s water rinse, 50nm NICr/1200nm Au evaporation

Lift off – 2hr 55℃ acetone, pipette clean, IPA rinse