UNIVERSITY OF GLASGOW

Advanced Gallium Nitride Technology for Microwave Power Amplifiers

by

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Abstract

Gallium nitride (GaN) based technology has been heavily researched over the past two decades due to its ability to deliver higher powers and higher frequencies that are demanded by the market for various applications. One of GaN's main advantages lies in its ability to form heterojunctions to wider bandgap materials such as Aluminium Gallium Nitride (AlGaN) and Aluminium Nitride (AlN). The heterostructure results in the formation of the so called 2 dimensional electron gas (2DEG), which exhibits high electron densities of up to 6x10^{13} cm^{-2} and high electron mobilities of up to 2000 cm^2/V·s that enable the devices to support high current densities. Furthermore, it supports very high breakdown fields of 3.3 MV/cm due to its wide bandgap of 3.4 eV. The main objective of this work was to further advance the transistor technology using simple, cost effective and reliable techniques.

The AlN/GaN material system exhibits higher sheet carrier concentrations compared to the conventional ternary AlGaN barrier, but introduces additional challenges due to its reduced thickness of 2-6 nm compared to 18-30 nm of AlGaN. The additional challenges of the thin AlN binary barrier include strain relaxation, high gate leakage currents and high Ohmic contact resistances due to its high bandgap of 6.2 eV. In this work, a thin (5 nm) in-situ SiN_x passivation layer was employed to reduce the strain relaxation, reduce gate leakage currents and improve Ohmic contacts resistances. The optimised Ohmic contact annealing condition resulted in an Ohmic contact resistance of 0.4 Ω·mm and a sheet resistance of 300 Ω/□. This result opens the door for realising microwave power amplifier circuits using the AlN/GaN material system for the first time.

The conventional dry etching techniques used to achieve device isolation for GaN based transistor technologies results in a three dimensional device structure, the mesa structure. This leads to high leakage currents which impact the noise performance and breakdown voltages of the devices. A new approach to achieve device isolation that employs an oxygen plasma treatment was demonstrated in this project. It results in a planar device structure with devices exhibiting one order of magnitude less gate leakage currents compared to mesa isolated devices. The achieved leakage currents of 1 μA/mm are comparable to those which employed the more complex and expensive ion implantation technique.

As GaN growth and device processing reaches maturity levels, thermal performance of the devices becomes the main limitation to achieving higher powers and higher frequencies since increased device self heating has a negative impact on the device performance. In this project, novel thermal management techniques were developed and include the use of dry etching techniques to create thermal vias that are located within few microns of the heat source in the semiconductor channel. The vias are then filled with copper, a metal with high thermal conductivity, that is in contact with the substrate to efficiently

transport the heat from the channel into the SiC substrate. The thermally efficient fabricated devices could sustain a DC power density of 38 W/mm without degradation compared to standard devices that exhibit only 15 W/mm at 40 V.

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Patents

1. Patent on thermally efficient devices (under consideration).
2. Patent on device isolation (under consideration).

List of publications

1. A. Al-Khalidi, A. Khalid and E. Wasige, "AlN/GaN HEMT technology with in-situ SiN_x passivation," *IEEE PRIME Conference*, Glasgow, UK, July 2015.
2. A. Al-Khalidi, K. Gallacher, A. Khalid, D. Paul and E. Wasige, "0.25 Ω·mm Ohmic contacts to AlN/GaN HEMT structure with in-situ SiN passivation," *7th Space Agency - MOD Workshop on Wide Bandgap Semiconductors and Components*, ESA/ESTEC, Frascati, Italy, September 2014.
3. A. Al-Khalidi, K. Gallacher, A. Khalid, D. Paul and E. Wasige, "Effect of annealing time and temperature on Ohmic contacts to AlN/GaN HEMT structure with in-situ SiN passivation," *UK Nitrides Consortium,* Sheffield, July 2014.
4. A. Al-Khalidi, A. Khalid and E. Wasige "Comparison of AlGaN/GaN HEMTs on silicon, sapphire and SiC substrates - a thermal perspective," *Compound Semiconductor Week*, Montpellier, France, May 2014.
5. A. Al-Khalidi, S. Taking and E. Wasige, "AlN/GaN HEMTs with SiN passivation and recessed Ohmics," *6th Space Agency - MOD Workshop on Wide Bandgap Semiconductors and Components*, ESA/ESTEC, Noordwijk, the Netherlands, October 2012.
6. A. Al-Khalidi, D. Macfarlane and E. Wasige, "Self-aligned recessed Ohmic contacts for GaN-based High Electron Mobility Transistors (HEMTs)," *UK Nitrides Consortium,* Sheffield, July 2012.
7. R. Brown, D. Macfarlane, A. Al-Khalidi, X. Li, G. Ternent, H. Zhou, I. Thayne and E. Wasige, "A sub-critical barrier thickness normally-off AlGaN/GaN MOS-HEMT," *IEEE Electron Device letters*, vol. 35, pp. 906-908, September 2014.

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13. R. Brown, A. Al-Khalidi, D. Macfarlane, S. Taking, G. Ternent, I. Thayne and E. Wasige, "A normally-off AlGaN/GaN HEMT technology," *UK Nitrides Consortium*, Sheffield, July 2013.

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Symbols

$2DEG$	2 Dimensional Electron Gas
$2DHG$	2 Dimensional Hole Gas
AFM	Atomic Force Microscopy
Ar	Argon
Al	Aluminium
Au	Gold
$AlGaN$	Aluminium Gallium Nitride
AlN	Aluminium Nitride
BCl_3	Boron tri-chloride
Cu	Copper
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposition
Cl_2	Chlorine
$CTLM$	Circular Transmission Line Model
CW	Continuous Wave
DC	Direct Current
DI	De-Ionised
E_C	Conduction band energy
E_f	Fermi level energy
E_g	Bandgap energy
f_{max}	Maximum frequency of operation
f_T	Unity current gain cut-off frequency
Ga	Gallium
GaN	Gallium Nitride
$GaAs$	Gallium Arsenide

g_m	Transconductance
HF	Hydrofluoric acid
H_2O	Water
$HVPE$	Hydride Vapour Phase Epitaxy
$HEMT$	High Electron Mobility Transistor
IV	Current - Voltage
ICP	Inductive Coupled Plasma
InP	Indium Phosphide
$InAlN$	Indium Aluminium Nitride
$JWNC$	James Watt Nanofabrication Centre
k	Thermal conductivity
$LTLM$	Linear Transmission Line Model
L_{GD}	Gate - drain distance
L_{GS}	Gate - source distance
L_{SD}	Source - drain distance
L_T	Transfer length
LOR	Lift-off resist
LED	Light Emitting Diode
$MMIC$	Monolithic Microwave Integrated Circuit
MBE	Molecular Beam Epitaxy
$MOCVD$	Metal Organic Chemical Vapour Deposition
N	Nitrogen
n_s	Sheet carrier concentration
Ni	Nickel
P_{PE}	Piezoelectric polarization
P_{SP}	Spontaneous polarization
$PECVD$	Plasma Enhanced Chemical Vapor Deposition
q	Electron charge
RO	Reverse Osmosis
RIE	Reactive Ion Etching
R_c	Ohmic contact resistance
R_{sh}	Sheet resistance
R_{ch}	Channel resistance

RF	Radio Frequency
SiC	Silicon Carbide
$SiCl_4$	Silicon tetrachloride
Si	Silicon
SiN_x	Silicon Nitride
TiN	Titanium Nitride
Ti	Titanium
TBR	Thermal Boundary Resistance
TEM	Transmission electron microscope
V_{BR}	Breakdown voltage
V_{DS}	Drain - source voltage
v_{eff}	Effective velocity
v_{sat}	Saturated electron Velocity
V_{GS}	Gate - Source voltage
V_p	Pinch-off voltage
V_T	Threshold voltage
W_g	Gate width
μ_n	Electron mobility
ε	Absolute permittivity
ϵ_o	Vacuum permittivity
ε_r	Relative permittivity
ϕ_b	Schottky barrier
σ	Polarisation charge

Dedicated to my parents: Dr. Koutaiba Al-Khalidi and Ibtehal Al-Hachim to whom I shall always be indebted...

CHAPTER 1

Introduction

1.1 Overview

Since the invention of the first electronic transistor in 1947, the demand for higher powers and higher frequencies has always increased. An alternative technology is needed to push the boundary beyond what is achievable with the existing silicon technology. The interest for III-V technologies such as Indium Phosphide (InP) [1], Gallium Arsenide (GaAs) [2] and Gallium Nitride (GaN) [3] based High Electron Mobility Transistors (HEMTs) has emerged as they exhibit higher electron mobilities which translates into higher operational frequencies. The wider bandgap of III-Vs enable higher operational voltages which translates into higher output powers. These technologies can therefore extend the transistor performance beyond what is possible with the current silicon technology. Among the III-V materials, GaN has been the favourite for high power and high frequency solid state applications due to its wider band gap (3.4 eV) compared to InP (1.35 eV) and GaAs (1.43 eV), and hence has higher breakdown voltages enabling it to deliver higher output powers. For example, GaN offers up to five times higher power density than GaAs [4, 5].

GaN technology has come a long way since the fabrication of the first GaN transistor in 1993 [6] in terms of growth maturity, design and fabrication techniques, allowing it to be adopted and implemented in many different applications. These include the automotive industry [7], photovoltaic power converters [8], DC-DC converters [9, 10], high power line converters, power switching [11], space applications [12], high efficiency LED lighting [13] and high power high frequency applications required for defence [14, 15] and wireless telecommunication systems [16]. High temperature operation of up to 1000°C has been demonstrated on InAlN/GaN HEMTs [17] making them suitable for the oil industry

and aircraft engines [18]. The fundamental material properties of GaN, SiC, Diamond, silicon, GaAs and InP are listed in Table 1.1.

Property (Units)	**GaN**	**SiC**	**Diamond**	**Si**	**GaAs**	**InP**
Relative permittivity, ϵ_r	9	10.1	5.5	11.8	12.8	12.8
Band gap energy, E_g (eV)	3.44	3.26	5.45	1.12	1.43	1.35
Breakdown field, E_c (MV/cm)	3.3	3	10	0.3	0.4	0.5
2DEG density, n_s (x10^{13} cm^{-2})	1	-	-	-	0.2	0.2
Thermal conductivity, κ (W/m·K)	130	400	2200	150	50	70
Electron mobility, μ_n (cm^2/V·s)	900	700	4800	1500	8500	5400
Saturated electron velocity, V_{sat}(x10^7 cm/s)	2.5	2	2.7	1	1	1
Power density, (W/mm)	>30	10	-	0.2	0.5	-

TABLE 1.1: Material properties of conventional and wide-band gap semiconductors.

One of GaN's main advantages lies in its ability to form heterojunctions to wider band gap materials such as Aluminum Gallium Nitride (AlGaN) and Aluminium Nitride (AlN). In doing so, a 2 dimensional electron gas (2DEG) channel is formed which exhibits high electron densities (>10^{13}/cm^2) and high electron mobilities of up to 2000 cm^2/V·s. Although this is lower than the mobilities of GaAs and InP, it compensates through having a much higher 2DEG density of 10^{13} cm^{-2}, resulting in an overall lower sheet resistance. This makes it suitable for high power high frequency applications like radar and space applications. The higher electron mobilities exhibited by the 2DEG compared to bulk GaN comes from the faster carrier transport in low-dimensional system due to reduced scattering and density of states. GaN has a relatively high band gap energy of 3.4 eV and breakdown field of 3.3 MV/cm compared to silicon, GaAs and InP. This enables high voltage operation of the GaN HEMTs before breaking down, which makes it suitable for high voltage applications like photovoltaic power converters and high power line converters. The thermal conductivity determines how quickly the heat can be extracted from the semiconductor, and since GaN has a thermal conductivity of 130 W/mK, this gives it a big advantage over GaAs and InP which have a much lower thermal conductivity. The wide bandgap and high thermal conductivity of GaN makes it suitable for high temperature applications such as oil industry and aircraft engine applications. Figure 1.1 illustrates some of the applications of GaN technology mentioned above.

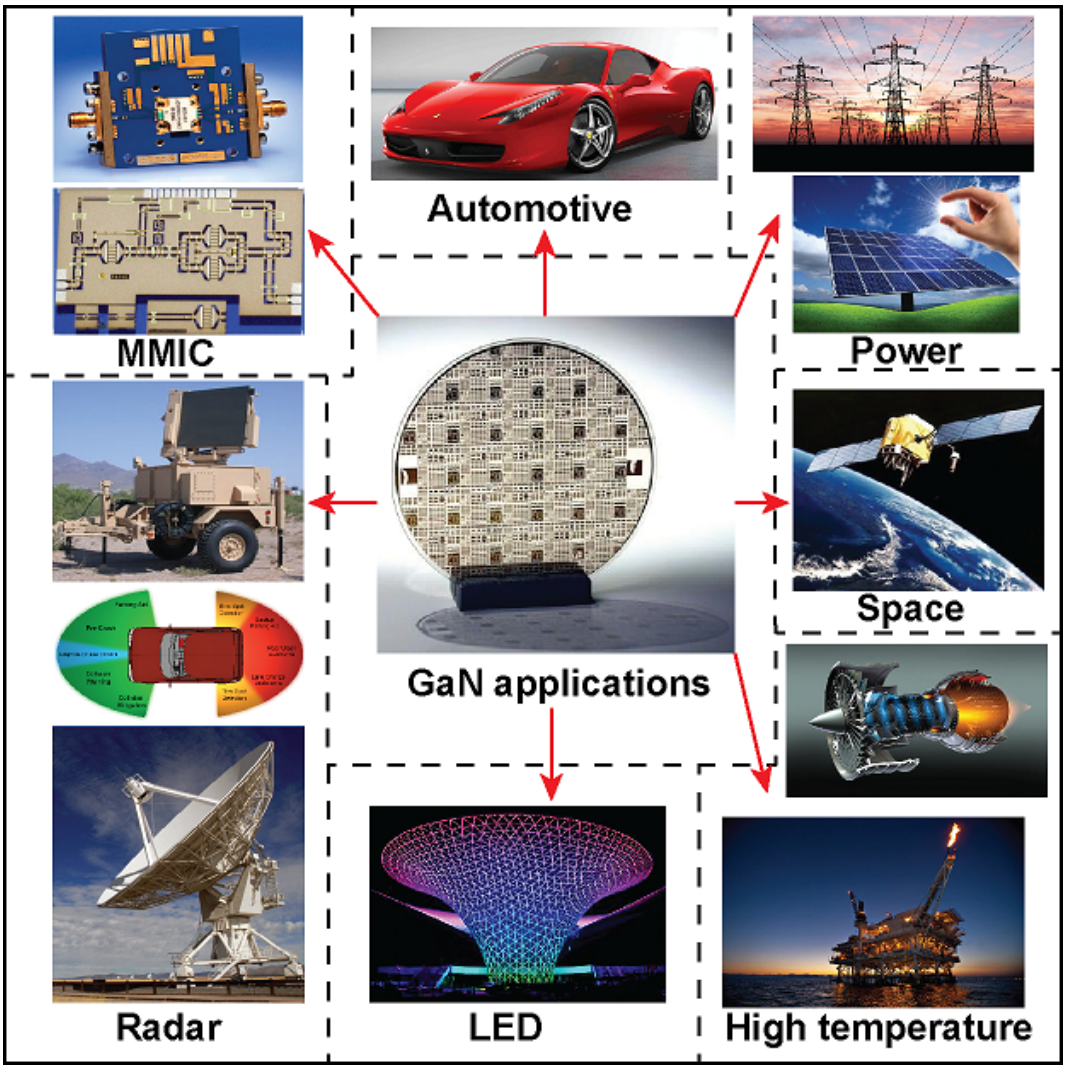

FIGURE 1.1: Applications of GaN technology.

1.2 Problem statement

Despite rapid progress over the last few years, GaN technology still requires significant improvements in various aspects. This section describes the challenges addressed by the work done in this project, which includes Ohmic contacts for the AlN/GaN material system, device isolation and thermal management of GaN-based HEMTs.

1.2.1 Ohmic contacts to AlN/GaN HEMT material system

AlN/GaN is a very interesting material system as it can potentially deliver at least double the output power that is delivered by the conventional AlGaN/GaN material system. State of the art DC and RF devices based on AlN/GaN [19, 20] have been demonstrated, with maximum current densities of up to 4 A/mm, transconductance of

1 S/mm and f_T/f_{max} of 342/518GHz using a 20 nm T-gate process [21], where f_T is the unity current gain frequency and f_{max} is the unity power gain frequency. However, there are several obstacles in realising such a technology. One is the Ohmic contacts, the other is material growth, and lastly surface sensitivity during processing. The thin AlN barrier is sensitive to processing solutions and causes the fabricated devices to suffer from high leakage currents if not protected during processing [22, 23]. For example, the AZ400K photo-resist developer was shown to etch the AlN barrier layer [24]. Therefore, protecting the AlN layer during processing is important. One way to achieve such protection is the use of an in-situ SiN_x passivation layer as will be described in chapter 4.

Ohmic contacts on the AlGaN/GaN material have been shown to exhibit a satisfactory contact resistance in the range of 0.2-0.5 Ω·mm. On AlN/GaN, however, the formation of low Ohmic contacts becomes more challenging as AlN has a band gap of 6.2 eV, which is higher than the band gap of $Al_{0.25}GaN_{0.75}$ of approximately 4 eV, and therefore devices exhibit contact resistance values in the range of 0.5-1 Ω·mm. Contact resistances under 0.2 Ω·mm are required for the performance of these devices to be competitive in terms of reaching the potential of high current densities and high output power. Low Ohmic contact resistance of 0.2 Ω·mm could be achieved by either lowering the barrier height or by easing tunneling through the barrier. Lowering the barrier height could be achieved by high temperature anneals, by highly doping the GaN cap layer with silicon [25], or using the Ohmic regrowth technique to regrow silicon rich GaN in the contact areas before depositing the Ohmic metal [26]. Easing tunneling through the barrier could be achieved by either starting with a thin barrier or thinning the barrier using dry etching [27]. The aforementioned techniques are either requiring regrowths or the contact resistance is still high.

In this project, the use of in-situ SiN_x passivation layer is proposed to protect the AlN surface during processing, reduce gate leakage current and reduce the Ohmic contact resistance, as will be described in chapter 4.

1.2.2 Device isolation for GaN-based HEMTs

Device isolation is required to electrically isolate devices from each other. The two common ways to isolate GaN based devices are mesa isolation and ion implantation. Mesa isolation is the most popular technique due to its low cost and availability in most research laboratories. Dry etch techniques are used to implement mesa isolation since GaN has strong ionic bonds, making it resistant to most acids and bases and therefore cannot be wet etched. The problem with dry etching is that it induces damage to the

AlGaN surface, making it conductive [28, 29], and results in the gate metal having a direct contact with the 2DEG channel. This results in increasing gate leakage currents by at least one order of magnitude (from the conventional 1 μA/mm to >10 μA/mm) due to the gate metal being in direct contact with the 2DEG channel. This leads to the reduction of breakdown voltages, and therefore a planar device structure is desirable to avoid the direct contact of the gate metal with the 2DEG channel. Ion implantation is one way to achieve a planar device structure and although it involves complex processing and high equipment cost, it is still used due to its advantages [30]. In one published example, devices isolated using ion implantation (planar devices) exhibited higher breakdown voltages of 650 V compared to devices isolated using mesa isolation (three dimensional devices) exhibiting breakdown voltages of 350 V [31]. The three dimensional structure was also shown to deteriorate the noise performance of GaN HEMTs under gate bias stress which severely affects low noise amplifier performance [32]. When compared to three dimensional devices, planar devices were demonstrated to exhibit better RF performance [33].

Due to the complexity of the ion implantation process and high cost of the equipment, in this project a new technique is proposed to realise device isolation using a planar process that is based on oxygen plasma treatment. The new technique will be described and discussed in chapter 5.

1.2.3 Thermal management on AlGaN/GaN HEMTs

As AlGaN/GaN technology has matured over the years, high power densities beyond 40 W/mm have been achieved. The highest reported RF power densities of GaN HEMTs to date are 41.4 W mm^{-1} at 4 GHz [34], 30.6 W mm^{-1} at 8 GHz [35], 13.7 W mm^{-1} at 30 GHz [36] and 10.5 W mm^{-1} at 40 GHz [37]. State of the art monolithic millimeter-wave integrated circuits (MMICs) have been demonstrated with powers of 58 W at X-band [38], 400 mW at 90 GHz [39], 1.7 W of output power at 91 GHz [40], 1 W across the 80-100 GHz band with a peak power of 2 W at 84 GHz [41], 5.2 W at 95 GHz [42], 5 W at 98 GHz [43] and 296 mW/mm at 180 GHz [44]. Despite the high power densities demonstrated, conventional devices are conservatively operated at power densities of 7 W/mm to keep the channel temperature below 200°C [45]. High power densities introduces the challenge of extracting the dissipated heat within the device, i.e. self heating. This needs to be addressed by introducing an integrated heat sink process to efficiently extract the excessive heat dissipated in the device and transport it in the most effective way to avoid degradation in performance that is usually caused by self heating [46]. This would enable the GaN technology to operate at much higher voltages and therefore, higher power densities than what is currently possible.

High power density GaN devices are usually realised on SiC substrates because of their high thermal conductivity. The limitation to efficient heat extraction in GaN HEMTs was identified by Kuball [47] to be caused by the thermal boundary resistance (TBR) between the GaN buffer layer and the SiC substrate. When GaN is grown on a foreign substrate, a nucleation layer is required to reduce the lattice mismatch between the GaN and the substrate and so, this layer cannot be omitted [48]. There are many approaches for heat removal from GaN devices. Those include the use of graphene [49], sputtered AlN [50] or nano-crystalline diamond [51] to extract the heat from the surface; back side processing to etch vias that are later filled with diamond, the removal of the SiC substrate and atomically bonding the GaN structure with a chemical vapour deposited (CVD) diamond substrate [52], optimising the growth of the nucleation layer to reduce the TBR [53, 54] and finally using microfluidic heat exchangers techniques to pump liquids into fins that are etched within the device to extract heat from the backside [55]. However, many of these techniques require complex processing and have not shown any significant improvement in power densities. A new, simple, reliable and effective thermal management technique is thus required to further advance the technology. Proposed herein an approach that is based on front side processing to remove the inactive GaN HEMT epi-layers from the top side and fill the vias with a high thermally conducting material to efficiently extract the heat from within the device. This technique will be described and discussed in chapter 6.

1.3 Research objectives

The ultimate goal of this project was to further advance the gallium nitride based transistor technology for microwave power amplifier applications. The project involved work on both AlGaN/GaN and AlN/GaN based material systems. Research objectives for the AlGaN/GaN based material system were as follows:

1. Introduce an innovative device isolation technique that simplifies the process flow, reduces the cost and lowers the gate leakage currents. The aim was to avoid using the conventional dry etching process that results in the gate metal being in direct contact with the 2DEG channel.

2. Fabricate devices using the new isolation technique and compare them to devices fabricated using the conventional isolation technique.

3. Evaluate and design new techniques to realise devices with integrated heat sinks that help improve device thermal performance and increase the output power by

enabling the devices to be operated at higher voltages without increasing the channel temperatures.

4. Develop the process flow of the integrated heat sinks, fabricate the devices using the new developed techniques and compare device performance between conventional devices and devices with integrated heat sinks.

The AlN/GaN material system exhibits superior properties compared to the conventional AlGaN/GaN material system. However there are still issues to be overcome including surface sensitivity, high Ohmic contact resistance and high gate leakage currents. The research objectives for the AlN/GaN material system were as follows:

1. Use a reliable material structure that employs a surface passivation layer to eliminate surface sensitivity and reduce gate leakage currents.
2. Optimise an Ohmic contact process on AlN/GaN material to reduce the contact resistance.
3. Use the optimised Ohmic contact process to fabricate devices and compare them to device performance on AlGaN/GaN material system.

1.4 Thesis structure

This thesis has seven chapters. Details of each chapter is as follows:

- **Chapter 1** (this chapter) gives an overview of GaN technology, highlighting its advantages over competing technologies such as silicon and GaAs. The different GaN applications are illustrated, and the recent advancements in GaN technology are mentioned. Finally the research problem statement is explained followed by a listing of the research objectives of this project.
- **Chapter 2** describes the basic GaN-based transistor structure and its principle of operation. The polarisation induced charges along with the band diagrams and the 2DEG formation are explained. The substrate choice and the role of each grown epi-layer and its effect on the device performance is also discussed. Finally, basic equations that characterise material and device performance are given.
- **Chapter 3** explains the standard fabrication techniques used in the cleanroom in making GaN HEMTs. The layout design is described first followed by device processing including photo and electron beam lithography, metallisation, wet and dry etching, high temperature annealing and dielectric deposition.

- **Chapter 4** describes the physics behind Ohmic contacts and the techniques for their characterisation using the transmission line method. It includes a literature review of Ohmic contacts on the GaN material system. Work on recessed Ohmic contacts is discussed, and the process of Ohmic contact fabrication and optimisation on the AlN/GaN material system using multi-temperature anneals is described and the achieved results presented. A comparison of device performance using the optimised Ohmic contacts on AlGaN/GaN and AlN/GaN HEMT material concludes the chapter.

- **Chapter 5** provides a literature review of conventional device isolation techniques and their limitations. The new device isolation technique developed in this project is described with experimental results presented and discussed.

- **Chapter 6** describes an experimental study on GaN technology from thermal perspective by evaluating device performance using three different substrates; silicon, sapphire and SiC. A literature review of different thermal management techniques is provided. The chapter then describes new approach for thermal management developed in this project, and concludes with a discussion of the achieved results.

- **Chapter 7** provides a summary of the work done and suggestions for future work.

CHAPTER 2

GaN HEMT Theory

2.1 Introduction

This chapter will give an overview of the physical properties of GaN based HEMTs. First, the polarisation induced charges in GaN will be explained. Second, the advantage of the different substrates available for GaN technology will be explained followed by the role of each epi-layer in the HEMT structure. Finally, the principle of operation of the devices will be given.

2.2 Polarisation in GaN HEMT

Group III-nitrides form a hexagonal structure called wurtzite when grown on sapphire, SiC or Si substrates. They exhibit significant polarisation effects especially at the interface, which make them unique when compared to other semiconductor technologies that are available in the market [56]. The structure is chemically stable and mechanically robust and therefore can withstand high temperatures. There are two types of polarisations; spontaneous and piezoelectric. Figure 2.1 illustrates the crystal structure of a Ga(Al)-face of an AlGaN/GaN structure and the vector polarisation induced charges in a strained AlGaN/GaN structure [57].

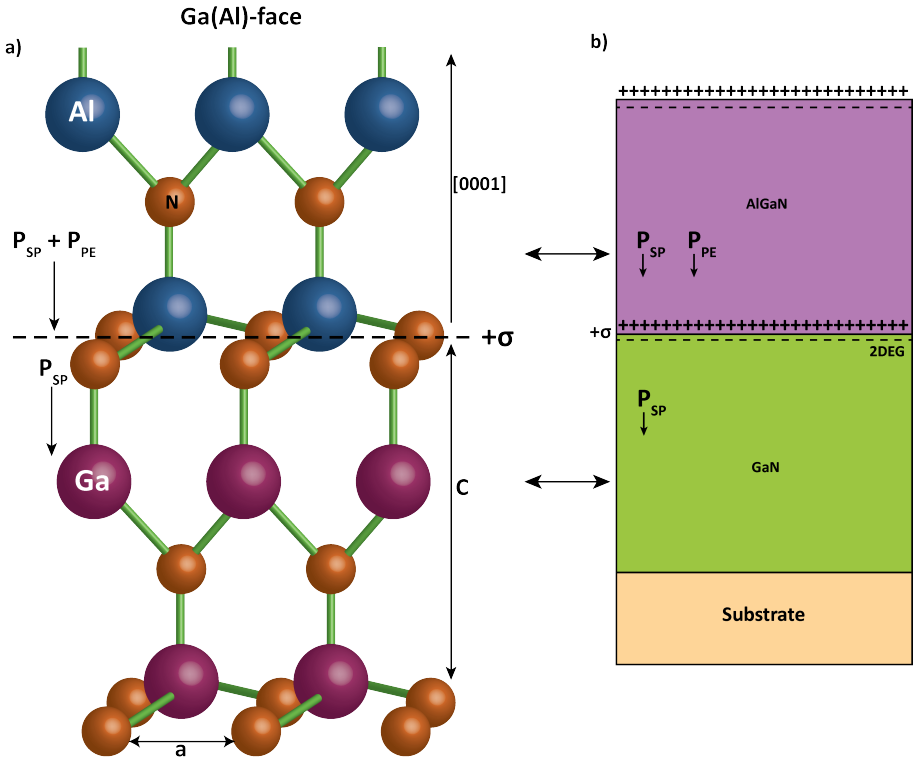

FIGURE 2.1: Illustration of a) Ga(Al)-face crystal structure and b) polarisation induced sheet charge density and direction of the spontaneous and piezoelectric polarisation in Ga-face strained AlGaN/GaN heterostructure.

2.2.1 Spontaneous polarisation

Spontaneous polarization occurs naturally in GaN when it is grown along the c-plane, which leads to strong electric fields of 3 MV/cm [57]. The spontaneous polarisation of an AlGaN/GaN and AlN/GaN structure can be calculated using the following equation [57]:

$$P_{SP,Al_xGa_{1-x}N/GaN}(x) = (-0.052 \cdot x - 0.029)Cm^{-2} \tag{2.1}$$

where P_{SP} is the spontaneous polarization and x is the aluminium mole fraction in the AlGaN layer. For a typical AlGaN layer that has a 25% Al content, $P_{SP}(0.25)$= -0.042 Cm^{-2}, while for the binary AlN layer which has 100% Al content $P_{SP}(1)$= -0.081 Cm^{-2}. This demonstrates that by increasing the Al content to 100% in the barrier, the spontaneous polarisation charge is almost doubled.

2.2.2 Piezoelectric polarisation

Piezoelectric polarization is a result of lattice mismatch between the barrier and GaN interface resulting in a compressive strain at the interface. By growing an AlGaN barrier on top of a GaN layer, an additional electric field of 2 MV/cm resulting from the introduced piezoelectric polarisation is added to the structure. This is mainly caused by the displacement of ions in the crystal lattice. When the lattice is strained, atoms will shift in the lattice which leads to generating an electric field that is dependent on the amount of strain; the higher the strain the higher the electric field. The piezoelectric polarisation gives GaN the ability to achieve high conductivity compared to other semiconductor materials.

2.2.3 Device engineering using polarisation charges

When an external electric field is absent, the total polarisation **P** of a GaN layer is the sum of the spontaneous P_{SP} and piezoelectric polarisation P_{PE}. In a conventional AlGaN/GaN HEMT, a 2DEG exhibit a sheet carrier concentration of $6x10^{12}$ cm^{-2} for aluminium content of 15%. The sheet carrier concentration can be increased to $2x10^{13}$ cm^{-2} when increasing the aluminium content to 31%. For the all binary AlN barrier (100% Al content) a maximum sheet carrier concentration of $6x10^{13}$ cm^{-2} can be achieved [57]. Therefore devices with an AlN barrier can deliver up to three times the output powers of conventional AlGaN/GaN HEMTs.

Figure 2.2 illustrates an AlGaN/GaN structure under three different conditions; relaxed AlGaN/GaN, tensile strained AlGaN on top of a relaxed GaN and a compressively strained GaN on top of a relaxed AlGaN. At an interface of a top/bottom layer structure (AlGaN/GaN or GaN/AlGaN), the polarisation can decrease or increase within a bilayer, causing a fixed polarisation charge density (σ). In the case where the polarisation induced charge density is positive ($+\sigma$) (Figure 2.2 (a) and (b)), free electrons will tend to compensate the polarisation induced charges resulting in the formation of a 2DEG within a quantum well at the AlGaN/GaN interface. In the case where the polarisation induced charge density is negative ($-\sigma$) (Figure 2.2c), holes will accumulate at the GaN/AlGaN interface to form a two dimensional hole gas (2DHG).

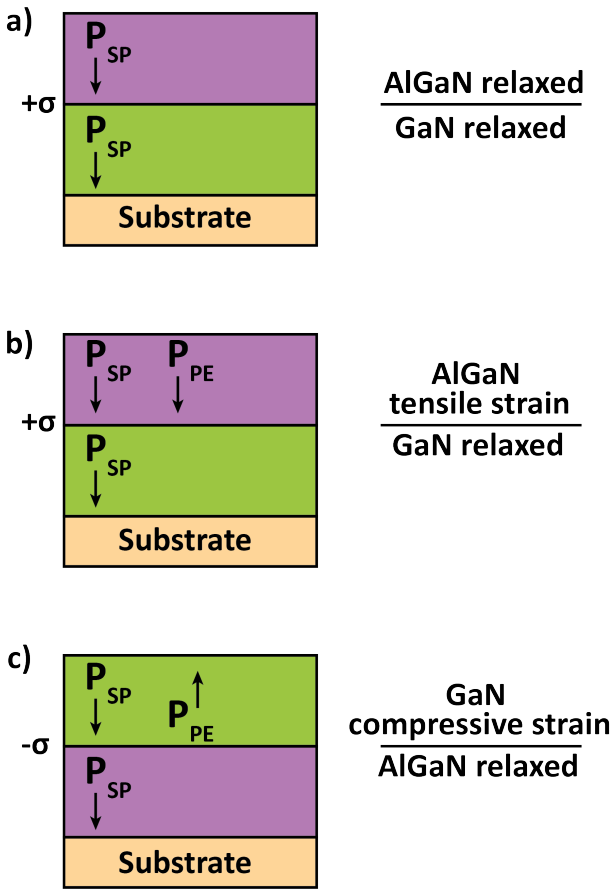

FIGURE 2.2: Polarisation charges a) relaxed AlGaN/GaN, b) tensile strained AlGaN on a relaxed GaN and c) compressively strained GaN on a relaxed AlGaN.

The polarisation charge, σ, in a structure can be calculated using:

$$\begin{aligned} \sigma &= P(bottom) - P(top) \\ &= [P_{SP}(bottom) + P_{PE}(bottom)] - [P_{SP}(top) + P_{PE}(top)] \end{aligned} \tag{2.2}$$

In the case of a conventional HEMT, a strained AlGaN layer is grown on a relaxed GaN as illustrated in Figure 2.2b and hence, σ becomes:

$$\sigma = P_{SP,GaN}(x) - [P_{SP,AlGaN}(x) + P_{PE,AlGaN}(x)] \tag{2.3}$$

The band gap difference between the AlGaN and GaN creates a large conduction band offset, ΔEc. A quantum well is formed at the conduction band offset. Figure 2.3 illustrates the band diagram of a conventional GaN HEMT. The 2DEG is highly conductive as it exhibits a high electron density, and the mobility increases from about 900 $cm^2/V{\cdot}s$ in unstrained GaN up to 2000 $cm^2/V{\cdot}s$ in the 2DEG region [58].

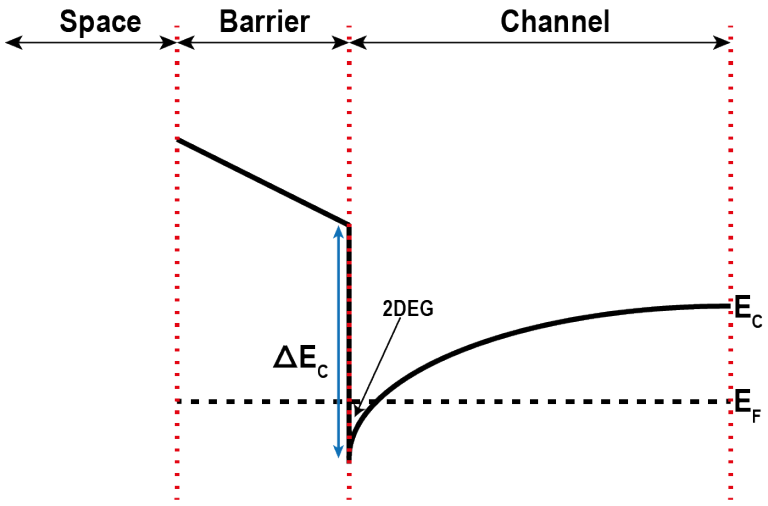

FIGURE 2.3: Band diagram of a GaN HEMT.

The maximum sheet carrier concentration (n_s) of the 2DEG channel can be calculated using [59]:

$$n_s(x) = \frac{\sigma(x)}{q} - \frac{\epsilon_0 \epsilon_r(x)}{dq^2}[q\phi_b(x) + E_F(x) - \Delta E_C(x)] \tag{2.4}$$

where x is the mole fraction of the aluminium content in the barrier layer, $\sigma(x)$ is the total sheet charge, q is the electron charge ($1.6\text{x}10^{-19}$), ϵ_0 is the vacuum permittivity, ϵ_r is the relative dielectric constant of the barrier layer, d is the thickness of the barrier layer, $\phi_b(x)$ is the Schottky barrier of the gate contact, E_F is the Fermi level with respect to the GaN conduction band edge energy and ΔE_C is the conduction band offset at the AlGaN/GaN interface where the 2DEG is formed.

2.3 Basic GaN HEMT-substrates and growth

One of the ultimate goals of the epi-layer structure growth is to achieve low surface and bulk defect density. The higher quality material growth results in higher carrier mobility and electron concentration density in the 2DEG channel. The two most popular methods for growing GaN are molecular beam epitaxy (MBE) and metal organic chemical vapour deposition (MOCVD). Figure 2.4 illustrates a standard GaN based HEMT structure. Conventionally, an AlGaN/GaN based HEMT employs a 2 nm GaN cap layer, a 20 nm AlGaN barrier layer (25% Al content), followed by a 3 μm GaN channel grown on a foreign substrate. On the other hand, a conventional AlN/GaN HEMT structure employs a 1 nm GaN cap layer, a 3 nm AlN barrier layer and a 3 μm GaN channel. An explanation of the role of the different substrate options and the consecutive epi-layers is provided next.

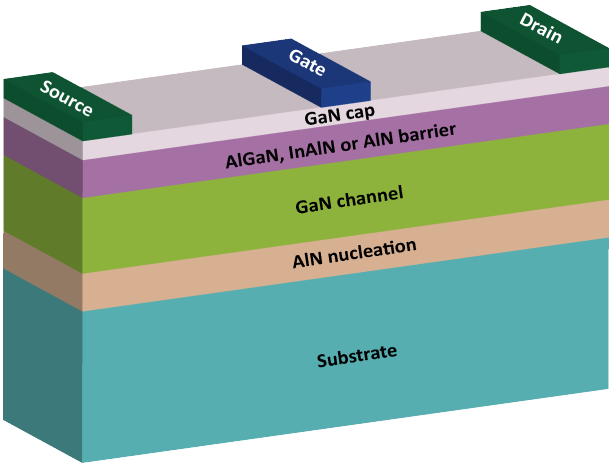

FIGURE 2.4: Cross-section of a basic GaN HEMT structure.

2.3.1 Substrate

Usually GaN is grown on a foreign substrate since native GaN substrates have not been available until recently. The different substrate options available for GaN epi-layer growth include, silicon, sapphire, silicon carbide (SiC), freestanding GaN and chemical vapour deposited (CVD) diamond. The choice of substrate is dependent on several parameters including thermal conductivity, lattice mismatch to GaN, available size, electrical isolation and cost. The substrate type will impact the growth quality, output power and thermal performance of the fabricated HEMT. This section lists the most popular types of substrates available for GaN epi-layer growth and discusses their advantages and disadvantages. The key properties of each substrate is listed in Table 2.1

Property/Substrate	**GaN**	**SiC**	**Silicon**	**Sapphire**	**CVD Diamond**
Lattice constant ($\AA$)	3.189	3.08	5.43	2.75	3.567
Mismatch to GaN (%)	0	3.1	17	13.9	11.9
Thermal conductivity (W/m·K)	130	400	150	35	2000
CTE ($1/10^6$K)	5.59	4.2	3.59	7.5	0.8
Isolation (Ω·cm)	10^9	10^{11}	10^4	10^{16}	10^{16}
Defect density (cm^{-2})	10^3	5×10^8	10^9	8×10^8	-
Wafer size with GaN Epi (inch)	2	6	6	6	4

TABLE 2.1: Properties of commonly used substrates for the growth of GaN HEMTs. CTE= Coefficient of Thermal Expansion.

2.3.1.1 Silicon carbide (SiC)

SiC is the favourite wafer option for high power RF applications as it has a high thermal conductivity of 400 W/mK, good electrical isolation (>10^9 Ω·cm) and low lattice mismatch to GaN of 3.1% which allows for low defect densities to be achieved. It costs relatively higher than silicon but is available in 2-6 inch sizes [60] which makes GaN on SiC able to compete with the 6 inch gallium arsenide (GaAs) technology that is dominant in the market. SiC comes in a semi-insulating form which is required for RF applications. Due to the combination of its uniqueness, SiC is the substrate of choice for this project as the intended application is for microwave power amplifier which requires thermal management. For example, a GaN HEMT generating 120 W of continuous wave (CW) RF power with a drain efficiency of 65% and a CW thermal resistance of 1.5°C/W, exhibits a dissipated power of 64 W. This results in a channel temperature rise of 96°C and allows the device to operate comfortably at base plate temperatures in excess of 100°C. A good review of GaN on SiC is given in [45].

2.3.1.2 Silicon

The interest in silicon wafers comes from their availability in large sizes of up to 12 inches and compatibility with the well established CMOS industry, making them cost effective for commercial power applications. Eight inch GaN on silicon was reported in 2012 [61]. However, there are few challenges associated with the growth of GaN on silicon such as the high lattice mismatch to GaN of 17% and the high coefficient of thermal expansion (CTE) mismatch of 56%. This makes it more challenging to grow GaN on silicon with the grown epi-layers having the highest defect densities among the wafer options. In addition to the nucleation layer, transition layers are required to compensate for the mismatches so the epi-structure is complicated to grow. Also, silicon has the lowest electrical isolation of 10^4 Ω·cm compared to 10^{11} Ω·cm of SiC which makes RF transmission lines made on silicon wafers lossy at high frequencies.

2.3.1.3 Sapphire

Sapphire was popular at the start of the GaN evolution in 1993 due to its affordability and availability at the time [6]. One of the main advantages of sapphire relative to SiC is the lack of micropipes. GaN on sapphire is commercially available in sizes of up to 6 inches. Since SiC and silicon wafers became available at an affordable cost, the use of sapphire substrates became limited to the LED market. Sapphire has a lattice mismatch to GaN of 13.9% [62] making it suitable for GaN growth. GaN epi-layers

grown on sapphire exhibit lower defect densities compared to GaN epi-layers grown on silicon.

2.3.1.4 Freestanding GaN

GaN wafers were not commercially available until recently and are now available in 2 inch sizes [63]. The advantage of native GaN wafer is that there is no lattice mismatch to GaN epi-layers and therefore, low defect density epi-layers can be achieved. Defect densities as low as 10^4 cm^{-2} [64] have been reported on GaN grown on freestanding GaN substrates. This is a major improvement compared to defect densities of 10^8-10^9 cm^{-2} exhibited by GaN grown on foreign substrates. The availability of freestanding GaN substrates is crucial for GaN based laser diodes since their performance is highly dependent on the defect densities [65]. A good review on GaN substrates is given in [66].

2.3.1.5 CVD Diamond

Chemical vapour deposited (CVD) diamond has the highest thermal conductivity of 2000 W/mK among the substrate choices. If used as a substrate, it helps in reducing the channel temperature of GaN HEMTs. GaN on diamond was recently reported [67], and is getting increasing attention in the high power RF market due to its high thermal conductivity. However, the thermal and lattice mismatch of diamond to GaN is high, making it very challenging to grow GaN on diamond and limiting its advantage.

A new technique to realise GaN on diamond uses foreign substrates to grow GaN. The foreign substrate is later removed from the back and the GaN epi-structure is atomically bonded to a diamond substrate. This technique has a potential to enable GaN on diamond devices delivering three times the power densities compared to GaN on SiC [68]. CVD Diamond wafers are available in sizes of up to 8 inches [69] and atomically attached GaN to diamond wafers of sizes up to 4 inches have been demonstrated [70]. The cost for diamond is the highest among the other wafer options.

2.3.2 GaN-based HEMT structure

Depending on the substrate choice, subsequent epi-layers are designed to achieve high mobility and high current density in the channel. They are also designed to compensate the mismatch of the lattice and the coefficient of thermal expansion between the substrate and the wafer. The role of each epi-layer is explained next.

2.3.2.1 Nucleation layer

The nucleation layer is required when GaN is grown on a foreign substrate to reduce the lattice mismatch and stress between the GaN buffer and the foreign substrate. The nucleation layer is usually a thin AlN (20-200 nm) depending on the chosen substrate. It helps reduce the defect density of the grown material.

2.3.2.2 Channel layer

The GaN channel layer has a lower band gap (3.4 eV) compared to the barrier layer (4 eV for AlGaN with 25% Al content). The difference in band gap energies between the GaN channel and the barrier layer forms what is called the 2DEG. Details about the 2DEG formation were given in section 2.2.3.

2.3.2.3 Barrier layer

The barrier layer is the most important layer in a HEMT structure since it determines the electron density and mobility in the 2DEG channel. The higher the band gap, the higher the electron density in the 2DEG channel, leading to higher output power of the fabricated HEMT. It can be engineered for optimum device performance. The most popular barrier layers are Aluminium Gallium Nitride (AlGaN) [71], Indium Aluminium Nitride (InAlN) [17] and Aluminium Nitride (AlN) [72].

- **AlGaN barrier** is the most common layer due to its earlier adoption in the GaN community. It usually comes in Al-Ga ratios between 20% and 40%, where if the percentage goes higher the structure suffers from poor quality [73]. Still, material with Al content >40% have been reported [74, 75]. A typical AlGaN thickness is between 20 and 30 nm, and the effect of variation in the thickness is reported in [76]. The defect density of AlGaN barrier on GaN increases significantly for Al content higher than 30% for a typical thickness of 18 nm.
- An **InAlN barrier** (with 17% In content and 83% Al content) can be grown lattice matched to GaN, and therefore reduce the surface defect density. It also benefits from the higher band gap of 4.7 eV compared to 4 eV of $Al_{0.25}Ga_{0.75}N$ and hence higher current densities in the channel can be achieved [77]. The typical ratio of indium in the InAlN barrier is 17% and the typical thickness is 7-10 nm [78]. Thus, InAlN/GaN is another interesting material structure which offers electron densities of up to two times the AlGaN/GaN material. State of the art DC and RF devices

based on InAlN/GaN have been demonstrated with competitive performance to AlGaN/GaN devices [79–81].

- The all binary **AlN barrier** has been increasingly researched over the last decade as the technology employing AlGaN barrier is approaching maturity and saturation in terms of both growth and device performance. The main advantage of AlN is that it has the widest band gap among the three barrier options and hence can offer up to three times the output current density compared to the $Al_{0.25}Ga_{0.75}N$ barrier. There are some challenges that are still left to be solved ranging from growth challenges to realisation of good Ohmic contacts and surface degradation during processing. The thinner AlN barrier (∼3 nm) compared to AlGaN barrier (∼20 nm) allow devices to be aggressively scaled down, leading to the delivery of higher current densities and higher frequencies. Impressive current densities of 4 A/mm and f_T/f_{max} of 342/518 GHz have been reported on AlN barrier [21].

2.3.3 Cap layer

The cap layer (usually GaN) terminates the HEMT structure (hence the name). It has many benefits including preventing the barrier from relaxation [82], which reduces the gate leakage current as it increases the barrier height [83]. It also provides surface passivation which reduces oxidation and increases the 2DEG density [84]. Since GaN has a lower band gap (3.4 eV) compared to the barrier (4 eV 25% Al content) [85], it helps in reducing the Ohmic contact resistance on an AlGaN/GaN structure. A p-doped GaN cap was shown to improve the breakdown voltage of AlGaN/GaN HEMTs [86]. The typical thickness of a GaN cap is 1-2 nm.

2.4 Principle of operation of GaN HEMTs

A GaN based field effect transistor is realised by fabricating a Schottky contact (gate) in addition to two Ohmic contacts (source and drain) as illustrated in Figure 2.5. In a standard depletion mode HEMT structure, the 2DEG exists without the need for an external bias to be applied. This is due to the polarisation effect that was explained earlier (section 2.2). To turn the device off, a negative gate bias is applied and the 2DEG channel starts to deplete until a gate bias greater than the threshold voltage is reached, at which the channel becomes totally depleted of electrons and the device is turned off. On the other hand when the gate bias is positive, the electron density in the 2DEG increases leading to a higher current flowing between the source and the drain. For a Schottky gate, the gate voltage is limited to +1 V after which the gate will

turn on and starts conducting, behaving like a Schottky diode. For enhancement mode devices, the 2DEG channel does not exist naturally and an external gate voltage must be applied to accumulate enough electrons to create the 2DEG channel. Enhancement mode structures can be achieved by different techniques including the use of p-type GaN cap layer to deplete the 2DEG channel, the use of a thin AlGaN barrier (3 nm) that is below the critical thickness for naturally creating the 2DEG channel or recessing the AlGaN barrier under the gate to locally deplete the 2DEG channel. For enhancement mode devices, a positive gate voltage is required to accumulate enough electrons in the channel.

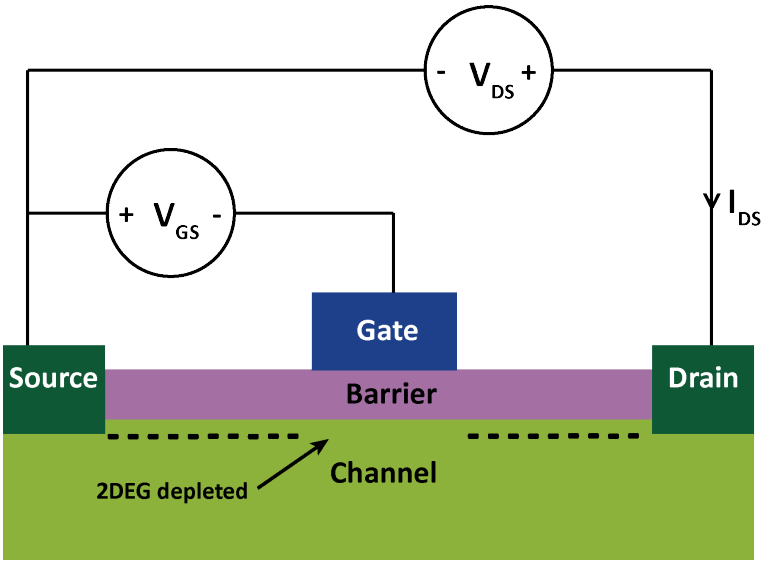

FIGURE 2.5: Illustration of HEMT operation principle and biasing.

GaN based HEMTs operate similarly to general Field Effect Transistors (FETs). In the linear region, the current flowing between the source and drain can be derived from the charge in the channel and the time taken for such charge to cross the channel due to an applied voltage (electric field). The time, t, taken for electrons to cross the channel at an effective velocity, v_{eff}, is given by L_{DS}/v_{eff}, where L_{DS} is the drain-source separation, while the total charge in the channel is given by $qn_s(\mathrm{L}_{DS}\mathrm{W}_G)$

Therefore, the current flowing is given by:

$$\begin{aligned} I_{DS} &= \frac{qn_s L_{DS} W_G}{\frac{L_{DS}}{v_{eff}}} \\ &= qn_s v_{eff} W_G \end{aligned} \tag{2.5}$$

where q is the electron charge, n_s is the sheet carrier concentration, v_{eff} is the effective velocity of the electrons in the channel and W_G is the gate width.

The typical current voltage characteristic of a GaN HEMT is illustrated in Figure 2.6. It shows the drain current characteristic as the drain voltage is increased at given gate voltages. As the gate voltage is increased, more electrons accumulate in the 2DEG channel and hence results in increasing the drain current.

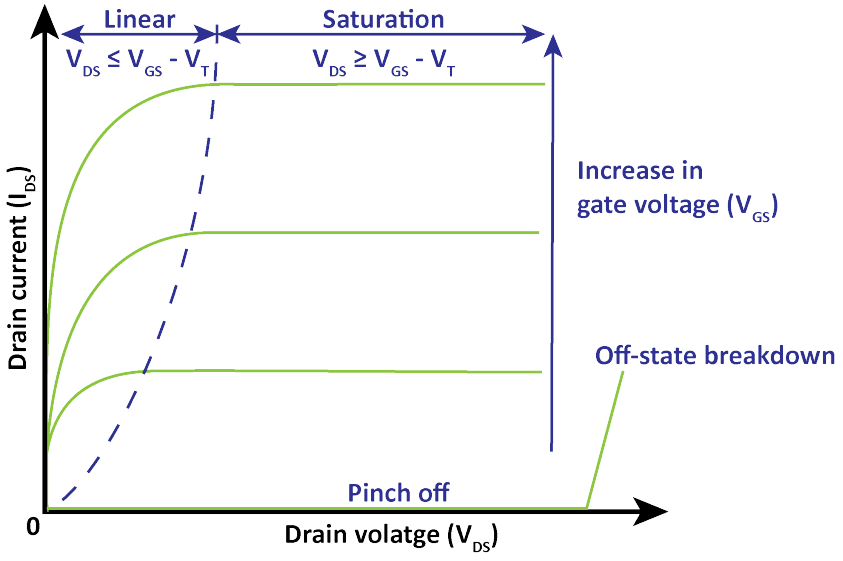

FIGURE 2.6: Output IV characteristic of a typical GaN HEMT.

The charge in the channel can also be expressed in terms of the gate voltage as:

$$Q = CV \tag{2.6}$$

where C is the gate capacitance, ($C = \epsilon \mathrm{L}_G W_G / d_{barrier}$) and V is the effective voltage (V= V_G-V_T). Using the expression for charge given earlier and in 2.6, n_s becomes:

$$n_s = \frac{\varepsilon_{barrier}}{q(d_{barrier} + \triangle d)} (V_G - V_T) \tag{2.7}$$

where $\mathrm{d}_{barrier}$ is the thickness of the barrier layer, $\triangle$d is the effective distance of the 2DEG from the heterointerface, V_G is the gate bias and V_T is the threshold voltage. When the gate voltage is equal to the threshold voltage, n_s is equal to zero and no current flows between the source and drain.

The velocity of the electrons in the channel is the product of their mobility and the applied electric field:

$$v_{eff} = \mu_n E = \mu_n(\frac{V_{DS}}{L_{DS}}) \tag{2.8}$$

where μ_n is the electron mobility, E is the applied electric field and V_{DS} is the drain-source voltage.

The sheet resistance (R_{sh}) of the 2DEG channel can be derived from 2.5 as follows:

$$I_{DS} = qn_s(\mu_n \frac{V_{DS}}{L_{DS}})W_G \tag{2.9}$$

From Ohms law, V=IR, the channel resistance, R_{ch} can be derived by rearranging 2.9 to:

$$\frac{V_{DS}}{I_{DS}} = R_{ch} = \frac{L_{DS}}{qn_s\mu_n W_G} \tag{2.10}$$

When L_{DS}=W_G, R_{ch} becomes the sheet resistance, R_{sh}

$$R_{ch} = \frac{1}{qn_s\mu_n} = R_{sh} \tag{2.11}$$

Electron velocity is linearly related to the electric field strength when the device is operated at a low drain voltage where $V_{DS} < V_G$ - V_T (linear region). However, at high drain biases where $V_{DS} > V_G$ - V_T (saturation region), the effective electron velocity saturates and becomes independent of the drain bias. Velocity saturation (v_{sat}) occurs due to electron scattering and causes the drain bias under the gate to start pinching off the channel at the drain end of the gate. This continues until the channel fully restricts the electrons, limiting their quantity, which results in the device operating under the saturation region condition. Devices are usually biased at high drain voltages (in the saturation region) to achieve high output powers. In this case, the drain current is calculated using:

$$I_{DS} = \frac{\varepsilon_{barrier} v_{sat} W_G}{d_{barrier} + \Delta d}(V_G - V_T) \tag{2.12}$$

Transconductance, g_m can be defined as follows:

$$g_m = \frac{\partial I_{DS}}{\partial V_G} \tag{2.13}$$

In the saturation region, the transconductance becomes:

$$g_m = \frac{\varepsilon_{barrier} v_{sat} W_G}{d_{barrier} + \Delta d} \tag{2.14}$$

2.5 Summary

This chapter covered the basic GaN HEMT theory from the simple physics to the substrate options and epi-layer growth and design. The spontaneous and piezoelectric polarisations have been explained and their role in creating the 2DEG channel. The polarisations in the HEMT structure can be engineered in to achieve wither enhancement mode or depletion mode operation. The barrier thickness and aluminium content of the barrier will affect the polarisation and the higher the thickness or the aluminium content the stronger the polarisation which in turn result in depletion mode. A 25% aluminium in a 3 nm AlGaN barrier will result in an enhancement mode operation, while 4 nm and beyond will result in depletion mode operation. The superiority of GaN HEMTs stems from their ability to form heterostructures to wider band gap materials which in turn results in creating 2DEG channel that exhibit high electron densities and high electron mobilities. The most popular barrier layers that are used to create the 2DEG channel are AlGaN, InAlN and AlN. The AlGaN barrier is the most popular due to the ease of epitaxial growth while it offers less electrons concentration compared to the widest band gap of AlN. A lot of effort is invested in optimising the growth of AlN as it offers increased electron concentration and hence higher output currents. The substrate choice has also been discussed in this chapter. As native GaN substrates have not been available until recently, foreign substrates are used to grow GaN and the most popular are SiC, silicon and sapphire. Although SiC is the most expensive, it offers the least lattice mismatch and the highest thermal conductivity. Silicon is the cheapest and has a decent thermal conductivity but suffers form high lattice mismatch and high coefficient of thermal expansion. To reduce the lattice mismatch between GaN and silicon, a thicker AlN nucleation layer (200 nm) is used and also a thicker GaN channel (5 *mu*) compared to material grown on sapphire and SiC with nucleation layer and channel layer typical thicknesses of 20 nm and 2 *mu* respectively. The role of substrates in thermal management will be discussed in more detail in Chapter 6. The next chapter will explain the basic fabrication techniques.

CHAPTER 3

GaN HEMT Device Fabrication

This chapter explains the various techniques used for the process development of fabrication steps required in this project. The different processes include, epitaxial growth, lithography, deposition methods for metals and dielectrics and etching techniques that are available in a standard clean room. All the work done for this project was carried out at the James Watt Nanofabrication Centre (JWNC) at the University of Glasgow. It houses all of the micro and nanofabrication facilities of the University. The processes will be outlined to illustrate the realisation of GaN HEMTs. A good overview of processing techniques on GaN is given in [87].

3.1 Epitaxial material growth

During epitaxial growth, the atoms are transported from sources of high purity to the surface of the substrate wafer. The optimisation of growth temperature and pressure is essential for the layered structure uniformity and quality. The two most popular techniques used for growing GaN based heterostructures are metal organic chemical vapour deposition (MOCVD) [88] and molecular beam epitaxy (MBE) [89, 90]. All the wafers used in this project were commercially grown, mostly using MOCVD.

3.1.1 MOCVD

Metal organic chemical vapour deposition (MOCVD) is the most popular growth method used in the GaN industry due to its low cost compared to other available growth techniques [91]. A typical MOCVD chamber can grow up to 41×2 inch wafers simultaneously and the growth speed is faster compared to MBE. Typical growth rates of GaN in an

MOCVD reactor are about 1-2 μm/h [92]. In general, MOCVD growth of GaN is performed at temperatures well higher than 1000°C. This is much higher than MBE growth which is performed at temperatures of ∼700°C.

3.1.2 MBE

Molecular beam epitaxy (MBE) is the second most popular growth technique used for growing GaN-based epi-layers. The advantage of an MBE system is the very precise definition as well as the increased flexibility of the polarity of the interfaces [93]. A typical MBE reactor is limited to growing up to 3×2 inch wafers. Typical growth rates for GaN in an MBE system are 0.5-1 μm/h which is much slower compared to MOCVD [94]. Therefore, MBE cannot meet the demand of the GaN industry in terms of wafer supply. As a result, its use is limited to the research domain due to the quality of growth that can be achieved, and the material can be used for proof of concept.

Most wafers used during this project were grown using MOCVD. AlN/GaN wafers were grown using MBE. MBE is more suitable for the growth of GaN HEMTs with ultra thin 3 nm AlN barriers. The work started with conventional structures and afterwards the epi-layer choice was determined based on the results of the first runs.

3.2 Lithography

Lithography is the process of transferring a designed pattern onto a wafer surface using a mask. The two most popular lithography processes are optical and electron beam lithography.

3.2.1 Photolithography

Photolithography (also known as Optical lithography) is the most common way of manufacturing semiconductor devices in the industry since it can meet the market demand for high throughput and minimum feature size. A Karl Suss MA6 mask aligner is used in the JWNC for photolithography processes and has a minimum feature size of 1 μm. The high throughput of optical lithography reduces the unit cost of fabricated devices and helps meet the market demand. All of the process optimisation work done for this project was carried out using photolithography since it is cheaper and faster compared to electron-beam lithography. Photolithography uses a UV light to expose a wafer that is covered in photo-resist. A hard chrome mask is usually manufactured using electron beam lithography.

3.2.2 Electron-beam lithography

Electron-beam lithography offers the advantage of high resolution and positioning accuracy. This is required especially for the fabrication of small features such as sub 100 nm transistor gates. The Vistec VB6-UHR-EWF is used for electron beam processing at the JWNC. It has a minimum resolution of 0.5 nm, a maximum field size of 1.2 mm and a minimum spot size of 4 nm. It was used for instance to realise 10 nm T-gates [95] and sub 5 nm gaps between metallic electrodes [96]. The main disadvantage of electron-beam lithography is that it can take few hours to write a pattern which otherwise could be written using photolithography in a few seconds. Nonetheless, electron-beam lithography is still used in many research-based facilities. This is because the design files are electronic and designs can therefore be easily altered using a CAD based software, unlike optical lithography where a hard mask has to be made every time the design needs to be changed.

3.2.3 Photo-resists

Photo-resist is a polymer that is sensitive to ultra-violet radiation. It is applied uniformly to the wafer surface using spinning or spraying. The thickness of the resist can be controlled by controlling the acceleration, spin speed and time. There are positive and negative photo-resists. In positive photo-resists, the polymer bonds break in the regions exposed to radiation and hence the resist clears during the development stage. In negative photo-resists, the radiation causes the exposed regions to exhibit cross-linking of the resist making the bond stronger. As a result, non exposed regions are soluble during the development stage while the exposed regions stay intact. Negative photo-resist is mostly useful when there is a need for large areas of photo-resist to be removed since the area which requires exposure is small. An illustration of positive and negative photo-resist exposure and development is shown in Figure 3.1.

One way to realise a metal structure on a semiconductor surface is to use a lift-off process. It is a technique which uses photo-resist, and windows are opened in the photo-resist in the areas where the metal presence is desired. The windows are opened using UV exposure. The metal is then blanket deposited covering the exposed areas of the semiconductor as well as the photo-resist surface. After using a solvent such as acetone, the photo-resist is dissolved causing the metal covering it to be removed. This leaves the metal deposited in the exposed windows to remain on the semiconductor's surface. A successful lift-off process requires the photo-resist to have an undercut so that the metal on the surface of the photo-resist is disconnected from the metal on the semiconductor. In photolithography, a single layer photo-resist (S1818 or S1805) can be used for a lift-off

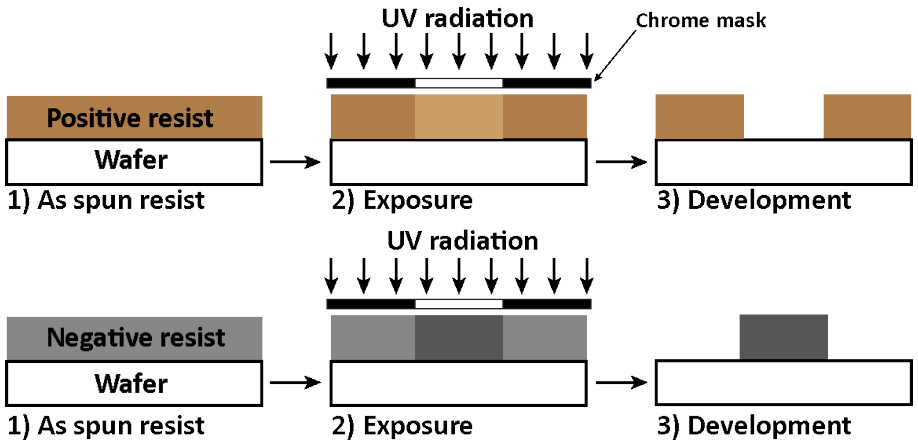

FIGURE 3.1: Positive and negative photo-resist spinning and development.

process. It is exposed to a developer (MF319 developer) before the UV exposure stage to harden the surface and make it less sensitive to the developer solution. This leads to the lower part of the resist to be developed faster. Figure 3.2a illustrates the single layer resist lift-off process flow.

Another option is to use a combination of two different photo-resists to achieve the undercut profile which is the case for this project where a combination of LOR10A and S1818 photo-resists were used. Figure 3.2b illustrates a bilayer photo-resist process flow. The photo-resist has an undercut profile so that the resist stripper can access the resist under the metal and result in the total removal of the resist along with the excess metal. To achieve such undercut profiles in electron-beam resists, a bilayer is used where the lower layer has a smaller molecular weight than the upper layer, making it more sensitive to radiation and hence gets developed faster than the upper layer.

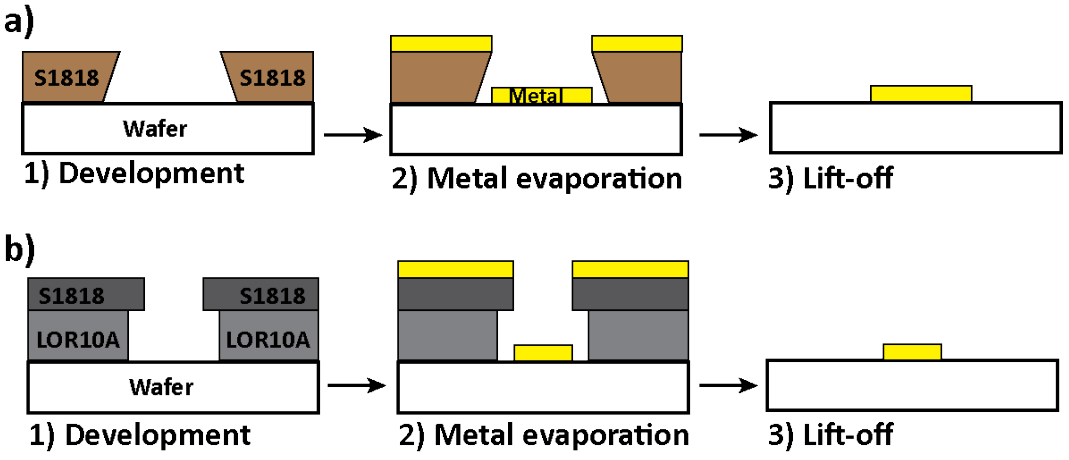

FIGURE 3.2: Illustration of a lift-off process flow using a) a single layer photo-resist and b) a bilayer photo-resist.

3.3 Metallisation

Making metal contacts to semiconductors is an important step in device fabrication since the use of metal is necessary for making electrical connections from the semiconductor to the outside world. There are three main techniques used for metallisation: evaporation, sputtering and electroplating.

3.3.1 Evaporation

Evaporation can be done by heating a metallic source to a temperature at which it vaporises. Therefore, all evaporation processes can be considered thermal. There are two ways to achieve thermal evaporation; resistive and electron beam. Resistive evaporators are usually called thermal since an electric current passes through a crucible which acts as a resistor that heats up until it reaches the evaporation temperature of the metal.

Evaporation can also be done using an electron beam focused directly towards the solid metal target causing it to evaporate, a technique known as electron beam evaporation. It differs from resistive evaporation as the crucible is water cooled so it does not heat up. Only the surface of the metal at which the beam is focused evaporates. In the case of resistive evaporators, there is a possibility of the crucible being evaporated if its melting point is similar to the target metal, which causes contamination. This is not the case in electron beam evaporated metals as a consequence of the local heating, which results a a high purity deposited film. For this project, the main metallisation technique used for making transistor contacts is electron beam evaporation. The tool used for evaporation is the Plassys MEB550S (Plassys II). At the start of the run, the wafer is loaded into the evaporation chamber and then the chamber is pumped into vacuum usually in the range of 10^{-6} - 10^{-8} Torr. The electron gun is then switched-on to establish a stable evaporation rate while the shutter protects the sample from initially evaporated metal during the initial heating stage. The shutter then opens and the deposited metal thickness is monitored using the feedback of the oscillation frequency from a quartz crystal. When the required thickness is acquired the shutter closes and the chamber is vented before the wafer is unloaded. The electron beam evaporation process is illustrated in Figure 3.3.

3.3.2 Sputtering

Sputtering is different from evaporation as it is a physical rather than a thermal process and therefore can be carried out at low temperatures. A DC or RF source is used

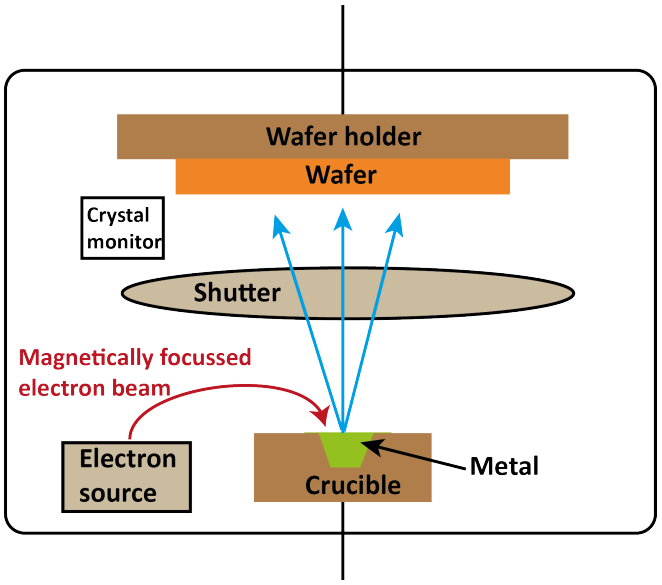

FIGURE 3.3: Illustration of the metal electron beam evaporation mechanism.

to excite a plasma generated using a noble gas such as argon to reach the activation energy required for sputtering a given metal. The target is negatively biased and the plasma sputters atoms of metal from the target. A DC source is usually used to sputter targets that are electrically conductive like metals, while RF sources are usually used to sputter alloys and compounds that are electrically insulating. Sputtering can be done using high pressures of around 10^{-4} Torr. As a result, the metal atoms collide together before hitting the target with random angles of incidence on the wafer. This results in a metal coating that is more conformal compared to evaporated films. The drawback of this technique is that the conventional lift-off process does not work with sputtered films. The advantage of sputtering is that it is independent of melting temperatures, and therefore metals that cannot be easily melted can be sputtered. At the JWNC, the Plassys III tool is used for sputtering. The sputtering process is illustrated in Figure 3.4.

3.3.3 Electroplating

Evaporation and sputtering are usually limited to the deposition of one or a few more micrometer-thick metal layers at a time. They also have the disadvantage of wasting metals by covering areas that are not required to be metallised including the chamber, and hence they are not the most efficient metallisation schemes. However, industrial processes require the deposition of layers that are in the order of few tens of micrometers thick. These thick layers are required to make interconnects, bondpads and backside processes. For such a requirement, electroplating is the most efficient process which is widely used in the industry.

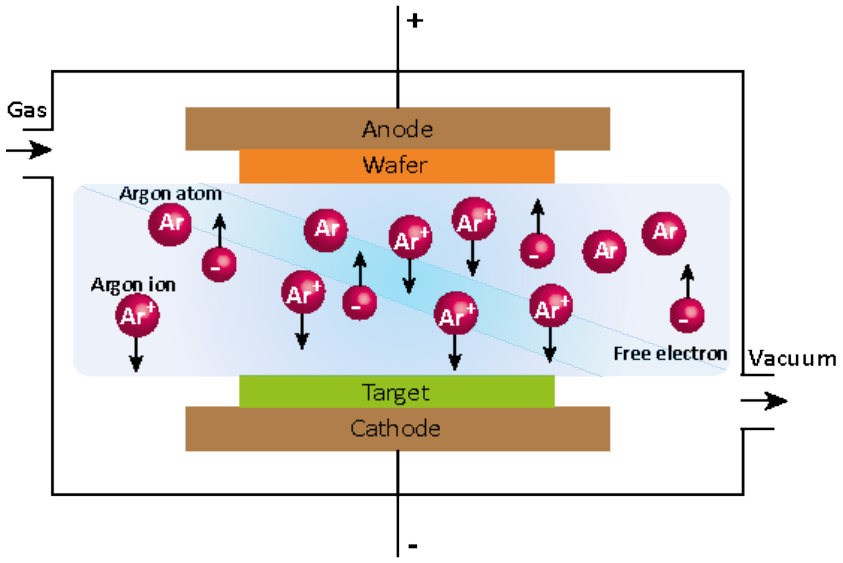

FIGURE 3.4: Illustration of the metal sputtering mechanism.

Electroplating is a process in which an electric current is used to reduce dissolved metal cations so that they form a coherent metal coating on an electrode. Usually before electroplating, the features are patterned using a photo resist followed by the deposition of electron beam evaporated or sputtered metals. This is called a seed layer which is used to make an electric connection to the surfaces that are required to be electroplated. The sample is then attached to the cathode in a beaker filled with an ion rich solution of the required metal to be plated. The cathode and anode are then biased to make the current flow, where the ions start moving from the anode and are deposited on the cathode. Usually, electroplating is used for large features which have a high tolerance and does not require high resolution since the electroplated metal layer is non uniform. For this project, the process of copper electroplating was used to create heat sink blocks. More details are given in section 6.8.5. The process of electroplating is illustrated in Figure 3.5.

3.4 Etching

Etching is the process of removing a metal or semiconductor material. It has many applications including device isolation, creating vias to connect the back of a wafer to the front side, removing unwanted metals or semiconductor layers from certain areas of the wafer. There are two etching methods; wet and dry etching.

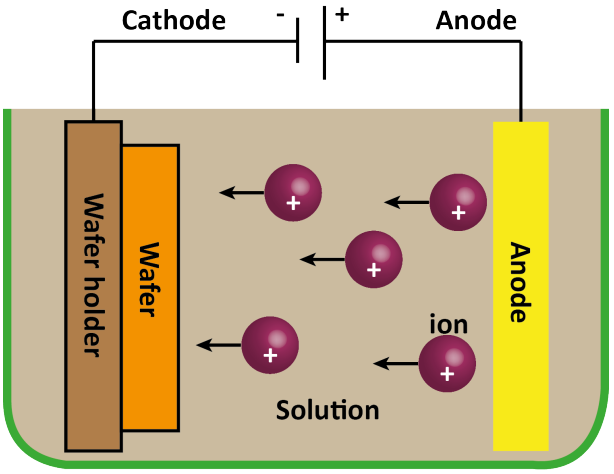

FIGURE 3.5: Illustration of the metal electroplating process.

3.4.1 Wet etching

The wet etching process is desirable since it is less damaging to the surface compared to dry etching. It relies on the chemistry between reactants in the liquid and the surface to be etched. The high chemical stability of GaN makes it highly resistant to conventional wet etching. Etching is polarity dependent, where N-polar GaN is more reactive to wet etchants than Ga polar GaN. The polar dependence may be due to the different banding states of the N-polar GaN and the Ga polar GaN [97]. Since the epi-structure grown for this work is Ga polar, wet etching cannot be used to remove GaN epi-layers. Wet etching during the project was used for the purpose of removing SiN passivation layers. The chemistry used is dilute hydrofluoric acid HF:H_2O with a ratio of (1:10), resulting in an etch rate of 200 nm/min. Wet etching of copper was also done during this project with details provided in Section 6.8.4.

3.4.2 Dry etching

Dry etching is widely used in GaN for the purpose of device isolation [98]. To achieve good electrical isolation, the epi-layers are etched down to the semi-insulating buffer layer, which is typically around 100-200 nm deep. Parameters such as gas flow and chamber pressure can be tailored to improve directionality of the etching profile and hence preserve the lithographically defined features. Dry etching of GaN will be discussed in more detail in section 5.4.1. There are two etching techniques for GaN that are available at the JWNC: reactive ion etching (RIE) and inductive coupled plasma (ICP) etching. A good comparison between the two techniques is given in [99].

RIE has a single RF plasma source which determines both the ion density and energy in the chamber. GaN etching using an RIE system has a typical etching rates of $\sim$ 100 nm/min. ICP has separate DC and RF generators, allowing for separate control of ion energy and ion density in the chamber. Increasing the RF power leads to an increase in ion energy while increasing the ICP power results in increasing the plasma density. If the balance between the physical and chemical aspects of the process is not maintained, it results in an unacceptable pitting or pillar formation on GaN surfaces. The ability to control the ICP and RF powers independently allows for higher process flexibility. GaN etch rates of up to 1 μm/min have been reported using an ICP etching system [100]. Figure 3.6 illustrates the RIE and ICP etching tools.

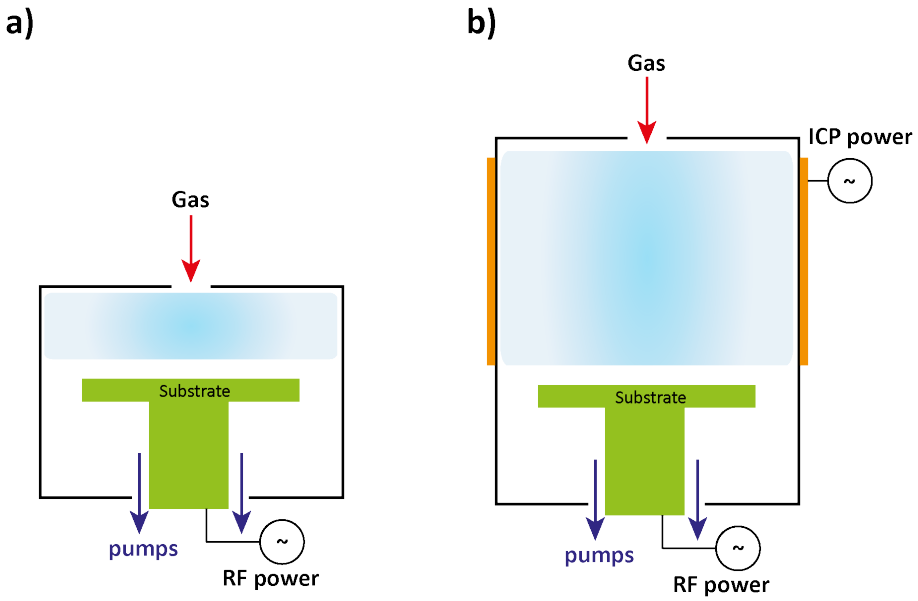

FIGURE 3.6: Illustration of a) RIE system, b) ICP system.

3.5 HEMT process flow

This section will describe the GaN HEMT process flow used to fabricate devices on this project. Two types of devices were fabricated, DC and RF devices. The layout of each device will be explained as well as the full fabrication process.

3.5.1 Mask design

Device fabrication in this project used optical lithography, and therefore a mask was designed and used for pattern transfer. L-edit software (from Tanner-EDA [101]) was

used to design the mask which was then made using an electron-beam lithography tool, the Vistec VB6-UHR-EWF.

A typical mask is designed to have a variety of device geometries in order to investigate the effect of the device geometry on device performance. The mask also has test structures such as CTLM to assess the quality of the Ohmic contacts after each run. Since the typical device has several layers, the alignment markers are used to align the different layers during exposure.

The gate wrap-around DC device layout is shown in Figure 3.7. It is used for process development since it requires only two lithography steps, and hence more iterations can be done when compared to RF device layout. Device fabrication starts by Ohmic contact metal deposition, followed by high temperature anneal and finally the gate metal deposition. More details are given in section 3.5.2. The mesa isolation step is not required as the gate wraps around the drain contact and hence, it can fully deplete the channel when biased below the threshold voltage. A typical gate warp-around DC device employs a gate width of 100 μm, a gate length of 3 μm, a source-to-drain separation of 9 μm and a gate-to-drain separation of 3 μm.

FIGURE 3.7: Layout of a DC device.

A typical RF device layout is shown in Figure 3.8. The processing starts with the Ohmic metallisation followed by mesa isolation. The gate metallisation is done next, followed by the bondpad metal deposition. The standard RF device fabrication requires four lithography steps. A typical RF device employs a gate width of 2×100 μm, a gate length of 3 μm, a source-to-drain separation of 9 μm, a gate-to-drain separation of 3 μm and a gate-to-gate pitch of 100 μm. An example of a mask design is shown in Figure 3.9.

3.5.2 Ohmic contact formation

The metal deposition in JWNC is done using a lift-off process. In order for the lift-off process to work, an undercut profile in the resist is vital to get a successful result as explained earlier in section 3.2.3. For this project, the bilayer LOR10A and S1818 photoresists were used. The conventional titanium(Ti)/aluminium(Al)/nickel(Ni)/gold(Au) metal scheme is used for the Ohmic contacts with thicknesses of 30/180/40/100 nm respectively. After lift-off, the contacts are annealed in N_2 ambient at 800°C for 30 seconds.

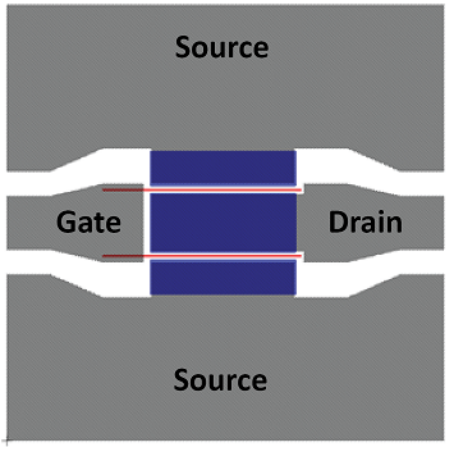

FIGURE 3.8: Layout of an RF device.

3.5.3 Mesa isolation

Mesa isolation is required to electrically isolate adjacent devices. In the JWNC, both RIE and ICP dry etching recipes are available to etch GaN. Device isolation is only required for the RF devices. The RIE recipe is as follows: $SiCl_4$ gas flow rate of 25 sccm, chamber pressure of 8 mT and 200 W of power. The etch depth for a 4 minutes duration is about 160 nm in the RIE tool, i.e. an etch rate of 40nm/min. The ICP recipe is as follows: $Cl_2/BCl_3/Ar$ gases with flow rates of 20/5/10 sccm respectively, chamber pressure of 10 mT and ICP and RF powers of 150 W and 28 W, respectively. For a 6 minute etch duration, the etch depth is 120 nm in the ICP tool. The etch rate is 20 nm/min. Before dry etching GaN, the surface is patterned using S1818 resist. After exposure and development, the sample is loaded into the chamber of the dry etching tool.

3.5.4 Gate metallisation

Gate metallisation is again defined using the bilayer LOR10A and S1818 photo resists similar to the Ohmic contact recipe. The Ni/Au metal scheme is used with thicknesses of 20/200 nm respectively. A typical gate has a gate width of 100 μm and a gate length of 3 μm.

3.5.5 Bondpad metallisation

The bondpad metallisation is required only for the RF devices and the metal scheme used is Ti/Au with thicknesses of 20/200 nm respectively.

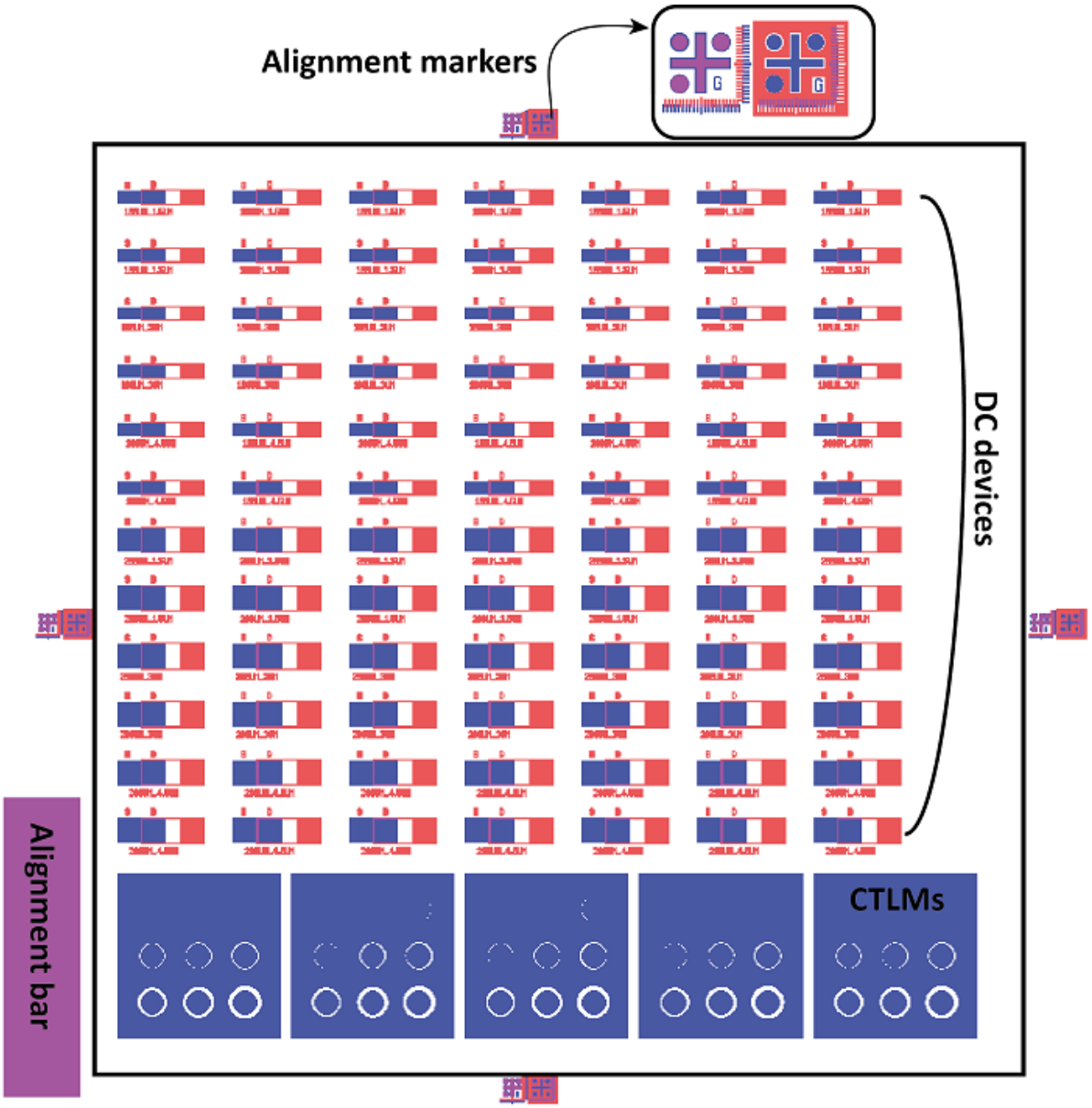

FIGURE 3.9: Complete photolithography mask for DC devices which includes CTLM structures and alignment markers.

3.6 Summary

This chapter described the details of the different processing techniques from epitaxial growth to the lithography and metallisation techniques. The process optimisation during this project involved the processes developed for realising thermal vias for heat sink integration of GaN HEMTs. Sputtering copper, evaporation of copper and electroplating copper were trilled. Wet etching of copper was also done. Basic processing techniques such as lift-off were explained. The fabrication steps for both DC and RF devices were also described. Chapter 4 will explain the Ohmic contact formation in more detail.

CHAPTER 4

Ohmic Contacts on GaN-Based Transistor Material

4.1 Introduction

The performance of GaN HEMTs is highly dependent on the Ohmic contacts. Achieving low Ohmic contact resistance is highly desirable since this will result in increasing current densities, reducing the total On-resistance and decreasing the power dissipation in the Ohmic contact. To reduce the Ohmic contact resistance, one can either reduce the barrier thickness, or lower the barrier height at the metal-semiconductor interface.

This chapter presents a new approach of using in-situ SiN_x passivation of an AlN/GaN HEMT grown on SiC wafer to achieve low Ohmic contact resistance. The process is reliable and repeatable, and opens the door to realising high power RF circuits on AlN barrier GaN devices for the first time. This chapter starts by explaining the theory of the metal-semiconductor interface and the transmission line model, followed by a literature review on Ohmic contacts made on AlGaN and AlN barriers. Work on recessed Ohmics on AlGaN/GaN material will then be discussed and finally the optimisation work for Ohmic contacts on AlN barriers done for this project will be presented.

4.2 Metal-semiconductor interface theory

In order to incorporate a semiconductor device into a system, the use of a metal contact is necessary. Electrons are required to move from the semiconductor into the metal and vise versa, and therefore, they must overcome the energy barriers at the metal-semiconductor interface. When a metal makes contact with a semiconductor, a barrier

is formed at the metal semiconductor interface. Current conduction is controlled by this barrier. A metal in contact with an n-type semiconductor will cause electrons to flow from the semiconductor into the metal's conduction band to lower their energy. Under equilibrium, Fermi levels will align on both sides forming a single system. The Fermi level in the semiconductor is lowered by an amount equal to the difference between the two work functions, which is referred to as band bending [102]. Figure 4.1 illustrates the energy-band diagram of a metal in contact with an n-type semiconductor.

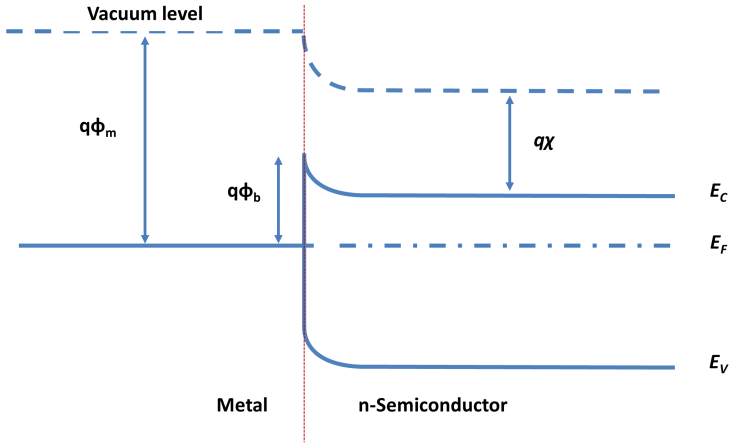

FIGURE 4.1: Energy-band diagram of metal-semiconductor (n-type) contact.

A discontinuity between the conduction bands of the metal and semiconductor is caused by band bending and is referred to as an energy barrier or Schottky barrier. The ideal Schottky barrier height can be calculated by [102]:

$$q\phi_b = q\phi_m - q\chi \tag{4.1}$$

where ϕ_m is the metal work function and qχ is the electron affinity, which is the potential difference between the bottom of the conduction band and the vacuum level of the semiconductor surface.

There are three main mechanisms that exist by which the electrons can transit through the barrier; thermionic emission, field emission and thermionic field emission. Thermionic emission depends on thermal energy to give the electrons sufficient energy to cross the energy barrier. Field emission depends on the quantum dimensions of the barrier, and therefore happens in highly doped contacts. Thermionic field emission is a combination of thermionic and field emissions. Figure 4.2 illustrates the three types of emission that can occur in a semiconductor. There are two types of metal-semiconductor contacts: Ohmic and Schottky.

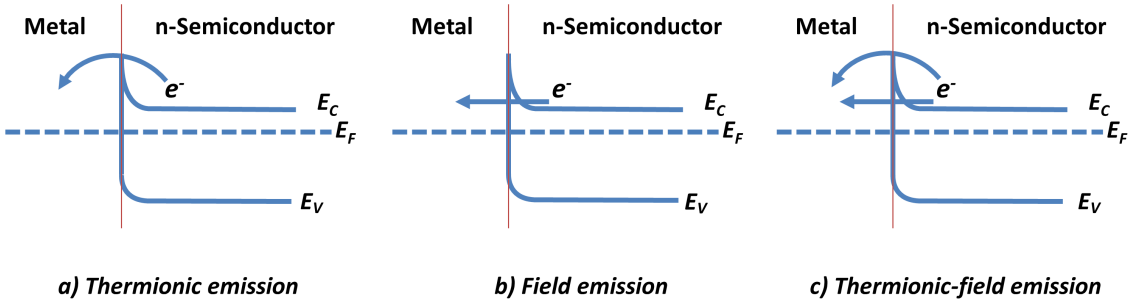

FIGURE 4.2: The three types of emissions in a semiconductor, a) thermionic emission, b) field emission and c) thermionic field emission.

4.2.1 Rectifying (Schottky) contacts theory

Rectifying (Schottky) contacts exhibit a non-linear behaviour and are typically used as a gate metal. As-deposited gate metal on the semiconductor surface is Schottky by nature. The high barrier height of a Schottky contact is desirable to reduce the current flowing from the semiconductor into the gate metal which is referred to as gate leakage current. Since the GaN material used for this project is undoped, the resulting barrier is wide leading to limiting tunneling of electrons and hence, the main transport mechanism in Schottky contacts is thermionic emission.

Figure 4.3 illustrates the IV characteristics of a Schottky contact (similar to a gate contact). The non-linear behaviour of the gate is similar to a diode behaviour. When the diode is under forward bias, large currents will flow when a voltage greater than the on-voltage is applied due to thermionic emission. On the other hand, when the diode is under small negative bias, small leakage currents occur due to field emission, while under large negative bias, field emission becomes larger and hence causes large current flow known as breakdown. Conventional GaN based devices are depletion-mode and require a negative bias on the Schottky gate electrode. Varying the gate voltage (e.g. with a superimposed ac signal) varies the 2DEG carrier concentration under the gate (through the electric field capacitive action), hence the output transistor current, the drain-source current can be modulated.

4.2.2 Ohmic contacts theory

Ohmic contacts exhibit linear transfer characteristics due to field emission. Field emission is controlled by the magnitude and width of the barrier. The width of the barrier can be decreased by increasing the doping in the semiconductor. GaN is usually heavily

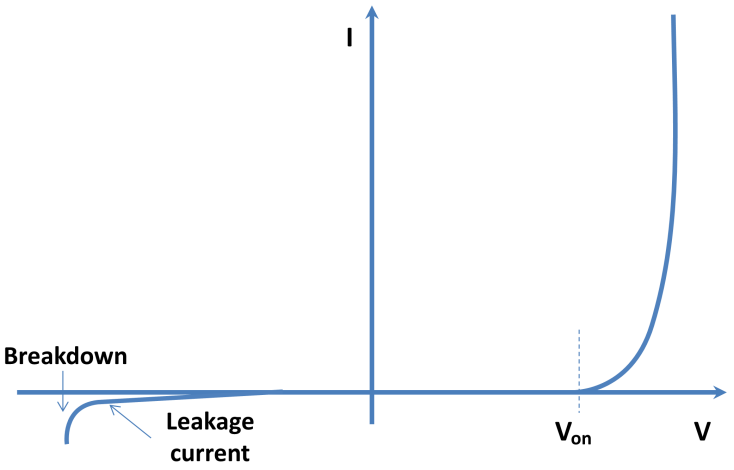

FIGURE 4.3: Typical IV characteristics for a Schottky contact.

doped with silicon at a typical doping densities of up to 1×10^{20} cm^{-3} to achieve low Ohmic contacts [103]. The barrier magnitude can be decreased by reducing the bandgap. The lower the bandgap, the easier the electron transport across the barrier, resulting in lower Ohmic contact resistance.

4.3 Transmission line model

Transmission line model (TLM) is commonly used to extract the Ohmic contact resistance. There are two transmission line models; the Linear Transmission Line Model (LTLM) and the Circular Transmission Line Model (CTLM). LTLM structures require mesa etching to isolate the surroundings of the metal contacts, and therefore prevent fringing currents from flowing at the surroundings of the metal contacts. On the other hand, CTLM structures do not require mesa etching as the active area is enclosed in circles, which means that only one lithography step is required.

4.3.1 Linear Transmission Line Model (LTLM)

The linear transmission line model was proposed by Reeves & Harrison [104]. The model, illustrated in Figure 4.4, consists of a series of Ohmic contacts that have the same width and separated by different gap spacings, L_x. The increasing gap spacing corresponds to increasing semiconductor series resistance.

Once the Ohmic contacts are fabricated, a four-probe measurement setup is used to measure the total resistance between consecutive pair of pads, where the current is

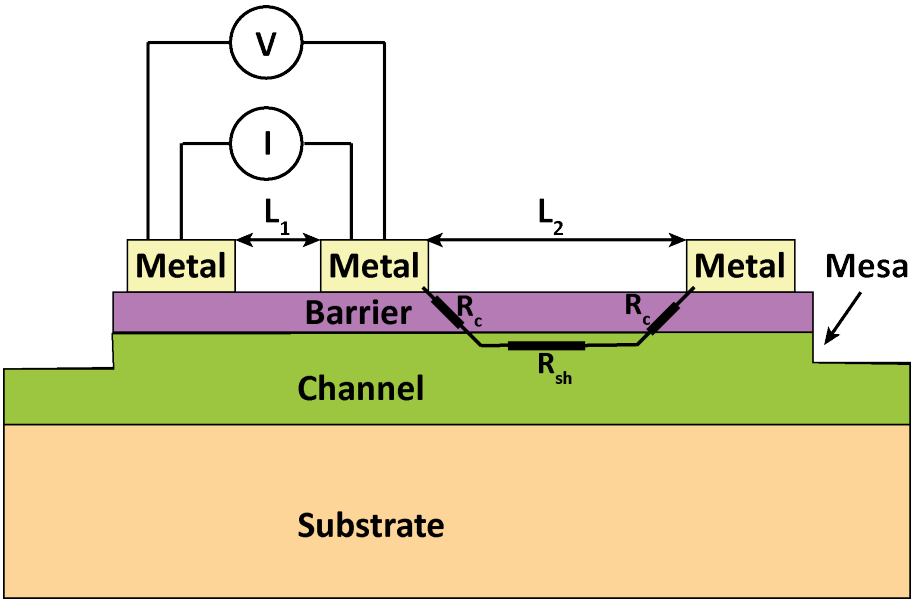

FIGURE 4.4: Cross section of an LTLM structure.

applied through one pair of probes and the voltage is measured by the other pair. This allows for the effect of the resistance of the probes and system cables to be reduced. The measured resistance is then plotted as a function of the gap spacing as illustrated in Figure 4.5, from which the Ohmic contact resistance and the material/semiconductor sheet resistance can be extracted.

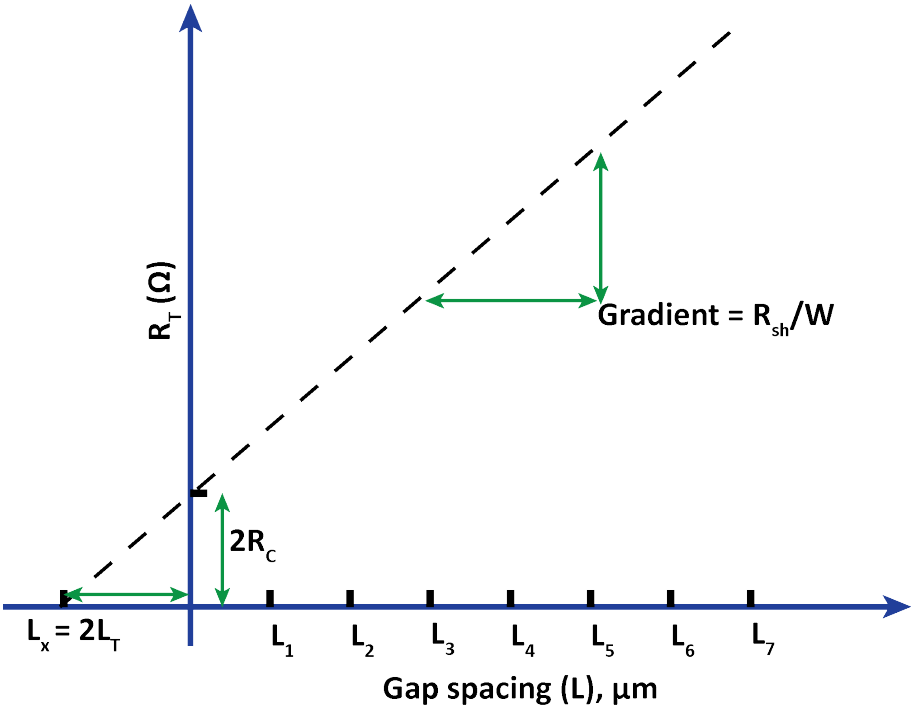

FIGURE 4.5: Total resistance versus the varying gap spacings.

From the illustration in Figure 4.4 we can derive the total resistance between two consecutive contacts to be:

$$R_T = 2R_c + R_{ch} = 2R_c + \frac{R_{sh}.L}{W} \tag{4.2}$$

where R_c is the contact resistance, R_{ch} is the channel resistance, R_{sh} is the sheet resistance, L is the separation between two adjacent contacts and W is the contact width.

The intercept with the y-axis yields $2R_c$ which is the contact resistance. Multiplying R_c with W yields the normalised contact resistance, R_c (Ω·mm). For semiconductors in general, the transfer length, L_T, which denotes the part of the pads through which the current enters or leaves, can be extracted from the intercept with the x-axis as:

$$L_x = 2L_T \tag{4.3}$$

where the sheet resistance between the metal pads is assumed to be equal to the sheet resistance under the metal. This assumption is not valid in the case of GaN technology as the Ohmic contacts are usually annealed at high temperatures to allow the Ti in the contact metal to react with the nitrogen in the barrier, forming TiN. This results in a reduction in barrier thickness which causes the sheet resistance under the metal to change.

4.3.2 Circular Transmission Line Model (CTLM)

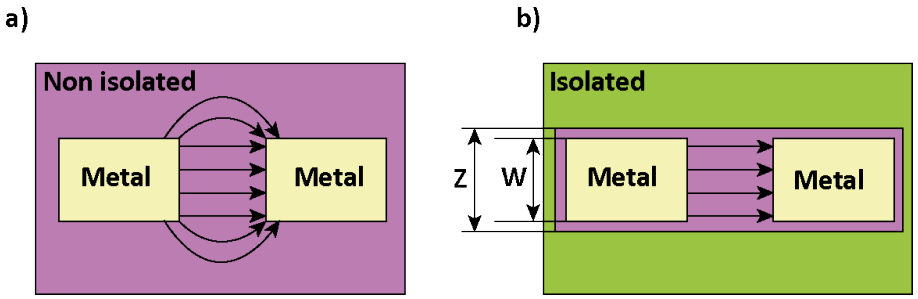

FIGURE 4.6: Current flow in an LTLM structure (a) non-isolated and (b) isolated structures.

LTLM structures require mesa isolation to confine the current between the pads. This is illustrated in Figure 4.6 which shows the electric fields for non-isolated and isolated mesa pads. The importance of the mesa isolation comes from the fact that it confines the current in the channel preventing fringe currents from flowing. As a result, more accurate extraction of R_C and R_{sh} can be obtained. Since GaN HEMTs exhibit low sheet resistances of 300 Ω/□, fringing currents can result in errors of up to 66%.

CTLM structures solve the fringing fields problem easily. The CTLM technique requires only one lithography step compared to two lithography steps required for LTLM structures. Since CTLM structures have the inner contact circled by the outer contact, the current flowing between the two contacts is confined and it is not possible for fringing currents to occur. Therefore, mesa isolation is not required for CTLM structures. Reeves proposed the concentric circular contacts [105]. It had the disadvantage that the current passed under the middle circles to reach the outer circles while assuming that the sheet resistance of the semiconductor between the contacts equals that under the metal contacts which was not accurate. Marlow followed by a new model of a single contact enclosed by a circle to omit Reeves design flaw [106].

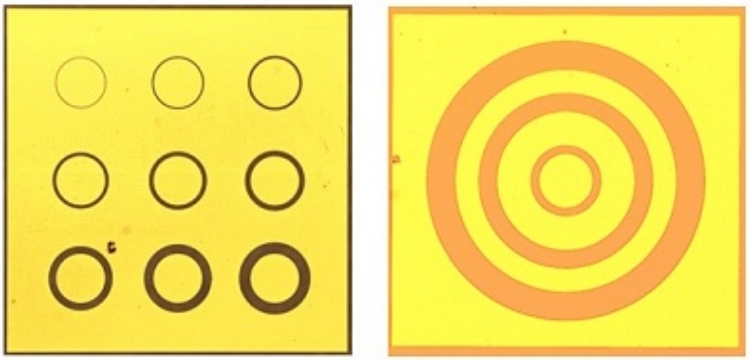

FIGURE 4.7: Illustration of a) Reeves concentric circular contacts and b) Marlow's enclosed contacts.

The method used for extracting the contact resistance from the CTLM structures is identical to the method used to extract the contact resistance from the LTLM structures. One exception is the requirement for a correction factor to be applied for data measured using CTLM structures since the circumference of the inner circle is not equal to the circumference of the outer circle, and hence the correction factor is needed to get a linear fit [107]. The correction factor depends on the gap size and is calculated as follows:

$$C = \frac{R_1}{s} ln \frac{R_1 + s}{R_1} \tag{4.4}$$

where R_1 is the radius of the inner circle and s is the gap spacing. Correction factors versus gap spacing for $R_1 = 100$ μm are listed in Table 4.1:

Gap spacing (μm)	4	8	12	16	20	24	32	40	48
Correction factor (C)	0.98	0.96	0.94	0.92	0.91	0.90	0.87	0.84	0.82

TABLE 4.1: Gap spacings with their equivalent correction factor.

4.4 Literature review of GaN-based Ohmic contacts

Historically, Ti/Al Ohmic contacts were made on n-GaN material where the Ti extracts the N atoms out of the GaN to form TiN interface layer [108, 109]. The N vacancies created in GaN are the electrically active donors responsible for the Ohmic contact behaviour. The active donors act as n-doping which reduces the barrier width and eases the tunneling of electrons through the barrier [110]. However, on AlGaN, Ti cannot create the electrically active N vacancies in AlGaN/GaN. This is due to the fact that the enthalpy of formation of GaN, TiN and AlN is -110.9, -265.5 and -318.1 KJ/mol, respectively. The AlGaN blocks the Ti from bonding with the N in the AlGaN due to the stronger bond of -318.1 KJ/mol of AlN compared to -265.5 KJ/mol of TiN [111]. This leads to the Ti to alloy with the Al in the metal scheme to form Al_3Ti leaving the AlGaN intact and resulting in high Ohmic contact resistance. Therefore, the conventional process using Ti/Al contacts cannot be simply transferred from n-type GaN to AlGaN/GaN structures. This can be solved by introducing SiN_x on top of the AlGaN barrier. The SiN_x will act as a passivation layer and will also enable the Ti to extract the N vacancies from the passivation layer forming TiN that provides the active electrical donors necessary for allowing the electrons to tunnel through the barrier. This leads to an Ohmic behaviour. A TEM of the TiN layer formed after annealing Ti/Al metal stack deposited on top of an in-situ SiN_x at 800°C is reported in [112] and illustrated in Figure 4.8.

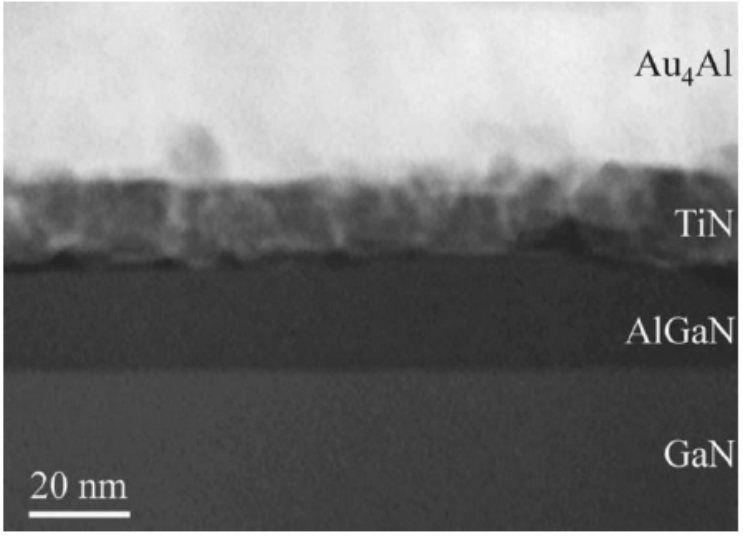

FIGURE 4.8: TEM of TiN formed after high temperature annealing.

Ti/Al/Ni/Au metal stack was shown to exhibit better Ohmic behaviour on AlGaN/GaN structures compared to Ti/Au contacts, and hence became the conventional metal stack

used in the formation of Ohmic contacts for GaN HEMTs [113]. The typical thicknesses for the Ti/Al/Ni/Au metal stack was optimised to 30/180/40/100 nm [114]. When as-deposited, they exhibit a Schottky behaviour with non-linear characteristics. To achieve an Ohmic behaviour (linear), the metal stack must be annealed at a high temperature, typically ≥800°C. The behaviour changeas from Schottky to Ohmic due to the high temperature anneal (800°C) as shown in Figure 4.9. The role of each metal in the conventional Ohmic metal stack is described below:

- **Titanium (Ti)** will react upon the high temperature anneal with the nitrogen in the GaN layer to form TiN that acts as a highly n-type doped region. This will reduce the width of the barrier allowing more electrons to flow across the barrier, resulting in a higher current density.
- **Aluminium (Al)** will react with Ti to form an Al_3Ti layer that prevents the oxidation of the underlying layer [111] and helps in the Ohmic contact formation [115].
- **Nickel (Ni)** is the diffusion barrier between the gold layer at the top and the Al layer at the bottom to prevent the formation of a highly resistive alloy known as purple plague [114].
- **Gold (Au)** is used to enhance the electrical contact between the contact and the measurement probes [113].

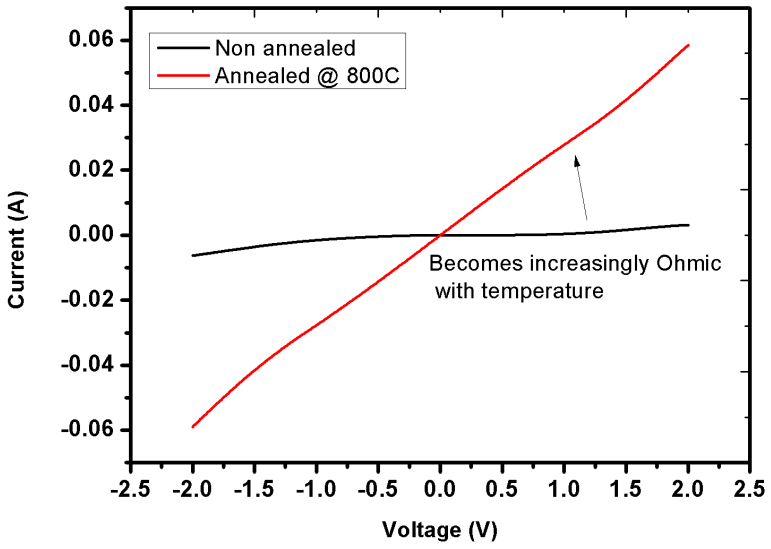

FIGURE 4.9: Measured TLM pattern before and after annealing.

For the AlGaN/GaN material system, several techniques to achieve low Ohmic contact resistances have been reported. These include the optimisation of the metal stack resulting in an Ohmic contact resistance of 0.2 Ω·mm [114], using a self-aligned recessed Ohmic contacts which resulted in an Ohmic contact resistance of 0.15 Ω·mm [27] and highly doping the GaN cap layer with silicon that resulted in a non-alloyed Ohmic contact resistance of 0.2 Ω·mm [25]. A good review of Ohmic contacts on AlGaN/GaN can be found in [116].

Several techniques are also described in the literature to achieve low Ohmic contacts to AlN/GaN. The same metal stack as for AlGaN/GaN was used. All the methods involve preparation of the AlN surface prior to metallisation, and include direct deposition [117], special surface cleaning and/or wet chemical etching [112, 118], and dry etching using RIE [119]. These techniques resulted in Ohmic contact resistances of 1.1 Ω·mm [117] and 0.5 Ω·mm [112, 118]. Ohmic regrowth is another technique, where the AlN barrier is etched away from the contact areas in which highly doped n-type GaN is grown [120]. Very low Ohmic contact resistances of 0.15 Ω·mm were achievable even though the technique adds complexity to the processing.

An unusual approach to realise Ohmic contacts was recently reported for AlGaN/GaN devices passivated with an in-situ SiN_x layer. It was reported that in-situ SiN_x helps reduce the Ohmic contact resistance on the AlGaN/GaN material system [121]. The Ohmic metallisation was deposited directly on the SiN_x cap layer. Unlike in conventional Ohmic contacts where the metallisation is deposited on the GaN cap layer, it was suggested that, in this case, the N in the SiN_x rather than the AlGaN barrier resulting in N vacancies that create a conducting channel through the AlGaN barrier. This technique of using SiN_x was adopted to realize low resistance Ohmic contacts on AlN/GaN HEMTs for this project. The SiN_x also serves to protect the sensitive AlN barrier from processing solutions. The experimental work and the achieved results are described in section 4.6.

4.5 Ohmic contact optimisation on AlGaN/GaN

Achieving low Ohmic contact resistance is key to unleashing the full potential of any semiconductor material. At the start of the project, the focus was on exploring new ways to further reduce the Ohmic contact resistance on AlGaN/GaN material compared to the lowest published contact resistance of 0.15 Ω·mm [27]. The conventional AlGaN/GaN HEMT structure was also used initially for process development and optimisation. The material consisted of the following epi-layers: 2 nm GaN cap layer followed by a 20 nm $Al_{0.25}Ga_{0.75}N$ barrier layer and a 3 μm channel on a sapphire substrate. Using Hall

measurements (by the grower), the material was determined to have an electron mobility of 1400 $cm^2/V{\cdot}s$ and a 2DEG sheet carrier concentration of $1x10^{13}$ cm^{-2}. In this work, CTLM structures were used to analyse the recessed Ohmic contact performance of all processed samples. Nine circles with gap spacing's ranging from 4 μm to 48 μm, as shown in Figure 4.10, were used in the extraction of the Ohmic contact resistance values. The process flow of the CTLM fabrication is illustrated in Figure 4.11. A key feature of the Ohmics was that the AlGaN barrier was etched and removed prior to metal deposition. This was expected to enable a side contact to the 2DEG channel or contact via the GaN buffer layer. From the CTLM structure, the lowest extracted contact resistance, R_C, for AlGaN/GaN HEMT was 0.079 $\Omega{\cdot}$mm from the data plotted in Figure 4.12. This result was however not repeatable due to the variation in etch rates between the different dry etch runs. The typical contact resistance achieved of a recessed Ohmic contact on the AlGaN/GaN material system was in the range of 0.2-0.4 $\Omega{\cdot}$mm.

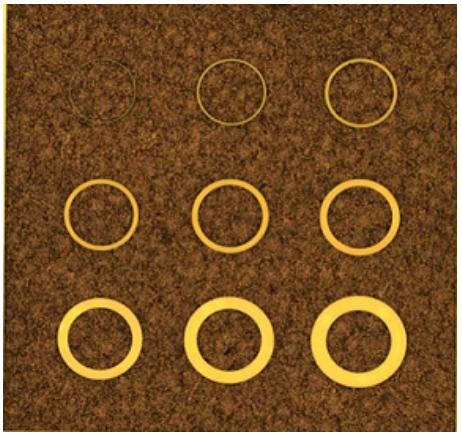

FIGURE 4.10: Micrograph of a fabricated CTLM structure.

Thorough testing was conducted to optimise the etch depth and annealing temperature. The Dektak and AFM surface profiler were used to determine the etch depths but this was not easy to do. The difficulty of determining the etch depth arose from the fact that the required etch depth is shallow (22 nm in AlGaN/GaN material) and was difficult to measure accurately. Furthermore, the dry etch rate seemed highly dependent on the chamber history.

The two-step fabrication technique was also investigated. The first step was to completely remove the barrier layer using dry etching, followed by depositing the overlapped Ohmic metal using a second lithography step. This is to ensure that the Ohmic metal overlapped the etch side wall to form a side contact with the 2DEG channel. This approach was also expected to reduce the annealing temperature and time as the Ohmic metal was in direct contact with the 2DEG channel. Characterising non-recessed and recessed CTLM structures on the same sample showed that the overlapping recessed

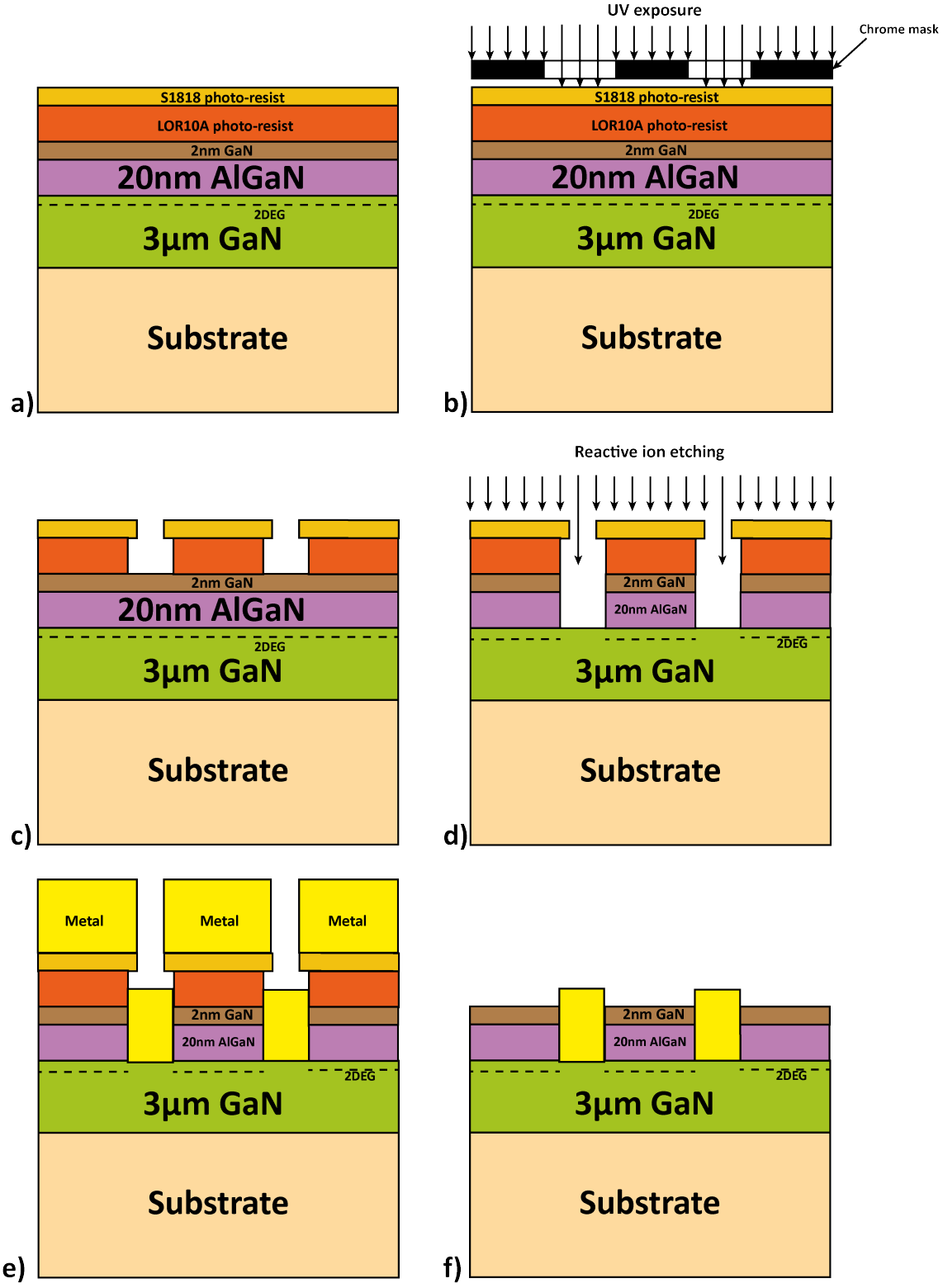

FIGURE 4.11: Process flow of a CTLM structure, a) LOR10A photo-resist spinning followed by S1818 photo-resist spinning, b) UV exposure for 6 seconds, c) development using MF319 for 2:30 min:sec, d) reactive ion etching using $SiCl_4$ with a power of 75 W, flow rate and pressure of 30 sscm and 30 mT, respectively, e) metallisation of Ti/Al/Ni/Au (30/180/40/100 nm) and f) lift-off using 1165 photo-resist stripper.

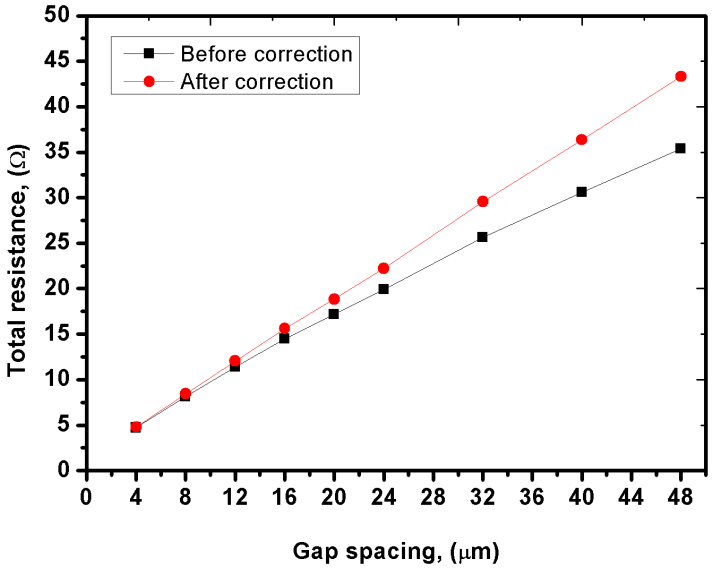

FIGURE 4.12: Measured resistance versus gap spacing.

structure did not offer any advantage, and hence both CTLM structures exhibited the same Ohmic contact resistance. A possible explanation for this result is illustrated in Figure 4.13 where in a) the annealing of the metal causes the 2DEG channel underneath the metal stack to be depleted. In Figure 4.13b there is an overlap of 2 μm between the metal stack and the active AlGaN barrier which is larger than the typical 1 μm transfer length of the contact in GaN. Therefore, the current effectively passes through the barrier rather than the side contact of the metal overlapping the depleted 2DEG.

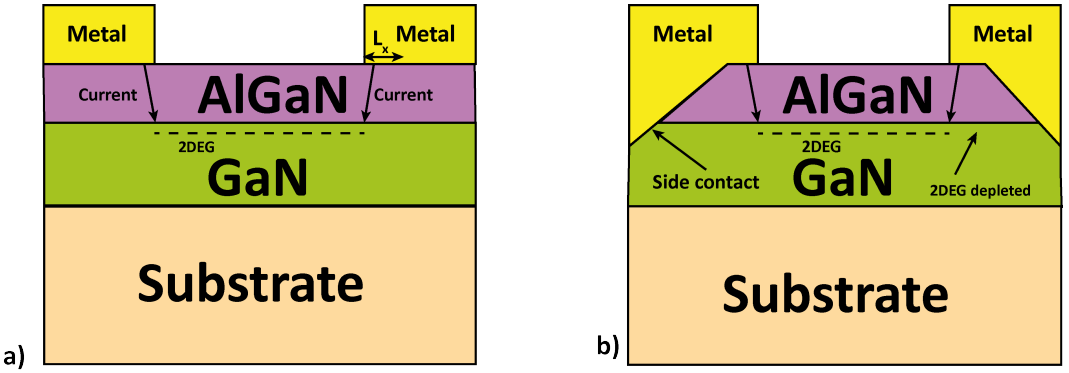

FIGURE 4.13: Illustration of the a) non-recessed and b) recessed Ohmic contacts after annealing. Both contacts exhibited similar contact resistances.

4.6 Ohmic contact optimisation on AlN/GaN

Two different AlN wafers from two different suppliers were used for Ohmic contact optimisation on AlN/GaN material. One was grown using MBE by SVT Associates and the surface was unprotected while the other was grown using MOCVD by EpiGaN Ltd with an in-situ SiN_x surface passivation. The two wafers will be be referred to as wafer 1 and wafer 2 respectively. Wafer 1 was grown by molecular beam epitaxy (MBE) on (0001) sapphire substrate. Using Hall measurements (by the grower), the material was determined to have a mobility of 1450 $cm^2/V{\cdot}s$ and a 2DEG sheet carrier concentration of 1.7 x 10^{13} cm^{-2}. The material consisted of the following epi-layers: 1 nm GaN cap layer followed by a 3 nm AlN barrier and a 3 μm GaN channel on sapphire substrate. Earlier work carried out in the project showed that the surface of the thin AlN was sensitive to processing solutions such as acetone, and iso-propanol, and hence the only cleaning mechanism allowed was reverse osmosis (RO) water. This introduced a new challenge when cleaving the wafer since photo-resist is usually used to protect the surface. Cleaving the wafer with no photo-resist results in surface contamination. The use of acetone is required to remove the photo-resist after the cleaving process which affects the thin AlN barrier. Therefore, wafer 1 was cleaved with no photo-resist protection and was only cleaned with RO water. Wafer 2 was grown by MOCVD and had the following epi-layers: 5 nm in-situ SiN_x followed by a 3 nm AlN barrier and a 1.3 μm GaN channel on a SiC substrate. From Hall measurements the wafer was determined to have a sheet resistance of 300 $\Omega/\square$. The cross section of wafers 1 and 2 is illustrated in Figure 4.14.

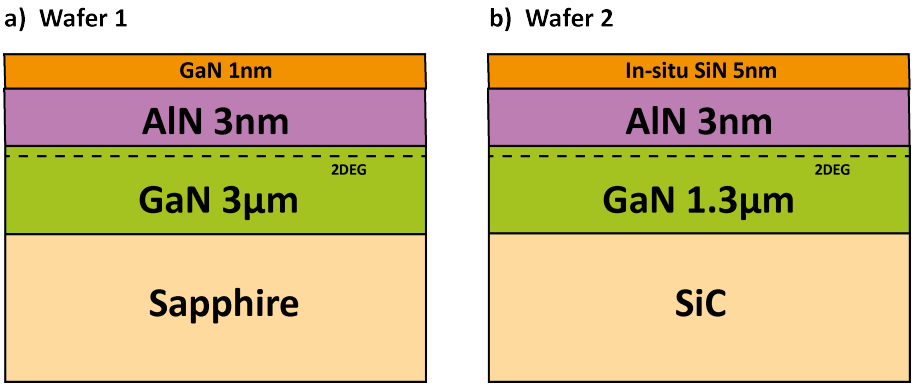

FIGURE 4.14: Cross section of a) an MBE grown AlN/GaN HEMT on sapphire and b) an MOCVD grown AlN/GaN HEMT on SiC.

Wafer 1 was processed at the early stage of the project when the recessed Ohmic contacts were under investigation. It was processed using the same process flow described in Figure 4.11, apart from the etch time which was 10 seconds since the AlN barrier is only

3 nm compared to the 20 nm of the AlGaN barrier. The extracted R_C value for wafer 1 was 0.6 Ω·mm using the optimised Ohmic contact processing.

Wafer 2 was processed towards the end of the project using the non-recessed Ohmic contact approach, where the SiN_x layer was left intact under the Ohmic metal. The metal was deposited directly on top of the SiN_x layer and then the wafer was cleaved into 12 small samples to be annealed at different times and temperatures. The processing was done as follows: a) standard sample cleaning using acetone and iso-propanol, b) spinning LOR10A and S1818 photo-resists, followed by exposure and development, c) Ohmic metal deposition: Ti/Al/Ni/Au (30/180/40/100 nm), d) wafer cleaving into 12 samples and annealing at different temperatures of 750°C, 800°C, 850° and 900°C, and for each temperature the samples were annealed at different times of 15, 30 and 45 seconds.

Figure 4.15 shows the extracted contact resistances at the different RTA conditions. At 750°C, the contact resistance is relatively high for the three annealing times. At temperatures above 800°C, the metal stack degrades resulting in higher contact resistances. The sheet resistance also increases at annealing temperatures >800°C to reach 370 Ω/□. At the annealing temperature of 800°C the sheet resistance remains at 300 Ω/□, and a contact resistance of 0.4 Ω·mm is achieved at an annealing time of 30 seconds.

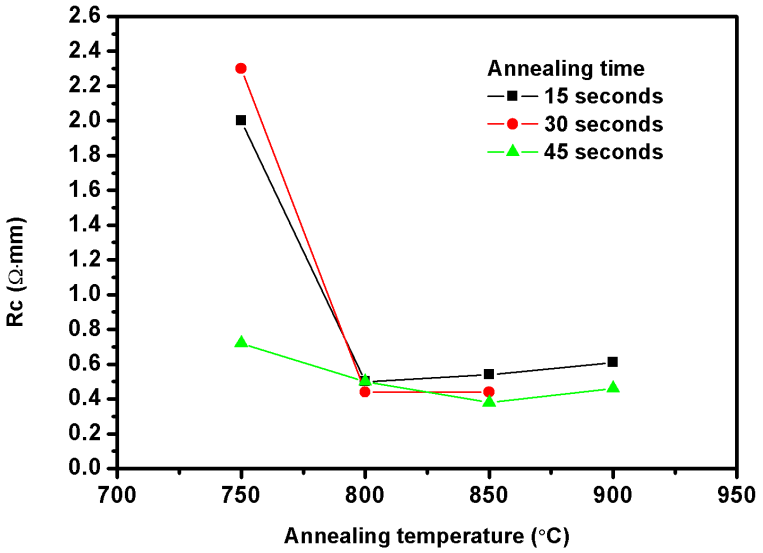

FIGURE 4.15: Measured contact resistances under different RTA conditions.

To compare this result with earlier approaches, the in-situ SiN_x was removed from the contact areas prior to metal deposition using a low damage RIE process with the following parameters: SF_6 gas with a flow rate of 25 sccm, chamber pressure of 15 mT

and a power of 20 W. The extracted contact resistance in this case was 0.7 Ω·mm. This result indicates that the in-situ SiN_x also plays an important role in the formation of the Ohmic contacts on the AlN/GaN HEMT material, as was earlier found for AlGaN/GaN HEMTs [121]. The optimised measured contact resistance of 0.4 Ω·mm is one of the best achieved resistances on AlN (excluding using regrowth technique) compared to state of the art published work. Figure 4.16 illustrates a comparison between Ohmic contacts optimised for this work and other published Ohmic contacts for AlN/GaN material system.

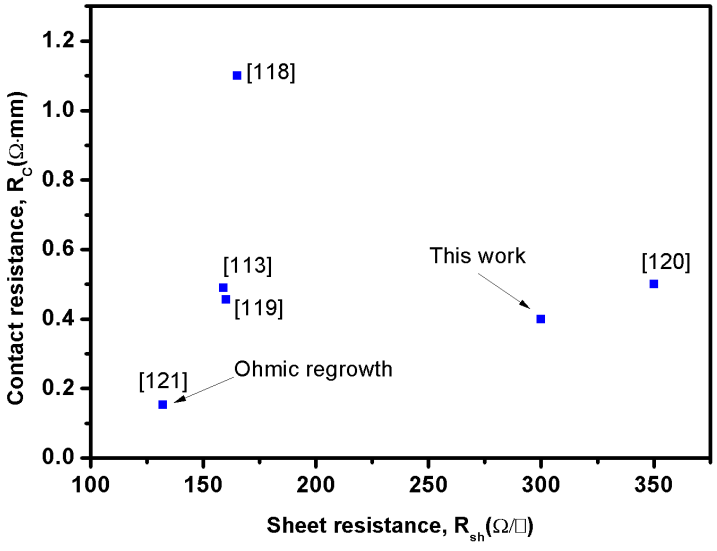

FIGURE 4.16: Comparison of Ohmic contacts on AlN/GaN optimised for this work and other published work.

4.7 Device performance using optimised Ohmic contacts

This section compares between the AlN/GaN and AlGaN/GaN HEMT material systems in terms of device performance.

4.7.1 Comparison of AlN/GaN and AlGaN/GaN HEMTs on sapphire

The recessed Ohmic contacts were used to fabricate DC devices on AlN/GaN and AlGaN/GaN HEMT material systems. Both devices employed a 10 nm PECVD SiN_x passivation layer. Figure 4.17 illustrates the schematic cross-section of the AlN/GaN and AlGaN/GaN MIS-HEMTs employing recessed Ohmic contacts.

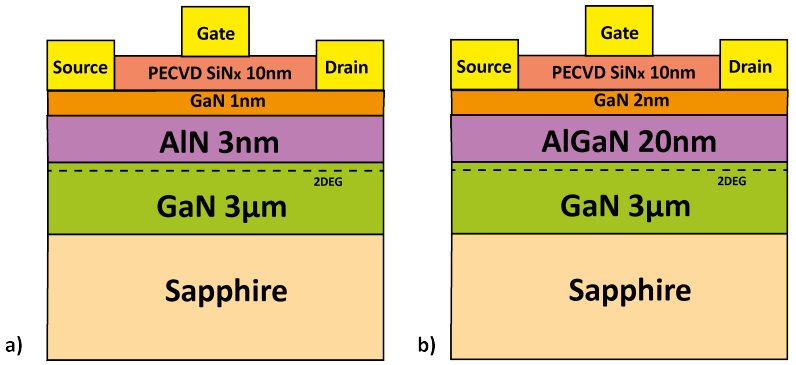

FIGURE 4.17: Cross section of a) MBE grown AlN/GaN HEMT on sapphire and b) MOCVD grown AlGaN/GaN HEMT on sapphire.

The device layout employed a gate width, W_G, of 100 μm, a gate length, L_G, of 1.5 μm, a source-drain distance, L_{SD}, of 8.5 μm and a gate-drain distance, L_{GD}, of 4 μm. The same mask was used for both AlGaN/GaN and AlN/GaN devices to make a consistent comparison. All fabrication was done using photolithography. The device processing was as follows: (a) Sample cleaning using acetone, iso-propanol and rinsing with de-ionised water, (b) deposition of 10 nm PECVD SiN_x, (c) lithography definition of the Ohmic contact areas (d) removing the PECVD SiN_x using CHF_3:O_2, (e) etching the AlN and AlGaN barriers using $SiCl_4$ for 10 seconds and 3:30 min:sec, respectively, (f) Ohmic metallisation using Ti/Al/Ni/Au (30/180/40/100 nm) followed by annealing using RTA at 800°C for 30 seconds, (g) gate metallisation using Ni/Au (20/200 nm). DC measurements were done at room temperature using Agilent's B1500A semiconductor device analyser.

CTLM structures were used to extract the contact and sheet resistances of the AlN/-GaN and AlGaN/GaN HEMTs which were found to be 0.6 Ω·mm, 160 Ω/□ and 0.4 Ω·mm, 450 Ω/□, respectively. Figures 4.18 and 4.19 show the output IV characteristics of a fabricated 1.5 μm x 100 μm AlN/GaN and AlGaN/GaN MIS-HEMTs, respectively. The AlN/GaN MIS-HEMT exhibits higher drain current densities of up to 1900 mA/mm compared to 1100 mA/mm of AlGaN/GaN MIS-HEMT at a gate bias of +2 V. Both devices exhibited good pinch off and good saturation characteristics. The results demonstrate the potential for AlN/GaN structure to deliver double the current density compared to the AlGaN/GaN structure. The trade-off is the added thermal dissipation in the AlN/GaN system due to the higher current density which makes thermal management more important. The current densities exhibited by the AlGaN/GaN and AlN/GaN devices fabricated during this project are comparable to the state of the art devices [34, 117]. The higher the current densities means smaller device sizes are

required in power amplifier circuits which is highly desirable since smaller device size means less parasitics which translates into easier circuit design.

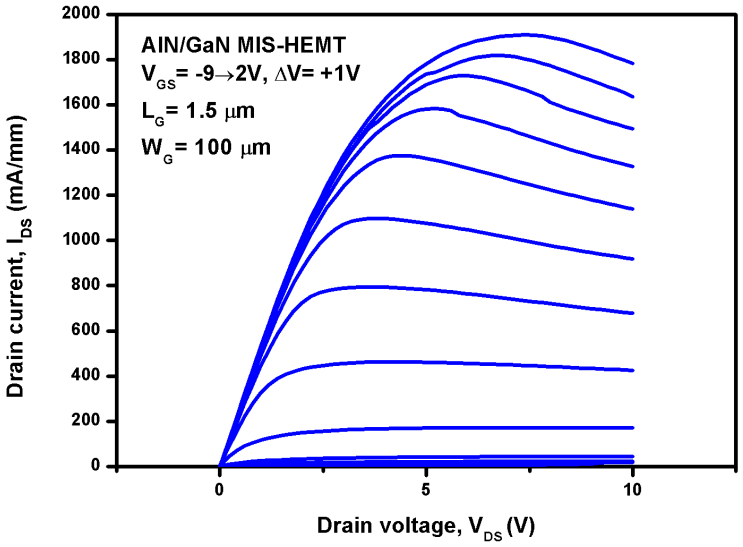

FIGURE 4.18: Output IV characteristics of the AlN/GaN MIS-HEMT on sapphire.

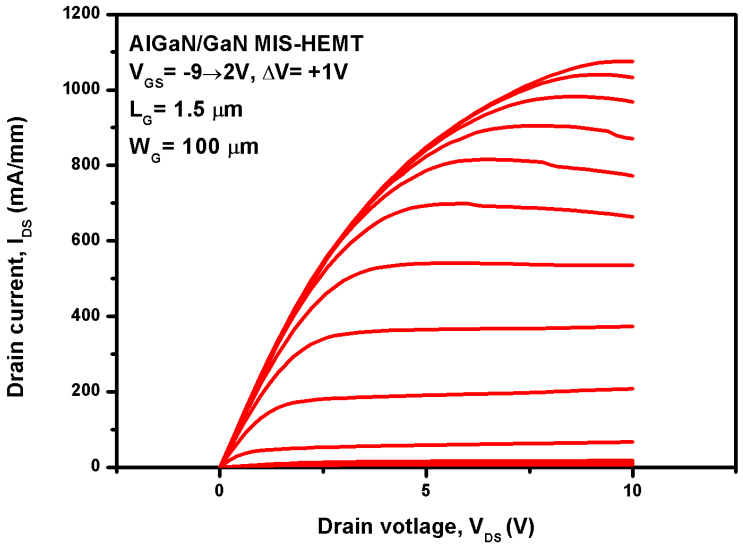

FIGURE 4.19: Output IV characteristics of the AlGaN/GaN MIS-HEMT on sapphire.

Figures 4.20 and 4.21 show the typical transconductance versus gate voltage (g_m - V_{GS}) characteristics of a fabricated 1.5 μm x 100 μm AlN/GaN and AlGaN/GaN MIS-HEMTs. The AlN/GaN MIS-HEMT exhibits higher transconductance of 330 mS/mm

compared to 160 mS/mm of AlGaN/GaN MIS-HEMT. The higher the transconductance, the higher cutoff frequency exhibited by the device in the RF domain and hence it is desirable to have a high transconductance. Since the transconductance is dependent on the gate capacitance and as the gate capacitance is partially determined by the barrier thickness, AlN/GaN HEMTs exhibit higher transconductance since the AlN barrier thickness is only 3 nm compared to 20 nm of AlGaN.

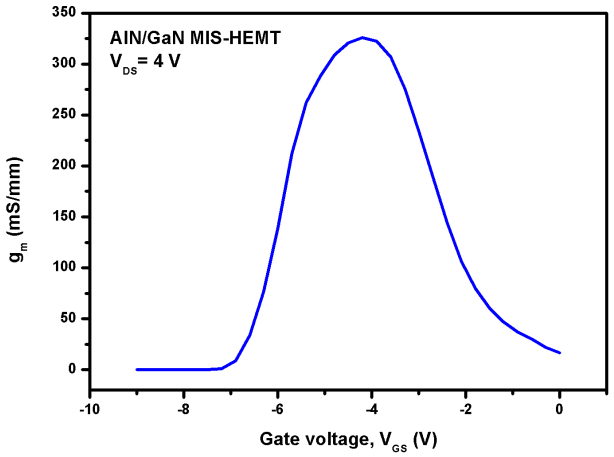

FIGURE 4.20: Transconductance (g_m) characteristics of the AlN/GaN MIS-HEMT.

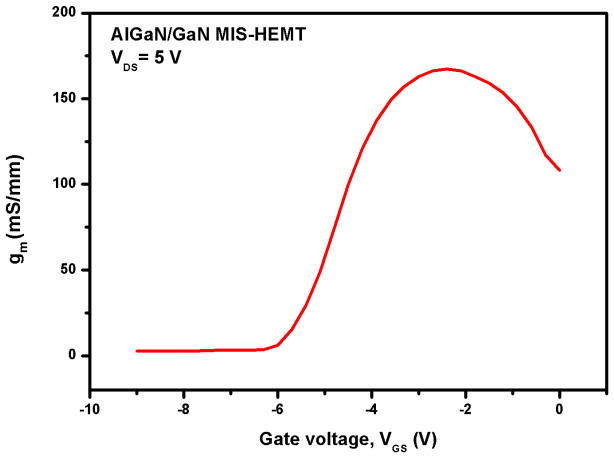

FIGURE 4.21: Transconductance (g_m) characteristics of the AlGaN/GaN MIS-HEMT.

4.7.2 Comparison of AlN/GaN and AlGaN/GaN HEMTs on SiC

On the SiC substrates, RF devices were fabricated both in the AlN/GaN and AlGaN/-GaN HEMT material systems. The Ohmic contact fabrication for the AlN/GaN material system was based on the new scheme employing in-situ SiN_x and using the optimised annealing temperature and time of 800°C and 30 seconds, respectively. The device layout employed a W_G of 2×200 μm, L_G of 3 μm, L_{SD} of 9 μm and L_{GD} of 3 μm. Device processing was done as follows: (a) Sample cleaning using acetone, iso-propanol and rinsing with de-ionised water, (b) Ohmic metallisation using Ti/Al/Ni/Au (30/180/40/100 nm) followed by annealing using RTA at 800°C for 30 seconds, (c) mesa isolation, (d) gate metallisation using Ni/Au (20/200 nm), (e) bond pad metallisation using Ti/Au (20/200 nm). The extracted contact and sheet resistances of the AlN/GaN and AlGaN/GaN HEMTs were 0.4 Ω·mm, 300 Ω/□ and 0.6 Ω·mm, 450 Ω/□, respectively. All fabrication was done using photolithography. Figure 4.22 illustrates the schematic cross-section of the AlN/GaN and AlGaN/GaN HEMT material systems on SiC.

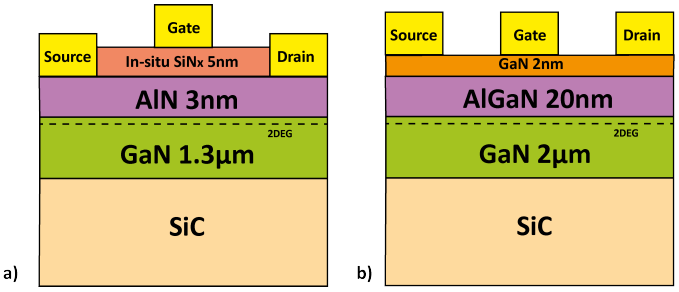

FIGURE 4.22: Cross section of a) MBE grown AlN/GaN HEMT on SiC and b) MOCVD grown AlGaN/GaN HEMT on SiC.

DC measurements were done at room temperature using Agilent's B1500A semiconductor devices analyser. Figures 4.23 and 4.24 show the output IV characteristics of the fabricated AlN/GaN and AlGaN/GaN HEMTs, respectively. The AlN/GaN HEMT exhibits a maximum drain current density of 700 mA/mm compared to 275 mA/mm of the AlGaN/GaN HEMT, both were measured at a gate voltage of 0 V. Clearly, the AlN/GaN HEMT delivers more than double the current density compared to the standard AlGaN/GaN structure. The lower current densities compared to the devices fabricated on sapphire are due to the fact that devices fabricated using the RF device layout are isolated, and therefore they offer more accurate current densities. RF device layouts had also longer gates of 3 μm compared to 1.5 μm of DC gate wrap-around devices. The layouts and processes for devices fabricated on SiC substrate were different from those used to fabricated devices on the sapphire substrates. Again, on SiC, the current densities exhibited by the AlN/GaN HEMTs are more than double the current densities

exhibited by the AlGaN/GaN HEMTs. Since SiC has a higher thermal conductivity of 400 W/mK compared to 35 W/mK of sapphire, there is no visible self heating effect and the drain bias needs to be pushed beyond 20 V for the self heating to kick in unlike the HEMTs on sapphire where the self heating is visible (as was shown in Figure 4.18) even at a drain bias of 10 V.

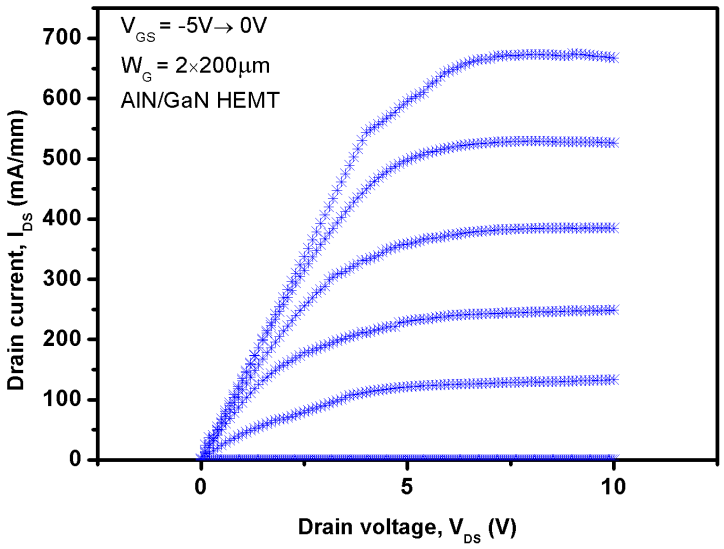

FIGURE 4.23: Output IV characteristics of the AlN/GaN MIS-HEMT on SiC.

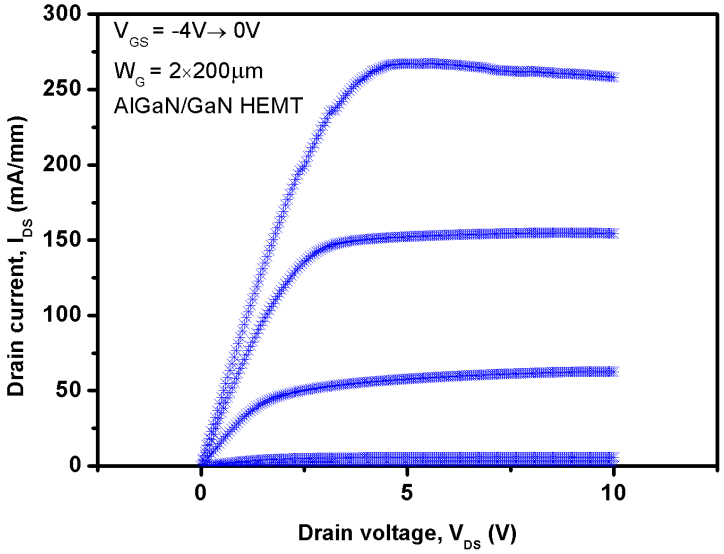

FIGURE 4.24: Output IV characteristics of the AlGaN/GaN HEMT on SiC.

4.8 Summary

This chapter described the basic metal-semiconductor interface theory and provided an overview of Ohmic contact technology on GaN. Circular TLM structures were used instead of linear TLM structures as they are simpler to fabricate and offer more accurate results. AlN/GaN material structure was demonstrated to exhibit double the current density compared to AlGaN/GaN material system. Due to the higher current density, a trade-off has to be made between current density and thermal dissipation in the AlN/GaN material system. Although the AlN/GaN material system offer superior performance compared to AlGaN/GaN, there are a couple of challenges associated with it; growth quality and Ohmic contact resistance. For this project, in-situ SiN_x was used to help protect the AlN barrier during processing and reduce Ohmic contact resistance by allowing the Ti in the metal scheme to extract N from the SiN_x to form TiN. Ohmic contact resistance of 0.4 Ω·mm was achieved on in-situ SiN_x passivated AlN/GaN material which is one of the best achieved resistances on AlN (excluding using regrowth technique) compared to state of the art published work. This result opens the door to realise RF power amplifiers in this material system. AlN/GaN HEMTs fabricated using the optimised Ohmic contact process exhibited a maximum drain current density of 700 mA/mm compared to 275 mA/mm of the AlGaN/GaN HEMT, both were measured at a gate voltage of 0 V. This demonstrated the superiority of the AlN/GaN material system compared to the AlGaN/GaN material system. The next chapter will describe a novel approach to realise AlGaN/GaN HEMTs with low leakage currents.

CHAPTER 5

Device Isolation Using Oxygen Plasma

5.1 Introduction

This chapter describes one of the main results of this research. A novel approach to achieve device isolation using oxygen plasma is proposed. It simplifies device processing and helps reduce gate leakage currents. Device isolation is required to electrically isolate adjacent devices from each other. Some device isolation techniques can lead to increasing gate leakage currents and also cause surface damage. Excessive gate leakage currents can deteriorate the noise performance in amplifiers and cause early breakdown of the devices [122]. Breakdown voltages can be improved either by adding a gate dielectric before depositing the gate metal [123] or employing field plates to suppress the electric field at the drain side of the gate [124]. Ideally the gate leakage current should be reduced without affecting the transconductance, g_m, or pinchoff voltage, V_p, of the device [125]. In this project, a new approach to achieve device isolation that helps in reducing the gate leakage currents without compromising the device transconductance is demonstrated.

5.2 Device isolation review

There are several ways that can be used to achieve device isolation, including mesa isolation, ion implantation and thermal oxidation. Ideally, the isolation choice should not compromise the gate leakage and surface leakage currents. The common isolation techniques are reviewed in the next sub-sections.

5.2.1 Mesa isolation

Mesa isolation is the simplest technique that is currently available for achieving device isolation. Using this technique, the active semiconductor layers between the devices are physically removed. The barrier is etched down to the insulating GaN buffer layer with a typical etch depth of 100-200 nm. Mesa isolation is not possible to achieve using wet etching since GaN has strong ionic bonds, making it resistant to most acids and bases. This makes wet chemical etching of GaN very difficult [126]. On the other hand, plasma etching techniques like reactive ion etching (RIE) [127] and inductively coupled plasma (ICP) [128] have been demonstrated to successfully achieve GaN etch rates of 200 nm/min and 600 nm/min respectively. The main gases used for etching GaN is a combination of BCl_3, Cl_2 and Ar. BCl_3 is used to de-oxidise the GaN during etching, offering a more uniform etching rate throughout [129]. Cl_2 is the main GaN etchant which is chemical-based, and Ar is a physical etchant of GaN which is usually used to increase the etch rate. $SiCl_4$ is another gas used to etch GaN which is based on chemical etching. High etch rates with anisotropic profiles and low surface damage can be achieved when optimising conditions like RF power, DC power, chamber pressure, gas flow rates and mixtures [130, 131]. For the early work done in this project, RIE was used for etching AlGaN/GaN epi-layers to achieve device isolation using the mesa technique. Figure 5.1 illustrates the structure of devices isolated using mesa isolation.

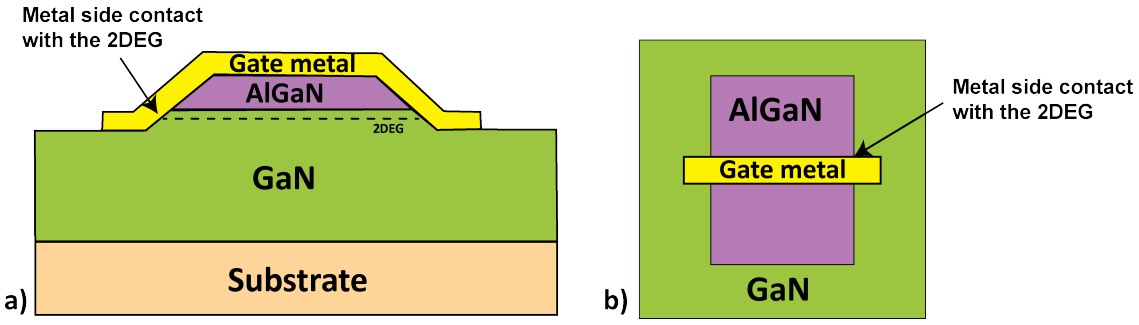

FIGURE 5.1: Strucutre of devices isolated using dry etch down to the GaN buffer, a) cross-section and b) top-view.

The issues associated with mesa isolation include the control and reduction of surface currents. Also, the gate metal lines along the conducting semiconductor layers at the mesa isolation edges. The control of the edged surface morphology is also important. The mesa process has the main disadvantage of resulting in a three dimensional device structure. This increases the complexity for the passive connection lines since they become susceptible to disconnection at the mesa edges. Mesa edges also increases gate leakage currents which limits high voltage isolation [132].

5.2.2 Ion implantation

Ion implantation is used to isolate devices by implanting ions that deplete the 2DEG channel. The benefit of using ion implantation technique for device isolation is that it is a planar process. Using this technique results in reducing leakage current and avoids the discontinuity in the gate metal. A good overview of the ion implantation process for GaN is explained in [133]. Critical parameters for ion implantation include ion mass, ion energy and implantation temperature. Figure 5.2 illustrates the structure of devices isolated using ion implantation.

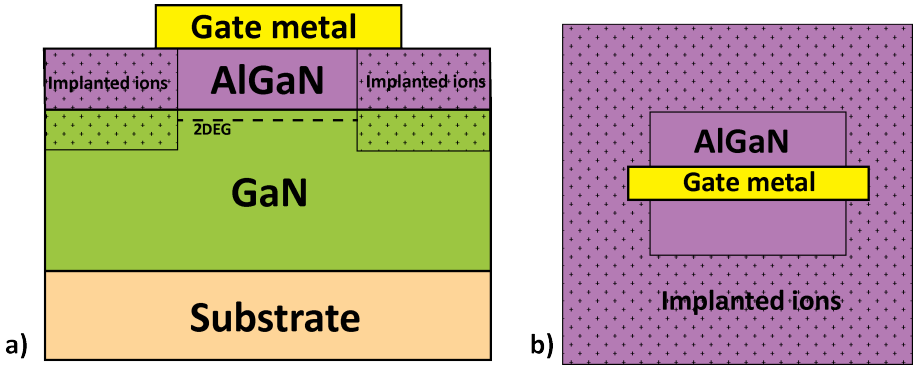

FIGURE 5.2: Structure of devices isolated using ion implantation, a) cross-section and b) top-view.

Ion implantation has been reported by many different groups. The use of many different ion species was reported, including nitrogen [134], oxygen [135], zinc [136], argon [137], magnesium [138], boron [139], krypton [140] and iron [141]. The effect of using hydrogen, helium and nitrogen ions for implantation was also reported [142]. The effect of using hydrogen, helium and argon ions on the resistivity of GaN is reported in [143]. A good comparative study showing the advantage of ion implantation over mesa isolation is reported in [33]. The study shows that devices fabricated with ion implantation show similar DC performance to the devices with mesa isolation, while exhibiting a higher breakdown voltage of 150 V for the same gate-to-drain distance of 10 μm.

5.2.3 Thermal oxidation

Thermal oxidation is based on the high temperature oxidation of GaN. The wafer is exposed to a high temperature of around 900°C for 30 minutes as reported in [144, 145]. Figure 5.3 illustrates the structure of devices isolated using thermal oxidation.

A thermal oxidation process done in Glasgow for locally oxidising the GaN beneath the gate metal was also reported [146]. This depletes the channel under the gate which helps

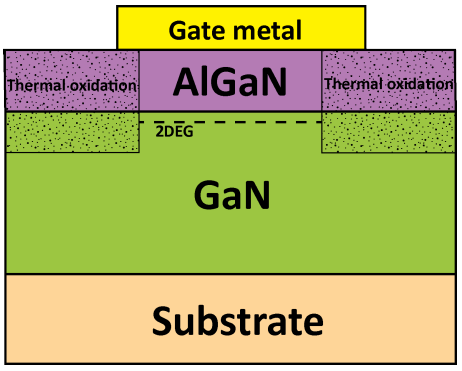

FIGURE 5.3: Structure of devices isolated using thermal oxidation.

in achieving normally-off operation. The thermal oxidation process is planar and has similar advantages to ion implantation. However, since the process exposes the sample to high temperatures for long durations, it is considered to be harsh and has not been a very popular technique to isolate GaN devices.

5.3 New approach to device isolation

In this project, a novel way to achieve device isolation was developed. Instead of the conventional RIE process, an oxygen plasma treatment is used to achieve device isolation. Compared to the conventional RIE process, the new process is simpler and does not compromise the gate leakage current. The new process results in a planar device that exhibits the characteristics of devices isolated using ion implantation. It saves the cost for the implantation process and avoids the disadvantage of exposing the sample to high temperatures, which is the case for thermal oxidation. The new approach was discovered when, during the project, it was noted that exposing the surface of unpassivated devices to oxygen plasma (to remove the residual photo-resist), caused the sheet resistance to significantly increase, thus reducing the drain currents. Therefore, a process for device isolation using oxygen plasma treatment was developed where the 1 μA/mm drain leakage currents exhibited by mesa isolated devices were used as a benchmark. Figure 5.4 illustrates the structure of devices isolated using oxygen plasma treatment.

5.4 Mesa and oxygen plasma isolation: process details

This section describes the device isolation process flow for both mesa isolation and oxygen plasma treatment. The mesa isolation is based on dry etching while oxygen plasma treatment is based on the surface treatment of the areas to be isolated using

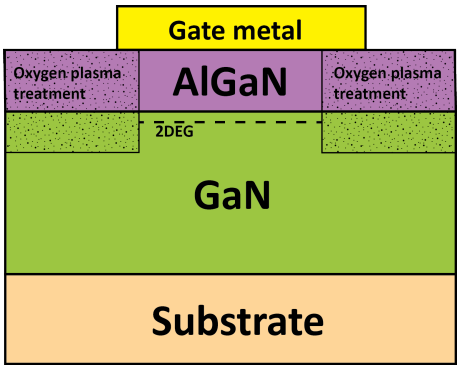

FIGURE 5.4: Structure of devices isolated using oxygen plasma treatment.

oxygen plasma. The process flow of the two techniques are demonstrated to show the simplicity of the new technique compared to the conventional mesa isolation.

5.4.1 Mesa isolation process

Figure 5.5 illustrate the process flow for the device isolation technique using mesa etching. The optimised $SiCl_4$ based RIE technique available at the JWNC was used. It had the following parameters: power of 200 W, gas flow rate of 25 sccm and chamber pressure of 8 mT. The etching time was 4 minutes and resulted in an etch depth of 160 nm. The process flow was as follows:

1. Sample cleaning using acetone and isopropanol.
2. Spinning S1818 photo-resist at 4000 rpm for 30 seconds.
3. Sample baking using hotplate at 110°C for 2 minutes.
4. Sample exposure to UV light using the MA6 mask aligner for 6 seconds.
5. Development using 1:1 Microdeveloper:H_2O for 45 seconds.
6. Photo-resist ashing using BP80 RIE tool with a power of 60 W, oxygen gas flow rate of 20 sccm and pressure of 20 mT for a duration of 3 minutes.
7. Sample hard-baking in oven at 90°C for 2 minutes.
8. Dry etching for mesa isolation using T-gate RIE tool.
9. S1818 photo-resist stripping using acetone in hot bath for 15 minutes.
10. Verifying the etch depth using Dektak profilometer which should be 160 nm.

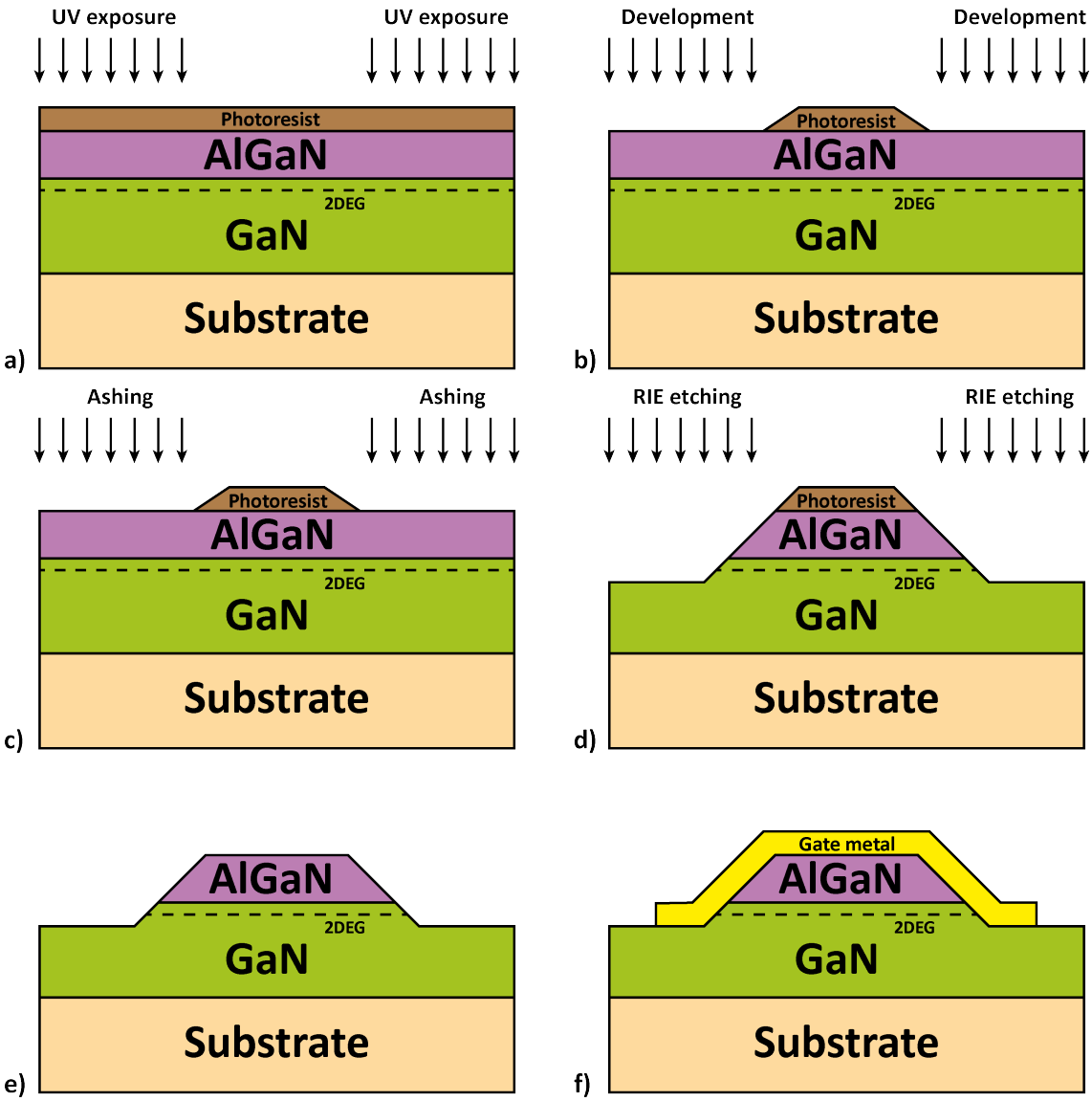

FIGURE 5.5: Mesa isolation process flow: a) photo-resist spinning and UV exposure, b) development, c) photo-resist ashing, d) RIE etching, e) photo-resist stripping and f) gate metal deposition.

5.4.2 Oxygen plasma treatment

Figure 5.6 illustrate the process flow for the device isolation technique using oxygen plasma. The first five steps of the process flow for isolation using oxygen plasma treatment were identical to those of mesa isolation, listed in subsection 5.4.1. Thereafter, the sample was exposed to oxygen plasma using the BP80 RIE tool at a power of 150 W, oxygen gas flow rate of 20 sccm and a pressure of 20 mT for a duration of 5 minutes (Figure 5.6c). The photo-resist was then stripped using 1165 photo-resist stripper (Figure 5.6d) and the gate metal was deposited, resulting in a planar structure (Figure 5.6e).

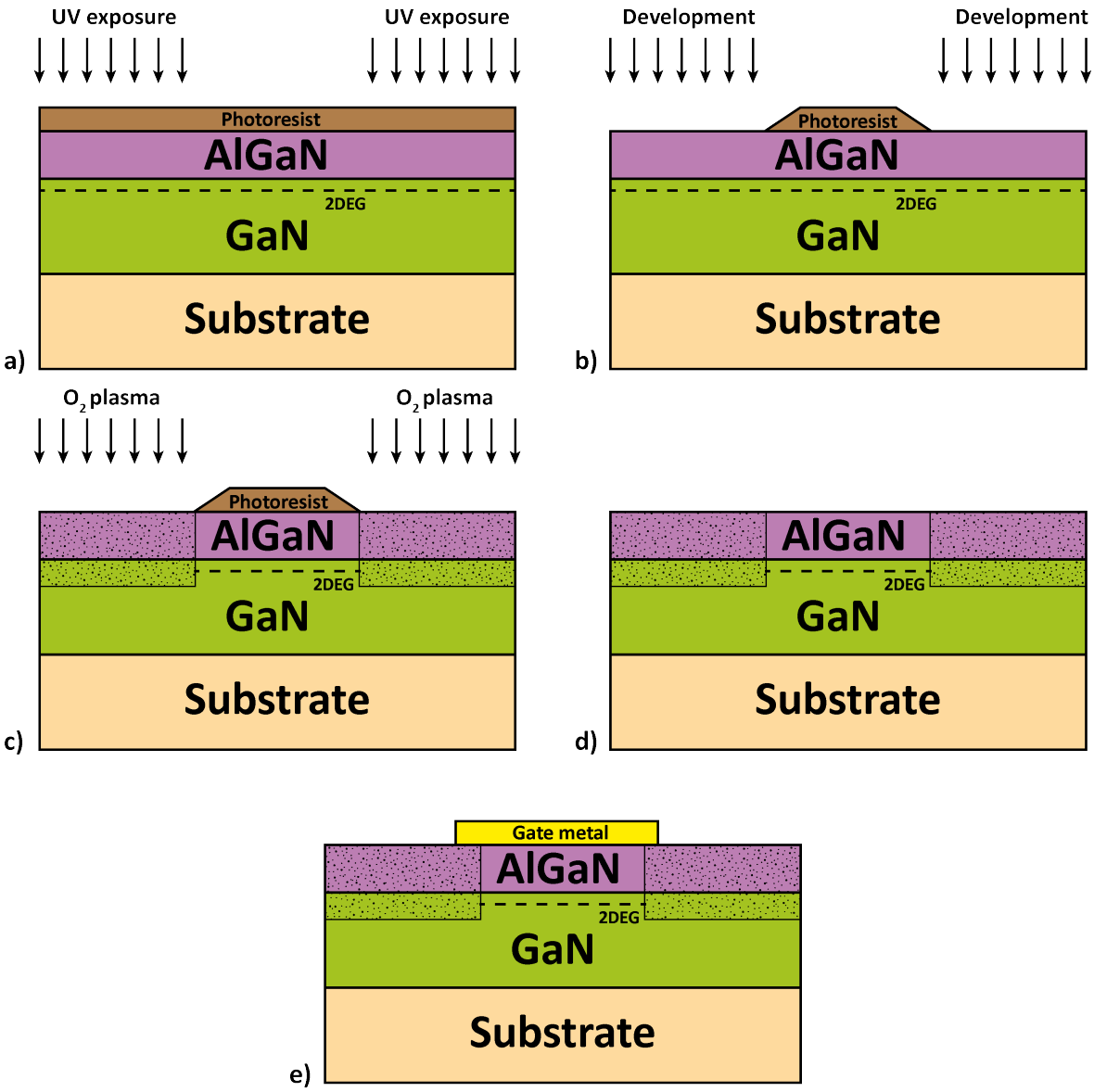

FIGURE 5.6: Oxygen plasma treatment process flow: a) photo-resist spinning and UV exposure, b) development, c) oxygen plasma treatment, d) photo-resist stripping and e) gate metal deposition.

As can be seen from the two isolation processes, the oxygen plasma treatment is similar to the photo-resist ashing process and hence achieves device isolation without the need for the RIE etching step. Two advantages result from the new process; simpler processing and planar devices with reduced gate leakage current.

5.5 Experimental results

Two samples with RF device layout were processed together. Devices on sample 1 were isolated using mesa etching and devices on sample 2 were isolated using oxygen plasma treatment. The device layout employed a gate width, W_G, of 2×100 μm, a gate length, L_G, of 3 μm, a source-to-drain distance, L_{SD}, of 9 μm and a gate-to-drain distance, L_{GD}, of 3 μm. All fabrication was done using photolithography. Device processing was done as follows:

1. Sample cleaning using acetone and isopropanol.
2. Ohmic contact metallisation using Ti/Al/Ni/Au (30/180/40/100 nm).
3. Rapid thermal annealing at 800°C for 30 seconds.
4. Device isolation using mesa isolation for sample 1 and oxygen plasma treatment for sample 2.
5. Gate metallisation using Ni/Au (20/200 nm).
6. Bond pad metallisation using Ti/Au (20/200 nm).

5.5.1 DC isolation

DC measurements were done using Agilent's B1500A semiconductor device analyser. Figure 5.7 shows the device-to-device current against applied voltage across the two devices. Before isolation, the device-to-device current was 300 mA/mm at 10 V. After isolation, the device-to-device current for mesa isolated devices was 1 μA/mm while device-to-device current for oxygen plasma treated devices was 10 μA/mm. This result demonstrated that the isolation process was effective in reducing the current to an acceptable level. It shows that oxygen plasma treatment can be used to isolate GaN HEMTs since the required level of isolation was 10 μA/mm matching the standard requirement for GaN technology.

To verify the effect of oxygen plasma treatment on device performance in terms of the output current, a comparison of IV characteristics was done on samples 1 and 2 as shown in Figure 5.8. Both devices exhibit a maximum drain current, I_{DSS}, of 325 mA/mm. Since the output currents are similar in both cases, it provided evidence that the new oxygen plasma treatment for isolation technique did not compromise the device performance and therefore, makes isoaltion using oxygen plasma treatment compatible with GaN HEMTs.

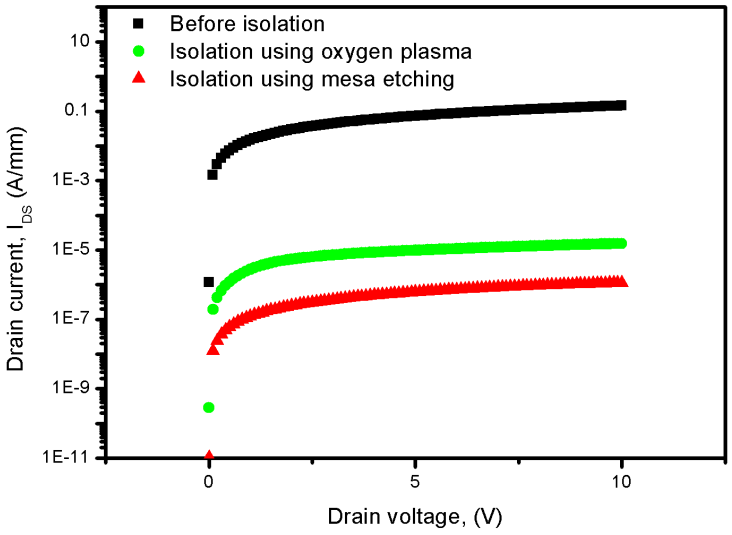

FIGURE 5.7: Comparison of device-to-device current in three different situations: before isolation, isolation using oxygen plasma and isolation using mesa etching.

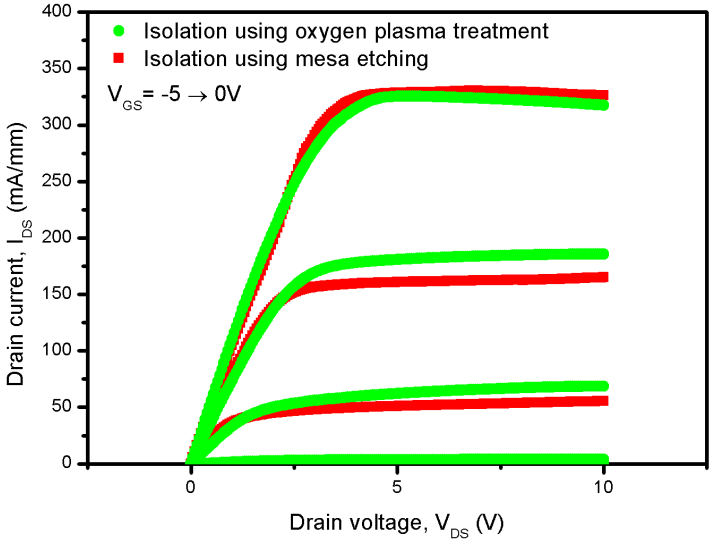

FIGURE 5.8: Comparison of IV characteristics of devices isolated using: oxygen plasma and mesa etching.

Figure 5.9 shows the I_{DS} versus V_{GS} graph. Both devices delivered a comparable drain current density of 325 mA/mm at a gate voltage of 0 V and drain voltage of 6 V and a comparable threshold voltage of -3.5 V. Devices isolated using oxygen plasma treatment showed a flat subthreshold drain current, indicating less drain leakage current compared to devices with mesa isolation that exhibit a small variation in subthreshold drain current. It seems that the lower subthreshold drain current exhibited by devices with mesa isolation was due to the lower device-to-device isolation currents shown in Figure 5.7. This result demonstrated the need for optimising the oxygen plasma treatment recipe to achieve comparable device isolation currents. Results from a modified oxygen plasma recipe will be provided later in this chapter.

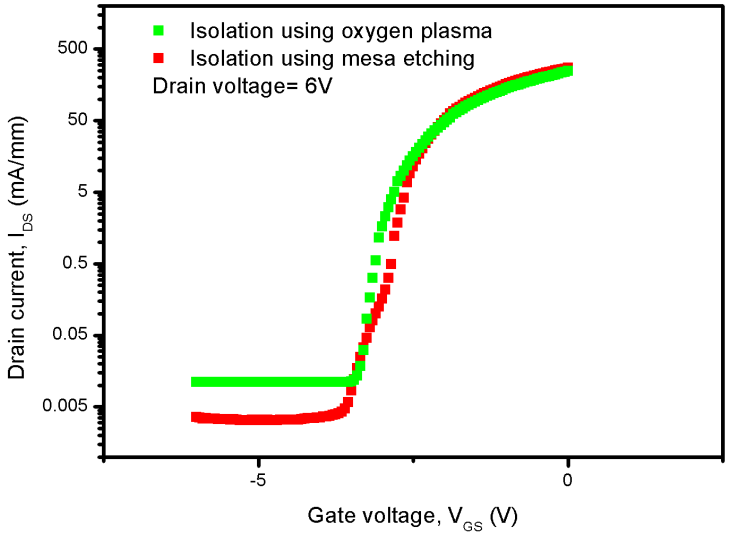

FIGURE 5.9: I_{DS} comparison of devices isolated using: oxygen plasma and mesa etching.

Figure 5.10 shows the transconductance of the two devices. Both devices exhibited a comparable maximum transconductance of 100 mS/mm and 110 mS/mm, respectively, at V_{GS} of 0 V and V_{DS} of 6 V. Figure 5.11 shows the gate leakage current of both devices with a gate voltage sweep from -20 V to +0.5 V and a drain voltage of 0 V. Devices isolated using mesa isolation exhibit one order of magnitude higher gate leakage currents (of 10 μA/mm) compared to devices isolated using oxygen plasma treatment (of 1 μA/mm) at a gate voltage of -20 V. This demonstrates the advantage of using oxygen plasma for device isolation since reducing the gate leakage current translates into higher breakdown voltage and improved noise performance of low noise amplifiers. Figure 5.12 shows the off state gate leakage current of both devices with a drain voltage sweep from 0 V to 10 V and gate voltage of -5 V. Devices isolated using mesa isolation

exhibit one order of magnitude higher gate leakage currents (of 10 μA/mm) compared to devices isolated using oxygen plasma treatment (of 1 μA/mm) at a drain voltage of 10 V. The oxygen plasma treated devices exhibited lower gate leakage currents as expected compared to mesa isolated devices. This is due to the fact that the gate in the mesa isolated devices is in direct contact with the 2DEG channel while the gate in the oxygen plasma treated devices have the AlGaN barrier acting as an insulator between the gate and the 2DEG channel.

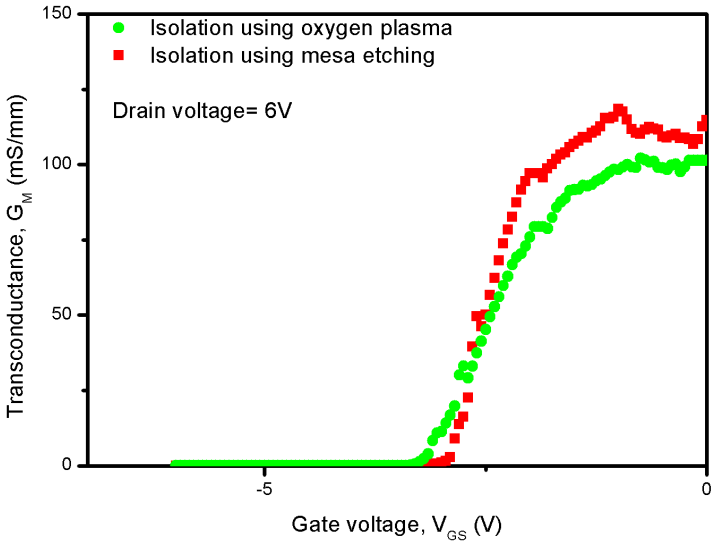

FIGURE 5.10: Transconductance (g_m) comparison of devices isolated using: oxygen plasma and mesa etching.

Since it was demonstrated earlier that the drain leakage currents for devices isolated using oxygen plasma treatment needed to be further reduced, the parameters for oxygen plasma treatment were changed. The power was increased from 150 W to 200 W and the duration was increased from 5 to 10 minutes. Figure 5.13 shows the result of the altered recipe comparing the two techniques. Before isolation, the device-to-device current was 300 mA/mm at 10 V. After isolation, the device-to-device current for mesa isolated and oxygen plasma treated devices was reduced to 1 μA/mm. These results demonstrate that the oxygen plasma treatment technique used for device isolation brings the advantage of reducing the gate leakage current without compromising the device performance in terms of output current and maximum transconductance.

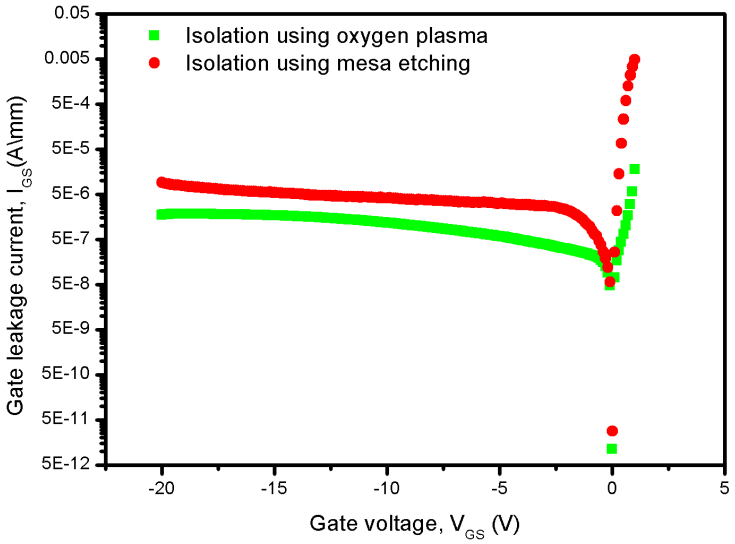

FIGURE 5.11: Gate leakage comparison of devices isolated using: oxygen plasma and mesa etching.

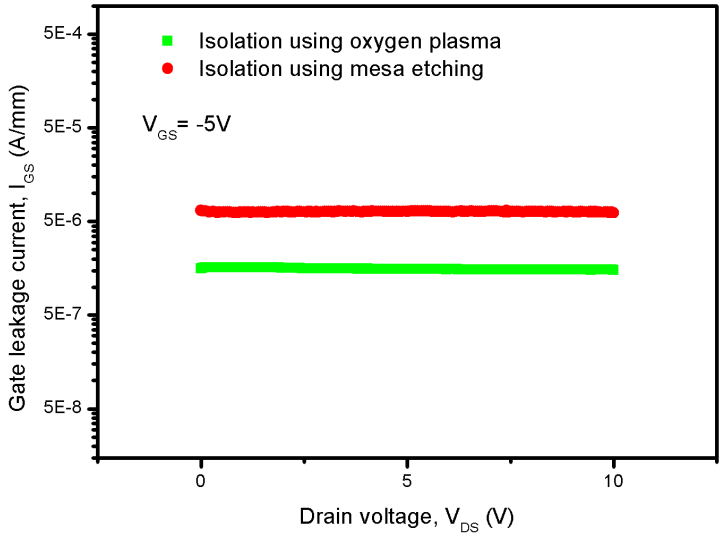

FIGURE 5.12: Off state gate leakage comparison of devices isolated using: oxygen plasma and mesa etching.

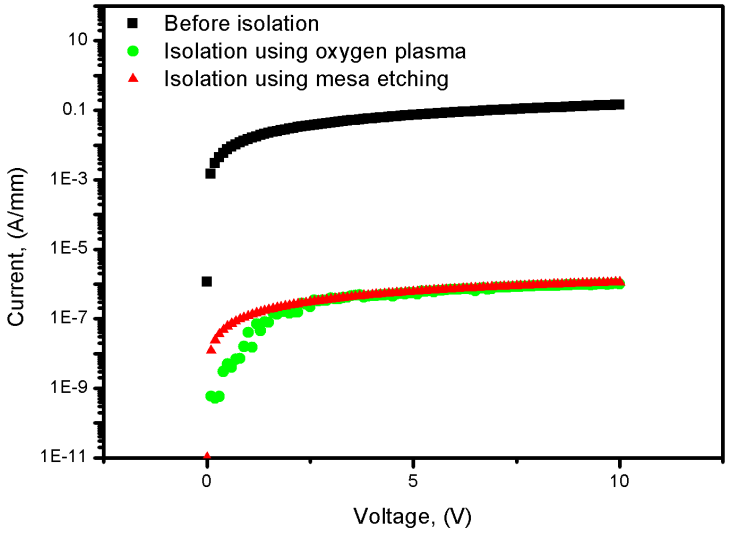

FIGURE 5.13: Comparison of device-to-device current in three different situations: before isolation, isolation using oxygen plasma and isolation using mesa etching.

5.5.2 RF isolation

To test the RF isolation of the oxygen plasma technique, a 2000 μm long coplanar waveguide (CPW) transmission line was fabricated on two AlGaN/GaN samples: one was not isolated, the other was isolated using oxygen plasma treatment. A CPW transmission line (called ideal here), which was usually used for calibration, was used for benchmarking. Figure 5.14 shows the RF isolation of the three transmission lines: the ideal line, the line on the isolated sample and the line on the non-isolated sample. The transmission line on the non-isolated sample exhibited high losses with increasing frequency, reaching -50 dB at 67 GHz from the measured transmission coefficient of the measured scattering parameters (S-parameters), S21. The transmission line on the isolated substrate exhibited losses of -2 dB at 67 GHz which are comparable to the losses on the ideal line. These results confirm that the new isolation technique is effective in reducing losses in the GaN-based HEMT material and can be used to make use of its advantage.

5.6 Summary and discussion

This chapter has described a novel approach to achieve device isolation. This approach is simple, repeatable and offers improved device performance compared to the conventional approach. The achieved gate leakage currents (of <1 μA/mm) are comparable to those exhibited by state of the art devices realised using the more expensive ion implantation

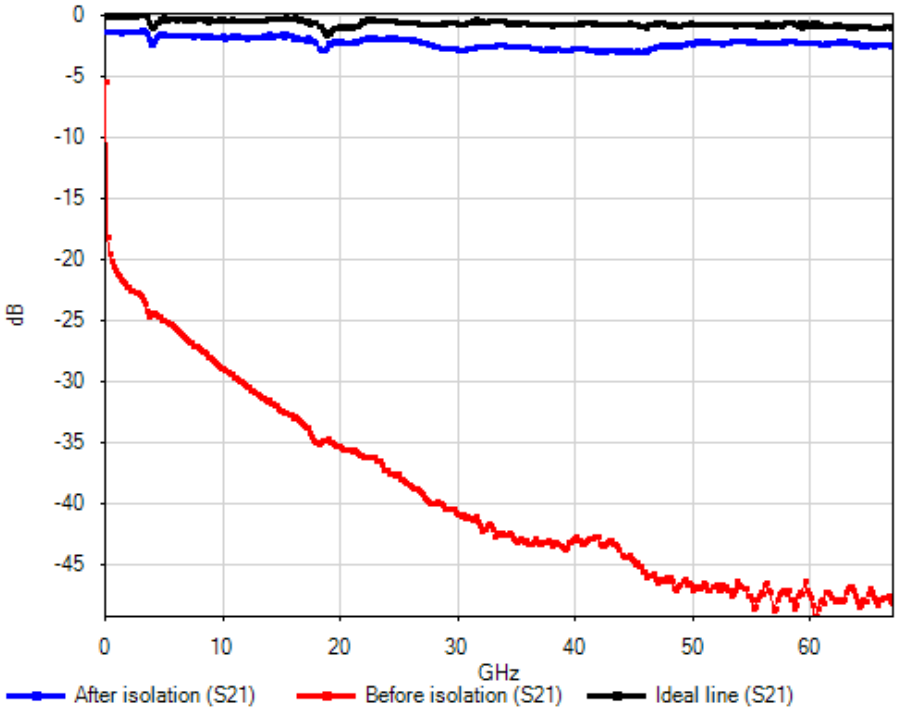

FIGURE 5.14: RF characteristics (S21) of three transmission lines: Ideal, isolated and non-isolated.

[147]. The reduced gate leakage current can lead to reduced noise which is helpful in realising low noise amplifiers [32]. Further investigation is however needed to determine the exact mechanism that occurs when treating the surface to oxygen plasma. There are two possibilities; surface oxidation [148] or plasma assisted oxygen doping [149]. Surface oxidation will neutralise the surface charges that are responsible for the polarisation while introducing oxygen ions in the GaN bulk will neutralise the charges in the bulk and in both cases, the 2DEG channel will be depleted. To test whether oxygen plasma was oxidising the barrier, the sample was treated with hydrochloric acid (HCl) which is a deoxidising agent for 30 minutes. After the HCl treatment, no recovery in the drain current occurred which indicates that the barrier was unlikely to have been oxidised. The surface was also still planar. In future work, the exact mechanism that is happening because of the oxygen plasma treatment needs further investigation. To do that, transmission electron microscopy (TEM) can be used to examine the cross section of the material for any oxidised layers. To investigate the presence of oxygen ions in the GaN structure low temperature photoluminescence (PL) [150], Raman spectroscopy [138], or high resolution x-ray diffraction (HRXRD) [151] can be used. The next chapter will describe a new thermal management technique for GaN HEMTs.

CHAPTER 6

Thermal Management of GaN HEMTs

6.1 Introduction

For a high power density technology such as GaN on SiC, the extraction of the heat generated due to dissipated power in the device is very important. This is because the device performance, e.g. drain current, drops with increasing junction temperature. The main limitation for further advancement in GaN technology today is thermal management, and therefore a major focus of this project was to investigate novel thermal management techniques. After reviewing various published techniques to address this challenge, an experimental study to demonstrate the thermal limitations of GaN devices on three different substrates; silicon, sapphire and SiC will be described. Device performance on sapphire using pulsed measurement will then be illustrated. A novel approach for extracting heat from GaN devices using integrated heat sinks will be then described. Finally, experimental results of conventional devices and devices with integrated heat sinks will be discussed.

6.2 Thermal considerations for GaN HEMTs

GaN's thermal conductivity was first determined in 1976 to be 130 W/mK [152]. Not until recently it was found that it is actually dependent on the dislocation density. Thermal conductivities of up to 230 W/mK were measured on free-standing hydride vapour phase epitaxy (HVPE) GaN with a low dislocation density of 10^5 cm^{-2} [153]. This could mean that the current thermal conductivity of GaN is underestimated as the

growth quality has improved significantly since 1976. The exact thermal conductivity of GaN in a HEMT material is difficult to measure, as GaN is incorporated in a multi-layer strcuture which include AlN and/or AlGaN on a foreign substrate that make the extraction of accurate figures complicated due to the number of uncertainties.

As discussed earlier in section 2.3.1, there are three popular types of substrates available for GaN to be grown on: silicon, sapphire and SiC. SiC has the highest thermal conductivity of 400 W/mK compared to 35 W/mK of Sapphire and 150 W/mK of Si. Therefore, SiC is the substrate of choice for GaN devices for high power RF applications. Figure 6.1 illustrates the epi-layer structure of a conventional HEMT with the respective thermal conductivity of each epi-layer. During device operation, heat is generated at the AlGaN/GaN interface in the device channel, the 2 dimensional electron gas (2DEG) channel. The thermal limitation to efficient heat extraction was identified by Kuball [47] to be mainly caused by the thermal boundary resistance (TBR) between the GaN buffer layer and the SiC substrate. When GaN is grown on a foreign substrate, a nucleation layer is required to reduce the lattice mismatch between the GaN and the substrate, and therefore this layer cannot be omitted [48]. The nucleation layer has however a low thermal conductivity varying between 1.5 and 23 W/mK which is two orders of magnitude lower compared to single crystal AlN [154]. This nucleation layer acts as a thermal bottleneck for the heat dissipated from the channel into the substrate. In fact, TBR associated with the nucleation layer is responsible for up to 50% of channel temperature in AlGaN/GaN devices [155]. A 25% reduction in TBR results in a 10% reduction in channel temperature. Using Micro-Raman spectroscopy, a channel temperature of up to 180°C was measured in devices fabricated on GaN/sapphire with power dissipation of 0.65 W, and 120°C in devices on GaN/SiC substrates with power dissipation of 1.75 W. TBR was determined to differ by a factor of four between the different device suppliers, all using MOCVD growth techniques. These results demonstrated the necessity of optimising the nucleation layers crystalline structure. An optimised nucleation layer growth leads to an improvement in the heat extraction which could result in reducing the peak channel temperatures by up to 40%. A good analysis of channel temperature with nonlinear thermal conductivity is given in [156].

The degradation in performance due to self-heating in AlGaN/GaN HEMTs is reported in [46]. Figure 6.2 shows the simulated and measured temperature rise due to self heating as a function of depth from the device into the substrate [157]. Raman spectroscopy was used to measure the temperature in the centre of ungated AlGaN/GaN device on SiC substrate. A power dissipation of 5.7 W caused the temperature to increase from 160°C to 220°C across the GaN/SiC interface due to the TBR. The thermal dissipation limitation associated with the TBR shows that thermal management using packaging techniques offers limited advantages. A good review on the reliability of power electronics

packaging components is given in [158]. Standard GaN based HEMTs are conservatively operated at power densities of 7 W/mm, to keep the channel temperature under 220°C for good device performance [45].

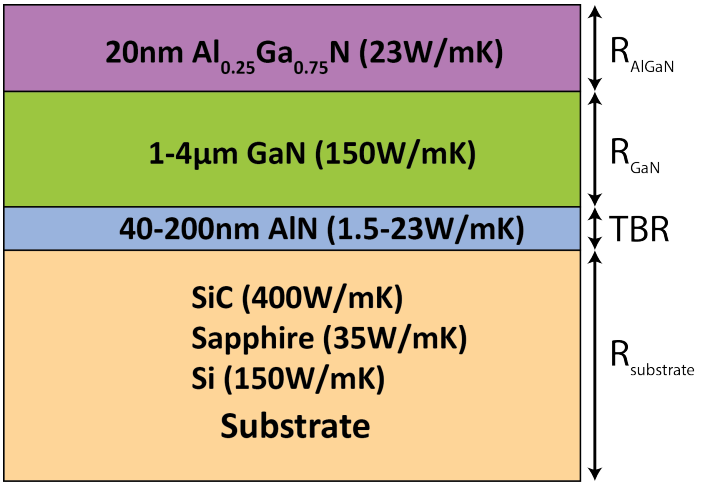

FIGURE 6.1: Cross-section of a GaN-based HEMT with the thermal conductivities of the respective epi-layers.

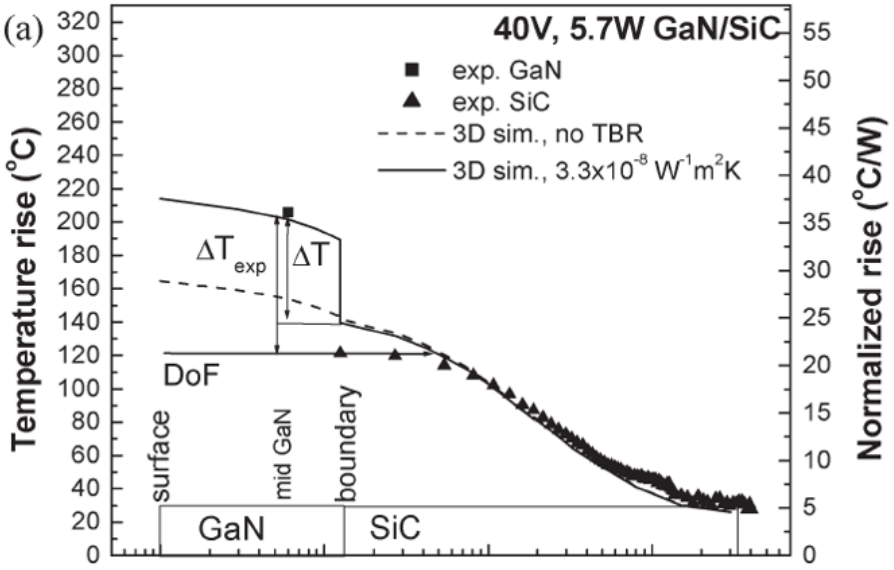

FIGURE 6.2: Simulated versus measured temperature of GaN on SiC substrate.

In this project, we investigated novel heat extraction methods that are expected to allow devices to operate at power densities in the order of tens of Watts per millimetre (W/mm), while maintaining the channel temperature below 200°C.

6.3 Review of thermal management techniques for GaN HEMTs

Despite the work done on thermal management of GaN devices over the past few years, the thermal limitation associated with the TBR remains the main challenge facing the advancement of GaN technology. By implementing novel heat extraction methods, including thermal vias that are located within microns of the active heat source (2DEG channel), the maximum power capabilities of GaN devices can be extended. The need for improving heat extraction in GaN HEMTs is demonstrated by the huge investments in the US through the Defence Advanced Research Projects Agency (DARPA), which is funding the Near Junction Thermal Transport (NJTT) programme [159]. The objective of the NJTT programme is to increase the power density of GaN devices by at least a factor of three. This can be achieved by reducing the near junction thermal barrier using different approaches, including the use of CVD diamond substrates, the removal of low conductivity epitaxial and transition layers at the interface of the GaN and the substrate and the utilisation of liquid cooling in the near-junction areas [160].

To assess the potential impact of diamond as a heat sink in GaN HEMTs, a commercial software package (CapeSym SYMMIC) was used to simulate the effect of selective growth of 30 μm CVD diamond layer in thermal vias under the GaN HEMTs [161]. The thermal vias were 100 μm x 100 μm and were located directly underneath the active region. For this structure, simulation showed that the channel temperature could be reduced from 221°C to 161°C at a power dissipation of 7 W/mm. Figure 6.3 shows the top view of the device (left) used in the thermal model and a section view (right) with arrows showing the thermal vias that are located directly below the devices.

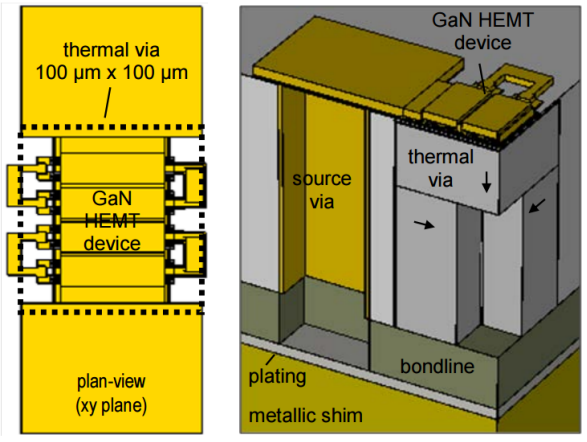

FIGURE 6.3: Thermal model renderings of (left) the HEMT and thermal via in plan-view and (right) a section view with arrows indicating the diamond high thermal conductivity orientation.

Under the NJTT programme, there are three main published approaches to integrated diamond in GaN devices: depositing nano-crystalline diamond on the surface of the device [51], etching vias from the back of the device and refilling them with diamond [162], removing the entire SiC substrate and replacing it with a diamond substrate [52].

In the first approach, the deposition of 0.4 μm nano-crystalline diamond (NCD) on the surface of AlGaN/GaN HEMTs (illustrated in Figure 6.4) offered an advantage of 20% higher transconductance and 1 W/mm output power compared to the reference HEMTs, which deliver an output power of 5.8 W/mm at a drain bias of 50 V [51]. On the other hand, no devices have been demonstrated yet using the second approach, in which selective deposition of diamond in vias in the SiC substrate is intended as shown in Figure 6.5. However, the advantage of this approach will be that the stress, due to the large thermal expansion mismatch associated with diamond and other semiconductors of interest can be managed more effectively compared to large area diamond growth. Diamond has a low coefficient of thermal expansion (CTE) of 0.8 pmm/K compared to the nitride layers, which exhibit a CTE in the range of 5.4-7.2 pmm/K. A selective diamond deposition process can largely eliminate wafer bow. The approach of removing the SiC substrate along with the low thermal conductivity epitaxial layers to within 1 μm of the 2DEG channel and attaching a diamond substrate at the back is illustrated in Figure 6.6. The full benefit of this approach will be limited by the thermal boundary resistance introduced by the bonding layer required to attach the diamond substrate to the GaN buffer. This approach is also yet to be experimentally demonstrated. Another closely related technique to realise GaN on diamond uses foreign substrates to grow GaN (usually SiC). The foreign substrate is later removed from the back and the GaN epi-structure is atomically bonded to a diamond substrate [52].

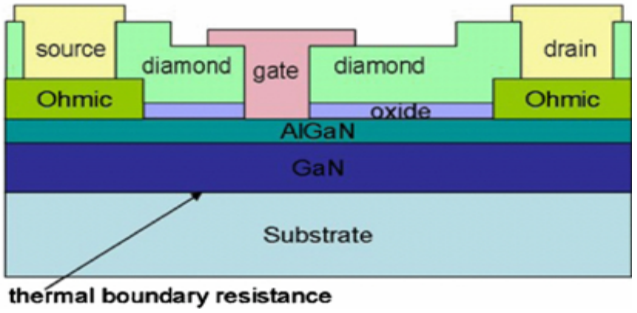

FIGURE 6.4: Illustration of nano-crystalline diamond (NCD) on the surface of AlGaN/GaN HEMT.

Other reported thermal management techniques for GaN technology include the use of graphene and sputtered AlN [49, 50]. In devices with graphene placed at the drain side (as illustrated in Figure 6.7) using micro-Raman spectroscopy, it was found that channel temperatures were reduced by 20°C for transistors operating at a power density of 13

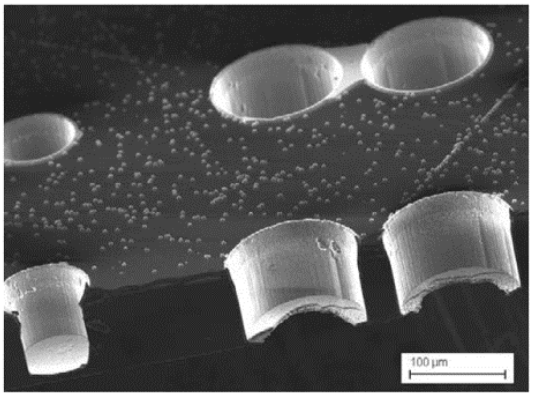

FIGURE 6.5: Micrograph of thermal vias in SiC substrate filled with diamond.

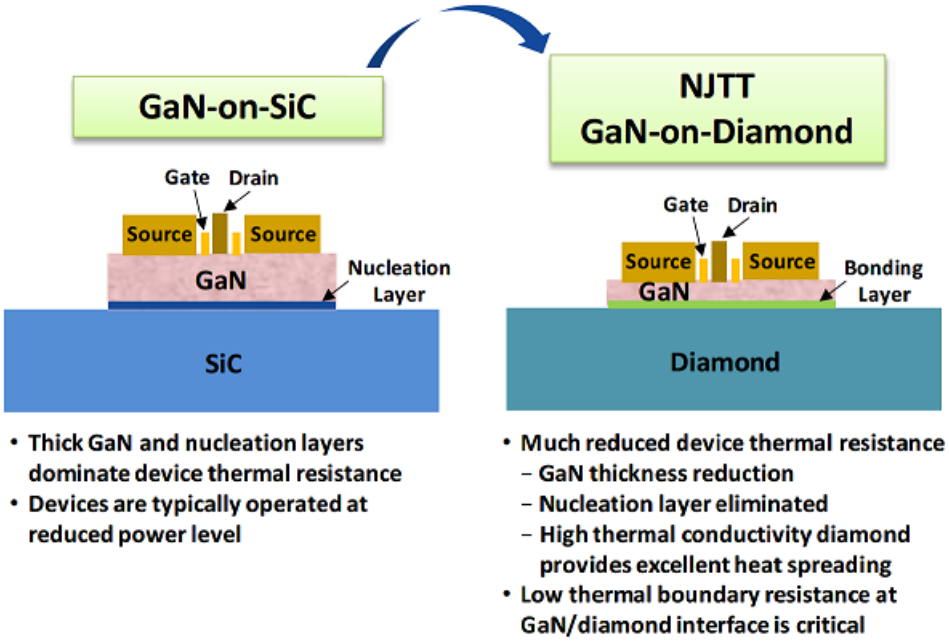

FIGURE 6.6: Comparison of a conventional GaN-on SiC HEMT to the DARPA Near Junction Thermal Transport (NJTT) GaN-on-Diamond device.

W/mm. This corresponds to an order of magnitude increase in the device lifetime. On the other hand, the use of sputtered AlN heat sinks deposited on the AlGaN surface showed an increase of drain currents of 30% and a reduction of the on-resistance by 66%. It is known, however, that an AlGaN layer with 40% Al content has a low thermal conductivity of only 25 W/mK [163]. As the AlGaN barrier layer is located between the 2DEG channel and the surface of AlGaN/GaN HEMTs, it limits the heat extraction from the surface as proposed in [50]. Although good improvement in device performance was shown, it is clear that the full potential of using AlN for heat sinking has not yet been fully exploited. Thermal conductivity of the nitride layers also drops with increasing temperature. It is therefore desirable to operate while the channel is at the

lowest temperature possible to avoid degrading the thermal conductivity [164] and device performance. The use of microfluidic heat exchangers is also reported in [160].

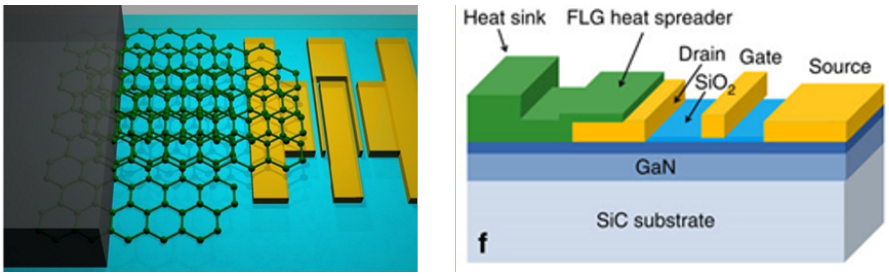

FIGURE 6.7: Illustration of graphene on the drain side of the device.

6.4 Device performance on silicon, sapphire and SiC substrates

This section describes GaN based device performance on the three different substrates: silicon, sapphire and SiC. SiC has the highest thermal conductivity of 400 W/mK compared to 150 W/mK of silicon and 35 W/mK of sapphire. The RF device layout was used to investigate the performance from a thermal perspective. For comparison, three samples with RF device layout were processed at the same time. All material on the three substrates had the following epi-layer structure: 2nm GaN cap, 20nm AlGaN barrier and a GaN channel. The device layout employed gate widths, W_G, of 2×10 μm, 2×100 μm and 2×200 μm. All devices employed a gate length, L_G, of 3 μm, a source-to-drain distance, L_{SD}, of 9 μm and a gate-to-drain distance, L_{GD}, of 3 μm. All fabrication was done using photolithography. The device processing steps were as follows:

1. Sample cleaning using acetone and isopropanol.
2. Ohmic contact metallisation using Ti/Al/Ni/Au (30/180/40/100 nm).
3. Rapid thermal annealing at 800°C for 30 seconds.
4. Device isolation using oxygen plasma treatment.
5. Gate metallisation using Ni/Au (20/200 nm).
6. Bond pad metallisation using Ti/Au (20/200 nm).

DC measurements were done at room temperature using Agilent's B1500A semiconductor device analyser. Figures 6.8, 6.9 and 6.10 show the IV characteristics of 2×100 μm GaN HEMTs fabricated on silicon, sapphire and SiC substrates, respectively.

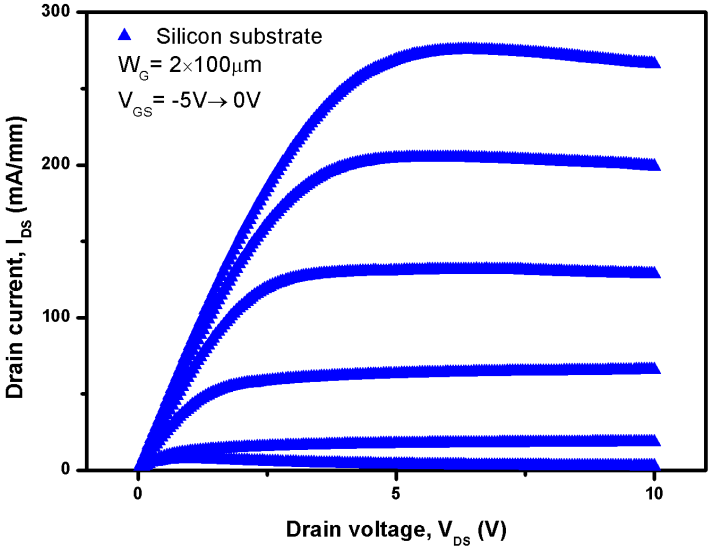

FIGURE 6.8: Output IV characteristics of 2x100 μm GaN HEMTs grown on a silicon substrate.

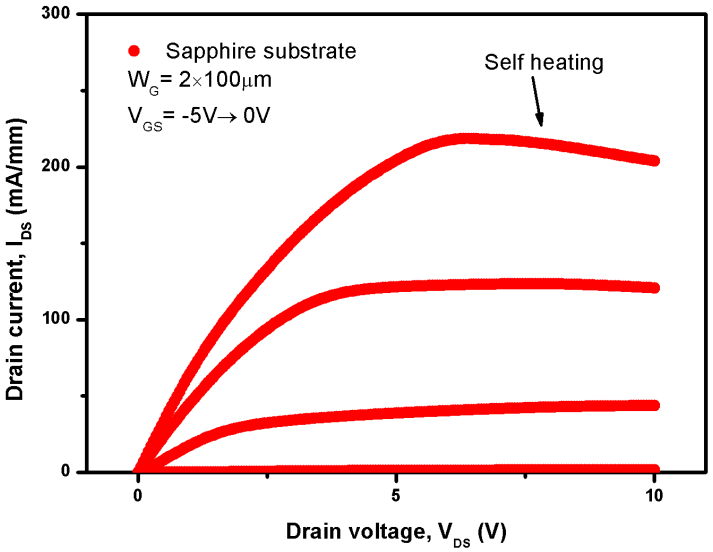

FIGURE 6.9: Output IV characteristics of 2x100 μm GaN HEMTs grown on a sapphire substrate.

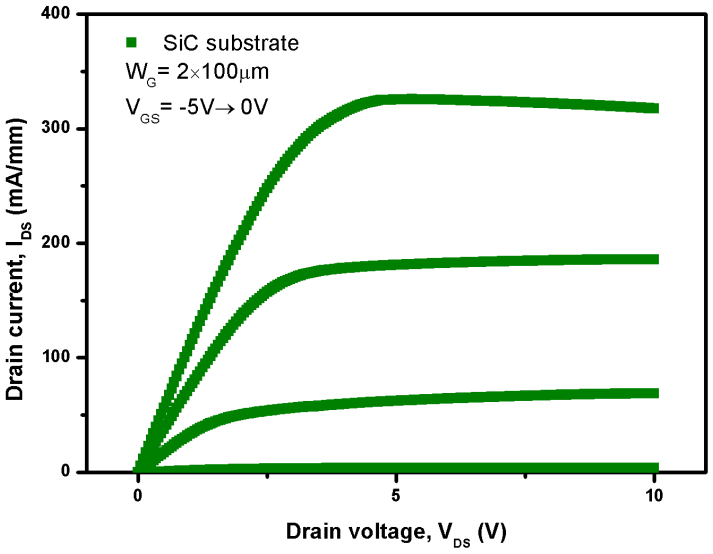

FIGURE 6.10: Output IV characteristics of 2x100 μm GaN HEMTs grown on a SiC substrate.

The 2×100 μm GaN HEMTs fabricated on silicon, sapphire and SiC substrates exhibited a maximum drain current density of 275 mA/mm, 220 mA/mm and 325 mA/mm, respectively at V_{GS}= 0 V. Self heating for devices on sapphire substrates is evident from the drop in drain current with increasing drain bias at V_{GS}= 0 V, as shown in Figure 6.9. Devices fabricated on SiC substrate exhibit the highest current density as expected with devices on sapphire exhibiting the least current density. Figure 6.11 shows the IV characteristics of the three devices superimposed.

Figure 6.12 shows the output characteristics for three different device sizes, 2x10 μm, 2x100 μm and 2x200 μm on SiC substrate. At V_{GS}= -2 V, the three devices exhibit similar current densities. At V_{GS}= 0 V, the difference in current densities (I_{DSS}) becomes clearer between the three device sizes, with the 2×10 μm wide device exhibiting the highest current density, while the 2×200 μm not only exhibiting the lowest current density but also self heating effect is more clear at the high drain bias voltage. Table 6.1 summarises the drain current densities on the different substrates. It also shows the effect of increasing device gate width on the different substrates. It shows that regardless of the substrate choice, increasing the gate width does impact the output current density. Therefore, a tradeoff has to be made between current density and absolute output power when designing GaN HEMTs for high power amplifier applications. The common device width in the literature is 100-200 μm.

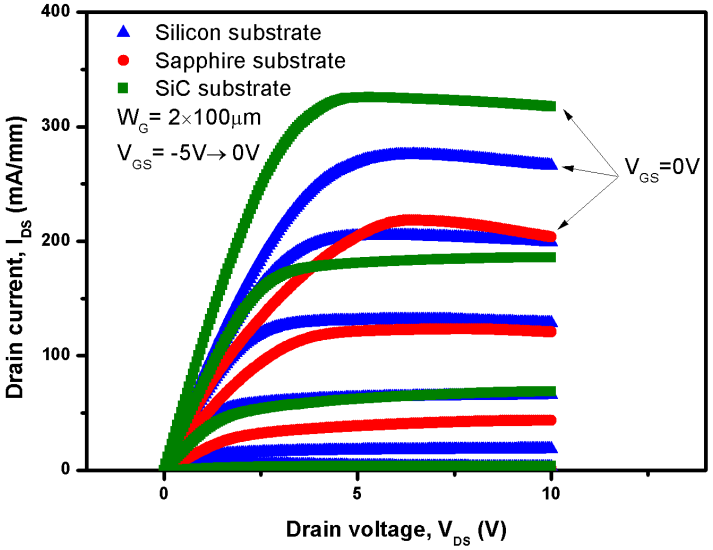

FIGURE 6.11: Output IV characteristics of 2x100 μm GaN HEMTs grown on the three different substrates.

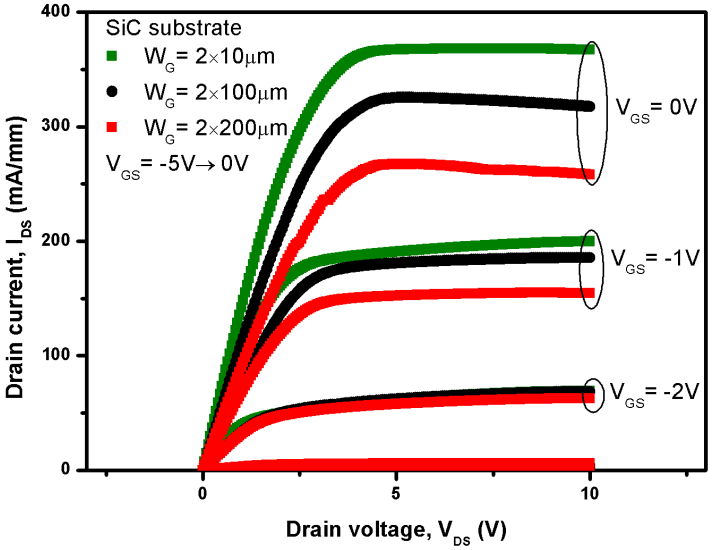

FIGURE 6.12: Output IV characteristics of 2x10 μm, 2x100 μm and 2x200 μm GaN HEMTs grown on a SiC substrate.

Device width	**2×10 μm**	**2×100 μm**	**2×200 μm**
I_{DSS} (mA/mm), Silicon	285	275	245
I_{DSS} (mA/mm), Sapphire	265	220	200
I_{DSS} (mA/mm), SiC	365	325	270

TABLE 6.1: I_{DSS} of devices on the different substrates employing variable gate widths of 2x10 μm, 2x100 μm and 2x200 μm.

Figure 6.13 shows a comparison of the drain current of devices fabricated on the three different substrates. They all show a low sub-threshold drain leakage current of below 10 μA/mm, with the sapphire and silicon wafers showing drain leakage currents below 1 μA/mm. The higher drain leakage current exhibited by devices fabricated on the SiC could be due to the non-optimised isolation recipe used as discussed in section 5.5.1. The silicon substrate shows a threshold voltage of -5 V while SiC and sapphire exhibit a threshold voltage of -3 V. Figure 6.14 shows the gate leakage current of devices fabricated on the three different substrates. The three devices show a low gate leakage currents of 1 μA/mm at a gate voltage of -20 V.

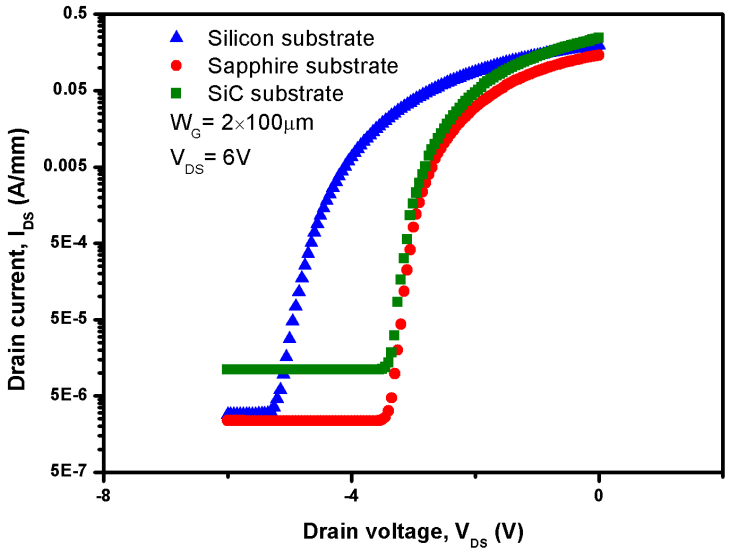

FIGURE 6.13: I_{DS} comparison of 2x100 μm GaN HEMTs fabricated on the three different substrates.

Figure 6.15 shows the output IV characteristics at zero gate voltage of 2x100 μm GaN HEMTs fabricated on the three different substrates. The drain voltage is biased from 0 V to 40 V for dissipation of up to 12 W/mm as heat in the channel. The reduction in drain current with increasing bias is clear in all the three cases. Table 6.2 shows a summary of the current densities on the different substrates to illustrate the percentage

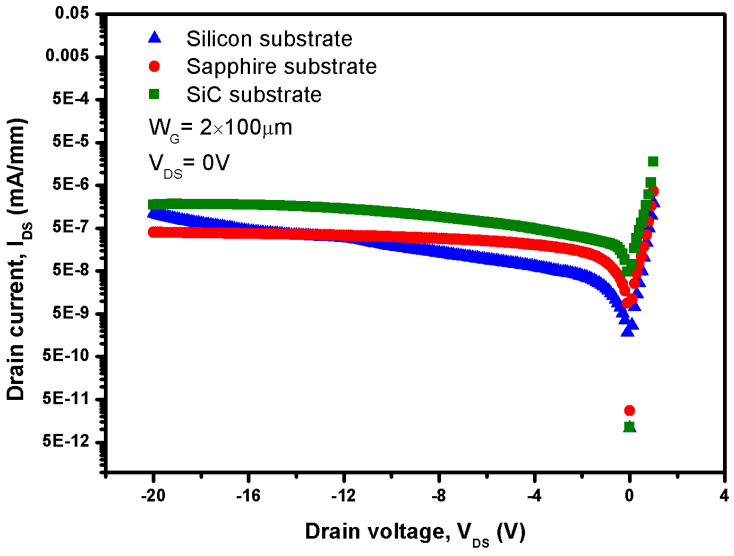

FIGURE 6.14: Gate leakage current comparison of 2x100 μm GaN HEMTs fabricated on the three different substrates.

reduction in current density with the increasing bias. As expected, the least percentage of reduction is exhibited by devices on SiC while the highest percentage of reduction is exhibited by the sapphire wafer due to it's low thermal conductivity.

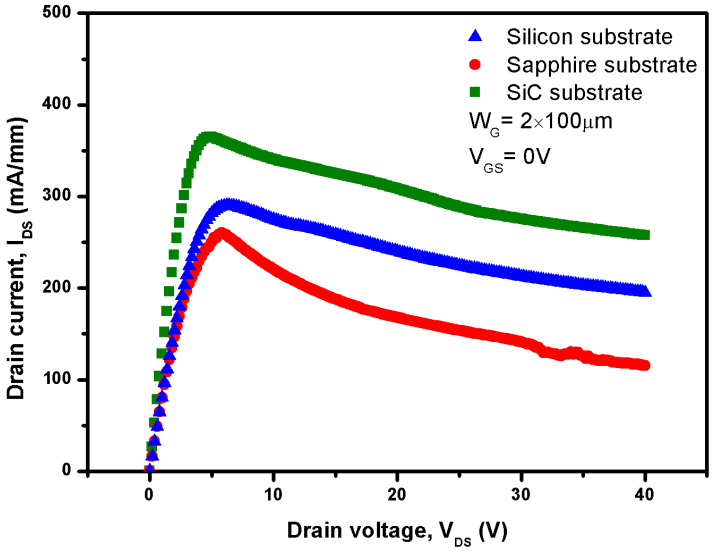

FIGURE 6.15: Output IV characteristics of 2x100 μm GaN HEMTs fabricated on the three different substrates.

	At V_{DS}= 5 V	**At V_{DS}= 40 V**	**% of reduction**
I_{DSS} (mA/mm), Silicon	290	195	33%
I_{DSS} (mA/mm), Sapphire	260	115	56%
I_{DSS} (mA/mm), SiC	365	255	30%

TABLE 6.2: I_{DSS} of 2x100 μm devices on the different substrates.

Figure 6.16 shows the current densities of devices fabricated on SiC substrate with varying gate widths. The drop in drain current with increasing bias is also evident. Table 6.3 shows a summary of the current densities on the SiC substrates with the different gate widths. As expected, it shows that the devices with small gate widths are least affected from dissipated heat than devices with larger gate widths that have a higher percentage of current drop. Clearly, for the same bias voltages (V_{GS} and V_{DS}) the larger devices support higher drain currents (I_{DS}), and therefore the dissipated power in the device is also higher.

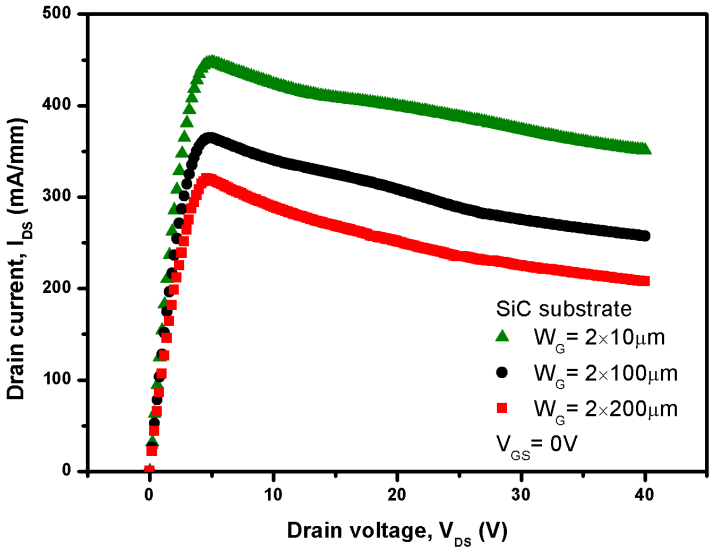

FIGURE 6.16: Output IV characteristics of 2x10 μm, 2x100 μm and 2x200 μm GaN HEMTs fabricated on a SiC substrate.

	At V_{DS}= 5 V	**At V_{DS}= 40 V**	**% of reduction**
I_{DSS} (mA/mm), 2x10μm	445	350	21%
I_{DSS} (mA/mm), 2x100μm	365	255	30%
I_{DSS} (mA/mm), 2x200μm	320	210	34%

TABLE 6.3: I_{DSS} of 2x10 μm, 2x100 μm and 2x200 μm devices on SiC substrate.

6.5 Pulsed IV measurements

Pulsed IV measurement is another technique that can be used to demonstrate the effect of dissipated heat on the output current of a device [165]. Short pulses of 1 μs are used with a duty cycle of 1 ms to allow the device to cool during the off-state. Figure 6.17 illustrates the on and off time of a pulsed IV bias setup. During the off-time, the device is allowed to cool down before turning-on again for the next pulse. The difference between the output current in the pulsed mode and the DC mode gives a good understanding of the extent of the self-heating problem.

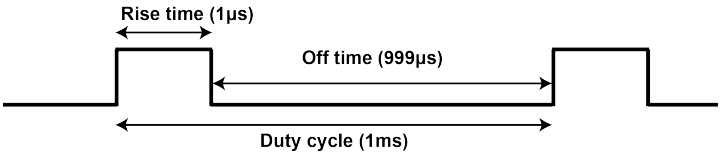

FIGURE 6.17: Illustration of pulsed IV bias in the on and off state.

To setup the experiment, two sets of devices were fabricated on sapphire substrate. One set had a Schottky gate and the other had 10 nm ICP-CVD SiN_x gate insulator. The devices employed a W_G of 2×200 μm, L_G of 1 μm, L_{SD} of 6 μm and L_{GD} of 3 μm. All fabrication was done using photolithography. The device processing steps were as follows:

1. Sample cleaning using acetone and isopropanol.
2. Ohmic contact metallisation using Ti/Al/Ni/Au (30/180/40/100 nm).
3. Rapid thermal annealing at 800°C for 30 seconds.
4. Device isolation using RIE with $SiCl_4$.
5. Deposition of 10 nm ICP-CVD SiN_x gate insulator on the second set of devices only.
6. Gate metallisation using Ni/Au (20/200 nm).
7. Bond pad metallisation using Ti/Au (20/200 nm).

Figure 6.18 shows the current-voltage (IV) characteristics of a Schottky gate HEMT conducted in continuous and in pulsed mode from the cold bias point of V_{DS} = 0 V and V_{GS} = 0 V. This cold point is chosen to eliminate the self-heating effect that would occur if the device was biased elsewhere. The choice of bias point gives a good indication of the performance degradation due to the self-heating effect. From Figure 6.18, it can

be seen that the maximum DC current, I_{DS}, is 300 mA/mm while the maximum pulsed current is 400 mA/mm, indicating 100 mA/mm degradation in output current due to self-heating.

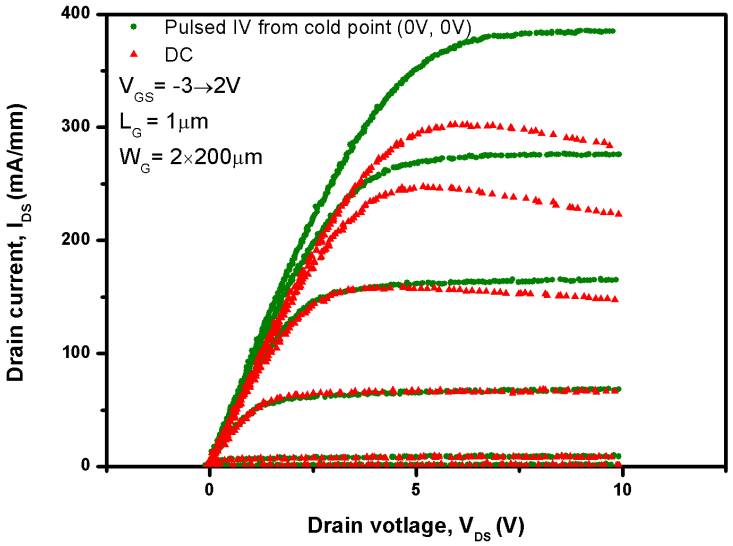

FIGURE 6.18: DC and pulsed IV characteristics of a Schottky gate HEMT. Drop in drain current of 100 mA/mm at $V_{GS} = 0$ V can be observed.

Figure 6.19 shows the DC and pulsed IV characteristics of a MIS-HEMT employing 10 nm of ICP-CVD SiN_x. The maximum I_{DS} is 450 mA/mm, which is a 50% improvement compared to the 300 mA/mm exhibited by Schottky gate HEMTs. From pulsed IV measurements, the maximum I_{DS} increases to 700 mA/mm, indicating 250 mA/mm degradation in output current due to self-heating. It is worth noting that the current reduction due to the self-heating effect in the Schottky gate HEMTs is less due to the lower I_{DS}. In both cases, the knee voltage reduces by 1 V which corresponds to an improvement (reduction) in the on-resistance. These results clearly show that techniques for reducing self-heating, by extracting the dissipated heat within the device, are necessary to advance the technology to the next level, i.e. handle higher power densities.

6.6 Proposed thermal management approach

In this project, the proposed approach to extract heat dissipated in the device is to provide a low thermal resistance path, located within few microns of the 2DEG channel (heat source), that is connected directly to the high thermal conductivity SiC substrate (heat sink). Figure 6.20 illustrates a schematic cross-section of the etched epi-layers,

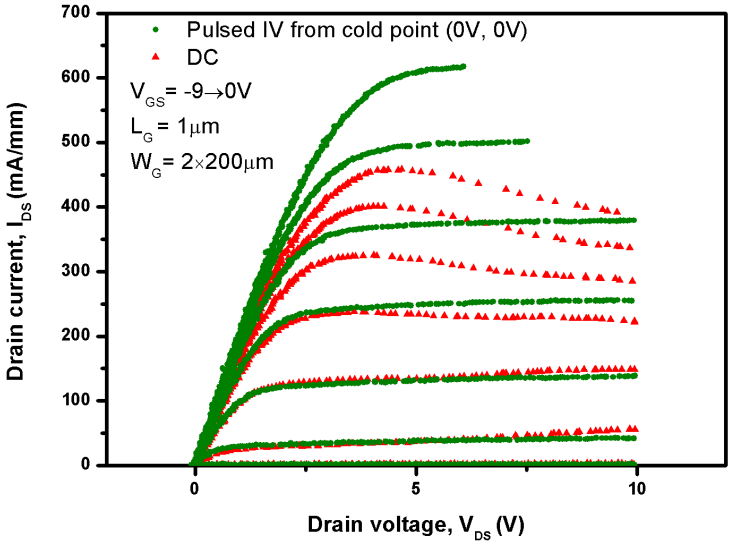

FIGURE 6.19: DC and Pulsed IV characteristics of a MIS-HEMT with 10nm of ICP-CVD SiN_x. Drop in drain current of 250 mA/mm at $V_{GS} = 0$ V can be observed. High drain currents are due to SiN_x passivation.

creating a via to the substrate to be filled with the heat sink material. Figure 6.21 illustrates the top view of the a) conventional versus b) the new RF device layout. Devices have the drain contact split into two 10 μm fingers to allow the thermally insulating nitride epi-layers between the two fingers to be etched down to the substrate. Thermal pathways are realised by etching the epi-layers, starting from the top and reaching the substrate. After filling the vias with a suitable material that has a high thermal conductivity, such as AlN or copper, a high thermally conductive pathway is created. This thermal pathway does not only dissipate heat away from the surface, it also reduces the thermal crosstalk between the gate fingers as it sits between the device gates where the heat is generated. This approach is much cheaper and straight forward compared to the aforementioned approaches adopted by other research groups as it is easier to etch the relatively thin (3 μm) GaN from the top, for instance, compared to etching the thick (350 μm) SiC substrate. To remove the epi-layers, a dry etch recipe has been developed to etch 3 μm of GaN down to the substrate, as will be described in section 6.8.

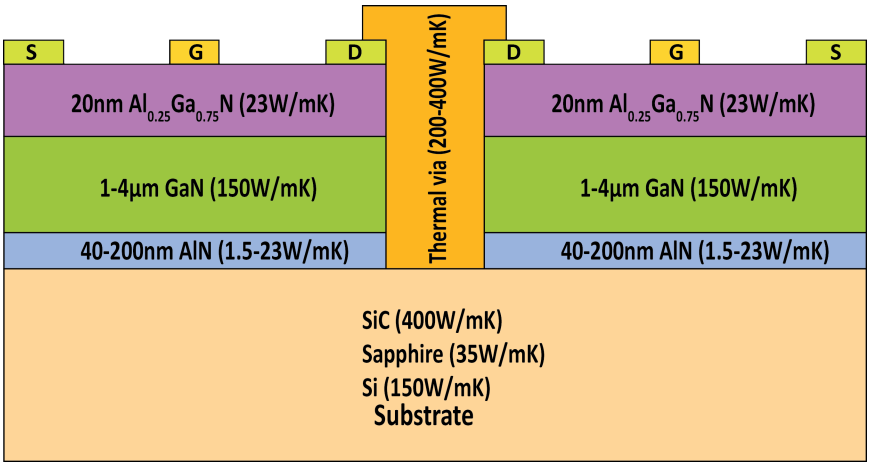

FIGURE 6.20: Cross-section of a GaN-based HEMT structure with integrated heat sinks.

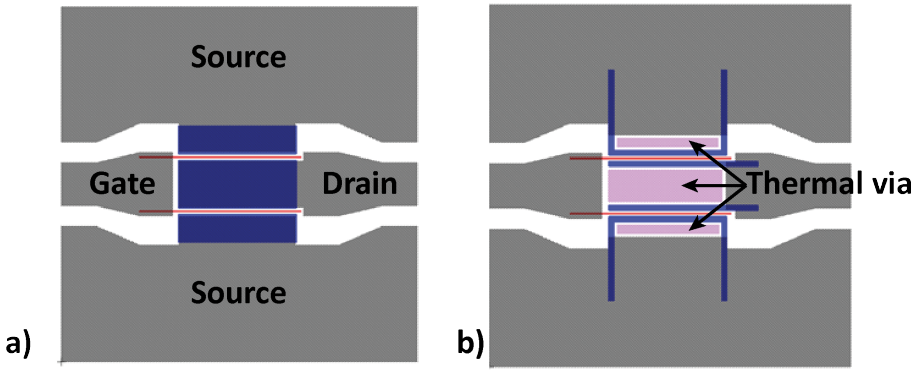

FIGURE 6.21: Layout of a) conventional RF device versus b) the new device with integrated heat sinks.

6.7 Thermal simulation

In this section, thermal simulation is demonstrated to explain the heat dissipation in GaN HEMTs. Comsol software is used to run the thermal simulations. Three types of devices are simulated, standard GaN HEMTs with no thermal boundary resistance (TBR), standard devices with TBR and HEMTs with integrated copper heat sinks. The channel temperature of the standard HEMTs with no TBR is simulated and compared to the channel temperature of the standard HEMTs with TBR to quantify how much the temperature rise in the channel is due to the TBR. The HEMTs with integrated copper heat sink is then simulated to demonstrate the advantage of introducing the copper heat sinks.

Figure 6.22 illustrates the cross section of the simulated structure. The structure is a

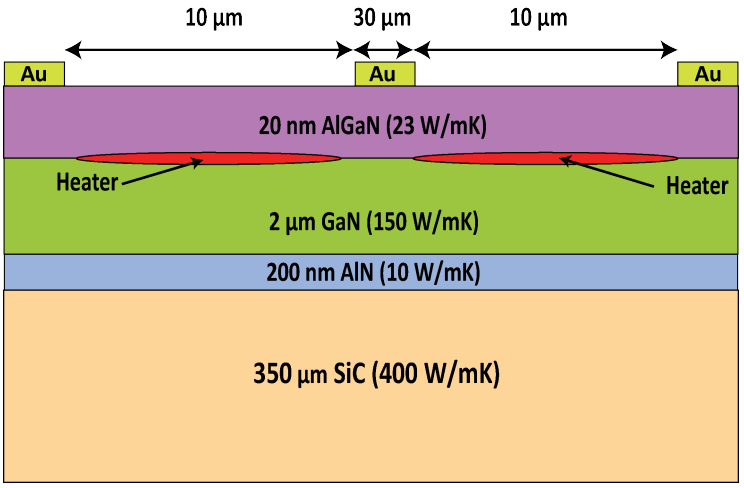

FIGURE 6.22: Standard GaN HEMT model

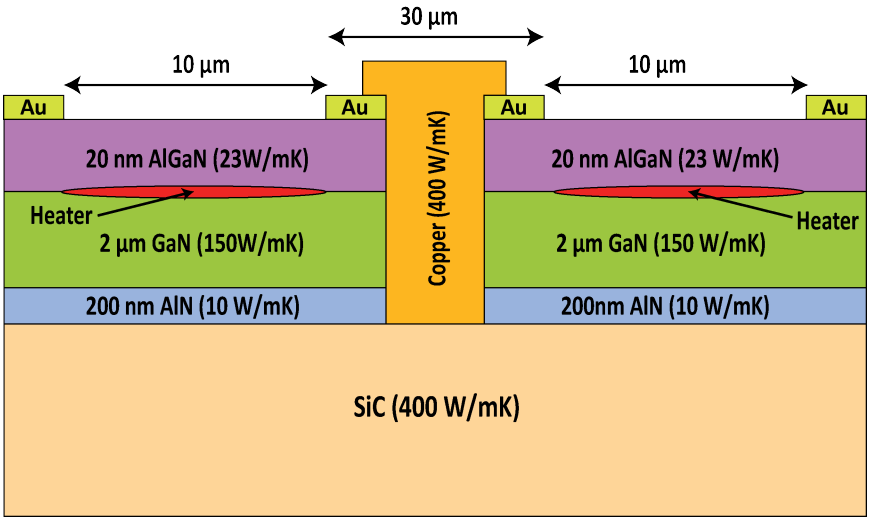

FIGURE 6.23: GaN HEMT model with integrated copper heat sink

standard GaN HEMT with the respective epi-layer thicknesses and thermal conductivities. The two heaters indicate the two finger device with gate to gate spacing of 30 μm. The channel length and width are 10 μm and 100 μm respectively. The total power dissipation in the channel is always fixed at 10W where each heater dissipates 5W. The structure given in Figure 6.23 is of a GaN HEMT with integrated copper heat sink. The heat sink is located between the two adjacent heaters in order to reduce the thermal cross talk between the two heaters and reduce the channel temperature. The TBR under the copper heat sink is removed so that the heat sink effectively transports the heat from the channel into the substrate with maximum while minimising the thermal resistance. The substrate in this case become the effective heat sink storing all of the heat that is generated in the channel which in the case of the standard devices is trapped in the GaN buffer due to the TBR limitation.

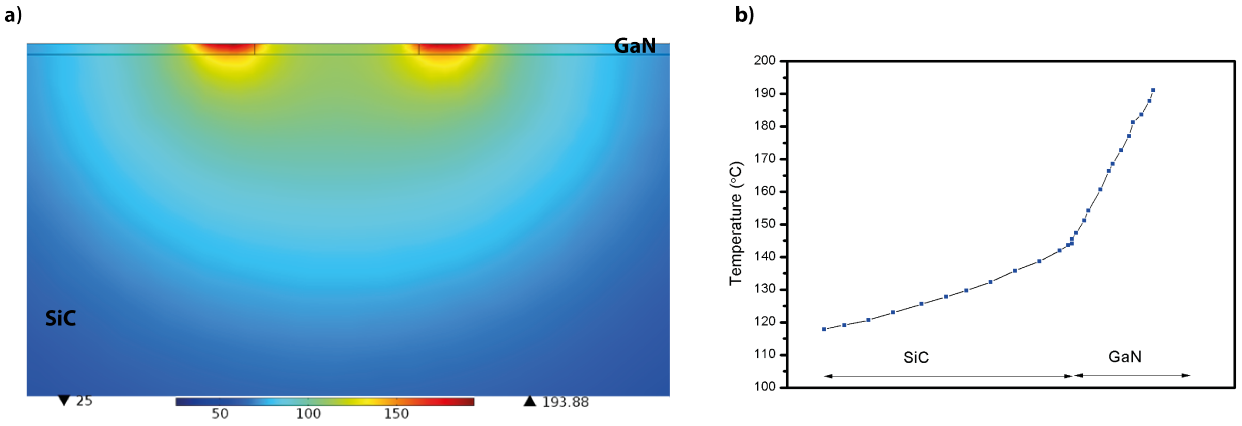

FIGURE 6.24: a) Standard GaN HEMT with no TBR, b) temperature profile of GaN on SiC substrate.

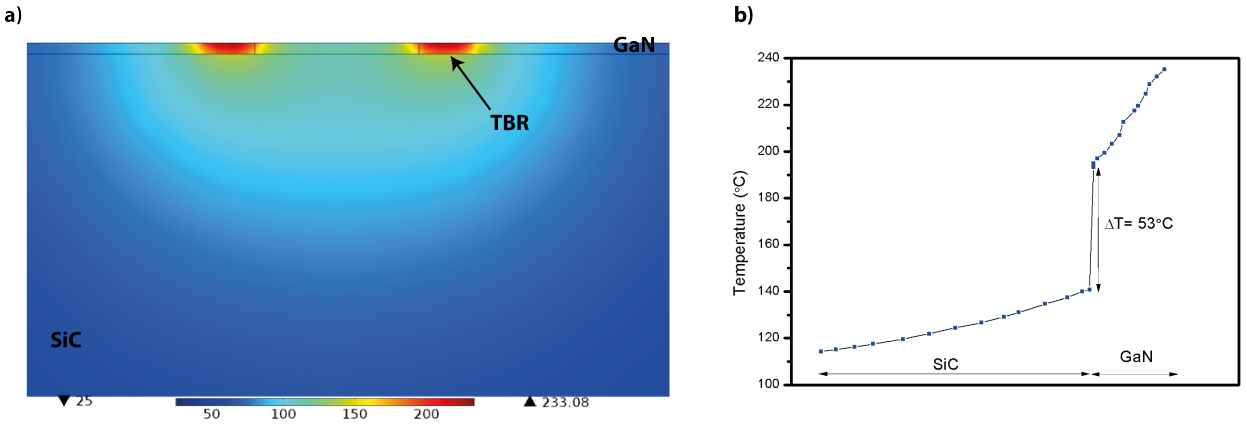

FIGURE 6.25: a) Standard GaN HEMT with TBR, b) temperature profile of GaN on SiC substrate.

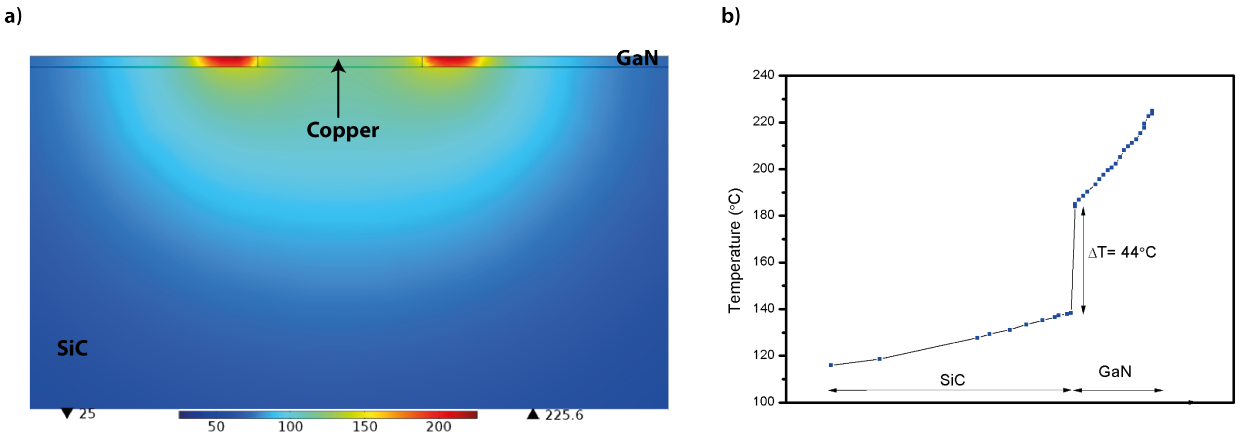

FIGURE 6.26: a) GaN HEMT with integrated heat sink, b) temperature profile of GaN on SiC substrate.

Figure 6.24a) illustrates the thermal simulation of a 2 finger GaN HEMT on SiC substrate. The device have the the TBR removed from the epi-structure and hence the maximum channel temperature is 193°C. The heat flux in the diagram is visibly evenly distributed since there is no TBR limiting the heat transfer from the GaN buffer into the substrate. Figure 6.24b) illustrates the temperature distribution of GaN on SiC epi-structure. Since GaN has a lower thermal conductivity of 150 W/mK compared to 400 W/mK of SiC, the slope of the temperature across the GaN is steeper than the temperature slope in the SiC.

Figure 6.25a) illustrates the thermal simulation of a 2 finger GaN HEMT on SiC substrate with TBR. Since the TBR limits the heat transfer from the GaN channel into the SiC substrate, the maximum channel temperature increases to 233°C. The heat flux in the diagram is disturbed at the TBR as it limits the heat transfer from the GaN buffer into the substrate. Figure 6.25b) illustrates the temperature distribution of GaN on SiC epi-structure. Since the TBR exists in this structure, the is a temperature drop at the GaN/SiC interface of 53°C which needs special design to reduce and transport the heat more effectively into the SiC substrate. Figure 6.26a) illustrates the thermal simulation of a 2 finger GaN HEMT on SiC substrate with integrated heat sinks. The TBR is removed at the copper/SiC interface allowing the heat to transfer more efficiently between the channel and the SiC substrate. The maximum channel temperature improves down to 225°C. Figure 6.26b) illustrates the temperature distribution of GaN on SiC epi-structure. Since the copper heat sink is introduced in this structure, the temperature drop at the GaN/SiC interface is reduced to 44°C indicating an improved heat transfer between the channel and SiC substrate.

6.8 Process development and experimental results

For the realisation of integrated heat sinks, new process modules, including the use of new layouts and dry etch techniques, to remove thermally insulating epi-layers were required. Details of the various processes are described below.

6.8.1 Dry etching of nitride epi-layers

Dry etching of the nitride epi-layers was done using ICP with $BCl_3/Cl_2/Ar$ gas chemistry to achieve high etch rates. The recipe was based on that from [100]. The dry etching process flow was as follows: after device realisation, i.e. Ohmic and gate metal steps (Figure 6.27a), AZ4562 photo-resist was spun at 4000 rpm for 60 seconds followed by baking using hotplate at 100°C for 6:20 min:sec and UV exposure for 25 seconds

(Figure 6.27b), development using AZ400K:H_2O at a ratio of 1:4 for a duration of 2 minutes (Figure 6.27c), dry etching using ICP180 tool with the following gas chemistry: $BCl_3/Cl_2/Ar$ with flow rates 10/14/16 sccm, pressure of 5 mT, ICP power of 800 W and RF power of 200 W with a GaN etch rate of 280 nm/min (Figure 6.27d), photo-resist stripping using 1165 stripper for 30 minutes (Figure 6.27e). At this stage thermal vias are created and the devices are ready to be processed for heat sink deposition.

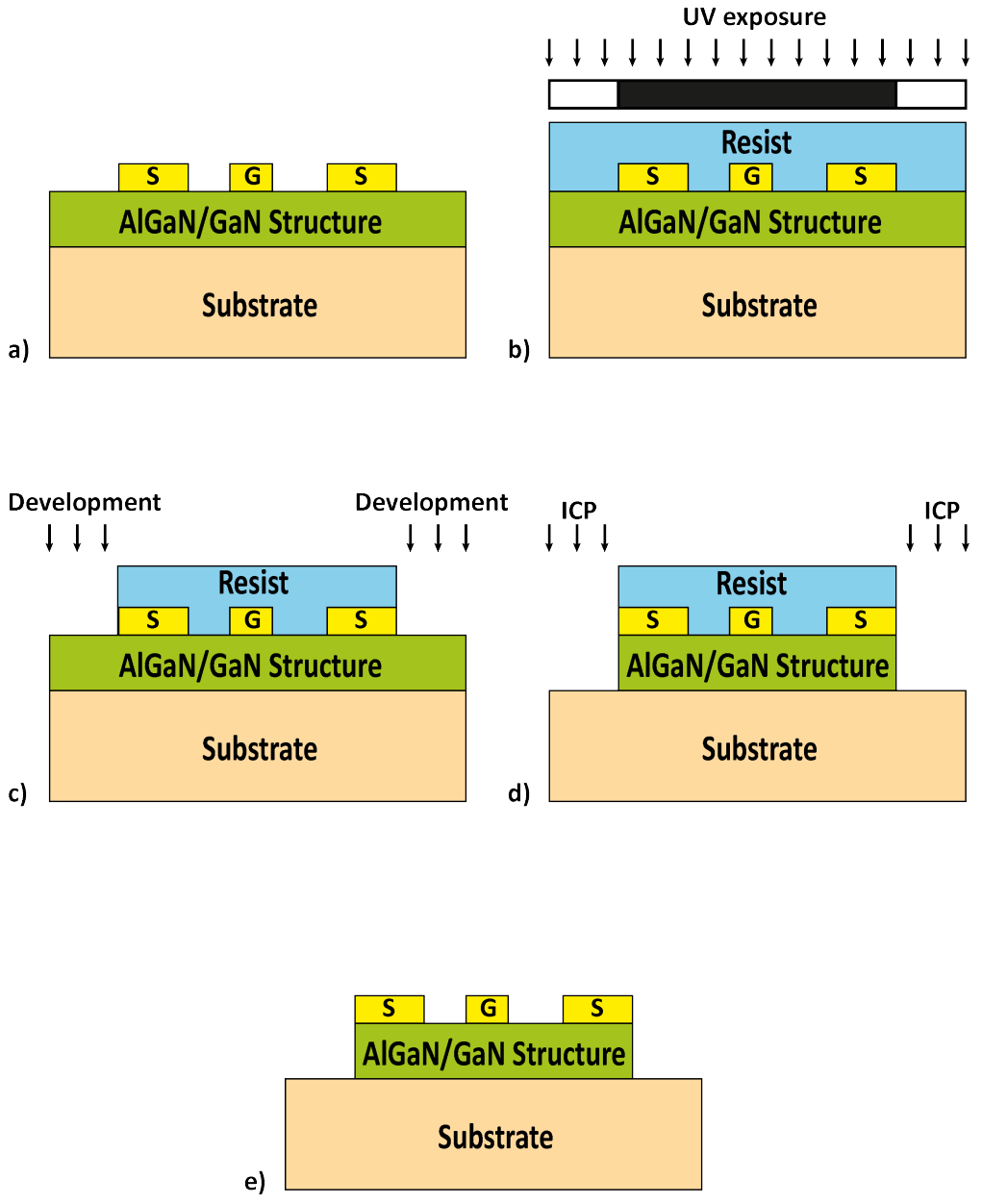

FIGURE 6.27: Illustration of dry etching of nitride epi-layers process flow. Device structure after a) contact deposition , b) photo-resist spinning and UV exposure, c) development, d) nitride epi-layers are etched and totally removed down to the substrate creating thermal vias using ICP dry etching and e) photo-resist stripping.

It is important to realise slanted side walls when doing deep etching. Slanted side walls ensure that the heat sink material deposited later covers the edges uniformly. To achieve a slanted side wall, the photo-resist profile during the etching stage should have a positive slope rather than vertical. This is achievable by post-baking the photo-resist after the development stage, which causes the photo-resist to reflow resulting in a positive slope as illustrated in Figure 6.28. It is, however, very important to control the photo-resist reflow and etching times. Post baking for longer will cause the photo-resist to "over-reflow", causing the etch to extend laterally and damage the Ohmic metal. Overetching the GaN material will also cause the etch to go laterally and damage the Ohmic metal, as shown in Figure 6.29a. Precise control of the photo-resist profile ensures good alignment of the thermal vias with the ohmic metal as shown in Figure 6.29b.

GaN HEMT material on sapphire substrate was used for process development due to its lower cost. Figure 6.30a is an SEM of thermal vias etched into the GaN HEMT material reaching the sapphire substrate. Figure 6.30b is an SEM showing the positively slanted side wall of the etched GaN using the optimised post-bake condition along with the optimised etch recipe. The optimised conditions can define fine features down to 20 μm as shown in Figure 6.31.

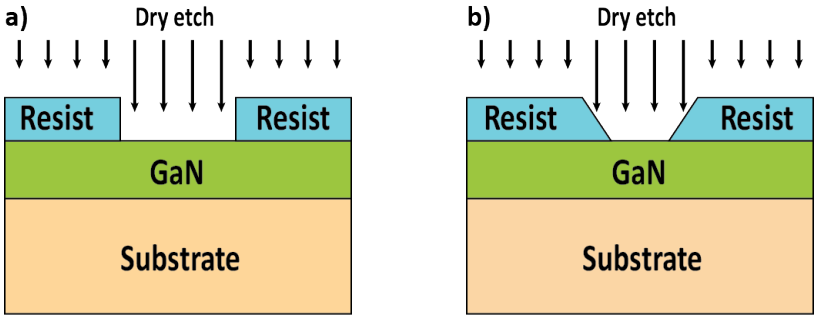

FIGURE 6.28: Illustration of a) non-postbaked photo-resist profile and b) post-baked photo-resist profile.

An interferometer was used during the process development to monitor the etch depth during the etching process [166]. The interferometer is useful in determining when the etch reaches the substrate. It uses a laser beam focussed inside the opening of the photo-resist mask where the epi-layer is to be etched. The laser beam had a wavelength of 905 nm. Figure 6.32 shows the reflectance of the interferometer used to monitor the etch depth. When etching the GaN epi-layers the signal oscillates, but when the etching reaches the substrate the signal becomes flat.

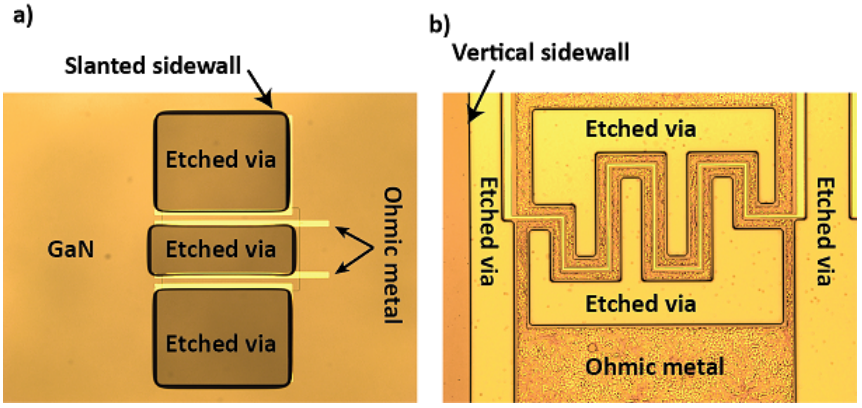

FIGURE 6.29: Optical micrograph of a) etched vias with postbaked photo-resist and b) etched vias with non-postbaked photo-resist.

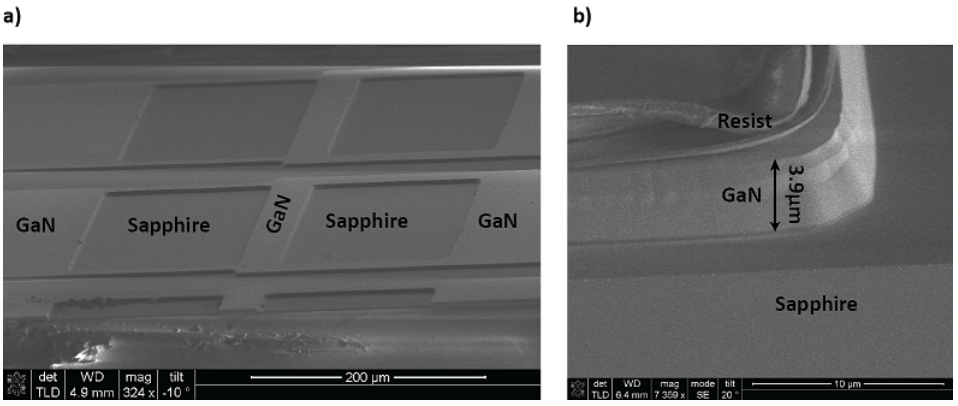

FIGURE 6.30: SEM of a) GaN etched down to the substrate, b) GaN sidewalls with a positive slope.

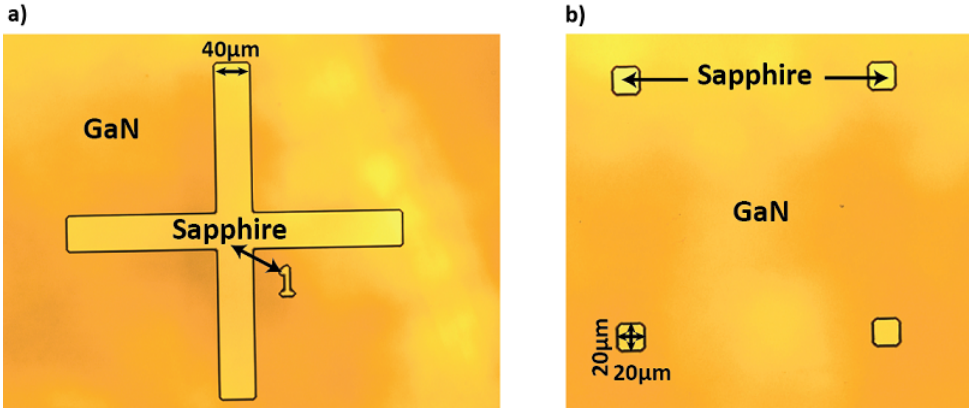

FIGURE 6.31: Optical micrograph of a) features etched into GaN, b) 20 μm square features etched into GaN.

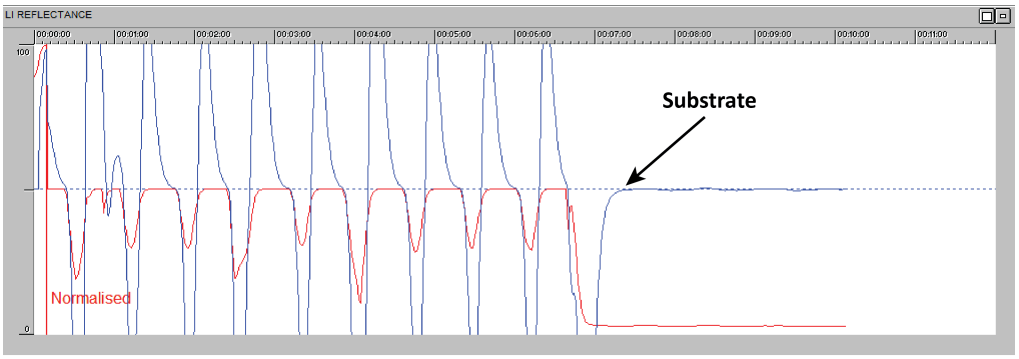

FIGURE 6.32: Reflectance of interferometer to monitor etch depth.

6.8.2 AlN sputtering

At the beginning of this project, the work focused on investigating the feasibility of using sputtered AlN and copper as heat sinks. At first, AlN of various thicknesses was deposited on pre-processed samples to act as a heat sink for the transistors when in operation. Thick (approx. 3 μm) sputtered layers of AlN have a high thermal conductivity of about 200 W/mK, and so if deposited close to the heat source, they can provide a low thermal resistance path for the heat to dissipate into the substrate. Another advantage of AlN is that it is an electrical insulator which means that it can be directly deposited on the surface of devices without the need for an insulator layer. Initial AlN depositions, however, suffered from adhesion issues between AlN and GaN's surface. Figure 6.33 shows a micrograph of a) AlN sputtered on RF GaN devices and b) AlN on the GaN surface in the form of flakes rather than a uniform layer. Therefore, the work moved to focus on using sputtered and evaporated copper heat-sinks which have a thermal conductivity of 400 W/mK.

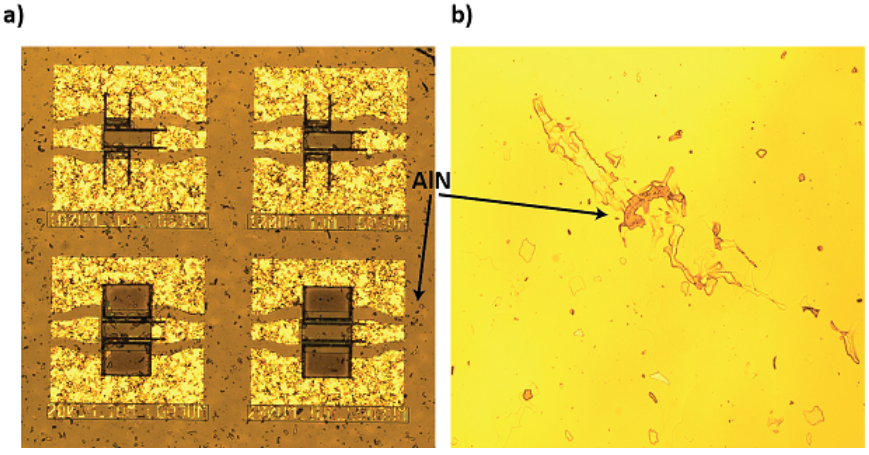

FIGURE 6.33: AlN sputtered on a) fabricated devices and b) GaN surface.

6.8.3 Copper evaporation

At the JWNC, three techniques of realising copper layers are available: evaporation using a thermal evaporator, sputtering and electroplating. Thermal evaporation is the easiest option for lift-off and hence was trialled first. First runs, however, suffered from adhesion problems to the GaN surface. This was attributed to the high stress level in the thick film (1 μm). The stress level could be reduced by reducing the evaporation rate which is challenging when using a thermal evaporator. Therefore sputtering was investigated next.

6.8.4 Copper sputtering

Since sputtering is a physical process, it promotes adhesion of copper with GaN surface. Sputtering has the advantage of the possibility to deposit thick layers copper (3 μm) in a single run compared to the 1 μm limit when using evaporation. One challenge though is that sputtering is non-directional, and therefore causes difficulties with lift-off as it covers the photo-resist sidewalls, which in turn blocks the photo-resist stripping solution from accessing the photo-resist underneath the metal. This is illustrated in Figure 6.34.

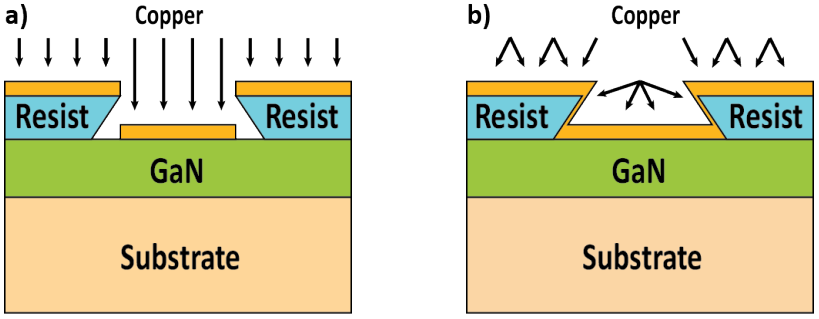

FIGURE 6.34: Illustration of copper metallisation using a) evaporation, b) sputtering.

Since lift-off using sputtered copper proved to be challenging, the blanket sputtering of copper was trialled next to investigate its feasibility. The blanket sputtering process flow illustrated in Figure 6.35, was as follows: after device realisation, i.e. Ohmic and gate metal steps (Figure 6.35a), the sample was covered with 20 nm of ICP-CVD SiN_x (Figure 6.35b). Thereafter, the SiN_x was removed from the thermal via regions using dry etch (RIE system: flow rate CHF_3:O_2 50/5 sccm, pressure 55 mT, power 150 W) with an etch rate of 50 nm/min exposing the nitride layers that were subsequently etched down to the substrate (Figure 6.35c). The next step was a blanket sputtering of copper to create the thermal vias (Figure 6.35d), followed by wet etching of the copper on top of the devices using dilute nitric acid (Figure 6.35e), and finally photo-resist stripping (Figure 6.35f). The use of sputtering was thought to provide better side coverage along

the etched nitride walls compared to metal evaporation. Process development for this work was carried out on an AlGaN/GaN transistor structure on a sapphire substrate.

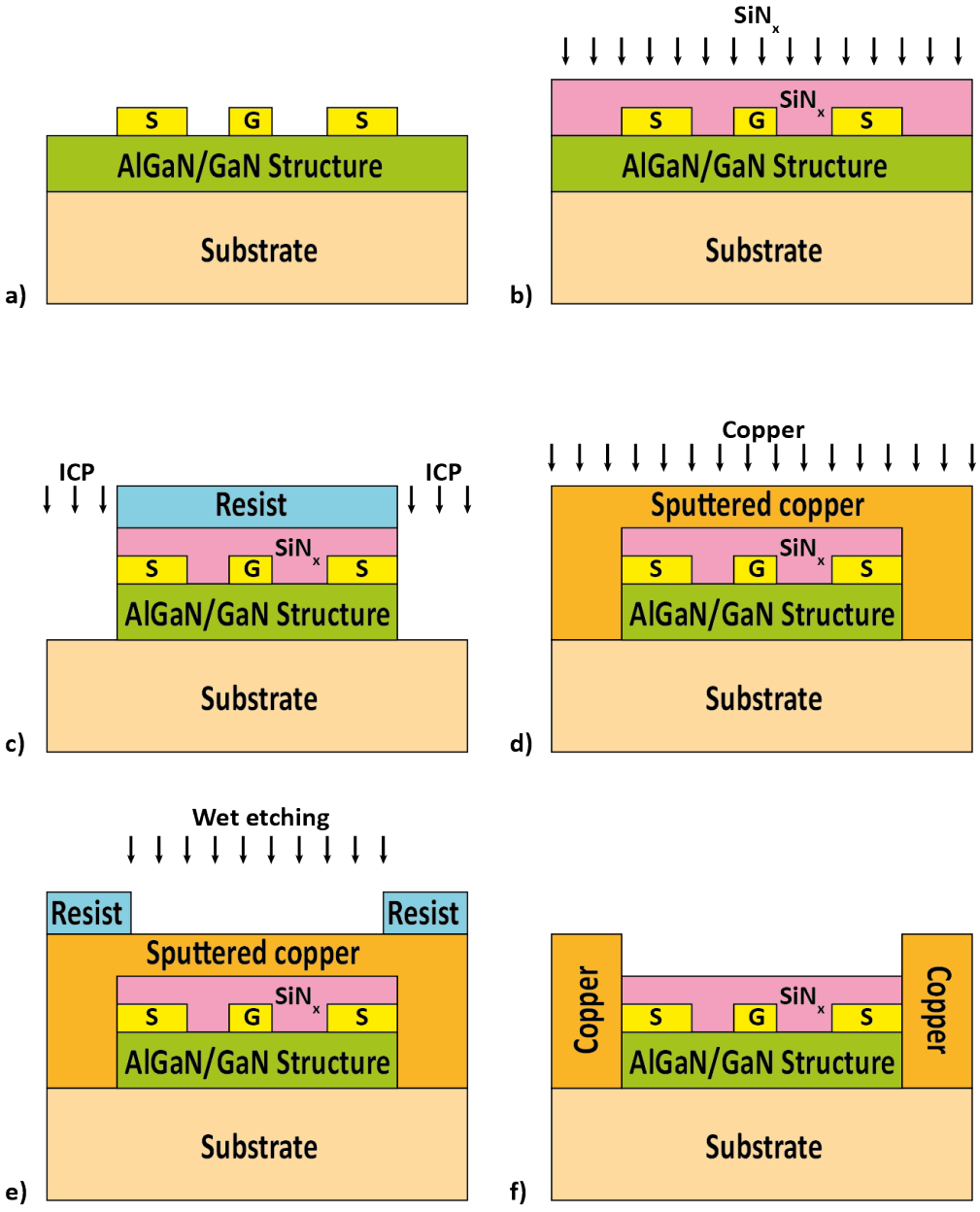

FIGURE 6.35: Illustration of copper wet etching process flow for integrating Cu thermal vias in DC GaN devices. Device structure after a) contact deposition, b) SiN_x passivation, c) nitride epi-layers are etched and totally removed down to the substrate creating a thermal via, d) blanket sputtering of Cu (RF sputtering: Plassys 3, 3 μm thick Cu, pressure of 10^{-3} mT, 250 W RF power), e) patterning of copper to expose the transistor contacts-wet etching using dilute nitric acid (HNO_3:H_2O) 1:5 for 5 minutes: 600 nm/min using AZ4562 photo-resist as an etch mask) and finally f) the remaining photo-resist is stripped using 1165 resist stripper.

The results of copper wet etching are shown in Figure 6.36. These were tested directly on devices. As can be seen from the micrograph, a severe undercut of copper during the

wet etching step leads to the disconnection between the Ohmic contacts and the thermal via, rendering the thermal vias ineffective.

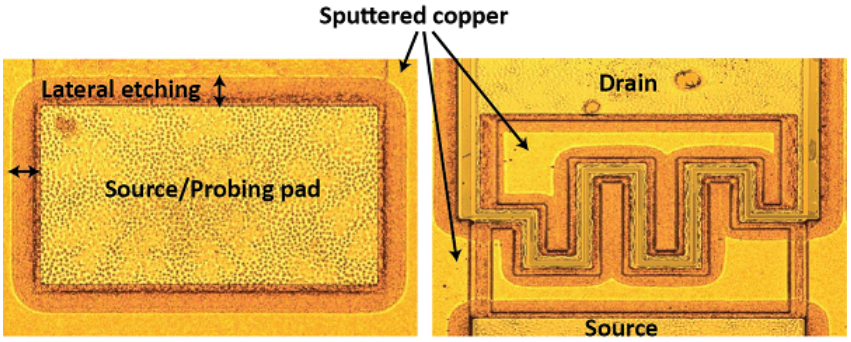

FIGURE 6.36: Copper wet etching results in lateral etching.

6.8.5 Copper electroplating

Electroplating was tested to avoid the issues associated with copper evaporation and sputtering. Electroplating has the advantageous ability to achieve high metal thicknesses. The process flow for electroplating is illustrated in Figure 6.37. The first step (Figure 6.37a) is a repetition of steps a), b) and c) of copper sputtering illustrated in Figure 6.35. This was followed by blanket sputtering of 50 nm of copper that acts as a seed layer, which is necessary to make the electrical connection required for the electroplating process (Fig. 6.37b), which was then followed by lithographically defining the areas to be electroplated (Fig. 6.37c). Then 3 μm of copper was electroplated using a current source of 50 mA. The electroplating rate was 1.6 μm/hour (Fig. 6.37d). The photo-resist was then stripped using flood UV exposure and development, after which the 50 nm copper seed layer was etched using HNO_3:H_2O 1:5 for 1 minute (Fig. 6.37e). Finally the remaining photo-resist was stripped using 1165 resist stripper (Fig. 6.37f).

Figure 6.38 shows a micrograph of 3 μm thick electroplated copper pattern. Good line definition makes this technique practical in realising heat sinks on GaN. Figure 6.39 shows a micrograph of a 10 finger device with 3 μm electroplated copper. The mask was not originally designed for the electroplating process, and therefore some modifications were needed to allow the electroplated copper to be in contact with the Ohmic source and drain metals. This was however not completed during the project due to time constraints.

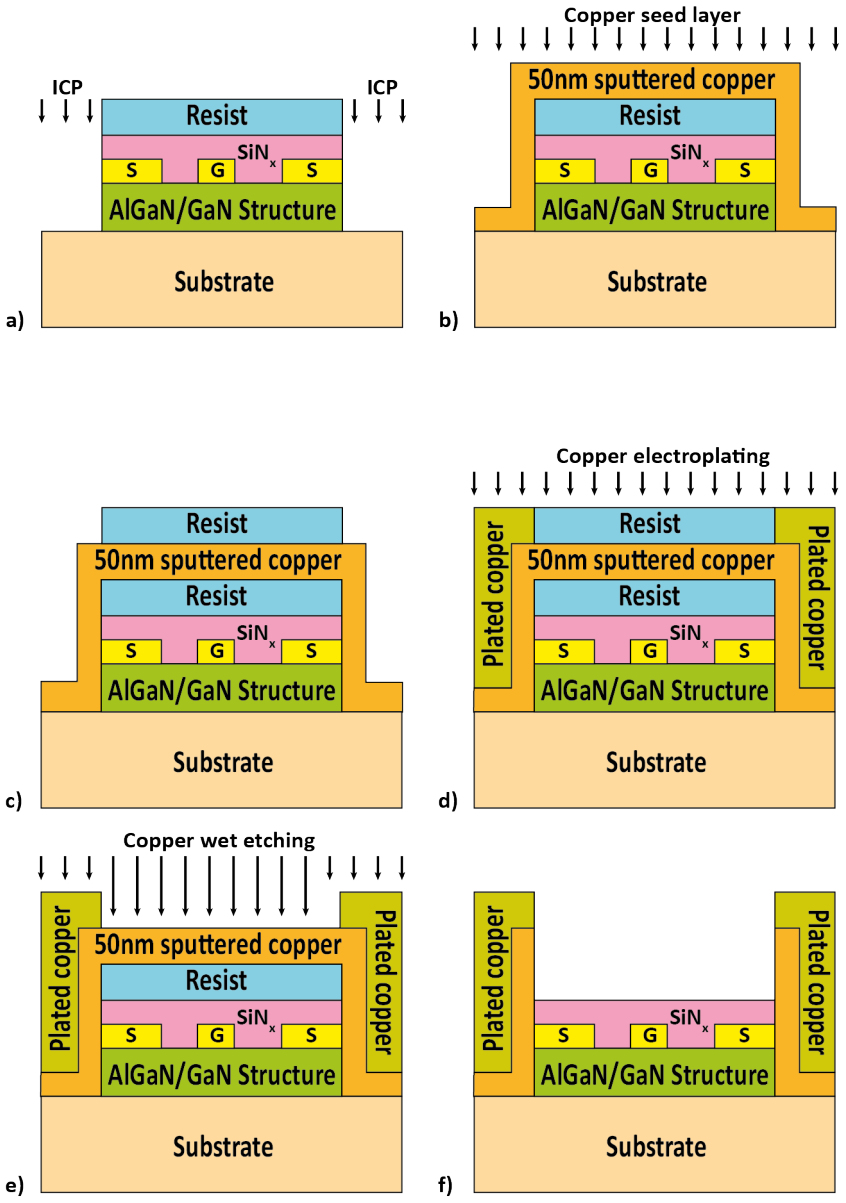

FIGURE 6.37: Copper electroplating process flow. Device structure after a) contact deposition, SiN_x passivation, nitride epi-layers are etched and totally removed down to the substrate creating a thermal via, b) blanket sputtering of Cu seedlayer c) patterning of copper to expose the areas required to be electroplated, d) electroplating 3 μm of copper, e) developing the photo-resist to access the underlying copper seedlayer followed by wet-etching the seed layer using HNO_3:H_2O 1:5 for 1 minute and finally f) the remaining photo-resist is stripped using 1165 resist stripper.

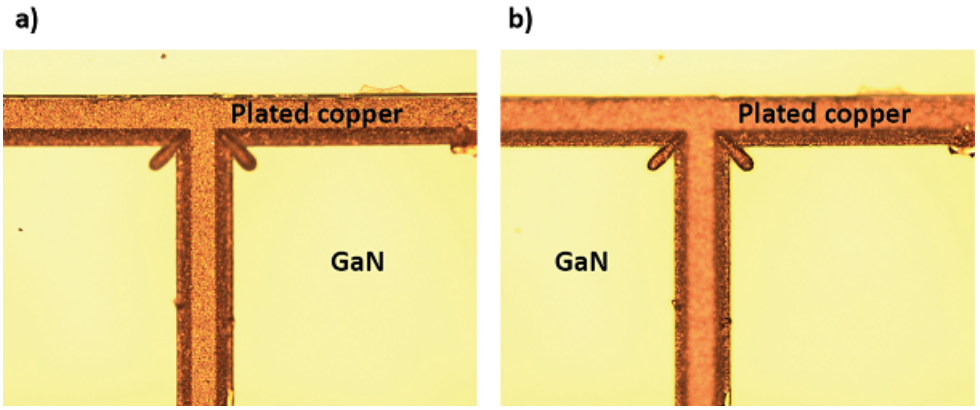

FIGURE 6.38: Micrograph of 3 μm electroplated copper (a) focus on the copper surface and (b) focus on the GaN surface.

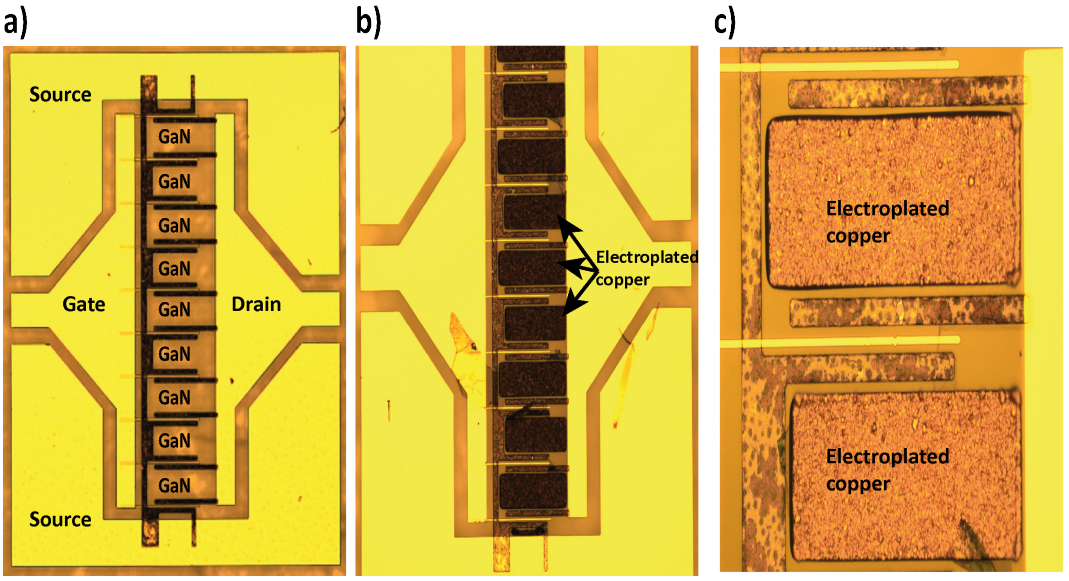

FIGURE 6.39: Micrograph of a 10 finger device a) before etching thermal vias, b) after etching and copper electroplating and c) enlarges image of b) to show the electroplated profile.

6.8.6 Aluminium evaporation

To avoid issues associated with the aforementioned deposition techniques, electron beam evaporation of Ti/Al was used to realise RF devices with integrated heat sinks. Since electron beam evaporation is directional, it offers a reliable lift-off process. The process flow illustrated in Figure 6.40 was as follows: after device realisation, i.e. Ohmic and gate metal steps (Figure 6.40a), the sample was covered with 20 nm SiN_x (Figure 6.40b). Thereafter the SiN_x was removed from the thermal via regions using dry etch (RIE system: flow rate CHF_3:O_2 50/5 sccm, pressure 55 mT, power 150 W) with an etch rate of 50nm/min exposing the nitride layers that were subsequently etched down to

the substrate (Figure 6.40c). The next step was a lift-off process to fill the vias with aluminium (Figure 6.40d) and finally the photo-resist was stripped using 1165 resist stripper, removing the overlying aluminium layer (Figure 6.40e). Figure 6.41 is an SEM of a cross section of evaporated Ti/Al on GaN/sapphire structure. There is no discontinuity in the evaporated metal along the sidewall of the thermal vias.

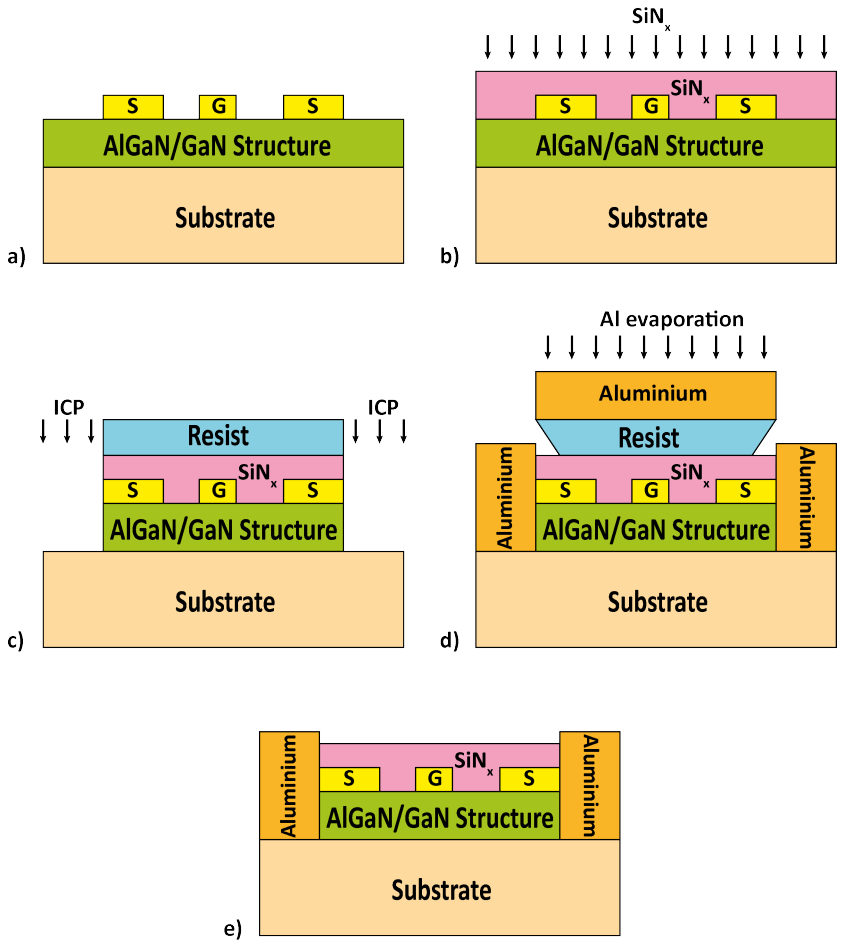

FIGURE 6.40: Illustration of the Al lift-off process flow. Device structure after a) contact deposition, b) SiN_x passivation, c) nitride epi-layers are etched and totally removed down to the substrate creating a thermal via, d) aluminium evaporation using lift-off process and finally e) the remaining photo-resist is stripped using 1165 resist stripper.

Figure 6.42 shows a micrograph of devices with gate widths of 10, 30, 60 and 100 μm. The top batch are standard devices with no etched vias. The bottom batch has the inactive GaN epi-layers around the devices etched down to the substrate. The etched areas are to be later filled with heat sink material (Al or Cu). Figures 6.43 and 6.44 show a micrograph of small (10 and 30 μm wide) and large devices (1 mm wide), respectively. An enlarged micrograph of the large device is shown in Figure 6.45. Good alignment of the etched vias with the Ohmic metal of the device ensures that the device performance is not compromised due to the etching process.

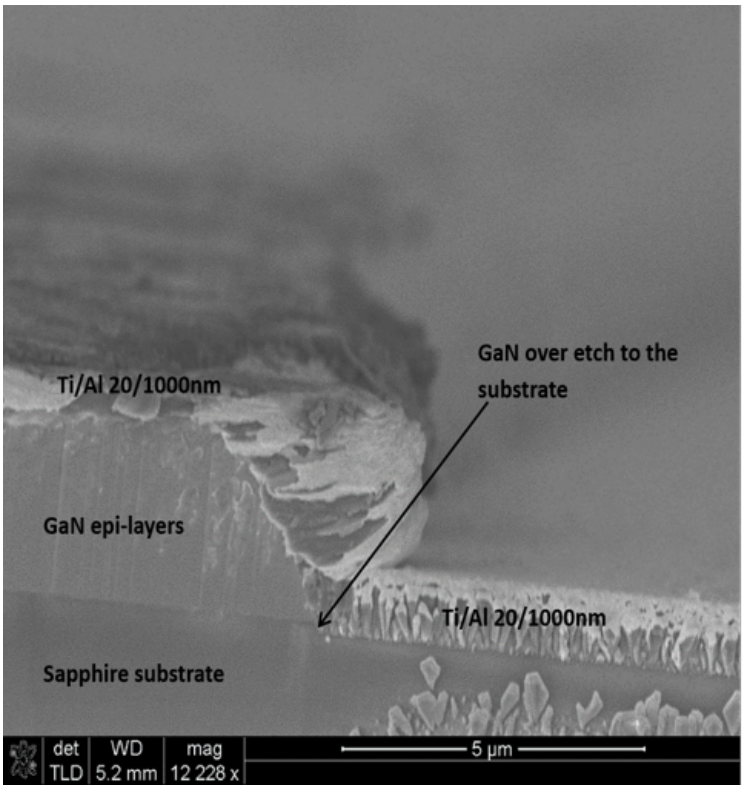

FIGURE 6.41: SEM of evaporated Ti/Al on sapphire substrate with continuous side wall coverage.

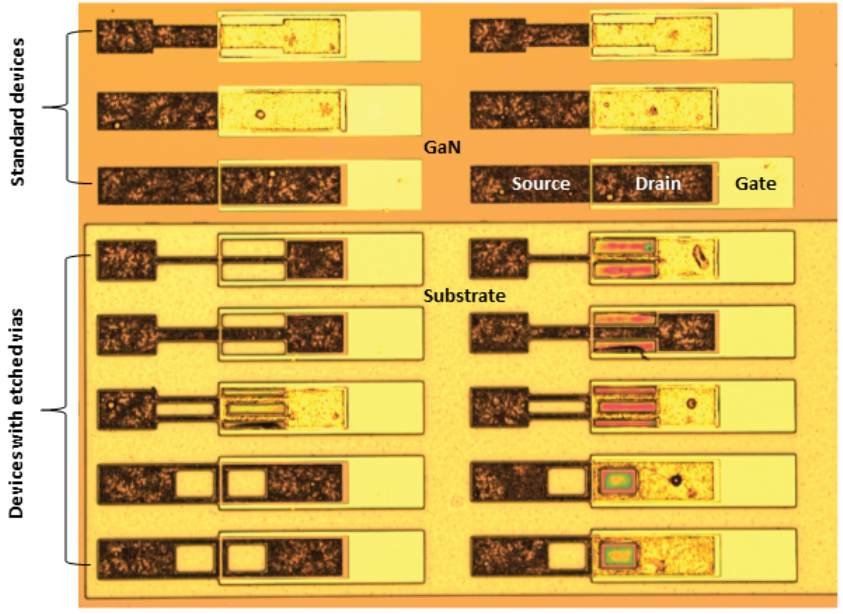

FIGURE 6.42: Micrograph of standard devices and devices with etched vias with gate widths of 10, 30 60 and 100 μm.

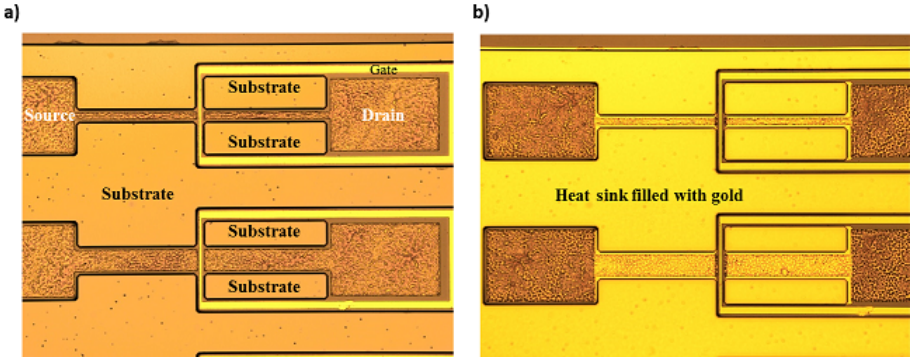

FIGURE 6.43: Micrograph of 10 and 30 μm wide fabricated devices (a) before and (b) after heat sink deposition.

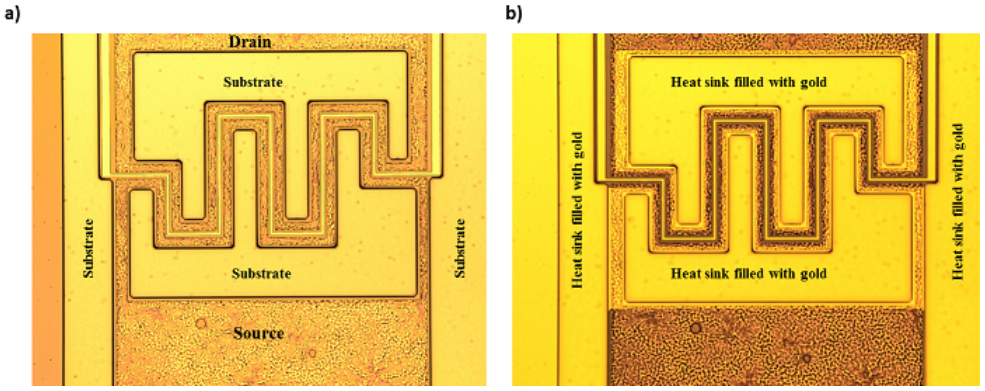

FIGURE 6.44: Micrograph of a 1 mm wide device (a) before and (b) after heat sink deposition.

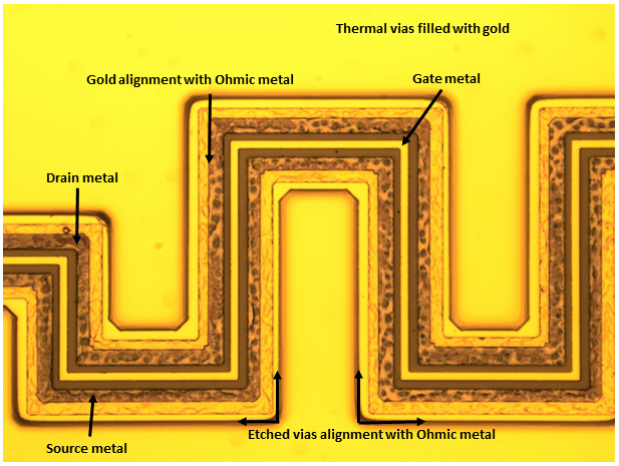

FIGURE 6.45: Micrograph of an enlarged image of a fabricated device after heat sink deposition.

Since these devices were fabricated on a sapphire substrate, the output IV characteristics did not show any improvement after integrating the heat sinks. Also, the fringing fields between the source and the drain of devices without heat sinks made any comparison to those with heat sinks impossible. The main aim at this stage was to develop the mechanical process for the heat sink integration. The developed process was implemented later with RF device layout.

6.9 RF devices with integrated heat sinks

At the beginning of this chapter, device performance on the different substrates was described and the effect of the gate width on the output IV characteristics was shown. To investigate the effect of the heat sink integration on the device performance, the RF layout was used since the device currents are in well defined active regions. The fringing fields in DC devices make them unsuitable to assess the thermal performance of devices with and without heat sinks.

6.9.1 Small periphery devices

Devices with an RF layout and a gate width of 2x100 μm were fabricated on SiC substrates. The devices employed L_G of 3 μm, L_{SD} of 9 μm and L_{GD}, of 3 μm. All fabrication was done using photolithography. Aluminium was chosen for heat sink material due to it's low cost and compatibility with lift-off. Standard device fabrication was done as follows:

1. Sample cleaning using acetone and isopropanol.
2. Ohmic contact metallisation using Ti/Al/Ni/Au (30/180/40/100 nm).
3. Rapid thermal annealing at 800°C for 30 seconds.
4. Device isolation using oxygen plasma treatment.
5. Gate metallisation using Ni/Au (20/200 nm).
6. Bond pad metallisation using Ti/Au (20/200 nm).
7. Dry etch to create thermal vias using ICP 180 dry etching tool.
8. Deposition of 1 μm thick aluminium using electron beam evaporation followed by lift-off.

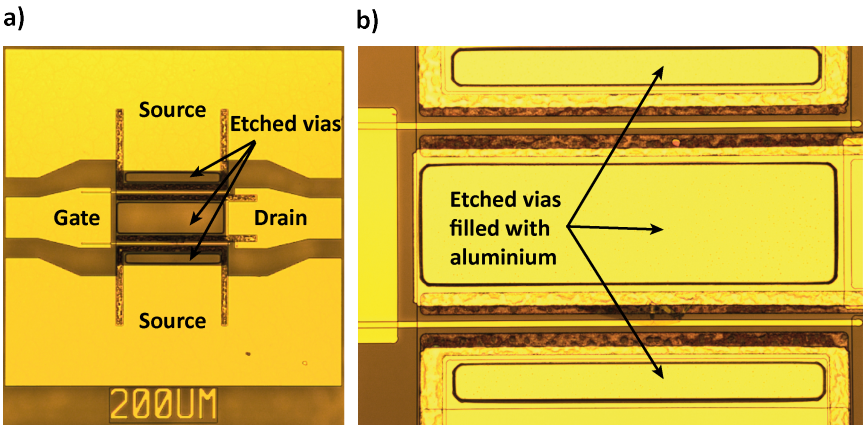

FIGURE 6.46: Micrograph of a fabricated RF device (a) after etching thermal vias and (b) after aluminium heat sink deposition.

The process resulted in good lithography as shown in Figure 6.46.

Figure 6.47 shows the output IV characteristics of standard (as fabricated) and advanced (with integrated heat sinks) AlGaN/GaN-on-SiC HEMT devices at a gate voltage of +1 V. The DC power capability of standard devices was only 15 W/mm at 40 V (due to device self-heating as seen by the drop in drain current with increasing bias), while after heat sink integration there was no noticeable thermal degradation with a DC power density as high as 38 W/mm. This is a promising result as it demonstrates that the integration of thermal vias indeed improves the device thermal performance.

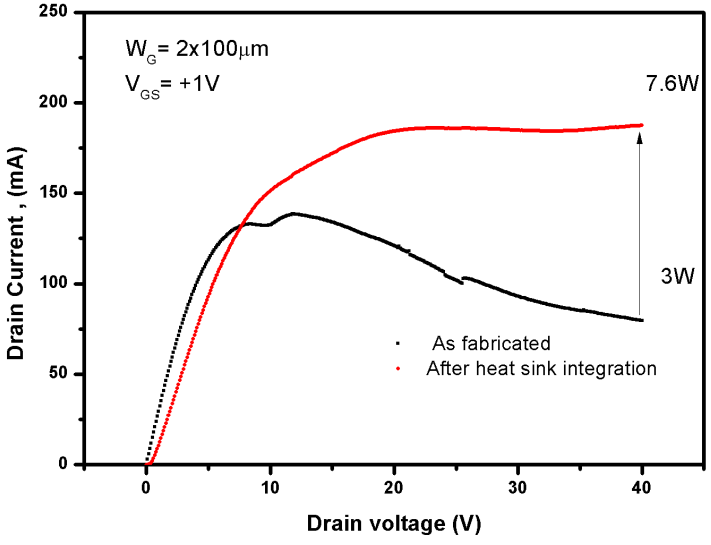

FIGURE 6.47: DC performance of a standard (as fabricated) and advanced (after heat sink integration) AlGaN/GaN on SiC HEMT device.

6.9.2 Large periphery devices

To make high power amplifiers, large periphery area devices are required to deliver high absolute powers. For this project, 10x100 μm devices were fabricated. Ideally, airbridges are required to connect the source terminals. In this case, the airbridge recipe had not been optimised yet. Therefore, an alternative to airbridges was to use a SiN_x layer to isolate the overlap of the gate metal across the source metal. The process flow was the same as for small periphery devices except that before gate metal deposition, a 10nm of ICP-CVD SiN_x is deposited to insulate the gate from the source metal.

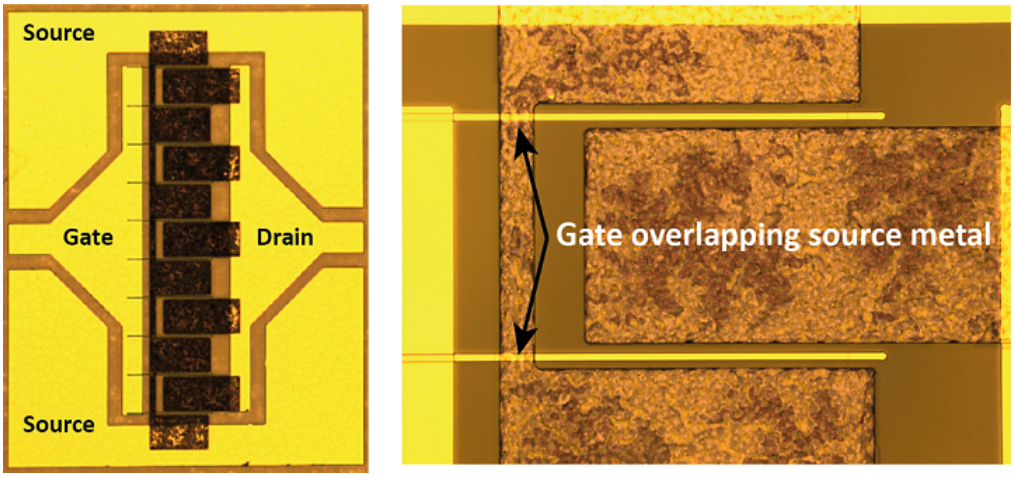

FIGURE 6.48: Micrograph of (a) a 10 finger device and (b) enlarged image to show the gate overlap with the source contact.

Figure 6.48 shows a micrograph of a fabricated 10x100 μm device. For comparison, a 2x100 μm device was fabricated on the same mask. The output IV characteristics of the 2x100 μm and 10x100 μm devices are shown in Figures 6.49 and 6.50. The 2x100 μm finger device exhibit an I_{DS} of 580 mA/mm, while the 10x100 μm finger device sustain I_{DS} of 475 mA/mm at zero gate voltage. The large device did not pinch-off due to the fact that the used insulator was only 10 nm, resulting in high leakage currents. Ideally, if airbridge technology is not used, the gate metal should be deposited first, and the source contact can be connected after deposition of a thick insulator (>100 nm). Large periphery devices of 10 fingers and more are used to achieve higher output power for power amplifier applications while small periphery devices (2 finger) are used for process development as they require less lithography steps. The large periphery devices does not scale linearly due to higher thermal dissipation in the channel and hence there is a tradeoff between the power density and absolute output power when choosing between large area and small area devices.

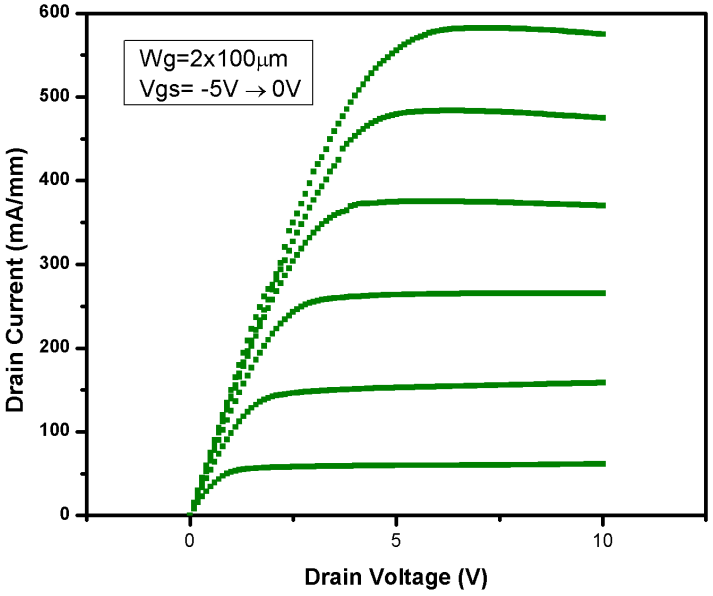

FIGURE 6.49: Output IV characteristics of a 2x100 μm device.

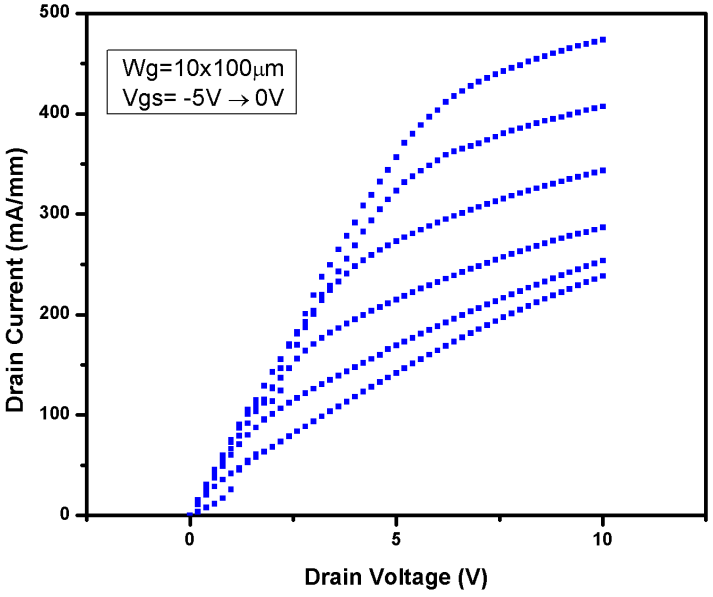

FIGURE 6.50: Output IV characteristics of a 10x100 μm device.

6.10 Summary

This chapter has reviewed GaN-based device performance on three substrates; silicon, sapphire and SiC. The effect of the device width on the current density was demonstrated. It was also demonstrated that as the device width is increased, the current density does not scale linearly due to the locally dissipated heat. The substrate plays a major role in thermal management since it acts as a heat sink. Thermal simulations done in Comsol proved demonstrated the advantage of integrating copper heat sinks over standard devices. Integrated heat sinks resulted in improving the channel temperature from 233°C to 225°C leading to imroved output drain current. Devices with different gate widths were also fabricated and characterised to show the importance of the layout in achieving thermally efficient operation. A novel thermal management technique was proposed, and the preliminary results are promising. More than double the DC power density was demonstrated using the thermal management technique incorporating aluminium as a heat sink metal. The novelty of the thermal vias lies in their location as they sit between the gate fingers and hence, reducing the thermal cross talk between adjacent fingers. For future work, copper is expected to offer enhanced improvement since it has double the thermal conductivity of aluminium (400 W/mK and 200 W/mK, respectively). Preliminary work on large periphery devices was also demonstrated, with room for improvement using airbridge technology. Future work can focus on copper electroplating since good line definition and uniformity across the wafer was achieved, making the electroplating technique practical in realising heat sinks on GaN HEMTs for power amplifier applications. The use of copper seed layer ensures that the TBR is not compromised by the use of a low thermal conductivity material at the interface.

CHAPTER 7

Conclusions and Future Work

The work done in this project has resulted in contributions made to three key areas in GaN technology: Ohmic contacts to AlN/GaN structure, device isolation for GaN based HEMTs and thermal management to AlGaN/GaN HEMT structures. The thesis outlined the motivation behind the research into AlGaN/GaN and AlN/GaN HEMTs based on exploiting their superior properties in terms of high current densities, leading to the delivery of higher output power compared to other technologies. A summary of the main achievements and the future outlook is provided in this chapter.

7.1 Ohmic contacts to AlN/GaN HEMTs

A new AlN/GaN HEMT structure that employs an in-situ SiN_x was demonstrated. CTLM structures were fabricated on the AlN/GaN structure and used to extract the Ohmic contact resistance. The optimised annealing process resulted in a low contact resistance of 0.4 Ω·mm and a sheet resistance of 300 Ω/□. The new Ohmic contact technique can form the basis for realising microwave power amplifier circuits using the AlN/GaN HEMT material for the first time. For future work, transmission electron microscope (TEM) can be used to better understand the exact metal-semiconductor alloying mechanism between the Ohmic metal stack, the in-situ SiN_x passivation layer and the nitride transistor layers.

A new material structure that further improves the Ohmic contacts to AlN/GaN HEMT structure is proposed and is illustrated in Figure 7.1a. It includes a highly doped n-type amorphous GaN cap layer grown on the in-situ SiN_x. The n-doping in the amorphous GaN will reduce the semiconductor-metal barrier width allowing more electrons to tunnel through the barrier. This reduces the Ohmic contact resistance. When annealed, the

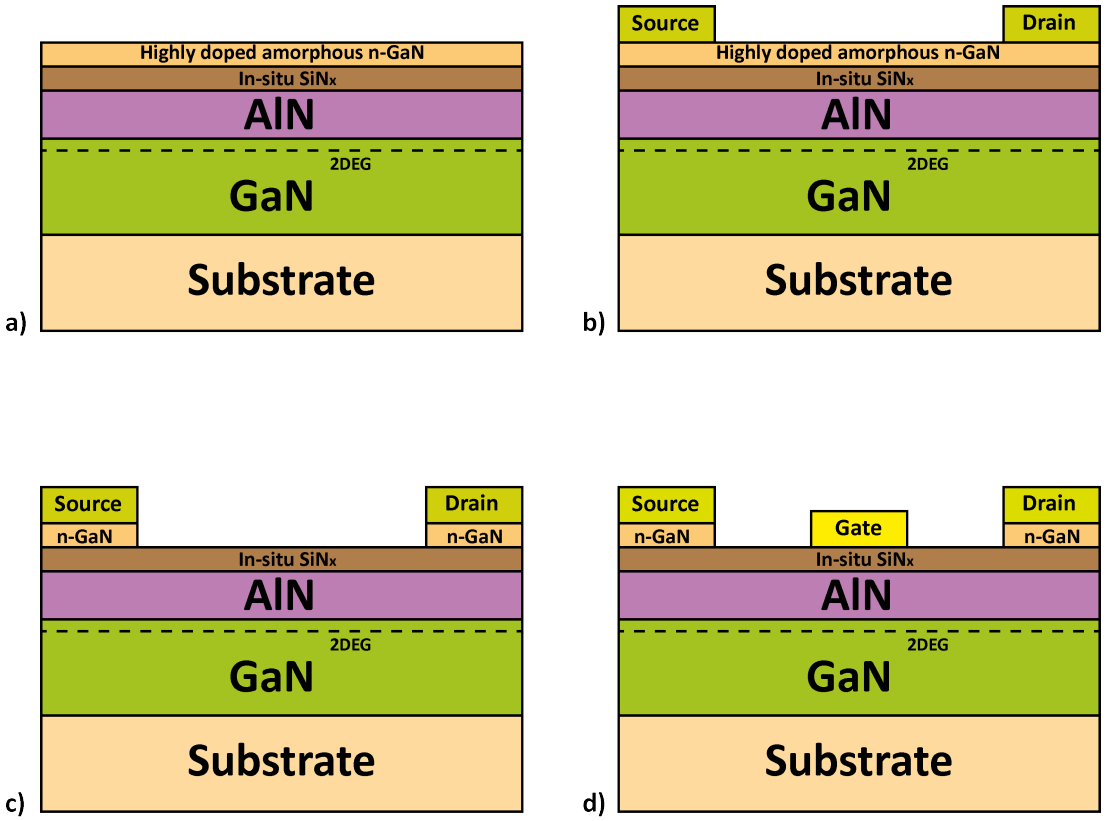

FIGURE 7.1: Illustration of the new Ohmic contact to AlN/GaN material structure a) unprocessed epi-layer structure, b) Ohmic source and drain metals are deposited followed by RTA c) the n-GaN is selectively etched and finally d) the gate metal is directly deposited on the in-situ SiN_x.

Ohmic contact metal will create an alloy with the in-situ SiN_x reaching the GaN buffer which will maintain the low contact resistance. The process flow illustrated in Figure 7.1 starts with depositing the conventional Ohmic source and drain metals, followed by rapid thermal annealing at 800°C for 30 seconds (Figure 7.1b). The conductive n-GaN can then be selectively removed from underneath the gate before the gate metal is deposited directly on top of the insulating in-situ SiN_x (Figure 7.1 (c) and (d)). The n-GaN can be selectively removed using a low power BCl_3/Cl_2 based plasma etch. The in-situ SiN_x should act as a stop layer protecting the underlying AlN barrier layer, and hence preserving the 2DEG channel electron concentration and mobility.

7.2 Device isolation using oxygen plasma

A new technique for achieving device isolation was developed during this project. Devices with RF layout were fabricated and isolated using both the conventional mesa isolation and the new oxygen plasma isolation techniques. Devices isolated using the

new technique demonstrated at least one order of magnitude reduction in gate leakage current from 10 μA/mm to 1 μA/mm at a gate voltage of -20 V and drain voltage of 0 V. Device-to-device isolation currents of 1 μA/mm were achieved at a drain voltage of 10 V. These results are comparable to state of the art devices realised using the more expensive ion implantation [147]. The device performance in terms of output characteristic currents was not compromised.

For future work, further investigation is needed to understand the exact mechanism of isolation using the oxygen plasma treatment. There are two possibilities: surface oxidation [148] or plasma assisted oxygen doping [149], both of which can lead to the depletion of the 2DEG channel. This could be confirmed by using many techniques to look for the presence of oxygen ions or oxidised GaN layers. These include low temperature photoluminescence (PL) [150], Raman spectroscopy [138], or high resolution x-ray diffraction (HRXRD) [151] to examine the cross section of the GaN HEMT structure after the oxygen plasma treatment.

7.3 Thermal management on AlGaN/GaN HEMTs

A new approach to thermal management of GaN based devices was demonstrated. The approach depends on the top side removal of the inactive GaN epi-layers between gate fingers using dry etching techniques. The resulting vias can be later filled with copper, a high thermally conducting metal that can efficiently transport the heat from where it is generated, at the 2DEG channel, to the substrate. The approach was demonstrated using integrated aluminium heat sinks. Devices with integrated heat sinks sustained 38 W/mm of output DC power density compared to standard devices sustaining only 15 W/mm at 40 V. The proposed approach is therefore promising for realising high power high frequency amplifiers with high efficiency. More thermal analysis is however needed to investigate the effect of the new heat sink technique on the channel temperature. The different techniques to achieve this include pulsed IV characterisation, micro Raman spectroscopy, thermal imaging or thermal surface profiling. In addition, the thermal resistance of the interface between copper heat sinks and GaN epi-layers needs to be determined. The channel temperature can also be measured to determine the extent of channel temperature reduction as a result of the integrated heat sinks.

In summary, this project delivered basic transistor design and fabrication processes that enable the realisation of devices suitable for implementing highly efficient practical amplifiers for radar systems and other applications.

Appendix A

GaN Based HEMT Device Fabrication

A.1 RF device fabrication using photolithography

A.1.1 Sample cleaning

1. Ultrasonic bath in acetone for 15 mins
2. Isopropyl alcohol (IPA) for 5 mins
3. Rinse with reverse osmosis (RO) water for 60 secs
4. Blow dry with N_2

A.1.2 Ohmic contacts

1. Clean sample
2. Spin LOR 10A photo-resist at 6000 rpm for 30 secs
3. Bake on hotplate for 2 mins at 150 °C
4. Spin S1818 photo-resist at 4000 rpm for 30 secs
5. Bake on hotplate for 3 mins at 115 °C
6. Expose using Mask Aligner (MA6) for 6 secs
7. Develop in MF319 developer for 150 secs

8. Rinse in RO Water for 60 secs
9. Blow dry with N_2
10. Oxygen ash in Gala Asher for 3 mins at 40 W
11. De-oxidise in $4H_2O$:HCl for 1 min
12. Deposit Ti/Al/Ni/Au 30/180/40/100 nm using electron beam evaporator
13. Soak in warm 1165 resist stripper (50 °C) for 15 mins for lift-off
14. Rinse in RO water for 30 secs
15. Blow dry with N_2
16. Anneal the sample at 800 °C for 30 sec in an N_2 environment

A.1.3 Device isolation

The process flow for the two device isolation techniques, mesa isolation and oxygen plasma are listed below:

A.1.3.1 Device isolation using mesa isolation

1. Clean sample
2. Spin S1818 photo-resist at 4000 rpm for 30 secs
3. Bake on hotplate for 2 mins at 110 °C
4. Expose using Mask Aligner (MA6) for 6 secs
5. Develop using 1:1 Microdeveloper:H_2O for 45 secs
6. Rinse in RO water for 60 secs
7. Blow dry with N_2
8. Oxygen ash in BP80 RIE tool with a power of 60 W, oxygen gas flow rate of 20 sccm and pressure of 20 mT for 3 mins
9. Bake in oven at 90 °C for 3 mins
10. Dry etch AlGaN/GaN using T-gate RIE tool with $SiCl_4$ flow rate of 25 sccm, chamber pressure of 8 mT and power of 75 W power for 4 mins

11. Soak in warm acetone (50 °C) for 15 mins for removing the resist
12. Rinse in IPA for 30 secs
13. Blow dry with N_2

A.1.3.2 Device isolation using oxygen plasma

1. Clean sample
2. Spin S1818 photo-resist at 4000 rpm for 30 secs
3. Bake on hotplate for 2 mins at 110 °C
4. Expose using Mask Aligner (MA6) for 6 secs
5. Develop using 1:1 Microdeveloper:H_2O for 45 secs
6. Rinse in RO water for 60 secs
7. Blow dry with N_2
8. Bake in oven at 90 °C for 3 mins
9. Oxygen ash in BP80 RIE tool with a power of 200W, oxygen gas flow rate of 20sccm and pressure of 20mT for 5 mins
10. Soak in warm acetone (50 °C) for 15 mins for removing the photo-resist
11. Rinse in IPA for 30 secs
12. Blow dry with N_2

A.1.4 Gate contacts

1. Clean sample
2. Spin LOR 10A photo-resist at 6000 rpm for 30 secs
3. Bake on hotplate for 2 mins at 150 °C
4. Spin S1818 photo-resist at 4000 rpm for 30 secs
5. Bake on hotplate for 3 mins at 115 °C
6. Expose using Mask Aligner (MA6) for 6 secs
7. Develop in MF319 developer for 150 secs

8. Rinse in RO water for 60 secs
9. Blow dry with N_2
10. Oxygen ash in Gala Asher for 3 mins at 40 W
11. Deposit Ni/Au 20/200 nm
12. Soak in warm 1165 photo-resist stripper (50 °C) for 15 mins for lift-off
13. Rinse in water for 30 sec
14. Blow dry with N_2

A.1.5 Bondpads

1. Clean sample
2. Spin LOR 10A photo-resist at 6000 rpm for 30 secs
3. Bake on hotplate for 2 mins at 150 °C
4. Spin S1818 photo-resist at 4000 rpm for 30 secs
5. Bake on hotplate for 3 mins at 115 °C
6. Expose using Mask Aligner (MA6) for 6 secs
7. Develop in MF319 developer for 150 secs
8. Rinse in RO water for 60 secs
9. Blow dry with N_2
10. Oxygen ash in Gala Asher for 3 mins at 40 W
11. Deposit Ti/Au 20/200 nm
12. Soak in warm 1165 photo-resist stripper (50 °C) for 15 mins for lift-off
13. Rinse in RO water for 30 secs
14. Blow dry with N_2

A.1.6 Thermal via etching

1. Clean sample
2. Spin AZ4562 photo-resist at 4000 rpm for 60 secs
3. Bake on hotplate for 6:20 mins:sec at 100 °C
4. Leave sample to rehydrate for 10 min before exposure
5. Expose using Mask Aligner (MA6) for 25 secs
6. Develop in AZ400K:H_2O at a ratio of 1:4 for 2 mins
7. Rinse in RO Water for 60 secs
8. Blow dry with N_2
9. Oxygen ash in Gala Asher for 2 mins at 200 W
10. Hard bake using hotplate at 120 °C for 2 mins
11. Dry etch in ICP180 tool with BCl3/Cl_2/Ar with flow rates of 10/14/16sccm, pressure of 5mT, ICP power of 800W and RF power of 200W for a duration of 15min
12. Soak in warm 1165 photo-resist stripper (50 °C) for 15 mins for lift-off
13. Rinse in RO water for 30 secs
14. Blow dry with N_2

A.1.7 Copper heat-sink sputtering

1. Clean sample
2. Spin AZ2070 negative photo-resist at 4000 rpm for 60 secs
3. Bake on hotplate for 1:30 min:secs at 110 °C
4. Expose using Mask Aligner (MA6) for 20 secs
5. Post bake on hotplate for 1 min at 110 °C
6. Develop in MF319 developer for 3 mins
7. Rinse in RO Water for 60 secs
8. Blow dry with N_2

9. Oxygen ash in Gala Asher for 2 mins at 200 W
10. Sputter 1000nm of copper using plassys 3
11. Soak in warm 1165 photo-resist stripper (50 °C) for 120 mins for lift-off
12. Rinse in RO water for 30 secs
13. Blow dry with N_2

A.1.8 Copper heat-sink electroplating

1. Clean sample
2. Spin AZ4562 photo-resist at 4000 rpm for 30 secs
3. Bake using oven at 90 °C for 30mins
4. Leave sample to rehydrate for 10 min before exposure
5. Expose using Mask Aligner (MA6) for 15 secs
6. Develop in AZ400K:H_2O at a ratio of 1:4 for 2 mins
7. Rinse in RO Water for 60 secs
8. Blow dry with N_2
9. Oxygen ash in Gala Asher for 2 mins at 200 W
10. Hard bake using oven at 120 °C for 10 mins
11. Dry etch in ICP180 tool with BCl3/Cl_2/Ar with flow rates of 10/14/16 sccm, pressure of 5 mT, ICP power of 800 W and RF power of 200 W for a duration of 15 min
12. Sputter 100 nm of copper as a seed layer
13. Spin S1818 photoresist at 3000 rpm for 30 seconds
14. Bake using oven at 90 °C for 15 mins
15. Expose using Mask Aligner (MA6) for 15 secs
16. Develop in MF319 for 75 secs
17. Rinse in RO Water for 60 secs
18. Blow dry with N_2

19. Oxygen ash in Gala Asher for 3 mins at 60 W
20. Electroplate 3 μm of copper using a current source of 50mA for 2 hours
21. Flood expose using Mask Aligner (MA6) for 15 secs
22. Develop in MF319 for 75 secs
23. Etch 100 nm copper seed layer using HNO_3:H_2O for 60 secs
24. Soak in warm 1165 photo-resist stripper (50 °C) for 15 mins for lift-off
25. Rinse in water for 30 secs
26. Blow dry with N_2

A.1.9 Aluminium heat-sink evaporation

1. Clean sample
2. Spin AZ2070 negative photo-resist at 4000 rpm for 60 secs
3. Bake on hotplate for 1:30 min:secs at 110 °C
4. Expose using Mask Aligner (MA6) for 20 secs
5. Post bake on hotplate for 1 min at 110 °C
6. Develop in MF319 developer for 3 mins
7. Rinse in RO Water for 60 secs
8. Blow dry with N_2
9. Oxygen ash in Gala Asher for 2 mins at 200 W
10. Deposit Ti/Al 20/1000 nm
11. Soak in warm 1165 photo-resist stripper (50 °C) for 30 mins for lift-off
12. Rinse in RO water for 30 secs
13. Blow dry with N_2

A.2 RF device fabrication using E-beam lithography

For RF device fabrication using electron beam evaporation, the ohmic contacts and gate contacts are realised using electron beam lithography.

A.2.1 E-beam alignment markers

The electron beam (E-beam) markers are realised using dry etching with the same process described in A.1.6 except for the etch duration of 5mins.

A.2.2 Ohmic contacts

1. Clean sample
2. Spin 12%2010 PMMA E-beam resist at 5000 rpm for 60 secs
3. Bake on hotplate for 2 mins at 155 °C
4. Spin 4%2041 PMMA E-beam resist at 5000 rpm for 60 secs
5. Bake on hotplate for 2 mins at 155 °C
6. Evaporate 10nm of Al as a discharge layer
7. Expose using leica VB6 E-beam tool with a dose of 700μCcm^{-2}, a beam current of 32nA and a variable resolution unit of 25
8. Soak in CD-26 for 4 mins
9. Rinse in RO Water for 60 secs
10. Blow dry with N_2
11. Develop with MIBK:IPA 2.5:1 for 45 secs at 23°
12. Rinse in IPA Water for 15 secs
13. Blow dry with N_2
14. Oxygen ash in Gala Asher for 3 mins at 40 W
15. De-oxidise in 4H_2O:HCl for 1 min
16. Deposit Ti/Al/Ni/Au 30/180/40/100nm using electron beam evaporator
17. Soak in warm acetone (50 °C) for 15 mins for removing the resist
18. Rinse in IPA for 30 sec
19. Blow dry with N_2
20. Anneal the sample at 800 °C for 30 sec in an N_2 environment

A.2.3 Device isolation

The process for realising device isolation is similar to the one described in A.1.3.

A.2.4 T-Gate process flow

1. Clean sample
2. Spin 4%2041 PMMA E-beam resist at 5000 rpm for 60 secs
3. Bake on hotplate for 90 secs at 155 °C
4. Spin 4%2041 PMMA E-beam resist at 5000 rpm for 60 secs
5. Bake on hotplate for 90 secs at 155 °C
6. Evaporate 10 nm of Al as a discharge layer
7. Spin 8%2010 PMMA E-beam resist at 5000 rpm for 60 secs
8. Bake on hotplate for 90 secs at 155 °C
9. Spin 8%2010 PMMA E-beam resist at 5000 rpm for 60 secs
10. Bake on hotplate for 90 secs at 155 °C
11. Spin 2.5%2041 PMMA E-beam resist at 5000 rpm for 60 secs
12. Bake on hotplate for 90 secs at 155 °C
13. Evaporate 10 nm of Al as a discharge layer
14. Expose using leica VB6 E-beam tool with a foot dose of 1000 μCcm^{-2}, a beam current of 4nA and a variable resolution unit of 4. The head dose is 430 μCcm^{-2}, a beam current of 8nA and a variable resolution unit of 10
15. Soak in CD-26 for 4 mins
16. Rinse in RO Water for 60 secs
17. Blow dry with N_2
18. Develop with MIBK:IPA 2.5:1 for 40 secs at 23°
19. Rinse in IPA Water for 15 secs
20. Blow dry with N_2
21. Soak in CD-26 for 100 secs

22. Rinse in RO Water for 60 secs
23. Develop with MIBK:IPA 2.5:1 for 40 secs at 23°
24. Rinse in IPA Water for 15 secs
25. Blow dry with N_2
26. Deposit Ni/Au 20/400 nm using electron beam evaporator
27. Soak in warm acetone (50 °C) for 15 mins for removing the E-beam resist
28. Rinse in IPA for 30 secs
29. Blow dry with N_2

A.2.5 Bondpads

The process for realising bondpads is similar to the one described in A.1.5.

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