25 years of Network Access Technologies: From Voice to Internet; the changing face of telecommunications

Duncan James Bremner

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Abstract

This work contributes to knowledge in the field of semiconductor system architectures, circuit design and implementation, and communications protocols.

The work starts by describing the challenges of interfacing legacy analogue subscriber loops to an electronic circuit contained within the Central Office (Telephone Exchange) building. It then moves on to describe the globalisation of the telecom network, the demand for software programmable devices to enable system customisation cost effectively, and the creation of circuit and system blocks to realise this.

The work culminates in the application challenges of developing a wireless RF front end, including antenna, for an Ultra Wideband communications systems applications.

This thesis illustrates how higher levels of integration over the period of 1981 to 2010 have influenced the realisation of complex system level products, particularly analogue signal processing capabilities for communications applications. There have been many publications illustrating the impact of technology advancement from an economic or technology perspective. The thesis shows how technology advancement has impacted the physical realisation of semiconductor products over the period, at system, circuit, and physical implementation levels.

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Author's Declaration

Declaration

The content of this thesis is a culmination of my work in industry over 28 years. Some of the publications submitted are the work of multiple contributors and I have acknowledged the contribution made by others. Clear reference is provided to third party material or information from others.

Duncan J Bremner
May 2015

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Acknowledgements

I would like to thank Professor David Hutchings, and other members of the academic staff in the University of Glasgow who have cajoled, persuaded, and encouraged me to complete and submit this thesis. I would like to acknowledge the expertise and professionalism of all my co-workers over the years who I have worked alongside in the creation of many of the innovations and products upon which this submission for a PhD via published works is based. I am particularly grateful to Mr Ray A Reed, Mr Roger K Benton, and Mr James B Wieser whose patience, dedication, and engineering integrity provided me with the rigorous training and foundation upon which to build my engineering confidence. Finally, I must acknowledge the late Roderick A. M. Gunn, my grandfather and a telephone engineer with the GPO, whose encouragement first sparked my interest in telecommunications and electronics back in the 1970s.

Table of Acronyms and Abbreviations

A-Law	PCM Coding Algorithm defined in G.711 (ITU-T); used in Rest of World (RoW)
APD	Avalanche Photodiode
ASIC	Application Specific Integrated Circuit
AWG	Arrayed Wave Guide
BS	Beam-splitter
BER	Bit Error Rate/Ratio
BERT	Bit Error Rate Testing
BTB	Back to Back
CMOS	Complementary Metal Oxide Semiconductor
CO	Central Office (Exchange)
CSIC	Customer Specific Integrated Circuit
CSMA/CD	Carrier Sense Multiple Access / Collision Detect
CO	Central Office
CoDec	Coder /Decoder; converts voice to/from PCM data
COMBO™	Combined CoDec / Filter pair; ™ of National Semiconductor
CW	Continuous Wave
DPD	Dial Pulse Distortion
EAM	Electro-Absorption Modulator
FFT	Fast Fourier Transform
FttH	Fibre to the Home
FttB	Fibre to the Building
FttC	Fibre to the Kerb
FttX	Fibre to the X (Generic term for fibre in the loop)
GDT	Gas Discharge Tube; Protection Device
GPON	Gigabit-capable Passive Optical Network
HDMI	High Definition Media Interface
IP	Internet Protocol
IPTV	Internet Protocol Television
ISDN	Integrated Services Digital Network
ISI	Intersymbol Interference
ITU	International Telecommunication Union
ITU-T	ITU Telecommunication Standardisation Body
MM	Multimode

MoDem	Modulator /Demodulator
NF	Noise Figure
O-E-O	Optical to Electrical to Optical
OLT	Optical Line Termination
ONU	Optical Network Unit
PIR	Passive InfraRed (Detector)
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDH	Pleisochronous Digital Hierarchy
PMD	Polarisation Mode Dispersion
PON	Passive Optical Network
POTS	Plain Old Telephone Service
QoS	Quality of Service
RHS	Right Hand Side
RMS	Root Mean Square
RoW	Rest of World; usually outside USA
RZ / NRZ	Return to Zero / Non-Return to Zero
SiO2	Silicon Dioxide / Silica
SM	Single Mode
SNR	Signal to Noise Ratio
SOA	Semiconductor Optical Amplifier
SONet	Synchronous Optical Network
SDH	Synchronous Digital Hierarchy
SLIC	Subscriber Line Interface Circuit
SLIM™	Subscriber Line Interface Module; ™ National Semiconductor
TDM	Time Division Multiplexing
TDMA	Time Division Multiple Access
VoIP	Voice over IP (Internet Protocol)
WAN	Wide Area Network
μ-Law	PCM Coding Algorithm defined in G.711 (ITU-T); used in USA
WDM	Wavelength Division Multiplexing
xDSL	One of the high speed subscriber line digital interfaces (ADSL, SDSL, VHDL etc)

Preface

This thesis is submitted under Schedule B: Degree of Doctor of Philosophy by Published Work to the University of Glasgow, School of Engineering. The work represents the published work by the author in the field of communications over a 28 year career in industry developing products to address a global market. The career started in the early 1980's as the semiconductor industry was growing from a $7Bn (1980) [1] global market into the $305Bn in 2012 [2]. It was this growth, combined with the introduction of low cost Application Specific Integrated Circuits (ASICS) that fuelled the worldwide growth in communications services, delivering the essential infrastructure which spawned the 'internet age'. With the availability of ASICs, low volume, high value processing functions such as complex telecommunications switching units became possible. The patents and commercial publications submitted examine the impact of both ASICs and Customer specific ICs (CSICs) on the modernisation of the telecommunications network deployed by the world's telecom operators.

The under-pining field of study is semiconductor technology, specifically analogue circuit and system design and development as applied to telecommunications, with specific emphasis on the replacement and modernisation of the Central Office (Exchange) switches and network access equipment [3], [4]. The material submitted shows the development and adoption of technology to enable cost effective network access over both copper and optical fibre to customers' premises. The work then explores one potential candidate for wireless local area networking to realise high density high speed connectivity for use in domestic or small office environments [5].

Due to the commercial nature of the work, the ownership of the original results, schematics, calculations, and intellectual property belong to the author's employer at the time and are no longer accessible. The material presented is freely available in the public domain in the form of patents, trademarks, publications, or product datasheets. Where analysis has been presented, this has been generated from information contained within these public records or re-created from first principles in order to demonstrate the novelty captured within the topic.

These 12 submissions represent some of the leading innovations serving the communications market at the time, and illustrate the development and evolution of network access technologies from the early digitisation of the network [6], through the exploration and deployment challenges of optical access technologies, into a proposal for next generation wireless access.

The work presented can be divided into three distinct themes in network access technologies:-

1. Analogue Subscriber Line Interface Circuit (SLIC) [7] Access Technology incorporating circuit and architecture innovations to deliver lower cost, lower power, more flexible solutions to the challenges presented to operators implementing digital network upgrades (9 submissions).

2. Optical access technology for multi-wavelength point-to-point network to deliver 10 Gigabit access directly into end user premises, and the impact of high data rates on the core network (1 submission).

3. Wireless network access technologies with emphasis on Ultra-Wideband communications customer premise equipment for high speed, in premise customer connections (2 submissions).

Explanatory Essay

A short history of telecommunications

In 1876, when Alexander Graham Bell spoke the immortal words, *"Mr. Watson, come here, I want you!"* [8], the telephone was born and later patented by the Bell Telephone Company, eventually to become AT&T, the world's largest telecommunications company. The invention of the telephone was of such significance that Sir William Thompson (later Lord Kelvin) exhibited Bell's telephone to the British Association for the Advancement of Science at Glasgow in September 1877; he described it as "*the greatest by far of all the marvels of the electric telegraph*" [9]. Thus began the development and migration of the original telegraph companies away from Morse code based communication into voice communication and gave rise to some of the largest and most powerful corporations of the 20th century [10], [11]. In the USA, the telecommunications and telegraph operators were predominantly under private ownership, while in Europe, most communications organisations were associated and owned by the existing postal services under government control, such as Bundespost (Germany), Postes, Telegraphes et Telephones (France), and the General Post Office (UK). This fundamentally different approach to ownership of the newly emerging and strategically important communications infrastructure between the leading countries of Europe and the USA had a significant impact on the manner and ethos of the development of the core switching equipment in the two geographic areas. In the USA there was (and still is) a strong focus on cost effectiveness, operational efficiency, and long haul communications whereas in Europe there was much more focus on technology, standardisation, and interoperability between competing systems [12], with commercial support and adoption by their home markets.

This situation remained until 1974, when an antitrust suit was brought against AT&T by the US Government [13]. After considerable legal wrangling, the decision was enacted to break up AT&T into a long haul network operator and 7 Regional Bell Operating Companies (RBOCs) on 1 January 1984 [14]. This resulted in the mini-Bells [15] with regional and geographic limits on their business. Some 10 years later the major European nations decided to split the connection between traditional postal services and telecommunications services as the rapid growth of telecommunications was being hampered by the very mature postal

services [16]. This break up also enabled the previously government owned national carriers to bid for international business by placing ownership at arm's length from their respective Governments.

Technology Progress

As deregulation was occurring on the political and commercial front, the developments and improvements in semiconductor technology was producing lower cost, higher quality components enabling the major manufacturers to incorporate more flexibility and features in their products; a requirement for customising equipment destined for overseas markets. Furthermore, the previous generation of equipment designed in the 1950's based on electromechanical switching technology such as the Strowger selector [17] and crossbar cross-connect, Figure 1 [18] was reaching the end of its life and required upgrade and replacement.

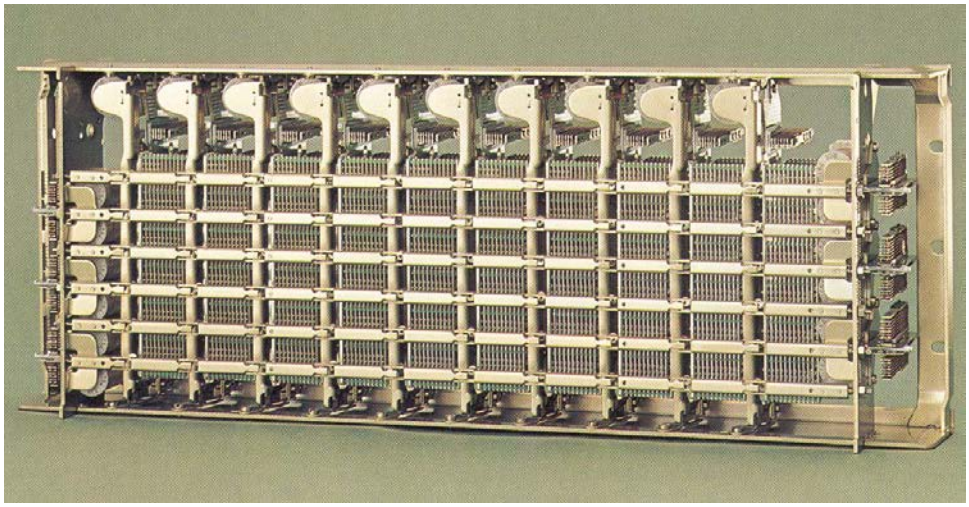


Figure 1: Western Electric 100 point Crossbar Switch; type B
(Source: Walker, P [19] **)**

By the mid 1970's, the advancement of semiconductor technology was sufficient that complex analogue and mixed signal circuits capable of converting the analogue signals to and from the digital domain could be integrated and international standards were agreed [20]. This now enabled the development of switches capable of converting the analogue voice information into digital information and passing it through a digital switch network without any loss of quality or information.

During the 1980's, the demand for telephony services expanded globally requiring switches capable of handling both a greater number of subscriber lines

and interoffice connections (trunks), and also a higher proportion of simultaneous connections. According to the World Bank & ITU figures captured in Figure 2, the global average of fixed wire telephone density was 6 per 100 of population in 1975, with all OECD nations at 24.1 per 100. By 2000 the global average had risen to 15 per 100 worldwide and 55.9 per 100 high income OECD [21], [22]. This growth represented an increase of over 180 Million new lines worldwide (not including replacement or upgrade to digitisation).

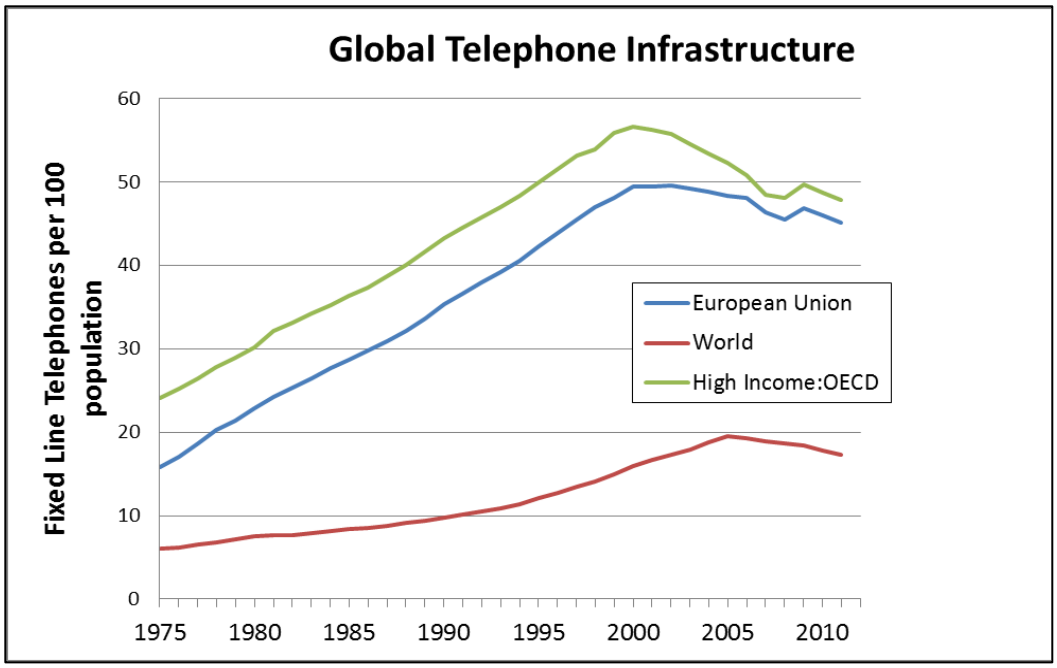


Figure 2: Fixed Wire Telephone Density
Defined as telephone lines that connect a subscriber's terminal equipment to the public switched telephone network and have a port on a telephone exchange. Integrated services digital network (ISDN) channels and fixed wireless subscribers are included. (Source : World Bank /ITU) [2]

This increase in demand required the replacement of the electro-mechanical telephone switches of the 1940 – 1960's, with a subscriber capacity of 15,000 [23], by new digital switches capable of handling up to 250,000 subscriber connections, 60,000 trunk connections, or a mixture of both [24]. The new digital architectures also gave rise to non-blocking switches [17], [25], essential to the delivery of service to all the subscribers' lines.

Worldwide, there were five major suppliers of telecom switch technology (Siemens, Ericsson, Alcatel, AT&T(Lucent), and Northern Telecom) engaged in the development of new switch architectures capable of servicing the emerging ISDN digital networks while still delivering services to conventional analogue

customers via POTS (Plain Old Telephone Service)[1] [26]. Anecdotally, the UK telecommunications network, still owned by the UK government via British Telecom, developed their own 'home grown' switch in conjunction with Plessey and GEC Ltd known as System X. This system failed to gain international acceptance in overseas markets other than some British dependencies such as the Falkland Islands. A summary of the leading global suppliers of telephone switches is shown in Table 1 along with their product first service dates. Further information on the development of the modern telecommunications equipment has been provided by Chapuis and Joel [27].

Manufacturer	Product	Max Subscribers	Trial- Date	Comments
Siemens	EWSD	250,000	1985	German based international conglomerate
Alcatel	System 12	100,000	1980	French/Belgium based international OEM
Ericsson	AXE10	64,000	1976	Swedish based independent OEM
AT&T / Lucent	5ESS	100,000	1982	North America Operator/OEM
Northern Telecom	DMS-100	100,000	1979	Canadian operator / OEM
Plessey / GEC (for BT in UK)	System X		1982	UK joint venture OEM; Acquired by Siemens
NEC Japan	NEAX61	100,000	1979	Japan OEM

Table 1: Summary of Switch Capabilities of major switch vendors worldwide (Source: Author)

By 1985, all of the above listed manufacturers had released their new switches into public service defining both the switch the system architectures and much of the core network capable of delivering both digital and analogue telephony services for the next 2 decades.

General Components of a Telephone switch

Although each manufacturer's switch had different architectural features, often influenced by historic preferences within their home market, a 1980's era telephone switch architecture consisted of 4 main components. The reference diagram used here is based on a Siemens EWSD switch [28], [29]:

1. A Digital Line Unit / Line Trunk Unit (DLU/LTU) responsible for interfacing the subscriber line pair or trunk lines[2] into the switch fabric. In a large switch

[1] Plain Old Telephone Service (POTS) is the most basic telephone service delivered to a 'standard' passive telephone with rotary dial such as a Western Electric Type 500 (USA) or BT (GPO) Type 746 (UK) Telephone.

[2] Trunk lines are 4 wire analogue connections (transmit and receive) between adjacent telephone switches (exchanges) to ensure backward-compatibility with legacy installed systems.

the DLU may provide capacity to terminate up to 250,000 subscriber line pairs occupying up to 80% of the physical equipment area in a central office.

2. A Common Channel signalling Unit for managing the signalling channels from both the line cards in the DLU/LTU and also within the core digital trunk network.

3. A call processing unit for the set-up and tear-down of individual calls. This unit also manages the charging and billing of the calls initiated by subscribers on the switch, or calls transiting the switch according to the billing policies of the operator.

4. A Switching Network unit (SN) responsible for the connection of each subscriber call to the chosen (dialled) far end party. The SN unit varies in architecture depending upon switch manufacturer but generally consisted of a Time-Space-Time cross connect, a non-blocking array capable of connecting any subscriber to any other subscriber or digital trunk connected to the switch [30].

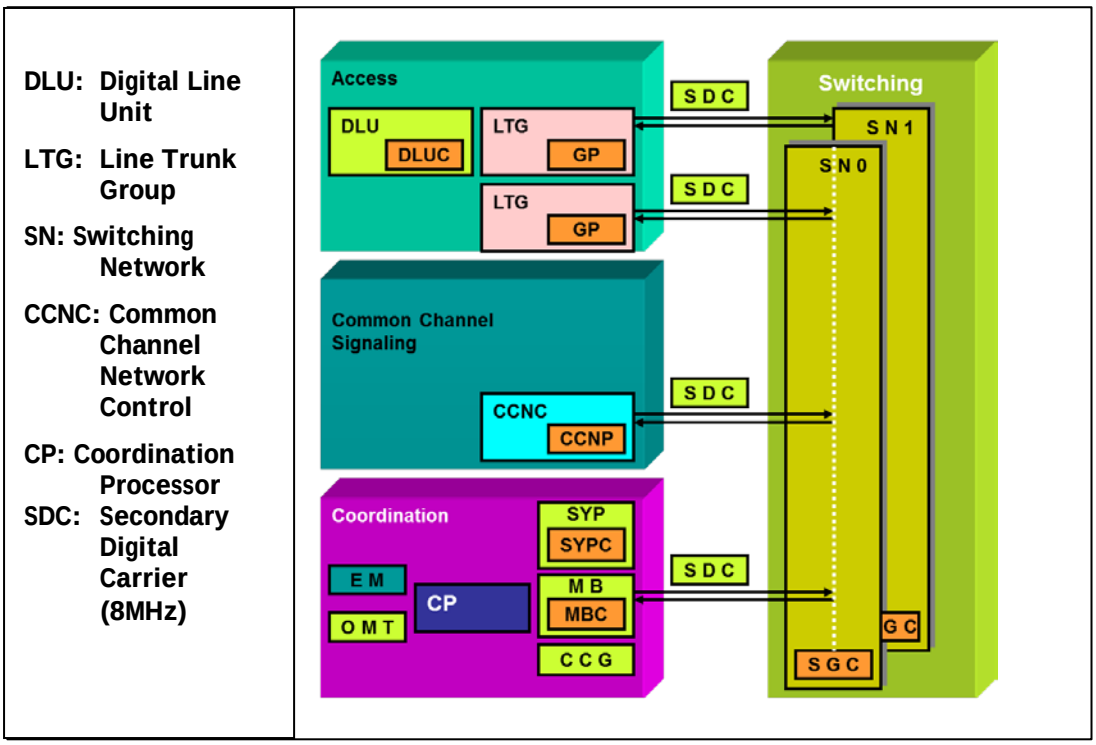


Figure 3: Siemens EWSD top level architecture (Source: Jalali, PTC [24])

Figure 3 shows the top level block diagram of the Siemens EWSD system; other manufacturers may adopt different partitions but the fundamental functions are always the same. This summary of a typical system level

architecture is included by way of background information in order to contexualise the work contained in the submitted material.

Telecommunications Market Development

As the overseas demand for increased telephone services grew, the switching products available to address the demand required localisation. Although international standards agreed and disseminated by the ITU governed the interoperability of telecoms networks at a national and international level [20], primarily through class 5 International exchanges, this standardisation did not apply to the local access network, dominated by the wire plant and connection boxes between the subscriber premises and the central office (exchange) locations [31]. Given that up to 50% of the capital costs for a telecom operator is associated with outdoor wire and cable plant, it was important that any central office switching product was compatible with this legacy of subscriber loops and end terminal equipment (telephone instruments) with the minimum of changes. As each telecom operating authority characterised their line installations differently depending on the mean or median deployment characteristics comprising underground cable, aerial cables, loop length, bridge taps[3], and terminating impedance of the customer terminal, switch manufacturers required an easy method of localisation. In the case of subscriber lines, localisation is determined by a dedicated subscriber circuit known as the Subscriber Line Interface Circuit (SLIC) responsible for connecting the analogue switch line cards, via the Central Office Main Distribution Frame[4], to the external subscriber wire plant; principally the 2-wire subscriber loop running from the Central Office (exchange) location to the subscriber premises [32].

As export sales increased with the development of emerging economies such as China, India, Brazil, and also network upgrading and conversion to digital in the developed world, there was a need by the manufacturers to have software configurable personalisation of a switch via firmware at installation and

[3] A bridge tap is a technique used by telephone operators to deliver service by tapping into a line running by a subscriber premise. The line doesn't connect to another premise, but it may terminate in an open circuit some distance away. Due to this, signals can bounce up and down the line interfering with the send or receive signals to/ from the customer equipment. Old subscriber lines may have up to 10 bridged taps still connected.

[4] The Main Distribution Frame (MDF) terminates all external subscriber and trunk cables into a Central Office (Exchange) Building. Primary voltage protection is installed on the MDF before connection to the electronic switching apparatus within the building.

commissioning. Due to technology limitations, the approach available to manufacturers of the day was the creation of custom line interface circuit boards (linecards) on a per market basis. These dedicated SLIC designs were expensive to develop and costly to hold in inventory for the manufacturer and operator. With the advent of greater level of integration and programmability, and the introduction of high voltage IC processes capable of operation up to 70V and therefore capable of being powered directly from the -48V Central Office (Exchange) common battery [33], switch manufacturers tasked their semiconductor suppliers to incorporate greater programmability into their line card solutions to enable market personalisation and feature enhancement.

The work contained in Theme 1 of this thesis discusses the author's contribution to the evolution of the Subscriber Line Interface Circuit (SLIC) from a simple passive transformer circuit addressing a single market, to a highly programmable system level component capable of addressing all global markets via software /firmware control.

The basic functions of a Subscriber Line Interface Circuit

The first requirement of an electronic solution is to be backwards compatible with existing cable plant and customer equipment. Much of the subscriber loop telephone cabling in the US and Europe can be up to 100 years old and was the largest business asset of the operators. The cost of repairing and maintaining the physical cabling between customer's premises and central office locations dwarfs the costs of both the customer equipment (telephones) and the central office equipment. Any 'upgrading' of a switch installation within a network must be capable of attachment and operation over the installed equipment and infrastructure cabling.

A Subscriber Line Interface Circuit (SLIC) must perform several functions simultaneously over a single pair of wires, of indeterminate length and unknown quality or characteristics. The interface circuit must provide DC power, signalling, and duplex communication over a single pair of balanced subscriber wires. This functionality is conveniently summarised into the so called 'BORSCHT' functions summarised in Table 2 [34].

	Function	Description
B	Battery	The SLIC is responsible for providing and managing power to the telephone instrument over a loop length ranging from 0 ohms (telephone is adjacent the Central Office) to approximately 2000 ohms loop (although exceptional cases can extend to 3000 ohms)
O	Overvoltage	The SLIC must protect the central office equipment and personnel from lightning strikes onto overhead cables, and power cross (mains contact) up to 600Vrms.
R	Ringing	The SLIC must provide a ringing signal (e.g. 20Hz at 95Vrms + 48Volt Battery) to subscriber equipment
S	Supervision	Detect on/off-hook condition, dial pulse replication, ring trip detection and other specialised signalling functions
C	Coding	The coding and decoding of digital speech information into PCM format according to ITU standard G.711 [35]
H	Hybrid	Conversion of 2->4 Wire and 4W-2 Wire to separate the Transmit (Tx) and Receive (Rx) analogue signals on the subscriber loop. It must also define the 2 wire termination impedance.
T	Test	Provide capability to undertake line testing of both the subscriber line and equipment, and loopback testing of the Interface circuit itself.

Table 2: BORSCHT Summary
(Source: Author & [34])

Traditional Line interface circuits were implemented using large iron core transformers but in later generation of switches, these were reduced in size by using modern ceramic transformers materials combined with flux cancellation techniques. A schematic of a typical transformer based SLIC using flux cancellation from a Nortel DMS100 switch is shown in Figure 4 [36].

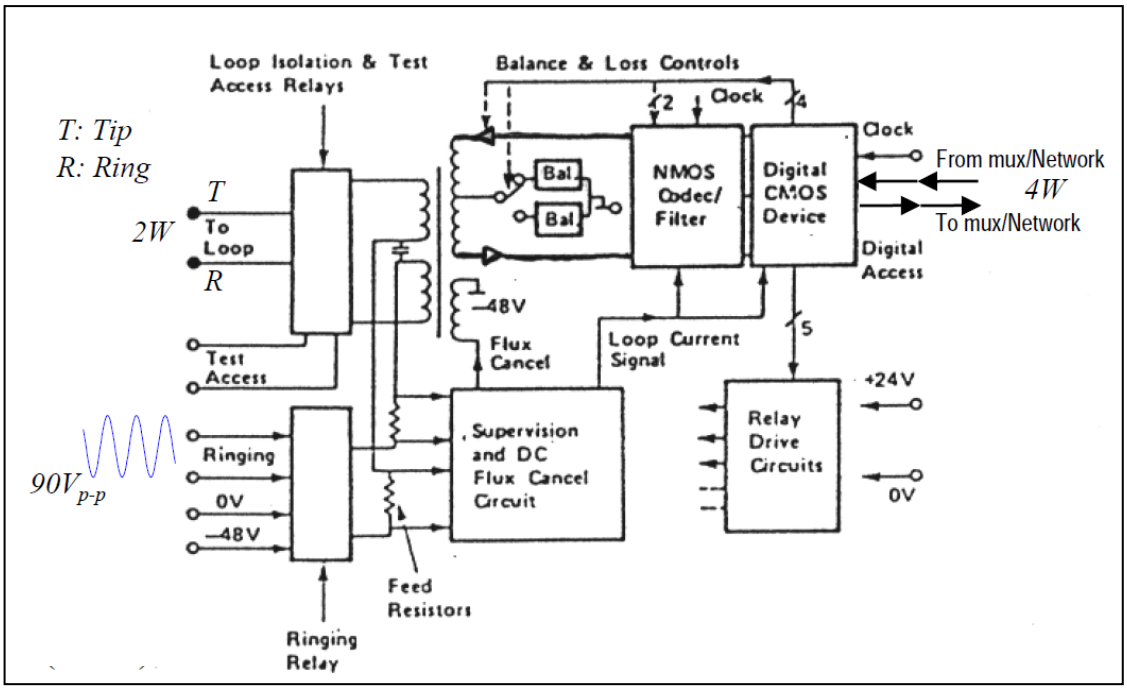


Figure 4: Nortel DMS 100 Line Circuit
(Source: Terry et al. [36])

Although simple in realisation, the flexibility of such solutions was severely limited. Additionally, for a large telephone switch, the PCB real estate occupied by these SLICs was large and the power dissipation within the system was dominated by the SLIC circuits and associated power supplies. However, through decades of optimisation in the development of electro-mechanical switches, the performance of transformer based SLICs was very good and presented a considerable design challenge to the electronic replacements, particularly in their ability to withstand and protect against high voltage and longitudinal balance[5] due to subscriber line faults [37], [38].

A simplified block diagram illustrating the main functional blocks of a generic SLIC circuit is shown in Figure 5 and the challenges and complexities of realising these functions in electronics are described in the submissions presented under theme 1. An example of a discrete SLIC Analog Subscriber Line Card is shown in Figure 6 demonstrating the complexity and density challenges for a modern telephone switch.

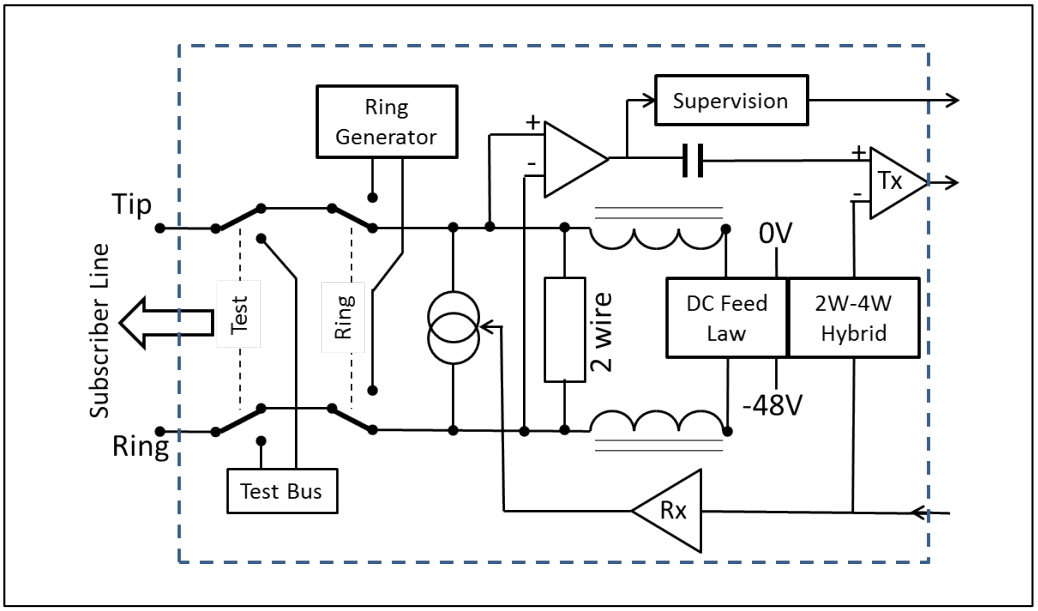


Figure 5: Conceptual functional blocks of a Subscriber Line Circuit (Source: Author)

These electronic SLICs, and the semiconductor devices and switch products which resulted, enabled the rapid rise in telecommunications voice traffic. However, a new demand was being placed on the network; it was now required

[5] Longitudinal balance is a specialised measurement associated with telecom subscriber line equipment and is a measurement of the equipment's ability to terminate a common mode (transverse) signal effectively such that it does not generate a differential (metallic) signal into the audio channel. Full details of the test method can be found in in the IEEE-455 standard [59].

to handle data from Modems proliferating due to the emerging internet connectivity. It was the drive for high speed modems, combined with the development of xDSL technologies which directly competed with, and eventually defeated, the short lived digital access technology promoted via the Integrated Services Digital Network (ISDN)[6].

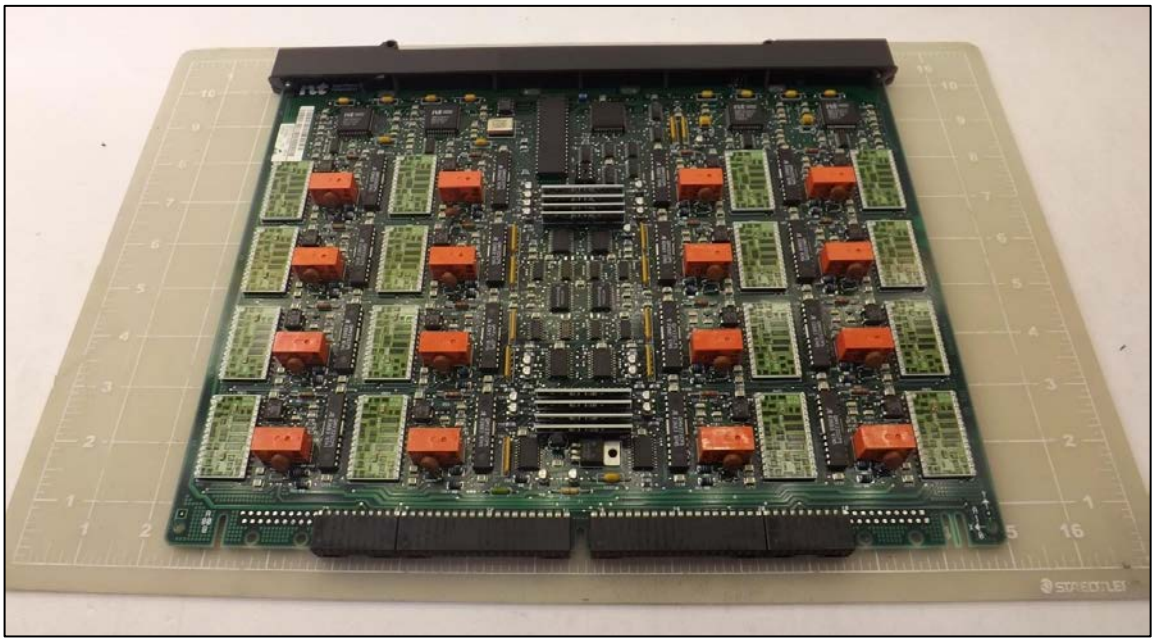


Figure 6: A 16 channel Analog Subscriber Line Card (Source: RUN-DLJ TELECOM [39])

The Internet age and packet based communications.

In the mid 1990's a new method of communications appeared; Ethernet, which initially threatened the Telecom operators and then overtook them. The phenomenal growth of the Internet in mid-to-late 1990s quickly changed the telecom landscape. As the Internet Protocol (IP) became widely adopted, the importance of multi-protocol switching & routing declined in which the telecom giants had invested heavily. The fundamental challenge to the telecom operators occurred on two fronts. Firstly the quality and reliability standards applied to telecom switches were extremely high (99.999% or 'five 9s'), and equipment had a design lifetime of 25 years of continuous operation. Anecdotally, the Failure in Time (FIT) [40] rate of the TP 3210 described in submission II was ~33; that is 33 failures in 1 billion device-hours operation; equivalent to 33 line faults in a 11,500 line switch after 10 years of continuous

[6] Although ISDN customer terminals failed to be adopted by the end users, primarily because the connection speed improvements were marginal over the best analogue modems (64kb/s vs 56kb/s), the digitisation of the core networks and conversion from PDH to SDH delivered many benefits into the core network.

operation assuming no maintenance. However this level of quality and reliability is expensive, and because telecom operators insisted on 99.999% equipment availability both in operating procedures and component design, this placed financial burdens on the equipment suppliers which were not required by datacom equipment suppliers.

The second challenge was based on the fundamental difference between the approaches used for message delivery between data-communications and telecommunications. In telecommunications, the network is based on 'connection based' protocols; requiring a dedicated circuit to be established between the transmitting and receiving parties of a telephone conversation, indeed 2 circuits are required, one in each direction. Irrespective of whether either party is communicating (speaking), the circuit remains established (and billed) until the call is terminated; the resources are reserved for the call's duration. Such a connection also means that the quality of the connection is guaranteed (usually 64kb/s) in both directions. A more full comparison between the different classes of networks is described by Perros [41] and illustrated in Figure 7.

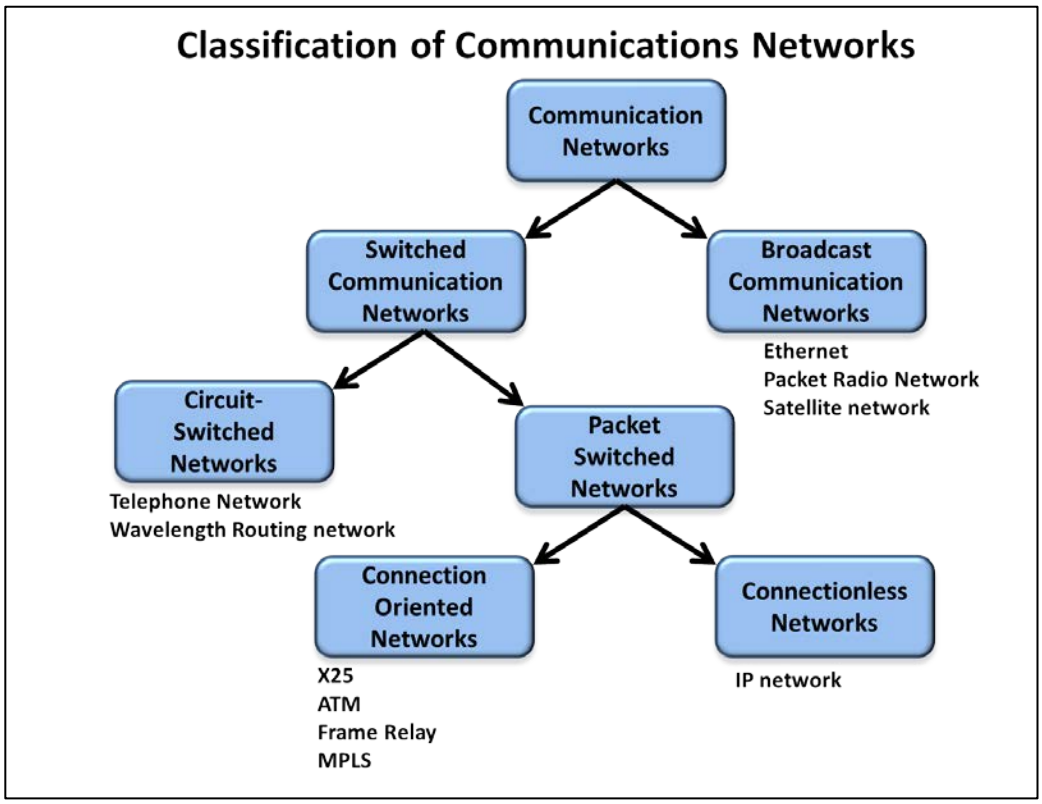


Figure 7: Classification of Communications Networks (Source: Perros) [41]

In datacoms, 'packet based' protocols are used (e.g. IP), where the information from the sender is packetised, labelled with the source and destination address, and sent into the network. If either end has no data to send, no packets are sent. If we restrict the comparison to speech communications, this means that the channel in one direction or the other is 'silent' for over 60% of the time [42]. In the case of connection based protocols this unused capacity is wasted, whereas in a datacom network, it can be used to carry other traffic thus increasing the utilisation of valuable resources. However, in a packet based system, the transfer of data packets from one end to the other is based on a 'best efforts' basis which can impact quality; the most apparent manifestation of this quality variation is experienced using VoIP systems such as Skype™.

The battle between datacoms and telecoms culminated in a technology crash; the dot-com bubble of 1997 – 2000 and subsequent collapse in 2001 [43]. This was driven by investment in new internet companies and away from traditional, capital intensive communications companies. It saw the rise of new technology giants such as Cisco Systems but also the fall of traditional telecom equipment suppliers such as Nortel Networks who tried (and failed) to incorporate IP network products (Bay Networks) into their product portfolio. In 2001, Nortel Networks were forced to lay off over two-thirds of its staff (60,000 people) and write down $16Bn [44].

Optical Access

The dot-com bubble was a wake-up call for the telecom operators and equipment providers who both immediately began to modify their SDH based core networks to transport packet data (IP). At the same time, the rise and rise of the mobile phone was significantly impacting their operator's voice call revenue which was constraining free cash to further upgrade the networks. However, the demand for domestic broadband was growing and although the xDSL [45] solutions were being deployed, investigations into optical network access were being considered. Although Passive Optical Networks (PONs) [46] were deployed on a test basis, the limitations these imposed on network architectures were significant. Point-to-point offered improved technical performance but had increased infrastructure costs. Much of this cost stemmed from the costs of the optical components themselves and the patent submitted

as submission 𝕏 is an approach invented by the author for the Intel Corporation as a lower cost alternative in developing optical access technology. The innovation was developed within a project in conjunction with British Telecom and the BBC to demonstrate 10Gbps point-point access technology using low cost network termination equipment built using new production techniques.

The Wireless age

Although W-LAN or Wi-Fi was established via the Wi-Fi Alliance in 1999 [47], the technology did not achieve mass adoption until ~2005, in part due to the $250M marketing push worldwide by the Intel Corporation of its Centrino branded chipset for wireless enabled laptops. However, the popularity of Wi-Fi rapidly revealed its short comings due to the limited bandwidth available. A new wireless standard based on Ultra-WideBand (UWB) communications was emerging as a complementary solution to Wi-Fi for in-room, very high data rate applications such as streaming video. The physical layer of this system operated at very low power (-41dBm/MHz) across a very wide band (3.1 – 10.6GHz) and was capable of providing up to 480Mbps end to end data bandwidth. In addition to the higher bandwidth, the industry led WiMedia Alliance created a new Media Access Controller (MAC) which was a considerable improvement on the original WiFi MAC, enabling channel reservation over the air interface. This effectively enabled connection based links to be established over a packet based system providing guaranteed Quality of Service (QoS) for time critical applications while also offering 'best efforts' service over the remainder of the channel.

Unfortunately, the technical aspects of UWB proved too great a hurdle to realise the full benefits while delivering significant bandwidth over sufficient range and was overtaken by the WiFi community who had developed improved speeds via 802.11n [48]. Due to market failure, the WiMedia Alliance activities ceased in 2004 although the bandwidth reservation feature has been adopted by a new, emerging 60GHz standard [49].

The following submissions present some of the innovations developed by the author and colleagues in the field of communications from early subscriber line access devices through to the development and application of the latest wireless technologies. Although technological advances such as power efficient DSP

processors have enabled these features to be realised using new methods, at the time of invention, many of these features were considered world leading and demonstrated the very best capabilities of analogue circuit and system design.

The Published Work

The published work presented here represents over 28 years of activity in the definition, creation, and productisation of communication products related to network access whether that be wired, wireless, or optical connections. Due to the period over which these developments took place, the majority of the original development material is unavailable to the author as it is confidential and owned by various companies. However, via the publication process of inventions disclosed and examined by patent offices, much of the major invention and innovation has been captured via granted and published patents.

The first Theme is associated with '**Analogue Subscriber Line Interface Circuit(SLIC) Access Technology'** and covers a period of approximately 15 years in National Semiconductor's Telecom Products division. The group's focus until 1998 was the high volume application associated with subscriber line access and the author led much of the development over this time. The specific area of expertise was in analogue circuit and system design, primarily using bipolar technology capable of withstanding the high voltages required for that application, and also in developing the complex analogue systems for use in the same application.

The second theme '**Optical Access Technology',** covers a career developing products for data communications, predominantly Ethernet technology running over standard copper twisted cable (e.g. CAT 5)[7]. These activities started in 1998 with Level One Communications based in Sacramento, California, USA focusing on physical Layer 1 of the ISO stack [50] Ethernet transceivers for 10/100Mbit/s, eventually extending to 1Gbit/s. The company was acquired in 1999 by the Intel Corporation just prior to the bursting of the dot-com investment bubble. In the higher rate Ethernet physical layer specifications

[7] 'CAT 5' or Category 5 cable is the standard configuration of 4 pairs of unshielded twisted pair cable used for structured wiring for data connections in office or factory buildings. The specifications were originally defined in in the standard TIA/EIA-568-A [78].

(under IEEE 802.3ae) there is provision for fibre links running up to 10Gbits/s. The work (and patent) listed under this piece of work built on several years of detailed work in data communications, an in-depth understanding of service delivery and topology of the existing subscriber loop plant serving consumers (via previous SLIC experience), and the technical trade-offs between Passive Optical Networks (PONs) and point-to-point configurations. The patent develops an idea for a network optical access unit in the subscriber's premises capable of delivering 10Gbits/s but realised in a very cost effective manner, addressing some of the key cost roadblocks associated with the mass production of optical technologies at the time.

The third theme '**Wireless network access technologies'** discusses a development project for an RF Front end device and antenna for a new wireless technology, Ultra WideBand (UWB) wireless, using a 7.5GHz section of spectrum extending from 3.1GHz to 10.6GHz to deliver short range (<7m), high bandwidth, next generation wireless connectivity for businesses and consumers [51]. The commercial drive for this technology was as a replacement to the existing Wi-Fi technology by populating homes or work places with high density wireless access points to deliver up to 480Mbps of data coupled with a guaranteed quality of service. The particular invention describes a modification of the UWB standard to deliver 2.7Gbps along with the design of a compatible antenna.

Theme 1: Analogue Subscriber Line Interface Circuit Access Technology'

The submissions presented under theme 1 are all associated with the realisation of advanced analogue line interface circuits for connecting to the external subscriber lines between the central office (exchange) and the subscriber's premises. The challenge posed to the designer was to deliver a solution which offered the equipment supplier increased flexibility and functionality while delivering transmission performance which exceeded the existing, transformer based solutions. Additionally, the power consumption and cost of the new solution should also compare favourably with the transformer (particularly difficult when competing with a passive component).

Submission I **Patent No. US 5,598,467:**

Title: Signal Interface Circuit with Selectable Signal Interface Parameters.

Inventors: **Duncan J Bremner**, Lochwinnoch, Scotland
Roger K Benton, Edinburgh, Scotland
James B Wieser; Pleasanton, Calif. USA

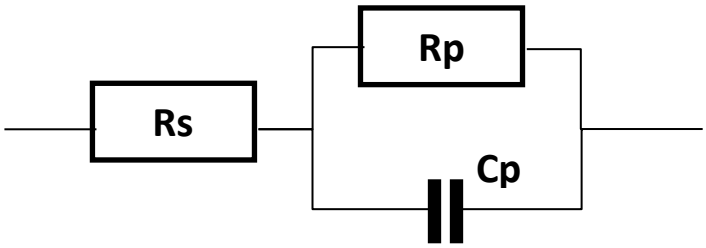
Assignee: National Semiconductor Corporation, Calif. USA.

Filed: Dec 9, 1994

This particular invention was critical in developing an electronic SLIC capable of synthesising complex (R+ R||C) 2-wire[8] termination impedances for the subscriber loop. Although originally, telecom networks were based on a 600Ω line impedance [52], in many countries this has been replaced by a complex impedance of the form (R1 + R2||C) to better match the characteristic line impedance. A typical example of this was the UK 2-wire impedance of 370Ω + 620 Ω ||310nF; other examples of complex 2-wire terminations can be found in Q.552 [53] a copy of which is shown in Table 3 below.

[8] In telecommunication networks, the 2-wire interface is the twisted pair (carrying duplex information) between the subscriber and the Central Office (Exchange) where it is converted (separated) into transmit and receive information for transmission through the core network. This avoids multiple impedance mismatches which would cause reflections and voice channel degradation

National Network	Rs (Ohms)	Rp (Ohms)	Cp (Farads)
Austria, FRG	220	820	115n
BT	300	1000	220n
NTT	600	infinity	1μ
USA	900	infinity	2.16 μ
ETSI	270	750	150n



The test network and the component values represent a configuration that exhibits the required exchange impedance. It need not necessarily correspond to any actual network provided in the exchange interface.

Table 3: 2-Wire termination Impedances
(Source: ITU Q.552) [53]

In order to appreciate the challenge of realising such complex terminating impedances accurately, first a simple circuit analysis must be performed according to the conceptual schematic shown in Figure 8.

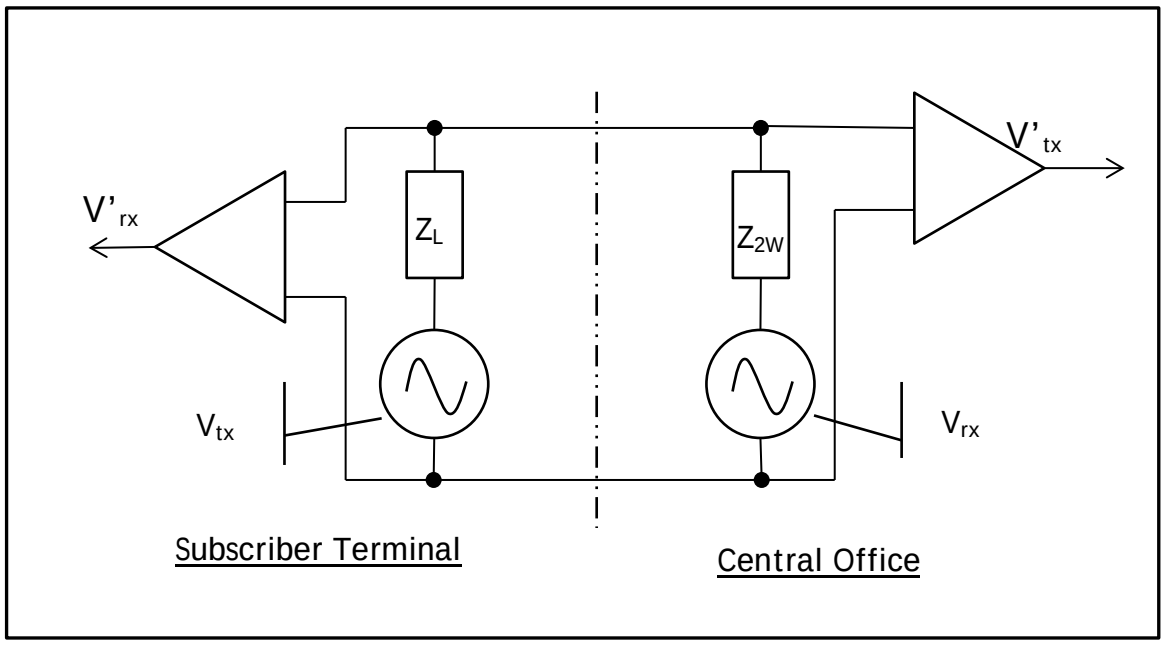


Figure 8: Simplified Conceptual Schematic
Source: Author

The diagram shows the AC Thevinin equivalent circuit of the transmission paths between 2-wire subscriber terminal interface (normally a telephone) and the 2-wire subscriber loop interface of a Central Office (exchange). Although the requirement of the impedance is to define return loss, it can be shown that this terminating impedance dominates the transmission characteristics.

Return Loss: $$RL = 20\ log\left|\left(\frac{Z_{2W}-Z_L}{Z_{2W}+Z_L}\right)\right| \quad (1)$$

Receive Gain: $$\frac{\acute{v}_{rx}}{v_{rx}} = \left(\frac{Z_L}{Z_{2W}+Z_L}\right) \quad (2)$$

Transmit Gain: $$\frac{\acute{v}_{tx}}{v_{tx}} = \left(\frac{Z_{2W}}{Z_{2W}+Z_L}\right) \quad (3)$$

Note: *Only V_{rx} or V_{tx} signals are present at any one time; hybrid cancellation in both the subscriber equipment and the CO equipment remove the un-wanted signal (not shown in simplified diagram). The impact of these through the system feedback mechanisms mean the above parameters are not impacted.*

By inspection, it can be seen that the respective values of the 2-wire termination impedance of the SLIC (Z2W) in conjunction with the test impedance (ZL) will directly influence the frequency response. The accuracy of this termination impedance is critical as the loss vs frequency (inverse of frequency response) performance of the SLIC is very tightly controlled via specification. The specifications vary according to administration but a typical requirement and that defined by the ITU [53] demands frequency response accuracy within the speech pass band of 300-3400Hz of +0.3dB, -0.35dB as illustrated in Figure 9. The red line shows a typical response curve of products meeting this requirement. In order to meet the gain specification across all operating conditions, a Return Loss >56dB (~+/-2.9% matching) is required.

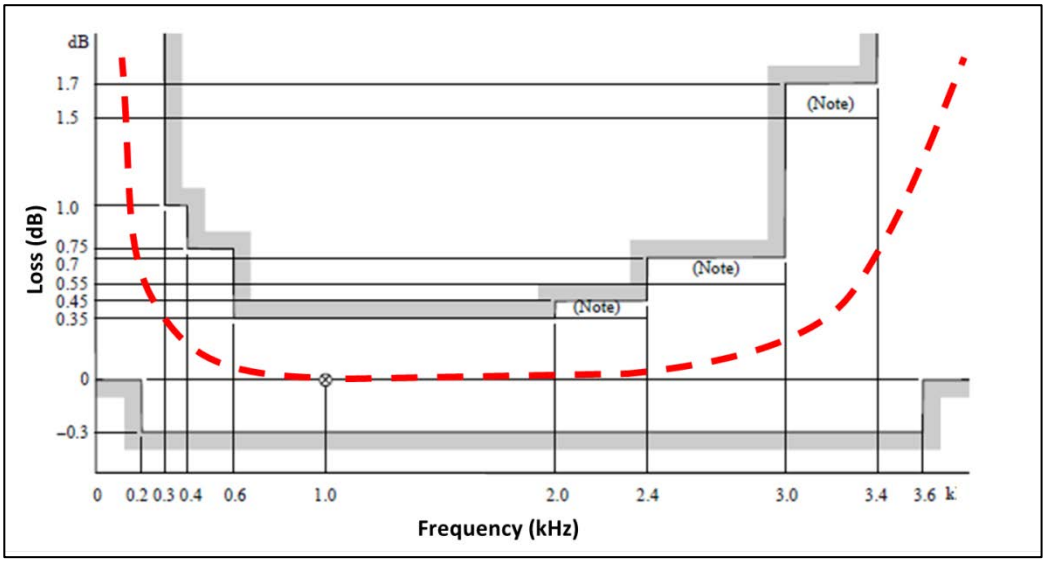


Figure 9: Subscriber interface Loss vs. Frequency (Source: ITU Q552) [53]

If the synthesis of the termination impedance is now translated into an electronic SLIC, realisation of simple resistive termination impedances (say 900Ω) is relatively straightforward as it relies on an external resistive component and on-chip matching. This can be implemented if the SLIC system level schematic is realised by driving current into the load and sensing the voltage appearing across that load [54] and using that information to control the current drive via feedback. (The corollary of driving voltage and sensing current also works [55]). By driving current/sensing voltage or vice versa this exploits silicon's capability for precision on-chip matching, but poor absolute realisation. The technology was certainly not capable of delivering the accuracy of +/- 0.25dB (approximately +/- 2.5%) required by the application. A full discussion is contained in the submission, however a simplified, single ended analysis of the AC termination circuit as realised on the actual electronic SLIC is shown in Figure 10.

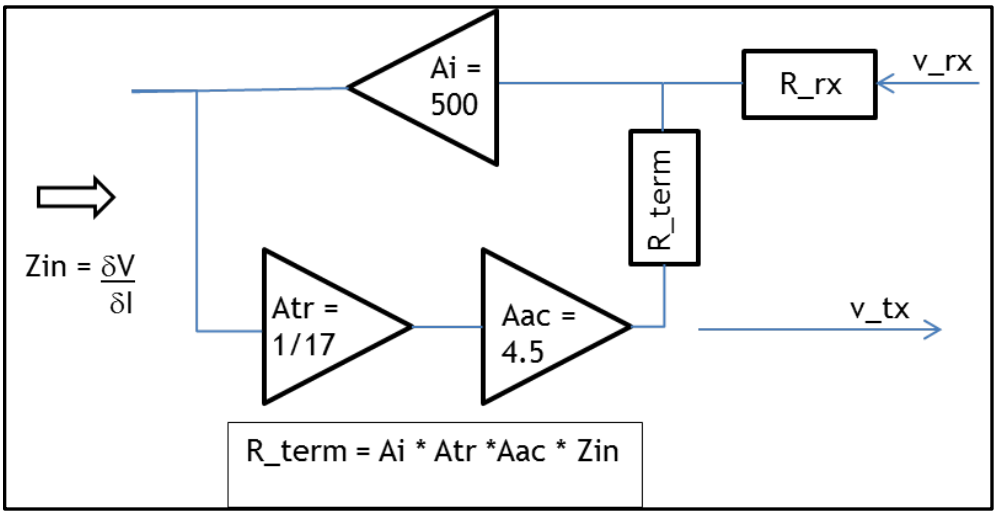


Figure 10: Simplified, single ended Impedance synthesis (Source: Author)

Defining highly accurate current amplifiers (Ai) and voltage amplifiers (Atr, Aac) using integrated, matched resistors is well understood but, in order to accurately define a resistive 2-wire termination impedance, an off-chip component '*R_term'* must be used between the output signal of the 'Aac' voltage amplifier and the virtual earth input port of the 'Ai' current amplifier. In the case of a simple resistive termination this is possible using a single high accuracy component. If a typical example of a 2-wire impedance of 900Ω is required, based on the block gains in the diagram, this corresponds to a value of *R_term* = 118.8 kΩ.

$$\frac{\delta i_L}{\delta v_l} = \frac{1}{Z_{in}} = \left(\frac{A_i * A_{tr} * A_{ac}}{R_{term}}\right) \quad (4)$$

Where: I_L, V_L are the small signal (ac) changes in line current and voltage, A_i, A_{tr}, A_{ac} are the block gains in the system.

This architecture approach is adequate and is used by several solutions to synthesise a resistive 2-wire impedance. However if the operation of the circuit is examined in response to a receive signal current (right to left) being injected into the same virtual earth input connection of Ai, it can be seen by inspection that *R_rx* will directly impact the level appearing on the 2-wire (left) side and for a fixed v_rx input level, the magnitude of *R_rx* impedance will define the receive gain of the circuit. In a simple resistively terminated circuit any mismatch of the *R_rx* and *R_term* will result in a simple gain error.

However if the desired termination impedance must be complex, such as those defined in ITU-T Q552 or [56], the approach defined in Figure 10 gives rise to difficult component matching issues. In order to maintain the transmission accuracies defined in the specification, both *R_rx* and *R_term* must be with precisely matched networks of the same form and order as the required termination impedance requiring 2 precisely selected (i.e. expensive) impedance networks both in absolute terms and matching.

However, by modifying the overall system architecture to place the terminating impedance in the forward path (i.e. such that the receive signal, v_rx and the line derived feedback signal, v_tx both pass through the same network), this single complex network defines both the 2-wire impedance and receiver transfer functions. This innovation uses a single network to define both parameters eliminating cost and variability in the application. A simplified diagram of the modified system schematic as incorporated in submission I is shown in Figure 11.

The key to this invention and the important innovation was a modification of the forward transfer function of the system such that the voltage to current conversion formerly undertaken via *R-term* and *R_rx* into the virtual earth input has been combined into a single circuit block with a single equivalent circuit to R-term which has the same effect on both the feedback signal from Atr, Aac,

and the forward signal Vrx. Furthermore, these inputs can now be changed into voltage inputs as the voltage to current conversion has now been incorporated into a single, albeit more complicated, voltage to current (Gm) converter. The result of this is the elimination of any relative frequency distortion between the v_rx and v_tx signals and the 2-wire impedance as all 2 parameters on are defined by the same complex network.

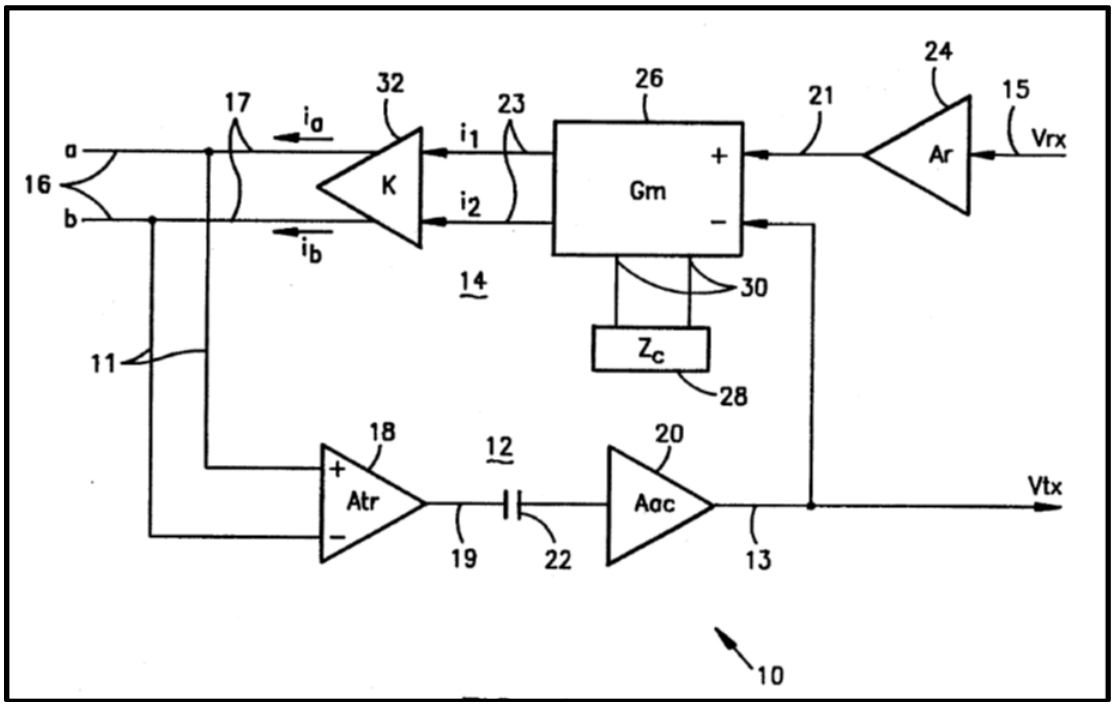


Figure 11: System Diagram of Complex Impedance synthesis (Source: Patent US 5,598,467)

This system level invention was vital in capturing emerging markets such as China who had adopted complex termination networks. The first product using this invention, the TP 3219 SLIM™ is shown in the Figure 12. Although the TP3219™ datasheet (in Chinese) is no longer available, the closely related product TP3210 SLIM™ is presented as submission II. The test specifications contained in submission 2 illustrate the complexity and accuracy demanded of such components.

The author's contribution to this work was in defining the application requirements of the system, researching and defining the accuracy of the complex termination network, and performing the system analysis on the design of the high voltage, line sense circuit blocks of the systems (23, 28, 32, 17, 11, 18, 19, 22, 20 and 13 in Figure 11). These blocks required an accuracy exceeding +/- 0.5% in a very challenging environment over an extended lifetime. While the

patent discusses some of the specific circuit design techniques employed on the device, the underlying system modification is the most valuable and novel.

Since grant in 1997, this patent has been referenced by 9 subsequent patents, all associated with line impedance matching applications by organisations such as IBM, LM Ericsson, Nokia, and Agilent Technologies. The most recent citations: US 8,611,385 (2013) by LSI Corporation, and US 7,957,522 (2011) by Winbond Electronics Corporation attest to its continued relevance.

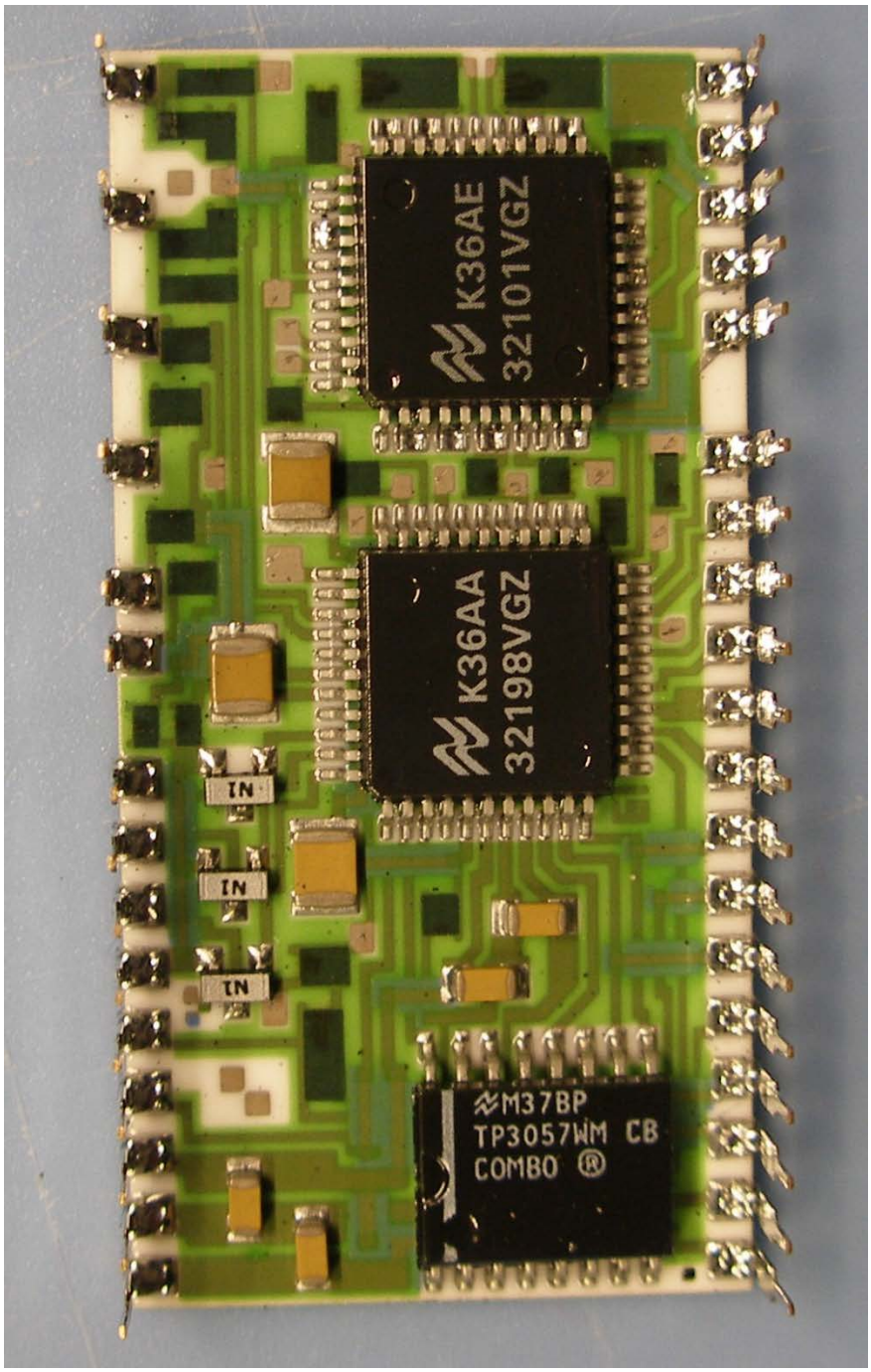


Figure 12: TP3219 SLIM™ Subscriber Module (Source: Author)

Submission II Book Extract: Datasheet: TP3210; pp 143 - 162

Title: TP3210 SLIM™ Subscriber Line Interface Module; Preliminary Datasheet; pp 143-162; National Semiconductor Telecommunications Products Databook; 1995

Authors: **Duncan J Bremner**, Lochwinnoch, Scotland;
Roger K Benton, Edinburgh, Scotland
James B Wieser; Pleasanton, Calif. USA

Submission II is the preliminary datasheet for the TP3210 SLIM™ device included in the 1995 telecom products databook from National Semiconductor. Functionally, the operation of the device and the specifications were identical to the production product; company policy required parts remained 'PRELIMINARY' until formal production release was complete.

The release of the TP3210 SLIM™ into the market place was the first fully integrated, single component solution available capable of meeting the very rigorous Bellcore specifications [3] for the US market, in particular the very challenging longitudinal balance requirements. This requirement arises due to the preponderance of long lines in the USA where, in rural regions [57], aerial telephone subscriber lines run for many miles on the same poles as power utility services to save cost. This resulted in the subscriber line being exposed to 60Hz mains interference levels as high as 20mArms appearing as a common mode signal on the subscriber lines due to induction. In practice this level of interference is manageable due to the balanced nature of the subscriber lines resulting in both the 'Tip(A)' and 'Ring(B)'[9] wires being exposed to the same common mode interference, but due to identical interference conditions, very little differential component resulted.

In the case of the original transformer based SLICs, shown previously in Figure 4, the method of construction resulted in highly effective flux cancellation of common mode induced interference signals while simultaneously presenting a low impedance to battery ground for these signals. Subject to the quality of

[9] Tip, Ring, Sleeve (TRS) connectors were the standard connector used in the telecommunications industry. 'Tip' was the end of the jack plug and usually the most positive terminal, 'Ring' was the second connection of the jack plug and usually the most negative potential, and sleeve was the ground connection. See [79] for further details.

manufacture, transformer SLICs could deliver 60dB longitudinal balance while simultaneously presenting as defined terminating impedance to longitudinal signals [58]. However in the case of electronic SLICs, and the necessity for real resistors to define the transmission performance, the challenge to deliver adequate longitudinal balance performance while protecting the device against damaging fault currents became acute.

On reaching the SLIC at the Central Office (Exchange), it was imperative that the line terminating interface circuit presented 'identical' impedances to earth to both the Tip(A) and Ring(B) legs. This requires that the circuit blocks connected to each leg are matched to a very high degree. In the USA, the specifications for 'Longitudinal Balance' (defined by the telecom standards body Bellcore via specification TR-TSY-000057 and now superseded by GR-507 [56]) required longitudinal rejection greater than 60dB. This corresponds to each leg of the interface circuit presenting an identical impedance to ground (better than +/- 0.1%) in order to meet the standard. The test circuit of Figure 13 shows the test setup requiring for any longitudinal signal 'Vs' up to a longitudinal current of 20mA rms per leg (Tip and Ring), balance must be maintained.

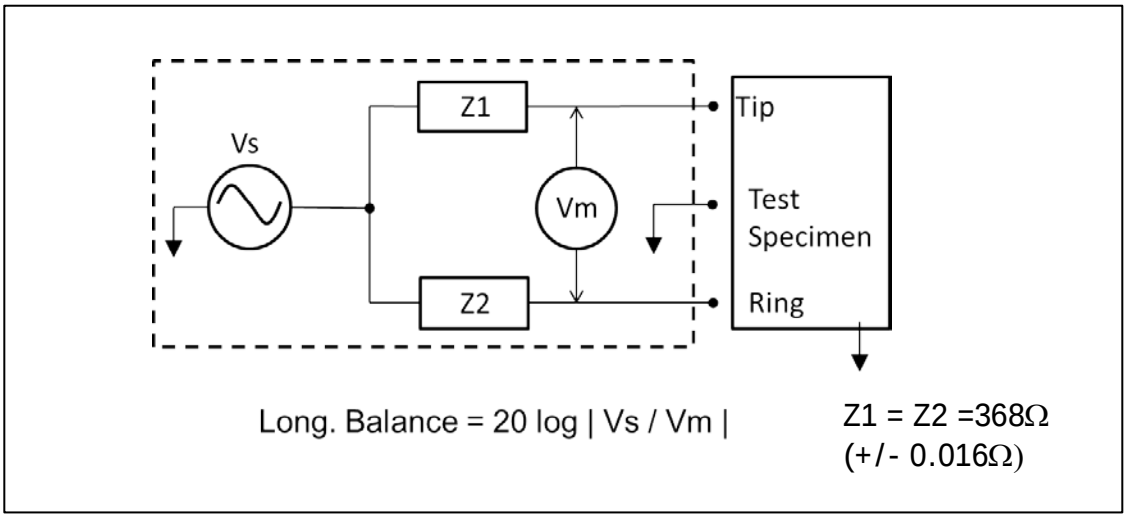


Figure 13: Longitudinal Balance test circuit as per IEEE method (Source: IEEE 455) [59]

In order to meet the required matching needed to deliver a longitudinal balance performance exceeding 60dB as required by the US, two fundamental approaches can be adopted. The first is to synthesise or otherwise realise a low common mode impedance to ground from both Tip and Ring terminals. As the test circuit in Figure 13 illustrates, this would meet the requirement. By way of

example, let the common mode impedance on both tip and ring to ground be R_t, R_r.

Then $$v_{tip} = v_s * \left(\frac{R_t}{Z_1+R_t}\right) \quad and \quad v_{ring} = v_s * \left(\frac{R_r}{Z_2+R_r}\right) \tag{5}$$

and since $v_m = v_{tip} - v_{ring}$ then $$v_m = v_s * \left[\left(\frac{R_t}{Z_1+R_t}\right) - \left(\frac{R_r}{Z_2+R_r}\right)\right] \tag{6}$$

and $Z_1 == Z_2$, and assuming $Z_1, Z_2 >> R_t, R_r$ then

Longitudinal Balance, $$L = 20\ log\left(\frac{v_s}{v_m}\right) \cong 20 \log\left|\left(\frac{Z_1+\left(\frac{R_t+R_r}{2}\right)}{(R_t-R_r)}\right)\right| \tag{7}$$

Selecting a range of R_t, R_r mean values for a given mismatch (Rt:Rr), the effective longitudinal balance 'L' can be calculated as shown in Table 4.

Mean R_t, R_r (Ω)	Matching R_t : R_r	L (dB)
10	10 %	51.5
10	1.0 %	71.3
20	10 %	45.8
20	1.0 %	65.6
100	10 %	33.4
100	1.0 %	51.5
100	0.50 %	59.4
150	1.0 %	50.7
150	0.25%	62.8

Table 4 : Longitudinal Balance vs. common mode impedance

According to the longitudinal balance specification [56], 'L' must exceed 60dB, however this would limit the Tip->Ground, Ring-> Ground impedance to less than 20Ω with a ~1% matching requirement. However, the current injection during fault conditions could then damage the SLIC device or the linecard.

Referring to Figure 14, the system level realisation of the innovative solution can be explained. During the presence of longitudinal interference signals appearing equally (due to the balanced nature of the interference) on Tip and Ring terminals, the SLIC circuit must present an equal impedance on each line to ground. As the circuit is completely symmetrical {Ai(Tip) == Ai(Ring)}, and as there is no differential signal, the 1/Gm differential block only provides a DC voltage reference, the impedance via the control loop can be calculated thus:

$$\frac{\partial v}{\partial i} = \frac{1}{A_i * A_{cm}} = 150\Omega \qquad (8)$$

If Ai = 5mA/V, and Acm = 1.33, and the effect of the 250kΩ sensing resistors is ignored, the synthesised common mode impedance is 150Ω per leg (Tip and Ring). In this case, if the sum of the external protection resistors (100Ω), plus the internal series resistance (50Ω per leg in TP3210 family), this means the line drive amplifiers 'Ai' do not require additional voltage headroom for the output stages. That is to say, in the presence of a 20mA rms longitudinal interference signal per leg (Tip, Ring), to a first order approximation, the amplifier output stages can be biased to operate much closer to the supply voltage thus reducing power dissipation.

Within the TP3210 family, this new and novel approach was taken to enable the use of high value (100Ω), loose tolerance (20%) series protection resistors while maintaining excellent balance longitudinal performance. This common mode control loop ensured the protection components did not impact any of the critical transmission characteristics. A more detailed explanation of how this performance was achieved is contained in submission IX.

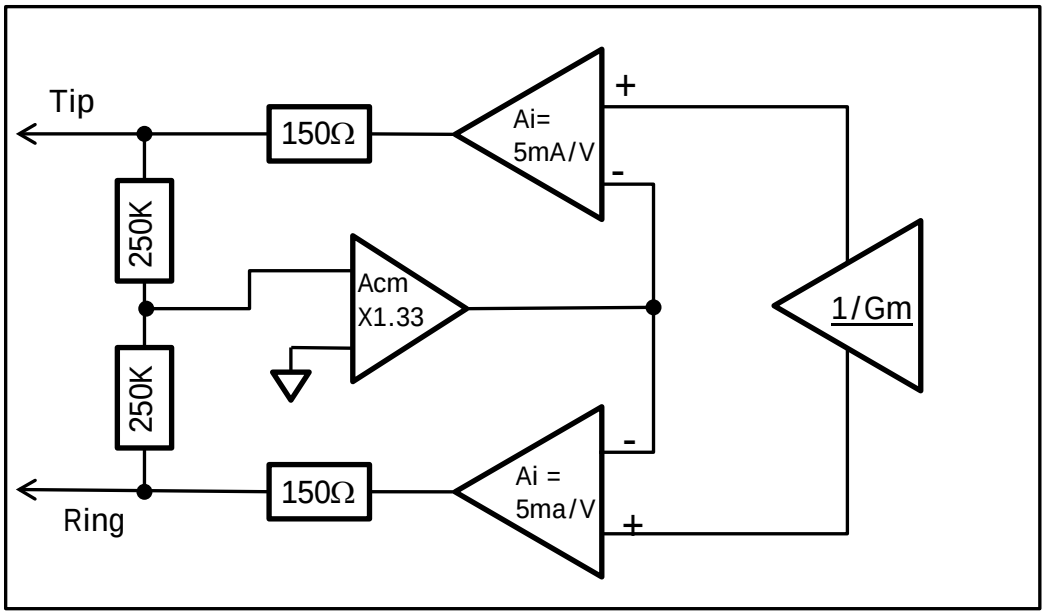


Figure 14 Common Mode Control Loop
Source: Author

The detailed datasheet submitted as submission II will gives a good insight into the complexity and performance accuracy required of an electronic SLIC

product. A further application brief [60] gives a short overview of the benefits and features of the SLIM programme to switch manufacturers.

The author's responsibility and contribution focused on the high voltage, line interface aspects including the realisation of the High Voltage electronic circuit blocks which connected to the subscriber line. The challenges and novelty in this work was creating and developing a product to meet the challenging Telcordia [56] specifications. The TP3210 was the first electronic SLIC to meet the extremely challenging longitudinal balance specifications while using high value (100Ω) protection resistors. This innovative approach supported the adoption and modification of the device for several overseas markets.

Submission III Patent No. US 5,973,516:

Title: Transient signal Detector with Temporal Hysteresis

Inventors: **Duncan J Bremner**, Lochwinnoch, Scotland;
Ray Allen Reed, San Jose, Calif. USA

Assignee: National Semiconductor Corporation, Calif. USA.

Filed: Aug 28, 1998

Submission III is a patent granted for the invention of a system level solution to address the problem of improving a SLIC products response to signalling information while still meeting transmission requirements. This development was part of the next generation solution to the TP3210 SLIM™ and incorporated significantly more user flexibility (hence design complexity) to meet the demands of the global market.

Table 2 summarises the functional requirements of a SLIC, one of which is supervision. In a conventional POTS telephone system operating over a normal subscriber loop, there are a limited number of methods for signalling information over the loop between the Central Office (Exchange) and the subscriber. The most common signalling method (prior to DTMF dialling) [61] is loop disconnect [62] used for generating dial pulses, subscriber going off-hook (initiating or answering a call), or subscriber on-hook (normal 'standby' mode or call termination). In addition to the on/off hook states, interruption of the loop current was, and still is used by rotary dial telephones to signal to the Central

Office (Exchange), the dial pulses corresponding to the digits of a far end (called) party. A traditional rotary dial makes/breaks the line current in synchronisation with the dial rotation and at a rate normally around 10pps. Each Service provider has their own Dialling specifications; an example of such a signalling specification can be found in [63]. At the Central Office (Exchange), the SLIC is required to monitor these pulses and replicate these accurately in the time domain[10] and logic level suitable for the internal logic circuits of the switch to interpret and decipher the information in order to connect to the called party.

The challenge presented to the SLIC is the AC transmission characteristics and the DC power feeding characteristics loops interact during dialling. This requires careful compromise between the AC transmission loop, the DC battery feeding control, and the dial pulse signalling requirements. To ensure the AC transmission performance is not compromised, the DC feeding requirements normally have a very long time constant; in the case of electronic SLICs, usually less than 5Hz which is defined by a time constant. However as the repetition rate of dial pulses is 10Hz, the normal DC loop filter is much too slow and must be 'speeded up' by modifying the time constants in order to replicate the duty cycle of the signalling information. The conventional method of improving this performance (and used in the TP3210 SLIM™) is based around relatively simple level detection of the line current (i.e. that current flowing in the subscriber line through the subscriber equipment). By setting a comparator to be triggered if the DC loop current exceeds a threshold; this can be used to trigger a speed-up circuit to reduce the DC loop time constant thus forcing the loop to replicate the dial pulses more accurately.

However, due to the loop interaction and also the presence of low frequency ringing due to highly inductive ringers (resonance ~20Hz), it is common to see the line current showing ringing behaviour which passes through the thresholds set to detect on/off hook or dial pulses. This ringing in disconnects the 'speed up' time constant resulting in smearing of the dial pulse mark-space ratio

[10] The absolute arrival time of the first digit 'break' is unimportant, the repetition rate and the duty cycle define the specification.

preventing the Central Office (Exchange) logic circuits from correctly decoding the dialled digits.

The important innovation in this system level invention described in submission III is the incorporation of a timing circuit capable of holding 'on' the speed up circuitry sufficiently long to enable the DC loop to stabilise using the 'fast' loop setting, but sufficiently slow that the AC transmission loop and the DC feeding loop does not cause instability (there were conditions when the SLIC had to pass special signalling information while transitioning from off to on-hook).

Whereas the existing approach to triggering the speed up circuit was based on the detection of a DC change in line current, the approach taken in this invention detected the dV/dt of the instantaneous voltage on the subscriber line, and when this transient signal exceeded a predetermined level (either positive or negative), the speed up circuit was engaged.

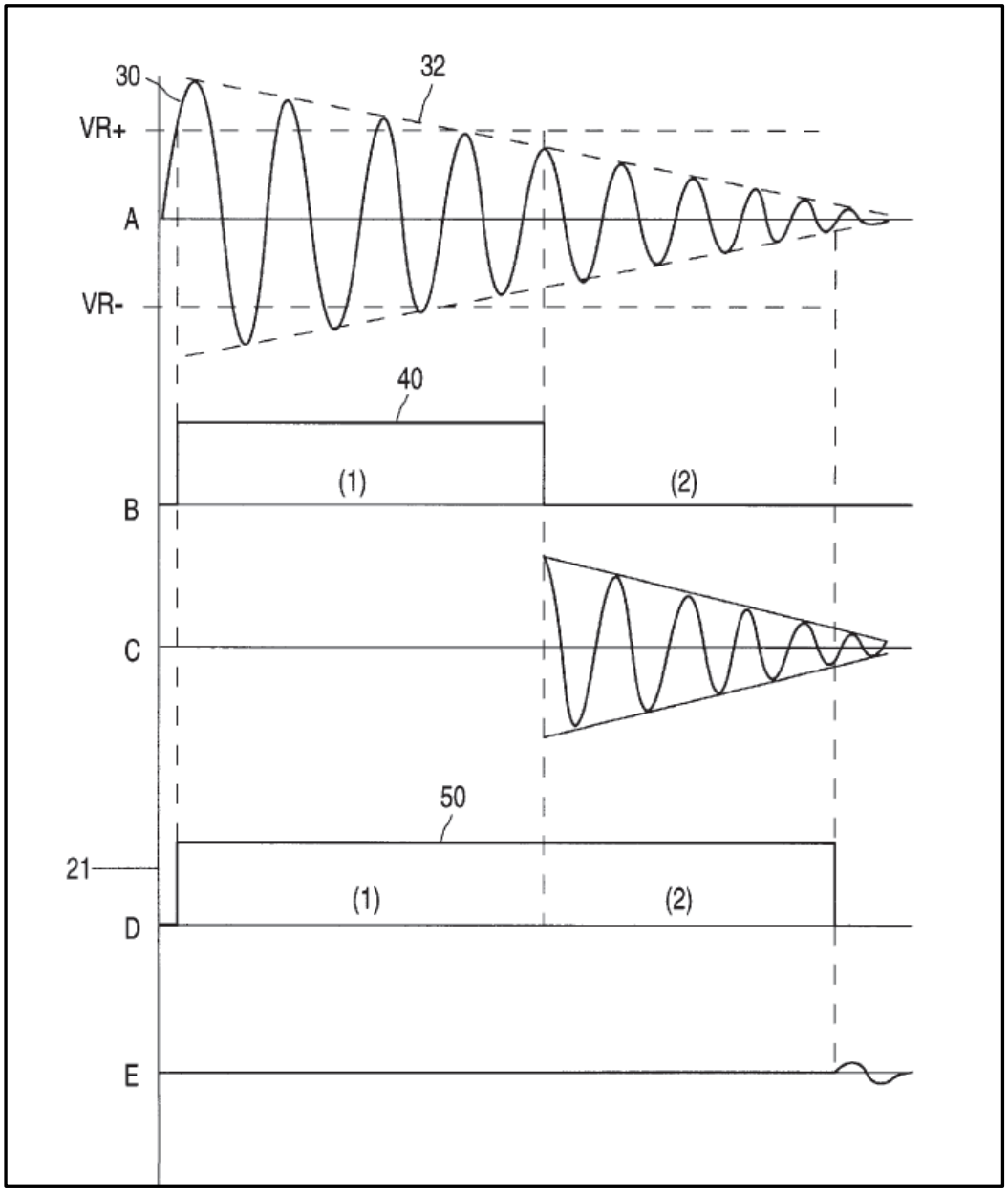


Figure 15 Conventional versus new transient signal detector
Source: **US 5,973,516 Patent: Figure 2**

Referring to Figure 15 (extracted from submission III) describes the function more fully. During the loop disconnect signalling, ringing transients appear on the subscriber line due to the interaction of the DC current feeding law, the AC termination impedance, and the resonant nature of the subscriber instrument (telephone). These transients can last up to 200ms if undamped. The top trace (A) shows the effect if the transients are permitted to exist unchecked. If a conventional level based detection system is used to engage the speed-up circuit, the period shown in trace (B) describes the drive signal to the speed-up circuit. As it is level based, when the signal level reduces below the threshold, the circuit dis-engages resulting in a residue of ringing shown in trace (C). However, if the rate of change of the transient triggers a timing circuit, with a

period set to include the worst case ringing (D) to appear on the line, virtually all the transient energy can be removed from the line improving the system response.

The innovation described was implemented into the next generation SLIC (TP3250).This system level invention delivered significant improvements on the critical parameter of Dial Pulse Distortion (DPD) enabling the system architecture to meet specifications suitable for the correct working of loop disconnect POTS services for all major global operators.

The author's contribution to this invention was the creation of the conceptual approach using transient detection combined with a time delay. The joint authors (Bremner & Reed) then spent considerable time modelling and researching the optimum thresholds and time delay. This problem is well known to be difficult to resolve in analogue telephony signalling. The final invention is a result of extensive systems analysis by both inventors using simulation, modelling, and laboratory experimentation. Both inventors contributed equally to this invention.

Since the grant of this patent in 1999, 7 subsequent patents have referenced this work. The most recent references in US 6988044 (2006) / US 7,164,997 (2007) by Rambus Inc, and US 7,312,597 (2007) by Infineon Technologies show that the original work by Bremner and Reed is still relevant and is now being applied to fields beyond the scope of telecommunications.

Submission IV Patent No. US 6,028,464:

Title: Transient Signal Detector

Inventors: **Duncan J Bremner**, Lochwinnoch, Scotland;

Assignee: National Semiconductor Corporation, Calif. USA

Filed: Apr 1, 1998

The invention contained in submission IV reflects the physical (circuit schematic) manifestation of the system innovation described in submission 3; a

method of detecting transients signals such as dial pulses and the schematic of that implementation is shown in Figure 16.

The challenge in developing commercial silicon circuits is to optimise the area occupied while reducing the variability and sensitivity to process or environmental variations. The invention described in the submission realises a 'window detector' centred about zero in a highly efficient and controllable manner compared with previous manifestations. Prior art solutions realised this function using many more components and requiring several different adjustments to modify the threshold parameters.

When considering the performance of the disclosed circuit in a SLIC application for detecting the transient signals described in submission 3, the benefits of this circuit implementation immediately become apparent.

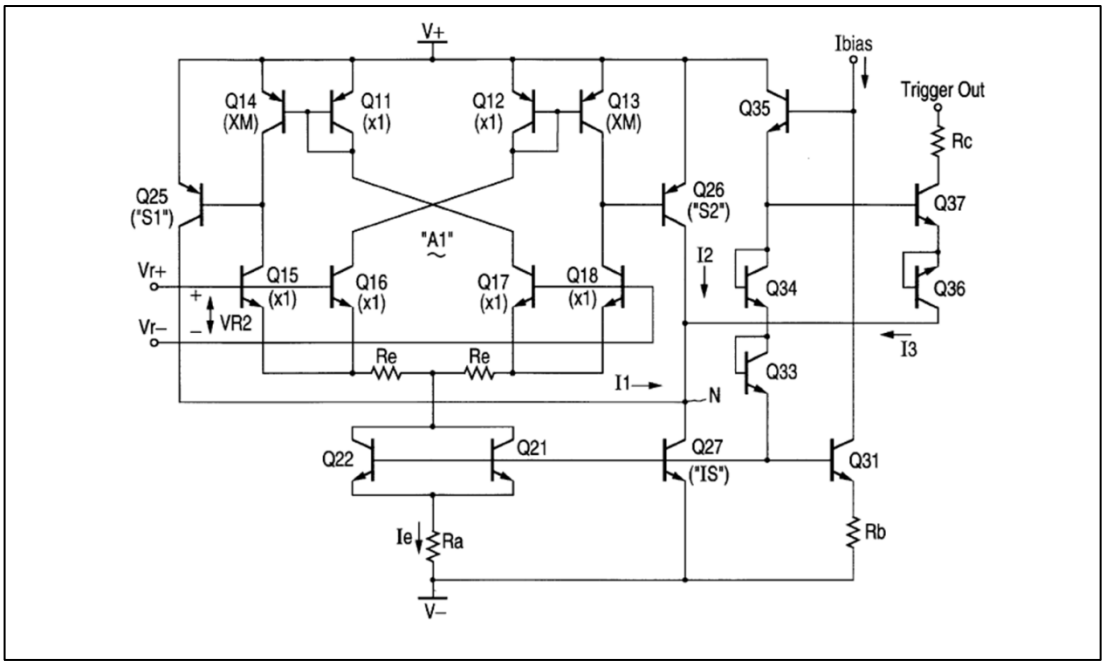


Figure 16: Schematic of Transient Signal Detector
(Source: US 6,028,464 Patent)

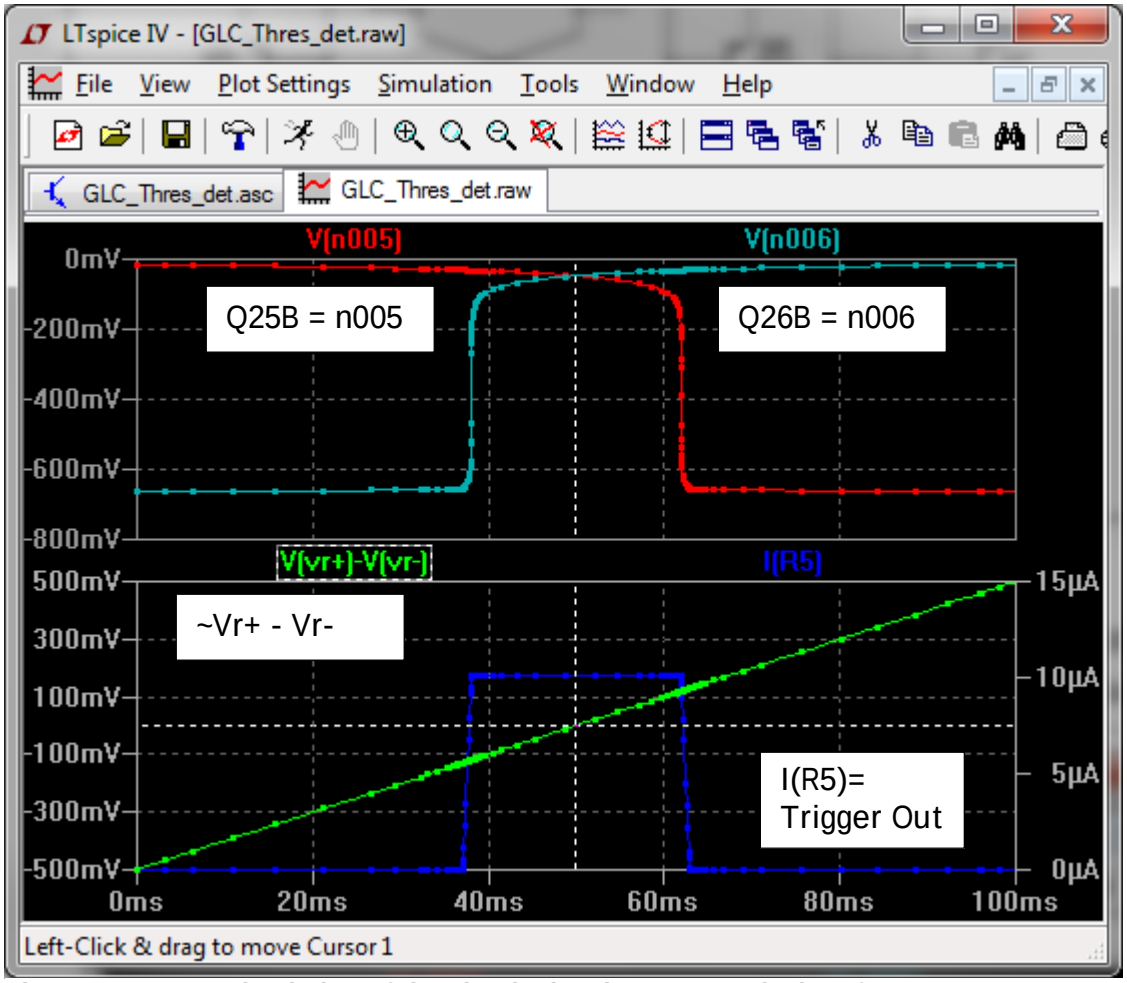


Figure 17: SPICE simulation of the circuit showing symmetrical performance
Source: Author

The first benefit is the threshold voltage for both positive and negative going transients is defined by circuit components and to a first order, can be designed to be independent of absolute circuit parameters; instead being defined by the matching of components or currents.

The second benefit is that all parameters can be adjusted independent of each other at the design stage, giving the capability to define non-symmetrical trigger thresholds for special applications. The conventional approach to establishing a threshold 'window' detector normally requires significant duplication of circuitry in order to manage the bidirectional operating envelope of the circuit.

The circuit was re-simulated in SPICE to obtain the waveform plot in Figure 17 which shows the response of the circuit to a slow, balanced transient ramp at the differential input. The top two traces show the action of the two current steering switches (Q25 and Q26) in the schematic, while the lower trace shows the current appearing at the 'trigger out' pin. As realised the output current is

inverted but it is obviously trivial to generate the logical inversion of this in subsequent circuitry.

This circuit was re-simulated using generic SPICE models as opposed to the bespoke models in the original design which slightly modify the results. In either case, the trigger point of the circuit is defined when either: I(Q14C) =I(Q15C) or I(Q18) = (Q13) at which point one or other of the switches(S1, S2) is turned on. The relationship defining the circuit characteristics as stated in the patent document is:

$$V_{th} = |((1 - M)/(1 + M))| * I_e * Re * \ln M \qquad (9)$$

Where V_{th} is threshold voltage, M is the Q11:Q14 and Q12:Q13 emitter ratio, I_e is the tail current, and Re is the emitter degeneration resistor on the tandem long tailed pair(Q15,16,17,18).

The final and most important feature of the circuit invokes the system level requirement to implement a hysteresis on the desired threshold voltage. In order to implement such a hysteresis and apply equally to both positive and negative detection thresholds, a simple adjustment to the bias current Ibias[11] will adjust the threshold voltage accurately and precisely even when the circuit is operating. This later feature is important when implemented in the system feature described in submission III; threshold adjustment must be applied during the timed delay period in order that a non-stable regenerative situation (instability) does not occur.

This invention, conceptual solution, and schematic realisation thereof is the sole work of the author. Since publication, the work has been cited in 7 subsequent patents by companies such as Agilent Technologies (US 6,556,050), Xilinx (US 6,956,905),and most recently by Matshushita Electric (US 7,282,965) granted in 2007.Although simple in realisation, this circuit is a good example of the analog designers 'art' in component matching and compensation to realise a stable design.

[11] Complex silicon analogue circuits such as SLIC have a central bias block responsible for the generation and distribution of both reference voltages and currents to all other blocks.

Submission V **Patent No. US 5,900,771:**

Title: Capacitive Multiplier for Timing Generation

Inventors: **Duncan J Bremner**, Lochwinnoch, Scotland;

Assignee: National Semiconductor Corporation, Calif. USA.

Filed: Dec 12, 1996

The patent submitted as submission V was developed while designing the TP3250 SLIC product but is applicable to any electronic circuit that requires long time constant timing generation. The specific innovation realised by this circuit design is the creation of relatively long (1-10ms) time delays on-chip without occupying a large amount of silicon area. The particular time delay required was the 'hold-on' delay for the transient speed-up circuit described in submissions III and IV. The absolute accuracy (+/- 20%) would be achievable using on-chip components but the area required was excessive; a novel approach to generating long time delays using innovative circuit design was required.

In discrete circuit design, there is frequently need for timing generation to realise circuit functionality. Timing delays can be generated in a variety of means; the most simple of which is a simple relaxation RC oscillator as shown in Figure 18.

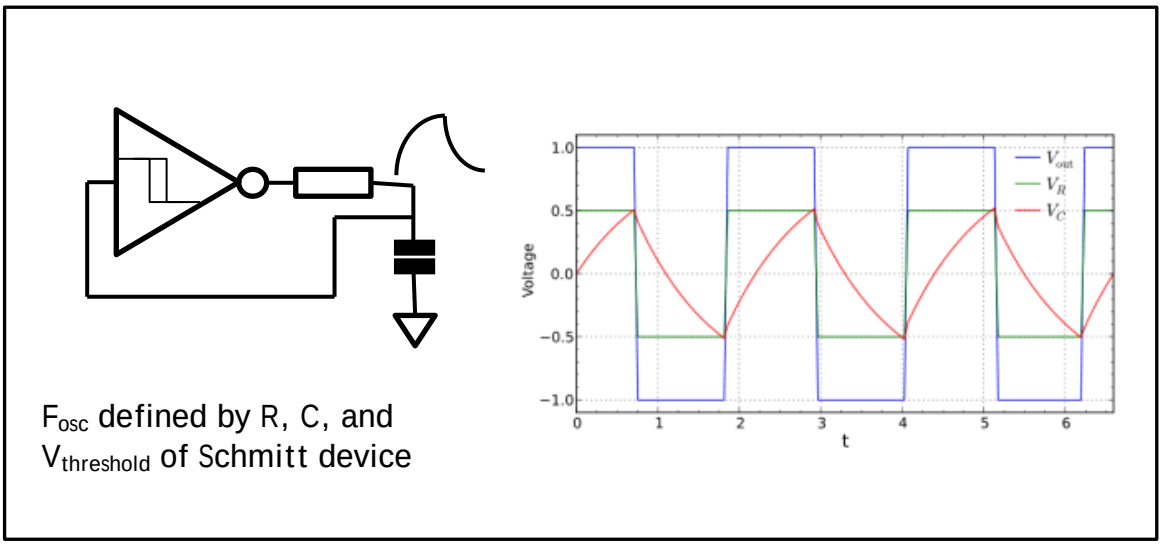


Figure 18: Simple RC Relaxation Oscillator (Source: Author)

In more complex timing circuits a simple Schmitt trigger oscillator may be replaced with a saw-tooth generator using a constant current source to charge the capacitor which improves the linearity of the output and remove the need for the resistor. On silicon circuits, the area occupied by resistors and capacitors

is much greater (expensive) than that of transistors and great effort is expended to eliminate large capacitors or resistors when implementing functions. The invention disclosed here is capable of generating a long time delay (of the order of 10ms) normally requiring a very small current and a very large capacitor to be used.

One solution would be to use a saw-tooth generator based on a very small charging current (typically 1-10nA for 1-10ms delays), however the generation of a defined and very small reference current on bipolar circuits is problematic if the current ratio between the 'standard' reference current (typically 10μA) generated from a central bias block, and that required for circuit operation exceeds a ratio of 10:1. Similarly, capacitor values exceeding approximately 10pF occupy too large an area and would not normally be acceptable for such a simple timing function. Furthermore, and particularly in bipolar design, any input connection to a comparator device connected to the sense node at the top of the capacitor would draw bias current introducing an undefined 'error' current due to bias conditions further limiting the designer's freedom. This error would be directly dependent on the variation in transistor gain (typically +100%, -50%) of any input device and introduce an excessive tolerance on the final delay time.

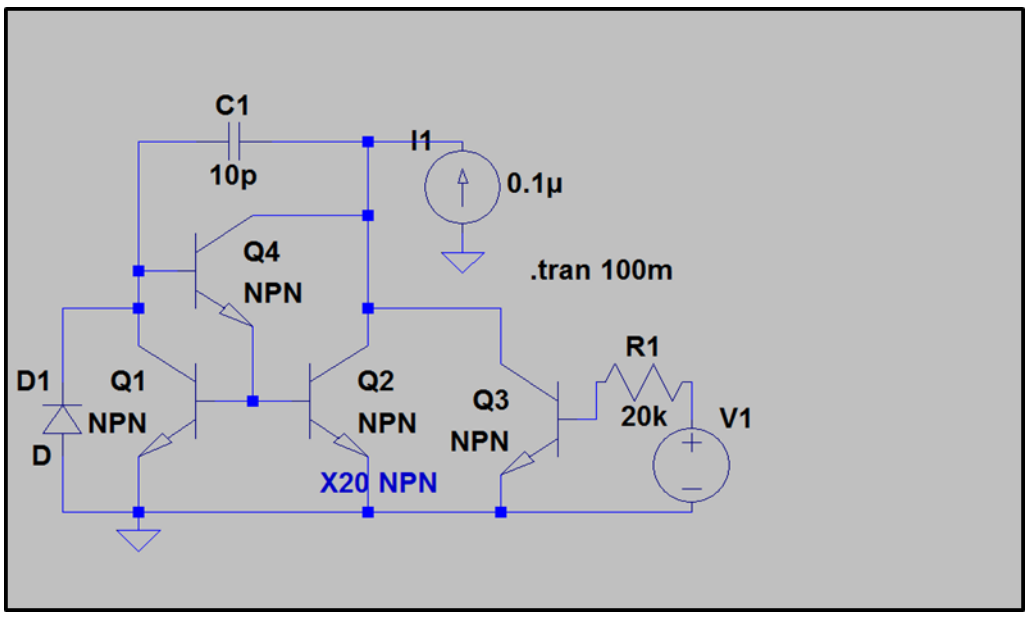


Figure 19: LT SPICE simulation of Capacitive Multiplier
Source: Author

In order to address the challenge of generating a low charging current a new circuit was developed based upon the well understood current mirror invented by Bob Widlar [64]. The circuit was so configured that the current ratio between the input and output could be connected across a charging capacitor such that an accurately defined charging current flowing into the capacitor was small and well controlled while the input level was much larger and derived from that distributed by the bias block. Through careful design of the current mirror, ratios as high as 50:1 could be attained with little degradation of the mirror accuracy while the output node connected to any downstream sense amplifier or comparator had sufficient drive such that any input bias current of such an amplifier did not introduce significant error in circuit operation.

Figure 19 shows the circuit schematic of the implemented scheme alongside the SPICE simulated transient behaviour of the invention (Figure 20). A current ratio of 20:1 between the defined reference current and the capacitor charging current has been established in this example. As the current ratio of the current mirror (comprising Q1, Q4, and Q2) is fixed and << than the β^2 of the transistors ($\beta = 100$), any parametric variation will not significantly affect the delay. Of particular note on the output waveform is the small (1.0V) voltage step occurring at the start of the timing ramp due to the turning on of the current mirror (Q1, Q2) and base compensation transistor (Q4).

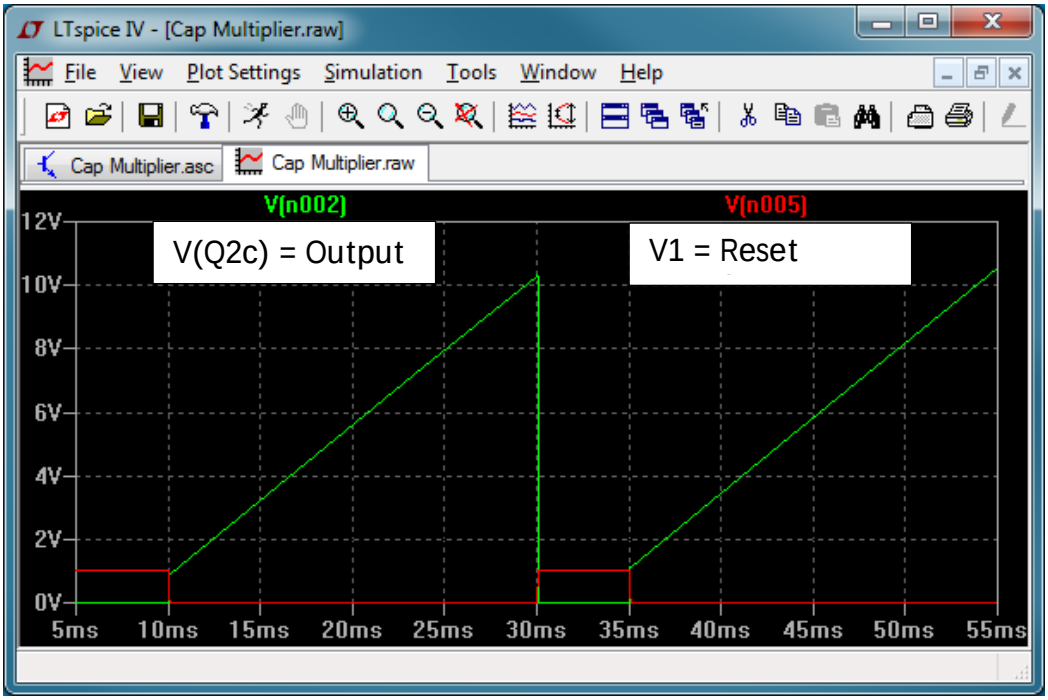


Figure 20 SPICE Simulation of Circuit
Source: Author

Although simple in concept and operation, this circuit innovation had hitherto been unknown for use in timing generation circuits and the patent was granted enabling significant savings in silicon die area compared with the conventional approach.

This invention, conceptual solution, and schematic realisation thereof is the sole work of the author and used in the TP3250 device for timing control. Since the original grant of this patent, it has been cited by 7 subsequent patents, most recently by Upi Semiconductor Corporation in US 8,816,760 (2013) and new application in US 20130241635 (2014). A brief review of the abstracts of these and earlier citations continues to support the underpinning innovation herein; the difficulty and challenge of generating large time delays or time constants on-chip economically. An important and relevant development of this work is captured in the patent US 7,323,928 (2008) where Linear Technology Corporation have further developed the idea to synthesise large value of capacitance for the compensation of Servo loops and similar circuits comprising AC signals.

Submission VI Patent No. US 6,377,681:

Title: Signal line driving circuit with self-controlled power dissipation

Inventors: **Duncan J Bremner**, Lochwinnoch, Scotland;

Assignee: National Semiconductor Corporation, Calif. USA.

Filed: Apr 1, 1998

Much of the developments in modern telecommunications switches focused on size reduction of the overall footprint of the switch while providing more features and functionality to the telephone operating company. However, the power feeding requirements remained fixed according to the specifications and standards adopted by the operator, often dictated by the legacy equipment on the network. The increase in subscriber line terminations within the switch cabinets resulted in a higher power density on the line interface cards and cabinets which increased the internal operating temperature and power dissipation of the switch.

The invention developed by the author to address this problem is described in submission VI and demonstrates a fundamental change to the way power is

supplied to SLICs in order to reduce the power consumption and dissipation within a modern telecommunications switch. Referring to Table 2 and Figure 5 describing the functional requirements of a SLIC; in either transformer or electronic based SLICs, a key challenge is limiting the power dissipation while feeding very short subscriber loops. In Central Office (Exchange) installations, power is derived from a common -48V supply provided by lead acid accumulators (24 x 2V each) capable of maintaining communications services for up to 8 hours [65]. In most modern switches, the common -48V power is converted to the switch operating voltages on a rack-by-rack basis; in the case for most electronic (non-ringing) SLIC solutions, this is between -52V and -60V DC for the high voltage electronic circuits attached to the subscriber loop[12].

Worst case power dissipation and consumption occurs when the switch is powering a majority of short subscriber loops such an a city centre location where line density (and real estate) is highest; therefore a method of reducing both power consumption and dissipation is needed to implement high density subscriber linecards with up to 32 channels per single PCB (measuring typically 250mm x 300mm). Figure 21 illustrates the power dissipation reduction on the linecard by 3 different means (dual supply, series off-load resistor, and per line switching regulator); the dual supply approach results in >30% power savings.

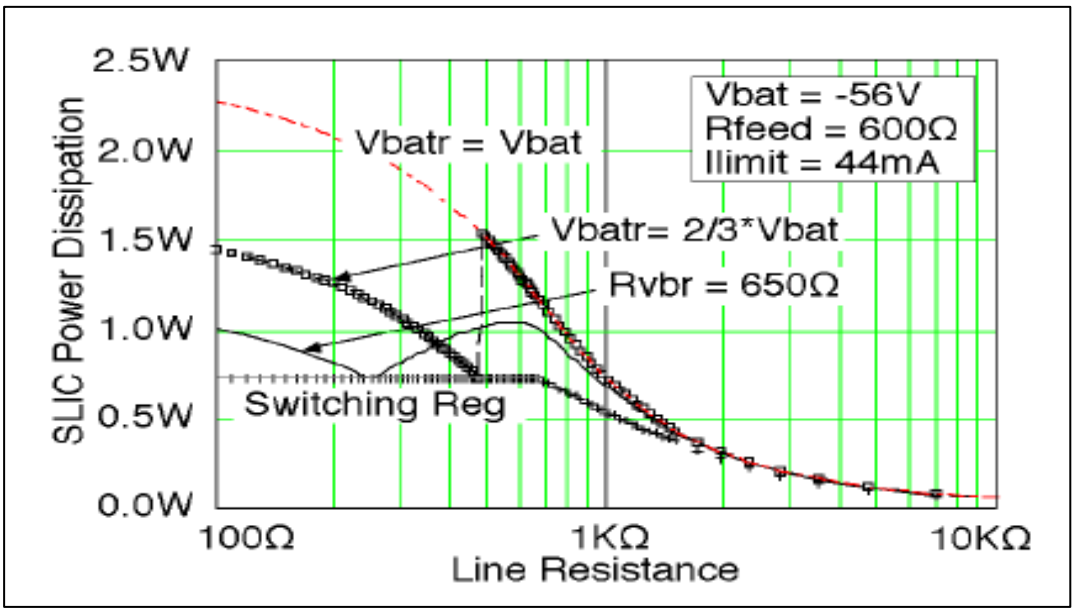


Figure 21: Device Power Dissipation using Power control

[12] Some customer equipment such as PABX's or modems require the ring terminal voltage from the CO to be less (more negative) than -40V before service can be delivered. This is a 'ground start' signal condition and a protection mechanism to prevent damage of equipment due to high voltage ringing signals [33, p. 6.2.2].

(Source: TP3250 datasheet [Submission VIII]

The circuit and system innovation described in submission VI realises a power reduction solution by enabling the high voltage portions of a line interface circuit to connect to the full supply voltage (say -56V) while on hook ensuring full signalling requirements are met, but can operate on a reduced supply voltage (Vbatr) when supplying feed current into short subscriber loops thus reducing power dissipation on the linecard.

An important feature of this solution is the fail safe mode, should the circuitry fail to operate correctly due to extreme or unusual line conditions, the subscribe will always obtain service. The derivation of this innovation was a result of feedback from customers regarding the alternative solution of utilising a built-in switch mode regulator incorporated into a product from AMD. Although the AMD solution reduced power, the switching noise both to the 2-wire line and across the linecard was unacceptable. The innovation described here and shown in Figure 22 overcame these problems by utilising a fully specified rack power supply to provide the reduced voltage for Vbatr while simultaneously providing the normal Vbat supply (-52 -> -60V) thus only marginally increasing costs. Further details of the circuitry and the application benefits are also explained in submission VIII under 'Power Management'.

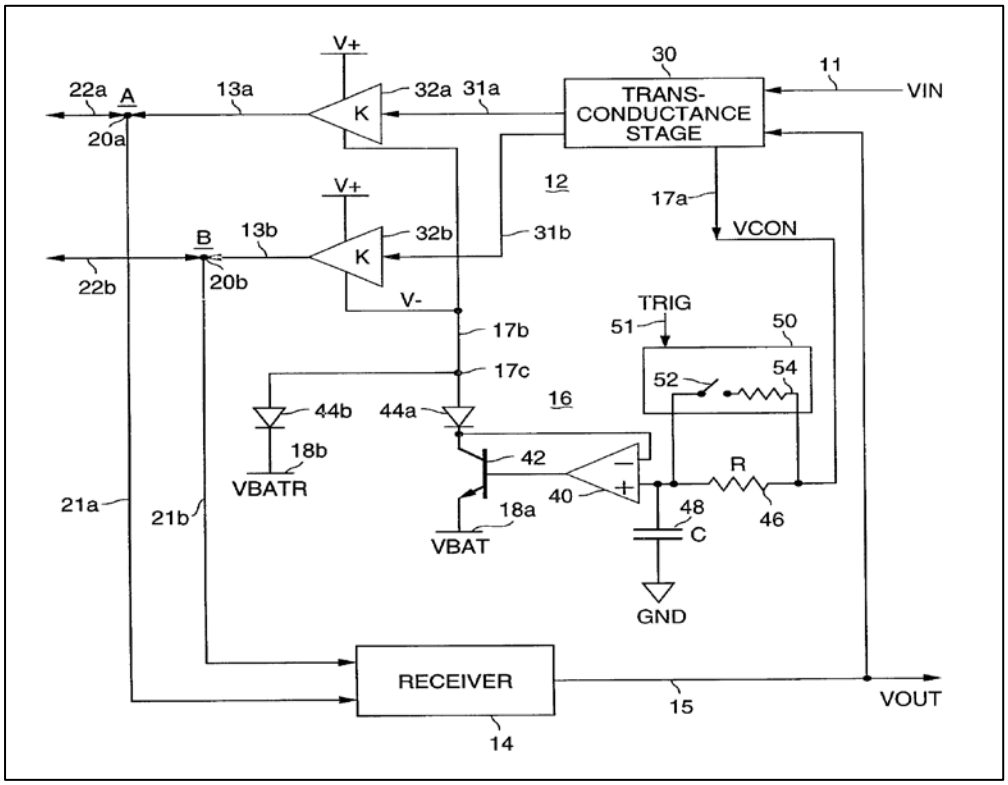


Figure 22: Dual Rail supply for Improved Power Efficiency
Source: Submission VI

This invention, conceptual solution, and schematic realisation thereof is the sole work of the author and was implemented in the TP3250 SLIC Solution. Since the grant of this patent in 2002, 5 more patents have cited this work, the most recent being patent US 8,379,839 granted to Microsemi Semiconductor Inc. in 2013.

The concept of utilising multiple power rails had been used with mixed success in some domestic audio amplifiers [66] prior to the date of this invention, however the operating conditions are considerably more benign. The challenge in this design is ensuring the circuit always works reliably (irrespective on the supply conditions on either supply) and the signalling specifications are achieved.

Submission VII **Patent Application No. DE 19,914,858: (published in German), accompanied by original concept document in English**

Title: Creating interface for local tests and for carrying out local tests at telephone user line and determining several electric characteristics of such user line

Inventors: **Duncan J Bremner**, Lochwinnoch, Scotland;

Assignee: National Semiconductor Corporation, Calif. USA.

Filed: Dec 12, 1996

Telephone network service providers incur significant costs due the maintenance and upkeep of both the central office equipment and the external cable plant [67]. In traditional Central Office (Exchange) architectures each subscriber interface circuit is provided with a test access relay which enables the service provider to check both the condition of the subscriber line and also the performance of the electronic SLIC circuit. In a traditional Central Office (Exchange) architecture, the test bus connects to a single suite of test equipment which although very expensive in absolute terms, when

Figure 23: Telestra Remote Integrated Multiplexer (DLC) (Source: [84])

amoritised across the total number of lines in a large Office, becomes financially viable. However, as the demand for telecommunications services increases, telecom providers began deploying remote units to terminate subscriber lines closer to the subscriber's premises and transporting the traffic back to the core network switch via digital connections over fibre links. These Digital Loop Carrier (DLC) [68] units are still required to provide full test capability but due to the smaller subscriber connections, cannot support the full test suite. An example of a typical DLC installation illustrating the problem is shown in Figure 23. The invention described in submission VII is a test solution integrated into the Subscriber Line Circuit which can deliver sufficient functionality and performance testing in a cost effective manner.

Submission VII (in German) is the text of a patent filed in Germany for a built-in test scheme and capability within the Interface circuit itself. The invention was filed in Germany as a key customer (Siemens) expressed interest in incorporating and exploiting the test capability within their EWSD switch modernisation programme. Included in the Appendix along with the German filing is the original National Semiconductor Invention disclosure. This was retrieved from private sources but explains the tests described in the patent document.

This invention, conceptual solution, and theoretical analysis thereof is the sole work of the author. This patent application was filed but never pursued by the company as the product group owning the work was disbanded. Nevertheless, the fundamental innovation of realising subscriber line testing on a per line basis utilising a modification of the existing circuitry remains valid.

Submission VIII Product Datasheet & International IC China (IIC) Conference Paper(1998)

Title: a. TP3250 Programmable SLIC; Preliminary Datasheet
b. Next Generation Subscriber Line Interface Solutions, International Integrated Circuit Conference, Shanghai, 1998.

Authors: **Duncan J Bremner**

Published: August 1997

Submission VIII reflects the culmination of knowledge in developing Subscriber Line Interface Circuits (SLICs) for analogue applications and incorporates all the previous innovations to realise a highly configurable line interface product, theTP3250. This device formed the High Voltage Interface between the subscriber line and the low voltage logic circuitry within the switch. The TP 3250 and the TP3090 (Combo IV™) pair combined to realise the application solution promoted by National Semiconductor as the Global Line Card ™ (GLC).

The system was capable of realising the transmission, signalling and feed characteristics of all major global operating authorities and as such, was the first such integrated solution to address all the major markets. In particular, the performance of the solution incorporated additional features such as Subscriber metering[13]. A key feature of the GLC system was the incorporation of on-chip ring signal generation sufficient to meet the requirements around the globe for analogue telephone instruments. Generation of on-chip ringing required the development of a specialist High Voltage process which combined the packing density sufficient to realise the complex circuit blocks with HV performance capable of 170V peak. This specialised process, knows as VIP-4H exploited bonded wafer, Silicon on Insulator technology and is described by Bashir [69]. This leading edge process also enabled the effective separation of subscriber line referred signals (High Voltage) and Central Office (Exchange) side low voltage referred signals in an architecture with a separation barrier capable of withstanding up to +/- 200V between these two, nominally ground referenced signals without any propagation or damage of any high voltage faults into the sensitive switching equipment logic shared by all subscribers. This ensured that any local fault did not compromise switch functionality for other subscribers and is further described in submission IX.

The TP3250 datasheet and preparation thereof was the work of the author who was team leader, system architect, and carried out some of the analogue circuit design on the project; however this was a large project and the datasheet contains the results of other team members, particularly Reed and Benton who worked on the project.

[13] Subscriber Metering [83]enabled customer premise equipment to register billing 'pulses' of either a 12 or 16 KHz high level signal (>2Vrms) which would record the cost of the call on a meter within the customer premises; these were particularly popular in Europe.

The IIC paper was the author's work based on the product known as the Global Line Card (GLC) and submitted to the conference.

Submission IX Book Extract: Application Note; AN-639:

Title: 'High Voltage Protection Application Note for protection of SLIC devices against power cross and lightning'; National Semiconductor Telecommunications Products Databook; 1995

Authors: **Duncan J Bremner**, Lochwinnoch, Scotland;

Published: January 1990

The final submission in theme 1 is an application note describing the challenges of protecting Subscriber Line Interface Circuits against the effects of Lightning strike or power (mains voltage) contact directly to the external subscriber line pair.

A significant challenge in designing telecommunications switches is ensuring resistance to hostile conditions where the external and exposed subscriber lines are exposed. Many of these conditions were historic in nature and experienced in the USA during the initial deployment of telecommunications. Due to the service provider's requirement to be backward compatible, interface circuits had to be capable of withstanding and protecting against these legacy situations. Two particular conditions place particular challenges on the linecard systems designer; lightning and power cross. As subscriber loops were historically strung

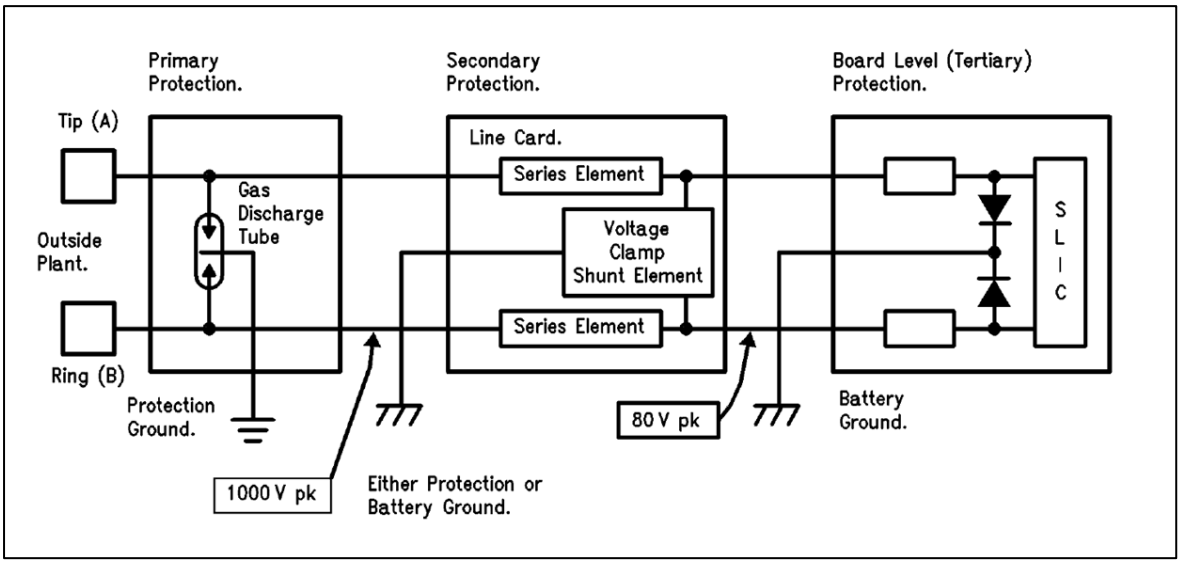


Figure 24: Protection Architecture for TP3210 and TP3250
Source: (AN-636 (submission IX))

overland on telegraph poles, the incidence of lightning strike to the subscriber cable plant was high. As the subscriber telephone was 'floating', that is, did not have any local connection to earth, it was the task of the central office to shunt the lightning to earth. The standard design requirement for lightning testing is 4000V from a source as defined in the ITU-T K.20 Standard [37]. Subscriber line protection is split into 3 levels; primary, secondary, and tertiary. Primary protection installed on the Main Distribution Frame (MDF) uses gas discharge tubes limits the disturbances to less than ~1000V peak, secondary protection on the line card uses electronic over-voltage protection to clamp transients to less than ~80V peak (Ringing SLICs such as TP3250 require a more complex device), before reaching the tertiary protection on the subscriber circuit which protects the sensitive logic signals in the core of the switch, Figure 24.

The second challenge is power cross which can occur either accidently or maliciously on the subscriber loop. Voltages up to 600Vrms must be withstood to ensure that no damage is incurred by the switch. In order to separate fault and isolate fault conditions occurring on the subscriber cable plant, the switch architecture utilised separate battery and electronic ground connections. However, during either lightening or power cross faults, the interfering pulses can give rise to inductive 'kick-back' between the high voltage battery ground and the internal electronic (logic) ground of as high as 100Volts[14]. It is imperative that transients or faults on one (or more) subscriber loop are not permitted to propagate into the switch core circuitry which could corrupt other calls in progress. Both the SLIM™ and the GLC™ had architectures and features which ensured effective separation between battery ground and electronic ground referenced circuitry. This architecture most closely mimicked the isolation performance of the original transformer SLICS and although not galvanically[15] isolated, provided similar levels of protection.

[14] A Central Office star grounding system is normally referenced to the protective earth external to the Central Office Building. The round trip wire distance between the subscriber line card and the logic ground could be up to 50metres although the physical separation on the linecard is only a few millimetres.

[15] **Galvanic isolation** is a principle of isolating functional blocks of a system to prevent current flow; no direct conduction path is permitted. Energy or information can still be exchanged by other means, such as capacitance, induction, electromagnetic, optical, acoustic or mechanical means.

This work was the sole work of the author who has particular expertise in high voltage design and protection. This work has been cited by several other organisations involved in the protection of telecom equipment. The most recent reference is in patent US 6,418,221 (2002) by Broadcom Corporation in association with signal coupling in ADSL connections.

Summary of Theme 1

The innovations and inventions captured within Theme 1 give a realistic summary of the development activities undertaken in the field telecommunications to extend and increase the capabilities of fixed wire connections. The greatest challenge presented to both the equipment providers and the component designers is managing the network legacy issues and the variability and unknown nature this presented. The external cable plant and legacy customer premise equipment are two areas which, due to space constraints in underground conduit installations, are limiting network development. The cost and practicalities of upgrading underground plant is now extremely challenging, not least due to the cost of providing temporary service while the upgrade takes place.

The technologies discussed delivered the capability to provide mass network access over the existing voice network and provided effective data access via modem technology. Modem technology delivered the first public access onto the internet in the late 1990s before giving way to first ADSL, and now VDSL; both operating over the same 20th century subscriber connections which were originally installed to provide simple voice communications and now being pushed to deliver streaming video signals up to 8Mb/s. There is general acknowledgement that the subscriber connection is the bandwidth bottleneck and requires upgrading. One solution could be simply to replace all subscriber loops by fibre connections capable of delivering greater access speeds however, as will be discussed in the next theme, the choice of technology and topology for a fibre roll-out is not simple and there are examples of several administrations who completed fibre roll-out in the 1990's only to realise their choices of technology has been overtaken and now must be replaced.

Theme 2: Optical Access Technology

Whereas the submissions in Theme 1 focused on the network access over the so-called 'last mile' from the network to the customer premise, the focus of theme 2 is the development of on-premise data networks and their extension into the network which culminated in network access from the customer premise to the network, referred to by data com specialists as the 'first mile'[16]. Although only a single submission is presented here, the work underpinning this was 3-4 years of development work on various Ethernet technologies [70] for intranet and datacom networks over both copper (Cat 5, Cat 5e, Cat 6) and also single and multi-mode fibre connections.

The work presented in submission 𝕏 is related to a prototype system developed for a demonstration of very high speed fibre connections (10Gbps) from the network to the customer's premise. This demonstration was performed in collaboration with BT and the BBC so the costs associated with fibre deployment could be examined between PON and Point-to-Point fibre connections.

PON vs Point-to-Point

During the period 2002 - ~2006 there was significant efforts by the service providers to investigate the business proposition of deploying fibre into the local loop. This approach was variously known as Fibre-to-the-Home (FttH), Fibre-to-the-Curb (FttC), or fibre last-mile. The providers had reluctantly reached the conclusion that copper loops from the last century would not be capable of delivering 25Mbps and beyond; the copper loop had to be replaced by fibre. The cost of replacing the copper subscriber in a simple 1 for 1 replacement exceeded the financial reserves of the service provider's finances[17] so various alternative architectures and compromises were explored to reduce the cost.
One area of technological comparison was between Passive Optical Networks (PONs) versus a direct point-to-point connection to the subscriber premises over fibre.

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[16] From the customer's point of view it is their "first" mile, although from the access networks' point of view it is known as the "last mile". A working group of IEEE produced the standard known as IEEE 802.3ah, which was later included in the overall standard IEEE 802.3-2008.

[17] Anecdotally, the cost of replacing the copper lines with fibre in the UK was estimated at £17B in 2004. Due to the falling subscriber revenues, this was judged too expensive for British Telecom (now Openreach) who manage the subscriber connections.

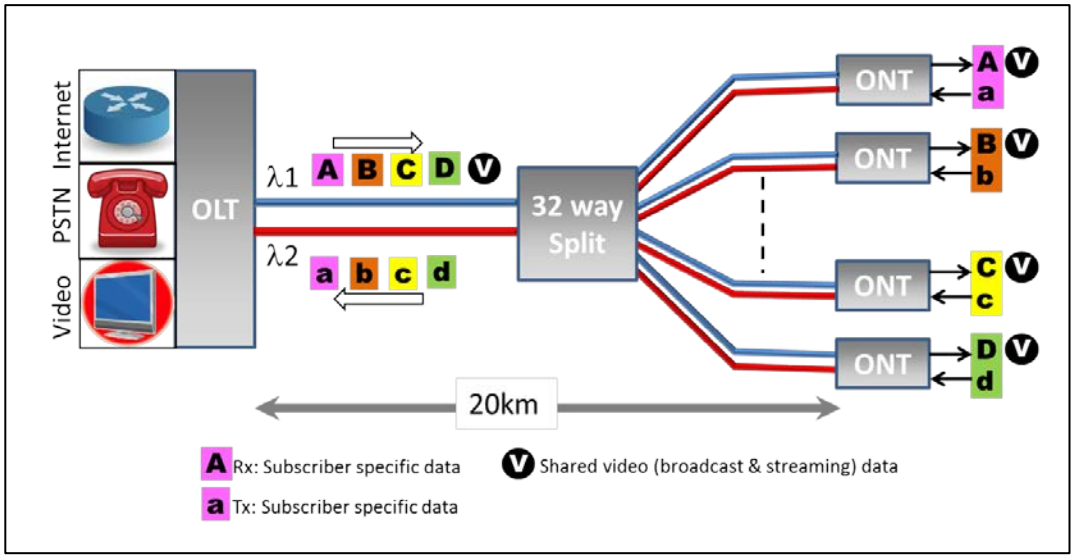

Figure 25: PON FttH Architecture
(Source: Author)

In PONs (Figure 25), the Central Office subscriber line interface consists of either a single or fibre pair (Tx & Rx) with a high speed physical layer transceiver driving the fibre which is split to many separate subscribers using passive optical splitters deployed along the fibre route. Although the split ration may vary, typically they are designed as 64 split or 128 split over a distance of 10km. However there are considerable challenges in operating a PON at high speed, not least because the propagation time through the fibre and splitters must be carefully balanced to ensure that the time of arrival of packets at the most remote nodes is comparable to the closest nodes. Additionally in a PON architecture, if the head end transceiver is capable of (say) 10Gbps, then all other nodes in the network must also be capable of receiving data at the 10Gbps rate even though, with a 64:1 split ratio, each end station can only receive a long term average of 156Mbps. Although this is considerably faster than the connections being deployed in 2010-2013, it is worth noting that high quality HD video information, such as is available over HDMI [71] cables would demand 340Mbps.

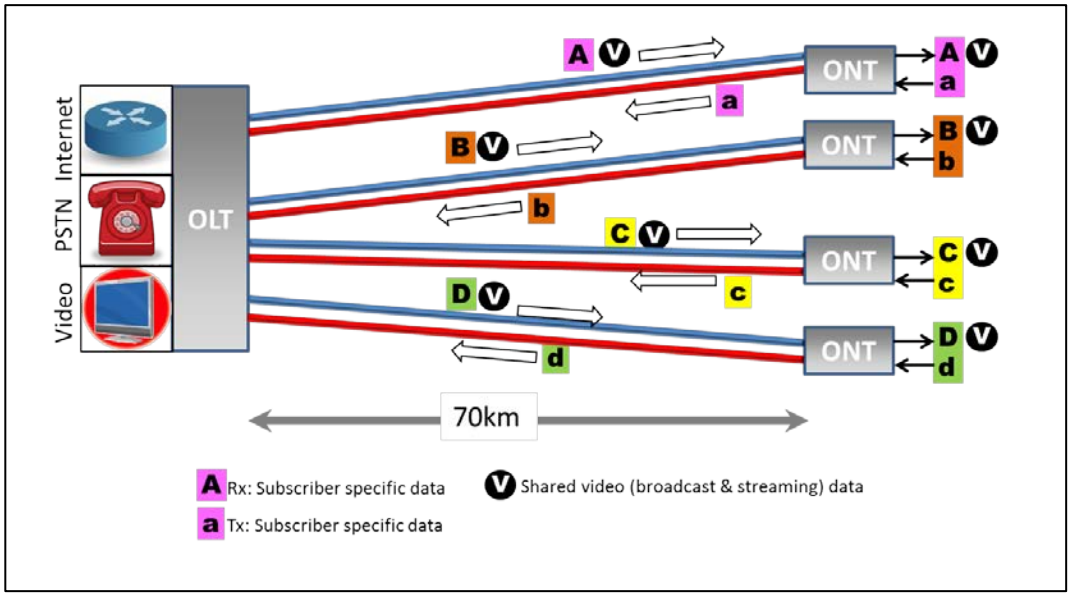

Figure 26: Point-to-Point Architecture
(Source: Author)

The alternative approach is to connect subscribers in a point-to-point architecture (Figure 26). In this format there is a 1:1 correlation of head end cables connecting directly to subscribers with no optical devices in between. If the same optical networking termination (10Gbps) is used as the PON solution then each subscriber would have a 10Gbps connection direct to the network termination point. However if the physical fibre connection was down-graded to 1Gbps, the optical transceiver cost would be reduced while the link speed to the subscriber would be 1Gbps, 6 times faster than the PON solution. Additionally, the removal of the splitter device allows longer fibre runs between the head end and the subscriber (or a reduction in launch power from the head end).

Submission 𝕏 describes an invention created as part of a business case and technical study into the challenges and benefits of delivering very high speed connections (up to 10Gbps) to end customers for video, voice, and data services.

The objective of the work was to investigate both the technical and business challenges in developing low cost Fibre-to-the-Home technology capable of delivering speeds up to 10Gbps over a single fibre connection. The project deliberately chose this very high speed connectivity in order to explore the implications and impact on both the network and end-user behaviour if connection bandwidth was effectively unlimited. Figure 27 shows the top level demonstration architecture showing the service delivery options implemented over a CWDM 4-lambda solution on a single fibre.

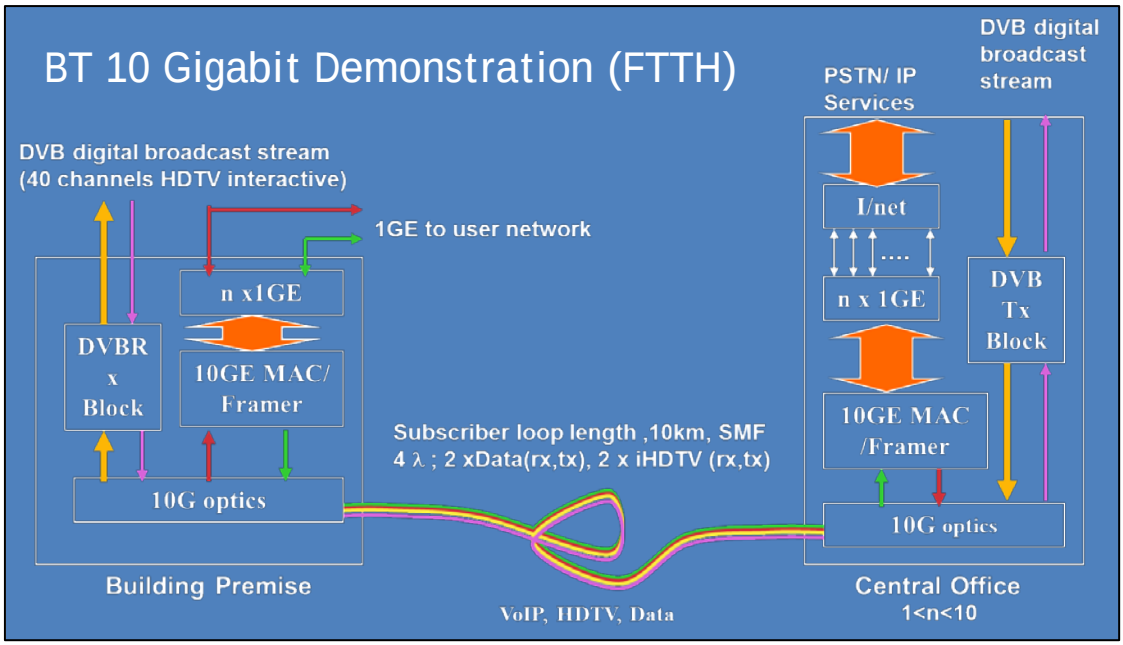

Figure 27: Service level overview of FTTH Demonstration (Source: Author)

Although this was a demonstration project drawing on commercially available products, equipment, and resources, significant effort was made to ensure when over specified components were used, the performance and requirements of more appropriate components were considered in cost and performance estimates. A case in point was the use of high performance 10Gbps long haul optical transceivers instead of optimised products for the 10km Metropolitan Area Network (MAN). Part of the project was the consideration of the optical componentry required at both the customer and network end of the fibre connection. Two solutions were considered, the first using 2 lambda optics (1 for data, 1 for broadcast information) combined with circulators to ensure the streams of bi-directional optical information were appropriately separated from each other. The second and preferred solution was to use a 4 lambda solution; one colour for each of the 2 bi-directional paths (Figure 28). This solution was chosen as a lower cost implementation when compared against the added costs of circulator components. Note that in both solutions, the broadcast and data (TCP/IP) connections were separate. This feature was and remains important as Quality of Service (QoS) for time sensitive video information is not possible over a packet network without buffering. During the project it was recognised that cost benefits could be gained if both information types could be integrated onto a single optical Tx/Rx channel pair. At the time of this work, no suitable

standard existed allowing this requirement to be met and this was identified as an opportunity on which the industry could collaborate.

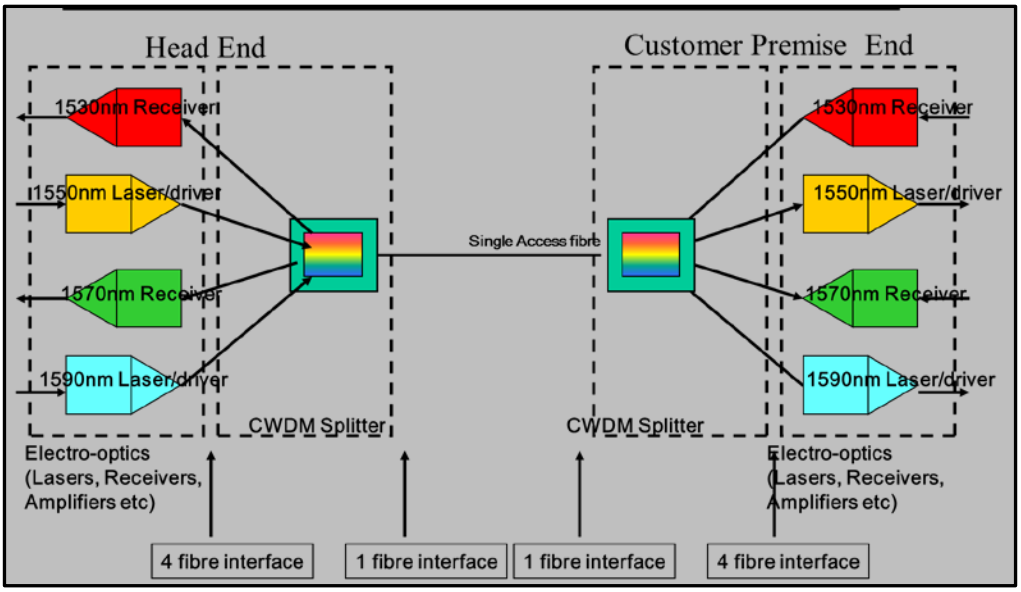

Figure 28: Conceptual Optical Architecture of Demonstrator (Source: Author)

In addition to the optical components significant electronic functionality is required to manage the connection. Again, for ease of demonstration, existing components were utilised (10Gbps product developments were notoriously expensive and complex). The electronic system architecture shown in Figure 29 illustrates the complexity of the high speed electronics required to realise such

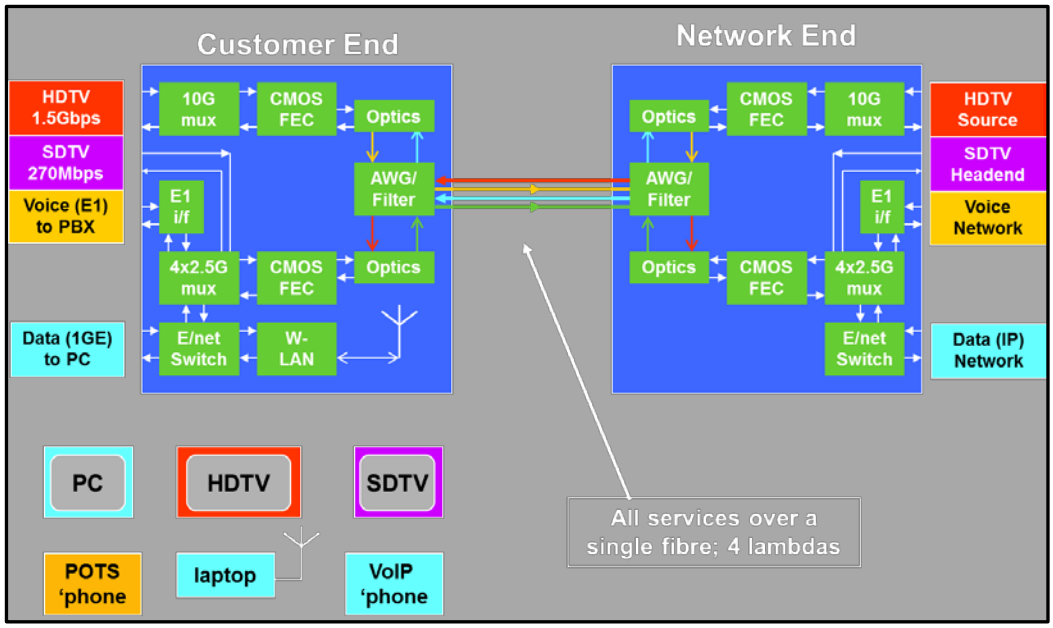

Figure 29: Electronic Functional Diagram of Demonstrator (Source: Author)

a demonstrator. The identified blocks had been developed in other products but would require integration to meet company cost targets (which are confidential).

The project was undertaken between the Intel Corporation, British Telecom Research (Martlesham), and BBC Research. The results of the study indicated the incremental cost difference between PON and point-to-point architectures showed a PON architecture was approximately 20% less expensive on initial deployment (predominantly fewer high speed optical transceivers at the network end) but the flexibility and upgrade possibilities using Point-to-point were considerably better. This information can only be offered anecdotally as the detailed analysis belongs to Intel Corporation and the consortia.

The author was the lead engineer in the creation of the demonstrator concept, overseeing and troubleshooting the development, and ultimately deploying the demonstrations in both at BT's Martlesham research facility and later with China Netcom in Ningbo. The photograph in Figure 30 shows the final demonstration system contained in the two blue rack systems (one Customer end, one exchange end).

Figure 30: Demonstration equipment on site
(Source: Author)

Submission X Patent No. US 7,266,302

Title: Asymetric Optical Network Traffic Flow Control

Inventors: **Duncan J Bremner**, Lochwinnoch, Scotland;
Finn Helmer, Blanefield, Scotland
Evind Johansen, Horsholm, Denmark

Assignee: Intel Corporation, Calif. USA.

Filed: Jan 28, 2003

The invention contained in this submission was a result of examining the impact of high speed optical access on the core network if end customers' bandwidths were able to upload or download full speed, high definition video files. Although the technology can be applied to the individual subscriber network connections over fibre, the invention is targeted at traffic management within the core network.

In order to appreciate the application for the invention we will consider the impact and bandwidth requirements of an on-line video provider (such as Netflix) delivering streaming video to a population of households. This example clearly demonstrates the asymmetric nature of such a service, however the analysis can be applied to any and all data traffic flows. In the Netflix application, the data sent to the provider to request a given movie download stream is small (title request, account details, and start time etc). The information from the provider is large (a complete movie) and places significant networks demands regarding Quality of Service (noting that as previously, packet networks can only use over provisioning instead of guaranteed bandwidth as demonstrated by connection based protocols.

The invention as described is for use within the core network to balance the demand for downstream data versus upstream. In the case of streaming video, the downstream path is two orders of magnitude greater than the upstream path. Although this can be managed at the time of network deployment by ensuring a greater bandwidth in one direction compared with the other, this is not reconfigurable dynamically. The invention proposed in the submission allows the re-provisioning of bandwidth according to the network traffic demands and can be reconfigured 'on-the-fly'.

The innovation of the invention is the use of electro-optical absorption detectors which can serve the alternative duties of laser modulator or receiver. As modulators, they are capable of modulating the chosen wavelength up to 10Gbps while as a receiver they are able to detect signals at the same speed. Using this approach, combined with low cost optical assembly techniques, it is possible to construct a 4 lambda communications channel with 'tidal traffic' management, that is the direction of information travel is adjustable under network control and can be modified on a channel by channel basis to optimise the gross end-to-end communications based on traffic statistics.

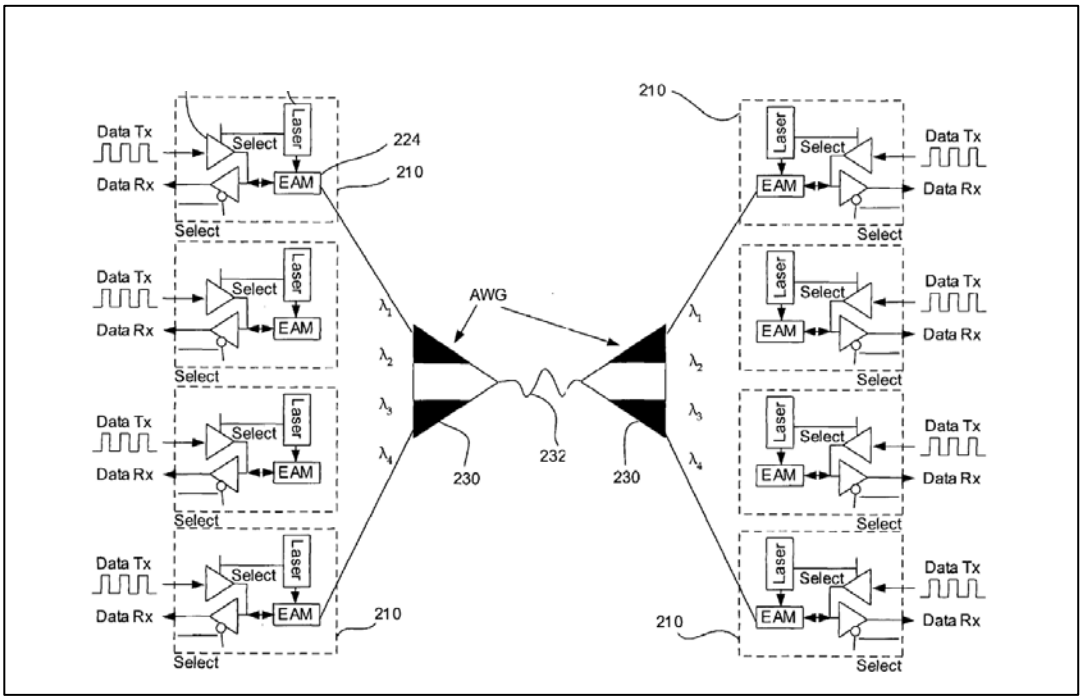

Figure 31: Asymmetric Traffic Flow over Fibre
(Source: US 7,266,302 Patent)

Figure 31 shows the block diagram of the scheme proposed over 4 wavelengths as this can be achieved cost effectively. The invention could be expanded to include many more wavelengths although the cost of the lasers and associated Arrayed Wave Guides (AWGs) would increase as the channel selection was improved.

This invention was the joint work of Bremner, Helmer, and Johansen building on their combined expertise and knowledge of optical access technologies and topologies. Elements of this invention were employed in the demonstrator.

Theme 3: Wireless network access technologies

The submissions submitted previously were focused at component or subsystem level, incorporating innovation into products to deliver marketing advantage over either the existing or emerging technologies.

The innovations and inventions submitted as part of theme 3 reflect the up-scaling of invention from the physical implementation and realisation of the function to the application level. Here, the innovation focuses on delivering improved functionality or capability to the end user at the application level.

The two submissions in this theme are associated with the emerging standard for Ultra-Wideband(UWB) wireless communications. The first submission proposes an extension of the capability of the UWB Standard created by the WiMedia Alliance to triple the download speed throughput for the express purpose of high speed file transfer with a burst rate of up to 2.7Gbps over a short distance. The second submission is the invention of a highly effective, low cost UWB antenna capable of operating over the 3GHz to 10GHz range.

Ultra-Wideband Technology and Development Programme

An £8.5M development programme was led by the author in 2004 to research and deliver critical components meeting the emerging global UWB standard being prepared by the WiMedia Alliance. The emergence of the new standard was in response to the rapid adoption and deployment of Wireless LAN (WiFi) by consumers resulting in band congestion and restricted bandwidth.

The emergent UWB technology was heralded as delivering individual connections between 53 and 480Mbps, multiple bands thus allowing several UWB routers to occupy the same air space. In addition to the improvement in data rates, the new standard developed a new Media Access Controller (MAC) capable of bandwidth reservation which is required for time sensitive information. This feature would allow the effective streaming of video or audio over wireless without the inherent problems of latency associated with WiFi's best efforts transmission protocol.

The development programme focused on opportunities to create differentiation in the emerging UWB market through the development of technology not yet available from other commercial suppliers or additional features which may enable new applications other than those converting from WiFi. After completing a competitive analysis of the products available or known to be in development, the programme identified 3 main areas for development: i. very short range (10-20cm), very high speed (up to 2.7Gbps) data transfer, ii. the design of an RF front end in a standard CMOS technology capable of operating across the whole band (3.1 – 10.6GHz), and iii. the development of antennae covering the full band and delivering improved performance compared with existing solutions at low cost.

System Analysis

A top level system analysis was performed to establish the overall capabilities of the system and the performance targets required by various system blocks [72]. Although the programme focused on the RF analogue front end design, the general architecture of the baseband processor and MAC was also considered to gain understanding of the overall systems limitations. After considerable analysis, it was decided that the system partitioning should occur immediately before the Digital to Analog Converters (DAC) in the transmit direction and immediately after the Analog to Digital Converters (ADC) in the receive direction. This decision permitted all the baseband and MAC functions to be implemented in a conventional digital process and development toolset, and provided a logical and clean interface to third party solutions. Furthermore, the

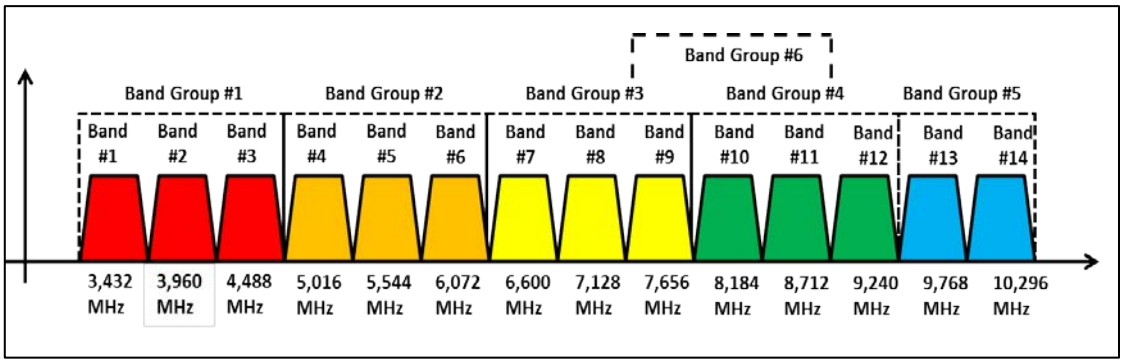

Figure 32: WiMedia Alliance band plan
(Source: WiMedia Alliance [75])

inclusion of the advanced high speed converters allowed the RF front end to implement an extension feature delivering very high speed data connections up to 2.7Gbps

The UWB architecture was developed around an air interface bit rate of 480Mbps per band and the standard allowed for 14 bands each of 528MHz, although not all bands were available in every geographic region. These 14 bands were then arranged into 6 band-groups used to ensure the wireless links were more reliable in the presence of fading. Full details of the standards are available as ECMA-368 and ECMA-369 [73], [74]. The original WiMedia specification still exists but no further work will be carried out on the original specification [75] as the WiMedia Alliance working groups are now disbanded.

The band plan shown in Figure 32 shows the centre frequency of each band and associated band group. Given the relatively high operating frequency and bandwidth, the standard includes frequency diversification (frequency hopping) per channel across each Band Group such that each symbol in the transmission is transmitted on a different band. This has the added advantage that the average transmitted power (dBm/MHz) remains within the -41.3dBm/MHz limit.
However, the frequency hopping characteristics between adjacent symbols place significant constraints on the implementation of the RF front end, the standard requiring frequency hops to settle within 9.47ns.
The TFC standard within the specification also enabled realisation of high speed communications as described in submission XI. Although this feature does not meet the standard defined by the WiMedia Alliance, in the case of the very short transmission distance (<20cm), the interference caused will be minimal.

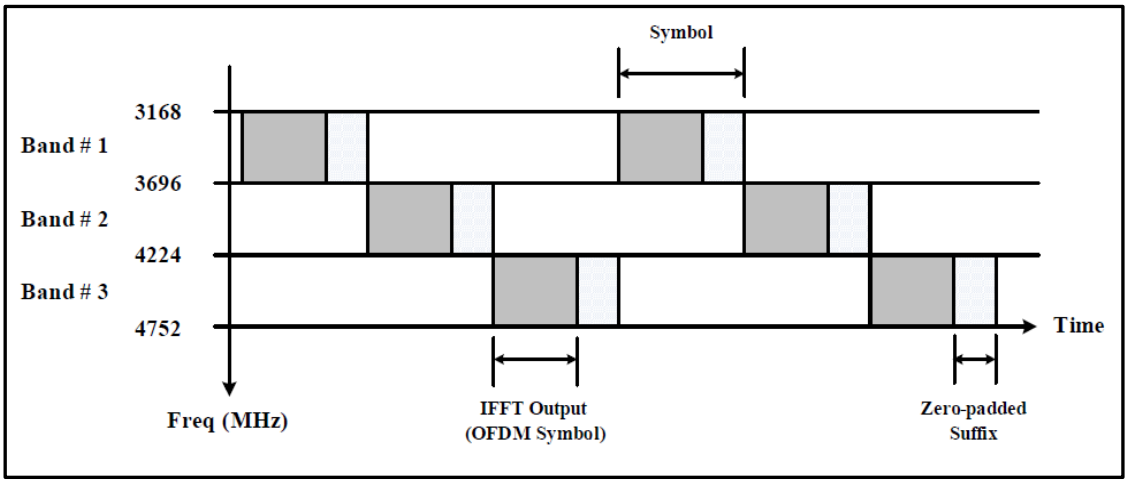

Figure 33: WiMedia Time-Frequency Coding(TFC)
(Source: Wimedia Alliance [75]**)**

UWB Range

The maximum transmit power mask of -41.3dbm/MHz places severe restriction on the maximum communication range for UWB equipment. This is further impacted by the reduction of range as a function of frequency and calculation of the maximum range possible at different data rates was necessary. A summary of these can be found in Table 5 and Table 6. Both tables show the range estimates based on Line-of-Sight (LoS) calculations, although in a real application a fading margin of at least 3dB should be considered. The differences in operating range between these two tables reflect the range reduction when operating in Band Group 5 compared with Band Group 1. This reduction is partially accounted for by the additional loss in the Mean Path Loss due to

UWB Link Budget - Standard Compliant Rates Calculated in 528MHz Bandwidth				**Notes**
Info Rate	480Mbps	200Mbps	110Mbps	Defined by WiMedia Spec
Frequency	3882 MHz	3882 MHz	3882 MHz	Band Group 1 Centre Frequency
TxPower	-41.3dBm/MHz	-41.3dBm/MHz	-41.3dBm/MHz	Defined by FCC / WiMedia Spec
Total Bandwidth (528MHz)	27.2dB	27.2dB	27.2dB	Adjusting for Channel Bandwidth (528MHz)
Averaging (over 3 bands)	4.8dB	4.8dB	4.8dB	Benefit through TFC technique (WiMedia Standard)
Tx Antenna Gain	0.0 dBi	0.0 dBi	0.0 dBi	Default / worst case
EIRP	-9.3dBm	-9.3dBm	-9.3dBm	= -41.3 + 27.2 + 4.8 = maximum Radiated Power
Range	9.1m	14.4m	21.1m	Iterated until EIRP + Mean Path Loss = Receiver Sensitivity
Mean Path Loss	-63.4dB	-67.4dB	-70.7dB	Free Space Path Loss = 10 log ((4 π d / λ) ^2)
Receive Antenna Gain	0.0dBi	0.0dBi	0.0dBi	Default / Worst Case
Shadowing/Fading Margin	0.0dB	0.0dB	0.0dB	0.0dB
Min Rx Signal Level	-72.7dBm	-76.7dBm	-80.0dBm	= EIRP + Path Loss = Received Signal
NPSD	-174dBm/Hz	-174dBm/Hz	-174dBm/Hz	Noise Floor
Rx Noise Floor BW	86.8dBHz	83.0dB	80.4dB	= 10 log (Infomation Rate)
Rx NF	7.1dB	7.1dB	7.1dB	Noise Figure (per Spec)
Rx Noise Floor	-80.1dBm	-83.9dBm	-86.5dBm	= Noise Floor + Rx Noise Floor BW + Rx NF
Eb/No	4.9dB	4.7dB	4.0dB	Required Energy/Bit : NPSD
Implementation Loss	2.5dB	2.5dB	2.5dB	Connectors & Filter loss
Required Eb/No	7.4dB	7.2dB	6.5dB	= Eb/No + Implementation Loss
Receiver Sensitivity	-72.7dBm	-76.7dBm	-80.0dBm	= Rx Noise Floor + Eb/No + Imp Loss = Minimum Sensitivity
Spec Requirement	-70.4dBm	-74.4dBm	-77.8dBm	Minimum WiMedia Receiver Sensitivity Spec

Table 5: UWB Link Budget; Band Group 1
(Source: ITI Scotland; UWB Raptor Specification 3.0 [72]**)**

frequency, however a significant increase in receiver Noise Figure (NF) of over 9dB dominates. This increase was a combination of device noise in the input amplifier plus a reduction in drive signal into the front end mixer stages due to loading within the silicon device.

UWB Link Budget - Standard Compliant Rates Calculated in 528MHz Bandwidth				Notes
Info Rate	480Mbps	200Mbps	110Mbps	Defined by WiMedia Spec
Frequency	10018 MHz	10018 MHz	10018 MHz	Band Group 1 Centre Frequency
TxPower	-41.3dBm/MHz	-41.3dBm/MHz	-41.3dBm/MHz	Defined by FCC / WiMedia Spec
Total Bandwidth (528MHz)	27.2dB	27.2dB	27.2dB	Adjusting for Channel Bandwidth (528MHz)
Averaging (over 3 bands)	4.8dB	4.8dB	4.8dB	Benefit through TFC technique (WiMedia Standard)
Tx Antenna Gain	0.0 dBi	0.0 dBi	0.0 dBi	Default / worst case
EIRP	-9.3dBm	-9.3dBm	-9.3dBm	= -41.3 + 27.2 + 4.8 = maximum Radiated Power
Range	3.2m	5.1m	7.4m	Iterated until EIRP + Mean Path Loss = Receiver Sensitivity
Mean Path Loss	-54.4dB	-58.3dB	-61.6dB	Free Space Path Loss = 10 log ((4 π d / λ) ^2)
Receive Antenna Gain	0.0dBi	0.0dBi	0.0dBi	Default / Worst Case
Shadowing/Fading Margin	0.0dB	0.0dB	0.0dB	0.0dB
Min Rx Signal Level	-63.6dBm	-67.6dBm	-70.9dBm	= EIRP + Path Loss = Received Signal
NPSD	-174dBm/Hz	-174dBm/Hz	-174dBm/Hz	Noise Floor
Rx Noise Floor BW	86.8dBHz	83.0dB	80.4dB	= 10 log (Infomation Rate)
Rx NF	16.2dB	16.2dB	16.2dB	Noise Figure (per Spec)
Rx Noise Floor	-71.0dBm	-74.8dBm	-77.4dBm	= Noise Floor + Rx Noise Floor BW + Rx NF
Eb/No	4.9dB	4.7dB	4.0dB	Required Energy/Bit : NPSD
Implementation Loss	2.5dB	2.5dB	2.5dB	Connectors & Filter loss
Required Eb/No	7.4dB	7.2dB	6.5dB	= Eb/No + Implementation Loss
Receiver Sensitivity	-63.6dBm	-67.6dBm	-70.9dBm	= Rx Noise Floor + Eb/No + Imp Loss = Minimum Sensitivity
Spec Requirement	-68.4dBm	-72.4dBm	-75.8dBm	Minimum WiMedia Receiver Sensitivity Spec

Table 6: UWB Link Budget; Band Group 5
(Source: ITI Scotland; UWB Raptor Implementation Specification 3.0 [72]**)**

The Device Architecture and Implementation

The implementation of an RF front end in standard RF CMOS presents significant challenges to any design team; the implementation of an RF front end capable of delivering performance up to 10.6GHz brings new and additional problems. Prior to this development, most of the high performance competitive RF designs being developed for UWB and other, more esoteric applications used expensive process technologies such as GaAs or BiFET to realise the high speed, high frequency functions. However, these processes are not suitable or cost competitive for mass market applications; this can only be achieved on CMOS. After evaluating the foundry process suppliers available, it was decided to work with IBM's 90nm CMOS process with RF option which provided greater characterisation of analogue transistors and capacitors. A small selection of critical blocks were designed and fabricated on this process to compare simulation versus actual silicon results; these were used to modify the modelling parameters of the actual device.

Figure 34 shows the entirety of the device as implemented and fabricated on silicon. The complete device consisted of 3 main blocks; Receive chain, Transmit chain, and PLL / Local Oscillator. The Analog / RF digital interface logic

consisting of the interface to a third party baseband controller was relatively straightforward. Examining the diagram, it is significant to note the design approach adopted differential signal paths throughout the interior of the device in an attempt to maintain signal integrity in the main analogue paths. Using balanced, differential signals also had the benefit of minimising the cross-chip interference which is problematic at these frequencies.

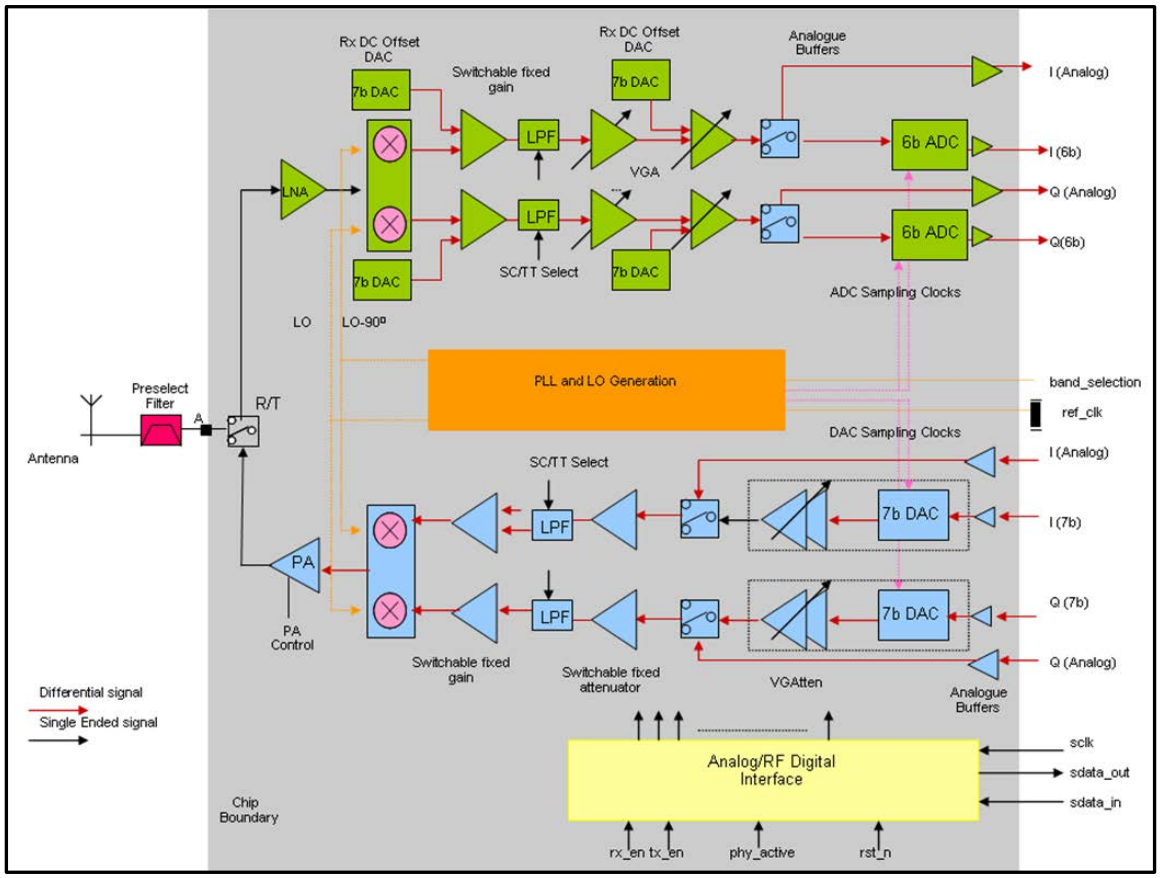

Figure 34: UWB RF Front End Block Architecture
(Source: ITI Scotland; UWB Raptor Specification 3.0 [72]**)**

The development of this UWB RF front end CMOS silicon solution was probably the most challenging piece of hardware development undertaken by the author. The responsibility of the author was to lead the project team through the design of a realisable system analysis, incorporating advanced features such as those described in submission XI, through a complex and challenging silicon design process, and into a final working silicon sample. At the time of this development, no-one had integrated a device of such technical complexity on CMOS at 10GHz. During evaluation of the silicon, the device was functional in Band groups 1 and 2, however it became apparent that the performance of Band Group 5 was worse than predicted due to cross chip losses at 7-8GHz.

UWB Antenna

As part of the UWB development programme it became apparent that there were limited UWB antenna available for incorporation into commercial products. This situation was particularly apparent in the higher band groups (>6GHz) so a development activity was funded to deliver a passive, low cost antenna suitable for integration into consumer equipment (TVs and Video players) capable of transmitting HDTV across a room. In order to ensure economic viability of the antenna, it was decided to use standard FR4 printed circuit board (PCB) material (1.6mm) rather than the lower loss materials such as Rogers 60. In addition to a material constraint, a physical constraint of 2.5 cm^3 was defined as a practical size suitable for integration into products. The electrical performance of the antenna was most critical and both the return loss (>10dB) and radiation efficiency (>70%) would be the criteria for determining the best antenna. As the antenna was to operate with the previously discussed UWB RF front end, it must be capable of operating in both transmit and receive modes.

After a literature review, the slotted bowtie structure was adopted as the most suitable candidate for optimisation. In particular it was simple to integrate with other electronic components and consumer equipment companies understood how to work with such material. The original slotted bowtie structure functioned adequately but matching to the RF circuitry required an additional strip-line feeder along with slight modifications to the geometry to optimise the return loss and radiation pattern.

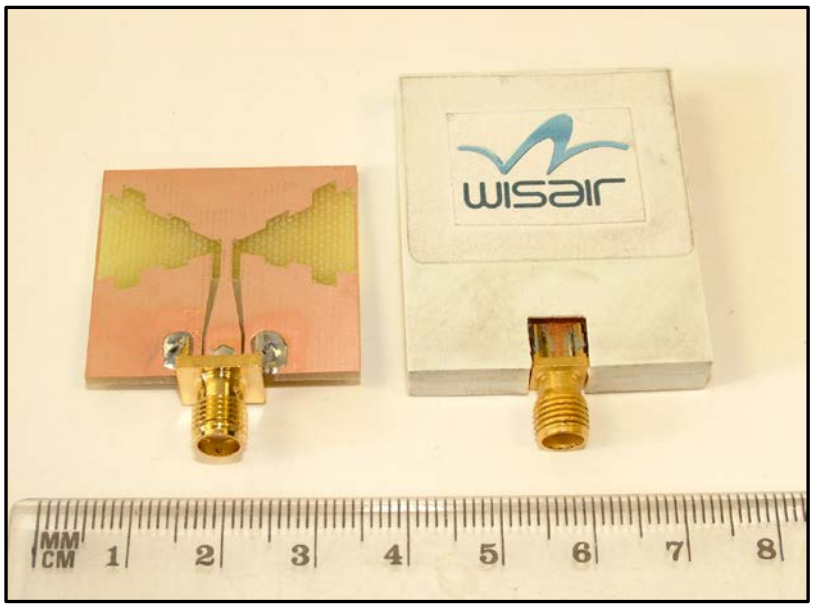

Figure 35: UWB (left) compared with competitor antenna (right) (Source: ITI Scotland; Passive Antenna Design [77]**)**

Using CST Microwave Studio, the design was optimised which resulted in an overall S11 response considerably better than the best available competitive antenna from Wisair, Figure 35, Figure 36. Further simulation versus actual performance was performed across the band and the azimuthal gain plots (antenna connector pointing vertical) are shown in Figure 37,Figure 38, Figure 39 indicating that the actual antenna performed very similar to the simulation confirming the accuracy of the modelling.

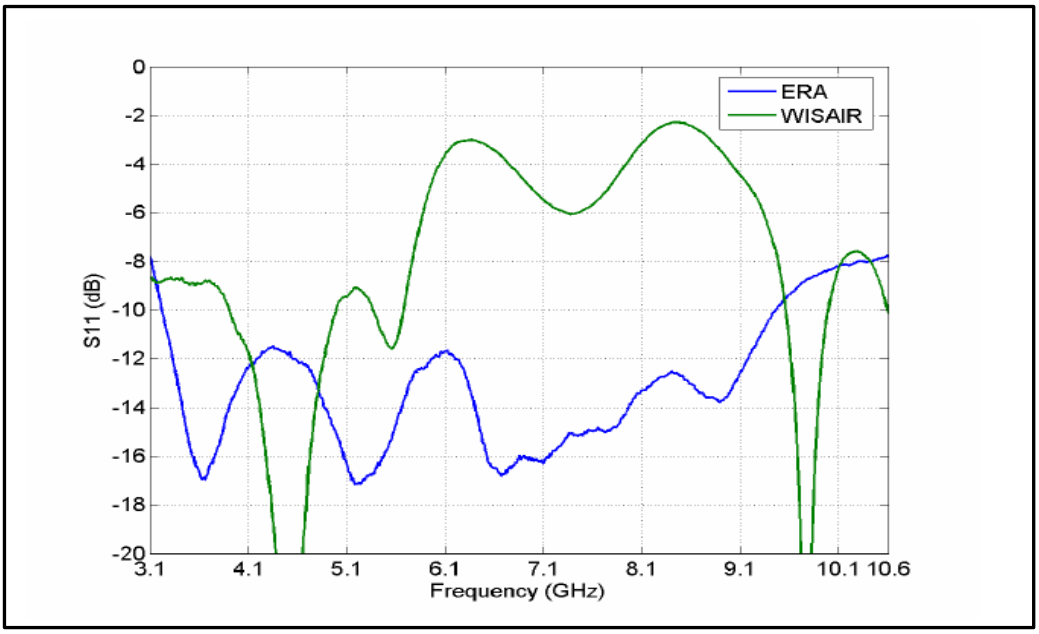

Figure 36: UWB (ERA) Antenna Design versus Wisair Antenna (Source: ITI Scotland; Passive Antenna Design [77]**)**

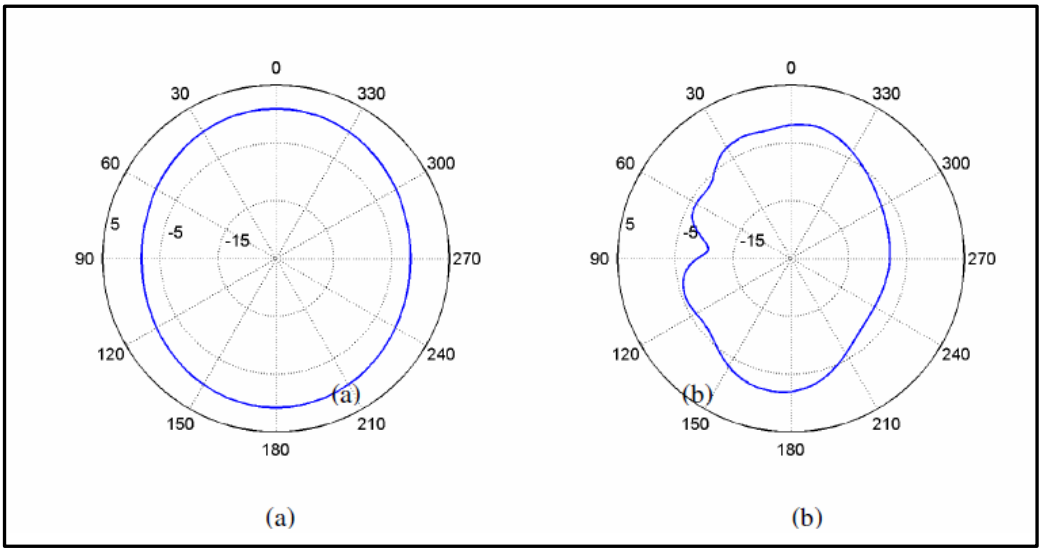

Figure 37: Azimuth 3.1GHz a. Predicted b. Measured (Source: ITI Scotland; Passive Antenna Design [77]**)**

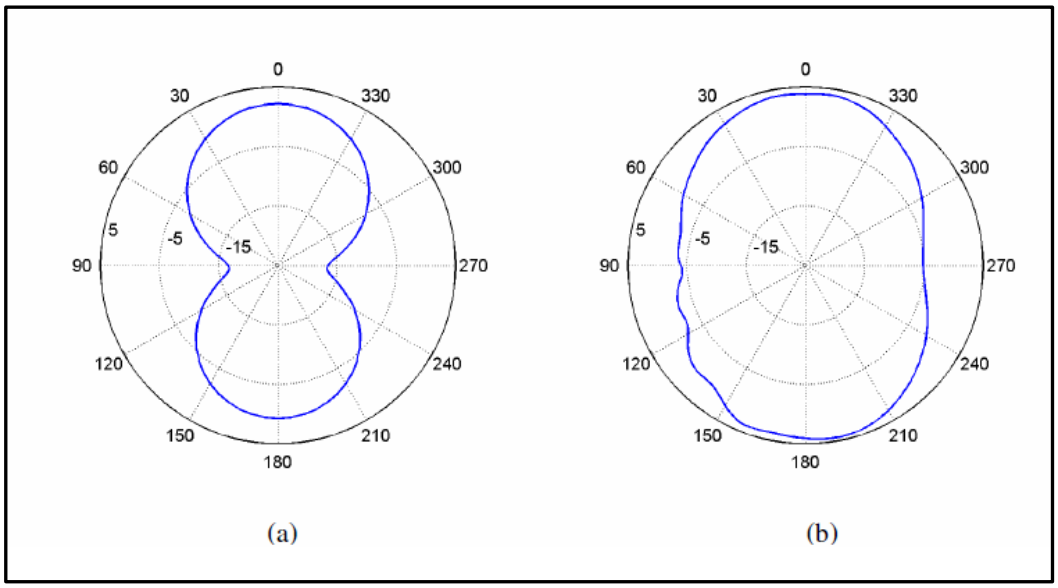

Figure 38: Azimuth 6.86GHz a. Predicted b. Measured
Source: ITI Scotland; Passive Antenna Design [77]

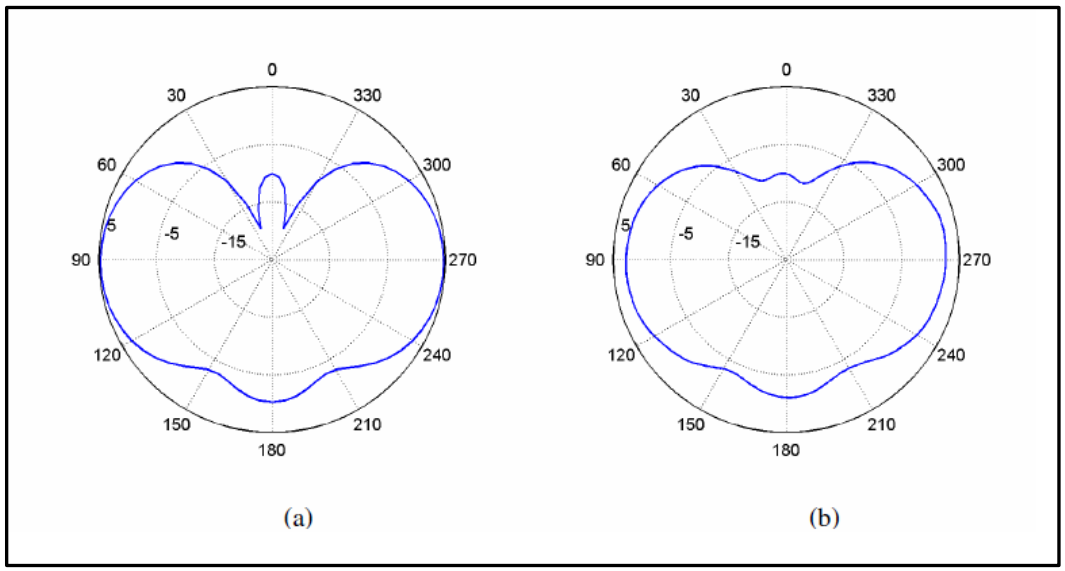

Figure 39: Azimuth 10.6GHz a. Predicted b. Measured
Source: ITI Scotland; Passive Antenna Design [77]

The completed passive antenna performed well and when measured in a practical UWB deployment scenario was praised for its performance.

Submission XI Patent No. GB 2,433,681

Title: Communication System and Method

Inventors: **Duncan J Bremner**, Lochwinnoch, Scotland;
Fraser Murray Edwards, Cambridge, England

Assignee: ITI (Scotland) Ltd, Scotland

Filed: Dec 21, 2005

In 2002 a group of device and equipment suppliers formed the WiMedia Alliance to create a set of standards and specifications for an emerging communications technology known as Ultra WideBand (UWB) wireless. The operating band for UWB lay between 3.1GHz and 10.6GHz, with a maximum power level of -41 dBm /MHz. During the system design phase of developing a UWB system to realise a Wireless front end, system analysis of the band and group structure suggested that it was possible to realise an extremely high bandwidth connection over a short distance while operating within the restrictions of the standard. submission XI details an innovation capable of providing a wireless connection up to ~2700Mbps over a spectrum of 1584MHz (3 bands; 1 group). The patent protects the system level innovation to use such a very high speed connection for the transfer of large amounts of data such as DVD or video files onto a portable device such as an iPod or portable storage unit in a very short period of time (less than 1 minute). At a system level, as long as the radio power between the transmitter and receiver is controlled or shielded, this system can operate alongside other devices without causing interference. Most importantly, the actual realisation of this innovation requires very minor modification to the electronic circuitry during the design phase to incorporate this feature enabling a device to be managed under software control to select between high speed and standard mode using the same circuitry.

This invention was jointly made by Bremner & Edwards during the system design phase of the UWB development project discussed earlier. This work continues to be relevant as illustrated by US patent application US 2012 202 426 by Henderson & Grossi from the NCR Corporation for use in the 60GHz standard [76]. It has also been cited by Hodges and Butler in their US 2013 082 818 application on behalf of Microsoft Corporation.

Submission XII Patent No. GB 2,448,541

Title: Ultra Wideband Antenna

Inventors: **Duncan J Bremner**, Lochwinnoch, Scotland;
Mark Norris, Cambridge, England
Dean Kemp, Leatherhead, England

Assignee: ITI (Scotland) Ltd, Scotland

Filed: Apr 20, 2007

The development of a UWB system architecture required the development of supporting system components such as an antenna suitable for use over the full band of UWB transmissions 7.5GHz wide. Although antenna capable of operation up to and beyond the maximum frequency of 10GHz (X-band) were commercially available, there were no antenna available capable of operating over the full band or appropriate for portable applications.

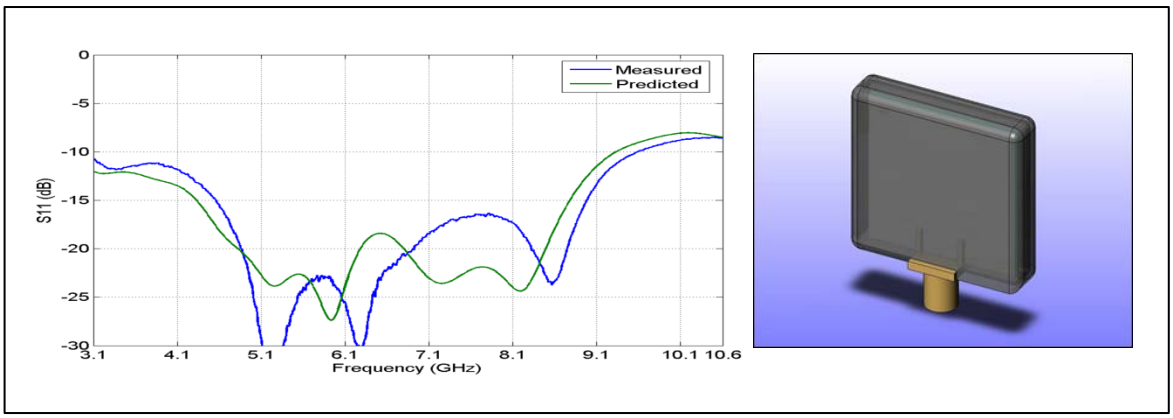

Figure 40: Passive UWB Antenna Performance (Source: Measurement Results) [77]

The solution developed and described in the submission consisted of single sided copper pattern on standard FR4 fibre-glass board which had a return loss better than 10dB and a radiation efficiency of over 75% across the majority of the band as shown in the results in Figure 40. This resulted in a full band antenna that had useful gain over the whole band resulting in improved range of the complete UWB system. Samples of this antenna were tested in an independent test facility and the results were very positive. Although the details remain confidential, the conclusion of the testing house was *'This is the best UWB antenna we have tested to date'*.

This invention was contributed to jointly by Bremner, Norris, and Kemp. Bremner was also the project lead on this work. Since the grant of this patent in

2010, the work has been cited 3 times, all by General Motors in association with antennae suitable for automotive applications, as can be found in patent US 8,686,906.

Concluding remarks

The 12 submissions presented here represent one individual's contribution to the field of communications from approximately 1985 until 2010; a period of 25 years. However, on a macro scale, this same period represented the modernisation (via digitisation) of the communications network, the rise and fall of ISDN as a customer premise technology, and the birth and growth of mass adoption of the internet, first through modem technology, then via ADSL solutions[18] . The last 2 submissions examine the challenges of wireless technology and one possible alternative to the already congested 802.11 bands with a protocol developed by the WiMedia Alliance that would deliver the equivalent of packet and connection based protocols over the same air interface, delivering the guaranteed QoS of connection based with the efficiency of packet based approaches in a single system. In the event, due to market failure of the UWB technology, the next generation Media Access Controller (MAC) defined by the WiMedia Alliance would not be deployed. However, the emergence of 60GHz communications technology has resurrected the UWB MAC specification within ECMA-367 [76] illustrating that although the intended market failed commercially, the technical effort expended on producing an improved solution was re-born in a new specification.

[18] Although there are no publically recorded references, the author undertook several design studies into subscriber line circuits capable of delivering standard voice communications and ADSL over the same Subscriber Interface Circuit.

The Published Work

Submission I

Type	Reference	Title
Patent	US 5598467	Signal Interface Circuit with Selectable Signal Interface Parameters
Citations	**5**	

US005598467A

United States Patent [19]

Bremner et al.

[11] **Patent Number: 5,598,467**

[45] **Date of Patent: Jan. 28, 1997**

[54] **SIGNAL INTERFACE CIRCUIT WITH SELECTABLE SIGNAL INTERFACE PARAMETERS**

[75] Inventors: **Duncan J. Bremner**, Lochwinnoch; **Roger K. Benton**, Edinburgh, both of Scotland; **James B. Wieser**, Pleasanton, Calif.

[73] Assignee: **National Semiconductor Corporation**, Santa Clara, Calif.

[21] Appl. No.: **353,095**

[22] Filed: **Dec. 9, 1994**

[51] **Int. Cl.**[6] **H04M 1/76**

[52] **U.S. Cl.** **379/398**; 379/399; 379/402

[58] **Field of Search** 379/398, 399, 379/406, 402, 412, 403

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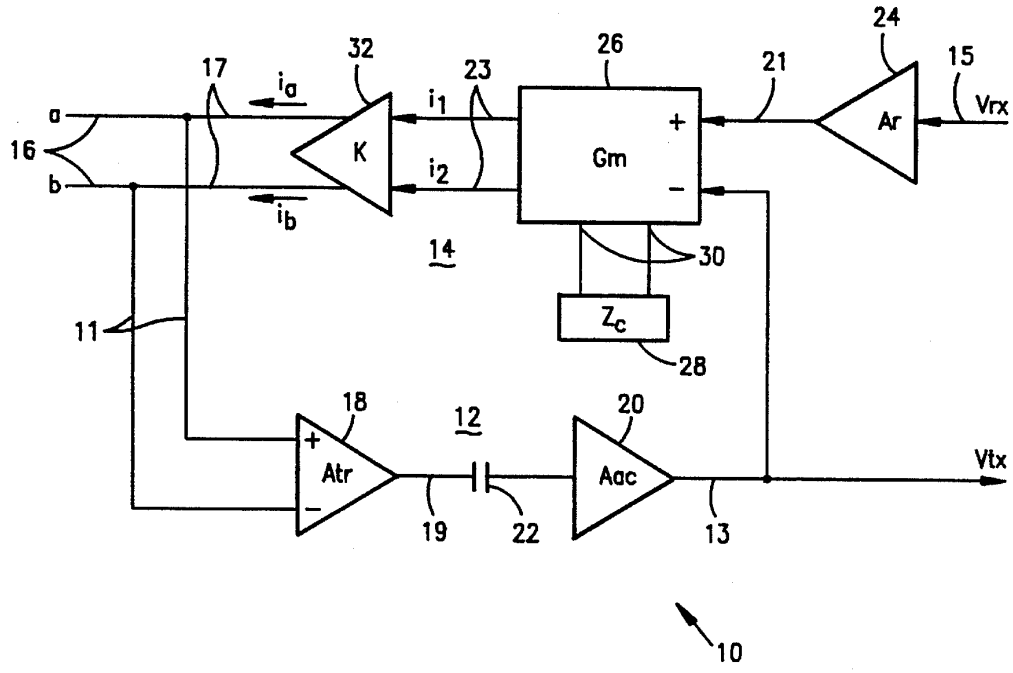
Primary Examiner—Krista M. Zele
Assistant Examiner—Jacques M. Saint-Surin
Attorney, Agent, or Firm—Limbach & Limbach L.L.P.

[57] **ABSTRACT**

A signal interface circuit with selectable signal interface parameters for a telephone subscriber line includes an impedance circuit having a selectable impedance value, signal terminals having an associated, definable termination impedance, a transmitter circuit having a definable transmitter transfer function and a receiver circuit having a definable receiver transfer function. The signal terminals connect to an external signal line pair having an associated line impedance for conducting outgoing and incoming signals therefrom and thereto, respectively. The transmitter circuit receives the outgoing signal from the signal terminals and provides a transmit signal in accordance with its transmitter transfer function. The receiver circuit, which includes a differential transconductance amplifier, receives an input signal and the transmit signal and provides the incoming signal to the signal terminals in accordance with its receiver transfer function. The termination impedance, transmitter transfer function and receiver transfer function are all defined by the selectable impedance, with the termination impedance defined to match the line impedance.

29 Claims, 9 Drawing Sheets



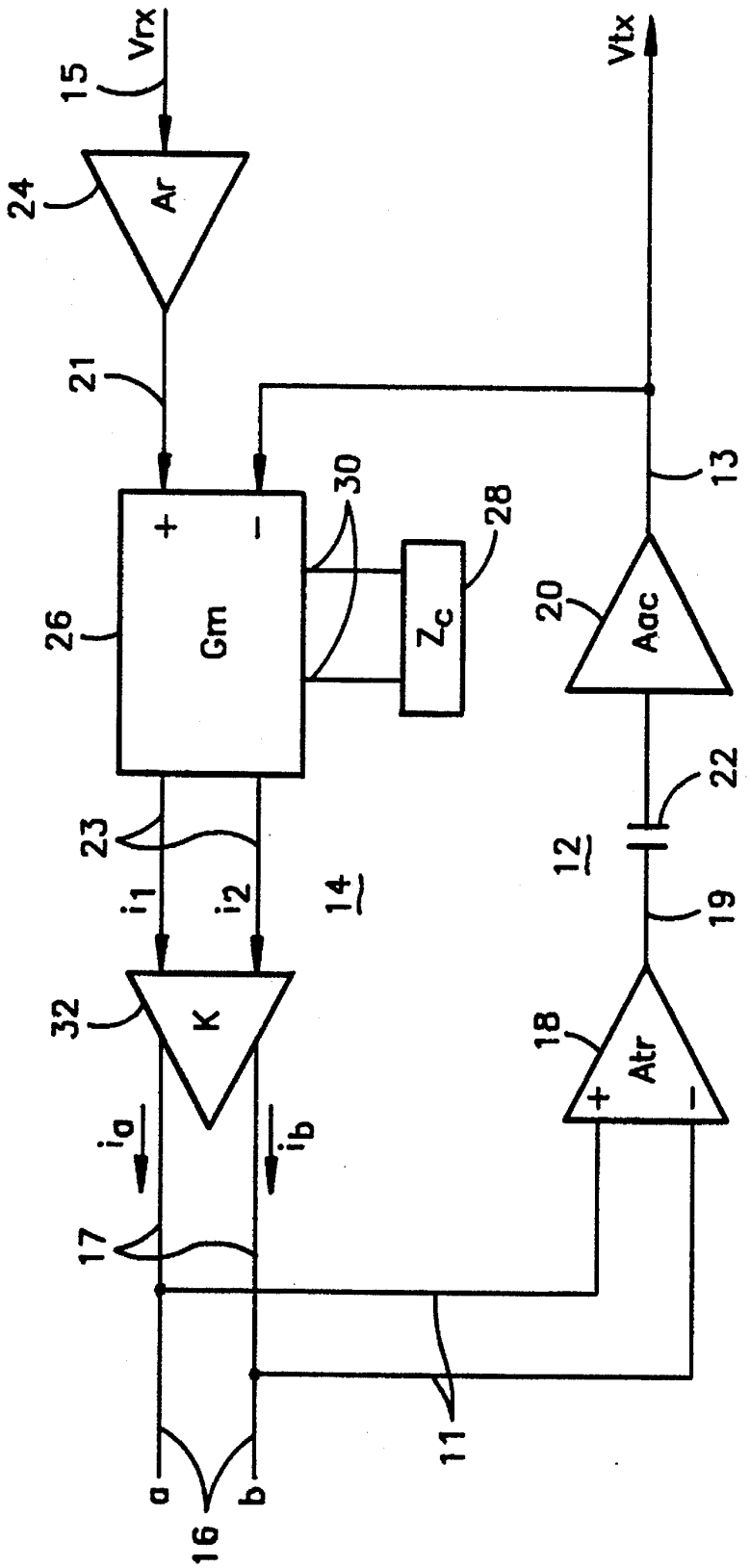

Vrx
15
24
Ar
21
Vtx
13
10
30
28
+
−
26
Gm
Z_c
20
Aac
22
23
12
i_1
i_2
14
19
32
K
18
Atr
+
−
i_a
i_b
17
11
a
b
16

FIG. 1

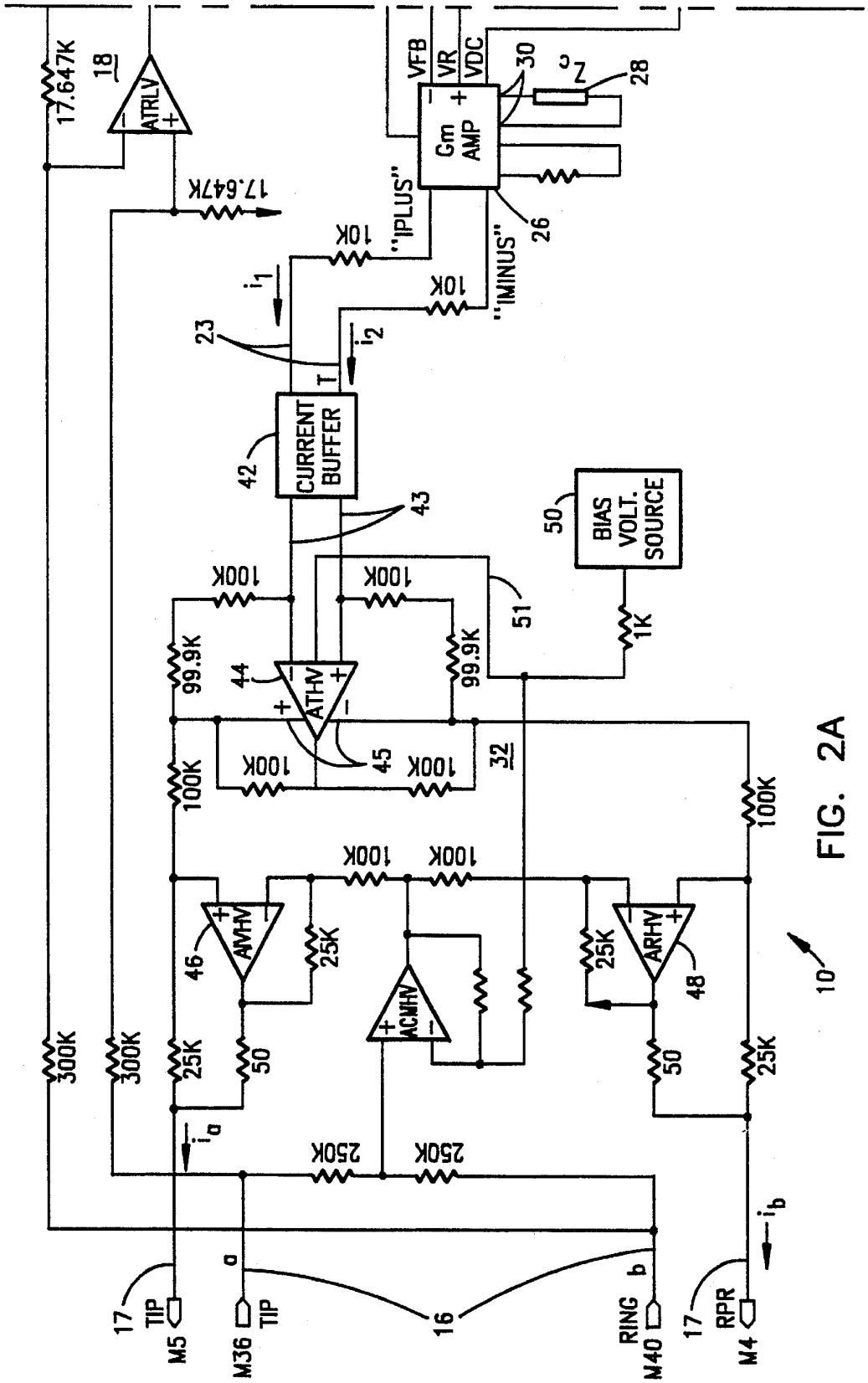

17.647K
18
ATRLV
VFB
VR
VDC
30
Z
28
Gm AMP
"IPLUS"
"IMINUS"
26
10K
10K
i_1
i_2
23
T
CURRENT BUFFER
42
43
50
BIAS VOLT. SOURCE
1K
51
100K
99.9K
44
ATHV
45
32
AMHV
ACMHV
ARHV
46
48
25K
50
300K
i_a
i_b
250K
17
TIP
M5
M36
TIP
a
16
RING
b
M40
RPR
M4
10

FIG. 2A

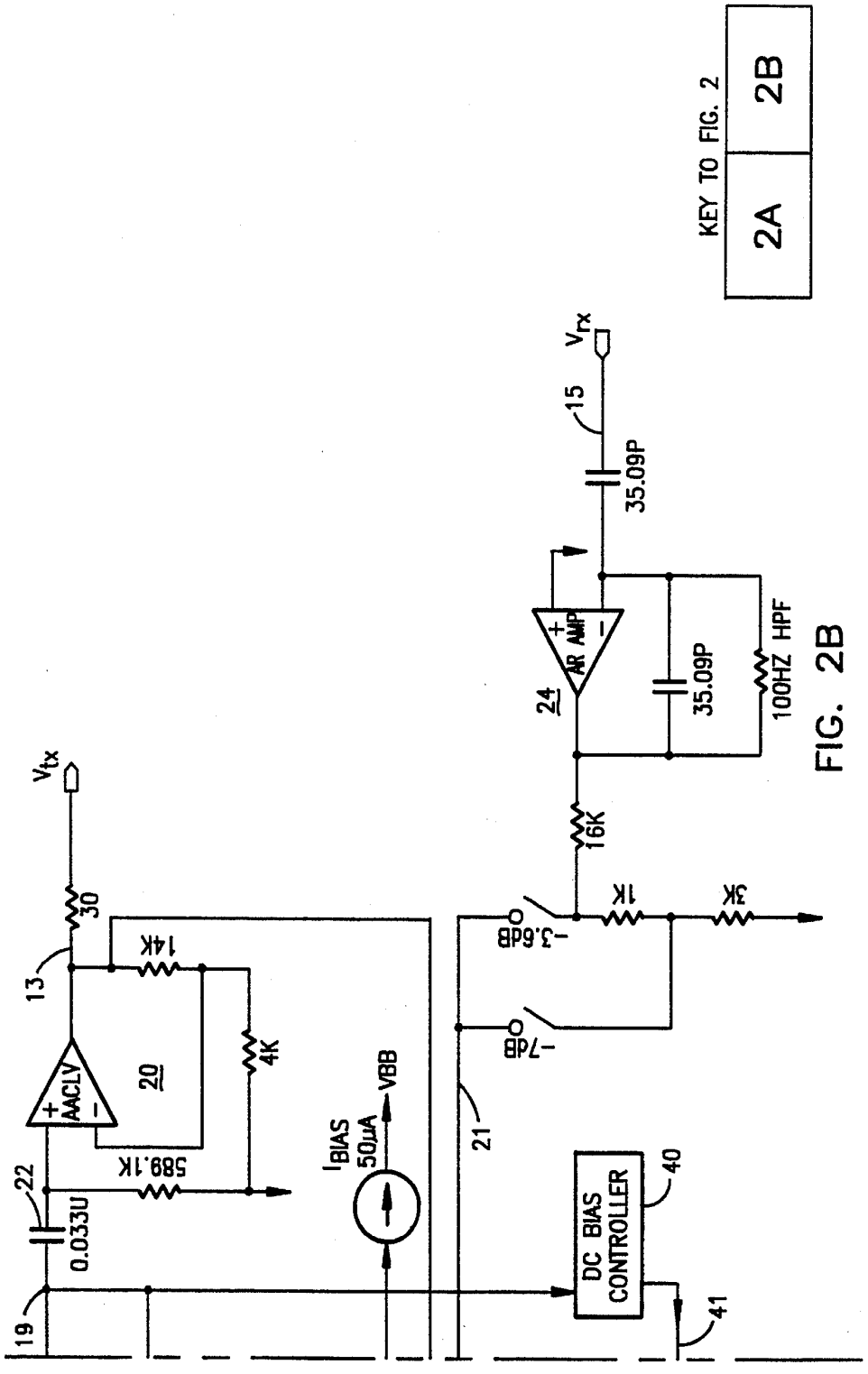

KEY TO FIG. 2
2A
2B
V_{rx}
15
35.09P
24
AR AMP
35.09P
100HZ HPF
16K
1K
3K
-3.6dB
-7dB
V_{tx}
30
14K
13
AACLV
20
4K
589.1K
22
0.033U
19
I_{BIAS}
50μA
VBB
21
DC BIAS CONTROLLER
40
41

FIG. 2B

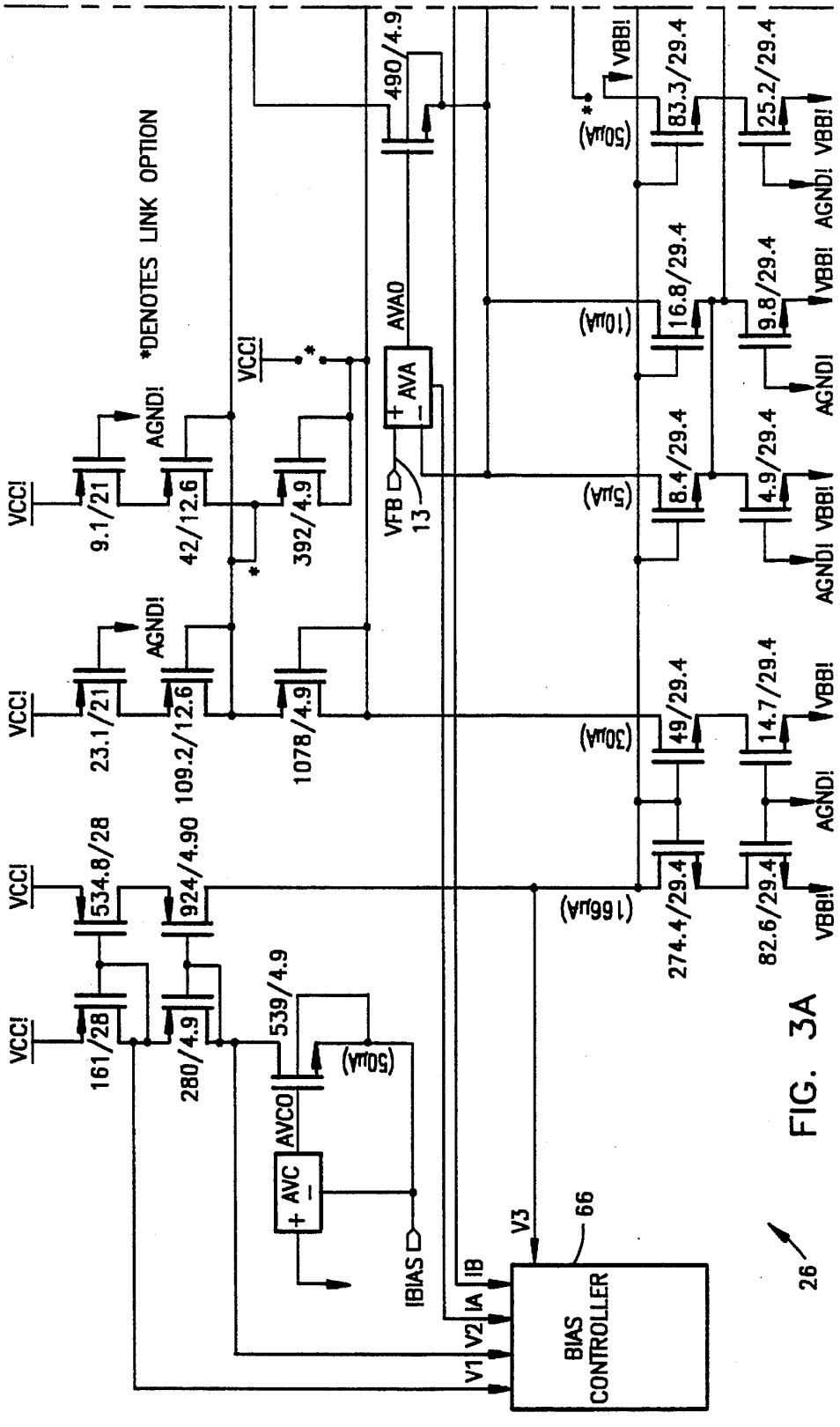

*DENOTES LINK OPTION
VCC!
AGND!
VBB!
9.1/21
42/12.6
392/4.9
490/4.9
AVAO
AVA
VFB
13
23.1/21
109.2/12.6
1078/4.9
534.8/28
924/4.90
161/28
280/4.9
539/4.9
AVCO
AVC
IBIAS
V1
V2
V3
IA
IB
BIAS CONTROLLER
66
26
83.3/29.4
25.2/29.4
16.8/29.4
9.8/29.4
8.4/29.4
4.9/29.4
49/29.4
14.7/29.4
274.4/29.4
82.6/29.4
50μA
10μA
5μA
30μA
166μA

FIG. 3A

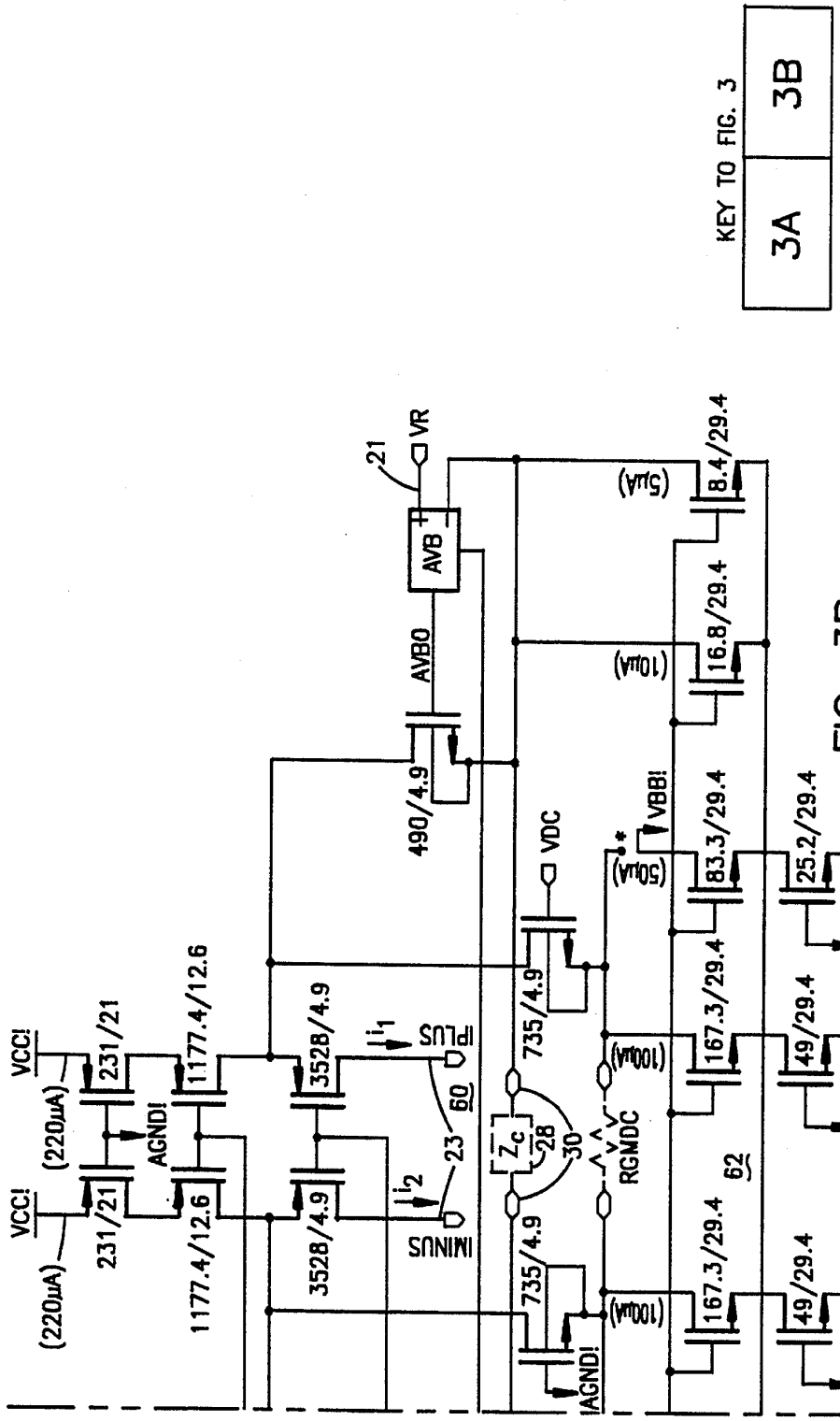

KEY TO FIG. 3
3A
3B
VCC!
(220μA)
231/21
AGND!
1177.4/12.6
3528/4.9
i1
i2
PLUS
MINUS
60
23
21
VR
AVB
AVBO
490/4.9
VDC
735/4.9
Zc
28
30
RGNDC
62
!AGND!
(5μA)
8.4/29.4
(10μA)
16.8/29.4
VBB!
(50μA)
83.3/29.4
25.2/29.4
(100μA)
167.3/29.4
49/29.4
AGND!

FIG. 3B

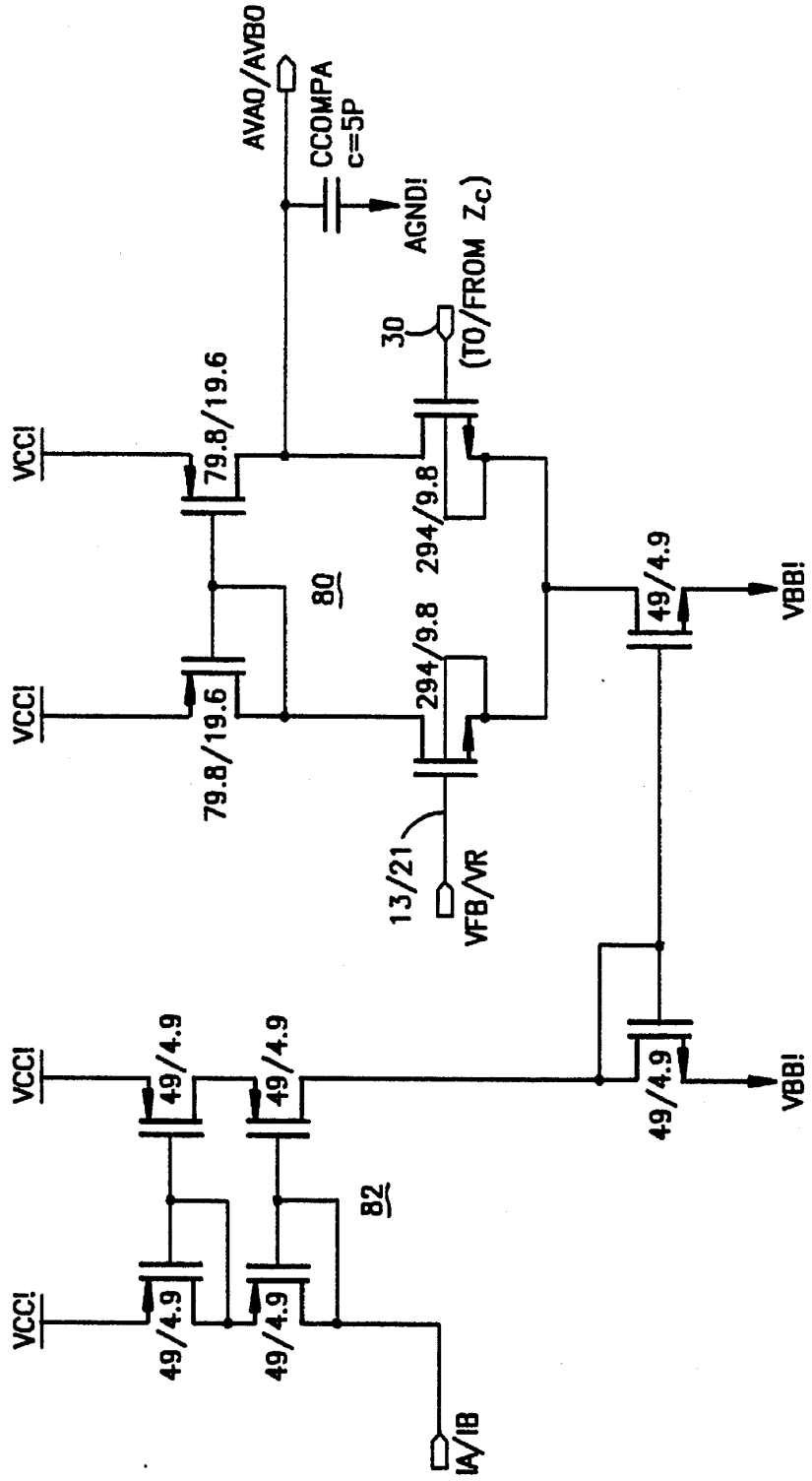

AVA0/AVB0
CCOMPA
c=5P
AGND!
30
(TO/FROM Zc)
VCC!
79.8/19.6
294/9.8
80
49/4.9
VBB!
13/21
VFB/VR
82
IA/IB
AVA/AVB

FIG. 4

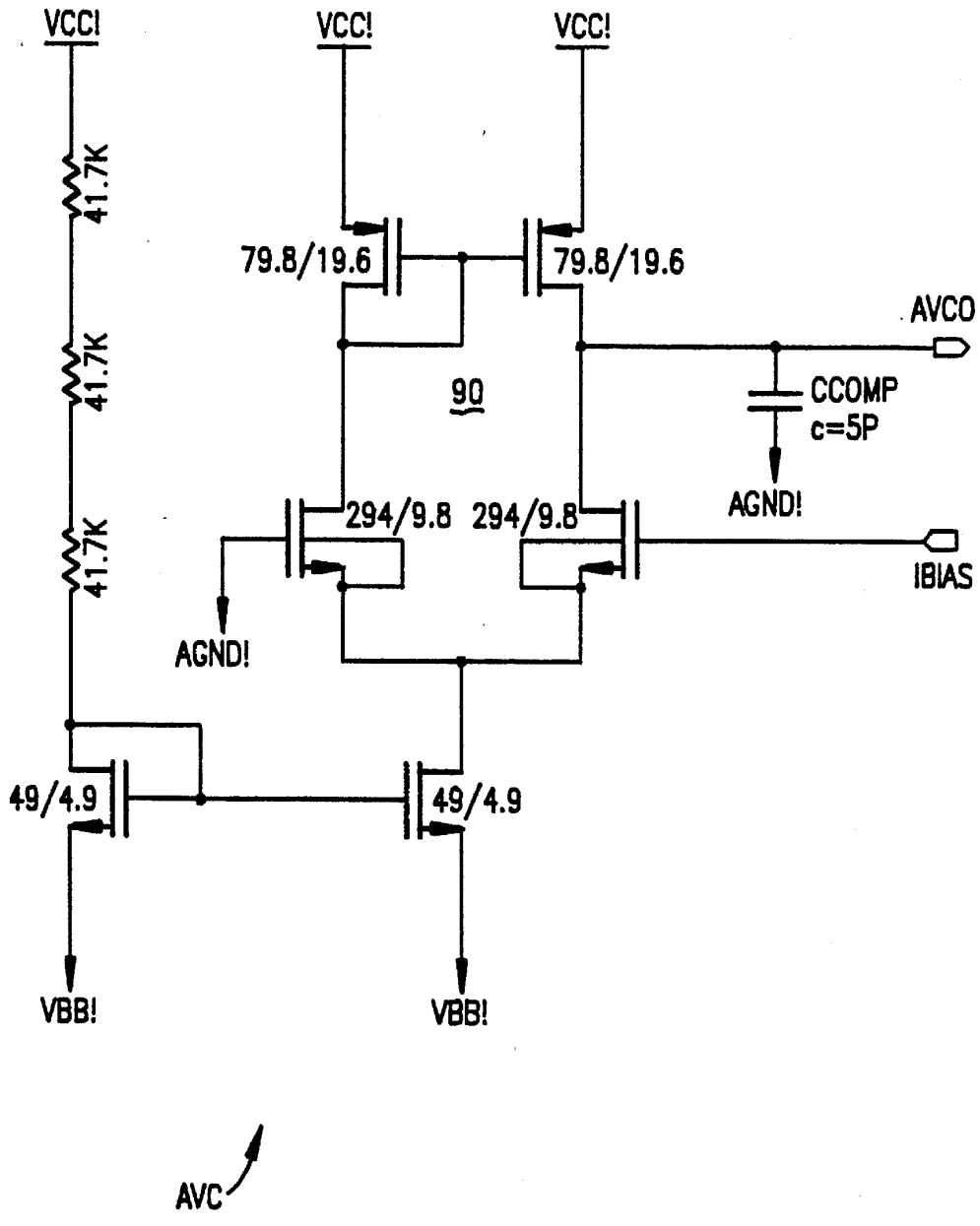

VCC!
VCC!
VCC!
41.7K
41.7K
41.7K
79.8/19.6
79.8/19.6
AVCO
90
CCOMP
c=5P
AGND!
294/9.8
294/9.8
IBIAS
AGND!
49/4.9
49/4.9
VBB!
VBB!
AVC

FIG. 5

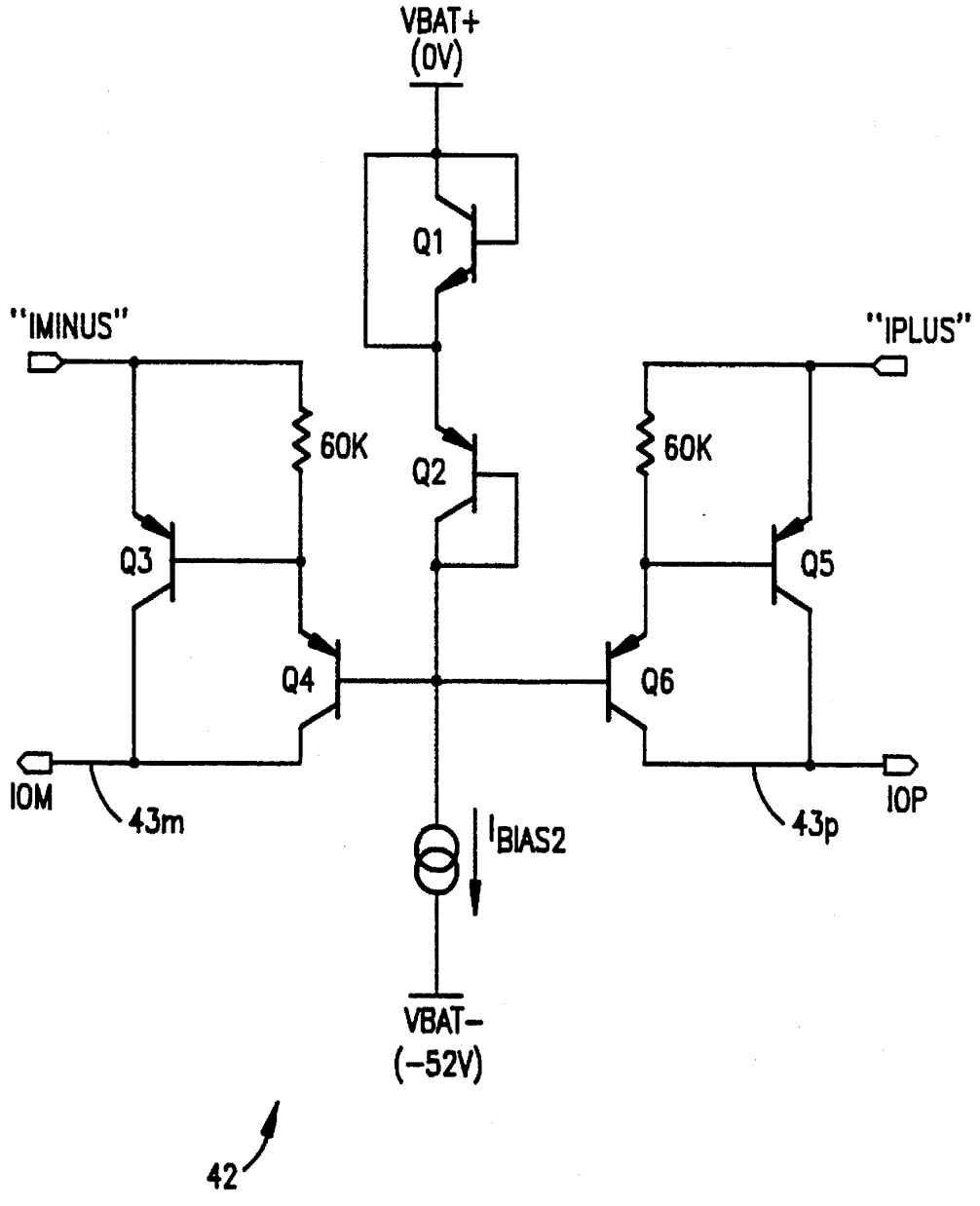

VBAT+
(0V)
Q1
"IMINUS"
"IPLUS"
60K
Q2
60K
Q3
Q5
Q4
Q6
IOM
43m
43p
IOP
I_{BIAS2}
VBAT-
(-52V)
42

FIG. 6

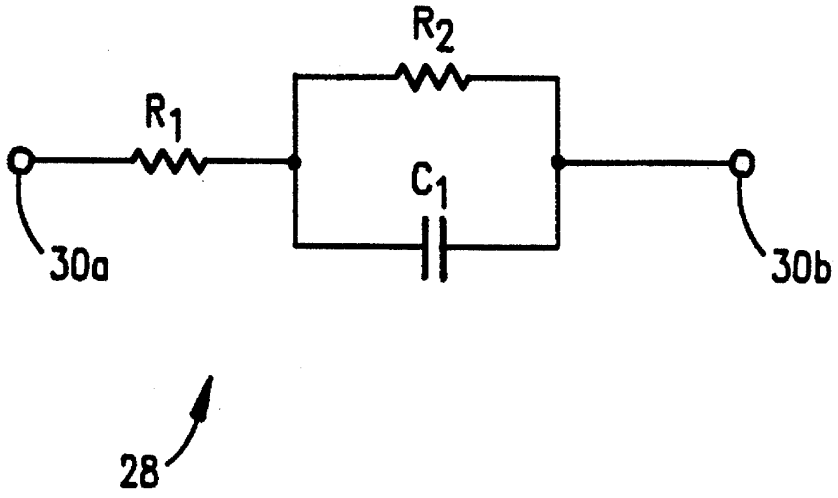


FIG. 7

SIGNAL INTERFACE CIRCUIT WITH SELECTABLE SIGNAL INTERFACE PARAMETERS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to signal interface circuits, and in particular, to signal interface circuits in which specific circuit parameters and performance characteristics, such as signal gain and terminal impedance, can be selectively controlled.

2. Description of the Related Art

Conventional signal interface circuits exist in many forms and configurations for performing many different functions. One function often performed by such circuits is that of impedance matching whereby two circuits or systems having different impedances can be interconnected so as to provide for maximum power transfer or signal gain. However, due to the inherent frequency dependency of all impedances, the impedance matching, power transfer and signal gain characteristics are dependent upon the frequencies of the signals being conveyed by such interface circuits and can, therefore, vary significantly. Further, attempts to optimize these performance parameters, i.e. establishing and maintaining the desired frequency response characteristics for these performance parameters, can be quite difficult since adjustment of one will generally affect the others as well.

This problem becomes further complicated when the interface circuit must pass signals in two directions. For example, the interface circuit may be required to provide impedance matching and signal gain adjustment simultaneously for transmit and receive circuits which are connected to and must send bidirectional signals through a shared signal node. One example of a circuit requiring such two-way impedance matching and frequency compensation is a subscriber line interface circuit used in telecommunications. Such an interface circuit must provide a complex impedance termination and matching transmit and receive frequency response characteristics to the subscriber line which is attached at the "tip" and "ring" terminals and which itself has a complex impedance associated therewith.

In conventional interface circuits of this type, optimization or adjustment of multiple performance parameters is typically done by providing for the adjustment or design of circuit components or groups Of circuit components which correspond to each individual performance parameter. For example, one set of circuit components would be designed or adjusted to provide for a desired complex impedance termination, while other circuit components would be designed or adjusted to provide for the desired transmit or receive signal frequency responses. Accordingly, matching all three performance parameters can be quite difficult.

This problem of matching multiple performance parameters is further exacerbated when manufacturing tolerances, temperature and other effects are taken into consideration. The circuit component or components designed or adjusted to provide these desired performance parameters must often be matched to one another and will have multiple parameter "bandwidths", i.e. a "bandwidth" associated with each operating parameter such as temperature, etc. Therefore, not only must each performance parameter be matched, but they must remain matched as various operating parameters, such as temperature, vary.

Accordingly, it would be desirable to have a signal interface circuit with selectable signal interface parameters which simplify the providing and maintaining of desired impedance and signal frequency response characteristics.

SUMMARY OF THE INVENTION

An apparatus including a signal interface circuit with selectable signal interface parameters in accordance with one embodiment of the present invention includes an impedance terminal, a pair of signal terminals, a transmitter circuit and a receiver circuit. The impedance terminal is for coupling to an impedance circuit having an associated, selectable impedance value. The pair of signal terminals has an associated, definable termination impedance which is defined in accordance with the selectable impedance value, and is for coupling to an external signal line pair having an associated line impedance for conducting outgoing and incoming signals therefrom and thereto, respectively. The transmitter circuit is coupled to the pair of signal terminals, has an associated, definable transmitter transfer function which is defined in accordance with the selectable impedance value and is for receiving the outgoing signal and providing a transmit signal in accordance with the definable transmitter transfer function. The receiver circuit is coupled to the impedance terminal, the pair of signal terminals and the transmitter circuit, has an associated, definable receiver transfer function which is defined in accordance with the selectable impedance value and is for receiving an input signal and the transmit signal and providing the incoming signal in accordance with the definable receiver transfer function.

A method of providing a signal interface with selectable signal interface parameters in accordance with another embodiment of the present invention includes the steps of: defining a termination impedance in accordance with a selectable impedance value; defining a transmitter transfer function in accordance with the selectable impedance value; defining a receiver transfer function in accordance with the selectable impedance value; coupling to a signal line pair having an associated line impedance with a pair of signal terminals having the defined termination impedance associated therewith; conducting an outgoing signal from the signal line pair via the pair of signal terminals; amplifying the outgoing signal and providing a transmit signal in accordance with the defined transmitter transfer function; receiving an input signal and the transmit signal and providing an incoming signal in accordance with the defined receiver transfer function; and conducting the incoming signal to the signal line pair via the pair of signal terminals,

These and other features and advantages of the present invention will be understood upon consideration of the following detailed description of the invention and the accompanying drawings,

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a functional block diagram of the small ac signal equivalent circuit for a signal line interface circuit with selectable signal interface parameters in accordance with one embodiment of the present invention.

FIG. **2** is a schematic diagram of one embodiment of the signal interface circuit of FIG. **1**.

FIG. **3** is a schematic diagram of one embodiment of the transconductance amplifier of FIG. **2**.

FIG. **4** is a schematic diagram of the differential input amplifiers of FIG. **3**.

FIG. **5** is a schematic diagram of the bias driver of FIG. **3**.

FIG. **6** is a schematic diagram of the current buffer of FIG. **2**.

FIG. **7** is a schematic diagram of one embodiment of the selectable impedance circuit of FIG. **1**.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. **1**, a signal interface circuit **10** with selectable signal interface parameters in accordance with one embodiment of the present invention includes a transmitter circuit **12** and a receiver circuit **14** connected to an external signal line pair **16** (e.g. the "tip" and "ring" terminals of a telephone subscriber line). The transmitter circuit **12** includes a differential voltage amplifier **18** having a transfer function A_{tr} and a buffer amplifier **20** having a transfer function A_{ac} capacitively coupled by a capacitor **22**. The receiver circuit **14** includes a buffer amplifier **24** having a transfer function A_r, a differential transconductance amplifier **26** having a transconductance G_m, an impedance circuit **28** having a selectable impedance Z_c (connected via impedance terminals **30** to the transconductance amplifier **26**) and a differential current amplifier **32** having a transfer function K. (The "transfer functions" discussed herein are intended to refer to the small ac signal components of the subject transfer functions.)

The differential amplifier **18** of the transmitter circuit **12** receives an outgoing signal **11** from the signal line pair **16** and provides a voltage signal **19** which is capacitively coupled by the capacitor **22** and further amplified by the buffer amplifier **20** to produce a transmit signal V_{tx} **13**. Accordingly, the transmit signal **13** is produced in accordance with the transmitter transfer function (discussed further below).

In the receiver circuit **14**, the input buffer amplifier **24** receives a receive signal V_{rx} **15** and provides a buffered input signal **21** which is received differentially with the transmit signal **13** by the transconductance amplifier **26**. In accordance with its transconductance G_m, as defined by the selectable impedance Z_c, the transconductance amplifier **26** provides a differential output current i_1–i_2 **23** which is amplified by the differential current amplifier **32** to provide a differential output current i_a–i_b **17** to the signal line pair **16**. Accordingly, the output current **17** is produced in accordance with the receiver transfer function (discussed further below).

Throughout the discussion, "outgoing", "transmit", "incoming" and "receive" are defined with respect to the telephone. For example, outgoing, or transmit, signals originate in a telephone (not shown) connected to the signal line pair **16** and pass into the signal interface circuit **10** and out thereof as the V_{tx} signal to a network (not shown), while incoming, or receive, signals come into the signal interface circuit **10** from the network as the V_{rx} signal and out thereof to the telephone via the signal line pair **16**. However,it should be understood, that these "directions" are merely exemplary and the claimed invention is not necessarily limited to such directivity.

The signal interface circuit **10** has a number of advantages which make it quite useful as a subscriber line interface circuit for a telecommunications system. In such a system, it is often required to provide a complex impedance termination for the signal line pair **16** while simultaneously providing transmit and receive transfer functions which have frequency responses matching those of the subscriber line pair **16** attached to terminals a and b, which itself has a complex impedance associated therewith. As discussed further below, the signal interface circuit **10** allows the termination impedance, i.e. the impedance as defined across the signal line pair **16**, as well as the transmit and receive transfer functions to be defined using one scaled complex impedance Z_c to set all three parameters. As a result, all three parameters will closely track one another over temperature, etc., thereby eliminating the need for multiple adjustments or matching networks. Accordingly, the relative signal gains and frequency response characteristics of the transmit and receive transfer functions can be easily set as desired.

The transconductance G_m of the transconductance amplifier **26** is defined by the impedance Z_c of the impedance circuit **28** such that the differential output current **17** is a function of the differential input voltage, i.e. the voltage levels V+ and V– of the input signal **21** and transmit signal **13** at the non-inverting and inverting inputs, respectively, as follows:

$$i_{out} = i_1 - i_2 \tag{1a}$$

$$i_{out} = \frac{2(V_+ - V_-)}{Z_C} \tag{1b}$$

The differential output current **17** provided to the signal line pair **16** is a function of the current amplifier **32** gain K and its differential input current **23**, as follows:

$$i_{ab} = i_a - i_b = \frac{K}{2}(i_1 - i_2) \tag{2}$$

It should be noted that, in practice, this gain K has second order gain and phase errors versus frequency. Accordingly, care should be taken to ensure that such errors have negligible effect upon the impedance desired at the signal line pair **16**.

The output impedance Z_o of the signal interface circuit **10** is essentially the output impedance, as defined by the feedback transfer function, of the current amplifier **32** (since the input impedance of the input transmitter amplifier **18** is so high as to have negligible effect). Accordingly, the output impedance Z_o is a function of the differential output voltage V_{ab} and differential output current i_{ab} (defined above) provided to the signal line pair **16** as follows:

$$Z_o = \frac{\delta V_{ab}}{\delta I_{ab}} \tag{3a}$$

$$Z_o = \frac{Z_C}{A_{tr}A_{ac}K} \tag{3b}$$

Therefore, the output impedance Z_o presented to the signal line pair **16** nodes a, b is directly proportional to the impedance Z_c of the impedance circuit **28** connected to the transconductance amplifier **26**.

Based upon the foregoing, the receiver transfer function, i.e. defined as the output voltage V_{ab} provided in accordance with a receive signal V_{rx} to a signal line pair **16** having a line impedance Z_L, can be defined as follows:

$$\frac{V_{ab}}{V_{rx}} = \frac{Z_L}{\left[\frac{Z_C}{A_{ac}A_{tr}K} + Z_L\right]} \cdot \frac{A_r}{A_{ac}A_{tr}} \tag{4}$$

Similarly, the transmitter transfer function, i.e. the transmit signal V_{tx} generated as a result of receiving a signal V_s from the signal line pair having a source impedance Z_L, can be defined as follows:

$$\frac{V_{tx}}{V_s} = \frac{Z_C}{\left[\frac{Z_C}{A_{ac}A_{tr}K} + Z_L\right]} \cdot \frac{1}{K} \quad (5)$$

As can be seen in the above equations, the transmitter and receiver transfer functions, and therefore their frequency response characteristics, as well as the output impedance Z_o presented to the signal line pair **16** are a function of the selectable impedance Z_c and the signal line pair **16** impedance Z_L. Accordingly, all three parameters are controlled by a single impedance (since the signal line pair **16** impedance Z_L is fixed) and, therefore, track each other over changes in temperature, etc.

Based upon the foregoing discussion, the operation of the signal interface circuit **10** can be summarized as follows. The termination impedance presented to the signal line pair **16** is defined as a change in voltage divided by a change in current (dV/dI). Hence, in order to generate a change in the line current (i_a–i_b), the voltage at the inverting terminal of the transconductance amplifier **26** must change relative to that at the noninverting terminal. Assuming no receive signal **15** is being received, this change in the inverting input must originate from a change in the voltage across the signal line pair **16**. Hence, a change in the line voltage results in a change in the line current, thereby defining an impedance. Accordingly, an outgoing signal **11** received at the signal line pair **16** causes the termination impedance to be defined, based upon the selectable impedance Z_c (since virtually no frequency dependency is introduced by the differential amplifier **18** and buffer amplifier **20**). Further accordingly, a buffered input signal **21** based upon a receive signal **15** is applied to the transconductance amplifier **26** differentially with respect to the feedback transmit signal **13** (which defines the output impedance of the circuit **10** as presented to the signal line pair **16** as discussed above). The resulting voltage across the selectable impedance **28** (Z_c) drives the current amplifier **32**, thereby producing the differential output current used for defining the termination impedance.

Referring to FIG. **2**, one embodiment of a signal interface circuit **10** with selectable signal interface parameters in accordance with the present invention can be realized as shown. Outgoing signals are received from the signal line pair **16** and amplified by the transmitter amplifiers **18**, **20** to produce the transmit signal **13**. The transmitter amplifiers **18**, **20** include operational amplifier ATRLV, AACLV and can be designed in accordance with well known principles. The output signal **19** from the first transmitter amplifier **18** is also provided to a dc bias controller **40** which provides a dc bias voltage **41** to the transconductance amplifier **26**. This dc bias voltage **41** is set typically between 10 millivolts and 1 volt in normal line feeding mode, i.e. the tip terminal more positive than the ring terminal. (The outgoing signal on the signal line pair **16** is also applied across a resistive voltage divider which provides an input to an operational amplifier ACMHV which, in turn, provides a biasing voltage within the receiver output amplifier **32**.)

The receive signal **15** is amplified by an operational amplifier ARAMP and applied to a switch network including switches C1 and C1B which selectively provide a gain of –3.5 DB or –7 dB. The resulting input signal **21** and the transmit signal **13** are applied to the transconductance amplifier **26**, as discussed above. The transconductance amplifier **26** is biased by a current source providing a bias current I_{BIAS} of approximately 50 microamperes.

The output currents i_1 ("IPLUS") and i_2 ("IMINUS") are applied to the current amplifier **32**. The input stage of the current amplifier **32** is a current buffer **42** (discussed further below) the differential output of which drives an operational amplifier AIVHV, which in turn, differentially drives two additional operational amplifiers **46**, **48** to provide the differential output currents i_a, i_b. The output currents i_a, i_b are applied to nodes TPR and RPR which, in turn, are resistively coupled (not shown) to the "tip" and "ring" terminals forming nodes a and b of the signal line pair **16**. The first operational amplifier **44** serves as a differential current-to-differential voltage converter, with the resulting differential output voltages driving the output operational amplifiers **46**, **48** which serve as voltage-to-current converters. A bias voltage source **50** provides a dc bias voltage **51** of approximately half the battery voltage, i.e. –26 volts when powered from a –52 volt battery supply.

The numeric legends adjacent the various MOSFETs shown in FIGS. **2–5** indicate the channel widths and lengths of their respective transistors. (For example, in FIG. **3**, the channel width and length of N-MOSFET MNV3 are 735 microns (735μ) and 4.9 microns (4.9μ), respectively. In FIGS. **3–5**, the power supply terminals labelled as VCC! and VBB! provide +5 and –5 volts dc, respectively, while the terminal labelled as AGND! is connected to circuit ground (e.g. as represented by the well known ground symbol "▽" in FIG. **2**).

Referring to FIG. **3**, one embodiment of the transconductance amplifier **26** can be realized as shown. The input signals **13**, **21** are buffered by input differential amplifiers AVA, AVB and applied to a complementary metal oxide semiconductor field effect transistor (CMOSFET) amplifier **60** across which the impedance circuit **28** is connected. Also connected across this differential amplifier **60** is a resistor RGMDC which sets the dc current gain for the transconductance amplifier **26**. (This resistor RGMDC has a value of approximately 26 kilohms.) The differential amplifier **60** is biased by a current biasing circuit **62** which, in turn, is driven by a current mirror circuit **64**. The current mirror circuit **64** is biased by the above-noted biasing current I_{BIAS} and is controlled by a differential bias driver AVC.

A bias controller **66** receives as inputs voltage V1 (approximately 3.5 volts) and voltage V2 (approximately 2.0 volts) from the current mirror circuit **64** and voltage V3 (approximately –2 volts). In accordance with these input voltages V1, V2, V3, the bias controller sinks bias currents IA and IB from the input differential buffer amplifiers AVA and AVB, respectively.

The connections identified by asterisks("*") are ones that can be modified from those as shown to provide for additional current drive for the differential amplifier **60**, thereby increasing the potential range of load impedances Z_L which can be driven by the signal interface circuit **10**.

Referring to FIG. **4**, the input differential amplifiers AVA and AVB of the transconductance amplifier **26** of FIG. **3** can be realized as shown. A CMOSFET differential amplifier **80** is biased by a current mirror circuit **82** which is driven by the bias current IA/IB (discussed above). One input is connected to the impedance circuit **28**, while the other input receives the transmit signal **13** or buffered receive signal **21** (discussed above). The output signal AVAO/AVBO is then provided to the appropriate input of the CMOSFET differential amplifier circuit **60** of FIG. **3**.

Referring to FIG. **5**, the bias driver AVC for the current mirror circuit **64** of FIG. **3** can be realized as shown. With the non-inverting input grounded and the inverting input biased by the voltage present on the I_{BIAS} current line, an output voltage AVCO is generated for driving the current mirror circuit **64** of FIG. **3**.

Referring to FIG. **6**, the current buffer **42** of FIG. **2** can be realized with NPN and PNP bipolar junction transistors as shown. Biased by a −52 volt dc source (VBAT) and a bias current I_{BIAS2} of approximately 150 microamperes, and with transistor **Q2** operating as a zener diode, a dc voltage of approximately −7.6 volts appears at the base terminals of transistors **Q4** and **Q6**. With the differential currents IPLUS and IMINUS from the transconductance amplifier **26** at the emitter terminals of transistors **Q5** and **Q3**, respectively, the differential output currents **43***m*, **43***p* are generated.

Referring to FIG. **7**, one embodiment of the impedance circuit **28** includes two resistors R_1, R_2 and a capacitor C_1, connected as shown. This impedance configuration, i.e. a resistor in series with a parallel combination of a resistor and capacitor, corresponds to the impedance configuration which typically represents the line impedance Z_L of the signal line pair **16** (FIG. **1**). The actual component values for the resistors R_1, R_2 and capacitor C_1, however, do not equal their counterparts in the line impedance Z_L. Rather, the component values for the impedance circuit **28** must be scaled in accordance with the gain factors of the transconductance amplifier **26**, current amplifier **32**, differential voltage amplifier **18** and buffer amplifier **20**. For the embodiment of the signal interface circuit **10** shown in FIG. **2**, this scaling factor is approximately 137. Accordingly, to provide an output impedance Z_o which equaled a signal line pair **16** impedance Z_L of 200 ohms in series with a parallel combination of 680 ohms and a capacitance of 100 nanofarads, the values of the components in the impedance circuit **28** would be: R_1=27.4 kilohms; R_2=93.16 kilohms; and C_1=730 picofarads.

Attached hereto as Appendix A and incorporated herein by reference is a preliminary data sheet prepared by the Assignee of the present invention for an integrated circuit containing an embodiment of a signal interface circuit with selectable signal interface parameters in accordance with the present invention.

Various other modifications and alterations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and spirit of the invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. It is intended that the following claims define the scope of the present invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.

What is claimed is:

1. An apparatus including a signal interface circuit with selectable signal interface parameters, said signal interface circuit comprising:

a pair of impedance terminals for coupling to an impedance circuit having a selectable impedance value associated therewith;

a pair of signal terminals for coupling to an external signal line pair and conducting outgoing and incoming signals therefrom and thereto, respectively, wherein said pair of signal terminals has a definable termination impedance associated therewith and said external signal line pair has a line impedance associated therewith, and wherein said definable termination impedance is defined in accordance with said selectable impedance value;

a transmitter circuit, coupled to said pair of signal terminals and having a definable transmitter transfer function associated therewith, for receiving said outgoing signal and providing a transmit signal in accordance with said definable transmitter transfer function, wherein said definable transmitter transfer function is defined in accordance with said selectable impedance value; and

a receiver circuit, coupled to said pair of impedance terminals, said pair of signal terminals and said transmitter circuit and having a definable receiver transfer function associated therewith, for receiving an input signal and said transmit signal and providing said incoming signal in accordance with said definable receiver transfer function, wherein said definable receiver transfer function is defined in accordance with said selectable impedance value.

2. An apparatus as recited in claim **1**, wherein said definable termination impedance is defined to match said line impedance.

3. An apparatus as recited in claim **1**, further comprising an impedance circuit having said selectable impedance value associated therewith.

4. An apparatus as recited in claim **3**, wherein said impedance circuit comprises resistive and capacitive elements.

5. An apparatus as recited in claim **1**, wherein said transmitter circuit comprises a differential amplifier and said outgoing signal comprises a differential signal.

6. An apparatus as recited in claim **1**, wherein said receiver circuit comprises a first differential amplifier, coupled to said pair of impedance terminals and said transmitter circuit, for differentially receiving said input signal and said transmit signal and providing a first differential output signal.

7. An apparatus as recited in claim **6**, wherein said receiver circuit further comprises a second differential amplifier, coupled to said first differential amplifier and said pair of signal terminals, for receiving said first differential output signal and providing a second differential output signal as said incoming signal.

8. An apparatus as recited in claim **1**, wherein said receiver circuit comprises a transconductance amplifier, coupled to said pair of impedance terminals and said transmitter circuit and having a definable transconductance associated therewith, for receiving a first voltage signal as said input signal and a second voltage signal as said transmit signal and providing an output current signal in accordance with said definable transconductance, wherein said definable transconductance is defined in accordance with said selectable impedance value.

9. An apparatus as recited in claim **1**, further comprising a buffer amplifier, coupled to said receiver circuit, for receiving and buffering a receive signal and providing said input signal, wherein operation of said buffer amplifier does not affect either one of said definable termination impedance or said definable transmitter transfer function.

10. An apparatus as recited in claim **1**, further comprising at least one integrated circuit into which said signal interface circuit is integrated.

11. A method of providing an apparatus including a signal interface circuit with selectable signal interface parameters, said method comprising the steps of:

providing a pair of impedance terminals for coupling to an impedance circuit having a selectable impedance value associated therewith;

providing a pair of signal terminals for coupling to an external signal line pair and conducting outgoing and incoming signals therefrom and thereto, respectively, wherein said pair of signal terminals has a definable

termination impedance associated therewith and said external signal line pair has a line impedance associated therewith, and wherein said definable termination impedance is defined in accordance with said selectable impedance value;

providing a transmitter circuit, coupled to said pair of signal terminals and having a definable transmitter transfer function associated therewith, for receiving said outgoing signal and providing a transmit signal in accordance with said definable transmitter transfer function, wherein said definable transmitter transfer function is defined in accordance with said selectable impedance value; and

providing a receiver circuit, coupled to said pair of impedance terminals, said pair of signal terminals and said transmitter circuit and having a definable receiver transfer function associated therewith, for receiving an input signal and said transmit signal and providing said incoming signal in accordance with said definable receiver transfer function, wherein said definable receiver transfer function is defined in accordance with said selectable impedance value.

12. A method as recited in claim **11**, wherein said step of providing a pair of signal terminals for coupling to an external signal line pair and conducting outgoing and incoming signals therefrom and thereto, respectively, comprises providing a pair of signal terminals having an associated, definable termination impedance which is defined to match said line impedance.

13. A method as recited in claim **11**, further comprising the step of providing an impedance circuit having said selectable impedance value associated therewith.

14. A method as recited in claim **13**, wherein said step of providing an impedance circuit having said selectable impedance associated therewith comprises providing resistive and capacitive elements.

15. A method as recited in claim **11**, wherein said step of providing a transmitter circuit comprises providing a differential amplifier and said outgoing signal comprises a differential signal.

16. A method as recited in claim **11**, wherein said step of providing a receiver circuit comprises providing a first differential amplifier, coupled to said pair of impedance terminals and said transmitter circuit, for differentially receiving said input signal and said transmit signal and generating a first differential output signal.

17. A method as recited in claim **16**, wherein said step of providing a receiver circuit further comprises providing a second differential amplifier, coupled to said first differential amplifier and said pair of signal terminals, for receiving said first differential output signal and generating a second differential output signal as said incoming signal.

18. A method as recited in claim **11**, wherein said step of providing a receiver circuit comprises providing a transconductance amplifier, coupled to said pair of impedance terminals and said transmitter circuit and having a definable transconductance associated therewith, for receiving a first voltage signal as said input signal and a second voltage signal as said transmit signal and generating an output current signal in accordance with said definable transconductance, wherein said definable transconductance is defined in accordance with said selectable impedance value.

19. A method as recited in claim **11**, further comprising the step of providing a buffer amplifier, coupled to said receiver circuit, for receiving and buffering a receive signal and providing said input signal, wherein operation of said buffer amplifier does not affect either one of said definable termination impedance or said definable transmitter transfer function.

20. A method as recited in claim **11**, further comprising the step of providing at least one integrated circuit into which said signal interface circuit is integrated.

21. A method of providing a signal interface with selectable signal interface parameters, said method comprising the steps of:

defining a termination impedance in accordance with a selectable impedance value;

defining a transmitter transfer function in accordance with said selectable impedance value;

defining a receiver transfer function in accordance with said selectable impedance value;

coupling to a signal line pair with a pair of signal terminals, wherein said signal line pair has a line impedance associated therewith and said pair of signal terminals has said defined termination impedance associated therewith;

conducting an outgoing signal from said signal line pair via said pair of signal terminals;

amplifying said outgoing signal and providing a transmit signal in accordance with said defined transmitter transfer function;

receiving an input signal and said transmit signal and providing an incoming signal in accordance with said defined receiver transfer function; and

conducting said incoming signal to said signal line pair via said pair of signal terminals.

22. A method as recited in claim **21**, wherein said step of defining a termination impedance in accordance with a selectable impedance value comprises defining said termination impedance to match said line impedance.

23. A method as recited in claim **21**, further comprising the step of establishing said selectable impedance value with an impedance circuit including resistive and capacitive elements.

24. A method as recited in claim **21**, wherein said step of amplifying said outgoing signal and providing a transmit signal in accordance with said defined transmitter transfer function comprises differentially amplifying a differential signal as said outgoing signal.

25. A method as recited in claim **21**, wherein said step of receiving an input signal and said transmit signal and providing an incoming signal in accordance with said defined receiver transfer function comprises differentially receiving said input signal and said transmit signal and generating a first differential output signal.

26. A method as recited in claim **25**, wherein said step of receiving an input signal and said transmit signal and providing an incoming signal in accordance with said defined receiver transfer function further comprises receiving said first differential output signal and generating a second differential output signal as said incoming signal.

27. A method as recited in claim **21**, wherein said step of receiving an input signal and said transmit signal and providing an incoming signal in accordance with said defined receiver transfer function comprises:

defining a transconductance in accordance with said selectable impedance value;

receiving a first voltage signal as said input signal;

receiving a second voltage signal as said transmit signal; and

generating an output current signal in accordance with said defined transconductance.

28. A method as recited in claim **21**, further comprising the step of receiving and buffering a receive signal and providing said input signal without affecting either one of said defined termination impedance or said defined transmitter transfer function.

29. A method as recited in claim **21**, further comprising the step of performing said recited steps for providing a signal interface with selectable signal interface parameters within at least one integrated circuit.

* * * * *

Submission II

Type	Reference	Title
Book Extract	Datasheet TP3210 SLIM™	Subscriber Line Interface Module; Preliminary Datasheet, pp 143-162; National Semiconductor Telecommunications Databook, 1995
Citations	**5**	

National Semiconductor

PRELIMINARY

TP3210 SLIM™ Subscriber Line Interface Module

General Description

The TP3210 is a complete electronic SLIC and PCM COMBO® CODEC/Filter module intended to interface the analog subscriber line to a PCM highway. It is designed to meet the requirements for U.S. central office and remote switching applications. When used in conjunction with a simple, non-critical, external protection network, two resistors and a ring relay, the TP3210 forms a complete line circuit, handling all the BORSCHT functions.

The TP3210 module consists of a line driver, a line receiver, a line impedance control circuit, a hybrid balance circuit, a line supervision circuit, a ring supervision circuit, three positive relay drivers, a TP3054 μ-Law COMBO CODEC/Filter and a serial control interface. Any changes in the status of the subscriber loop generate an interrupt, allowing the device to be used in either polled or interrupt driven applications.

Features

- Complete COMBO CODEC/Filter and SLIC functions
- Exceeds LSSGR central office specifications
- In-band on-hook transmission capability
- Resistive loop feed with current limit
- Power denial mode
- Compatible with loop start and ground start signalling
- Automatic ring trip compatible with all U.S ringing conditions
- Four selectable hybrid balance networks
- Three relay drivers
- Thermal overload protection
- Compatible with inexpensive protection networks
- Withstands 500V RTN to GND surge
- Compatible with standard PCM highway
- Small physical size and minimal external components

Simplified Block Diagram

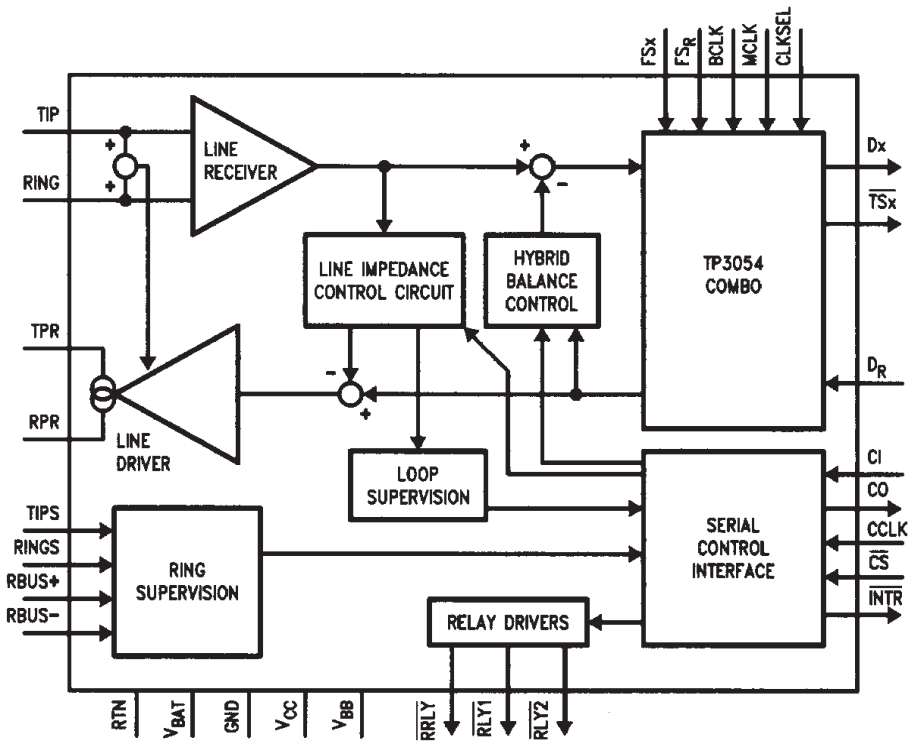


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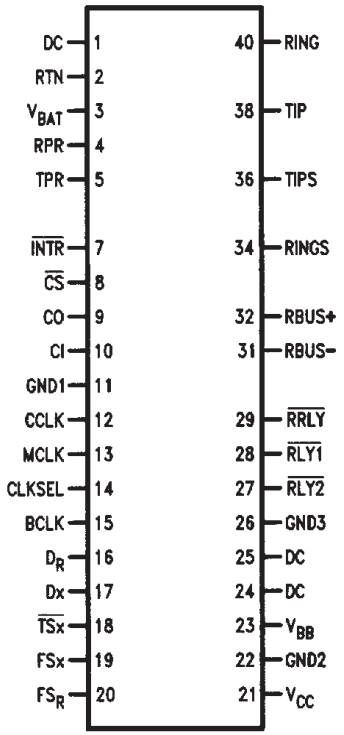
FIGURE 1. Simplified Block Diagram

Connection Diagram

Top View



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Order Number TP3210J
NS Package Number HY40C

Pin Descriptions

Pin	Description
TIP	Normally positive side of the subscriber line.
RING	Normally negative side of the subscriber line.
TPR	High voltage line driver output. Connects to TIP via an external protection network.
RPR	High voltage line driver output. Connects to RING via an external protection network.
TIPS	Positive ring sensing input. Connected to the positive side of the subscriber loop during ringing.
RINGS	Negative ring sensing input. Connected to the negative side of the subscriber loop during ringing.
RBUS+	Positive ring bus sensing input. Connected to the positive side of the ring bus.
RBUS−	Negative ring bus sensing input. Connected to the negative side of the ring bus.
BCLK	Bit Clock used to shift PCM information into D_R and out of Dx. May vary from 64 kHz to 2.048 MHz in 8 kHz increments.
MCLK	Master Clock. Must be 1.536, 1.544 or 2.048 MHz.
CLKSEL	Master Clock Select Input. Must be connected high for 1.536 or 1.544 MHz operation. Must be connected low for 2.048 MHz operation.
FSx	Transmit frame synchronization pulse input which enables BCLK to shift the PCM information out of Dx. FSx is an 8 kHz pulse train. See *Figures 8* and *9* for timing details.
Dx	The TRI-STATE® PCM data output which is enabled by FSx.
$\overline{TSx}$	Open drain output which pulses low during the period when the Dx output is enabled.
FS_R	Receive frame synchronization pulse input which enables BCLK to shift the PCM information into D_R. FS_R is an 8 kHz pulse train. See *Figures 8* and *9* for timing details.
D_R	Receive data input. PCM data is shifted into D_R during the receive timeslot determined by FS_R.
CCLK	Control clock used to shift control data into CI and out of CO during $\overline{CS}$ low.
$\overline{CS}$	Chip select input. Must be low to enable the shifting of control data into CI and out of CO.
CI	The serial control data input used to set the operating state of the module.
CO	The serial status output used to monitor the operating state of the module. CO is TRI-STATE when $\overline{CS}$ is high. See *Figure 3* for timing diagram.
$\overline{INTR}$	Open drain interrupt output. A logic low indicates a change in the status of the subscriber loop, or a change in thermal shutdown.
V_{BB}	Negative power supply. V_{BB} = 5V ±5%. Decoupled by internal 0.047 μF to ground.
V_{CC}	Positive power supply. V_{CC} = 5V ±5%. Decoupled by internal 0.047 μF to ground.
$\overline{RRLY}$	Ring Relay Driver. Controlled by State Control Data Word bit D4 (see Table I). It is automatically turned off when ring trip is detected.
$\overline{RLY1}$	General purpose relay driver controlled by State Control Data Word bit D5.
$\overline{RLY2}$	General purpose relay driver controlled by State Control Data Word bit D6.
GND1 GND2 GND3	Low Voltage Ground. V_{BB}, V_{CC} and all digital signals are referenced to these pins. GND1, GND2 and GND3 should be externally connected together close to the module. Collectively referenced as GND in electrical specifications.
V_{BAT}	Negative high voltage supply. V_{BAT} = −55V to −59V.
RTN	High voltage ground return. V_{BAT} and all analog signals are referenced to this pin.
DC	Don't connect. Do not make external connections to these pins.

Functional Block Description

Functional Block	Description
Line Driver	The Line Driver is a differential output transconductance amplifier which provides the d.c. power and balanced a.c. signals to the subscriber line. The d.c. power is determined by the d.c. Loop Impedance Control circuit. The a.c. signal applied to the line is controlled by the a.c. Loop Impedance Control and the analog signal generated by the TP3054 COMBO CODEC/Filter from the received PCM information. Feedback from the TIP and RING lines produces an effective longitudinal input impedance of about 150Ω from TIP and RING to RTN (75Ω total). In the presence of large longitudinal currents, each output of the Line Driver is capable of sourcing or sinking current to limit the longitudinal voltage.
Line Receiver	The Line Receiver monitors the metallic (differential) voltage on the line in the presence of large longitudinal (common mode) voltages.
Loop Impedance Control	The Loop Impedance Control feeds back the line voltage to produce a resistive/inductive d.c. feed impedance for longer loops and a constant current d.c. feed for shorter loops while maintaining an a.c. 2-wire input impedance of 900Ω + 2.16 μF over the voice band, easily meeting the 2-wire return loss requirements.
Hybrid Balance Control	The Hybrid Balance Control circuit consists of four software selectable networks, assuring that the 4-wire return loss requirements are met for a variety of conditions.
Loop Supervision	The Loop Supervision circuit monitors the d.c. current flow in the subscriber loop under non-ringing state and detects on-hook, off-hook and replicates dial pulses.
Ring Supervision	The Ring Supervision circuit monitors the d.c. current flow in the subscriber loop during the ringing state. This circuit is capable of detecting an off-hook condition in less than 200 ms in the presence of large a.c. ringing signals. It operates on loops with ringing superimposed on TIP or RING or with balanced ringing. It supports bridged ringers, ringers to ground on either TIP or RING and with superimposed ringers.
Relay Drivers	The three NPN relay drivers are capable of driving +5V or +12V relays directly. $\overline{RRLY}$ is dedicated to the ring relay and is automatically turned off when ring trip is detected by the Ring Supervision circuit. $\overline{RLY1}$ and $\overline{RLY2}$ are general purpose. Relay current will be returned to GND3 at pin 26.
COMBO	The COMBO provides the PCM filtering, encoding and decoding functions necessary to interface the PCM highway to the analog signals on the subscriber loop. This function is identical to the industry standard TP3054 COMBO CODEC/Filter (see the TP3054 datasheet for full details).
Control Interface	The Control Interface circuit provides easy control and monitoring of the state of the TP3210 via a simple serial interface. Via this circuit the user can program the operating mode of the module, and monitor the line status (see Table I for details).

Functional Description

Power-On

When power is first applied, the power-on reset circuitry initializes the TP3210 and places it in a standby mode. The State Control Data Word is cleared to "0". All unnecessary circuitry is powered down. The serial control interface and the loop supervision circuitry remain fully functional. The device is now ready for activation, either by the user programming it into the ring mode by writing into the State Control Data Word or by the subscriber going off-hook, powering-up the device automatically.

The State Control Data Word

The State Control Data word is a single eight-bit word as shown in Table I. Bits D0–D7 of the control word program the operating state of the device. The module can override the control bits D2 and D3 to activate the power denial mode in order to protect itself from damage under a thermal overload condition.

Status Word

The eight-bit Status Word indicates the status of the TP3210 at the instant a read operation is performed. Table IV shows the definitions of the status word. A logic high indicates that the state or function is enabled, a low indicatse that it is disabled.

The Control Interface

The Control Interface consists of a single eight-bit shift register and a buffer register. The shift register is written via the serial input CI, under the control of $\overline{CS}$ and CCLK, to program the device's operating state. Several bits of the shift register may be altered by the device itself in response to changes in the subscriber loop status. These changes in state may be read via the serial output CO. The S2 and S3 status bits are over-written by the occurrence of a thermal overload, forcing the device into the Power-Denial mode. S7 is the hook-switch status bit. A logic "0" for S7 indicates an Off-Hook or Ring-Trip condition exists at the instant of access and a logic "1" indicates on-hook. Any changes in line status, or thermal shutdown condition will generate an interrupt at $\overline{INTR}$ output.

Functional Description (Continued)

TABLE I. State Control Data Word

Control Bit	Description
D7	Don't Care. This bit is overwritten by the line supervision circuitry.
D6	A logic "1" turns on $\overline{RLY2}$.
D5	A logic "1" turns on $\overline{RLY1}$.
D4	A logic "1" enables Ring mode, turns on $\overline{RRLY}$ and Ring Supervision circuit. Status Bit S7 indicates ring-trip. Logic "0" at D4 enables the normal non-ringing mode.
D3	Used with D2 to select Power Denial, Battery Reversal and On-Hook Transmission modes. See Table II. Under Power Denial mode, the Line Driver is disabled, denying power to the subscriber loop. It can be set or cleared by a write operation. Under a thermal overload condition, D2 is forced to "0" and D3 is forced to "1" in order to protect the device from damage. As long as the thermal overload condition exists, the Power Denial mode cannot be cleared by a write operation.
D2	Used with D3 to select Power Denial, Battery Reversal and On-Hook Transmission modes. See Table II.
D1	Used with D0 to select hybrid balance network. See Table III.
D0	Used with D1 to select hybrid balance network. See Table III.

TABLE II. Operating Modes of TP3210

D4	D3	D2	Mode
0	**0**	**0**	Normal
0	0	1	Reverse Battery
0	1	0	Power Denial
0	1	1	On-Hook Transmission
1	X	X	Ring

TABLE III. Hybrid Balance Test Networks

D1	D0	Reference Test Network
0	**0**	900Ω
0	1	1650Ω‖(100Ω + 0.005 μF)
1	0	800Ω‖(100Ω + 0.05 μF)
1	1	900Ω + 2.16 μF

There are several ways of accessing the serial control interface. They are:

a. Write/Read

b. Read/Write

c. Quick Status Read

In the Write/Read operation, the objective is to change the state of the device. While shifting the new state control data into CI, the previous status information is shifted out of CO. This data should be compared with the previous status information to determine if a change had occurred since the last access.

In the Read/Write operation, the objective is to monitor the state of the module. While the current status is shifted out at CO, the last known state of the device is shifted into CI externally. If a thermal overload condition has occurred since the last access, the device will automatically set itself to the power denial mode (S2 bit will be forced to "0" and S3 bit will be forced to "1") prior to the access and will be reset by writing the previous state. This has no detrimental effect, however, since the power-denial mode will immediately be set again and the device will remain in the Power-Denial mode as long as the thermal overload continues to exist. If ring trip has occurred or the hook switch status has changed since the last access, the S7 bit will also be altered by the device. The timing for the Write/Read or Read/Write modes is shown in *Figure 2*.

The Quick Status Read operation allows a fast read of the S7 status bit, which indicates if a Ring-Trip or Off-Hook condition exists. It does not cause the shift register to shift, thus no control data is required. *Figure 3* is the timing diagram for the Quick Status Read Mode.

Functional Description (Continued)

TABLE IV. Status Information Word

Status Bit	Description
S7	Indicates switch hook status. S7 is a "1" if the subscriber is on-hook. If D4 is programmed to be "0" for normal mode, a logic "0" at S7 indicates off-hook. If the device is in the Ring mode (D4 = "1"), a logic "0" at S7 indicates ring-trip.
S6	A logic "1" indicates that $\overline{RLY2}$ is on.
S5	A logic "1" indicates that $\overline{RLY1}$ is on.
S4	A logic "1" indicates Ring mode is on. $\overline{RRLY}$ is turned on, and the Ring Supervision circuit is activated. A logic "0" at S7 indicates that a ring trip has occurred, forcing $\overline{RRLY}$ to be de-activated. D4 should be cleared to "0" by a write/read operation in order to program the device into the normal mode.
S3	S2 and S3 indicate Power-Denial, Battery Reversal and On-Hook Transmission modes. See Table II. When an overload condition exists which raises the junction temperature to exceed about 170°C, the TP3210 will automatically initialize a power denial mode (S2 forced to "0" and S3 forced to "1") to protect itself from damage. The device will not go back to the normal mode even if the thermal overload ceased to exist. The system can determine if the thermal overload condition has cleared itself by programming the TP3210 into the desired operating mode and read back status bits S2 and S3. If the overload still exists, the power denial mode will be activated again as long as the device's junction temperature exceeds approximately 170°C.
S2	S2 and S3 indicate Power-Denial, Battery Reversal and On-Hook Transmission modes. See Table II.
S1	S0 and S1 indicate the selected hybrid balance test network. See Table III.
S0	S0 and S1 indicate the selected hybrid balance test network. See Table III.

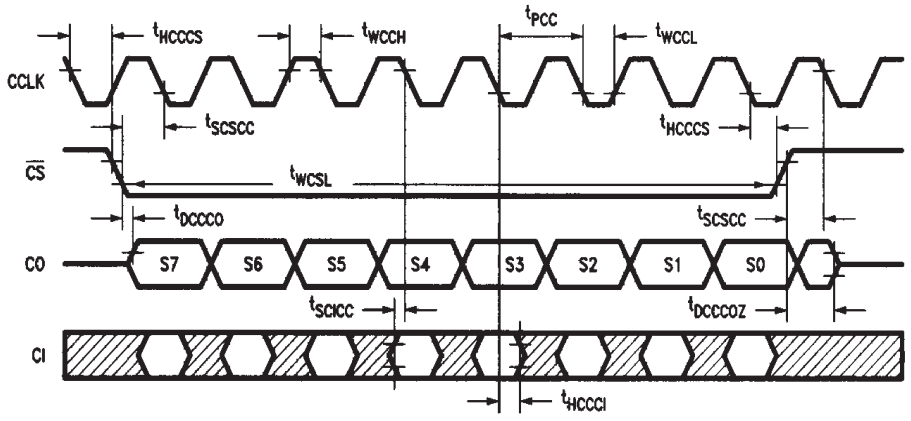

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FIGURE 2. Control Interface Timing—Write/Read or Read/Write Modes

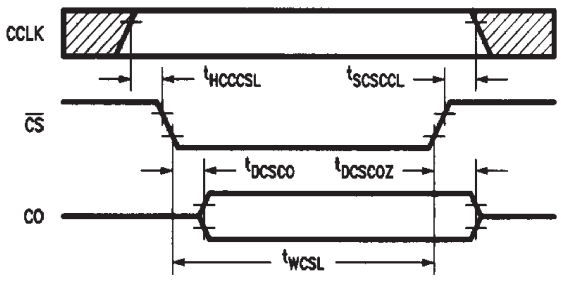

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FIGURE 3. Control Interface Timing—Quick Status Read Mode

Functional Description (Continued)

Battery Feed

The apparent battery voltage across the line is approximately 0.86 × V_{BAT}. With V_{BAT} = −56V, the TP3210 provides a nominal apparent battery voltage of −48V across TIP and RING. The module provides a resistive/inductive feed at longer loops. The d.c. current feed has been designed to guarantee 21 mA into a 1900Ω loop at nominal battery. At shorter loops, the d.c. feed is current-limited to nominally 43 mA in order to conserve power. At normal battery polarity (D2=0 and D3=0), TIP is more positive than RING. The current feed characteristic is shown in *Figure 4*.

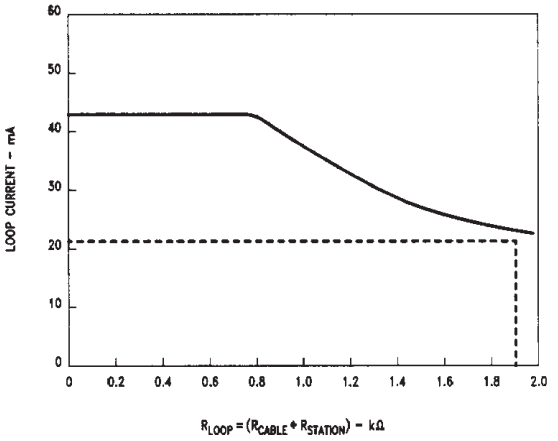

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FIGURE 4. DC Feed Characteristics

2-Wire Impedance

The nominal 2-wire input impedance is 900Ω + 2.16 μF. This is shunted by a feed inductance which is nominally 26 Henries on long loops, and approaches infinity on short loops.

Transmission Level

The 0 TLP is referenced at the PCM interface of the four wire ports. The TP3210 has 0.1 dB loss for both transmit and receive signals. On the 2-wire analog interface, the transmit is +0.1 TLP and the receive is −0.1 TLP. 0 TLP is defined as 0 dBm into 900Ω.

Hybrid Balance

The Hybrid Balance Control circuit contains four selectable balance networks which are selected by programming State Control Word bits D0 and D1. The balance networks are intended to be used with the corresponding reference test networks for hybrid balance as shown in Table III.

Longitudinal Balance and Longitudinal Current Capability

The 2-wire input of the device exhibits a longitudinal impedance of 150Ω from TIP to ground and from RING to ground. These impedances are extremely well matched and are not strongly dependent on impedance matching in the external protection network. The longitudinal voltage is sensed on the loop side of the protection network and fed back to the Line Driver, thus any component variations external to the device can be corrected by the feedback loop. The Line Driver is capable of handling 20 mA_{rms} of longitudinal current in each of the TIP and RING leads.

Loop Supervision

The Loop Supervision circuit operates in the normal (nonringing) state. At normal battery polarity, off-hook is indicated when loop current exceeds nominally 8.5 mA and on-hook indicated when the current falls below nominally 6.5 mA, providing a 2 mA hysteresis. The Loop Supervision has been designed to maintain the dial pulse make interval greater than 25 ms regardless of the distortion introduced by the loop characteristics. At reversed battery polarity, off-hook is detected when loop current exceeds nominally 12 mA and on-hook indicated when current falls below nominally 10 mA. A logic "1" at status bit S7 indicates on-hook, while a logic "0" indicates off-hook. For Ground Start Signalling, TIP is opened with an external relay. Off-hook is indicated when the current from RING to ground exceeds nominally 17 mA and on-hook when the current falls below nominally 13 mA.

A typical example of hook switch timing is illustrated in *Figure 5*. While in the standby mode, all unnecessary circuitry is powered down. When Loop Supervision detects off-hook, the module is powered up, $\overline{INTR}$ goes low and status bit S7 is cleared (A). The $\overline{INTR}$ remains active until $\overline{CS}$ goes low and status is read, at which time the status of the switch hook is latched, clearing $\overline{INTR}$ (B). When the Loop Supervision detects on-hook, all unnecessary circuitry is again powered down, status bit S7 is set and $\overline{INTR}$ is again set low (C). When the status information is read, the present switch hook status is latched, clearing the interrupt, and $\overline{INTR}$ goes high (D). In the case of either on-hook or off-hook, if the system fails to read the status before the switch hook reverts to its previous state, the interrupt will clear itself (E). If the device's control interface is being accessed when off-hook occurs, i.e., $\overline{CS}$ is low, $\overline{INTR}$ is set low immediately (F) but S7 is cleared only after $\overline{CS}$ returns high (G). On the next Read/Write access, S7 is latched.

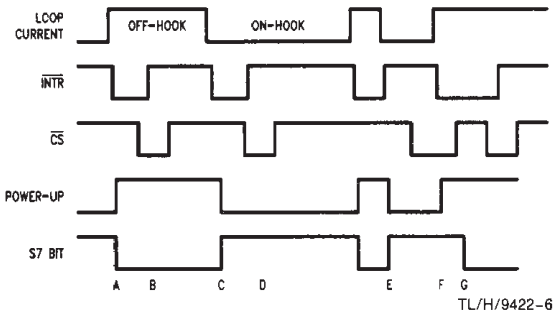

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FIGURE 5. Typical Hook Switch Detect Timing

Ring Supervision

The Ring Supervision circuit measures the loop current across two 360Ω ring sensing resistors with a 1 MΩ internal resistive bridge (see *Figure 10*). The voltage at the output of the bridge is filtered, then algebraically added and subtracted from a voltage corresponding to a loop current of about 11 mAdc. Each of the resulting voltages are integrated over one period of the ring frequency and compared to zero. If either of the resulting voltages is less than zero for two consecutive cycles, ring-trip is detected. $\overline{RRLY}$ is de-activated, status bit S7 is cleared to "0" indicating ring trip, and an interrupt is also generated. Control bit D4 is not automatically reset to "0", it has to be cleared to "0" by a write/read operation after a ring trip is detected. If the MCLK is interrupted and stays continuously high or low for more than 200 μs, the ring relay driver will be turned off.

Functional Description (Continued)

The ring supervision circuit works with zero to five bridged ringers (1 ringer = 7 kΩ at 20 Hz),with ring frequencies from 16 Hz to 67 Hz, with ring voltages from 90 Vrms to 155 Vrms applied to either TIP or RING, superimposed on positive or negative battery voltages of from 42V to 56V on loops up to 1700Ω. Furthermore, it operates with up to five ringers connected from TIP or RING to ground or with up to three superimposed ringers connected from TIP to ground and three from RING to ground with a battery voltage of ±38 ±2V. The ring sensing inputs at TIPS, RINGS, RBUS+ and RBUS− when connected as shown in *Figure 10*, will present an effective load of about 500 kΩ across the ring bus.

A typical example of ring trip timing is illustrated in *Figure 6*. When the Ring Supervision circuit detects a ring trip, the device immediately turns off $\overline{RRLY}$, clears S7 and sets $\overline{INTR}$ low (A). The interrupt remains active until $\overline{CS}$ goes low and the status is read, at which time the status of the switch hook is latched, clearing $\overline{INTR}$ (B). Status bit S7 will remain a zero until the D4 bit is written to a zero, removing the device from the Ring mode (C). At this time, the S7 bit will indicate the switch hook status. Even though the station equipment is normally off-hook at this time, S7 will generally return to a "1" for several milliseconds (C) after D4 is cleared. This is because the Loop Supervision circuit was disconnected from the loop during ringing mode (D4 = 1), and it takes several milliseconds to detect the off-hook at which time S7 will be cleared and $\overline{INTR}$ will be set low (D). At this point the device is in the normal (non-ringing) mode, all necessary circuitry is powered up.

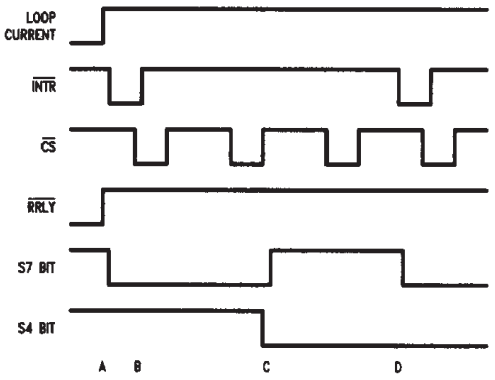

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FIGURE 6. Typical Ring Trip Detect Timing

Thermal Overload

The Line Driver incorporates a built-in thermal overload detection circuitry. In the event of a fault on the subscriber line which causes the Line Driver to reach an internal junction temperature of approximately 170°C, the Line Driver will protect itself by forcing the device into the power-denial mode (S2 is forced to "0" and S3 is forced to "1"). The device will remain in power-denial mode even though the thermal overload ceases to exist. After the line fault has been cleared, the device can be put back into service under system control (see Table IV).

A typical example of thermal overload detection timing is illustrated in *Figure 7*. When a thermal overload is detected, S2 is set low and S3 is set high (A), forcing the device into the Power-Denial mode, and $\overline{INTR}$ is set low. The interrupt remains active until $\overline{CS}$ goes low, clearing $\overline{INTR}$ (B). As long as the thermal overload condition exists, the power denial mode cannot be reset by a write operation (B). When the thermal overload condition clears, the $\overline{INTR}$ will again be set low, but the device continues to remain at power denial mode (C). Thus the device does not automatically reapply power to the line since the fault that originally caused the failure may still exist and would simply cause the overload to reoccur. In this example, the Power-Denial mode is cleared by a control write to normal mode, clearing S2 and S3 to "0" (D). If the device is being accessed at the instant the thermal shutdown indication occurs, $\overline{INTR}$ is set low immediately, but S2 will be set low and S3 will be set high only after $\overline{CS}$ returns high (E).

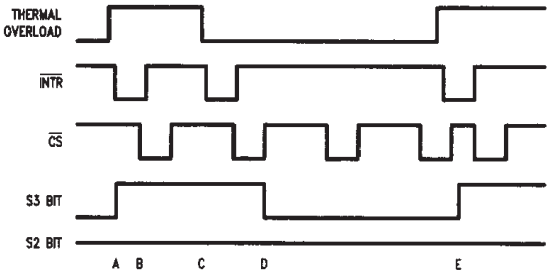

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FIGURE 7. Typical Thermal Overload Detection Timing

On-Hook Transmission Mode

The device is in the on-hook transmission mode when bit D3 and D2 of the State Control Data Word is set to the logic "1" and the loop is under "on-hook". In this mode, the line drivers operate in a reduced power state but all circuitry is active. This enables the system to communicate with a subscriber terminal or the subscriber to communicate through the network or to a terminal in the central office to provide alarm and telemetry services. When the loop goes off-hook, the loop supervision circuitry behaves normally and causes the line drivers to power up. Bit S7 of the Status Information Word is cleared and an interrupt is initiated. This enables the system to terminate any transmissions and handle the call initiation in the normal manner.

PCM Interface

The PCM interface consists of inputs MCLK, BCLK, FSx, FS_R and D_R, and outputs Dx and $\overline{TSx}$. MCLK controls the internal operation of the COMBO Codec/Filter's encoder and decoder, and must be 1.536 MHz or 1.544 MHZ if CLKSEL is connected high and 2.048 MHz if CLKSEL is connected low. BCLK shifts the PCM data out of Dx on its rising edge and latches the PCM data into D_R on its falling edge. It must be synchronous with MCLK and may be any integer multiple of 8 kHz from 64 kHz to 2.048 MHz. FSx and FS_R are 8 kHz pulse waveforms which determine the beginning of the PCM data transfer out of Dx and into D_R respectively. Both must be synchronous with MCLK but may have any phase relationship with each other. $\overline{TSx}$ is an open drain output which pulses low for the duration of the data transfer out of Dx. It is intended to be wire-ORed with the $\overline{TSx}$ outputs of other subscriber line interface modules to provide an enable signal for external TRI-STATE drivers buffering the PCM transmit data from a line card onto the backplane.

Short Frame Sync Operation

The TP3210 Subscribe Line Interface Module can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, the frame sync pulses applied to both FSx and FS_R must be one BCLK period long and with timing relationships as specified in *Figure 8*. With FSx high during a

Functional Description (Continued)

falling edge of BCLK, the next rising edge of BCLK enables the Dx TRI-STATE output buffer, which will output the PCM sign bit. The following seven rising edges of the bit clock shifts out the remaining seven bits of PCM data, MSB first. The next falling edge disables the Dx output. With FS_R high during a falling edge of BCLK, the next falling edge latches the PCM sign bit into D_R. The next seven falling edges latch the remaining seven bits, MSB first.

Long Frame Sync Operation

To use the long frame sync mode, the frame sync pulses applied to both FSx and FS_R must be three or more bit periods long, with timing relationships as specified in *Figure 9*.

Based on the transmit frame sync pulse, the device will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The Dx TRI-STATE output buffer is enabled with the rising edge of FSx or the rising edge of BCLK, whichever comes later, and the first bit clocked out is the PCM sign bit. The following seven rising edges of BCLK shift out the remaining seven bits, MSB first. The Dx output is disabled by the falling edge of BCLK following the eighth rising edge or by FSx going low, whichever comes later. A rising edge of the receive frame sync will cause PCM data at D_R to be latched in on the next eight falling edges of BCLK.

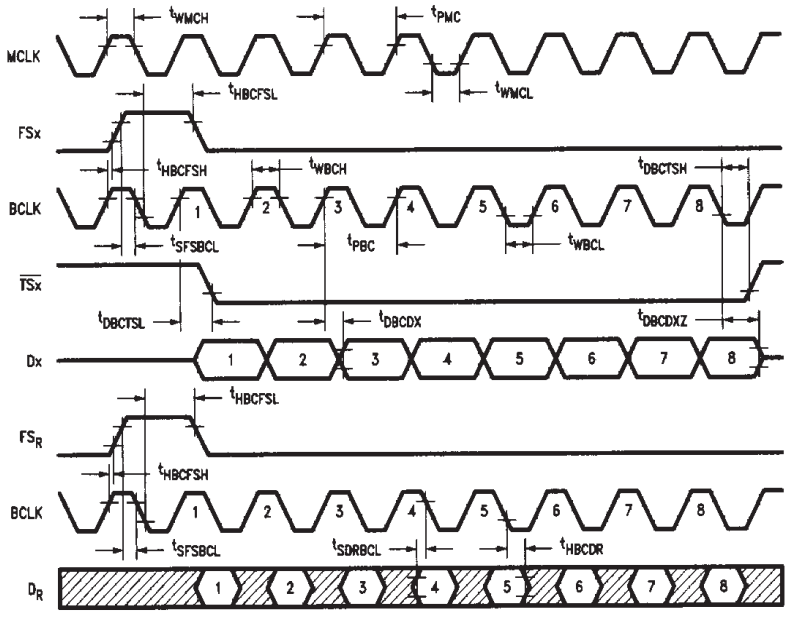

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FIGURE 8. Timing Diagram for Short Frame Mode

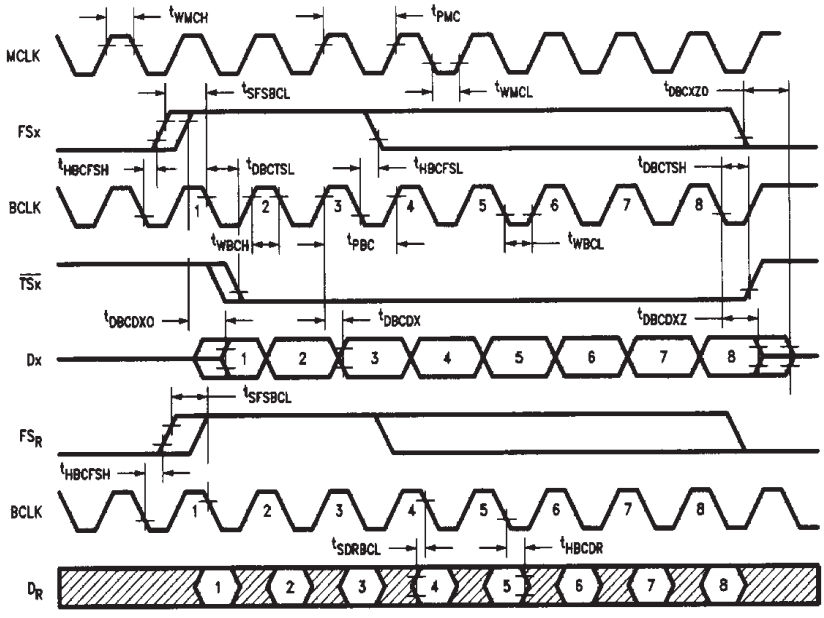

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FIGURE 9. Timing Diagram for Long Frame Mode

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	−0.5V to +7V
V_{BB} to GND	+0.5V to −7V
V_{BAT} to RTN	+0.5V to −70V
RTN to GND	±500V, 10 μs/50 μs Pulse
Voltage at Any Digital Input or Output	V_{CC} + 0.3V to GND − 0.3V
TPR, RPR to RTN	+2V to −85V (50 ms)
TIP, RING, TIPS, RINGS RBUS+, RBUS− to RTN	±1000V, 10 μs/1000 μs Pulse
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Sec)	300°C
Maximum Junction Temperature	150°C

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION (Normal Mode: D2=0, D3=0)						
I_{BAT0}	V_{BAT} Idle Current	I_{Loop} = 0 mA, V_{BAT} = −57V		2.1	**3.2**	mA
I_{BB0}	V_{BB} Idle Current	I_{Loop} = 0 mA		1.9	**3.5**	mA
I_{CC0}	V_{CC} Idle Current	I_{Loop} = 0 mA		2.9	**4.5**	mA
I_{BAT1}	V_{BAT} Active Current	I_{Loop} = 20 mA, V_{BAT} = −57V		23	**25**	mA
I_{BB1}	V_{BB} Active Current	I_{Loop} = 20 mA		8.9	**15.2**	mA
I_{CC1}	V_{CC} Active Current	I_{Loop} = 20 mA		11.8	**15.2**	mA
POWER DISSIPATION (On-Hook Transmission Mode: D2=1, D3=1)						
I_{BAT0H}	V_{BAT} Idle Current	I_{Loop} = 0 mA, V_{BAT} = −57V		2.1	**3.2**	mA
I_{BB0H}	V_{BB} Idle Current	I_{Loop} = 0 mA		8.9	**15.2**	mA
I_{CC0H}	V_{CC} Idle Current	I_{Loop} = 0 mA		11.8	**15.2**	mA
DIGITAL INTERFACE (Note 1)						
V_{IL}	Input Low Level				**0.7**	V
V_{IH}	Input High Level	All Digital Inputs except CLKSEL CLKSEL	**2** **4**			V V
V_{OL}	Output Low Level	Dx, $\overline{TSx}$, CO, I_L = 3.2 mA $\overline{INTR}$, I_L = 2.0 mA			**0.4** **0.4**	V V
V_{OH}	Output High Level	Dx, CO, I_H = −3.2 mA	**2.4**			V
I_{IL}	Input Low Current	GND < V_{IN} < V_{IL}, All Digital Inputs	**−100**		**100**	μA
I_{IH}	Input High Current	V_{IH} < V_{IN} < V_{CC}, All Digital Inputs	**−100**		**100**	μA
I_{OH}	Output High Current	$\overline{TSx}$ and $\overline{INTR}$, V_{OH} < V_{OUT} < V_{CC}	**−100**		**100**	μA
I_{OZ}	Output Current in the High Impedance State (TRI-STATE)	CO, Dx	**−100**		**100**	μA

Note 1: See Appendix I for the definition of digital interface parameters.

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BATTERY FEED						
I_{Loop+}	Loop Current	R_{Loop} = 1900Ω, V_{BAT} = −55V R_{Loop} = 1300Ω, V_{BAT} = −57V R_{Loop} = 200Ω, V_{BAT} = −59V V_{BB} = −5V ±5%	**21** **27** **40**	 43	**24** **33** **46**	mA mA mA
I_{Loop-}	Reverse Loop Current	R_{Loop} = 1900Ω, V_{BAT} = −55V R_{Loop} = 1300Ω, V_{BAT} = −57V R_{Loop} = 200Ω, V_{BAT} = −59V V_{BB} = −5V ±5%	**20** **26** **38**	 43	**25** **34** **46**	mA mA mA
I_{PD}	Power Denial Loop Current	R_{Loop} = 200Ω		0.1	**2**	mA
V_{Loop}	Loop Voltage	R_{Loop} = 10 kΩ		−46.8		V
LOOP SUPERVISION						
Roffhk0	Loop Resistance to Produce an Off-Hook Indication at Loop Start	Roffhk0 Connected from TIP to RING, V_{BAT} = −55V			**2400**	Ω
Ronhk0	Loop Resistance to Produce an On-Hook Indication at Loop Start	Ronhk0 Connected from TIP to RING, V_{BAT} = −59V	**9**			kΩ
Roffhk1	Loop Resistance to Produce an Off-Hook Indication at Ground Start	Roffhk1 Connected from RING to RTN, TIP Open V_{BAT} = −55V			**2450**	Ω
Ronhk1	Loop Resistance to Produce an On-Hook Indication at Ground Start	Ronhk1 Connected from RING to RTN, TIP Open V_{BAT} = −59V	**9**			kΩ
DPD	Dial Pulse Distortion	R_{Leak} = 10 kΩ ‖ (5 kΩ + 2.16 μF) R_{Loop} = 200Ω, 12 pps, Break = 64% R_{Loop} = 1900Ω, 12 pps, Break = 64% $\overline{CS}$ High, Measure Width of Make Period at $\overline{INTR}$	 **25** **25**		 **58** **58**	 ms ms
RING SUPERVISION						
RNGTRP1	Ring Trip Detect, Normal Ringing	RBUS+ = 0V, RBUS− = −48V TIPS = −4.70V, RINGS = −43.3V, Must Detect Ring-Trip within the Specified Time	**50**		**180**	ms
RNGTRP2	Ring Trip Detect, Reverse Ringing	RBUS+ = −48V, RBUS− = 0V, TIPS = −43.3V, RINGS = −4.7V, Must Detect Ring-Trip within the Specified Time	**50**		**180**	ms

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RING SUPERVISION (Continued)						
RNGTRP3	Ring Trip Non-Detect Normal Ringing	RBUS+ = 0V, RBUS− = −48V, TIPS = −3.25V, RINGS = −44.75V, Must Not Detect Ring-Trip within the Specified Time (Note 2)	**0**		**180**	ms
RNGTRP4	Ring Trip Non-Detect Reverse Ringing	RBUS+ = −48V, RBUS− = 0V, TIPS = −44.75V, RINGS = −3.25V, Must Not Detect Ring-Trip within the Specified Time (Note 2)	**0**		**180**	ms
RNGTRP5	Ring Trip Detect, Normal Ringing	TIPS, RBUS− = −4.7V, RINGS, RBUS+ = 17 Vrms, f = 20 Hz, Must Detect Ring-Trip within the Specified Time	**100**		**190**	ms
RNGTRP6	Ring Trip Detect Reverse Ringing	TIPS, RBUS− = 17 Vrms, RINGS, RBUS+ = −4.7V, f = 20 Hz, Must Detect Ring-Trip within the Specified Time	**100**		**190**	ms
RNGTRP7	Ring Trip Non-Detect Normal Ringing	TIPS, RBUS− = −3.25V, RINGS, RBUS+ = 17 Vrms, f = 20 Hz, Must Not Detect Ring-Trip within the Specified Time (Note 2)	**0**		**190**	ms
RNGTRP8	Ring Trip Non-Detect Reverse Ringing	TIPS, RBUS− = 17 Vrms, RINGS, RBUS+ = −3.25V, f = 20 Hz, Must not Detect Ring-Trip within the Specified Time (Note 2)	**0**		**190**	ms
HYBRID BALANCE Unless otherwise specified, I_{Loop} = 20 mA, D2=0, D3=0						
ECHO1	4-Wire Return Loss	Z_{REF} = 900Ω across Tip-Ring D1 = 0, D0 = 0 f = 203.125 Hz = 484.375 Hz = 1015.625 Hz = 2500 Hz = 3406.25 Hz	 **21** **26** **26** **26** **21**	 40 	 	 dB dB dB dB dB
ECHO2	4-Wire Return Loss	Z_{REF} = 1650Ω ‖ (100Ω + 0.005 μF) D1 = 0, D0 = 1 f = 203.125 Hz = 484.375 Hz = 1015.625 Hz = 2500 Hz = 3406.25 Hz	 **21** **26** **26** **26** **21**	 40 	 	 dB dB dB dB dB
ECHO3	4-Wire Return Loss	Z_{REF} = 800Ω ‖ (100Ω +0.05 μF) D1 = 1, D0 = 0 f = 203.125 Hz = 484.375 Hz = 1015.625 Hz = 2500 Hz = 3406.25 Hz	 **21** **26** **26** **26** **21**	 40 	 	 dB dB dB dB dB

Note 2: The intent of Ring Trip Non-Detect tests are to ensure that ring does not occur under the specified conditions even after an essentially infinite period of time. For practical purposes of cost effectively testing the SLIC Subscriber Line Interface Module, the wait time to determine that a false ring trip has not occurred has necessarily been limited to a value which has been determined through characterization to ensure that false ring trip never occurs.

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
HYBRID BALANCE (Continued)						
ECHO4	4-Wire Return Loss	Z_{REF} = 900Ω + 2.16 µF D1 = 1, D0 = 1				
		f = 203.125 Hz	**21**			dB
		= 484.375 Hz	**26**			dB
		= 1015.625 Hz	**26**	40		dB
		= 2500 Hz	**26**			dB
		= 3406.25 Hz	**21**			dB
TRANSMISSION Unless Otherwise Noted, Z_{REF} = 900Ω + 2.16 µF, f = 1015.625 Hz, I_{Loop} = 20 mA, D2 = 0, D3 = 0						
RTNLOSS	2-Wire Return Loss	f = 203.125 Hz	**21**			dB
		= 484.375 Hz	**27**			dB
		= 1015.625 Hz	**27**	40		dB
		= 2500 Hz	**27**			dB
		= 3406.25 Hz	**27**			dB
0 dBmO	The Absolute 2-Wire Reference Level	The Absolute Reference Level at at the 2-Wire Interface is Defined as 0 dBm into 900Ω.		0.949		Vrms
GRA	Absolute Receive Gain	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −56V, f = 1015.625 Hz, T_A = +25°C, Input = Digital Code for 0 dBm0 at D_R, Measure Voltage across TIP-RING.	**−0.35**	−0.1	**0.15**	dB
GXA	Absolute Transmit Gain	V_{CC} = 5V, V_{BB} = −5V V_{BAT} = −56V, f = 1015.625 Hz, T_A = +25°C, Input = 0 dBm0 at 2-Wire Port, Measure Digital Code at Dx.	**−0.35**	−0.1	**0.15**	dB
GRA0H	Absolute Receive Gain at On-Hook Transmission Mode	V_{CC} = 5V, V_{BB} = −5V V_{BAT} = −56V, T_A = +25°C, Z_{REF} = 900Ω + 2.16 µF I_{Loop} = 0 mA, D2=1, D3=1	**−1.1**	−0.1	**0.9**	dB
GXA0H	Absolute Transmit Gain at On-Hook Transmission Mode	V_{CC} = 5V, V_{BB} = −5V V_{BAT} = −56V, T_A = +25°C, I_{Loop} = 0 mA, D2=1, D3=1	**−1.1**	−0.1	**0.9**	dB
GRAV	Absolute Receive Gain over Supply Range	V_{CC} = 5V ±5%, V_{BB} = −5V ±5% V_{BAT} = −55V to −59V, f = 1015.625 Hz	**−0.4**	−0.1	**0.2**	dB
GXAV	Absolute Transmit Gain over Supply Range	V_{CC} = 5V ±5%, V_{BB} = −5V ±5% V_{BAT} = −55V to −59V, f = 1015.625 Hz	**−0.4**	−0.1	**0.2**	dB
GRT	Receive Gain Variation over Temperature	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −56V, f = 1015.625 Hz Reference to GRA	−0.1		0.1	dB
GXT	Transmit Gain Variation over Temperature	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −56V, f = 1015.625 Hz Reference to GXA	−0.1		0.1	dB

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMISSION Unless Otherwise Noted, Z_{REF} = 900Ω + 2.16 μF, f = 1015.625 Hz, I_{Loop} = 20 mA, D2=0, D3=0 (Continued)						
GRF	Receive Frequency Response	Measure Relative to GRA,				
		f = 203.125 Hz	**−1.9**		**0**	dB
		= 296.875 Hz	**−0.4**		**0.25**	dB
		= 484.375 Hz	**−0.25**		**0.25**	dB
		= 2015.625 Hz	**−0.25**		**0.25**	dB
		= 2703.125 Hz	**−0.25**		**0.25**	dB
		= 3015.625 Hz	**−0.25**		**0.25**	dB
		= 3203.125 Hz	**−0.25**		**0.25**	dB
		= 3390.625 Hz	**−1.2**		**0**	dB
		= 3984.375 Hz			**−14**	dB
SOS	Spurious Out of Band Signals (Alias Tones)	Measure Relative to GRA,				
		f = 4796.75 Hz			**−30**	dB
		= 6703.125 Hz			**−30**	dB
		= 11390.625 Hz			**−30**	dB
GXF	Transmit Frequency Response	Measure Relative to GXA,				
		f = 62.500 Hz			**−21**	dB
		= 203.125 Hz	**−2.5**		**0**	dB
		= 296.875 Hz	**−0.4**		**0.25**	dB
		= 484.375 Hz	**−0.25**		**0.25**	dB
		= 2015.625 Hz	**−0.25**		**0.25**	dB
		= 2703.125 Hz	**−0.25**		**0.25**	dB
		= 3015.625 Hz	**−0.25**		**0.25**	dB
		= 3203.125 Hz	**−0.25**		**0.25**	dB
		= 3390.625 Hz	**−1.2**		**0**	dB
		= 3984.375 Hz			**−14**	dB
		= 5046.875 Hz			**−32**	dB
		= 11890.625 Hz			**−32**	dB
GRL	Receive Gain Variation with Signal Level	Measure Relative to GRA PCM Level				
		= 3.1 dBmO	**−0.25**		**0.25**	dB
		= −2.3 dBmO	**−0.25**		**0.25**	dB
		= −11.4 dBmO	**−0.25**		**0.25**	dB
		= −17.6 dBmO	**−0.25**		**0.25**	dB
		= −23.9 dBmO	**−0.25**		**0.25**	dB
		= −29.9 dBmO	**−0.25**		**0.25**	dB
		= −37.8 dBmO	**−0.25**		**0.25**	dB
		= −47.1 dBmO	**−0.45**		**0.45**	dB
		= −55.7 dBmO	**−1.3**		**1.3**	dB
GXL	Transmit Gain Variation with Signal Level	Measure Relative to GXA PCM Level				
		= 3.1 dBmO	**−0.25**		**0.25**	dB
		= −2.3 dBmO	**−0.25**		**0.25**	dB
		= −11.4 dBmO	**−0.25**		**0.25**	dB
		= −17.6 dBmO	**−0.25**		**0.25**	dB
		= −23.9 dBmO	**−0.25**		**0.25**	dB
		= −29.9 dBmO	**−0.25**		**0.25**	dB
		= −37.8 dBmO	**−0.25**		**0.25**	dB
		= −47.1 dBmO	**−0.45**		**0.45**	dB
		= −55.7 dBmO	**−1.3**		**1.3**	dB

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMISSION Unless Otherwise Noted, Z_{REF} = 900Ω + 2.16 μF, f = 1015.625 Hz, I_{Loop} = 20 mA, D2 = 0, D3 = 0 (Continued)						
STDR	Receive Signal to Total Distortion	Measure through C Message Filter f = 1015.625 Hz, PCM Level				
		= 3.1 dBmO	**33**			dBC
		= 0.0 dBmO	**36**			dBC
		= −2.3 dBmO	**36**			dBC
		= −11.4 dBmO	**36**			dBC
		= −17.6 dBmO	**36**			dBC
		= −23.9 dBmO	**36**			dBC
		= −29.9 dBmO	**35**			dBC
		= −37.8 dBmO	**31**			dBC
		= −40.0 dBmO	**29**			dBC
		= −45.0 dBmO	**25**			dBC
		= −47.1 dBmO	**23**			dBC
		= −55.7 dBmO	**14**			dBC
STDX	Transmit Signal to Total Distortion	Measure through C Message Filter f = 1015.625 Hz, PCM Level				
		= 3.1 dBmO	**33**			dBC
		= 0.0 dBmO	**36**			dBC
		= −2.3 dBmO	**36**			dBC
		= −11.4 dBmO	**36**			dBC
		= −17.6 dBmO	**36**			dBC
		= −23.9 dBmO	**36**			dBC
		= −29.9 dBmO	**35**			dBC
		= −37.8 dBmO	**31**			dBC
		= −40.0 dBmO	**29**			dBC
		= −45.0 dBmO	**25**			dBC
		= −47.1 dBmO	**22**			dBC
		= −55.7 dBmO	**13**			dBC
DRA	Absolute Receive Delay	f = 1600 Hz		190		μs
DRR	Receive Delay Distortion	Measure Relative to DRA, f = 500 Hz		−2		μs
		= 1000 Hz		−10		μs
		= 2600 Hz		70		μs
		= 2800 Hz		100		μs
		= 3000 Hz		150		μs
DXA	Absolute Transmit Delay	f = 1600 Hz		300		μs
DXR	Transmit Delay Distortion	Measure Relative to DXA, f = 500 Hz		250		μs
		= 600 Hz		150		μs
		= 800 Hz		65		μs
		= 1000 Hz		30		μs
		= 2600 Hz		60		μs
		= 2800 Hz		80		μs
		= 3000 Hz		140		μs

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
NOISE Z_{REF} = 900Ω + 2.16 μF, I_{Loop} = 20 mA, D2=0, D3=0						
NRC	Receive C Message Weighted Idle Channel Noise	PCM Code is Alternating Positive and Negative Zeroes		9	**13**	dBrnC0
NXC	Transmit C Message Weighted Idle Channel Noise	Measured by Extrapolation from Signal to Distortion Measurements at −50 dBmO		13	**16**	dBrnC0
POWER SUPPLY REJECTION RATIO Unless Otherwise Specified, Z_{REF} = 900Ω + 2.16 μF, I_{Loop} = 20 mA, D2=0, D3=0						
$PPSR_R$	V_{CC} Power Supply Rejection, Receive	f = 328.125 Hz f = 1078.125 Hz f = 3328.125 Hz	**30** **30** **30**			dB dB dB
$VPSR_R$	V_{BAT} Power Supply Rejection, Receive	f = 328.125 Hz f = 1078.125 Hz f = 3328.125 Hz	**30** **40** **40**			dB dB dB
PPSRx	V_{CC} Power Supply Rejection, Transmit	f = 328.125 Hz f = 1078.125 Hz f = 3328.125 Hz	**30** **30** **30**			dB dB dB
VPSRx	V_{BAT} Power Supply Rejection, Transmit	f = 328.125 Hz f = 1078.125 Hz f = 3328.125 Hz	**30** **40** **40**			dB dB dB
LONGITUDINAL BALANCE AND CAPABILITY						
I_{LLS1}	Longitudinal Current Capability, Loop Start	I_{Loop} = 5 mA, f = 60 Hz, Inject I_{LLS1} into TIP and RING. Device Must Not Detect Off-Hook. Triangular Waveform	**21**			mArms
I_{LLS2}	Longitudinal Current Capability, Loop Start	I_{Loop} = 21 mA, f = 60 Hz, Inject I_{LLS2} into TIP and RING. Device Must Not Detect On-Hook. Triangular Waveform	**21**			mArms
I_{LGS1}	Longitudinal Current Capability, Ground Start	f = 60 Hz, I_{Ground} = 0 mA Triangular Waveform. Inject I_{LGS1} into RING, TIP Open. Device Must Not Detect Off-Hook	**8.5**			mArms
I_{LGS2}	Longitudinal Current Capability, Ground Start	I_{Ground} = 50 mA, f = 60 Hz. Inject I_{LGS2} into RING, TIP Open. Device Must Not Detect On-Hook. Triangular Waveform	50			mArms
BAL2W	2-Wire Longitudinal Balance	IEEE Method 455-1976, I_{Loop} = 20 mA, $I_{Longitudinal}$ = 20 mArms/leg, Measure $V_{metallic}$ across TIP-RING f = 62.5 Hz = 203.125 Hz = 1015.625 Hz = 2015.625 Hz = 2703.125 Hz = 3000 Hz = 3406.25 Hz	 **61** **61** **61** **61** **56** **54** **51**	 64 64 59 	 	 dB dB dB dB dB dB dB

1-157

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Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LONG FRAME SYNC MODE *(Figure 9)*						
t_{HBCFSH}	Hold Time from BCLK Low to FS		**0**			ns
t_{SFSBC0}	Setup Time from FS to BCLK Low		**80**			ns
t_{WFSL}	Width of FS Low		**160**			ns
t_{DBCDX0}	Delay Time from BCLK or FS, Whichever Comes Later to Dx Valid	C_L = 150 pF Plus 2 LSTTL Loads	**20**		**165**	ns
t_{DBCDX}	Delay Time from BCLK to Dx Valid	C_L = 150 pF Plus 2 LSTTL Loads	**0**		**140**	ns
t_{DBCDXz}	Delay Time from BCLK to Dx Disabled	C_L = 50 pF	**50**		**165**	ns
$t_{DBCDXz0}$	Delay Time from BCLK or FS, Whichever Comes Later, to Dx Disabled	C_L = 50 pF	**20**		**165**	ns
t_{SDRBC}	Setup Time from D_R to BCLK Low		**50**			ns
t_{HBCDR}	Hold Time from BCLK Low to D_R Valid		**50**			ns
DIGITAL TIMING, SERIAL CONTROL INTERFACE (See *Figures 2* and *3*, Notes 4 and 5)						
$1/t_{PCC}$	CCLK Frequency	Frequency Accuracy < ±100 ppm	0.08		**2.048**	MHz
t_{WCCH}	Width of CCLK High		**200**			ns
t_{WCCL}	Width of CCLK Low		**200**			ns
t_{WCSL}	Width of $\overline{CS}$ Low				**100**	µs
READ/WRITE, WRITE READ MODES *(Figure 2)*						
t_{HCCCS}	Hold Time from CCLK to $\overline{CS}$		**100**			ns
t_{SCSCC}	Setup Time from $\overline{CS}$ to CCLK		**100**			ns
t_{DCCCO}	Delay Time from CCLK or $\overline{CS}$, Whichever Comes Later, to CO Valid	C_L = 150 pF Plus 2 LSTTL Loads			**150**	ns
t_{DCCCOZ}	Delay Time from CCLK or $\overline{CS}$, Whichever Comes Later, to CO Disabled				**150**	ns

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
READ/WRITE, WRITE READ MODES *(Figure 2)* (Continued)						
t_{SCCCI}	Setup Time from CI to CCLK		**100**			ns
t_{HCICC}	Hold Time from CCLK to CI		**100**			ns
t_{DCSIN}	Delay Time from $\overline{CS}$ Low to $\overline{INTR}$ High	R_L = 1 kΩ from $\overline{INTR}$ to V_{CC}			**200**	ns
QUICK STATUS READ MODE *(Figure 3)*						
t_{HCCCSL}	Hold Time from CCLK to $\overline{CS}$ Low		**100**			ns
t_{SCSCCL}	Setup Time from $\overline{CS}$ to CCLK Low		**100**			ns
t_{DCSCO}	Delay Time from $\overline{CS}$ to CO Valid	C_L = 150 pF Plus 2 LSTLL Loads			**150**	ns
t_{DCSCOZ}	Delay Time from $\overline{CS}$ to CO Disabled				**150**	ns

Note 4: See Appendix I for the definition and naming conventions used for digital timing parameters.

Note 5: See Table V for the definition of the mneumonics used for the digital timing parameters.

TABLE V. Timing Parameter Mneumonics

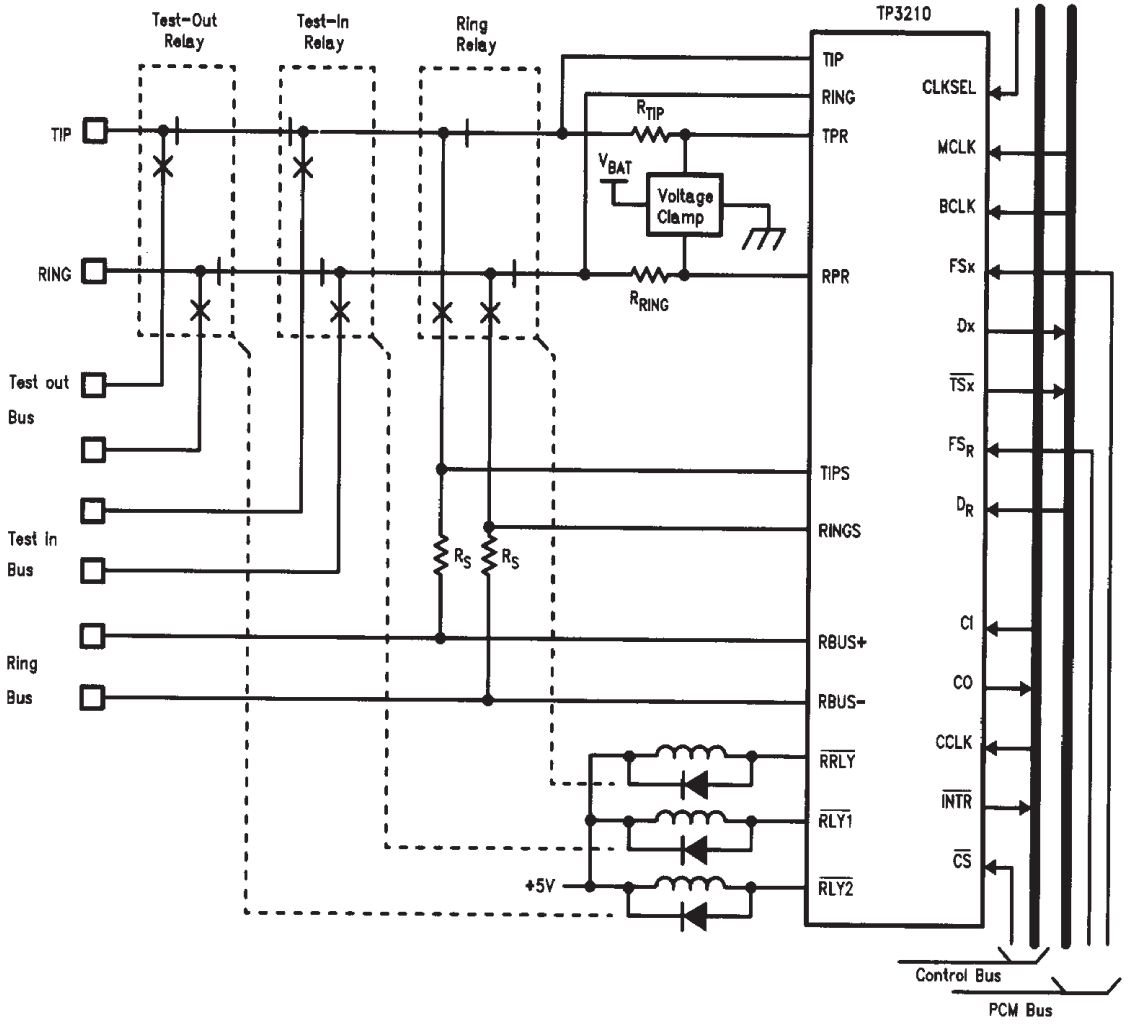
Pin Name	Mneumonic
$\overline{INTR}$	IN
$\overline{CS}$	CS
CO	CO
CI	CI
CCLK	CC
MCLK	MC
BCLK	BC
D_R	DR
Dx	DX
$\overline{TSx}$	TS
FS_R	FS
FSx	FS

Applications Information

Typical Line Circuit

Relatively few external components are required to implement a full featured central office line circuit. As shown in *Figure 10*, a complete line circuit is implemented using TP3210 with an external protection network consisting of fuse resistors R_{TIP} and R_{RING}, and a voltage clamp device, two 360Ω ring sensing resistors, a ring relay and two test relays. It should be noted that no supply decoupling capacitors are required for each line circuit at ±5V supplies, although the use of one larger electrolytic capacitor may be advisable for each power supply near the point at which it enters the line card.

Protection resistors R_{TIP} and R_{RING} should be nominally 100Ω matched to within ±1%. The selection of these protection resistors is important because they are fundamental to the ability of the line circuit to meet lightning and power cross requirements. R_{TIP} and R_{RING} should be designed such that they can withstand level one lightning and power cross requirements, while fusing open when over-stressed by level two lightning and power cross. TPR and RPR are protected by an external voltage clamp device to limit the voltage at these two pins to within +2 to −85V. The ring sensing resistors, R_S are 360Ω which sets the ring trip threshold to about 11 mAdC. The heavy relay current will be returned to GND3 at pin 26.



TL/H/9422–11

FIGURE 10. Complete Central Office Line Circuit

Applications Information (Continued)

Secondary Protection

The surge protection network in *Figure 10* consists of resistors R_{TIP}, R_{RING} and a voltage limiting circuit which limits the voltage at TPR and RPR. A number of low cost possibilities for this voltage limit are shown in *Figure 11*. The lowest cost solution is a simple full wave rectifier diode bridge used to clamp the voltage to no more than one or two volts above RTN or below V_{BAT}, provided that the V_{BAT} supply is capable to absorb the power surges. The TIP and RING input terminals of the TP3210 are internally connected in series to two 300 kΩ thick film resistors, which are capable to withstand power cross and surges.

Typical Line Card

A complete N-channel line card is illustrated in *Figure 12*. The backplane control interfaces vary greatly in different applications, and this example illustrates a possible arrangement.

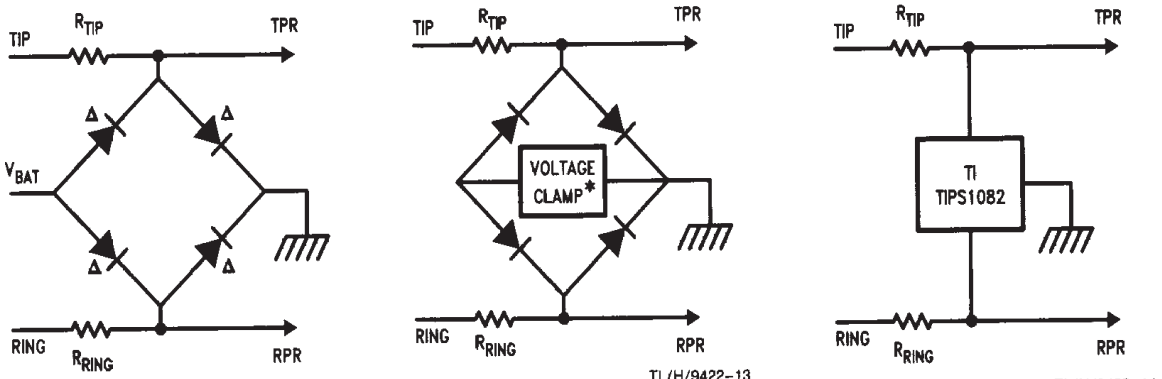


FIGURE 11. Some Secondary Protection Networks

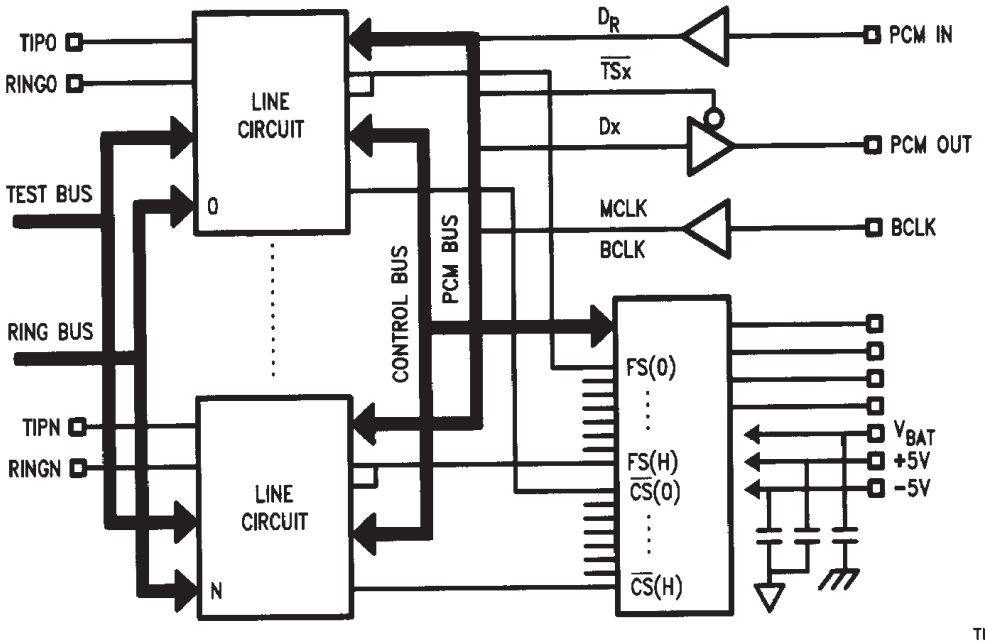


FIGURE 12. Typical N-Channel Linecard

Submission III

Type	Reference	Title
Patent	US 5973516	Transient Signal Detector with Temporal Hysteresis
Citations	**4**	

US005973516A

United States Patent [19]

Bremner et al.

[11] **Patent Number: 5,973,516**

[45] **Date of Patent: Oct. 26, 1999**

[54] **TRANSIENT SIGNAL DETECTOR WITH TEMPORAL HYSTERESIS**

[75] Inventors: **Duncan James Bremner**, Lochwinnoch, United Kingdom; **Ray Allen Reed**, San Jose, Calif.

[73] Assignee: **National Semiconductor Corporation**, Santa Clara, Calif.

[21] Appl. No.: **09/139,011**

[22] Filed: **Aug. 24, 1998**

[51] **Int. Cl.**[6] **H03K 5/153**

[52] **U.S. Cl.** **327/74**; 327/24; 327/205

[58] **Field of Search** 327/24, 68, 71, 327/74, 75, 76, 87, 205, 206

[56] **References Cited**

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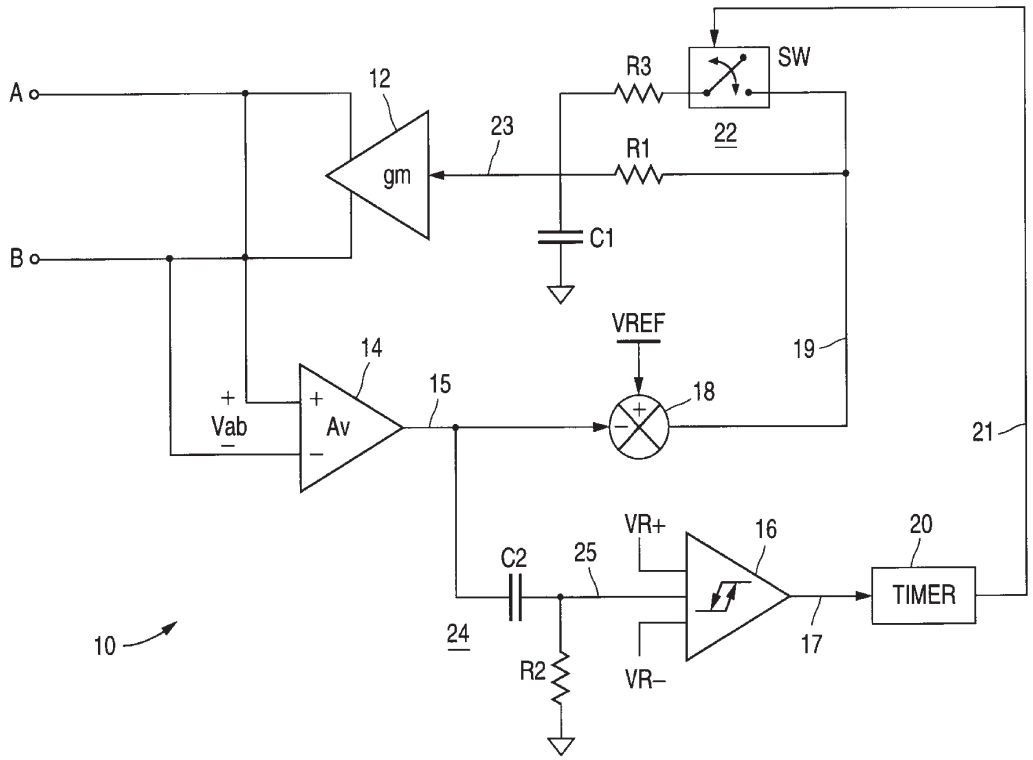
Primary Examiner—Timothy P. Callahan
Assistant Examiner—An T. Luu
Attorney, Agent, or Firm—Limbach & Limbach L.L.P.

[57] **ABSTRACT**

A subscriber line interface circuit which includes a transient signal detector with temporal hysteresis. During steady state operation, the drive current for the subscriber loop allows the loop to respond to changes in loop conditions according to a steady state time constant of the loop filter. Upon detection of a line voltage transient which exceeds a predetermined threshold in either a positive or negative direction, the filter time constant is significantly reduced (e.g., 100:1) and held at such reduced value following the initial transient and for a predetermined time period after the line voltage has fallen back below such predetermined threshold. This allows the transient conditions to be fully compensated prior to resetting the filter time constant back from the lower transient value to the higher steady state value.

22 Claims, 2 Drawing Sheets



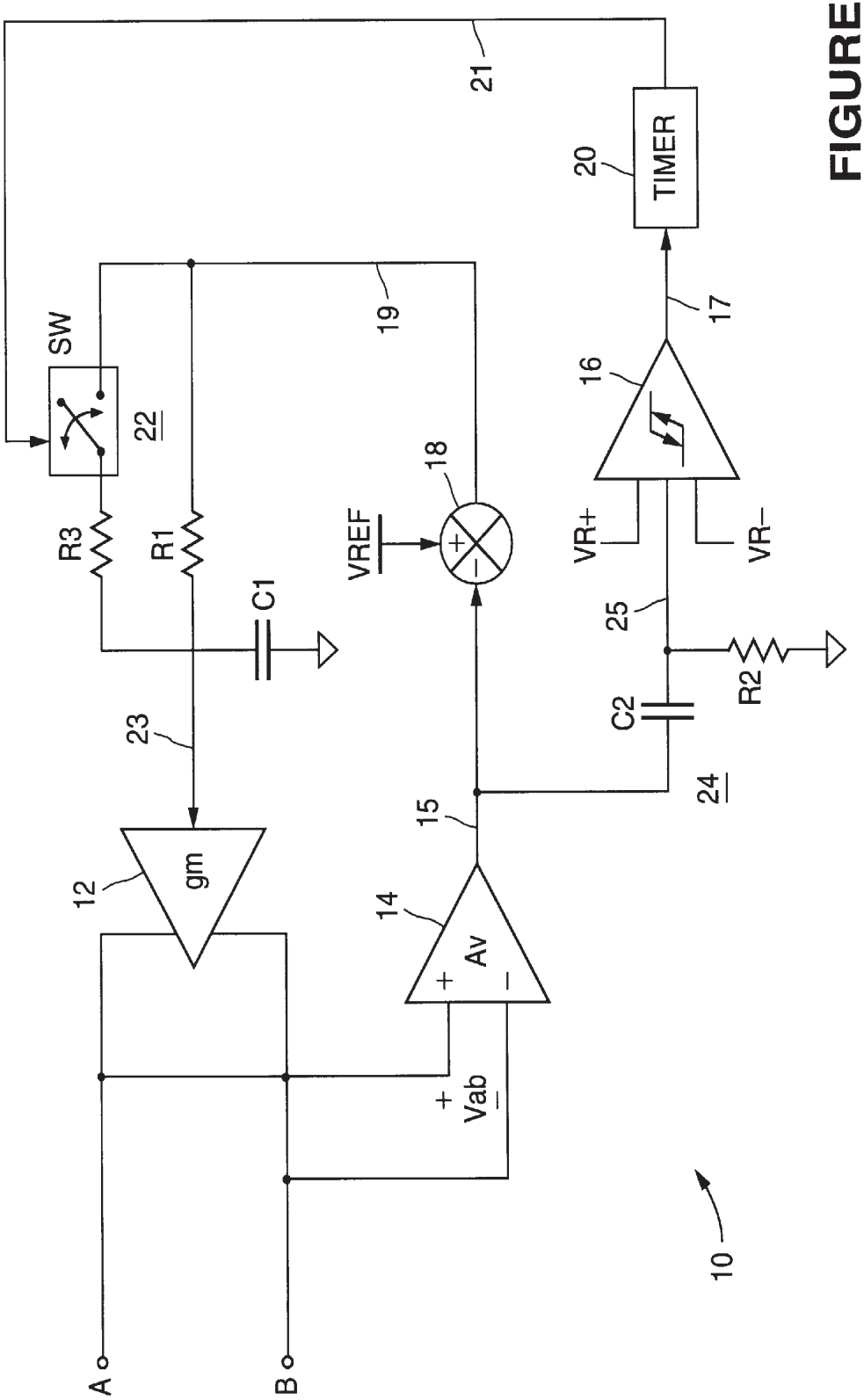

21
20
TIMER
SW
22
19
17
16
18
VREF
VR+
VR–
R3
R1
C1
25
R2
C2
24
23
15
12
gm
14
Av
Vab
A
B
10

FIGURE 1

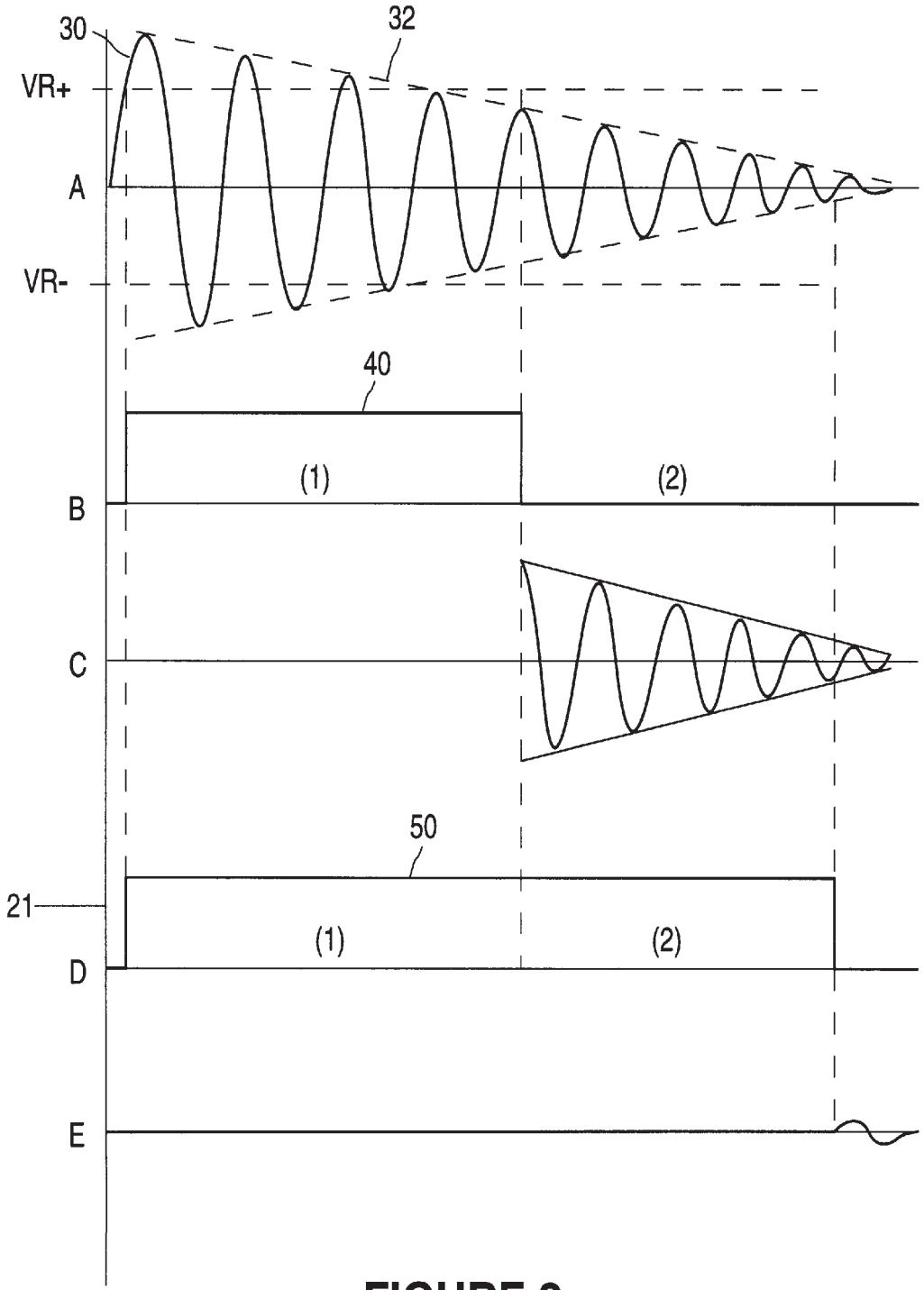


FIGURE 2

TRANSIENT SIGNAL DETECTOR WITH TEMPORAL HYSTERESIS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to transient signal detectors, and in particular, transient signal detectors for use with subscriber line interface circuits for detecting and compensating transient signals while allowing such transient signals to settle.

2. Description of the Related Art

Many types of circuits require some form of transient signal detection whereby signals within the monitored signal path which exceed some predetermined voltage threshold, and which are frequently transient in nature, can be reliably detected. Rapid and reliable detection of such signals allows such circuits to then either filter out or attempt to compensate or suppress such transient signals.

One such type of circuit is that of a subscriber line interface circuit (SLIC) for telecommunications. Signal transients in a telecommunications environment are quite common. For example, aside from any transient signals introduced by the operating environment (e.g., electrical motors, lightning strikes, ground loops, etc.), transient signals due to transitions between on-hook and off-hook conditions and normal dialing impulses caused by older rotary telephones are often encountered. In many applications such transient signals can cause the circuit operation to become, at best, unreliable and, at worst, fail.

Conventional transient signal detectors generally rely upon the detection of the level, or magnitude, of the transient signal. Typically, when the transient signal magnitude exceeds some predefined threshold, the transient detector indicates the presence of the transient signal, and continues to do so for as long as the transient level remains higher than the threshold. Once the transient signal decreases back below such threshold, the transient detector changes state to indicate that the transient signal has terminated. However, since the threshold value at which the transient detector switches between its positive and negative transient indication states has a non-zero value, even when the transient signal has fallen below such threshold and the transient detector indicates that the transient signal has terminated, the transient signal nonetheless remains, albeit at a reduced level, for some period of time until it actually settles out, or decays, completely. In other words, a positive indication of the presence of a transient signal in a conventional transient signal detector lasts only as long as the transient signal exceeds the predefined threshold, and once the transient signal ceases to exceed such threshold, albeit with some amount of magnitude-dependent hysteresis, it is then identified as having settled when, in fact, some residual amount of transient signal energy remains for some period of time thereafter.

Accordingly, it would be desirable to have a transient signal detector which, notwithstanding a significant reduction in magnitude of the transient signal, maintains a positive indication of the presence of a transient signal for a period of time sufficient to allow the transient signal to more completely settle out.

SUMMARY OF THE INVENTION

A transient signal detector in accordance with the present invention uses both a magnitude detector and a time delay element to maintain a positive indication of a transient signal, thereby allowing the transient signal to settle out more completely before such transient signal becomes identified as having ended.

In accordance with one embodiment of the present invention, a transient signal detector with temporal hysteresis for a subscriber line interface circuit includes a driver circuit, a monitoring circuit and a control circuit. The driver circuit is configured to connect to a subscriber line and receive a drive control signal and in accordance therewith provide to the subscriber line an adjustable line current which varies in relation to the drive control signal. The monitoring circuit is configured to connect to and monitor a voltage on the subscriber line and in accordance therewith provide a monitor signal which varies in relation to the subscriber line voltage. The control circuit is coupled to the monitoring circuit and the driver circuit, and is configured to receive the monitor signal and in accordance therewith provide the drive control signal such that the control circuit provides the drive control signal in accordance with the monitor signal while using: one transfer function following when the monitor signal indicates that the subscriber line voltage has extended outside of a range of voltages defined by upper and lower range limits and for a predetermined time period after the monitor signal indicates that the subscriber line voltage has returned inside of the range of voltages; and another transfer function otherwise.

In accordance with another embodiment of the present invention, a method of detecting and responding with temporal hysteresis to transient signals on a subscriber line includes the steps of:

connecting to a subscriber line;

receiving a drive control signal and in accordance therewith generating in the subscriber line an adjustable line current which varies in relation to the drive control signal;

monitoring a voltage on the subscriber line and in accordance therewith generating a monitor signal which varies in relation to the subscriber line voltage; and

generating the drive control signal in accordance with the monitor signal while using

one transfer function following when the monitor signal indicates that the subscriber line voltage has extended outside of a range of voltages defined by upper and lower range limits and for a predetermined time period after the monitor signal indicates that the subscriber line voltage has returned inside of the range of voltages, and

another transfer function otherwise.

In accordance with still another embodiment of the present invention, a subscriber line interface circuit which includes a transient signal detector with temporal hysteresis includes a transconductance amplifier, a sense amplifier, a subtraction circuit, an adjustable filter and a transient detector. The transconductance amplifier is configured to connect to a subscriber line and receive a drive voltage and in accordance therewith provide to the subscriber line an adjustable line current which varies in relation to the drive voltage. The sense amplifier is configured to connect to and sense a voltage on the subscriber line and in accordance therewith provide a sense signal which varies in relation to the subscriber line voltage. The subtraction circuit is coupled to the sense amplifier and is configured to receive a reference signal and the sense signal and in accordance therewith provide a difference signal which indicates a difference between the reference and sense signals. The adjustable filter includes first and second associated filter time constants, is

coupled to the subtraction circuit and the transconductance amplifier, and is configured to receive a control signal with first and second control signal states and in accordance therewith receive and filter the difference signal and in accordance therewith provide the drive voltage such that the difference signal is filtered in accordance with the first and second associated filter time constants when the control signal is in the first and second control signal states, respectively. The transient detector is coupled to the subtraction circuit and the adjustable filter, and is configured to receive the sense signal and in accordance therewith provide the control signal which is: in the first control signal state following when the sense signal indicates that the subscriber line voltage has extended outside of a range of voltages defined by upper and lower range limits and for a predetermined time period after the sense signal indicates that the subscriber line voltage has returned inside of the range of voltages; and in the second control signal state otherwise.

These and other features and advantages of the present invention will be understood upon consideration of the following detailed description of the invention and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram of a transient signal detector with temporal hysteresis in accordance with one embodiment of the present invention.

FIG. **2** is a set of signal waveforms and timing diagrams comparing the operation of the circuit of FIG. **1** to a conventional transient signal detector.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. **1**, a transient signal detector **10** with temporal hysteresis for a subscriber line interface circuit in accordance with one embodiment of the present invention uses a closed loop circuit topology which includes a transconductance amplifier **12**, a sense amplifier **14**, a bipolar signal comparator **16**, a subtractor **18**, a timer circuit **20**, a controllable low-pass filter **22** and a high-pass filter **24**, all interconnected substantially as shown. Each of these elements individually is well known in the art and can be implemented in accordance with a number of conventional design techniques.

The subscriber wire pair is connected at nodes A and B which, in turn, are connected to a subscriber instrument, such as a telephone (not shown). The transconductance amplifier **12**, with a gain of gm, amplifies its single-ended, low-pass filtered input voltage **23** to provide a nominal differential line current to nodes A and B. The resulting differential voltage Vab is monitored by the sense amplifier **14**, with a gain of Av, to produce a monitor signal **15** which varies in relation to the subscriber line voltage Vab.

This monitor signal **15** is compared to a reference voltage Vref in the subtractor **18**. The resulting comparison signal **19**, which represents the difference between the monitor signal **15** and the voltage reference Vref, is low-pass filtered by the low-pass filter **22**. In normal, or non-transient, operating mode, the time constant T1 of the low-pass filter **22** is defined by its capacitance C1 and primary resistance R1 (T1=R1*C1). This time constant is normally very high, i.e., the bandwidth of the low-pass filter **22** is normally very low (e.g., 1.5 Hertz) to prevent impacting the voice transmission path in the subscriber loop. When no current is demanded from the subscriber loop, the monitor signal **15** is equal to the voltage reference Vref. As noted above, the resulting low-pass filtered signal **23** drives the transconductance amplifier **12**.

The monitor signal **15** is also high-pass filtered by the high-pass filter **24**. The time constant T2 of the high-pass filter **24** is defined by its capacitance C2 and resistance R2 (T2=R2*C2). The resulting high-pass filtered signal **25** is compared against two voltage references VR+, VR− in the bipolar comparator **16**. When the high-pass filtered signal **25** indicates that the transient level of the subscriber line voltage Vab exceeds a predetermined threshold in either a positive or negative direction, as defined by the positive VR+ and negative VR− reference voltages, respectively, a logic signal **17** is asserted which starts the timer circuit **20**. The timer circuit **20** (e.g., a monostable multivibrator) generates a timing control signal **21** which has a predetermined timed duration pulse length, as discussed in more detail below.

This timing control signal **21**, when asserted and de-asserted, causes the switch SW in the low-pass filter **22** to close and open, respectively. When the switch SW is closed, the time constant T1 of the low-pass filter **22** is reduced due to the reduced resistance of the combination of resistances R1 and R3 connected in parallel.

During steady-state operation, the loop **10** responds to changes in subscriber loop conditions, as reflected in the subscriber loop voltage Vab, according to the primary time constant T1 (=R1 *C1) of the low-pass filter **22**. However, if a rapid change in the subscriber loop voltage Vab is detected, such as that which might occur during off-hook or dial pulse make/break transitions, the transient detector **10** recognizes the fast transition using the high-pass filter **24** and signal comparator **16**. This causes the timer circuit **20** to be triggered which, in turn, reduces the loop time constant by connecting the secondary resistance R3 in shunt with the primary resistance R1 of the low-pass filter **22**. This reduced loop time constant allows the circuit **10** to react more quickly for compensating, or suppressing, the transient condition in the subscriber loop.

As discussed in more detail below, the effect of using the timer circuit **20** is to maintain the reduced time constant following a substantial decrease from the initial magnitude of the transient, thereby allowing the transient to be brought under control virtually completely before returning the loop to its original, higher time constant. (For example, in one application, this time duration for maintaining the reduced loop time constant is approximately 7 milliseconds after the transient level has been detected as being brought within the non-detect range of the signal comparator **16**.) Accordingly, the "hold" time for the reduced loop time constant is "stretched" beyond that of conventional techniques which rely merely upon detection and reaction to the magnitude of the transient signal.

Referring to FIG. **2**, operation of the circuit **10** of FIG. **1** can perhaps be better understood by discussing its operation in view of a transient signal **30** having a signal envelope **32** as shown in waveform A. As shown in waveform A, the transient signal **30** starts with a peak amplitude and gradually decays, or settles, to zero over time. The successive peaks of the transient signal **30** define a transient signal envelope **32**. Waveform B illustrates the asserted state **40** of a conventional transient detector which relies solely on magnitude detection. As is shown, during time period (1), i.e., so long as the peaks of the transient signal **30** extend beyond the positive VR+ and negative VR− thresholds, plus some magnitude-dependent hysteresis, the conventional transient detector provides a positive indication **40** of the presence of the transient signal **30**. However, during time period (2), i.e., following when the peaks of the transient signal **30** have returned to within the reference voltage

range, the conventional transient signal detector provides a negative indication of the presence of a transient signal, thereby causing transient compensation, or suppression, operations to be terminated. However, such a termination of transient suppression is premature since, as shown in waveform C, a significant amount of transient signal energy remains in the loop.

Referring to waveform D of FIG. **2**, a transient signal detector with temporal hysteresis in accordance with the present invention provides a positive indication **50** of the presence of the transient signal for a longer period of time, i.e., through time periods (1) and (2). Accordingly, as shown in waveform E, by the time transient signal suppression operation becomes terminated, the transient signal has settled almost completely, thereby leaving only minimal residual offset within the loop when the primary, lower time constant is reinstated.

Based upon the foregoing, it can be seen that the time-dependent hysteresis of a transient signal detector in accordance with the present invention provides significant transient suppression capability over conventional transient signal detectors which rely solely upon magnitude-dependent hysteresis.

Various other modifications and alterations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and spirit of the invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. It is intended that the following claims define the scope of the present invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.

What is claimed is:

1. An apparatus including a transient signal detector with temporal hysteresis for a subscriber line interface circuit, comprising:

a driver circuit configured to connect to a subscriber line and receive a drive control signal and in accordance therewith provide to said subscriber line an adjustable line current which varies in relation to said drive control signal;

a monitoring circuit configured to connect to and monitor a voltage on said subscriber line and in accordance therewith provide a monitor signal which varies in relation to said subscriber line voltage; and

a control circuit, coupled to said monitoring circuit and said driver circuit, configured to receive said monitor signal and in accordance therewith provide said drive control signal, wherein said control circuit provides said drive control signal in accordance with said monitor signal while using

one transfer function following when said monitor signal indicates that said subscriber line voltage has extended outside of a range of voltages defined by upper and lower range limits and for a predetermined time period after said monitor signal indicates that said subscriber line voltage has returned inside of said range of voltages, and

another transfer function otherwise.

2. The apparatus of claim **1**, wherein said driver circuit comprises a transconductance amplifier configured to receive a voltage signal as said drive control signal and in response thereto generate said adjustable line current.

3. The apparatus of claim **1**, wherein said monitoring circuit comprises a differential sense amplifier configured to sense a differential voltage as said monitored subscriber line voltage and in response thereto generate said monitor signal.

4. The apparatus of claim **1**, wherein said control circuit comprises:

a controllable filter circuit configured to receive a filter control signal and in accordance therewith filter said monitor signal and in accordance therewith provide said drive control signal; and

a control signal generator circuit configured to detect transients in said monitor signal and in accordance therewith provide said filter control signal.

5. The apparatus of claim **4**, wherein said controllable filter circuit comprises:

a signal comparison circuit configured to receive and compare a reference signal and said monitor signal and in accordance therewith provide a comparison result signal which indicates a difference between said monitor signal and said reference signal; and

an output filter circuit, coupled to said signal comparison circuit, configured to receive said filter control signal and in accordance therewith receive and filter said comparison result signal and in accordance therewith provide said drive control signal.

6. The apparatus of claim **4**, wherein said control signal generator circuit comprises:

a transient detection circuit configured to detect said monitor signal transients and in accordance therewith provide a transient detection signal; and

a signal comparison circuit, coupled to said transient detection circuit, configured to receive and compare said transient detection signal and at least one reference signal and in accordance therewith provide said filter control signal which is

in one signal state following when said transient detection signal indicates that said subscriber line voltage has extended outside of a range of voltages defined by upper and lower range limits and for a predetermined time period after said transient detection signal indicates that said subscriber line voltage has returned inside of said range of voltages, and

in another signal state otherwise.

7. The apparatus of claim **6**, wherein said transient detection circuit comprises a high-pass filter circuit configured to high-pass filter said monitor signal and in accordance therewith provide said transient detection signal.

8. The apparatus of claim **6**, wherein said signal comparison circuit comprises:

a bipolar comparator circuit configured to receive first and second reference signals as said at least one reference signal and to compare said transient detection signal with said first and second reference signals and in accordance therewith provide a comparison result signal; and

a timer circuit, coupled to said bipolar comparator circuit, configured to receive said comparison result signal and in accordance therewith provide said filter control signal.

9. A method of detecting and responding with temporal hysteresis to transient signals on a subscriber line, comprising the steps of:

connecting to a subscriber line;

receiving a drive control signal and in accordance therewith generating in said subscriber line an adjustable line current which varies in relation to said drive control signal;

monitoring a voltage on said subscriber line and in accordance therewith generating a monitor signal which varies in relation to said subscriber line voltage; and

generating said drive control signal in accordance with said monitor signal while using

one transfer function following when said monitor signal indicates that said subscriber line voltage has extended outside of a range of voltages defined by upper and lower range limits and for a predetermined time period after said monitor signal indicates that said subscriber line voltage has returned inside of said range of voltages, and

another transfer function otherwise.

10. The method of claim **9**, wherein said step of receiving a drive control signal and in accordance therewith generating in said subscriber line an adjustable line current which varies in relation to said drive control signal comprises receiving a voltage signal as said drive control signal and in response thereto generating said adjustable line current.

11. The method of claim **9**, wherein said step of monitoring a voltage on said subscriber line and in accordance therewith generating a monitor signal which varies in relation to said subscriber line voltage comprises sensing a differential voltage as said monitored subscriber line voltage and in response thereto generating said monitor signal.

12. The method of claim **9**, wherein said step of generating said drive control signal in accordance with said monitor signal while using said one and another transfer functions comprises:

receiving a filter control signal and in accordance therewith filtering said monitor signal and in accordance therewith generating said drive control signal; and

detecting transients in said monitor signal and in accordance therewith generating said filter control signal.

13. The method of claim **12**, wherein said step of receiving a filter control signal and in accordance therewith filtering said monitor signal and in accordance therewith generating said drive control signal comprises:

receiving and comparing a reference signal and said monitor signal and in accordance therewith generating a comparison result signal which indicates a difference between said monitor signal and said reference signal; and

receiving said filter control signal and in accordance therewith filtering said comparison result signal and in accordance therewith generating said drive control signal.

14. The method of claim **12**, wherein said step of detecting transients in said monitor signal and in accordance therewith generating said filter control signal comprises:

detecting said monitor signal transients and in accordance therewith generating a transient detection signal; and

comparing said transient detection signal and at least one reference signal and in accordance therewith generating said filter control signal which is

in one signal state following when said transient detection signal indicates that said subscriber line voltage has extended outside of a range of voltages defined by upper and lower range limits and for a predetermined time period after said transient detection signal indicates that said subscriber line voltage has returned inside of said range of voltages, and

in another signal state otherwise.

15. The method of claim **14**, wherein said step of detecting said monitor signal transients and in accordance therewith generating a transient detection signal comprises high-pass filtering said monitor signal and in accordance therewith generating said transient detection signal.

16. The method of claim **14**, wherein said step of comparing said transient detection signal and at least one reference signal and in accordance therewith generating said filter control signal in said one and another signal states comprises:

receiving first and second reference signals as said at least one reference signal;

comparing said transient detection signal with said first and second reference signals and in accordance therewith generating a comparison result signal; and

generating said filter control signal in response to said comparison result signal.

17. An apparatus including a subscriber line interface circuit which includes a transient signal detector with temporal hysteresis, comprising:

a transconductance amplifier configured to connect to a subscriber line and receive a drive voltage and in accordance therewith provide to said subscriber line an adjustable line current which varies in relation to said drive voltage;

a sense amplifier configured to connect to and sense a voltage on said subscriber line and in accordance therewith provide a sense signal which varies in relation to said subscriber line voltage;

a subtraction circuit coupled to said sense amplifier and configured to receive a reference signal and said sense signal and in accordance therewith provide a difference signal which indicates a difference between said reference and sense signals;

an adjustable filter with first and second associated filter time constants, coupled to said subtraction circuit and said transconductance amplifier, and configured to receive a control signal with first and second control signal states and in accordance therewith receive and filter said difference signal and in accordance therewith provide said drive voltage, wherein said difference signal is filtered in accordance with said first and second associated filter time constants when said control signal is in said first and second control signal states, respectively; and

a transient detector, coupled to said subtraction circuit and said adjustable filter, configured to receive said sense signal and in accordance therewith provide said control signal which is

in said first control signal state following when said sense signal indicates that said subscriber line voltage has extended outside of a range of voltages defined by upper and lower range limits and for a predetermined time period after said sense signal indicates that said subscriber line voltage has returned inside of said range of voltages, and

in said second control signal state otherwise.

18. The apparatus of claim **17**, wherein said sense amplifier comprises a differential sense amplifier configured to sense a differential voltage as said sensed subscriber line voltage and in response thereto generate said sense signal.

19. The apparatus of claim **17**, wherein said adjustable filter comprises an adjustable low-pass filter circuit.

20. The apparatus of claim **17**, wherein said transient detector comprises:

a transient filter configured to filter said sense signal and in accordance therewith provide a transient detection signal; and

a comparator coupled to said transient filter and configured to receive and compare said transient detection signal and at least one reference signal and in accordance therewith provide said control signal.

21. The apparatus of claim **20**, wherein said transient filter comprises a highpass filter circuit.

22. The apparatus of claim **20**, wherein said comparator comprises:

a bipolar comparator circuit configured to receive first and second reference signals as said at least one reference signal and to compare said transient detection signal with said first and second reference signals and in accordance therewith provide a comparison result signal; and

a timer circuit, coupled to said bipolar comparator circuit, configured to receive said comparison result signal and in accordance therewith provide said control signal.

* * * * *

Submission IV

Type	Reference	Title
Patent	US 6028464	Transient Signal Detector
Citations	**6**	

US006028464A

United States Patent [19]

Bremner

[11] **Patent Number: 6,028,464**

[45] **Date of Patent: Feb. 22, 2000**

[54] **TRANSIENT SIGNAL DETECTOR**

[75] Inventor: **Duncan James Bremner**, Lochwinnoch, United Kingdom

[73] Assignee: **National Semiconductor Corporation**, Santa Clara, Calif.

[21] Appl. No.: **09/053,193**

[22] Filed: **Apr. 1, 1998**

[51] **Int. Cl.**[7] **H03K 5/08**

[52] **U.S. Cl.** **327/309**; 327/53; 327/66; 327/74; 330/253; 330/257

[58] **Field of Search** 327/52, 53, 65, 327/66, 74, 310, 563, 309; 330/252, 257, 253

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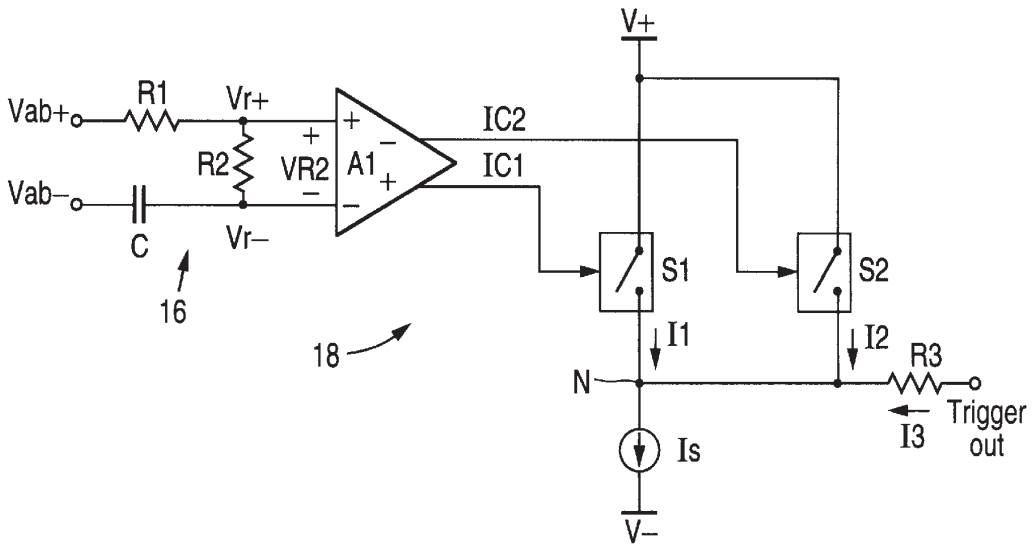
Primary Examiner—Kenneth B. Wells
Assistant Examiner—Minh Nguyen
Attorney, Agent, or Firm—Limbach & Limbach L.L.P.

[57] **ABSTRACT**

A transient signal detector for monitoring a signal line and generating a control signal which indicates when the magnitude of a differential signal on the line exceeds either a positive or negative threshold value. The threshold value is defined by a single current, thereby allowing for a single, simple adjustment of such threshold in both the positive and negative directions.

6 Claims, 2 Drawing Sheets



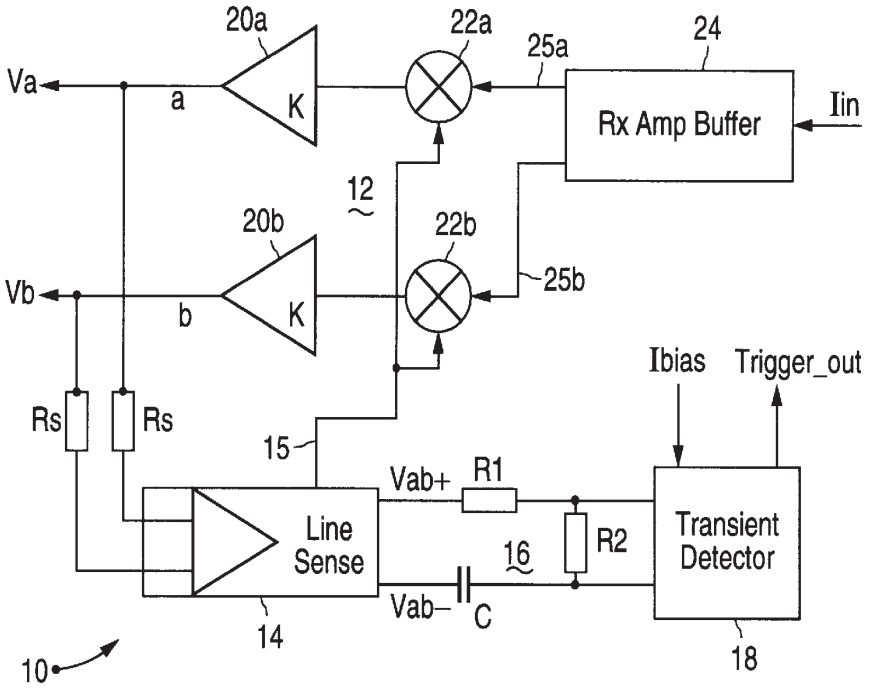


FIGURE 1

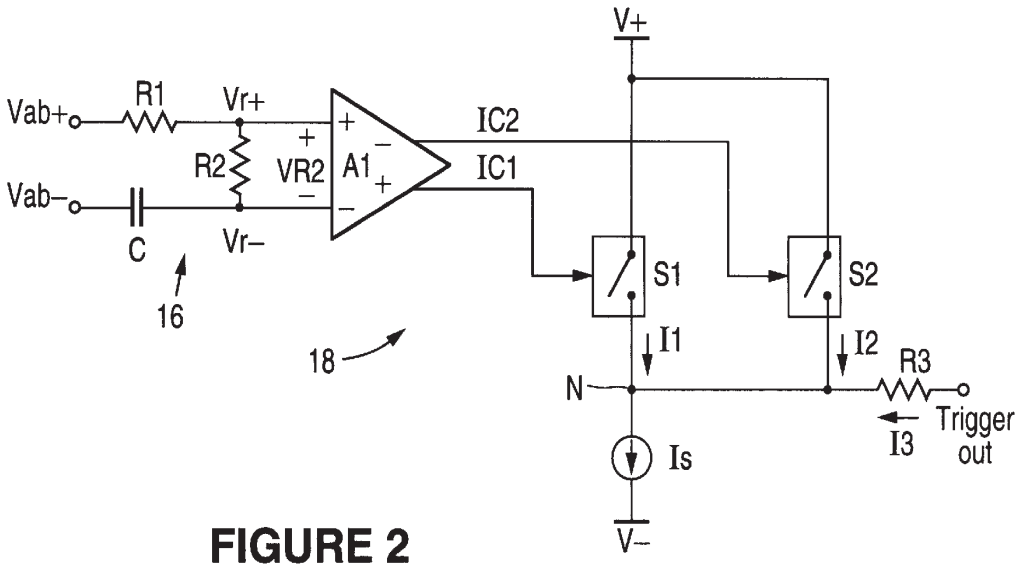


FIGURE 2

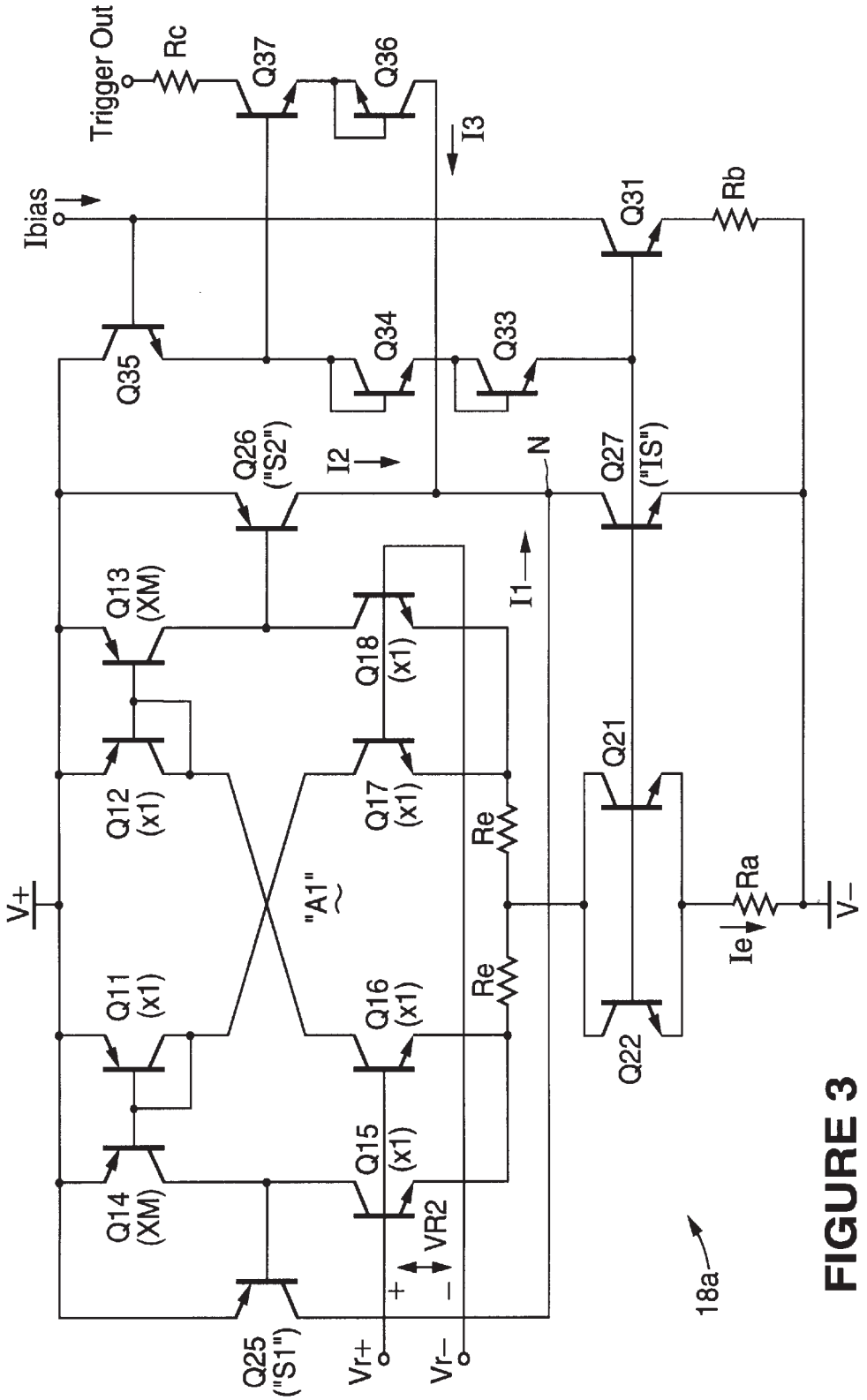

Trigger Out
Rc
Q37
Q36
I3
Ibias
Q31
Rb
Q35
Q34
Q33
Q26
("S2")
I2
N
Q27
("IS")
Q13
(XM)
Q18
(x1)
I1
Q12
(x1)
Q17
(x1)
Q21
Re
V+
"A1"
Ra
V–
Ie
Q11
(x1)
Q16
(x1)
Re
Q22
Q15
(x1)
Q14
(XM)
VR2
+
–
18a
Q25
("S1")
Vr+
Vr–

FIGURE 3

TRANSIENT SIGNAL DETECTOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to transient signal detectors, and in particular, to transient signal detectors for detecting transient signal excursions which exceed threshold levels in both positive and negative directions.

2. Description of the Related Art

Many circuit applications can benefit from, or in many cases absolutely require, some form of transient signal detection whereby signals within the monitored signal path which exceed some predetermined threshold and which are frequently transient in nature can be reliably detected. This will allow appropriate responsive action to be initiated, such as filtering or suppression of such transient signals.

One such circuit application is that of a subscriber line interface circuit (SLIC) for telecommunications. Signal transients in a telecommunication environment are quite common. For example, aside from any transient signals introduced by the operating environment (e.g., electrical motors, lightning strikes, ground loops, etc.), transients due to transitions between on-hook and off-hook conditions and normal dialing impulses caused by rotary telephones are often encountered. For many applications, such transients can be problematic and result in unreliable or otherwise unacceptable circuit performance.

Monitoring transient signals in a SLIC application, while already difficult, can be further complicated by the fact that the signal environment is differential in nature due to the "tip" and "ring" signal connections. Accordingly, transient signals with both positive and negative differential signal polarities can be and often are encountered. Accordingly, it would be desirable to have a simple transient signal detection circuit which can detect both positive and negative signal transients in a differential signal environment.

SUMMARY OF THE INVENTION

A transient signal detector in accordance with the present invention provides for the monitoring of a signal line and the generating of a control signal which indicates when the magnitude of the differential signal on the line exceeds either a positive or negative threshold value. Such threshold value can be defined by a single circuit parameter, such as a current, thereby allowing for a single, simple adjustment of the threshold for both the positive and negative threshold values.

In accordance with one embodiment of the present invention, a transient signal detector for monitoring a signal and indicating when such signal has a magnitude which extends in either direction outside of a range defined by positive and negative threshold values includes a differential buffer circuit, an output circuit and a current sinking circuit. The differential buffer circuit is configured to receive a differential signal and in accordance therewith selectively provide first and second currents. The first current is provided when the differential signal has a first polarity and a magnitude which exceeds a first threshold value. The second current is provided when the differential signal has a second polarity and a magnitude which exceeds a second threshold value. The output circuit is configured to selectively convey a third current. The current sinking circuit is coupled to the differential buffer circuit and the output circuit and is configured to: sink the first current when the differential signal has the first polarity and the differential signal magnitude exceeds the first threshold value; sink the second current when the differential signal has the second polarity and the differential signal magnitude exceeds the second threshold value; sink the third current when the differential signal has the first polarity and the differential signal magnitude is less than the first threshold value; and sink the third current when the differential signal has the second polarity and the differential signal magnitude is less than the second threshold value.

In accordance with another embodiment of the present invention, a method of monitoring a signal and indicating when such signal has a magnitude which extends in either direction outside of a range defined by positive and negative threshold values includes the steps of:

receiving a differential signal and in accordance therewith

generating a first internal current when the differential signal has a first polarity and a magnitude which exceeds a first threshold value, and

generating a second internal current when the differential signal has a second polarity and a magnitude which exceeds a second threshold value;

sinking the first internal current when the differential signal has the first polarity and the differential signal magnitude exceeds the first threshold value;

sinking the second internal current when the differential signal has the second polarity and the differential signal magnitude exceeds the second threshold value;

sinking an external current when the differential signal has the first polarity and the differential signal magnitude is less than the first threshold value; and

sinking the external current when the differential signal has the second polarity and the differential signal magnitude is less than the second threshold value.

These and other features and advantages of the present invention will be understood upon consideration of the following detailed description of the invention and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a functional block and circuit schematic diagram of a subscriber line interface circuit containing a transient signal detector in accordance with one embodiment of the present invention.

FIG. **2** is a circuit schematic and functional block diagram of a transient signal detector in accordance with one embodiment of the present invention.

FIG. **3** is a circuit schematic diagram of a transient signal detection circuit in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. **1**, a SLIC **10** containing a transient signal detector in accordance with one embodiment of the present invention includes a drive circuit **12**, a line sense stage **14**, a filter circuit **16** and a transient detector stage **18**, interconnected substantially as shown. The drive circuit **12** includes two amplifiers **20***a*, **20***b* which drive the individual subscriber lines at nodes a and b. In turn, these amplifiers **20***a*, **20***b* are driven by signals **25***a*, **25***b* from a receiver amplifier buffer **24**, following the mixing of such signals **25***a*, **25***b* with the feedback signal from the sense circuit **14**. The sense circuit **14** senses voltages Va and Vb at nodes a and b, respectively, via sense resistors Rs.

In accordance with well known principles, the line sense stage **14** monitors the individual line voltages Va, Vb via the sense resistors Rs. In addition to the feedback signal **15** for the driver circuit **12**, the line sense stage **14** also generates a differential voltage Vab having a "positive" phase Vab+ and a "negative" phase Vab−. This differential signal Vab+/Vab− is applied to the filter **16** which is a high-pass filter formed by a serial connection of two resistors R1, R2 and a capacitor C. The differential voltage across the second resistor R2 is applied to the transient detector stage **18**. (With resistor values of R1=467 kilohms and R2=33 kilohms and a capacitor value of C=0.22 microfarad, a pole is formed at 1.5 Hertz and a fractional value of 1/15 of the input differential signal Vab+/Vab − is generated across resistor R2.) The transient detector **18** receives a bias current Ibias and generates a trigger output signal (discussed in more detail below).

Referring to FIG. **2**, the function performed by the transient detector stage **18** can be represented as shown. The fractional differential voltage Vr+/Vr− across the second resistor R2 is applied to the inputs of a differential amplifier stage A1 which generates two control signals (e.g., currents) IC1, IC2. Control signals IC1 and IC2 are activated when respective opposing peak excursions of the voltage VR2=(Vr+)−(Vr−) across resistor R2 are greater in magnitude than predetermined opposing (e.g., "positive" and "negative") threshold values (discussed in more detail below). When control signal IC1 is activated, switch S1 is closed, thereby allowing current I1 to flow into node N. When control signal IC2 is activated, switch S2 is closed, thereby allowing current I2 to flow into node N. These control signals IC1, IC2 are activated in a mutually exclusive manner, i.e., only one control signal IC1, IC2 is active at one time.

When neither control signal IC1, IC2 is active, current I3 flows through the output resistor R3 into node N and is sunk by the current source circuit Is to the negative power supply terminal V−. Whenever one of the control signals IC1, IC2 is activated, its corresponding current I1, I2 is sunk by the current source Is and output current I3 is zero. Hence, if the voltage VR2 across resistor R2 remains within the predetermined positive and negative threshold values, output current I3 flows and a voltage is generated across the output resistor R3. However, if the input voltage VR2 is greater in magnitude than either threshold value, regardless of polarity, current I3 is cut off and either current I1 or current I2 is sunk by the current source circuit Is.

Referring to FIG. **3**, a preferred embodiment **18***a* of the transient detector stage **18** of FIG. **2** includes a number of PNP transistors Q11, Q12, Q13, Q14, Q25, Q26, a number of NPN transistors Q15, Q16, Q17, Q18, Q21, Q22, Q27, Q31, Q33, Q34, Q35, Q36, Q37, and several resistors Re, Ra, Rb, Rc, all interconnected substantially as shown. The differential amplifier A1 includes a dual differential amplifier (one being composed of transistors Q15 and Q18 and the other being composed of transistors Q16 and Q17), cross-coupled to two current mirrors (one being composed of transistors Q11 and Q14 and the other being composed of transistors Q12 and Q13). The "switch" circuits S1, S2 are implemented as current amplifying switch circuits in the form of transistors Q25 and Q26. The input bias current Ibias, via transistors Q31, Q33, Q34 and Q35, establishes the biasing for transistors Q21, Q22 and Q27, thereby establishing the current sinking capability of transistor Q27 (Is), as well as the current source operation of transistors Q21 and Q22 to generate a tail current Ie for the differential amplifier A1.

Transistors Q11, Q12, Q15, Q16, Q17 and Q18 are all identical in size (x1), while transistors Q13 and Q14 are ratioed to be larger by a factor of M (xM). Two resistors Re serve as emitter degeneration resistors for the dual differential amplifiers (Q15/Q18, Q16/Q17). Input voltage Vr+ is applied to the bases of transistors Q15 and Q16, while input voltage Vr− is applied to the bases of transistors Q17 and Q18.

During quiescent operation, both input voltages Vr+, Vr− are at equal potentials. Accordingly, the output nodes of the differential amplifier A1, i.e., the collectors of transistors Q14, Q15, Q13 and Q18, are holding the output buffer transistors Q25, Q26 in an "off" state by sourcing and sinking equal currents with transistors Q14 and Q15 and transistors Q13 and Q18, respectively. Consequently, currents I1 and I2 are zero and current I3 (via an output circuit formed by transistors Q36 and Q37 and resistor Rc) flows into node N and is sunk by transistor Q27, thereby indicating that the input voltage VR2 is inside the threshold potentials.

As the input voltage VR2 increases, however, an operating point is reached where the current sharing of transistors Q15, Q16, Q17 and Q18 is such that the net output current ceases to hold off the bases of transistors Q25 and Q26. Accordingly, one of these output transistors Q25, Q26 turns on and substitutes either current I1 or I2 for current I3 at node N. Hence, output current I3 drops to zero, thereby indicating that one of the input threshold levels has been exceeded.

The threshold level which is the same for either polarity of the input voltage VR2 is determined by the ratio M of the devices within the current mirrors, the emitter degeneration resistance Re and the tail current Ie and is computed in accordance with the following equation:

$$Vth=|(1-M)/(1+M)|*Ie*Re+Vt*\ ln(M)$$

(where Vth is the threshold voltage level, Vt is the kT/q factor for bipolar transistors (where k=Boltzman's constant, T=temperature in degrees Kelvin and q=electronic charge), approximately equal to 26 millivolts at 300° Kelvin, and "ln(M)" represents the natural logarithm of factor M). For a tail current Ie of 5 microamperes, an emitter degeneration resistance Re of 64 kilohms, a transistor ratio M of 2.5, the threshold voltage Vth is 150 millivolts.

As should be understood from the foregoing discussion, a transient signal detector in accordance with the present invention can be advantageously used in virtually any application where a simple method is needed for detecting when an incoming signal has exceeded a threshold level. Such a circuit is economical with respect to circuit area and does not require complex matching arrangements. However, for high precision applications, the layout of the circuit devices should be cross-coupled. Further, where the thresholds are not symmetric about a mean value, the emitter degeneration resistors Re, or, alternatively, the current mirror ratio M on one side, may be offset from each other so as to provide a different threshold level in one direction.

Further, as should also be understood in accordance with the foregoing discussion, a transient signal detector in accordance with the present invention need not necessarily be implemented only with bipolar technology, i.e., bipolar junction transistors. Rather, such a circuit can also be implemented with MOS technology, i.e., metal oxide semiconductor field effect transistors (MOSFETs). For example, in place of bipolar devices as shown in FIG. **3**, counterpart MOS devices (e.g., P-MOSFET for PNP and N-MOSFET for NPN) can be used instead with appropriate substitutions of drain, source and gate terminal connections for the

corresponding collector, emitter and base terminal connections of the counterpart bipolar devices, respectively.

Various other modifications and alterations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and spirit of the invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. It is intended that the following claims define the scope of the present invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.

What is claimed is:

1. An apparatus including a transient signal detector for monitoring a signal and indicating when such signal has a magnitude which extends in either direction outside of a range defined by positive and negative threshold values, comprising:

a differential buffer circuit configured to receive a differential signal and in accordance therewith selectively provide first and second currents, wherein

said first current is provided when said differential signal has a first polarity and a magnitude which exceeds a first threshold value,

said second current is provided when said differential signal has a second polarity and a magnitude which exceeds a second threshold value, and

said differential buffer circuit includes

a differential amplifier circuit, with a dual differential amplifier and a dual current mirror cross-coupled to said dual differential amplifier, configured to receive said differential signal and in accordance therewith provide first and second control signals, and

a current switching circuit, coupled to said differential amplifier circuit, configured to receive said first and second control signals and in accordance therewith provide said first and second currents;

an output circuit configured to selectively convey a third current; and

a current sinking circuit coupled to said differential buffer circuit and said output circuit and configured to

sink said first current when said differential signal has said first polarity and said differential signal magnitude exceeds said first threshold value,

sink said second current when said differential signal has said second polarity and said differential signal magnitude exceeds said second threshold value,

sink said third current when said differential signal has said first polarity and said differential signal magnitude is less than said first threshold value, and

sink said third current when said differential signal has said second polarity and said differential signal magnitude is less than said second threshold value.

2. The apparatus of claim **1**, wherein:

said dual differential amplifier comprises

a first differential amplifier configured to receive said differential signal, and

a second differential amplifier configured to receive said differential signal; and

said dual current mirror comprises

a first current mirror coupled to said first and second differential amplifiers, and

a second current mirror coupled to said first and second differential amplifiers.

3. The apparatus of claim **2**, wherein said current switching circuit comprises:

a first current amplifying switch circuit coupled to said first differential amplifier and said first current mirror; and

a second current amplifying switch circuit coupled to said first differential amplifier and said second current mirror.

4. The apparatus of claim **1**, wherein said current switching circuit comprises:

a first current amplifying switch circuit coupled to said dual differential amplifier and said dual current mirror; and

a second current amplifying switch circuit coupled to said dual differential amplifier and said dual current mirror.

5. An apparatus including a transient signal detector for monitoring a signal and indicating when such signal has a magnitude which extends in either direction outside of a range defined by positive and negative threshold values, comprising:

a differential buffer circuit configured to receive a differential signal and in accordance therewith selectively provide first and second currents, wherein

said first current is provided when said differential signal has a first polarity and a magnitude which exceeds a first threshold value, and

said second current is provided when said differential signal has a second polarity and a magnitude which exceeds a second threshold value;

an output circuit configured to selectively convey a third current;

a current sinking circuit coupled to said differential buffer circuit and said output circuit and configured to

sink said first current when said differential signal has said first polarity and said differential signal magnitude exceeds said first threshold value,

sink said second current when said differential signal has said second polarity and said differential signal magnitude exceeds said second threshold value,

sink said third current when said differential signal has said first polarity and said differential signal magnitude is less than said first threshold value, and

sink said third current when said differential signal has said second polarity and said differential signal magnitude is less than said second threshold value; and

a signal division circuit coupled to said differential buffer circuit and configured to receive and divide an input signal and in accordance therewith provide said differential signal, wherein said signal division circuit comprises a high pass filter.

6. A method of monitoring a signal and indicating when such signal has a magnitude which extends in either direction outside of a range defined by positive and negative threshold values, said method comprising the steps of:

receiving a differential signal and in accordance therewith

generating a first internal current when said differential signal has a first polarity and a magnitude which exceeds a first threshold value, and

generating a second internal current when said differential signal has a second polarity and a magnitude which exceeds a second threshold value;

sinking said first internal current when said differential signal has said first polarity and said differential signal magnitude exceeds said first threshold value;

sinking said second internal current when said differential signal has said second polarity and said differential signal magnitude exceeds said second threshold value;

sinking an external current when said differential signal has said first polarity and said differential signal magnitude is less than said first threshold value;

sinking said external current when said differential signal has said second polarity and said differential signal magnitude is less than said second threshold value;

receiving and dividing an input signal and in accordance therewith generating said differential signal; and

high pass filtering said input signal.

* * * * *

Submission V

Type	Reference	Title
Patent	US 5900771	Capacitive Multiplier for Timing Generation
Citations	**1**	

US005900771A

United States Patent [19]

Bremner

[11] **Patent Number: 5,900,771**

[45] **Date of Patent: *May 4, 1999**

[54] **CAPACITIVE MULTIPLIER FOR TIMING GENERATION**

[76] Inventor: **Duncan J. Bremner**, Lochwinnoch, United Kingdom

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **08/764,524**

[22] Filed: **Dec. 12, 1996**

[51] **Int. Cl.**[6] **H03G 3/02**

[52] **U.S. Cl.** **327/524**; 327/103; 327/538; 327/530; 327/540; 327/552

[58] **Field of Search** 327/261, 266, 327/268, 524, 538, 575, 589, 390, 534, 103, 560, 563, 530

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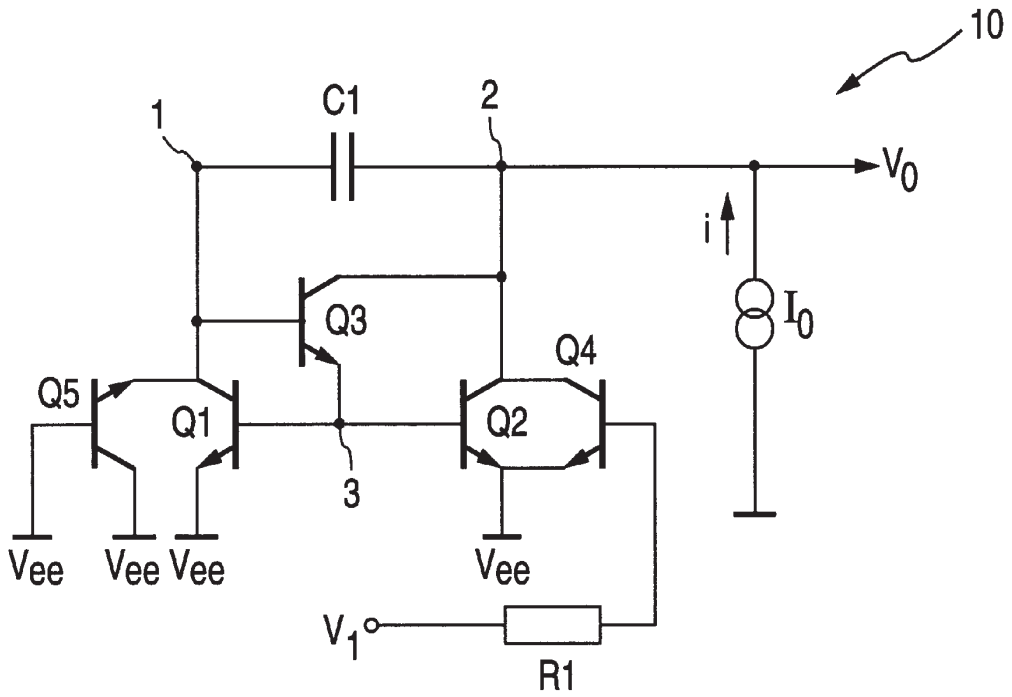
Primary Examiner—Dinh Le

[57] **ABSTRACT**

A capacitive multiplier circuit for an integrated circuit includes a capacitor coupled between a first node and a second node. A current source is coupled to provide a controlling current to the second node. A first current path shunts the first node and a second current path shunts the second node. The first current path is a first transistor having its conductance path connected between the first node and the substrate and its control electrode connected to the first node. The second current path is a second transistor having its conductance path connected between the second node and the substrate and its control electrode connected to the first node. The current ratio between the two current paths will be determined by the relative areas of the respective conductance paths.

10 Claims, 2 Drawing Sheets



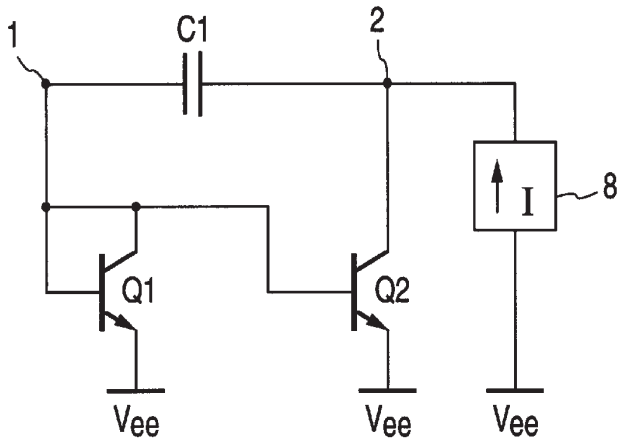


FIG. 1

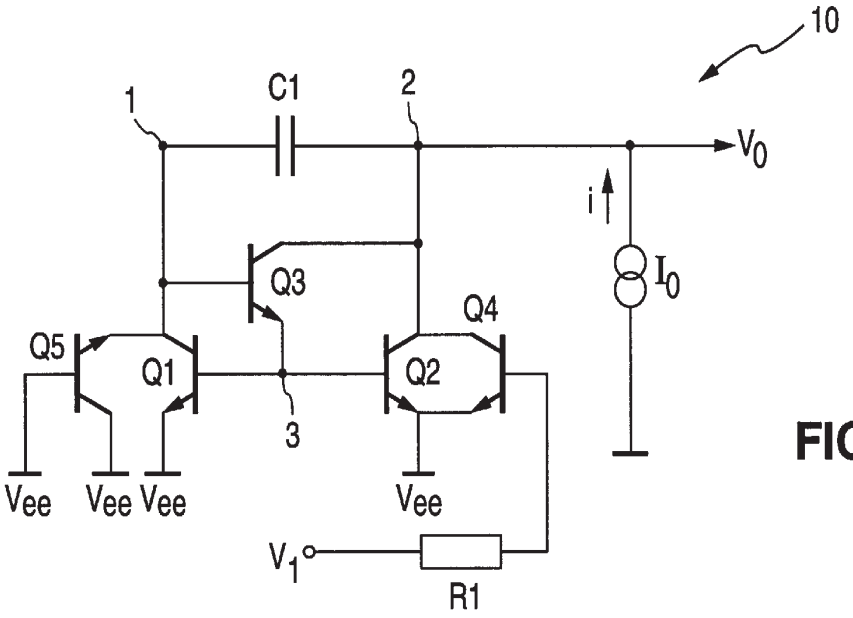


FIG. 2

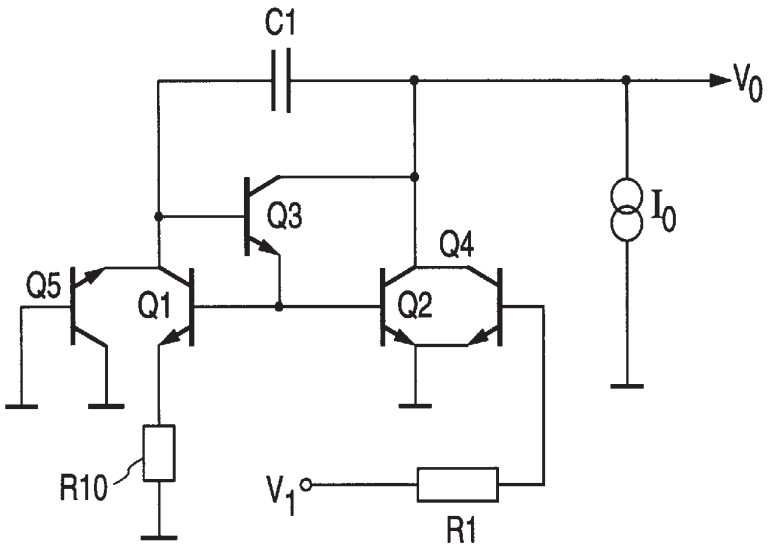


FIG. 3

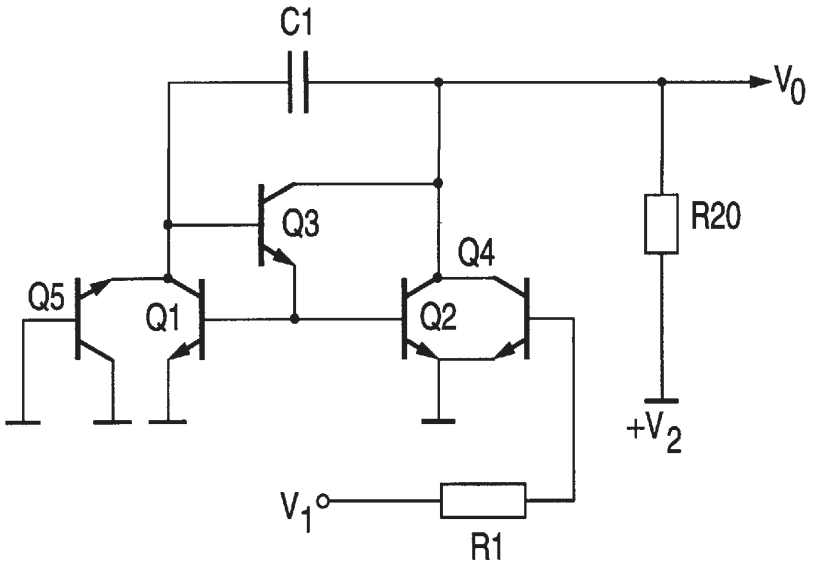


FIG. 4

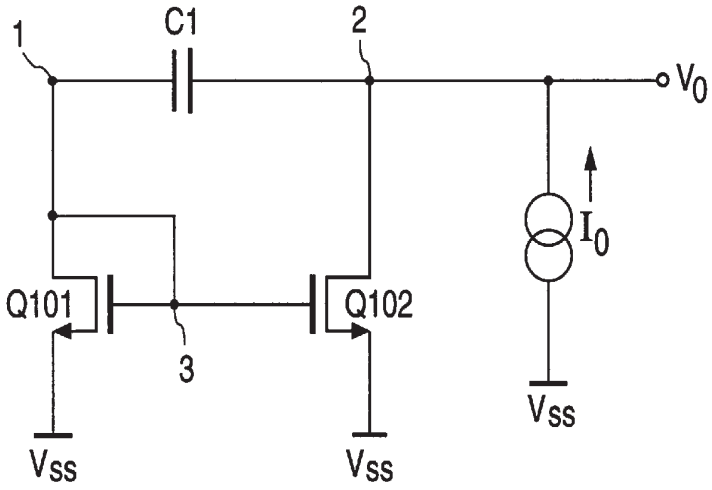


FIG. 5A

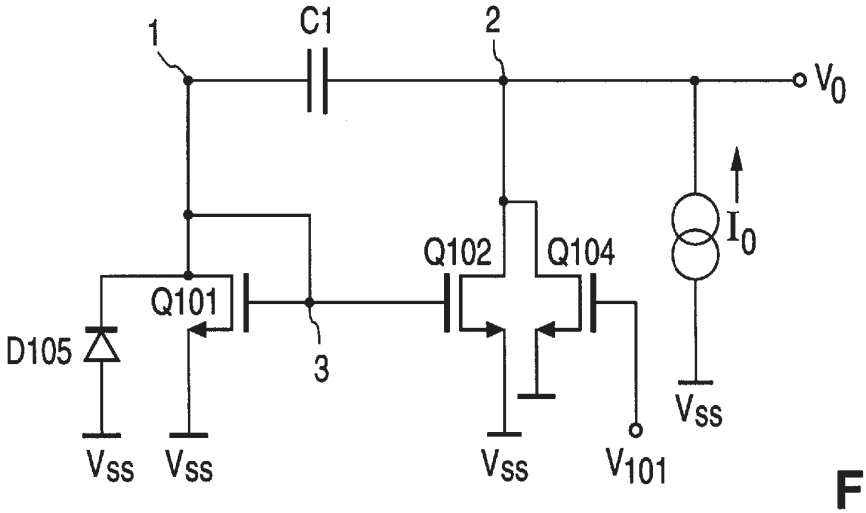


FIG. 5B

CAPACITIVE MULTIPLIER FOR TIMING GENERATION

FIELD OF THE INVENTION

The present invention relates to time delay circuitry for semiconductor integrated circuits, and more particularly, to a capacitive multiplier circuit which provides long delays for integrated circuits without taking up much silicon area.

BACKGROUND OF THE INVENTION

The ability to generate medium to long delays in semiconductor integrated circuits has been limited due either to the very small charging currents required, or to the large value of capacitors required which result in large, expensive areas of silicon. Additionally, if a method for producing small charging currents is implemented, the loading effects of measurement circuitry can give rise to errors. Therefore, it would be desirable to have a circuit which can provide significant time delays while avoiding these problems.

SUMMARY OF THE INVENTION

A capacitive multiplier circuit for a semiconductor integrated circuit includes a capacitor coupled between a first node and a second node and a current source coupled to the second node. A first current path shunts the first node and a second current path shunts the second node. The first current path conducts a first current which is a fractional portion of a second current in the second current path.

Preferably, the first current path includes a first bipolar transistor having its collector connected to the first node, its emitter connected to a reference voltage, and its base connected to the first node. The second current path includes a second bipolar transistor having its collector connected to the second node, its emitter connected to the voltage reference, and its base connected to the first node. The emitter of the second bipolar transistor has an area which is larger than an area of the emitter of the first bipolar transistor by a factor of N.

The bipolar transistors could of course be replaced with MOS transistors, wherein the current ratio is determined by the relative widths and lengths of the channels in respective transistors.

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description of the invention and accompanying drawings which set forth an illustrative embodiment in which the principles of the invention are utilized.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic circuit diagram of a conceptual embodiment of a capacitive multiplier in accord with the-present invention.

FIG. **2** is a schematic circuit diagram of the preferred embodiment of a capacitive multiplier in accord with the present invention.

FIG. **3** is a schematic circuit diagram of an alternative embodiment of a capacitive multiplier in accord with the present invention.

FIG. **4** is a schematic circuit diagram of another alternative embodiment of a capacitive multiplier in accord with the present invention.

FIG. **5***a* is a schematic circuit diagram of yet another alternative embodiment of a capacitive multiplier in accord with the present invention, and

FIG. **5***b* is the full application circuit implementing the circuit of FIG. **5***a*.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is a capacitive multiplier circuit for an integrated circuit. The capacitive multiplier is useful for providing relatively long time constants using small capacitor values thereby avoiding the use of excessive silicon area in the semiconductor integrated circuit.

The capacitive multiplier circuit may be formed by taking a charging current which flows into a capacitor and dividing it into at least two current paths. Preferably, each current path includes a bipolar transistor, and the amount of current which flows through each current path is proportional to the relative size of the emitter in each current path. Thus, the time constant required for a particular application may be adjusted by sizing respective emitters appropriately. The invention may also be implemented with MOS transistors by choosing the size (i.e. width and length). of the source and/or drain regions appropriately.

A simplified conceptual implemtation of the circuit is shown in FIG. **1**, wherein a capacitor C**1** is coupled between a first node labeled **1** and a second node labeled **2**. A source **8** is connected to the second node **2** for providing a control current to the circuit. A first current path shunts the first node **1** and comprises a first bipolar transistor Q**1** having its base and collector commonly connected to node **1** and its emitter connected to a reference voltage V_{ee}, usually ground. A second current path shunts the second node **2** and comprises a second bipolar transistor Q**2** having its base connected to node **1**, its collector connected to node **2**, and its emitter connected to reference voltage V_{ee}. The emitter of the second transistor Q**2** is formed to have an area which is larger than that of the emitter of the first transistor Q**1** by a factor of N. Therefore, the current flow in the two current paths formed by transistors Q**1** and Q**2** is in the ratio 1:N.

Referring now to FIG. **2**, the preferred embodiment for a capacitive multiplier circuit according to the present invention is illustrated. It should be recognized that circuit elements in all the Figures may be formed with conventional semiconductor fabrication techniques and a detailed description thereof is not necessary for the understanding of the present invention.

A capacitor C**1** is connected between a pair of nodes which are labeled for reference as node **1** and node **2**, respectively. A current source I_0 is coupled to provide a control current to node **2**. A first bipolar transistor Q**1** is formed having its collector coupled to node **1** and its emitter coupled to a reference voltage V_{ee}, which is typically the substrate and usually grounded. A second bipolar transistor Q**2** is formed having its collector coupled to node **2** and its emitter coupled to the substrate. However, in accord with the present invention, the emitter of the second transistor Q**2** is formed to have an area which is larger by a predetermined factor N than the emitter area of the first transistor Q**1**. Since the emitters of transistors Q**1** and Q**2** are formed such that their relative sizes have a ratio that is nominally 1:N, then the charging current is shared between transistors Q**1** and Q**2** in the following proportion (assuming the charging current is not significantly affected by current in transistor Q**3**):

$$\text{for transistor } Q1: \quad I_{Q1} = I_0 \times \frac{1}{1+N}$$

-continued

for transistor $Q2$: $I_{Q2} = I_0 \times \frac{N}{1+N}$

A third bipolar transistor Q3 has its base connected to node 1, its collector connected to node 2, and its emitter connected to a third node, node 3, which is connected both to the base of the first transistor Q1 and to the base of the second transistor Q2, such that transistor Q3 drives transistor Q2 in the well known Darlington configuration.

A fourth bipolar transistor Q4 has its collector connected to node 2, its emitter connected to the substrate, and its base connected to a voltage reference V1 through a resistor R1. Transistor Q4 is used to reset the timing circuit, and upon application of a voltage V1, which is sufficient based upon the value of the resistor R1, to cause transistor Q4 to saturate, for example, +3 V, the capacitor C1 will be fully discharged and ready for another timing cycle.

A fifth bipolar transistor Q5 has its emitter connected to node 1 and its base and collector connected to the substrate thereby effectively forming a diode. The diode-connected transistor Q5 serves the dual purpose of discharging the capacitor during reset, and to limit the potentially damaging negative-going voltage excursion at node 1.

The operation of the capacitive multiplier circuit will now be described. Initially, the effects of Q4, Q5, R1 and V1 are ignored and all the node voltages are zero. Then, upon application of the control current I_0, the common collectors of transistors Q2 and Q3 begin to rise since the devices are initially off. The charging current through capacitor C1 turns on transistor Q3, thereby turning on transistors Q1 and Q2.

The current in transistor Q3 can be ignored when N is much less than beta. Therefore, the charging current is dominated by the collector current of transistor Q1 and is less than the controlling current I_0 by a factor of N+1. However, the current ratio between transistor Q1 and transistor Q2 remains proportional to the ratio of the emitter areas. Hence, the charging current flowing through transistor Q1, and therefore into capacitor C1, is a fixed proportion of the controlling current I_0 and is independent of the transistor parameters, such as beta. This allows a relatively large current, which is easily generated, to be uses as the controlling current in the circuit while allowing small charging currents into the timing capacitor C1, hence allowing a smaller timing capacitor.

In one illustrative example, the circuit components have the following values: C1=10 pF, I_0=10 μA, and R1=10 kΩ.

An alternative embodiment is shown in FIG. 3, wherein the current ratio between transistors Q1 and Q2 can be established by using degeneration resistor R10 in the emitter connection of transistor Q1. For example, the emitters of transistors Q1 and Q2 could be nominally the same and resistor R10 have a value of 68.6 kΩ to provide a current ratio of 1:11, assuming I_0=10 μA.

In the embodiments of FIGS. 2 and 3, the controlling current is generated by a constant current source. However, the constant current source could be replaced by a resistor R20, as shown in FIG. 4, which generates an exponential voltage wave form similar to a conventional RC charging circuit, except that in this case, the time constant is multiplied by a factor of N+1. If the ratio of emitter Q1:Q2=1:N, the time constant is defined as t=(N+1)*R20*C1. It should be obvious to one with skill in this art that other methods could also be devised to provide a suitable contol current.

As previously mentioned, the inventive circuit could also be implemented with MOS technology, as illustrated in FIGS. 5*a* and 5*b*. A first CMOS transistor Q101 is formed having so that its source/drain conductance path, i.e. channel, is coupled between node 1 and a reference voltage V_{ss}, which is usually a grounded substrate. A second CMOS transistor Q102 is formed having its source/drain conductance path coupled between node 2 and the substrate. The gates or control electrodes of transistors 101 and 102 are mutually coupled together and also to the first node 1.

In accord with the present invention, the conductance path of the second transistor Q102 has an area which is larger by a predetermined factor N than the area of the conductance path of the first transistor Q101. Thus, if the channel width to length ratio of the conductance path of the first transistor Q101 is formed to be a/b, then the channel width to length ratio of the conductance path of the second transistor Q102 is formed to be N*a/b. That is, the ratio of currents between the first current path and the second current path is defined the relative width to length ratios for Q101 and Q102.

The full application circuit is shown in FIG. 5*b*, and includes CMOS transistor Q104, which corresponds to reset transistor Q4 in the bipolar embodiments. Upon application of a voltage V101 sufficient to saturate transistor Q104, for example +5 V, the capacitor C1 will fully discharge and be ready for another timing cycle. A diode D105 acts in the same manner described in the previous embodiments.

It should be understood that the invention is not intended to be limited by the specifics of the above-described embodiment, but rather defined by the accompanying claims.

I claim:

1. An integrated capacitive multiplier circuit comprising:

a source for generating a current,

a capacitor connected to the source,

a current divider network connected across the capacitor, wherein the current divider network includes at least first and second current paths each shunting opposite terminals of the capacitor and having first and second transistors, respectively, formed therein, wherein the first transistor provides a first charging current flow through the first current path and the second transistor provides a second charging current flow through the second current path, and wherein the second charging current flow is proportional to the first charging current flow, and further wherein upon charging by the capacitor to a predetermined charge level the first and second transistor are turned off and the first and second charging current flows decrease to approximately zero, and

a reset circuit, connected to said terminals of the capacitor, wherein the reset circuit receives a reset signal and in accordance therewith causes the capacitor to fully discharge.

2. An apparatus including a capacitance multiplier circuit, comprising:

a first node for receiving an input current and in accordance therewith providing a charging current and a shunting current, wherein a sum of said charging and shunting currents equals said input current;

a second node for receiving and conveying said charging current;

a capacitive element, connected between said first and second nodes for receiving and conducting said charging current from said first node to said second node;

a charging transistor circuit, connected to said second node, for receiving said charging current and in accordance therewith turning on, conducting said charging current and providing a bias voltage;

a shunting transistor circuit, connected to said first node and said charging transistor circuit, for receiving said bias voltage and in accordance therewith turning on and receiving and conducting said shunting current, wherein upon charging by said capacitive element to a predetermined charge level said charging transistor circuit is turned off and said charging current decrease to approximately zero; and

a reset circuit, connected to said first and second nodes, for receiving a reset signal and in accordance therewith causing the capacitor to fully discharge.

3. The apparatus of claim **2** wherein said capacitive element comprises a capacitor.

4. The apparatus of claim **2**, wherein said charging transistor circuit comprises a bipolar transistor.

5. The apparatus of claim **2**, wherein said shunting transistor circuit comprises a bipolar transistor.

6. The apparatus of claim **2**, wherein said charging transistor circuit comprises a metal oxide semiconductor field effect transistor.

7. The apparatus of claim **2**, wherein said shunting transistor circuit comprises a metal oxide semiconductor field effect transistor.

8. The apparatus of claim **2**, wherein:

said charging transistor circuit provides a first current conductance path for said charging current; and

said shunting transistor circuit provides a second current conductance path for said shunting current, wherein said second current conductance path is larger than said first current conductance path.

9. The apparatus of claim **8**, wherein:

said charging transistor circuit has a first emitter area; and

said shunting transistor circuit has a second emitter area which is larger than said first emitter area.

10. The apparatus of claim **8**, wherein:

said charging transistor circuit has a first channel width-to-length ratio; and

said shunting transistor circuit has a second channel width-to-length ratio which is larger than said first channel width-to-length ratio.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 5,900,771
DATED: May 4, 1999
INVENTOR(S): Duncan J. Bremner

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the cover page, at [73], please insert --Assignee: NATIONAL SEMICONDUCTOR CORPORATION, Santa Clara, California--.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 5,900,771
DATED: May 4, 1999
INVENTOR(S): Duncan J. Bremner

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Col. 4, line 47, delete "transistor" and replace with --transistors--.

In Col. 5, line 7, delete "decrease" and replace with --decreases--.

In Col. 5, line 12, after "2" insert --,--.

Signed and Sealed this

Ninth Day of November, 1999

Attest:

Attesting Officer

Q. TODD DICKINSON

Acting Commissioner of Patents and Trademarks

Submission VI

Type	Reference	Title
Patent	US 6377681	Signal line driving circuit with self-controlled dissipation
Citations	**4**	

US006377681B1

(12) **United States Patent**
Bremner

(10) **Patent No.: US 6,377,681 B1**
(45) **Date of Patent: Apr. 23, 2002**

(54) **SIGNAL LINE DRIVING CIRCUIT WITH SELF-CONTROLLED POWER DISSIPATION**

(75) Inventor: **Duncan James Bremner**, Lochwinnoch (GB)

(73) Assignee: **National Semiconductor Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/053,110**

(22) Filed: **Apr. 1, 1998**

(51) **Int. Cl.**[7] **H04L 12/66**; H04M 1/00; H04M 7/04

(52) **U.S. Cl.** **379/394**; 379/413; 379/398; 370/463

(58) **Field of Search** 713/300, 326, 713/327; 379/378, 398, 413, 399, 402, 403, 394, 404, 324; 370/522, 311, 463; 340/662, 663, 635

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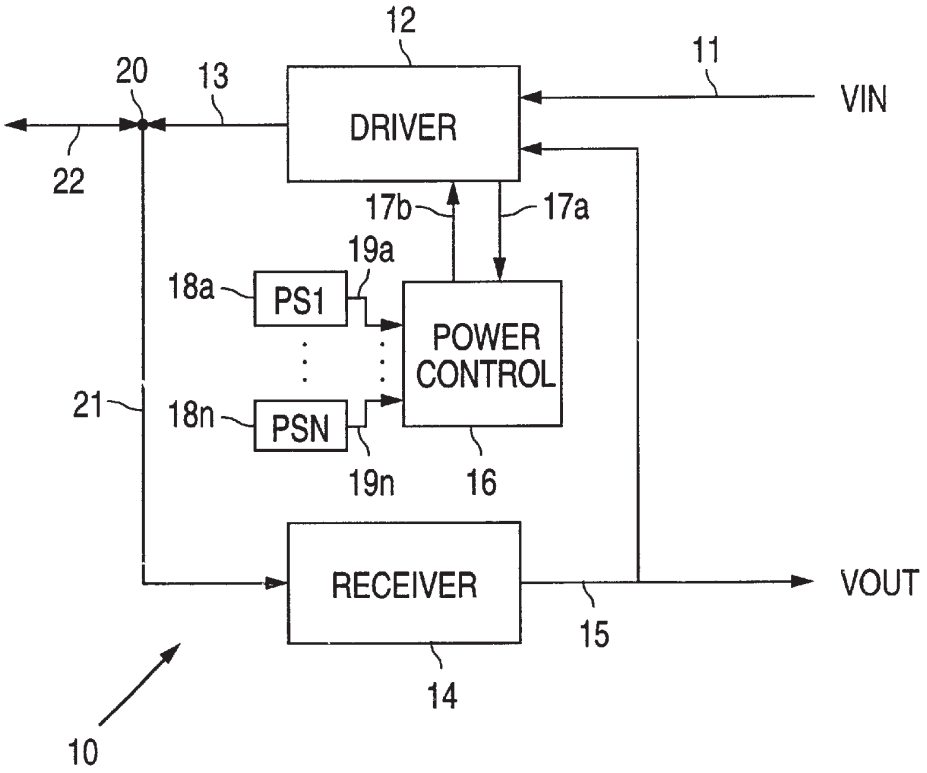
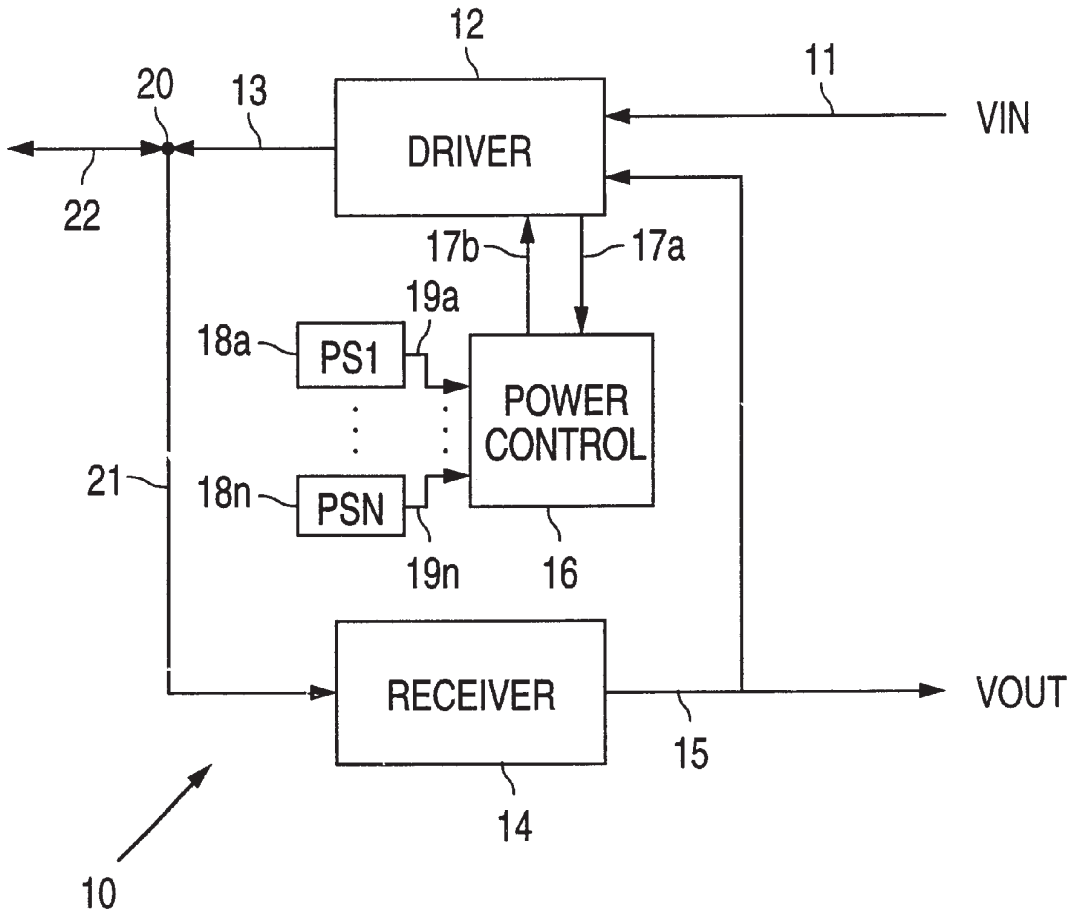
Primary Examiner—Ajit Patel
Assistant Examiner—Hanh Nguyen
(74) *Attorney, Agent, or Firm*—Wildman, Harrold, Allen & Dixon; Mark Dalla Valle

(57) **ABSTRACT**

A signal line driving circuit with power control for selectively reducing internal power dissipation when driving an external load. While driving the external load with a constant current the output voltage generated across such load is monitored. If the load impedance decreases sufficiently to cause the output voltage to fall below a predetermined threshold value and, therefore, cause the voltage across the signal line driving circuit to increase, the magnitude of the power supply voltage is automatically reduced, thereby reducing the voltage across the signal line driving circuit. Such a signal line driving circuit is particularly advantageous as a subscriber line interface circuit (SLIC). As the subscriber goes from an on-hook condition to an off-hook condition and if the subscriber loop is sufficiently short (or low in impedance), a lower power supply voltage is used to minimize the power dissipation of the SLIC while still maintaining the required subscriber loop current.

16 Claims, 2 Drawing Sheets




12
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DRIVER
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PS1
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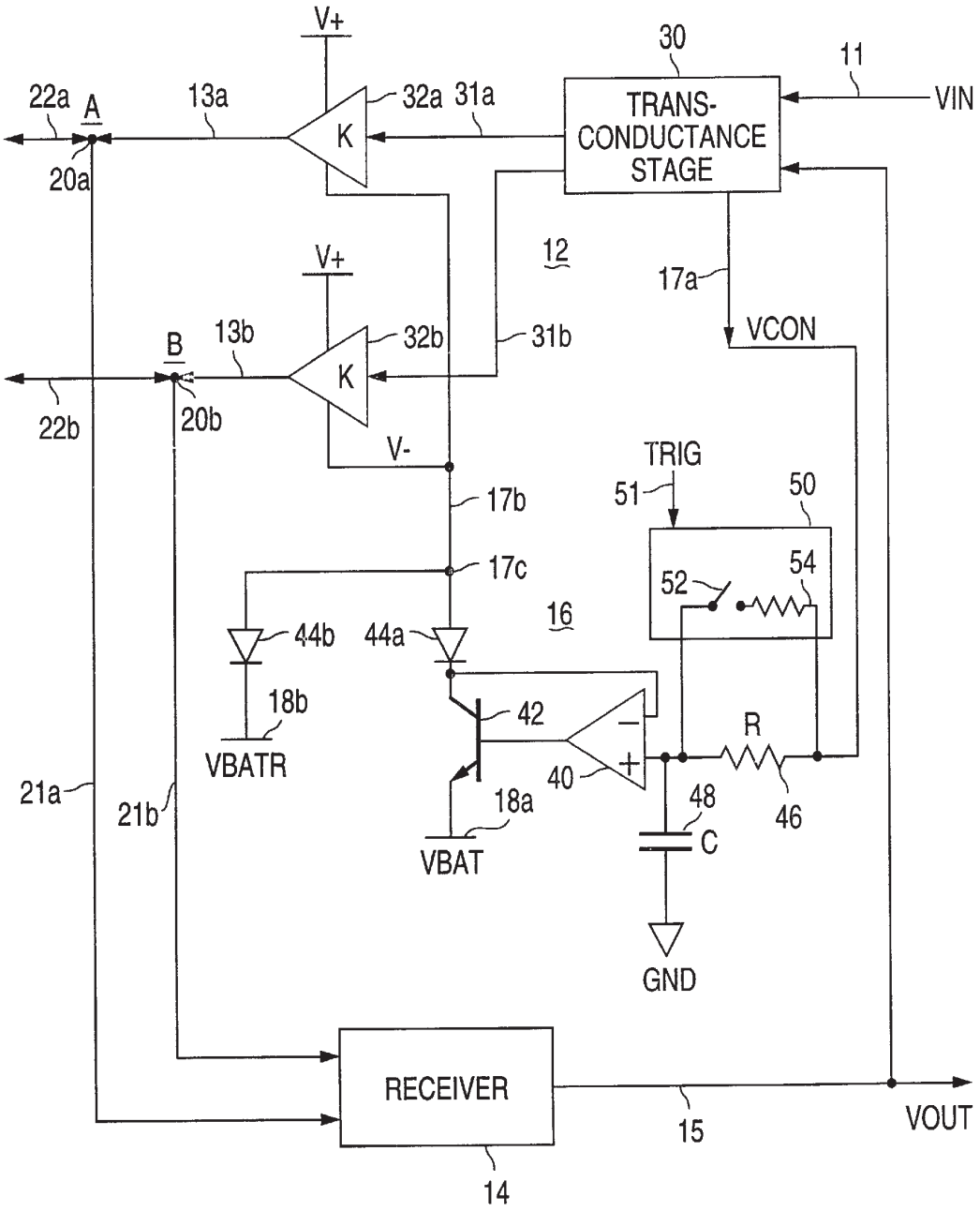
FIG. 1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17a
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13b
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TRIG
51
50
17b
17c
52
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16
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44a
18b
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VBATR
40
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46
VBAT
C
GND
RECEIVER
15
VOUT
14

FIG. 2

SIGNAL LINE DRIVING CIRCUIT WITH SELF-CONTROLLED POWER DISSIPATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to signal line driving circuits for providing output signals with approximately constant output currents, and in particular, to subscriber line interface circuits for telephone lines.

2. Description of the Related Art

A subscriber line interface circuit (SLIC) is used for each pair of wires ("tip" and "ring") forming a subscriber telephone line and is responsible for conveying both incoming and outgoing signals (e.g., voice, facsimile and data) while providing necessary power and impedance matching. Such circuit is typically located in the central office and is analog in its function, although digital versions (e.g., ISDN) are being used more often.

When the subscriber telephone is on-hook the DC output current, neglecting any leakage impedances, is substantially zero. When the subscriber loop goes into an off-hook state, industry standards require a DC output current through the subscriber loop to be approximately constant, e.g., within the nominal range of 30–40 milliamperes (mA). This DC current provides power to the subscriber telephone circuitry, such as the digital keypad. The impedance of the subscriber loop will depend upon the particular telephone, or telephones, connected to the loop, as well as the transmission length of the loop itself. Therefore, the SLIC must be designed to provide the nominal required DC output current for this range of loop impedances while still providing for transmission of the AC signals (voice, facsimile, etc.).

Based upon the foregoing, the following typical scenarios will be encountered. With an output current of 30 mA, a nominal DC power supply voltage of 50 volts for the SLIC, and a subscriber loop impedance of 1000 ohms (resistive), the output voltage presented to the subscriber loop will be 30 volts (=30 mA×1000 ohms). Accordingly, 20 volts will be dropped across the SLIC output circuitry, thereby resulting in approximately 0.6 watts (=30 mA×20 volts) of power dissipation in the output circuitry of the SLIC. However, if the subscriber loop impedance is instead only 500 ohms, then the output voltage becomes 15 volts (=30 mA×500 ohms). This results in 35 volts being dropped across the output circuitry of the SLIC, which, in turn, results in an internal power dissipation of approximately 1.05 watts (=30 mA×35 volts). Hence, it can be seen that, depending upon the subscriber loop impedance, a wide variance in the internal power dissipation of the SLIC can be encountered. Such a wide variance in internal power dissipation imposes substantial design constraints for the SLIC, and prevents such SLIC from performing at maximum efficiency.

A number of attempts to minimize the internal power dissipation of the SLIC have included such techniques as using an external resistor (connected in series with the power supply) for dissipating the excess power and using a switching voltage regulator. However, both techniques have significant disadvantages. Simply relocating the power dissipation to an external resistor does not improve overall efficiency of the system, and while a switching voltage regulator may improve power efficiency, significant switching noise can be induced into the subscriber loop.

Accordingly, it would be desirable to have a technique by which internal power dissipation can be automatically reduced by maximizing power efficiency and avoiding any introduction of signal noise.

SUMMARY OF THE INVENTION

A signal line driving circuit with self-controlled internal power dissipation in accordance with the present invention minimizes internal power dissipation while maximizing overall power efficiency and avoiding introduction of extraneous signal noise into the system.

In accordance with one embodiment of the present invention, a signal line driving circuit with power control for selectively reducing internal power dissipation when driving an external load includes a signal driver circuit and a power control circuit. The signal driver circuit is configured to connect and provide an output signal to an external impedance and to receive a source current and an input signal which corresponds to such output signal and in accordance therewith provide such output signal and a control signal which varies in relation to such output signal. The output signal includes an output current which is approximately constant and an output voltage which varies in relation to the external impedance and output current. The power control circuit, coupled to the signal driver circuit, is configured to connect to a plurality of voltage sources and receive therefrom a plurality of source voltages and to receive the control signal and in accordance therewith convey the source current from one of the plurality of voltage sources to the signal driver circuit.

In accordance with another embodiment of the present invention, a method of driving an external load via a signal line while selectively reducing power dissipation includes the steps of:

connecting to an external impedance;

connecting to a plurality of voltage sources;

applying an output signal to the external impedance;

receiving a source current and an input signal which corresponds to the output signal and in accordance therewith generating the output signal and a control signal which varies in relation to the output signal, wherein the output signal includes an output current which is approximately constant and an output voltage which varies in relation to the external impedance and the output current;

receiving a plurality of source voltages from the voltage sources; and

receiving the control signal and in accordance therewith conveying the source current from one of the plurality of voltage sources.

These and other features and advantages of the present invention will be understood upon consideration of the following detailed description of the invention and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a functional block diagram of a signal interface system using a signal line driving circuit with self-controlled internal power dissipation in accordance with one embodiment of the present invention.

FIG. **2** is a more detailed functional block and schematic diagram of the signal line driving circuit portion of the system of FIG. **1**.

DETAILED DESCRIPTION OF THE INVENTION

(While the following discussion is in the context of a subscriber line interface circuit (SLIC) for telephone signals, it should be recognized that the underlying principles of the present invention can be applied to other forms of circuits

which provide output signals with substantially constant currents and for which self-control of internal power dissipation is desired.)

Referring to FIG. **1**, a bi-directional signal interface system **10** using a signal line driving circuit with self-controlled internal power dissipation in accordance with one embodiment of the present invention includes a driver stage **12**, a receiver stage **14**, a power control stage **16** and multiple power sources **18**, interconnected substantially as shown. The driver stage **12** provides an output signal **13** to an output node **20** for conveyance to an external signal line **22**. The output node **20** also conveys from the external signal line **22** an input signal **21** which is processed by the receiver **14**. The output signal **15** from the receiver **14** is fed back to the driver stage **12**. As is well known in the art of SLICs, this allows for duplex operation of the external signal line **22** by subtracting out the receiver output signal **15** from the input signal **11** to the driver stage **12**.

The driver stage **12** provides a feedback signal **17***a* to the power control stage **16** which provides DC power **17***b* to the driver stage **12**. Based upon the feedback signal **17***a*, the power control stage **16** selects one of multiple DC voltages **19** from the DC power sources **18**. For example, when the load impedance presented via the external signal line **22** is low, based upon the output signal **13** current, the output voltage presented to the output node **20** is low. When this output voltage becomes low enough that the resulting voltage drop across the output of the driver stage **12** (Vdriver=Vsource−Voutput) exceeds a predetermined threshold (Vdriver>Vthreshold), the feedback signal **17***a* can instruct the power control stage **16** to select a lower power supply voltage **19** from another power source **18** (discussed in more detail below).

Referring to FIG. **2**, the driver **12** and power control **16** stages in accordance with one embodiment of the present invention are shown in more detail. In this embodiment, as would be typical for a SLIC, the external circuit is a differential circuit. Accordingly, the output node **20** includes two nodes **20***a*, **20***b* and the external signal line **22** includes two lines **22***a*, **22***b*. In the context of a SLIC, these two signal lines **22***a*, **22***b* form the subscriber loop.

The driver stage **12** includes a transconductance stage **30** which differentially receives the input voltage signals **11**, **15** and generates two intermediate current signals **31***a*, **31***b* which are buffered by output driver amplifiers **32***a*, **32***b*. These amplifiers **32***a*, **32***b* provide the approximately constant output current signals **13***a*, **13***b* (discussed in more detail below) to the output nodes **20***a*, **20***b*. (As discussed above, the output nodes **20***a*, **20***b* also receive the incoming signals **21***a*, **21***b* from the subscriber loop **22***a*, **22***b* which are processed by the receiver **14** in accordance with well known principles.) These amplifiers **32***a*, **32***b* are powered by positive and negative power sources. The positive power source V+ is typically zero for telecommunications applications. The negative power source V− is a negative supply.

The power control stage **16** includes a differential amplifier **40** which drives a pass transistor connected between a diode **44***a* and the primary power source **18***a* which provides a negative power supply voltage Vbat. The input signal to the differential amplifier **40**, which is the feedback, or control, signal **17***a* from the transconductance stage **30**, is filtered by a low pass filter formed by the series resistor **46** (e.g., 500 kilohms) and shunt capacitor **48** (e.g., 220 nanofarads). Connected across the resistor **46** is a "speed up" circuit **50** which, as discussed in more detail below, selectively reduces the overall resistance so as to speed up the change in the voltage across the capacitor **48**.

Another diode **44***b* is used to connect another power source **18***b* having another negative voltage Vbatr to the same node **17***c* as that to which the first diode **44***a* is connected. It is this node **17***c* which provides the negative power supply voltage **17***b* for the output driver amplifiers **32***a*, **32***b*. The first power supply voltage Vbat is the more negative voltage (e.g., −56 volts), while the second power supply voltage Vbatr is a less negative voltage (e.g., −30 volts).

As the impedance of the subscriber loop **22***a*, **22***b* reduces, such as when the subscriber goes off-hook, the differential voltage Vab at the loop nodes **20***a*, **20***b* also decreases. This voltage Vab is sensed by the receiver **14** (which typically has a high input impedance relative to the impedance of the subscriber loop and the output impedances of the driver amplifiers **32***a*, **32***b*). Accordingly, the receiver output voltage **15**, which corresponds to the subscriber loop node voltage Vab, also decreases. This, in turn, causes the control voltage **17***a* from the transconductance stage **30** to also decrease. This control voltage **17***a* is generally proportional to the receiver output voltage **15** (which in turn, is generally proportional to the subscriber loop node voltage Vab), plus some amount of overhead voltage Voh necessary for the driver amplifiers **32***a*, **32***b* to operate.

As this voltage **17***a* decreases further, the differential amplifier **40** gradually causes the pass transistor **42** to turn off. If the control voltage **17***a* decreases sufficiently, the transistor **42** becomes cut off and the supply current for the negative supply terminals of the driver amplifiers **32***a*, **32***b* is then drawn through the second diode **44***b* from the second power supply **18***b* instead of through the first diode **44***a* from the first power supply **18***a*. Since this second power supply **18***b* has a reduced voltage Vbatr, the voltage dropped across the driver amplifiers **32***a*, **32***b* is reduced, thereby reducing the internal power dissipation of the driver amplifiers **32***a*, **32***b*. Since the output current **13***a*, **13***b* is maintained approximately constant, the signal provided to the subscriber is remains unaffected. Hence, the transition between power supply voltages is not dependent upon the actual voltage values of the power supplies **18** and occurs without introducing any signal noise.

As noted above, the output current signals **13***a*, **13***b* are approximately constant. More specifically, the output current signals **13***a*, **13***b* are approximately constant for a given impedance Zloop of the subscriber loop **22***a*, **22***b*. Hence, for example, if the impedance Zloop (e.g., the resistance Rloop) of the subscriber loop **22***a*, **22***b* increases (e.g., the loop becomes longer) and becomes less negligible with respect to the subscriber loop feed resistance Rfeed (e.g., 150 ohms) within the output circuits (not shown) of the driver amplifiers **32***a*, **32***b*, then the magnitude Iloop of the output current signals **13***a*, **13***b* will decrease in accordance with the relationship Iloop=(Vbat−Voh)/(Rloop+Rfeed). However, provided that the impedance Zloop of the subscriber loop **22***a*, **22***b* remains constant, the magnitude Iloop of the output current signals **13***a*, **13***b* will also remain constant.

Furthermore, it should be recognized that notwithstanding the similar directions of the arrows for the output current signals **13***a*, **13***b* in FIG. **2**, the directions of such current signals **13***a*, **13***b* are opposite to one another. In other words, if output current **13***a* is flowing out to subscriber loop leg **22***a* via node **20***a*, then output current **13***b* is flowing in from subscriber loop leg **22***b* via node **20***b*, and vice versa.

During transient signals in the loop **22***a*, **22***b*, such as on/off-hook transient signals or dialling, the voltage provided to the loop nodes **20***a*, **20***b* must be allowed to slew

quickly enough to avoid impacting the dial pulsed distortion parameters. This is achieved by shunting the resistor **46** in the input filter for the differential amplifier **40**. A transient detection circuit elsewhere in the system (not shown) generates a trigger signal **51** which closes a switch **52** within the speed of circuit **50**. This places a shunting resistor **54** in parallel with the original resistor **46** to reduce the overall resistance value by a sufficiently significant amount (e.g., by a factor of 100). This allows the circuit to reject speech signals during normal transmission and yet quickly slew in response to normal transient signals.

Based upon the foregoing, it should be recognized that although the power control stage **16** has been discussed in terms of switching between two power sources, it is possible to design another power control stage which, in conformance with the foregoing discussion, can select between more than two power sources. For example, by duplicating the combination of filter circuit **46**, **48**, differential amplifier **40**, transistor **42** and diode **44***a* and connecting such duplicate circuits between other power sources having voltages with values intermediate to voltages Vbat and Vbatr, it is possible to provide for multiple stepped reductions in the power supply voltage provided to the driver amplifiers **32***a,* **32***b*. This would allow the power dissipation of the driver amplifiers **32***a,* **32***b* to be maintained within a fairly narrow power range.

Further based upon the foregoing, it should also be recognized that the principles of the presently claimed invention are not limited to use with circuits using negative power supplies or only bipolar technologies, but can also be applied to circuits using positive power supplies or other device technologies as well, such as metal oxide semiconductor (MOS).

Various other modifications and alterations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and spirit of the invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. It is intended that the following claims define the scope of the present invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.

What is claimed is:

1. An apparatus including a signal line driving circuit with power control for selectively reducing internal power dissipation when driving an external load, comprising:

a signal driver circuit that connects and provides an output signal to an external impedance, receives a source current and receives an input signal which corresponds to said output signal and in response thereto provides said output signal and a control signal which varies in relation to said output signal, wherein said output signal includes an output current which is approximately constant and an output voltage which varies in relation to said external impedance and said output current; and

a power control circuit, coupled to said signal driver circuit, that connects to a plurality of voltage sources and receives therefrom a plurality of source voltages and receives said control signal and in response thereto conveys a selected one of said plurality of source voltages and said source current from one of said plurality of voltage sources to said signal driver circuit, wherein, a voltage difference between said selected one of said plurality of source voltages and said output voltage varies in relation to said control signal.

2. The apparatus of claim **1**, wherein said output signal comprises a differential signal.

3. The apparatus of claim **1**, wherein said signal driver circuit comprises an amplifier circuit that receives an intermediate signal and said source current and in response thereto provides said output signal.

4. The apparatus of claim **3**, wherein said signal driver circuit further comprises a transconductance circuit, coupled to said amplifier circuit, that receives said input signal and in response thereto provides said control signal and said intermediate signal.

5. The apparatus of claim **1**, wherein said power control circuit comprises a plurality of current paths that connect between said signal driver circuit and said plurality of voltage sources, wherein, in response to said control signal, one of said plurality of current paths conveys said source current.

6. The apparatus of claim **5**, wherein one of said plurality of current paths comprises a current control circuit that receives said control signal and in response thereto selectively activates and inactivates said one of said plurality of current paths, and wherein all remaining ones of said plurality of current paths become inactivated when said one of said plurality of current paths is activated, and further wherein one of said remaining ones of said plurality of current paths become activated when said one of said plurality of current paths is inactivated.

7. The apparatus of claim **6**, wherein said current control circuit includes a filter circuit that filters said control signal.

8. The apparatus of claim **5**, wherein each one of said plurality of current paths includes a series-connected diode.

9. A method of driving an external load via a signal line while selectively reducing power dissipation, said method comprising the steps of:

connecting to external impedance;

connecting to a plurality of voltage sources;

applying an output signal to said external impedance;

receiving a source current;

receiving an input signal which corresponds to said output signal and in response thereto generating said output signal and a control signal which varies in relation to said output signal, wherein said output signal includes an output current which is approximately constant and an output voltage which varies in relation to said external impedance and said output current;

receiving a plurality of source voltages from said plurality of voltage sources; and

receiving said control signal and in response thereto conveying a selected one of said plurality of source voltages and said source current from one of said plurality of voltage sources, wherein, a voltage difference between said selected one of said plurality of source voltages and said output voltage varies in relation to said control signal.

10. The method of claim **9**, wherein said step o f applying an output signal to said external impedence comprises applying a differential signal to said external impedance.

11. The method of claim **9**, wherein said step of receiving an input signal which corresponds to said output signal and in response thereto generating said output signal and a control signal which varies in relation to said output signal comprises receiving an intermediate signal and in response thereto generating said output signal.

12. The method of claim **11**, wherein said step of receiving an input signal which corresponds to said output signal

and in response thereto generating said output signal and a control signal which varies in relation to said output signal further comprises receiving said input signal and in response thereto generating said control signal and said intermediate signal.

13. The method of claim **9**, wherein said step of connecting to a plurality of voltage sources comprises connecting to said plurality of voltage sources via a plurality of current paths.

14. The method of claim **13**, wherein said step of receiving said control signal and in response thereto conveying a selected one of said plurality of source voltages and said source current from one of said plurality of voltage sources comprising receiving said control signal and in response thereto selectively

activating said one of said plurality of current paths and inactivating all remaining ones of said plurality of current paths, and

inactivating said one of said plurality of current paths and activating one of said remaining ones of said plurality of current paths.

15. The method of claim **14**, further comprising the steps of filtering said control signal, and wherein said step of receiving said control signal and in response thereto conveying a selected one of said plurality of source voltages and said source current from one of said plurality of voltage sources comprises receiving said filtered control signal and in response thereto conveying a selected one of said plurality of source voltages and said source current from one of said plurality of voltage sources.

16. The method of claim **13**, wherein said step of connecting to said plurality of voltage sources via a plurality of current paths comprises connecting to each one of said plurality of current paths via a series-connected diode.

* * * * *

Submission VII

Type	Reference	Title
Patent	DE 199144858	Creating interface for local tests and for carrying out local tests at telephone user line and determining several electric characteristics of such user line
Citations	**Not Known**	

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(71) Anmelder:
National Semiconductor Corp., Santa Clara, Calif., US

(74) Vertreter:
Sparing . Röhl . Henseler, 40237 Düsseldorf

(72) Erfinder:
Bremner, Duncan James, Lochwinnoch, Schottland, GB

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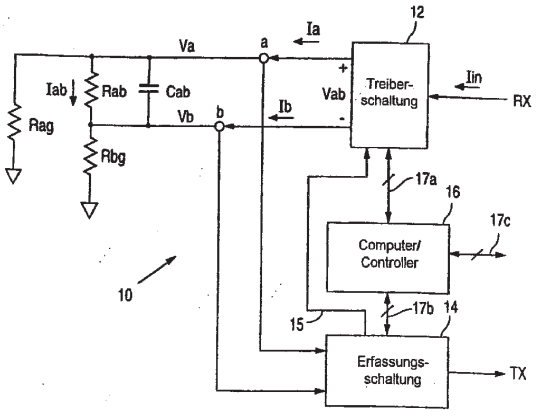
(54) Verfahren und Vorrichtung zur Schaffung einer Schnittstelle für lokale Tests und zur Ausführung von lokalen Tests für Telefonteilnehmerleitungen

(57) Die Erfindung betrifft ein Verfahren und eine Vorrichtung zur Schaffung einer Schnittstelle für lokale Tests und zur Ausführung lokaler Tests an Telefonteilnehmerleitungen sowie zur Bestimmung mehrerer elektrischer Eigenschaften einer solchen Telefonteilnehmerleitung. Durch wahlweises Erzeugen und Schalten von vier verschiedenen analogen Signalen in einer Leitungsansteuerungs-Schaltungsanordnung können viele verschiedene Teilnehmerleitungstestparameter als normale Gleichstromsignale auf einer solchen Teilnehmerleitung gemessen werden. Diese Parameter umfassen den Widerstand nach Erde von jeder der Leitungen, den Leckwiderstand zwischen den Leitungen sowie die Kapazität zwischen den Leitungen.



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Beschreibung

Die Erfindung betrifft ein Verfahren und eine Vorrichtung zur Schaffung einer Schnittstelle für lokale Tests und zur Ausführung von lokalen Tests für Telefonteilnehmerleitungen nach den Oberbegriffen der Ansprüche 1 bzw. 10.

Wie in **Fig.** 3 gezeigt ist, enthält ein typisches lokales Telefonsystem ein Vermittlungsamt, das die lokalen Telekommunikationssignale (z. B. Sprache, Daten, Telefax usw.), für die es verantwortlich ist, sammelt und verteilt. Diese Signale werden von Untersystemen, die in zahlreichen Straßengeräteschränken untergebracht sind, weiterverteilt und gesammelt, wobei jedes Untersystem die Signale von den einzelnen Teilnehmern sammelt und an diese einzelnen Teilnehmer verteilt.

Um die Funktionsfähigkeit des Gesamtsystems aufrechtzuerhalten, muß jede einzelne Teilnehmerschleife periodisch getestet werden, um Fehler im System zu erfassen und einen Schutz vor derartigen Fehlern zu schaffen, ferner müssen die Leistungsanforderungen zum Betreiben der Schleife minimiert werden. Ein solcher Test wird in Koordination mit jeder einzelnen Teilnehmerleitung-Schnittstellenschaltung (= SLIC = Subscriber Line Interface Circuit), die für die Schaffung einer Schnittstelle mit jedem einzelnen Teilnehmer verantwortlich ist, ausgeführt.

Wenn ein solcher Test im Vermittlungsamt oder alternativ in größeren Straßenschränken implementiert ist, kann er in verhältnismäßig kosteneffizienter Weise unter Verwendung einer üblichen Testvorrichtung, die für eine große Anzahl von Leitungen gemeinsam genutzt wird, ausgeführt werden. Im allgemeinen ist es wünschenswert, eine solche Testausrüstung im System soweit wie möglich nach "unten" zu schieben, d. h. näher an jede einzelne Teilnehmerschleife, um so die Auflösung der zugehörigen Tests zu erhöhen. Wenn jedoch solche Tests stärker verteilt sind, werden die Kosten der Testgeräte für die Unterstützung solcher Tests zu einem Hindernis, da die Anzahl der Leitungen, die eine übliche Testvorrichtung gemeinsam nutzen, reduziert ist.

Aufgabe der Erfindung ist es, ein Verfahren und eine Vorrichtung nach den Oberbegriffen der Ansprüche 1 bzw. 10 zu schaffen, die es ermöglichen, in Verbindung mit einer SLIC zu arbeiten, um einen entfernten Leitungstest einzelner Teilnehmerschleifen auszuführen.

Diese Aufgabe wird entsprechend den kennzeichnenden Teilen der Ansprüche 1 bzw. 10 gelöst.

Dadurch wird ein wirtschaftlicher Fern-Leitungstest einzelner Teilnehmerschleifen in einem Telefonsystem geschaffen. Durch einfaches Ausführen von Gleichstromsignalmessungen in der Teilnehmerleitung können viele verschiedene Teilnehmerleitung-Testparameter gemessen werden. Diese Parameter umfassen den Leckwiderstand in der Schleife und den Leckwiderstand zwischen der Schleife und Erde sowie die Leitungskapazität in der Schleife. Ferner können Gleichstromfehler in solchen Messungen aus diesen Messungen wirksam eliminiert werden. Diese Testfähigkeit kann als Teil der Funktion einer Teilnehmerleitung- Schnittstellenschaltung (SLIC) enthalten sein. Dadurch kann eine solche SLIC sowohl eine normale Schnittstellenfunktion als auch eine Testfunktion schaffen, wodurch ein Test implementiert wird, der in bezug auf die Kosten pro Leitung sehr kostengünstig ist.

Weitere Ausgestaltungen der Erfindung sind der nachfolgenden Beschreibung und den Unteransprüchen zu entnehmen.

Die Erfindung wird nachstehend anhand eines in den beigefügten Abbildungen dargestellten Ausführungsbeispiels näher erläutert.

Fig. 1 ist ein funktionaler Blockschaltplan einer Schnittstellenschaltung zur Ausführung lokaler Tests an einer Telefonteilnehmerleitung gemäß einer Ausführung der Erfindung.

Fig. 2 ist ein genauerer funktionaler Blockschaltplan der Schaltung nach **Fig.** 1.

Fig. 3 ist ein Blockschaltplan, der ein bekanntes lokales Telefonsystem zeigt.

Gemäß der in **Fig.** 1 dargestellten Ausführung enthält eine Teilnehmerleitung-Schnittstellenschaltung (SLIC) **10** für die Schaffung einer Schnittstelle für lokale Tests und zur Ausführung lokaler Tests für eine Telefonteilnehmerleitung eine Treiberschaltung **12**, eine Erfassungsschaltung **14** und einen Computer/Controller **16**, die miteinander wie gezeigt verbunden sind. Die Schnittstellen **17**a, **17**b zwischen dem Computer/Controller **16** und der Treiberschaltung **12** und der Erfassungsschaltung **14** ermöglichen dem Computer/Controller **16**, die Treiberschaltung **12** und die Erfassungsschaltung **14** nach Bedarf zu steuern und von der Treiberschaltung **12** und von der Erfassungsschaltung **14** Signale zu empfangen, die verschiedene Testparameter darstellen, wie sie in den Schaltungen **12**, **14** gemessen werden.

Weiterhin schafft die Erfassungsschaltung **14** eine Rückkopplung **15** zur Treiberschaltung **12**.

Gemäß **Fig.** 2 enthält die Treiberschaltung **12** zwei Verstärker **20**a, **20**b, die die einzelnen Teilnehmerleitungen an den Knoten a und b ansteuern. Diese Verstärker **20**a, **20**b werden ihrerseits durch Signale **25**a, **25**b von einem Empfängerverstärkerpuffer **24** angesteuert, die vorher mit dem Rückkopplungssignal **15** von der Erfassungsschaltung **14** gemischt werden. Die Erfassungsschaltung **14** erfaßt Spannungen Va und Vb an den Knoten a bzw. b über Erfassungswiderstände Rs. Eine Vorspannungsstufe **26** erzeugt die Vorspannung Vbat für die verbleibenden Stufen in der SLIC **10**.

Die Funktionsweise dieser Schaltung für die Schaffung einer Schnittstelle für lokale Tests und für die Ausführung lokaler Tests an der Telefonteilnehmerleitung ist die folgende. Es werden einzelne Knotenspannungen Va, Vb erzeugt, wenn einzelne Knotenströme Ia, Ib mit unterschiedlichen Größen in die Knoten a, b fließen. Diese Knotenspannungen Va, Vb werden erzeugt, um in zwei Betriebsarten zu testen: In einer "Vorwärts"-Betriebsart, in der Va > Vb ist; und in einer "Rückwärts"-Betriebsart, in der Va < Vb ist. Die Messungen dieser Spannungen Va, Vb und dieser Ströme Ia, Ib werden ausgeführt und in Verbindung mit der gemessenen Vorspannung Vbat dazu verwendet, den effektiven Leckwiderstand Rab in der Schleife sowie die einzelnen Leckwiderstände Rag, Rbg zwischen den Schleifenknoten a, b und Schaltungserde zu berechnen.

Anhand einer Messung der Spannung Vab zwischen den Knoten a und b, d. h. der Differenz zwischen der Spannung Va am Knoten a und der Spannung Vb am Knoten b, und anhand der Kenntnis der Vorspannung Vbat können einzelne "Vorwärts"-Knotenspannungen Vaf und Vbf (d. h. wenn Va > Vb) sowie einzelne "Rückwärts"-Knotenspannungen Var und Vbr (d. h. wenn Va < Vb) für die Knoten a bzw. b in Übereinstimmung mit den folgenden Gleichungen (1) bis (4) berechnet werden:

$$Vaf = \frac{Vbat}{2} + \frac{Vab}{2} \quad (1)$$

$$Vbf = \frac{Vbat}{2} - \frac{Vab}{2} \quad (2)$$

$$Var = \frac{Vbat}{2} - \frac{Vab}{2} \quad (3)$$

$$Vbr = \frac{Vbat}{2} + \frac{Vab}{2} \quad (4)$$

Anhand dieser berechneten Spannungen Vaf, Vbf, Var, Vbr und des gemessenen Werts der longitudinalen Ströme für die "Vorwärts"-Bedingung (Ilongf) und die "Rückwärts"-Bedingung (Ilongr) können die Beziehungen zu den einzelnen Knoten-nach-Erde-Leckwiderständen Rag, Rbg gemäß den folgenden Gleichungen (5) und (6) dargestellt werden:

$$Ilongf = \frac{Vaf}{Rag} + \frac{Vbf}{Rbg} \quad (5)$$

$$Ilongr = \frac{Var}{Rag} + \frac{Vbr}{Rbg} \quad (6)$$

Aus den Gleichungen (5) und (6) geht hervor, daß der longitudinale "Vorwärts"-Strom Ilongf gleich dem Zwischenknotenstrom Iab ist, wenn die Spannung Vb am Knoten b gleich null ist. In ähnlicher Weise ist der longitudinale Rückwärts-Strom Ilongr gleich dem Zwischenknotenstrom Iab, wenn die Spannung Va am Knoten gleich null ist.

Sobald diese Spannungen Vaf, Vbf, Var, Vbr und die Ströme Ilongf, Ilongr berechnet sind, können die einzelnen Knotennach-Erde-Leckwiderstände Rag, Rbg anhand der folgenden Gleichungen (7) und (8) berechnet werden:

$$Rag = \frac{Vaf \cdot Vbr - Var \cdot Vbf}{Ilongr \cdot Vaf + Ilongf \cdot Var} \quad (7)$$

$$Rbg = \frac{Vbf \cdot Var - Vbr \cdot Vaf}{Ilongr \cdot Vbf + Ilongf \cdot Vbr} \quad (8)$$

Der Zwischenknoten-Leckwiderstand Rab kann anhand der folgenden Gleichung (9) berechnet werden:

$$Rab = \frac{Vab}{Iab} \quad (9)$$

Zusätzlich zu den obenbeschriebenen Messungen der Gleichstromparameter auf der Teilnehmerleitung kann diese Technik auch eine Messung für die Kapazität Cab zwischen den Knoten a und b schaffen. Dies kann durch Schicken eines kleinen Teststroms Itest anstelle des normalen Eingangsstroms Iin in den Empfängerverstärkerpuffer **24** (**Fig.** 1 und 2), der verstärkt und als Zwischenknotenstrom Iab in die Teilnehmerleitungsknoten a, b eingegeben wird, erzielt werden. Durch Messen der Änderungsrate der Zwischenknotenspannung Vab kann die Zwischenknotenkapazität Cab anhand der folgenden Gleichung (10) berechnet werden:

$$Cab = \frac{Iab \cdot \Delta t}{\Delta Vab} \quad (10)$$

Um die Wirkung des Zwischenknotenswiderstandes Rab zu beseitigen, kann der Wert des Zwischenknotenstroms Iab für das ausgewählte Zeitintervall Δt skaliert werden, wie in Gleichung (10) gezeigt ist. Durch eine geeignete Skalierung des Teststroms Itest anhand der momentanen Teilnehmerleitungs-Spannungs- und Teilnehmerleitungsstromstandards kann eine Zwischenknotenkapazität Cab im Bereich von 10 nF bis 5 µF gemessen werden.

Aus der obigen Beschreibung wird eine Anzahl von Vorteilen der beschriebenen Technik deutlich. Aus den in den Gleichungen (1) bis (6) dargestellten Beziehungen geht hervor, daß die Gleichstromfehler in den Messungen durch Umkehren der relativen Polaritäten der Spannungen Va, Vb an den Teilnehmerleitungsknoten a, b eliminiert werden können. Weiterhin können dann, wenn die vom Computer/Controller **16** bei der Ausführung dieser Berechnungen verwendeten

Algorithmen eine Mittelung der gemessenen Signale vornehmen, die Auswirkungen der Wechselstromsignale, die in der Leitung induziert werden könnten, beseitigt werden. Ebenso können Hochspannungssignale aufgrund irgendeines Fehlerzustandes in der Leitung erfaßt werden.

Patentansprüche

1. Verfahren zur Schaffung einer Schnittstelle für lokale Tests und zur Ausführung lokaler Tests an einer Telefonteilnehmerleitung und zum Bestimmen mehrerer elektrischer Eigenschaften einer solchen Telefonteilnehmerleitung,
gekennzeichnet durch,
Erzeugen einer ersten und einer zweiten Spannung (Va, Vb) an einem ersten bzw. einem zweiten Telefonteilnehmerleitungsknoten (a, b),
Messen der ersten und der zweiten Spannung (Va, Vb),
Ausgeben eines ersten und eines zweiten Stroms (Ia, Ib) über den ersten bzw. den zweiten Telefonteilnehmerleitungsknoten (a, b),
Messen des ersten und des zweiten Stroms (Ia, Ib),
Berechnen eines ersten Widerstandes (Rag) zwischen dem ersten Telefonteilnehmerleitungsknoten (a) und einem Referenzknoten als eine erste Funktion der gemessenen ersten und zweiten Spannungen (Va, Vb) und der gemessenen ersten und zweiten Ströme (Ia, Ib),
Berechnen eines zweiten Widerstandes (Rbg) zwischen dem zweiten Telefonteilnehmerleitungsknoten (b) und dem Referenzknoten als eine zweite Funktion der gemessenen ersten und zweiten Spannungen (Va, Vb) und der gemessenen ersten und zweiten Ströme (Ia, Ib), und
Berechnen eines dritten Widerstandes (Rab) zwischen dem ersten und dem zweiten Telefonteilnehmerleitungsknoten (a, B) als eine dritte Funktion der gemessenen ersten und zweiten Spannungen (Va, Vb) und der gemessenen ersten und zweiten Ströme (Ia, Ib).
2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß der Schritt des Messens der ersten und zweiten Spannungen (Va, Vb) das Messen der ersten und der zweiten Spannung (Va, Vb) enthält, wenn die erste Spannung (Va) größer als die zweite Spannung (Vb) ist.
3. Verfahren nach Anspruch 2, dadurch gekennzeichnet, daß der Schritt des Messens der ersten und zweiten Spannungen (Va, Vb) das Messen der ersten und der zweiten Spannung (Va, Vb) enthält, wenn die erste Spannung (Va) kleiner als die zweite Spannung (Vb) ist.
4. Verfahren nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, daß der Schritt des Messens der ersten und zweiten Ströme (Ia, Ib) das Messen des ersten und des zweiten Stroms (Ia, Ib) enthält, wenn die erste Spannung (Va) größer als die zweite Spannung (Vb) ist.
5. Verfahren nach Anspruch 4, dadurch gekennzeichnet, daß der Schritt des Messens der ersten und zweiten Ströme (Ia, Ib) das Messen des ersten und des zweiten Stroms (Ia, Ib) enthält, wenn die erste Spannung (Va) kleiner als die zweite Spannung (Vb) ist.
6. Verfahren nach einem der Ansprüche 1 bis 5, dadurch gekennzeichnet, daß der Schritt des Messens der ersten und zweiten Ströme (Ia, Ib) das Messen der ersten und des zweiten Stroms (Ia, Ib) enthält, wenn die erste und die zweite Spannung (Va, Vb) im wesentlichen den gleichen Wert haben.
7. Verfahren nach einem der Ansprüche 1 bis 6, dadurch gekennzeichnet, daß der Schritt des Messens der ersten und zweiten Ströme das Messen des ersten und des zweiten Stroms (Ia, Ib) enthält, wenn die zweite Spannung (Vb) im wesentlichen gleich einer Referenzspannung am Referenzknoten ist.
8. Verfahren nach einem der Ansprüche 1 bis 7, gekennzeichnet durch
Ausgeben eines Teststroms über einen der ersten und zweiten Telefonteilnehmerleitungsknoten (a, b) während eines Zeitintervalls,
Messen des Teststroms (Itest),
Messen der ersten und zweiten Spannungen (Va, Vb) während des Zeitintervalls,
Berechnen einer Spannungsdifferenz (Vab) zwischen den gemessenen ersten und zweiten Spannungen (Va, Vb) während des Zeitintervalls, und
Berechnen einer Kapazität (Cab) zwischen dem ersten und dem zweiten Telefonteilnehmerleitungsknoten (a, b) als Funktion der berechneten Spannungsdifferenz (Vab) und des Teststroms (Itest).
9. Verfahren nach Anspruch 8, dadurch gekennzeichnet, daß der Teststrom (Itest) skaliert wird.
10. Vorrichtung, die eine Teilnehmerleitung-Schnittstellenschaltung mit einer Selbsttestfähigkeit zum Ausführen lokaler Tests an einer Telefonteilnehmerleitung und zum Bestimmen mehrerer elektrischer Eigenschaften einer solchen Telefonteilnehmerleitung enthält,
dadurch gekennzeichnet, daß die Teilnehmerleitung-Schnittstellenschaltung enthält:
eine Treiberschaltung (**12**), die so beschaffen ist, daß sie
eine Telefonteilnehmerleitung an einen ersten Knoten (a) und an einen zweiten Knoten (b) anschließt und enthält:
einen ersten Widerstand (Rag) zwischen dem ersten Telefonteilnehmerleitungsknoten (a) und einem Referenzknoten,
einen zweiten Widerstand (Rbg) zwischen dem zweiten Telefonteilnehmerleitungsknoten (b) und dem Referenzknoten und
einen dritten Widerstand (Rab) zwischen dem ersten und dem zweiten Telefonteilnehmerleitungsknoten (a, b),
erste und zweite Spannungen (Va, Vb) am ersten bzw. am zweiten Telefonteilnehmerleitungsknoten (a, b) erzeugt und
erste und zweite Ströme (Ia, Ib) über den ersten bzw. den zweiten Telefonteilnehmerleitungsknoten (a, b) ausgibt,
eine Erfassungsschaltung (**14**), die so beschaffen ist, daß sie

an den ersten und den zweiten Telefonteilnehmerleitungsknoten (a, b) angeschlossen ist,
die ersten und zweiten Spannungen (Va, Vb) mißt und
die ersten und zweiten Ströme (Ia, Ib) mißt, und
einen Computer (**16**), der an die Treiberschaltung (**12**) und an die Erfassungsschaltung (**14**) angeschlossen ist, und so beschaffen ist, daß er
den ersten Widerstand (Rag) als eine erste Funktion der gemessenen ersten und zweiten Spannungen (Va, Vb) und der gemessenen ersten und zweiten Ströme (Ia, Ib) berechnet,
den zweiten Widerstand (Rbg) als eine zweite Funktion der gemessenen ersten und zweiten Spannungen (Va, Vb) und der gemessenen ersten und zweiten. Ströme (Ia, Ib) berechnet, und
den dritten Widerstand (Rab) als eine dritte Funktion der gemessenen ersten und zweiten Spannungen (Va, Vb) und der gemessenen ersten und zweiten Ströme (Ia, Ib) berechnet.

11. Vorrichtung nach Anspruch 10, dadurch gekennzeichnet, daß die Erfassungsschaltung (**14**) so beschaffen ist, daß sie die ersten und zweiten Spannungen (Va, Vb) mißt, wenn die erste Spannung (Va) größer als die zweite Spannung (Vb) ist.

12. Vorrichtung nach Anspruch 11, dadurch gekennzeichnet, daß die Erfassungsschaltung (**14**) so beschaffen ist, daß sie die ersten und zweiten Spannungen (Va, Vb) mißt, wenn die erste Spannung (Va) kleiner als die zweite Spannung (Vb) ist.

13. Vorrichtung nach einem der Ansprüche 10 bis 12, dadurch gekennzeichnet, daß die Erfassungsschaltung (**14**) so beschaffen ist, daß sie die ersten und zweiten Ströme (Ia, Ib) mißt, wenn die erste Spannung (Va) größer als die zweite Spannung (Vb) ist.

14. Vorrichtung nach Anspruch 13, dadurch gekennzeichnet, daß die Erfassungsschaltung (**14**) so beschaffen ist, daß sie die ersten und zweiten Ströme (Ia, Ib) mißt, wenn die erste Spannung (Va) kleiner als die zweite Spannung (Vb) ist.

15. Vorrichtung nach einem der Ansprüche 10 bis 14, dadurch gekennzeichnet, daß die Erfassungsschaltung (**14**) so beschaffen ist, daß sie ersten und zweiten Ströme (Ia, Ib) mißt, wenn die ersten und zweiten Spannungen (Va, Vb) im wesentlichen den gleichen Wert besitzen.

16. Vorrichtung nach einem der Ansprüche 10 bis 15, dadurch gekennzeichnet, daß die Erfassungsschaltung (**14**) so beschaffen ist, daß sie die ersten und zweiten Ströme (Ia, Ib) mißt, wenn die zweite Spannung (Vb) im wesentlichen gleich einer Referenzspannung am Referenzknoten ist.

17. Vorrichtung nach einem der Ansprüche 10 bis 16, dadurch gekennzeichnet, daß
die Treiberschaltung (**12**) so beschaffen ist, daß sie
- während eines Zeitintervalls einen Teststrom (Itest) über einen der ersten und zweiten Telefonteilnehmerleitungsknoten (a, b) ausgibt,

die Erfassungsschaltung (**14**) so beschaffen ist, daß sie
- den Teststrom (Itest) mißt und die ersten und zweiten Spannungen (Va, Vb) während des Zeitintervalls mißt, und

der Computer so beschaffen ist, daß er
- eine Spannungsdifferenz (Vab) zwischen den gemessenen ersten und zweiten Spannungen (Va, Vb) während des Zeitintervalls berechnet und
- eine Kapazität (Cab) zwischen den ersten und zweiten Telefonteilnehmerleitungsknoten (a, b) als eine Funktion der berechneten Spannungsdifferenz (Vab) und des Teststroms (Itest) berechnet.

18. Vorrichtung nach Anspruch 17, dadurch gekennzeichnet, daß die Treiberschaltung (**12**) so beschaffen ist, daß sie den Teststrom skaliert.

Hierzu 2 Seite(n) Zeichnungen

- Leerseite -

Nummer: DE 199 14 858 A1
Int. Cl.[6]: H 04 M 3/30
Offenlegungstag: 14. Oktober 1999

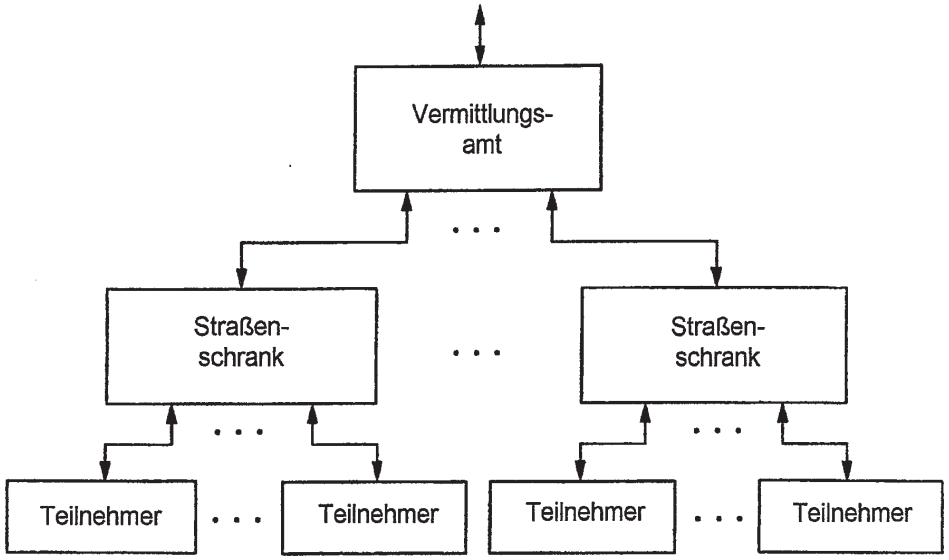

Fig. 3

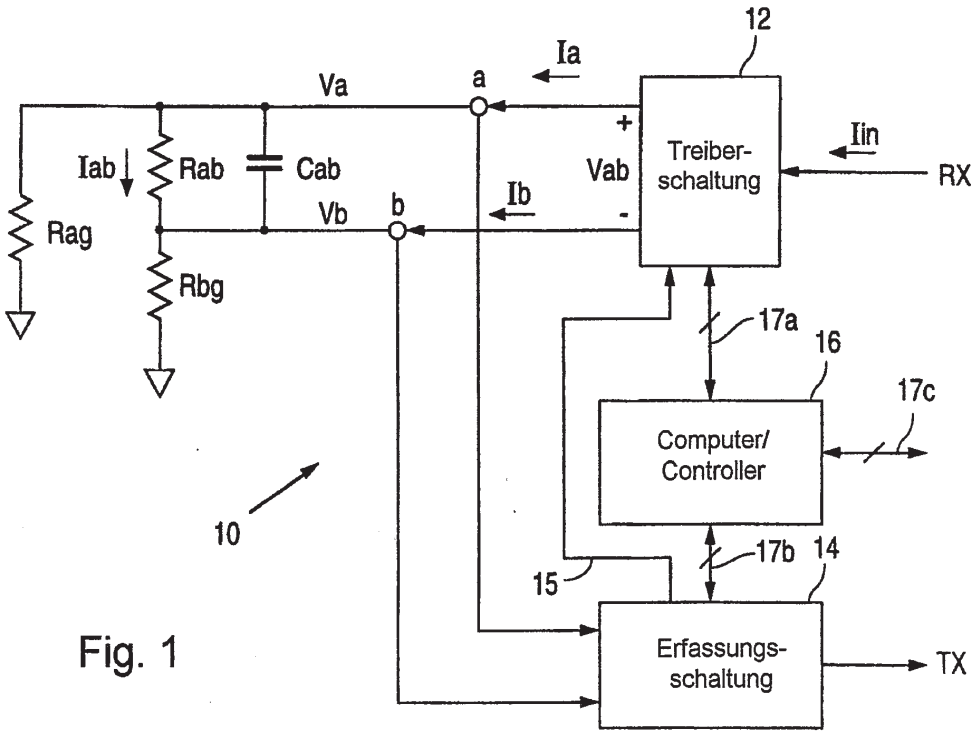

Fig. 1

Nummer: DE 199 14 858 A1
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Offenlegungstag: 14. Oktober 1999

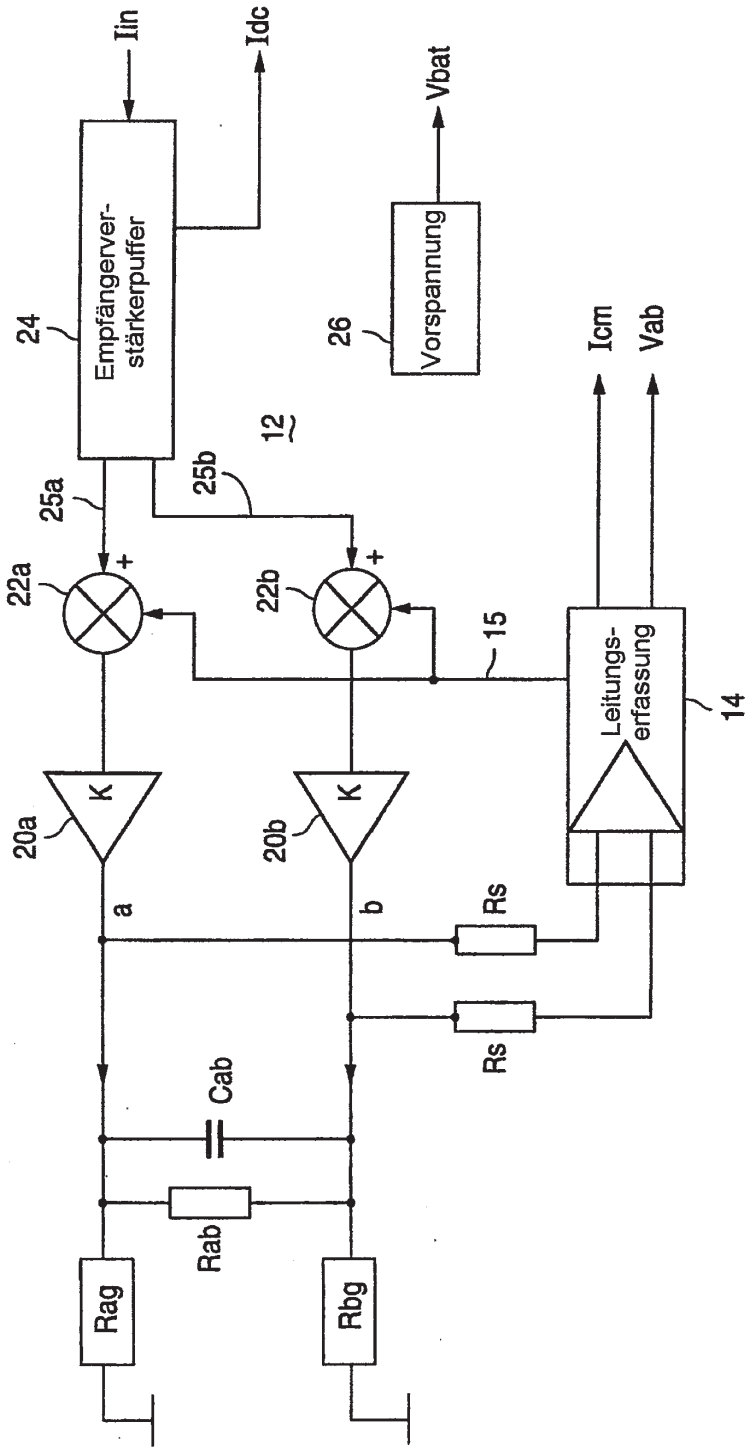


Fig. 2

902 041/792

Patent Committee Presentation

Method of subscriber line testing via solid State SLIC circuit.

Inventors: Duncan J Bremner; Telecom Products; CCG Division, NSUK

1. General Overview

The invention is designed to operate as part of a Subscriber Line Interface Circuit (SLIC) system which will allow operation of said SLIC to carry out functional line testing of the subscriber loop without requiring a dedicated test buss connecting to specialised test equipment as presently. This is possible due to the high integration abilities of VIP4H, and the sophisticated drive and programming abilities of the DSP Combo control device.

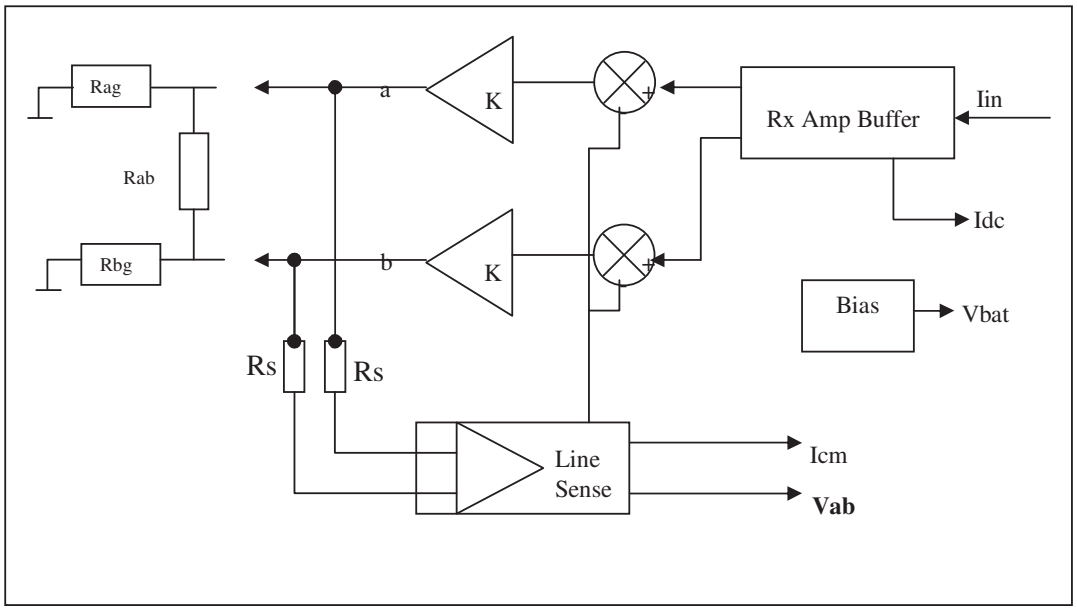
This SLIC component resides either in the Central Office or a streetside cabinet, and is responsible for terminating, powering, signalling and transmission of a subscriber telephone line pair of wires. In a CO, the cost of the test equipment can be defrayed across many lines, but in a small line concentrator(as small as 4), this gets prohibitive. The ability to do remote, built in line testing is therefore very attractive.

Products to use the Invention

The invention was developed for use in the Global Linecard Circuit being designed in the Telecom Products Group. This product is estimated to generate $155 M in revenue over next 5 years(TP3250 NPPRS; Phase 4 revision). NPPRS available if required. Any customer derivative products for SLIC devices are likely to use this invention.

2. Closest Prior Art

The closest existing prior art is an idea from Siemens Semiconductor on device PEB3465 but does not offer all the testing functions available using the GLC. Presently, they are the only competitor offering this feature. GLC offers, over the transmission level testing offered by Siemens, the ability to measure currents and voltages which can be used to



calculate fault conditions on the subscriber line. There are no other products offering the test features available here.

4. Block Diagram

The invention functions as follows:

1. The HV SLIC device is capable of switching 4 different analog signals to the transmit amplifier under the control of the digital control interface. These signals are, sensed in relatively conventional ways, but are combined to allow subscriber loop diagnostics:-

i. The instantaneous Vab voltage across the subscriber loop,

ii. The common mode or longitudinal current flowing in the subscriber wires,

iii. The DC value of the loop current flowing from ‘a’ to ‘b’, and

iv. The battery voltage supplied to the device.

Using these measurements, a variety of subscriber line test parameters can be measured as normal DC measurements on the subscriber line. These include the leakage resistance

from wire'a' to wire'b'(Rab), or the resistance from 'a' or 'b' to ground, Rag or Rbg respectively. Additionally, the DC errors in the measurement can be nulled out from the measurements by reversing polarity on the 'a' and 'b' nodes and incorporating these terms in the calculations such that they cancel. Based on this approach, the above 3 terms can be calculated from the following equations:-

In the forward direction, Va >Vb

1. Vaf = (Vbat/2) + (Vab/2)

2. Vbf = (Vbat/2) – (Vab/2)

And in the reverse direction; Va < Vb

3. Var = (Vbat/2) – (Vab/2)

4. Vbr = (Vbat/2) + (Vab/2)

In addition, the longitudinal current measurement yields:-

Ilongf = (Vaf/Rag) + (Vbf/Rbg) for forward

Ilongr = (Var/Rag) + (Vbr/Rbg) for reverse

From these the resistances to ground are calculated thus:

Rbg = [Vaf*Vbr – Var*Vbf] / [Ilongr*Vaf + Ilongf*Var]

Rbg = [Vbf*Var – Vbr*Vaf] / [Ilongr*Vbf – Ilongf*Vbr]

And resistance between 'a' and 'b' wires is:

Rab = Vab / Iab

From the above measurements, the resistances Rag, Rbg, Rab can be calculated

In addition to the measurement of the DC parameters on the line, the system is also capable of measuring the capacitance connected between 'a' and 'b' wires. This is achieved by applying a small test current at the Iin input of the Rx Amp buffer block This is amplified via the various signal amplifier blocks, and applied to the subscriber line terminals, 'a', 'b'. Via the test measurement, Vab, the rate of change of voltage may be measured, and the line capacitance calculated. This can be done by the expression:-

$$\mathbf{C = I * \Delta t / \Delta Vab}$$ where $\mathbf{\Delta t}$ is time interval between Vab measurements and $\mathbf{\Delta Vab}$ is change in voltage.

In order to eliminate the effective of parallel resistance modifying the result, the value of '**I'** can be scaled to maintain linearity in the measurements. This ability to measure line capacitance is unique on a SLIC device, and by scaling the test current, this allows a range of between 10nF and 5uF to be measured.

1. General Points of Interest

If this invention is compared to that cited by Siemens, the key advantages are that this procedure allows measurement of capacitance and resistances of the subscriber loop, whereas the Siemens solution only provides a means of measuring the transmission levels.

Furthermore, if the algorithms in the board controller are modified to incorporate averaging of the signals measured, the effects of AC induction on the line are removed from the calculations. Similarly, the presence of high voltage (mains) signals due to a fault condition on line may be derived.

Finally, given the drive towards remote concentrators etc in the field, where the cost of dedicated test equipment would be prohibitive, this solution allows operating companies to provide a per line test capability at a very economic cost.

Submission VIII

Type	Reference	Title
Product Datasheet & IIC Conference Paper	TP3250	A. TP3250 Programmable SLIC; Preliminary datasheet. B. Next Generation Subscriber Line Interface Solutions (International IC China Conference, Shanghai, 1998)
Citations	**Not Known**	

National Semiconductor

Preliminary Information
August 1997

TP3250
Programmable SLIC

General Description

The TP3250 is a single chip monolithic programmable Subscriber Line Interface Circuit built with National's advanced 170V high voltage bipolar process. The device is designed to operate over a wide voltage range and provide on-chip balanced ring feed to the subscriber line. It also supports external ring feed using a ring relay and ring sense bridge. The line feed characteristics, supervision thresholds and operating modes are programmable through a simple parallel control interface. It supports loop start, ground start, silent battery reversal and metering pulse signalling. Advanced power management may be implemented with an on-chip battery switching feature.

The TP3250 must be protected from over-voltage by an external shunt protector together with an external series current limiting network. Transmission performances are independent of the matching of the series external network.

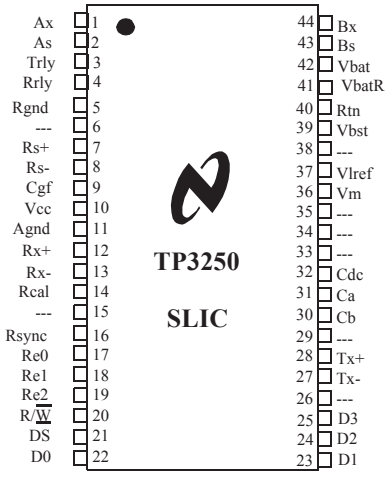
When used with National's TP3090 Quad Programmable PCM Codec/Filter COMBO® IV, the TP3250 forms a software configurable line circuit, handling all the BORSCHT functions.

Features

- On-chip balanced ring feed
- Supports balanced or unbalanced external ringing.
- Flexible power management
- Battery boost mode for loop range extension
- Thermal overload protection
- Withstands ±200 V transient between battery return and analog ground
- Transmission performance independent of external protection resistors
- Software programmable:
  - feed resistance, current limit, operating modes and signalling thresholds
- Operating modes:
  - scan, active, ring and power denial
- Signalling:
  - loop start, ground start, quiet battery reversal and metering
- On-hook transmission
- Test Modes
- Simple parallel control interface
- Single +5V low voltage supply
- Surface-mount power package

Connection Diagram

PSOP3 Package



Top View
Order Number TP3250
See NS Package Number (MWC 44A)

COMBO is a registered trademark of National Semiconductor Corporation

Simplified Block Diagram:

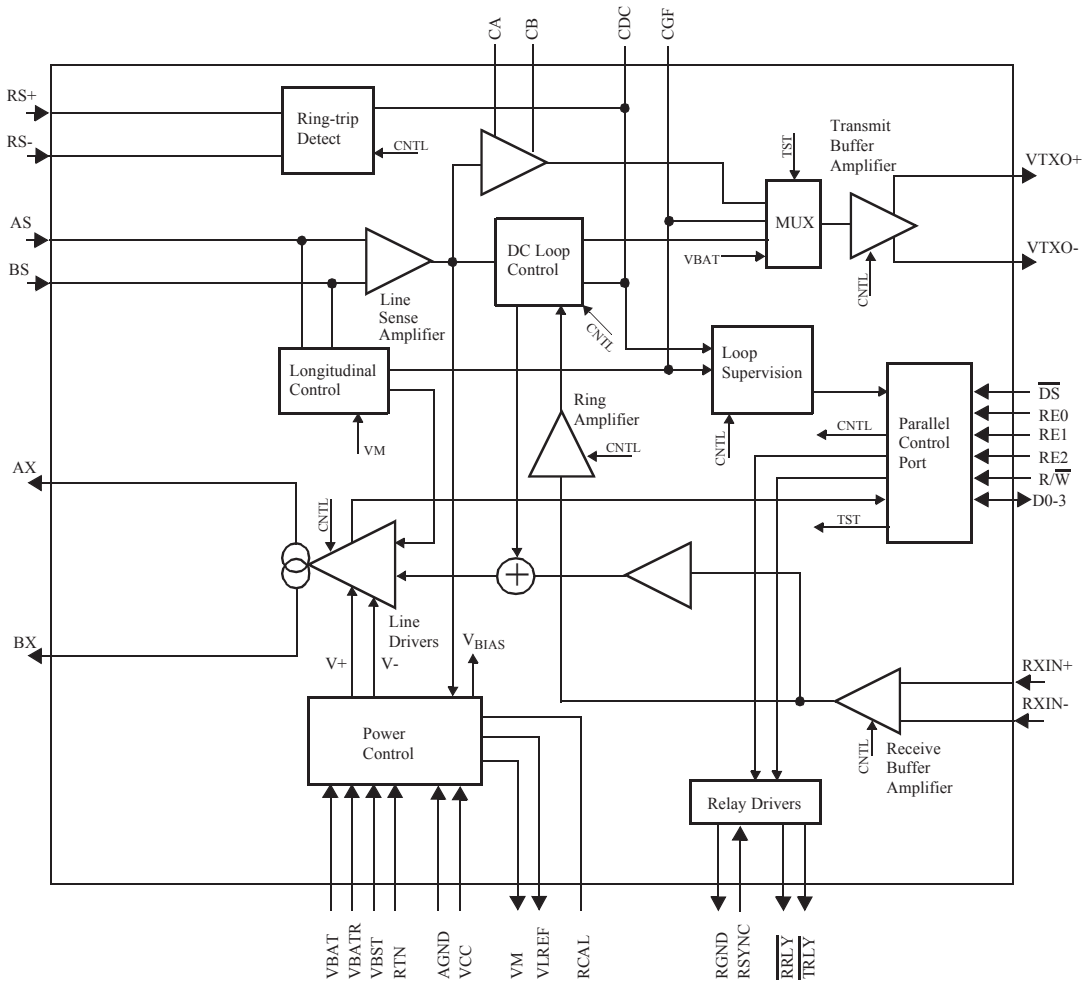


Figure 1. Simplified block diagram

Pin Descriptions

AX, BX
High voltage line driver outputs. AX and BX provide battery feed and on-chip balanced ring feed to the A and B leads of the subscriber loop through a pair of external protection resistors. AX is positive with respect to BX in forward battery.

AS, BS
Line sense inputs. AS and BS are connected to the A and B leads respectively through a pair of external protection resistors. AS and BS sense the line voltage across the A and B leads.

VBAT
Negative high voltage battery supply.

VBATR
Optional reduced battery supply for power dissipation reduction on short loops. VBATR is nominally half of VBAT for effective power management. Alternatively, an external power resistor may be connected from VBATR pin to VBAT for reducing internal power dissipation.

VBST
Positive high voltage supply. VBST is needed for on-chip ring feed or battery boost mode for loop range extension. The potential difference between VBST and VBAT must be less than 142V If a positive high voltage supply is not available, VBST should be connected to RTN.

RTN
High voltage ground return. VBAT, VBATR and VBST are referenced to RTN.

VM
High voltage common-mode reference output. A capacitor is connected from CDC1 to VM for dc loop filtering.

VLREF
Power Control Reference.

RS+, RS-
Ring Trip detection inputs for use with an external ring feed through a ring relay. RS+ and RS- are enabled during ring mode. An external resistive bridge connected to RS+ and RS- is used for ring-trip detection.

CDC
A capacitor connected from CDC1 to VM, together with an internal resistor, forms a low pass filter for the dc feed control. The RC time constant determines the feed inductance.

CGF
A capacitor is connected from CGF to AGND for ground fault detection filtering.

RCAL
A resistor connected from RCAL to AGND determines the internal bias current. RCAL should be 120 KΩ ±1%.

$\overline{\text{RRLY}}$
Open collector output driver for an optional external ring relay. In the external Ring mode, $\overline{\text{RRLY}}$ is turned on a high level on RSYNC. After ring trip detection, $\overline{\text{RRLY}}$ is turned off under system control. RRLY is internally voltage limited to approximately 15V.

$\overline{\text{TRLY}}$
Open collector output driver for optional external test relays. TRLY is internally voltage limited to approximately 15V.

VCC
Low voltage positive supply. V_{CC}=+5V ±5%.

AGND
Low voltage ground. V_{CC}, logic signals, and low voltage analog signals are referenced to AGND.

RGND
Low voltage ground return for relay current.

Pin Descriptions (continued)

CA, CB
A capacitor is connected between CA and CB for separating the ac transmit signals from the dc component of the line voltage.

VTXO-, VTXO+
Inverting and non-inverting outputs of the differential transmit buffer amplifier. They are referenced to an internal reference voltage of approximately 2.25V. VTXO- and VTXO+ are connected to the VXI+ and VXI- differential transmit inputs of the TP3090 COMBO IV.

RXIN-, RXIN+
Inverting and non-inverting differential current inputs of the receive buffer amplifier. RXIN- and RXIN+ connect to the VRO+ and VRO- differential receive outputs of the TP3090 COMBO IV.

Logic Pins:

$\overline{\text{DS}}$
Device select logic input. Must be logic low to enable control data to be latched into the selected register and data to be enabled on the data bus.

RE0, RE1, RE2
Register select logic inputs. When $\overline{\text{DS}}$ is low, RE0,RE1 and RE2 enable communication to/from one of the internal registers.

R/$\overline{\text{W}}$
Read/Write selection, when this pin is LOW a write access is operated on the device access interface, when it is HIGH a read access is operated.

D0-D3
Control Bus, bidirectional. During $\overline{\text{DS}}$ LOW, data on this bus are written/read on/from an internal register.

RSYNC
Ring Synchronization logic input. RSYNC is a logic signal generated by an external zero crossing detector that monitors the ringing voltage. It is used to synchronize the closing of the external ring relay at the zero crossing of the ringing voltage to minimize impulse noise and possible relay contact arcing. If RSYNC is not used, and external ringing is applied, it should be tied high, otherwise it should be tied to AGND.

Functional Description

The TP3250 is a third generation single chip monolithic SLIC implemented with National's advanced 170V high voltage and high density bipolar process. The operating modes and line feed characteristics are selectable through a simple parallel control interface. When used in conjunction with National's TP3090 COMBO IV - Quad Programmable PCM Codec/Filter, the TP3250 forms a fully software configurable line circuit, adaptable to world-wide requirements.

The TP3090 COMBO IV is optimized for use with the TP3250 Programmable SLIC, supporting advanced features such as on-chip ringing, metering pulse shaping, filtering and level control, as well as line diagnostics and self test.

System commands are downloaded from the line card controller to the COMBO IV, and transferred to four TP3250 SLICs via the common Parallel Control Port. Status information is transferred from the TP3250 to the COMBO IV and uploaded to the line card controller. Figure 2 shows the implementation of line circuits using four TP3250 SLICs and a TP3090 COMBO IV.

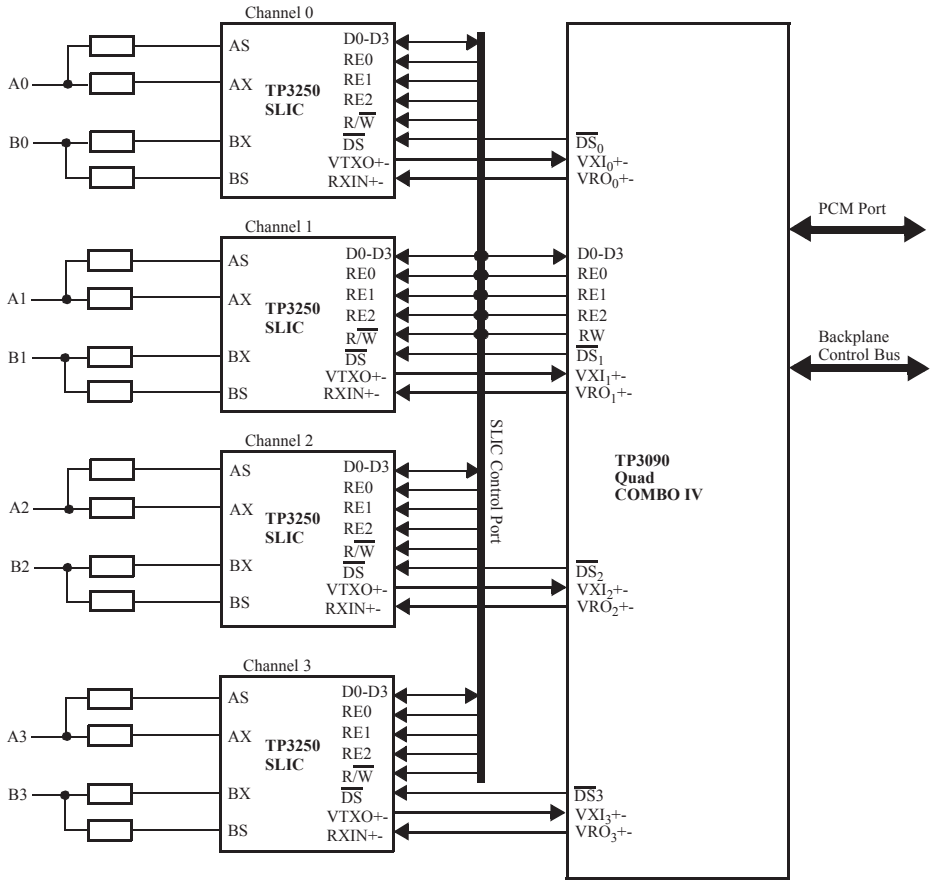


Figure 2. Typical line circuit implementation using the TP3250 SLIC and TP3090 COMBO IV.

Parallel Control Port

The parallel control port is used to program the operating modes and feed characteristics, or read back the status, of the TP3250. The control port consists of the following signals

- $\overline{DS}$, chip select (input)

- R/$\overline{W}$, read/write signal (input)

- RE0,RE1,RE2, register address (input)

- D0,D1,D2,D3, data signals (input/output).

During $\overline{DS}$ low, RE0, RE1 and RE2 select the slic internal register to be accessed and RW the kind of access (read or write).

The slic contains the following 4bits registers

Mode Register, MD

Current Limit Register, CLR

Loop Feed Register 1, LFR1

Loop Feed Register 2, LFR2

Test Mode Register, TMR

Loop Status Register, LSR

addressed according to the following table

RE0	RE1	RE2	Register
0	0	0	Loop Status Register (LSR)
1	0	0	Mode Register (MD)
0	1	0	Loop Feed Register 1 (LFR1)
1	1	0	Loop Feed Register 2 (LFR2)
0	0	1	Test Mode Register (TMR)
1	0	1	Current Limit Register (CLR)

When power is first applied, power on reset circuitry puts the TP3250 into a default operating state. The user may then program the device to the desired operating configuration and mode. When V_{CC} falls below approximately 3V, the power on reset circuitry activates and puts the device into the default operating state. The previously programmed contents of the registers will be lost and the device must be re-programmed when the proper voltage is re-established. Detailed register and default state definitions may be found in the section under "Programming Information".

Write/Read Operation

An access to any register of the slic is performed according to the following figures

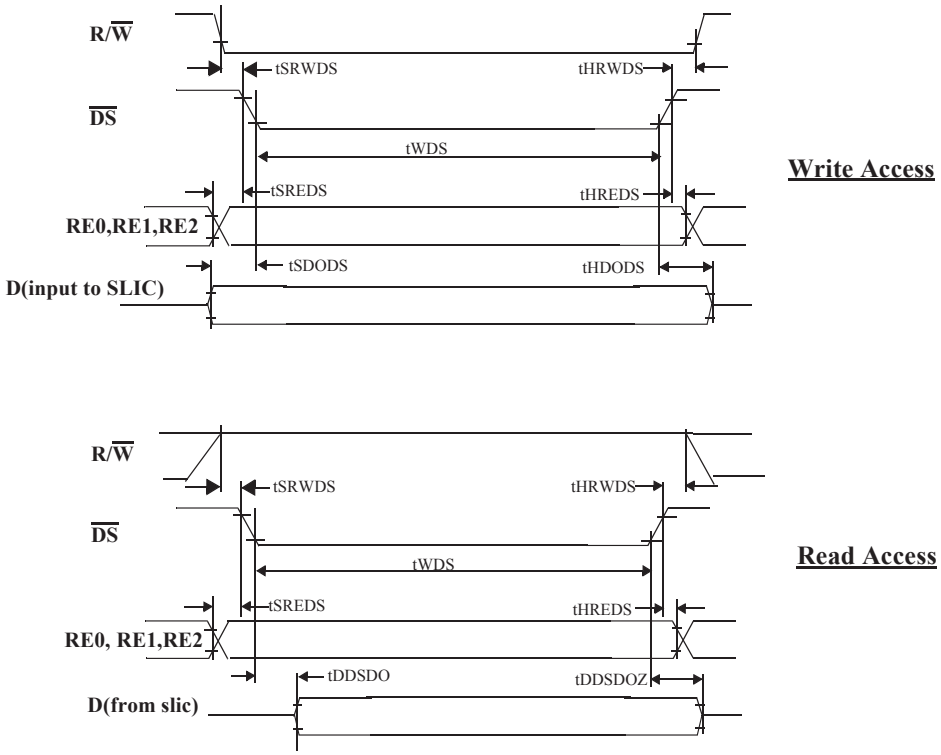


Figure 3

where the timing parameters are specified in the Electrical Characteristic table.

The interface does not only operate in the above latched mode, but also in the transparent mode. When $\overline{DS}$ is active, any register can be accessed by driving properly the REi signals and the R/$\overline{W}$ select (for read and write), and placing the desired value on D0-3, for writing, or allowing the slic to place the selected register's content on the bus, see figure 4.

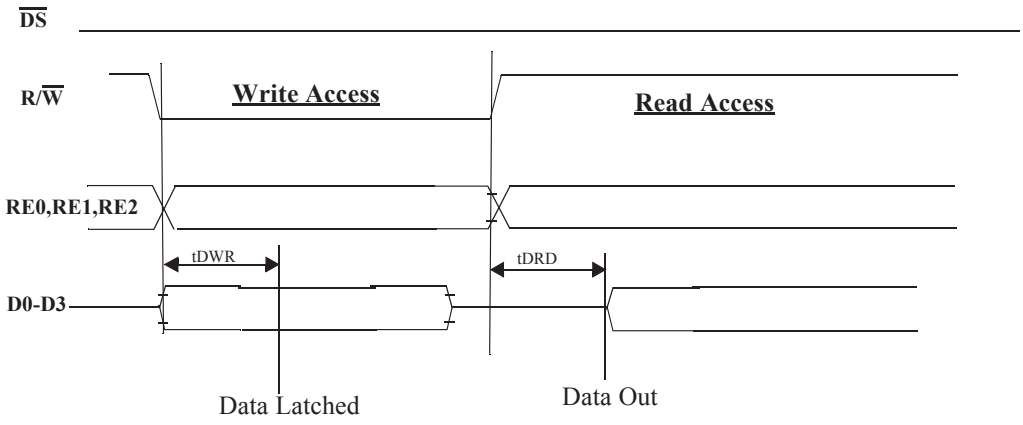


Figure 4

Operating Modes

The TP3250 may be programmed into the following operating modes:

1. Scan Mode (Forward battery only)
2. Active Mode
3. Ground Start Mode
4. Power Denial Mode
5. On chip Ring Mode
6. Off Chip Ring Mode

Scan Mode

When the subscriber is on-hook, the TP3250 may be programmed to the Scan mode to reduce idle power consumption. The Scan mode is activated by programming the Mode Register. In the Scan mode, all non-essential circuitry is powered off to maintain a very low idle power of typically 25 mW. The line sense amplifier, longitudinal and dc control, transmit and receive buffer amplifiers are de-activated. The line drivers operate at reduced current levels and the outputs are current limited to approximately 10 mA. The open circuit line voltage is approximately 4V below VBAT. Figure 5 shows the dc feed characteristics of the Scan mode.

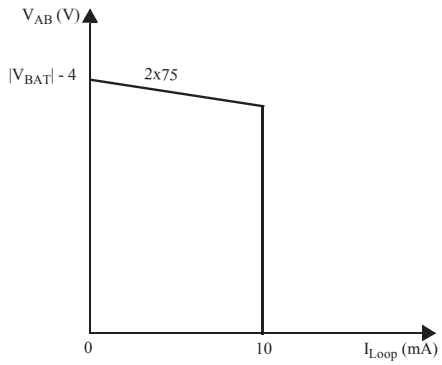


Figure 5. DC feed characteristics in the Scan mode.

Because the longitudinal control is disabled, longitudinal capability is reduced and the SLIC may be subject to false off-hook indications. For lines subjected to more than 7mArms longitudinal induction in each of the A and B wires, the Active mode may be used. Alternatively, the Scan mode may be used and the off-hook indication re-examined after the device is placed into the Active mode.

Active mode

When off-hook is detected, the Mode Register is normally written to enable the Active mode. In this mode, all circuits are fully powered, and the device is ready for transmission. The Active mode is also used during on-hook transmission.

The line driver outputs, AX and BX, provide dc battery feed to the subscriber loop through an external protection resistor network. Feedback circuitry is used to monitor the line voltage via the line sense inputs, AS and BS. The TP3250 synthesizes a resistive/inductive feed characteristics on long loops and constant current feed on short loops. Both the feed resistance and current limit are selectable through the internal Registers. The RC time constant formed by an internal resistor R_{DC}, nominally 500KΩ, and an external capacitor, C_{DC1}, determines the feed inductance. A C_{DC1} value of 0.22µF is recommended. The external protection resistors are located within a feedback loop, hence, and do not contribute to the effective feed resistance. Figure 6 shows a typical family of dc feed characteristics.

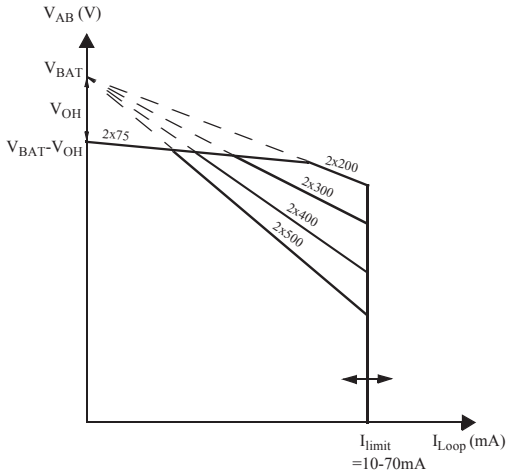


Figure 6. DC feed characteristics in the Active mode

The line drivers require enough headroom to handle the maximum signal levels without distortion. The headroom of the line drivers is adjusted depending on the metering pulse amplitude selected. VOH0-1 of the Line Feed Register 1 determine the headroom V_{OH} to support one of three options, None, 2.5Vrms or 5.0Vrms metering levels.

Ground Start Mode

The Ground Start mode is activated by programming the Mode Register. The Ground Start mode is a signal-

ling only mode that operates in forward or reverse battery states. In this mode, the mostpositive line driver, normally AX, is turned off, producing a high output impedance, and the line sense input for the positive most line, normally AS, is disconnected and internally connected to a reference voltage. This results in the normal voltage being applied to the negative most wire, normally B, and current flowing from the negative wire to ground appears internally as if it were loop current

In the addition, other non-critical circuits operate on reduced current or are powered off to maintain a low idle power of typically 40mW. The TP3250 is capable of operating with 30mArms of longitudinal current in the negative most wire. Transmission is inhibited.

OH of the Status Register indicates the ground start status and may be read through the Parallel Control Port. After the subscriber goes off-hook, the Mode Register may be written to enable the Active mode. The device is now ready for transmission.

Power Denial Mode

The Power Denial mode is entered by programming the Mode Register or by the occurrence of a thermal shutdown. In the Power Denial mode both line drivers are disabled and the AX and BX outputs are in a high impedance state, denying battery feed to the subscriber.

Thermal Shutdown

The line drivers have built-in thermal overload detection circuitry. In the event of a fault or external excitation on the subscriber line that causes the line drivers to over-heat and reach an internal junction temperature of approximately 160^{o}C, the line drivers will protect themselves by forcing the SLIC into Power Denial. The SLIC will remain in Power Denial after the thermal overload condition ceases to exist. After the fault has been serviced, the device may be programmed back to the normal operating mode under system control.

Ring Mode

The TP3250 supports both on-chip ring feed and external ring feed using a relay. The ringing method is selected by the logic state of RING-SEL of the LFR2 Register. A logic low on RING-SEL selects on-chip ringing, a logic high selects external ringing.

On-chip Ring Feed

When the Ring mode is enabled, the line drivers are powered from VBST and VBAT, and the battery switching mechanism is disabled. The feed resistance is forced to 2x75Ω, the current limit is forced to 70mA, and the feed inductance is bypassed. The internal current gain from RXIN+ and RXIN- to the subscriber line is increased. Both the ac and dc ring voltage of the line may be controlled via the RXIN+ and RXIN- inputs.

The TP3090 COMBO IV is optimized to work with the TP3250 for on-chip ringing and other enhanced features. The COMBO IV has the capability of generating both the dc offset and the ac low level ringing voltage. The ringing voltage is always applied and removed at the zero crossings of the ringing voltage.

Figure 7 shows the waveforms for on-chip ring feed. Both the open circuit line voltage and the ac ringing amplitude may be adjusted by the users.

When on-hook transmission is not required, the COMBO IV controls the ringing cadence by alternately applying and removing the ac ringing voltage. The dc offset is kept constant, maintaining a fixed open circuit line voltage throughout.

When on-hook transmission is needed, the TP3250 is placed in the active mode between ring bursts, restoring normal transmit and receive gains for transmission. Figure 8 shows the waveforms for on-chip ring feed when on-hook transmission is implemented.

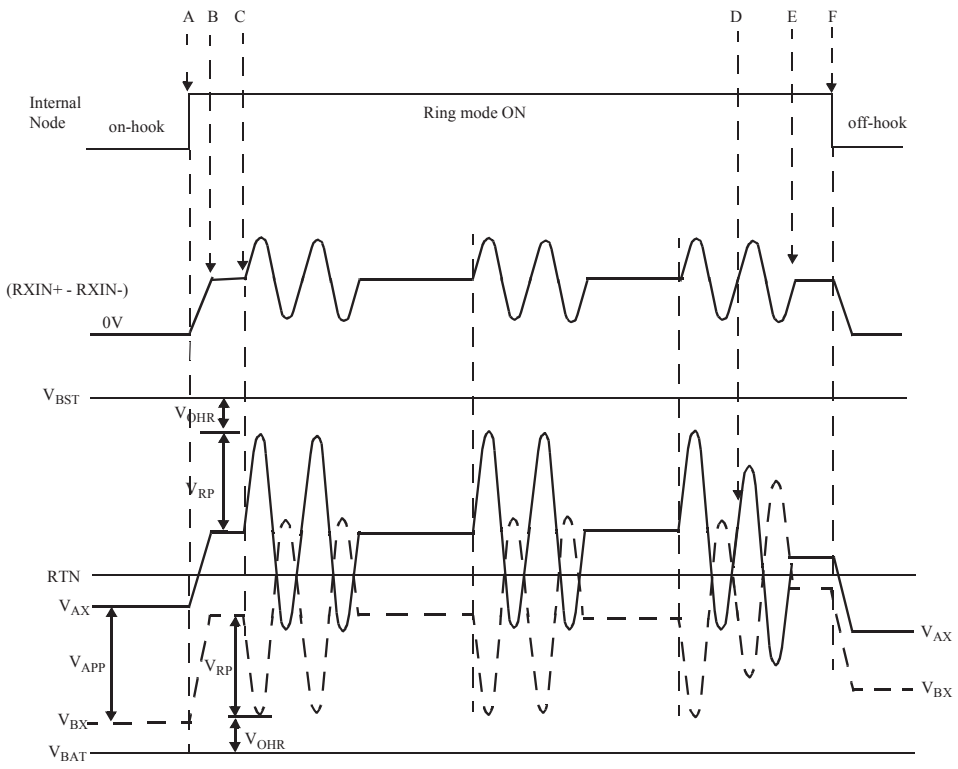
External Ring Feed

When a positive high voltage is not available for VBST, or an unbalanced ringing voltage is required, an external ring relay may be used for off-chip ring feed. When the Ring mode is enabled, the ring relay driver $\overline{\text{RRLY}}$ is turned on when RSYNC goes high, ensuring that the relay contacts close at approximately zero ac ringing voltage. The subscriber loop is connected to an external ringing source through a pair of ring feed resistors and the line driver outputs AX and BX are isolated from the line by the ring relay.

The $\overline{\text{RRLY}}$ relay driver is internally voltage limited at +15V for protection against the inductive kick-back voltage of the relay coil. The external ring relay may be powered from either +5V or +12V, with relay current returned to RGND.

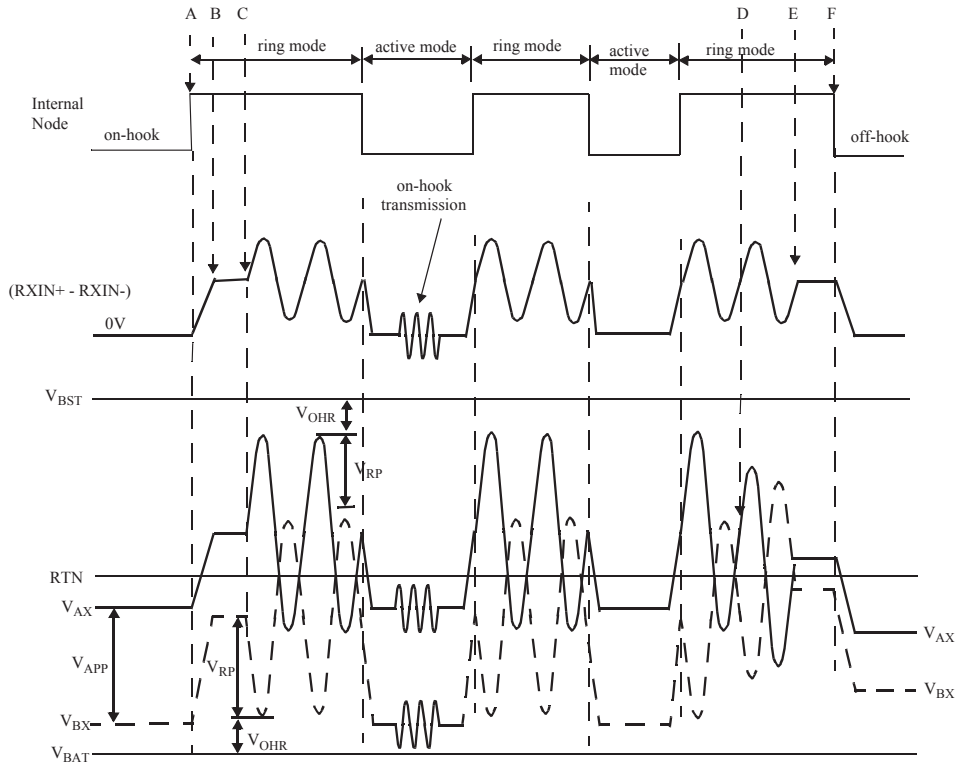
Battery Boost State

The battery boost mode is used to extend the loop range of the feed characteristics. The slic is placed in Battery Boost Mode by programming the BST bit in the LFR2 register. A positive high voltage supply,



A: Enable On-chip ringing
B: Apply dc offset to RXIN+- to set up open circuit voltage at AX-BX
C: Apply ac ringing voltage at RXIN+- at zero crossing
D: Subscriber goes off-hook
E: Ring trip detected by COMBO IV, terminate ac ringing signal at zero crossing
F: Ring mode disabled, removed dc offset at RXIN+-, SLIC programmed to Active mode

Figure 7. On-chip ring feed without on-hook transmission between ring bursts



A: Enable On-chip ringing
B: Apply dc offset to RXIN+- to set up open circuit voltage at AX-BX
C: Apply ac ringing voltage at RXIN+- at zero crossing
D: Subscriber goes off-hook
E: Ring trip detected by COMBO IV (within 3 cycles), terminate ac ringing signal at zero crossing
F: Ring mode disabled, removed dc offset at RXIN+-, SLIC programmed to Active mode

Figure 8. On-chip ring feed with on-hook transmission between ring bursts

VBST, is needed for on-chip ring feed as well as battery boost. When battery boost is enabled, the line drivers are powered from VBST and VBAT (or VBATR on short loops). Figure 9 shows a typical family of feed characteristics in battery boost. The

TP3250 is designed to deliver more than 18 mA into a 4KΩ loop with VBST of +32V and VBAT of -56V.

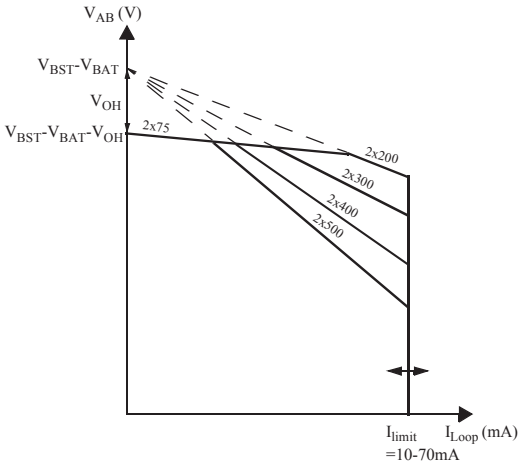


Figure 9: Line Feed Characteristics in Battery Boost

Test States

Through the use of the TST0-TST2 (in the Test Mode Register) it is possible to select one of five test mode, which pass test access signals via the VTX± outputs for measurement by the TP3090 COMBO IV. After the COMBO IV digitizes the measurements, the line card or system controller calculates the appropriate parameters. The five test modes, TM0 - TM4, which are described in Table 4, are operational in the Active, Ground Start and Ring modes.

Mode	Test Access Signal
TM0	AC transmit voltage, normal operation
TM1	DC loop current, VTX=50V/I
TM2	Line voltage, VTX=VAB/40
TM3	DC longitudinal current, VTX=50V/I
TM4	Battery voltage, VTX=VBAT/40

Table 1: TP3250 Test Access Modes

The device also includes the driver for an external test relay, managed directly by a dedicated bit in the Test Mode Register (TRLY).

Transmission and Signaling

2-Wire Impedance

The TP3250, in combination with the TP3090 COMBO IV can synthesize all world-wide 2-wire impedances. The 2-wire impedance is synthesized by the COMBO IV's programmable Z-filter. More detailed information on impedance synthesis may be found in the TP3090 COMBO IV data sheet.

Transmit Gain

The transmit gain from the subscriber loop to the differential transmit outputs (VTXO+ and VTXO-) is -10 dB. VTXO+ and VTXO- are dc coupled to the analog inputs VXI+ and VXI- of the COMBO IV. The line circuit transmit, Li, level is programmable via the COMBO IV transmit filter (GX).

Receive Gain

When used with the TP3090 COMBO IV, RXIN+ and RXIN- are connected to the analog outputs VRO+ and VRO- of the COMBO IV. The receive gain of the TP3250 is set by two external networks Z_R connected between the combo output and the RXIN pins. The SLIC acts as a current amplifier, with a nominal gain of 500, and the Z_R impedance transforms the voltage output from the combo into the current input into the slic. So in case the Z feedback through the combo synthesises a two wire impedance of Zo, the total receive gain G_{RX} is given by the following formula

$$G_{RX} = \frac{Zo}{Zo + ZL} \cdot \frac{ZL}{ZR} \cdot GM \cdot GR$$

Where ZL is the loop impedance, GM is the current gain of the SLIC.

The line circuit receive level, Lo, is software programmable via the COMBO IV's receive filter, GR.

Hybrid Balance

The programmable HB-filter in the TP3090 COMBO IV is used to replicate the echo signal and provide hybrid balance cancellation when the subscriber line is terminated by a hybrid balance reference impedance. The HB-filter is designed to meet hybrid balance requirements for all world-wide hybrid balance reference networks.

Quiet Battery Reversal

Battery polarity is determined by the logic state of the POL bit (in the Mode Register). When POL is a logic low, the SLIC is in forward battery, with AX more positive than BX. When POL is a logic high, the battery is reversed, with AX more negative than BX. During the polarity transition, the levels of AX and BX are slowly reversed. The transition time, controlled by the external capacitor C_{DC}, is on the order of 17-100 ms depending on the programmed feed characteristics. This polarity transition produces negligible noise. The POL bit can be used in both Active Mode and Ground Start Mode; it has no effect in Scan Mode (only Normal battery).

Metering

The line drivers of the TP3250 are designed to deliver metering pulses of up to 5Vrms at 12KHz or 16KHz into a 200Ω termination. The headroom of the line drivers is programmed by the VOH0 and VOH1 bits of the LFR 1 which are set according to the desired metering pulse amplitude.

The TP3090 COMBO IV is optimized for metering pulse insertion in conjunction with the TP3250. COMBO IV has an on-chip metering signal generator. The metering pulses are superimposed with in-band signals on the analog outputs, VRO+ and VRO-, of the COMBO IV and passed to the receive inputs, RXIN+ and RXIN-, of the TP3250. The pulse shaping, transmit filtering and level control are performed by the COMBO IV. More detailed information may be found in the TP3090 COMBO IV data sheet.

Supervision

The TP3250 supports loop start, ring trip, ground start and ground fault supervision. All supervision thresholds are programmed by THR0 and THR1 in the LFR 2. If Vbat is not present, all supervision outputs are inhibited.

Loop Start

In the Active mode, the loop supervision, illustrated in Figure 10, works in forward or reverse battery. The voltage at CDC, which is proportional to the line current, is compared with the selected loop detection thresholds to determine the hook-switch status. The external capacitor C_{DC}, connected from CDC to VM, provides loop detection filtering. The RC time constant formed by C_{DC} and an internal resistor, R_{DC}, is dynamically adjusted during dial pulsing to reduce dial pulse distortion. Hook-switch status is reported in the Status Register. A logic high indicates on-hook and a logic low indicates off-hook.

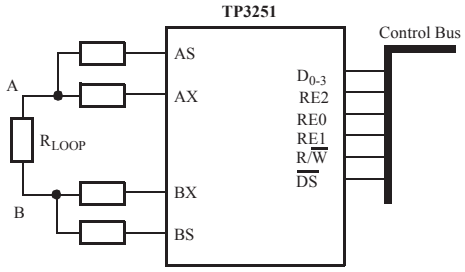


Figure 10. Loop start signalling

In the Scan mode, which only operates in forward battery, the threshold is not programmable. Off-hook is reported in the Status Register when the loop current is between 7.5mA to 10mA.

Ring Trip

During on-chip ring feed, the line sense inputs, AS and BS, provide the necessary information for ring trip detection. The output of the line sense amplifier is subtracted from the desired open circuit ring voltage, filtered by $R_{DC}C_{DC}$ and compared with the ring-trip threshold by the hook-switch comparator. The output of the comparator is reported in the Status Register and is passed to the COMBO IV. A digital filter in the COMBO IV is used to detect ring-trip. When the dc loop current exceeds the selected ring-trip threshold, ring-trip is detected. The COMBO IV automatically terminates ringing at the next zero crossing of the ringing voltage and reports the ring-trip status to the line card controller. After ring-trip, the TP3250 SLIC must be programmed to the active mode by the system.

When off-chip ringing is used, an external resistive bridge is connected to the ring sense inputs, RS+ and RS-, to monitor the loop current through ring feed resistors. The output of the ring sense circuit is filtered by C_{DC} and subsequently processed exactly in the same way as for on-chip ringing. As soon as the COMBO IV detects ring trip, a command is sent from COMBO IV to the TP3250 to exit from the Ring mode. The TP3250 turns off $\overline{RRLY}$ at the next positive transition of RSYNC.

Ground Start

In the Ground Start mode, Figure 11, AX is in a high impedance state. The supervision circuit compares the current flowing from the B-lead to RTN against the selected ground start thresholds. Ground start status is reported in the Status Register. A logic low indicates detection of valid ground start signalling. The ground start signalling also works in reverse battery, in which case BX is in a high impedance state.

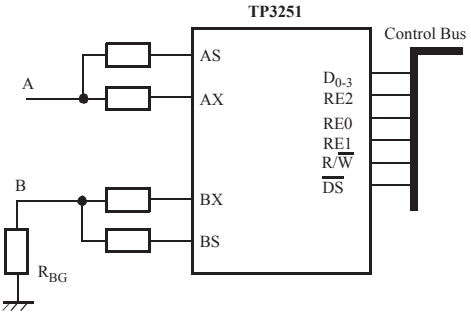


Figure 11. Ground start signalling

Ground Fault

A ground fault detector is used to monitor the longitudinal current flowing into the A and B leads, Figure 12. The output of the longitudinal control circuit is filtered by an external capacitor, C_{GF} from CGF pin to AGND , and compared with the selected ground fault thresholds. The ground fault status is reported as a dedicated bit in the Status Register. A logic low indicates detection of a ground fault. Ground fault supervision is operational in the Active, in either forward or reverse battery.

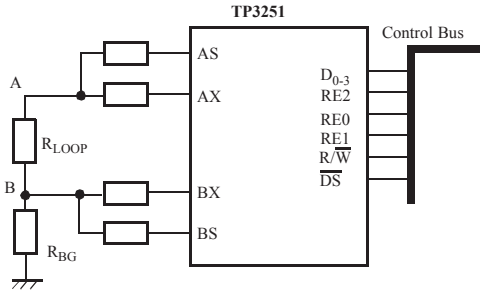


Figure 12. Ground fault detection

Power Management

The TP3250 is equipped with a battery switching mechanism which provides for very flexible power management. In all, three options are provided and in all cases, the power management is transparent to subscriber terminal equipment. Typical power dissipation curves are shown for each of these power management options in Figure 13.

On long loops, the line drivers are powered from VBAT and RTN. On short loops, a soft switching mechanism is used to gradually switch the negative supply rail of the line drivers from VBAT to VBATR. VBATR is a reduced battery supply voltage, typically

1/2 to 2/3 of VBAT, used for reducing both the system power and the internal power dissipation of the SLIC.

If a reduced battery supply is not available, an external power resistor may be connected from VBATR pin to VBAT, thereby reducing the device's effective operating voltage drop and its power dissipation. As the line voltage increases, or the subscriber goes on-hook, the line drivers return to the normal working condition, with the negative supply powered from VBAT.

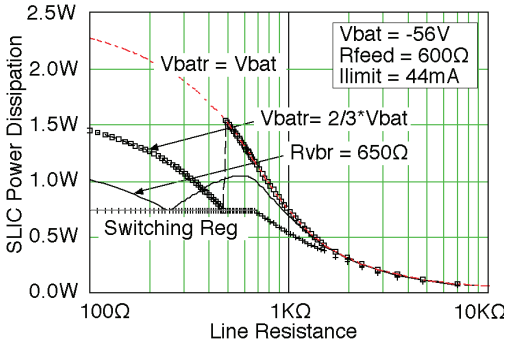


Figure 13: Dissipation versus Loop Resistance

A third power management mechanism supported by the TP3250 is the use of external per-line switching regulators. The VLREF output provides the desired output reference voltage to the regulator which in turn drives VBATR. This method provides the lowest overall power dissipation.

Longitudinal Balance

The longitudinal voltage on the subscriber line is sensed by AS and BS on the loop side of the protection network, and fed back through the longitudinal control circuit to the line drivers. The A-lead and the B-lead of the line circuit exhibits a longitudinal impedance of nominal 75Ω to RTN. These impedances are extremely well matched and are not dependent on the matching of the external protection resistors, allowing PTR's to be used as the current limiting protection elements. The line drivers are designed to handle 30mArms of longitudinal current in each of the A and B-leads in Active, Ground Start, or Ring modes.

Programming Information

The slic contains the following 4bits registers

- Mode Register, MD
- Current Limit Register, CLR
- Loop Feed Register 1, LFR1
- Loop Feed Register 2, LFR2
- Test Mode Register, TMR
- Loop Status Register, LSR

MODE REGISTER. MD.

RE2	RE1	RE0	D3	D2	D1	D0
0	0	1	POL	M2	M1	M0

where

M2	M1	M0	Operating modes
0	0	0	***Active***
0	0	1	Ring
0	***1***	***0***	Power Denial
0	1	1	Scan
1	0	0	Ground start
1	0	1	
1	1	0	
1	1	1	

CURRENT LIMIT REGISTER, CLR

RE2	RE1	RE0	D3	D2	D1	D0
1	0	1	I3	I2	I1	I0

where

I3	I2	I1	I0	Current limit
0	0	0	0	10mA
0	0	0	1	14mA
0	0	1	0	18mA
0	0	1	1	20mA
0	1	0	0	22mA
0	1	0	1	24mA
0	***1***	***1***	***0***	***26mA***
0	1	1	1	28mA
1	0	0	0	30mA
1	0	0	1	35mA
1	0	1	0	40mA
1	0	1	1	45mA
1	1	0	0	50mA
1	1	0	1	55mA
1	1	1	0	60mA
1	1	1	1	70mA

LOOP FEED REGISTER 1, LFR1

RE2	RE1	RE0	D3	D2	D1	D0
0	1	0	THR1	THR0	VOH1	VOH0

where

VOH1	VOH0	Metering Pulse Amplitude
0	***0***	***No Metering***
0	1	Up to 2.5Vrms
1	0	2.5 to 5.0Vrms
1	1	Reserved

THR1	THR0	Loop Start	Ground Start	Ground Fault	Ring Detection
0	0	5mA	10mA	5mA	5mA
0	1	7.5mA	15mA	7.5mA	7.5mA
1	***0***	***9.5mA***	***19mA***	***9.5mA***	***9.5mA***
1	1	12mA	24mA	12mA	12mA

LOOP FEED REGISTER 2, LFR2

RE2	RE1	RE0	D3	D2	D1	D0
0	1	1	BST	RINGSEL	RF1	RF0

where

BST	Battery Boost Enable.
0	***Normal Battery***
1	Boost Battery

RINGSEL	Ring Mode Selection.
0	***on-chip ring***
1	off-chip ring

RF1	RF0	Feed Resistance
0	***0***	***2x200 Ohm***
0	1	2x300 Ohm
1	0	2x400 Ohm
1	1	2x500 Ohm

TEST MODE REGISTER, TMR

RE2	RE1	RE0	D3	D2	D1	D0
1	0	0	TRLY	TST2	TST1	TST0

where

TRLY	Test relay enable.
0	***Test Relay not activated***
1	Test Relay activated

TST2	TST1	TST0	Test modes
0	***0***	***0***	***TM0: Normal operation***
0	0	1	TM1: V_{CDC} to VTXO±
0	1	0	TM2: Line voltage to VTXO±
0	1	1	TM3: V_{CGF} to VTXO±
1	0	0	TM4: V_{BAT} to VTXO±
1	0	1	TM5: not used
1	1	0	TM6: not used
1	1	1	TM7: not used

LOOP STATUS REGISTER, LSR

RE2	RE1	RE0	D3	D2	D1	D0
0	0	0	X	TS	GF	OH

where

OH	Hook-switch status indicator. In the Scan mode or Active mode, OH reports the loop start hook switch status. In the ground start signalling mode, OH reports the ground start signalling status. In the ring mode, OH provides loop current information for ring-trip detection.
0	OFF HOOK
1	ON HOOK

GF	Ground fault detect indicator.
0	valid ground fault
1	no ground falut

TS	Thermal Shutdown indicator.
0	Thermal shutdown ON
1	No thermal Shutdown

Absolute Maximum Ratings

V_{CC} to AGND	-0.5V to 7V
V_{BAT} or V_{BATR} to RTN	0.5V to -90V
V_{BATR} to V_{BAT}	-0.5V to +90V
V_{BST} to RTN	-0.5V to +90V
V_{BST} to V_{BAT}	142V
RTN to AGND	±25V
Voltage at any digital input	AGND -0.5V to V_{CC} +0.5V
AX, BX to RTN	
Continuous	+1V to -70V
10mS, 0.1Hz	+5V to -70V
Current into AS, BS	±0.5mA
Current into RS+ or RS-	±10mA
$\overline{RRLY}$ or $\overline{TRLY}$ to RTN	15V
Current through relay driver	60mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10Sec)	300°C
Maximum junction temperature	150°C
Maximum power dissipation	TBD

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC}=+5.0V±5%, V_{BAT}=-40V to -59V, V_{BST} = 0V, T_A=-40°C to +85°C by correlation with 100% electrical testing at T_A=25°C. All other limits are assured by testing at V_{CC}=5.0V, V_{BAT}=-56V, T_A=25°C.

Symbol	Parameter	Conditions	min	Typ	Max	Units
Supply currents						
I_{BAT}	V_{BAT} Current	Power denial mode, R_L=100Ω				mA
		Scan mode, I_{LOOP}=0mA		0.1	1	mA
		Active mode, I_{LOOP}=20mA		21.1	23	mA
I_{CC}	V_{CC} Current	Power denial mode, R_L=100Ω				mA
		Scan mode, I_{LOOP}=0mA		**4**	**TBD**	mA
		Active mode, I_{LOOP}=20mA		7	TBD	mA
Digital Interface ($\overline{DS}$, RE0, RE1, RE2, D_{0-3})						
V_{IL}	Input low level	All digital inputs			0.7	V
V_{IH}	Input high level	All digital inputs	2			V
I_{IL}	Input low current	GND<V_{IN}<V_{IL}, all digital inputs	-100			µA
I_{IH}	Input high current	V_{IH}<V_{IN}<V_{CC}, all digital inputs	-100		100	µA
V_{OL}	Output low level	D_{0-3}, IL=3.2 mA			0.4	V
V_{OH}	Output high level	D_{0-3}, IL=-0.1mA	2.4			V
I_{OZ}	Output current in high impedance state	D_{0-3}	-100		100	µA

Symbol	Parameter	Conditions	min	Typ	Max	Units
Battery Feed						
I_{LOOP1}	Loop current in Active mode	V_{BAT}=-56V, R_L=1900Ω, ILIMIT =26mA, R_{FEED}=2x200Ω Forward or reverse battery		19		mA
I_{LOOP2}	Loop current in Scan mode	V_{BAT}=-56V, R_L=1900Ω		10		mA
I_{LOOP3}	Loop current in Battery Boost mode	V_{BAT}=-56V, V_{BST}=+40V, R_L=4KΩ, R_{FEED}=2x200Ω Forward or reverse battery		19		mA
I_{LOOP4}	Loop current in Power Denial mode	V_{BAT}=-56V, R_L=200Ω			1	mA
I_{LOOP5}	Loop current in Ground Start mode	V_{BAT}=-56V, R_L=200Ω Forward or reverse battery			**TBD**	mA
I_{LIMA}	Current limit accuracy	V_{BAT}=-56V, R_L=200Ω Forward or Reverse battery	5		-5	%
V_{AB1}	Open circuit voltage	V_{BAT}=-56V No metering 2.2Vrms metering 5.0Vrms metering		 **44** **38** **30**	 TBD TBD TBD	 V V V
V_{AB2}	Open circuit voltage, Scan mode	V_{BAT}=-56V		50		V
V_{AB3}	Open circuit voltage, Battery Boost mode	V_{BAT}=-56V, V_{BST}=+40V, No metering 2.2Vrms metering 5.0Vrms metering		 **82** **76** **68**		 V V V
T_{SD}	Thermal shutdown temperature			160		°C
Supervision						
ITHLP	Loop threshold accuracy	Applicable to Loop Start, Ground Start or Ring Trip. Forward or reverse battery.	**-20**		**20**	%
DPD	Dial pulse distortion	R_L = 200 to 1900Ω, I_{LIMIT} = 20 to 70mA			4	ms
ITHGF	Ground fault threshold accuracy		-20		20	%

Symbol	Parameter	Conditions	min	Typ	Max	Units
On-chip Ring Feed						
VDCR	Open circuit line voltage in ring mode	VBAT=-56V, VBST=+80V VRX = 0.65Vdc, ZR=88.7KΩ || (220pF + 22.1KΩ)	TBD	24	TBD	Vdc
VACR	Balanced AC ringing voltage between AX and BX	VBAT=-56V, VBST=+80V VRX =1.9Vrms + 0.65Vdc, ZR=88.7KΩ || (220pF + 22.1KΩ), F=20Hz	TBD	68	TBD	Vrms
I_{LIMR}	Current limit	V_{BAT}=-56V, R_L=200Ω V_{RX} = ±1.0V_{dc}, Z_R=88.7KΩ || (220pF + 22.1KΩ)		70		mA
Ring-bridge detector inputs (RS+, RS-)						
V_{OS}	Offset voltage at RS+, RS-	V_{RS+} - V_{RS-}. I_{RS+}=I_{RS-} = 10µA.	-10		10	mV
Relay Drivers						
V_{ON}	Driver on voltage	Idriver=50mA sink		1	2	V
I_{LEAK}	Off state leakage current			0.5	100	µA
V_{CLAMP}	Driver clamp voltage	I = 1mA	14	15		V
Longitudinal Balance and current capability						
LBAL	Longitudinal to metallic balance	F=62Hz F=300Hz to 3.4KHz R_L=600Ω	58 52			dB dB
LSG	Longitudinal signal generation, 4-wire to 2-wire	F=300Hz to 800Hz	42			dB
ILONG1	Longitudinal current capability, on hook	I_L = 0mA Active mode Scan mode	30	7		mArms mArms
ILONG0	Longitudinal current capability, off hook	R_L = 1900Ω Active mode Scan mode	30	7		mArms mArms

Analog ports

Symbol	Parameter	Conditions	min	Typ	Max	Units
Z_{TXO}	Output impedance at VTXO+ or VTXO-			3		Ω
V_{CMTX}	Common-mode voltage at VTXO+ or VTXO-		2.1	2.25	2.4	V
V_{OSTX}	Offset voltage at V_{TXO+} - V_{TXO-}		**-30**		**30**	mV
R_{LTX}	Load resistance from VTXO+ or VTXO- to AGND		10			KΩ
Z_{RXIN}	Input impedance at RXIN+ or RXIN-	F=300Hz to 3.4KHz Z_R = 88.7KΩ || (220pF + 22.1KΩ)		10		Ω
V_{OSRX}	Offset voltage at RXIN+ or RXIN-		-10		10	mV

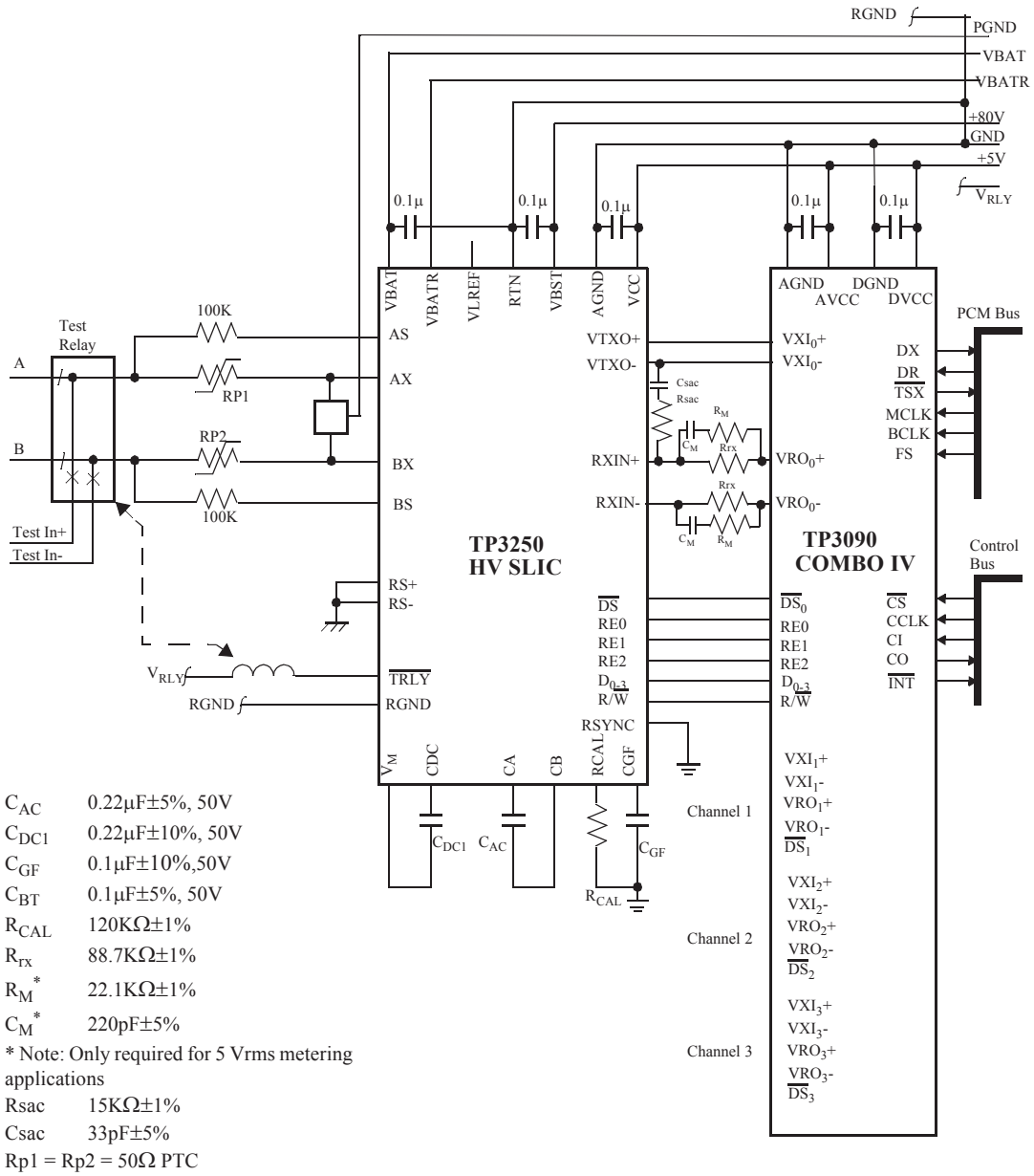
V_{OVL}	Overload voltage	Z2w=600Ω, THD=1% 4-wire port: VTXO±, RXIN± 2-wire port: 0Vrms metering 2.2Vrms metering 5.0Vrms metering		 3.375 TBD TBD TBD		 Vpk Vpk Vpk Vpk
Transmission - 2wire return loss (Z2w=600Ω)						
RTL	2-wire return loss See Note 1	F= 300Hz to 500Hz 500Hz to 2.5KHz 2.5KHz to 3.4KHz	26 26 20			dB dB dB
Gain accuracy						
G_{XA}	Insertion loss, transmit	V_{AB}=-10dBm, F=1KHz, T_A=25°C Measured from VAB to differential voltage VTXO+/VTXO-	9.85	10.0	10.15	dB
G_{RA}	Gain, receive	V_{RX}=-10dBm, F=1KHz, T_A=25°C Measured from differential voltage between RXIN+ and RXIN- to V_{AB}, Z_R=88.7KΩ || (220pF + 22.1KΩ), R_L = 600Ω	10.85	10.7	10.55	dB
GM	Current Gain, from RXIN+/- to Line	DC signal		500		A / A
G_{EA}	Insertion loss, echo	V_{RX}=-10dBm, F=1KHz, T_A=25°C Measured from RXIN± to VTXO±, R_L = 600Ω	-0.4	-0.7	-1.0	dB
Attenuation distortion						
G_{RX}	Attenuation distortion, transmit	F=300Hz to 3.4KHz, relative to 1KHz	-0.1		0.1	dB
G_{RR}	Attenuation distortion, receive	F=300Hz to 3.4KHz, relative to 1KHz	-0.1		0.1	dB
G_{RE}	Attenuation distortion, echo	F=300Hz to 3.4KHz, relative to 1KHz	-0.1		0.1	dB
Gain tracking						
G_{XL}	Gain tracking, transmit	+3dBm to -55dBm, relative to 0dBm	-0.1		0.1	dB
G_{RL}	Gain tracking, receive	+3dBm to -55dBm, relative to 0dBm	-0.1		0.1	dB
G_{EL}	Gain tracking, echo	+3dBm to -55dBm, relative to 0dBm	-0.1		0.1	dB

Note 1: Return Loss is calculated based on the presence of TP3090

Symbol	Parameter	Conditions	min	Typ	Max	Units
Group delay						
D_{XA}	Group delay, transmit	F=1KHz		TBD		µS
D_{RA}	Group delay, receive	F=1KHz		TBD		µS
D_{EA}	Group delay for echo signal path	F=1KHz		TBD		µS
Total harmonic distortion						
THD_X	Total harmonic distortion, transmit	F=300Hz to 3.4KHz, V_{AB}=-10dBm, no metering V_{AB}=-10dBm, with 2.2Vrms metering			-50 -35	dB dB
THD_R	Total harmonic distortion, receive	F=300Hz to 3.4KHz, V_{RX}=-10dBm, no metering V_{RX}=-10dBm, with 2.2Vrms metering			-50 -35	dB dB
Idle channel noise						
N_X	Idle channel noise, transmit	Zl = 900Ω C-message weighted Psophometric weighted		8 -83	12 -79	dBrnC dBmp
N_R	Idle channel noise, receive	Zl = 900Ω C-message weighted Psophometric weighted		8 -83	12 -79	dBrnC dBmp
Power supply rejection (Vripple=50mVrms)						
PSR_{VBAT}	V_{BAT} supply rejection Va - Vb	1KHz 50Hz to 3.4KHz 3.4KHz to 50KHz	30	 45 40		dB dB dB
PSR_{VCC}	V_{CC} supply rejection Va - Vb	1KHz 50Hz to 3.4KHz 3.4KHz to 50KHz	30	 45 35		dB dB dB

Symbol	Parameter	Conditions	min	Typ	Max	Units
Digital Timing, Parallel Control Interface (See Figures 3, 4)						
t_{DSW}	DS minimum width		600			ns
t_{DSR}	DS rise time				20	ns
t_{DSF}	DS fall time				20	ns
Read/Write, Write/Read modes (see Figure 3)						
t_{SRWDS}	Set-up time from RW to $\overline{DS}$		20			ns
t_{SREDS}	Setup time from REi to $\overline{DS}$		20			ns
t_{SDODS}	Setup time from Di to $\overline{DS}$		20			ns
t_{HREDS}	Hold time from REi to $\overline{DS}$		100			ns
t_{HDODS}	Hold time from Di to $\overline{DS}$		10			ns
t_{DDSDO}	Delay time from $\overline{DS}$ LOW to Di valid		100			ns
t_{DDSDOZ}	Delay time from $\overline{DS}$ HIGH to Di High Imp.				100	ns
t_{DWR}	Delay time from RW LOW, REi valid to DO valid (Write Access)		100			ns
t_{DRD}	Delay time from RW HIGH, REi valid to DO valid (READ)				100	ns

Application Information



C_{AC}	0.22µF±5%, 50V
C_{DC1}	0.22µF±10%, 50V
C_{GF}	0.1µF±10%,50V
C_{BT}	0.1µF±5%, 50V
R_{CAL}	120KΩ±1%
R_{rx}	88.7KΩ±1%
R_M*	22.1KΩ±1%
C_M*	220pF±5%

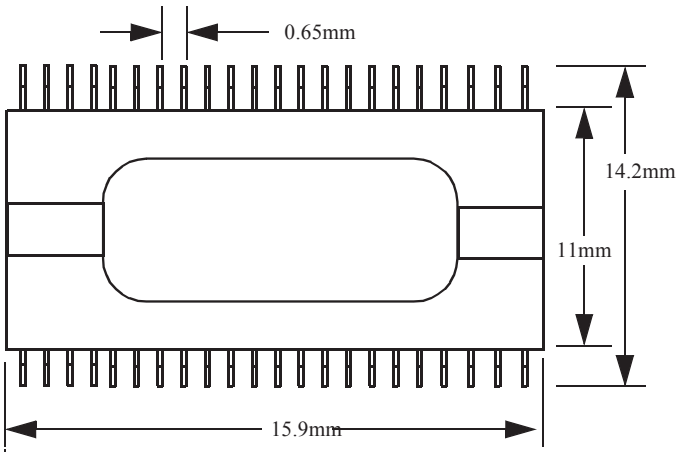
* Note: Only required for 5 Vrms metering applications

Rsac	15KΩ±1%
Csac	33pF±5%

Rp1 = Rp2 = 50Ω PTC

Figure 14. A programmable line circuit implemented with the TP3250 and the TP3090 COMBO IV

Package Dimension



44 Pin PSOP3

NS Package Number (MWC 44A)

Next Generation Subscriber Line Interface Solutions.

Duncan J. Bremner
Application Manager, Telecom Products
National Semiconductor, Larkfield Industrial Estate
GREENOCK, PA16 0EQ, Scotland,
United Kingdom

Abstract

Subscriber Line Interface Circuits (SLICs) implemented using silicon technology are now in their fourth generation providing many sophisticated features via software control. This enables the user to address both domestic and export markets with the same hardware components and manage all the custom interface configuration issues via firmware down loaded on initial commissioning of a new switch. This paper gives a brief overview of the development of solid state SLIC devices, and highlights the feature set available in the latest line circuit devices. There are also practical details on how to design cost effective line circuits that conform to the demands of the modern telecommunications environment.

Introduction

This paper examines the development of the subscriber line interface circuit (SLIC) from the original transformer based solutions through the previous generations of silicon solutions to the latest devices offering on-chip ring generation, testing, self-diagnostics and fully re-configurable via software and firmware to meet any international specification. This allows the same hardware components to address several export markets offering equipment manufacturers the advantages of economies of scale, and improved inventory control. The final section of the paper goes on to examine the practical implications of using the latest generation of SLIC solutions and offers advice on the pitfalls and problems which may be encountered during the design phase of line cards.

Background

When the telephone was first introduced as a means of long distance communication, the entire system was based around electro-mechanical exchange systems. These systems were based on analog transmission, and within a given Central Office, there was no ability to amplify the signals or to allow more than one signal to occupy a circuit simultaneously. This led to the development of extremely large Central Offices within cities, and the control of the network and the losses induced in the switch increased to the point of significantly degrading the transmission quality. Furthermore, the electro-mechanical mechanism's reliability began to significantly impact the performance of the switch. Additionally, the volume of traffic was increasing exponentially, placed great demands on the limited analog trunk connections between switching centres.

In the 1970s, the development of the Time Division Multiplexing (TDM) along with Pulse Code modulation (PCM) standards gave rise to the development of the digital switch which made use of the new integrated circuit technologies which allowed digital, lossless switching throughout an office. This also permitted digital transmission between offices using the TDM technology that effectively increased the available trunk connections to cope with the increase demand in traffic. However, although the switching and the transmission within the Central Office converted to digital technology, the external plant remained analog. This meant that the interface within the office had to maintain the same transmission and signalling standards as the older analog equipment, and also provide the customers equipment similar power feeding via the loop. Consequently, the line interface circuits used in the early digital switches were based using transformers an example of which is shown in figure 1.

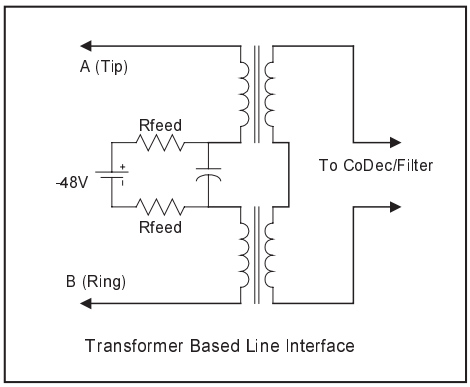


Figure 1

The main specifications for SLICs are encompassed in the so called BORSCHT functions and are detailed in Table 1 along with some typical performance criteria. These parameters remained fixed irrespective of the advances in technology, and indeed gave rise to several complex problems in implementing the line interface function into silicon. For this reason, the transformer remained as the standard line interface circuit for many years although several methods were attempted to improve the performance of this simple interface. These included magnetic compensation of the DC

current, using AC coupled transformers, or advanced magnetic materials, but eventually the excessive weight, board space, and limited feature set demanded that a more modern solution.

Abreviation	Function	Typical Specification
B	Battery Feed	Min 20mA loop current from –48V battery for Rloop = 2000 ohms
O	Over Voltage	Must withstand lightning & Power Cross per CCITT K.20
R	Ringing	Balanced or Unbalanced ringing of 16 – 66 Hz superimposed onto –48 battery
S	Signalling	Minimum must signal On/off-hook, Dialling, Ring trip functions
C	Coding/Decoding	Must Implement CoDec / Filter functions for voice transmission
H	Hybrid Balance	Cancels the Rx signal in Tx direction to avoid far end echo
T	Test	Provide capability for Test in (SLIC) and Test Out (Line), normally via relays to dedicated test equipment

Table 1

Electronic SLICs

When improved high voltage bipolar processes became available, several manufacturers developed line interface circuits that would replace the traditional transformer. Due to the technical demands being made on these devices, especially dealing with the over voltage protection issues, the development of these interfaces followed two distinct approaches.

On one hand, there were several manufacturers that implemented the DC Feeding, Signalling, Ringing (via Relay), and Test (via relay) functions on a single, high voltage device, but avoided dealing with the tricky issue of over voltage in the application. In addition, there were several parameters, such as longitudinal balance in which the transformer solutions performed very well, but due to compromises in the architecture proved difficult to implement in the silicon solutions. Some of these transmission parameters were affected by the external components employed thus making it difficult to meet full specification over time in the real field application. Power dissipation was also a problem and some device employed a switching regulator to reduce the heating effect of the line current while feeding short loop lengths with high constant currents. Although initially this looked attractive due to the improved efficiencies of the power consumption, the additional switching noise generated on the subscriber loop proved very difficult to eliminate without the use of expensive filter components.

On the other hand, other manufacturers adopted the use of thick film hybrid technology to improve the over voltage performance and integrated both the Line interface function and the CoDec / Filter function into one component. This had the advantage of reducing the external components to a minimum, and by ensuring that the transmission parameters were independent of the external components, provided the customer with a guaranteed path to compliant line circuits.

However, in both these cases, the key requirements of Test and Ringing were performed using external relays which although suitable for the existing large central office switches was unsuitable for the smaller rural switches or Digital Loop Concentrators (DLC). These may only have less than 250 lines and require built-in ring generation and test facilities.

Next Generation SLICs

The new generation of global line circuits, so called because of their international feature sets, utilise the latest developments in process technology and offer a feature set which is ideal to meet all the requirements for modern subscriber line access. These devices are equipped with on-chip ringing, line diagnostic test, advanced power saving, full surface mount packaging, and simple application circuits. The most common configuration of these new interfaces consists of a high voltage front end, plus a highly integrated Digital Signal Processor (DSP) shared over 4 or more channels. An example of this is shown in figure 2. In addition, these devices have been designed to be much more rugged in the application allowing more cost effective power supplies and protection components to be used.

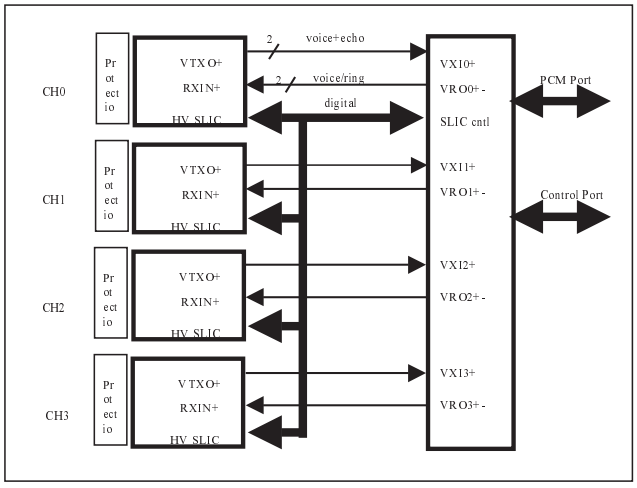


Figure 2

In order to understand the benefits of these features, it is worthwhile examining some of these features in greater detail, in particular, Ringing, testing, programming and power switching.

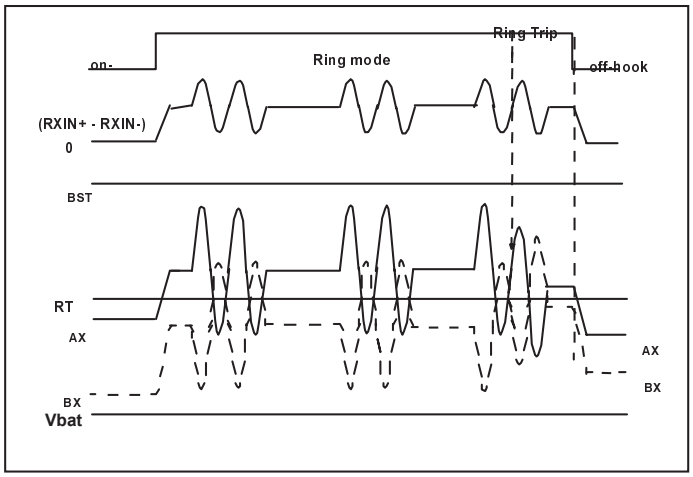


Figure 3

Ringing.

Modern SLIC solutions are capable of generating both the AC ring signal and the DC bias signal used to detect ring trip. This is achieved by using an additional positive supply voltage that is approximately equal to the battery voltage. The SLIC can generate up to 70Vrms ring plus 20VDC at all standard ring frequencies from 16.67Hz up to 66Hz (the most common being 20 or 25Hz). These signals are generated digitally in the DSP device and amplified by the HV interface device. This allow a high purity signal to be used for the ring signal which reduces cross-channel interference, and the system has a built-in zero crossing detector. It is also important that the device be capable of reproducing the ring signal without clipping as trapezoidal ringing can interfere with adjacent lines. This is very important for lines running adjacent to data lines as the EMI generated can generate errors in the data transmission. Figure 3 shows the balanced ring signals generated by a modern global line card solution.

Testing

Line test, both inward and outward is an important tool for network diagnosis. In the traditional large central office, this function was carried out at regular intervals by a dedicated line test function, but as switch sizes decrease, the cost of this function increases. By including testing as part of the interface circuit, more through testing may be carried out than present since the testing function is available on a per line basis. This enables a line history to be developed and stored within the switch so any changes in line performance or unauthorised equipment can be detected immediately.

The testing function is capable of measuring the leakage resistance present on the subscriber loop both between the ‘a’ and ‘b’ legs, and from each leg to earth. This can be measured to an accuracy of typically 5% that is sufficient to provide functional testing. Also, by using the advanced features provided by the CoDec device, the internal signal generator and level meter can be used to carry out transmission tests on the line. The CoDec is also capable of producing DC test signals which, when used in conjunction with the test modes, allows measurement of line and bell capacitance in the range 5nF to 10uF. There is also the capability of measuring AC and DC longitudinal currents that may be induced into the subscriber loop, and when all these testing capabilities are configured together permits a comprehensive set of line diagnostics.

Parameter Programming

Previous generations of line interfaces have used hardware selection of external components connected around the device. This method was effective when adjustment was limited, but is not suitable to meet the demands of modern transmission requirements, especially data services. This also gave rise to many different line card configurations to meet the specific specifications of the different markets, but the inventory management and manufacturing planning was complex.

Parameter	Programming Range	Comments
DC Feeding		
Current Limit	10mA to 70mA	High resolution 20 – 30mA
DC Feed Resistance	2x200 to 2x500 ohms	4 options
Detector Threshold Currents	5mA to 12mA	4 options,
Transmission		
Transmit Gain	18dB range, 0.1dB steps	
Receive Gain	18dB range, 0.1dB steps	
2 wire Impedance	500 to 1000 ohms	Includes all complex networks
Hybrid Balance	500 to 1500 ohms	Includes all complex

Special Services

Metering Pulse frequency	12 or 16kHz	
Metering Amplitude	200mV to 5Vrms	Does not distort transmission
Metering shape control	Automatic envelope control	

Ringing

Level	25Vrms to 85Vrms(balanced)	
DC Ring Battery	14 to 25VDC	
Ring Frequency	16.667Hz to 66Hz	All ring frequencies covered
Off-chip ringing(unbalanced)	Any standard ring buss	All ring options covered

Table 2; Programming Variables

The next generation global line circuit solutions address this problem by allowing all parameters of the interface to be configured via the software based on coefficients held in the switch firmware. These parameters and the programming ranges are shown in Table 2.

Power Switching

The final important feature that this paper wants to highlight is the advanced power switching and management techniques employed by the next generation global line circuit solutions. The management of power on the line card has become much more significant in modern equipment. The reason for this is the market demand for smaller equipment footprint and the elimination of special air conditioning plant in small or remote central offices. In addition, the industry is now demanding that 32 subscribers are supplied from one card which gives additional problems with on-board heating.

The next generation solutions provide the ability to supply the interface with two separate supply batteries, the first a normal –56V supply, and a second, lower voltage supply around –30V. This allows the circuit to generate a normal on-hook voltage while the off hook subscriber is supplied from the reduced supply. This is highly efficient in power as many of subscriber lines are relative short, (<600 ohms) and can be supplied from the reduced battery, while the remaining long lines are powered from the high voltage battery. This selection is automatic.

Another important power saving method is the ability to operate in a very low power ‘scan’ mode during on-hook periods, however the interface must still be capable of signalling hook switch status and withstanding the effects of longitudinal currents without signalling false off-hook status. In the next generation global line card solutions, the best circuits offer a scan mode which consumes less than 30mW while being capable of rejecting longitudinal currents up to 7mA rms. Based on extensive studies carried out by Bell Core in the US, this level of longitudinal is the maximum observed during a study of many subscriber lines.

Practical Line Card Design

In the highly competitive equipment business, it is no longer acceptable to allow several revisions of development before a fully compliant solution is achieved and reduced time to market is an important competitive advantage. This final section of this paper attempts to highlight potential pitfalls in the design of line cards and illustrates the points using a reference design of a 16 channel, 2 layer board. The key problems normally encountered can be reduced to 5 main areas:

Power. The most common problems with power are the mixing of different supplies to the various components. For good board layout, each supply should be connected only to pins of a similar nature, i.e. digital supplies should only be connected to other digital supplies and never to analog supplies. If it is necessary to connect analog and digital supplies together to a common Gnd or Vcc point, this should be done adjacent to the back plane connector, not at the device.

Protection. The surge currents that appear on the protection components are considerable and must be treated carefully. Protection components should always be routed on separate protection ground lines away from the main components on the board. The current surges in the protection lines are capable of inducing currents into adjacent wiring so should be laid out carefully. Ideally, the protection ground connection should be taken to separate pins on the back plane connector to avoid damage to the supply pins.

Noise. This is most common cause of re-works on board layouts. In order to eliminate noise problems, close attention should be paid to the grounding arrangements between the CoDec and the SLIC device. If these components have differential analog connections, the problems are considerably reduced. The key is to ensure that the signal grounds are star connected on a per channel basis, and all channels are then taken to a reference star point. Care should be taken to avoid transient or switching currents from appearing on these star points, and connection to the common ground point should be adjacent to the back plane connector.

Crosstalk. The solution to crosstalk is similar to that for noise, the most common cause is the sharing of signal references between channels and correct star connections between channels will resolve.

Hot Insertion. This is possibly the most over-looked problem that occurs in line card design and gives rise to the most applications problems. The golden rule for hot insertion is to ensure that the ground connection ALWAYS makes first and breaks last during the insertion and removal of the card. This may be achieved using extended finger connections or special ground connections, and in conjunction with these, over-voltage diodes should be installed as further protection against voltage over stress during insertion.

If the above guidelines are followed, and reference is made to the conceptual layout in figure 4, then many of the standard errors can be avoided and successful board layouts can be achieved.

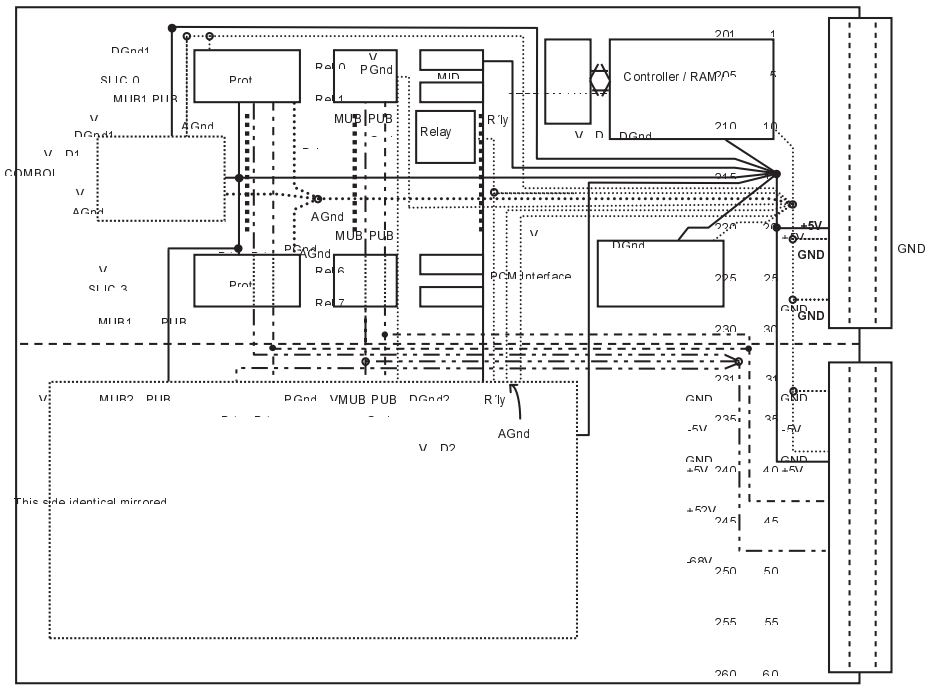


Figure 4

Conclusion

This paper has attempted to highlight the most recent developments in line interface components and the advantages these bring to designers and manufacturers of modern switch equipment. The new features offer hitherto unattainable performance levels and features, and while keeping the line costs constant, deliver additional features that are demanded by customers. The important features of ringing, programming, power switching and testing were examined, and a practical guide to board layout was offered. Components offering these specifications are available and details of products meeting these can be obtained from the author's company via the normal sales channels or the World Wide Web at http://www.national.com.

Submission IX

Type	Reference	Title
Book Extract	AN-639	'High Voltage Protection Application Note for protection of SLIC devices against power cross and lightning' National Semiconductor Telecommunications Databook, 1995
Citations	**3**	

High Voltage Protection Techniques with TP3210 Subscriber Line Interface Module

National Semiconductor
Application Note 639
Duncan Bremner
Telecom Products
January 1990

1.0 INTRODUCTION

The objective of this application note is to demonstrate a solution which removes some of the traditional accuracy constraints on the protection components without impacting performance. It then goes on to develop protection schemes which are completely resettable. The note begins with a brief discussion of the protection problems associated with subscriber line interface circuits, and outlines the basic requirements which these devices meet. This is followed by a discussion of the National Semiconductor **S**ubscriber **L**ine **I**nterface **M**odule (**SLIM™**) device, demonstrating the unique advantages this part has over the more conventional solutions. Finally, two protection systems are analyzed in detail, and the measured performance of these is shown. These results, combined with the information contained in the note, will allow a linecard designer to completely specify the protection components required to meet the desired performance level.

2.0 SLIC PROTECTION PROBLEMS

To understand the problems in protecting line circuits, a basic review of the traditional protection layout is useful in appreciating the direction in which protection technology is moving. The line interface protection networks are traditionally split into primary, secondary, and tertiary protection components. *Figure 1* shows the layout of a conventional switch protection scheme for both subscriber and trunk lines exiting the central office. The secondary and tertiary levels are normally combined at the linecard. The protection levels are typically 1000V peak after primary protection and around 80V peak after secondary protection. This value is, of course, dependent on the clamp voltage of the shunt protection element used in the secondary circuit.

2.1 Primary Protection

The primary components are responsible for handling the large disturbances such as a lightning strike close to the central switch location. They are normally situated on the main distribution frame (MDF), where the subscriber cables enter the office. All disturbing currents arrested by the primary protection components are directed away from the main body of the switch, via a separate protection ground connection and are discharged harmlessly to earth. A typical implementation of primary protection would employ gas discharge tubes (GDT), which limit the voltages exiting the MDF to less than 1000V peak. The benefit of positioning primary protection on the MDF is twofold.

Firstly, it avoids having large transient currents flowing in the office wiring. This ensures that the current rating of the wiring is never exceeded, and also ensures that the voltages present after the MDF are relatively low (less than 1000V peak), which avoids any damaging secondary arcing between adjacent points inside the office. Secondly, by ensuring that the energy is shunted safely away to earth, the operation of the majority of the switch remains unaffected. This is especially important when serving large rural areas with a high incidence of thunderstorms.

2.2 Secondary Protection

The secondary protection components reside either on the linecard itself, or immediately on the backplane adjacent to the card connector, and are designed to handle the residual current which passes the primary protection. This consists of power cross currents and power induction products which are of sufficiently low voltage to pass through the primary protectors. The secondary protection schemes employ two separate elements to protect the sensitive line card components. Firstly, a series element which limits the current flowing onto the linecard, and secondly, a shunt element which limits the voltage. This shunt element can be a simple bridge rectifier connected between the battery terminals which shunts the current to either battery or ground, or more commonly, an active thyristor device which shunts the current to protection ground only. This device, when triggered, returns transient energy either to the local protection ground connection at the linecard or, preferably, returns it to a remote protection ground, usually the same as the protec-

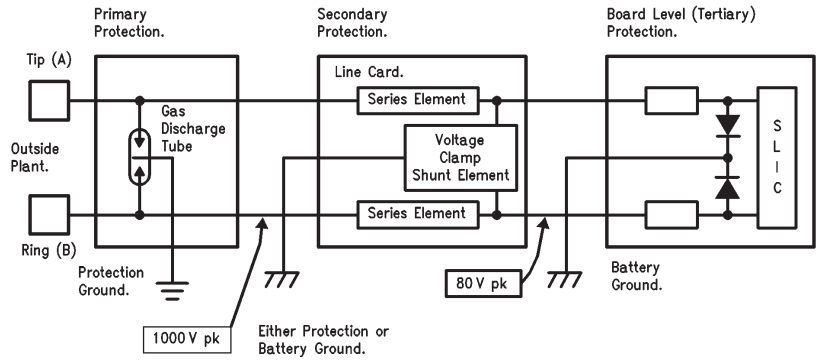


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FIGURE 1. Conventional Switch Protection Arrangement

tion ground used on the MDF. When using remote grounds, this can give rise to 1000V differences between Battery ground and the protection ground. This configuration is popular in North America and specialized knowledge and design techniques must be employed to cope with this since the voltage stress on the line card components is high. The **SLIM** device is one of the few devices which can meet this requirement and thus is especially useful for applications using separate ground systems.

While providing the necessary protection, the protection components must not degrade the transmission characteristics in any way during normal speech and signaling modes. It is this area that compromises between good protection and meeting specifications are frequently made, but these are avoided when using the **SLIM** device.

3.0 PROTECTION COMPROMISES

There are two areas which affect the selection of the protection components used. These are the DC voltage headroom requirements for the electronic SLICs to operate correctly, and the Longitudinal Balance requirements imposed on the circuit by the transmission specifications.

3.1 DC Headroom Limitations

The DC headroom implications are shown in *Figure 2.* In order for an electronic SLIC to function correctly, a certain voltage headroom is required for linear operation. This means that there is an interaction between feeding line current to the maximum long loop requirement, and allowing sufficient headroom for SLIC amplifer operation. From *Figure 2*, it can be seen that line current flows from the amplifier via Rprotect, the series protection elements. If the values of these are not carefully chosen, the voltage headroom may be impacted, and hence maximum long loop requirements compromised.

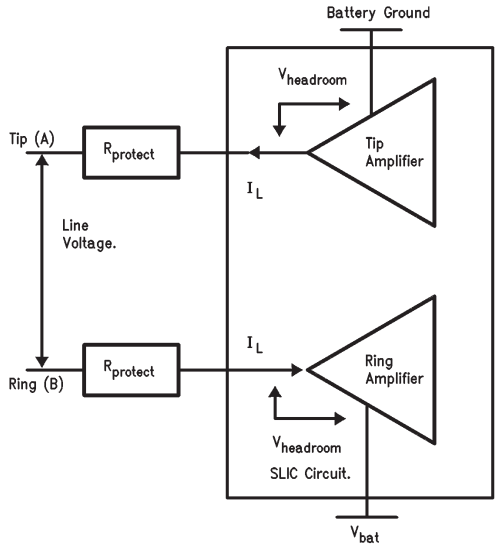

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FIGURE 2. DC Headroom Limitations

The longitudinal balance tests are probably the most stringent requirements placed on the front end of the line interface circuit, and are normally directly affected by the selection of the protection resistors. In order to meet these requirements, the matching of resistance from the Tip(A) and Ring(B) legs of the circuit to ground must typically be better than 1%. In most circuits, the burden of this precise matching requirements is placed directly on the series protection elements. This results in escalating costs for these components, but with the **SLIM**, these precise requirements are eliminated.

However, the problems of DC headroom and longitudinal balance can be eliminated if resourceful design techniques are employed to desensitise the series protection elements from impacting the feeding law. These techniques are employed in the new National Semiconductor **SLIM** which, by optimal use of complementary technologies, removes much of the restrictions on accuracy requirements from the protection components.

3.3 SLIM Protection

The National Semiconductor **SLIM** device is a completely new concept in subscriber connections to the central switch which uses a mixture of technologies to attain an optimal performance/cost ratio. This ratio is not just in the component cost required to implement the SLIC function, but the total manufacturing cost. The **SLIM** device is designed to minimize the number and cost of external components resulting in a substantial cost saving on a complete line circuit basis. This system cost reduction philosophy is particularly prevalent in the way the protection scheme is implemented. The tolerances for the protection components are orders of magnitude less than normally required to attain the performance levels which this part achieves, with a corresponding reduction in the cost of these components. A working knowledge of the principles employed to allow this will now be presented, followed by some results showing how insensitive the technique is to changes and mismatches in the protection components.

Conventional protection schemes, outlined in *Figure 1*, separate the linecard protection into secondary protection and tertiary protection. Using the **SLIM** approach, the module itself carries the tertiary protection components, and the series elements of the secondary protection are included in a sensing loop which cancels any errors which may arise due to poor matching of the resistance values as shown in *Figure 3*. The benefit of this approach is that the burden of matching these components is removed to a large degree from the board manufacturer.

This approach is only possible using a careful mix of technologies which enable the voltage ratings at the primary/secondary interface to be met. This is achieved by manufacturing SLIM on a thick film hybrid module which will stand in excess of 1000V peak without failing. By using these thick film techniques, and by accurately trimming, a very high degree of longitudinal rejection can be maintained. Typical figures of 75dB are measured at the final test stage of the completed module using 100Ω, 1% protection resistors.

Since the module employs a control loop to guarantee the longitudinal balance of the system, it can also synthesize the longitudinal terminating resistance on each leg of the subscriber line, i.e., the resistance from each leg to ground

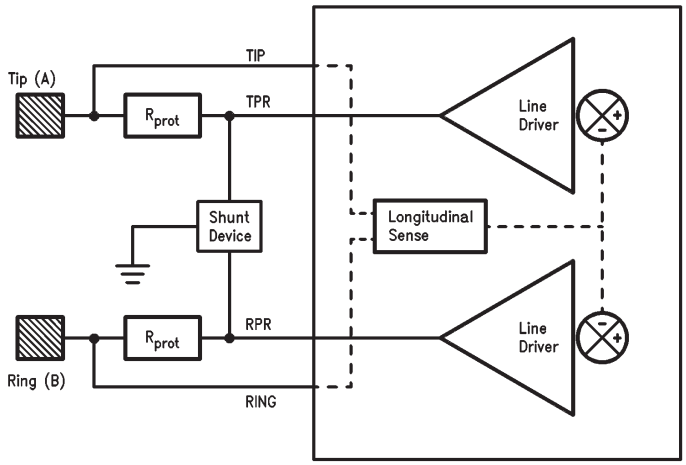

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FIGURE 3. SLIM Protection Arrangement

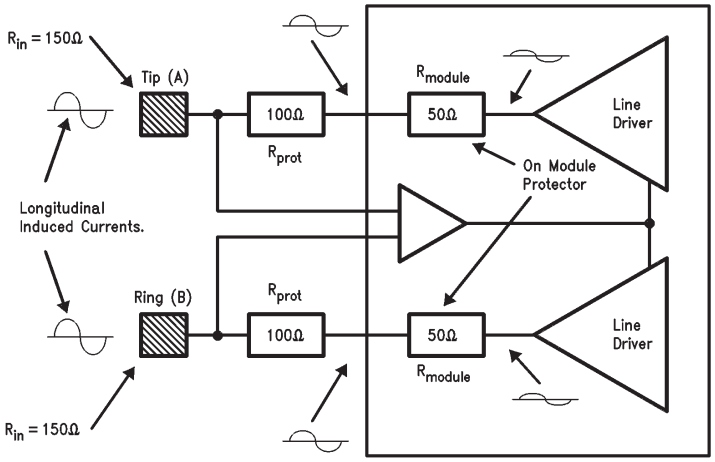

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FIGURE 4. Synthesized Longitudinal Resistance

in response to longitudinal signals. The advantage of synthesizing this resistance is that the control of longitudinal voltages appearing at the line terminals is much tighter, maintaining a more consistent longitudinal balance figure. Secondly, and more importantly, by carefully matching the synthesized resistance with the physical resistance consisting of the on module resistance and the external protection resistance, an improvement in signal handling capability in the presence of high levels of longitudinal current can be achieved. *Figure 4* shows this graphically.

Referring to the conventional protection layout in *Figure 1,* it is important that the module protection is sufficient to withstand the currents which are allowed to pass through the secondary shunt protection device. Using the **SLIM**, the module has series protection elements incorporated in the design which are capable of surviving in excess of 80V each leg. The applications advantage of this is that the shunt protector can be directly connected across the output of the **SLIM** device at the TPR and RPR terminals.

Overall the **SLIM** device has been designed with the end application in mind. The optimum mix of technologies has been used to achieve the most cost effective solution to the OEM, not just in component cost, but also in the external components and manufacturing costs. This philosophy can be seen in the way in which the protection function is partitioned, enabling the user to achieve previously unattainable levels of performance from wide tolerance components. It is this systems approach to the problem which enables **SLIM** users to obtain a competitive advantage compared with conventional solutions to the protection problem. The remaining sections of this applications note will deal with the results of laboratory tests, followed by an examination of the various protection options available with this versatile device, outlining the strengths and weakness of the different solutions.

4.0 LABORATORY MEASUREMENTS

The previous sections have concentrated on the effectiveness of the **SLIM** device in meeting longitudinal requirements while incorporating very loose tolerance protection components. However, as yet there have been no quantitive measure of the performance which can be attained with the part. The results which are presented here were measured under laboratory conditions using a Wilcom T207E Longitudinal Balance Test Set, measured in accordance with IEEE 455-1976 Recommendations. The tests were measured on typical devices from standard production runs, and are representative of the results which can be expected from a **SLIM** based line circuit.

The tests were designed to investigate the behavior of the part under 3 different line conditions, while varying the protection resistances, $R_{protect}$. The graphs show results for 3 different test frequencies to allow appreciation of the sensitivity of the results. The devices were tested for sensitivity to the absolute value of resistors (both resistors matched to within 0.1%) and then the mismatch sensitivity between the two protection resistors, one resistor being held constant and the other was reduced in value. This second test was carried out with the fixed resistor having the values of 120Ω, 100Ω, and 80Ω, the other leg having resistors 20% different.

The results presented below are the worst case results of the devices tested. The measurements were made at 0 mA, 20 mA, and 42 mA line current. These correspond to on-hook, 1900Ω loop resistance, and 750Ω loop resistance.

4.1 Absolute Value Sensitivity

Figures 5, 6 and *7* show the results of Longitudinal Balance against Resistor Value of Rprotect both resistors matched to within 0.1%. These results are measured at 62 Hz, 1000 Hz, and 3400 Hz for the 3 stipulated line conditions.

The overall trend of these results indicate that the Longitudinal Balance is better than 60 dB for all values of protection resistor between 90Ω and 120Ω. Values substantially greater than 120Ω are not recommended since these will reduce the operating voltage headroom of the output amplifiers as explained earlier.

4.2 Matching Sensitivity

The tests for the matching sensitivity were carried out in a similar fashion except the resistor in one of the legs was held constant. The results recorded in *Figures 8, 9* and *10* indicate the worst case result between the two legs. The results shown in *Figure 8* illustrate the trade-off between resistor matching ratio and the longitudinal balance which can be achieved for I_{loop} = 0 mA, while *Figures 9* and *10* show I_{loop} = 20 mA and 42 mA respectively. This is shown for fixed resistors of 120Ω, 100Ω, and 80Ω while the other leg was varied. The graphs show the results for 20% mismatch between legs. From the graphs, it can be seen that the longitudinal balance achieved using very loose tolerance parts is very high. If tighter specifications are required, slightly closer tolerance resistors may be specified, but these are still cheaper than the high tolerance devices required to meet these specifications using conventional line circuits. It is important to note that during all these tests,

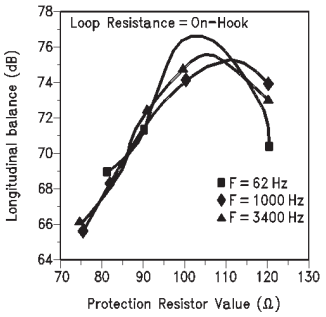

FIGURE 5. Longitudinal Balance vs Resistor Value

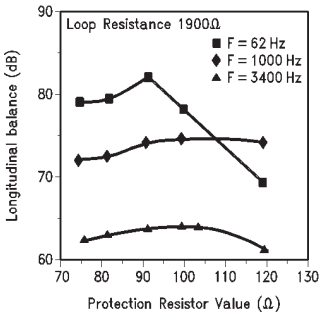

FIGURE 6. Longitudinal Balance vs Resistor Value

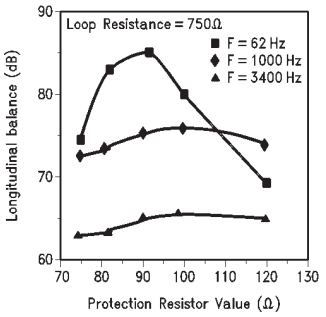

FIGURE 7. Longitudinal Balance vs Resistor Value

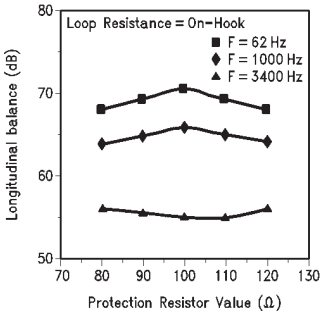

FIGURE 8. Longitudinal Balance for 20% Mismatch

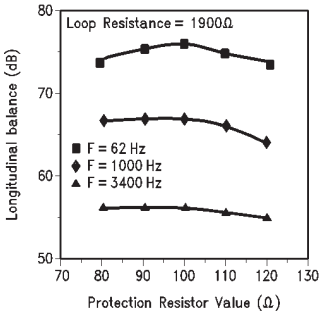

FIGURE 9. Longitudinal Balance for 20% Mismatch

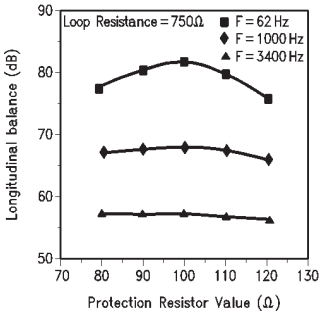

FIGURE 10. Longitudinal Balance for 20% Mismatch

the module passed all the longitudinal capability tests, easily handling the 21 mArms per leg specified in the Datasheet.

Summarizing the results presented in this section, the absolute value of the resistors can be in the range 80Ω to 120Ω, with a matching tolerance up to 20%. However, in order to meet the more stringent requirements such as Bellcore, and to cope with the long term effects of Lightning and power cross, the resistors should be 100Ω, ±5%. This will ensure meeting the requirements at end of life. These results now enable protection options to be examined in detail, and with an understanding of the capabilities of the **SLIM** device, a prediction of the effectiveness of these options can be made.

5.0 PROTECTION OPTIONS

These options can be split into roughly two areas, which follow slightly different philosophies regarding the purpose of protection. These are Fusible, or manual resettable systems, and Auto-resetting systems. Both of these consist of the same elements. The difference between these is the type of series protection element used. Before discussing the differences in detail, a study of the individual protection components is worthwhile.

5.1 Shunt Protection Devices

The shunt protection device in this application can be any one of three configurations. *Figure 11* shows the least expensive shunt protector available for the application. It consists of a bridge rectifier connected across the subscriber wires, and returning the fault current to either the battery ground or the battery supply, dependent on the polarity of the fault current. This system is very effective at protecting the line circuits since the voltage transitions are restricted to approximately a forward diode voltage beyond the supply rails, however, the injection of large fault transients onto the battery supply is not desirable for many administrations. This is particularly a problem when the negative battery potential is generated using a switch mode power supply, which while capable of sourcing large currents, is incapable of sinking current. A fault condition which dumps substantial current into the battery could increase the battery potential causing damage. If this protection system does prove adequate for the application, then the required specification for the diode bridge is 20A surge capability (2A continuous), 100V rating.

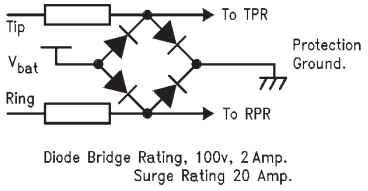

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FIGURE 11. Low Cost Shunt Protector

The second shunt protection configuration, *Figure 12*, is designed to avoid dumping the fault transients into the office battery supply, thus ensuring that the battery potential remains unaffected during a fault condition. In this circuit, the positive going transients are returned to battery ground connection as in the diode bridge, but the negative transients are passed to a transient surge protector.

This 2 terminal device operates as a voltage/current sensitive thyristor. When the voltage appearing at the terminals of the device exceed the zener voltage (V_Z) rating of the device, the unit enters a voltage clamp region. If the fault voltage continues to rise, the current into the shunt protector will rise correspondingly through the series protection element, until the breakover current threshold (I_{bo}) is exceeded. At this point the device fires, causing the voltage across the device to collapse, and returning all the current to the battery ground terminal. The device remains in this state until the current has reduced to below the holding current of the device, whereupon the protector resets itself.

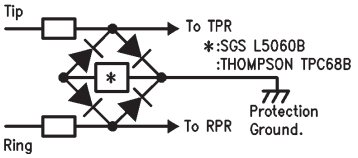

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FIGURE 12. Protection Using a Shunt Suppressor Device

To aid understanding, the V-I characteristics are shown in *Figure 13*, highlighting the important features on the characteristics. This diagram also shows the characteristics of the two basic types of suppressor; namely symmetric and asymmetric types. The Asymmetric (shown dotted), have the advantage of a forward diode characteristic in one direction which reduces the power dissipated by the SLIC during a fault condition.

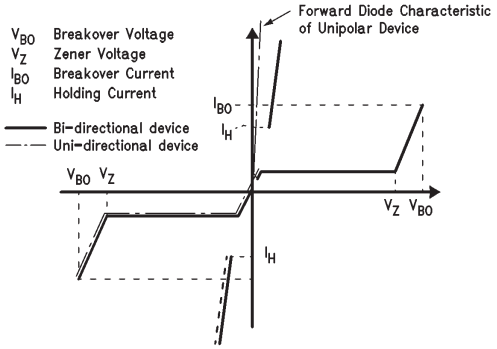

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FIGURE 13. Shunt Suppressor V-I Characteristic

The final shunt protection scheme, *Figure 14*, is a development of the circuit shown in *Figure 12*. In this circuit, the diode bridge is discarded, and the two shunt components are replaced by a single device. This 3 terminal device protects against faults occurring between the two subscriber wires and to ground. These devices are slightly more expensive than the previous option, but are competitive when the savings in board area and assembly costs are taken into account.

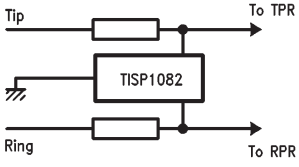

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FIGURE 14. Terminal Shunt Protector

For use with the **SLIM** module, the ideal type of shunt protector is the unipolar type since this limits the potential to within a forward diode voltage (V_{BE}) of the battery ground potential. The advantage of this is a limitation of the power dissipation on module during a fault condition. The breakover voltage should be 85V or less, but the breakover current is not important for correct **SLIM** operation. The choice of 2 or 3 terminal can be made on a purely financial basis of whether the addition of a diode bridge circuit increases the cost over the 3 terminal device.

5.2 Series Protection Elements

To complete the protection function, a method of limiting the current into the shunt device is required, and this is the task of the series elements. These elements, one in each of the subscriber wires operate by, in the case of fusible systems, interrupting the current flow after it exceeds a predefined value, or, in the case of auto-resetting systems, by reducing the current level to a safe level when hot. To ensure that the choices are not constrained, the strengths and weaknesses of both manual and auto resetting systems are put forward, thus allowing the designer to appraise both systems and choose the most suitable one.

The choice of series protector must be made with the protection specifications in mind. Many specifications require that the protection components must withstand a particular level of disturbance without damage. Usually it is these which govern the choice of series element. The principle factors affecting the choice are the power dissipation of the device during a fault condition, and the rupturing current in the case of fusible systems. However, if there is a time constraint placed on the test conditions, the thermal mass of the device must be incorporated into the calculations, though this can often be done by referring to the manufacturers datasheet which contains this information.

The choice between a fusible and a resettable system is one which is often governed by the specifications, usually because the resettable systems cannot achieve the long term balance requirements. As has been shown in the results section previously, this constraint does not apply to users of the **SLIM** device, thus opening new opportunities to users who desire auto-resetting protection without the compromise on balance performance.

5.3 Fusible (Manual Resettable) Systems

The benefit of employing a manual resettable system is that if a fault occurs on a particular line, after the protection has been fired, the line is disconnected from the switch until the fault is cleared and the system reset. This means that the remainder of the switch can function completely, without the board heating problems etc. which may occur using other protection systems. However, the disadvantage of the manual system is the requirement for human intervention to replace or reset the line protection. This is especially important in a distributed switch system where the protection circuits are not all in the same location.

Figure 15 shows the schematic for a fusible protection circuit. The series elements can be fuses, resistors, or circuit breakers which are triggered if the rupturing current of the device is exceeded. For the **SLIM** device, the maximum current which the element must pass for correct operation is the maximum line feed current plus the worst case longitudinal current which may appear on line. However, many authorities require that the protection elements can withstand a short term power cross for a finite period of time, a typical

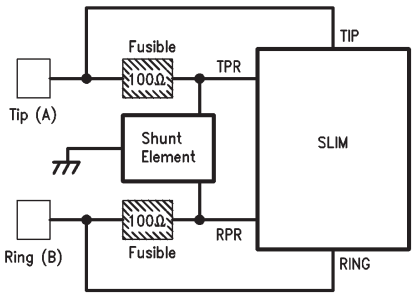

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FIGURE 15. Fusible Resistor Implementation

example may be 200 Vrms, from a generator impedance of 150Ω for a period of 5 seconds. The reason for this is to ensure that the protection systems do not trip on short term faults caused by a transient power cross situation, but survive long enough for the electricity supply authority circuit breakers to respond to the fault, thus avoiding a false or unnecessary failure.

Until now, the manual resettable or fusible systems have been most popular in the industry since the matching accuracy of the series elements can be carefully controlled to ensure good balance. The problem in the future using this type of protection is the expansion in distributed switching systems employing local street furniture. The costs of replacing protection in these locations is much greater, but it is argued that the incidence of faults will also reduce due to the shorter line lengths. In order to reduce this cost to a minimum, and improve the time taken to reinstate service to the client, auto resetting systems can be more effective, and these are described in the following section.

5.4 Auto-Resetting Systems

The Auto-Resettable protection system has always been attractive to line card designers. The inherent advantage is the system guards against any fault which may occur on the line, and after occurence, resets automatically, without any requirement for human intervention. Unfortunately, the compromises to achieve this were traditionally too great to warrant the change to auto systems. With the advent of the **SLIM**, these compromises are not necessary, and the implementation of automatic protection becomes a realistic possibility irrespective of the severity of the longitudinal balance specification.

The basic principle behind these protection schemes is the use of a PTC device as the series element in the secondary protection circuit. During a fault condition, this device dissipates power which causes self heating. The temperature increase of the device causes the resistance to increase, thus regulating the current flow. Eventually, thermal equilibrium is reached, and this state is held until the fault condition is removed. The device then cools and normal service is re-established. The choice of the PTC device is relatively painless once the critical parameters are decided, but to understand the impact of these parameters, an appreciation of the operation and construction of the device is useful.

6.0 PTC CONSTRUCTION AND OPERATION

Positive temperature coefficient devices come in a variety of forms depending on the application required. For the line card protection application, the devices required are designed to act as switching elements with a carefully defined,

abrupt switching characteristic. The most common method of implementing the switching function is to use thermistors. The operation of these is now discussed.

6.1 Thermistors

Switching type PTC thermistors are made from semiconducting barium titanate ceramic material. This material exhibits a temperature-resistance characteristic as shown in *Figure 16.* Over the lower portion of their characteristic, the thermistor resistance is low and relatively constant (a slight negative coefficient is present at low temperatures due to the intrinsic negative temperature coefficient from the semiconducting material). As the temperature is raised above the Curie point, the magnetic domains in the material realign themselves, and the material becomes more resistive until eventually the material approaches an insulator. In a switching type of device, this action is designed to take place abruptly over a 10–15°C temperature change. Over this range, the resistance of the thermistor changes by five or six orders of magnitude, from say 10Ω to 1 MΩ.

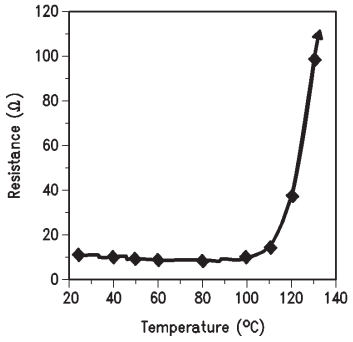

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FIGURE 16. Thermistor Temperature-Resistance

If, instead of using external temperature as the heating source, current flowing through the device is used, the traditional V-I characteristic for this type of device can be measured, see *Figure 17*. This curve has two distinct regions which are important for the application.

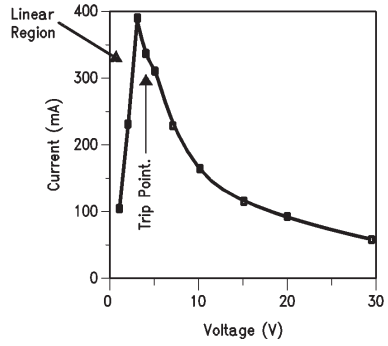

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FIGURE 17. V-I Thermistor Characteristics

First the linear region. This is the area of normal operation where the device does not exhibit any switching behavior. If current value less than the value of the trip current, It, is flowing through the device, the temperature rise of the thermistor is insufficient to trip the device. If however, the current is increased above the trip level, the temperature rise is sufficient for the resistance to increase. To ensure correct operation in the application, the thermistor chosen must be rated so that the Trip Point is never exceeded during normal operation at the maximum ambient temperature.

6.2 Maximum Ratings

When using thermistors it is imperative never to exceed the manufacturers ratings for the device. These ratings give the maximum voltage and current which the device is capable of switching. The voltage rating is principally defined by the thickness and resistivity of the device. The switching current rating is very important since exceeding this value will cause the device to fracture. This is caused by the physical properties of the material which have an intrinsic energy-time product capacity. If attempts are made to dissipate an excessive amount of energy, the differential expansion inside the device due to local heating set up large stresses in the brittle ceramic material which consequently shears and fractures. In general the larger the cross sectional area of the device, the greater the switching current can be handled, and this parameter is one of the most crucial in selecting the correct device.

If these limits are not exceeded, the resistance value of the thermistor is very predictable, and will return to the initial starting value repeatedly, independent of the number of switching cycles the device has undergone. In lab tests, a thermistor was repeatedly hit with a 30 second burst of 250 Vrms mains voltage, sufficient to stress it at the maximum ratings, then allowed to cool for 5 minutes, after which a resistance measurement was made. This cycle was repeated over 450 times, and the results logged. The resistance of the device did not vary more than ±0.5% over this test.

Hopefully, this is sufficient to dispel the myth that thermistors are unstable devices and are not repeatably resettable after undergoing numerous switching operations. Now that the basic operating principles of thermistors have been explained, the limitations from an applications point of view can be appreciated, and put into context.

6.3 Specifying Thermistors

As outlined in the above section, thermistors have five basic parameters which must be specified on ordering. These are:

1. Operating temperature range. Normally for telecom equipment this is 0°C to +70°C. This does not need to take the temperature rise due to self heating into account.
2. Maximum operating current (non switch). This is normally in the range 80–100 mA, for most telecom applications. It is important to rate this parameter at the maximum operating ambient temperature.
3. Maximum voltage rating. This parameter is set by the voltage which the device must withstand when the source resistance of the generator is zero. This is important when the resistance of the device increases to a high value, (much greater than the source resistance of the generator), when the rating should be equal to or exceed the test voltage.

4. Maximum current capability. This parameter must be chosen dependant on the peak cold current the device will be required to handle at the instant a fault occurs.
5. Finally, the cold resistance of the device. This will be defined to a large extent by the previous parameters, but if a choice exists, should be chosen to be as large as possible in order to increase switching time, and reduce the currents injected into the line card during a fault.

7.0 WORKED EXAMPLE 1

Take the case of a linecard which must survive a mains cross fault of 250 Vrms for 15 minutes, from a source resistance of 30Ω, after which the part must reset to normal operation. Assume that the longitudinal specification must exceed 50 dB across the frequency band 50 Hz to 3400 Hz. Operating temperature range 0°C to +70°C.

First, referring to the performance graphs in the measurements section, it can be seen that the absolute value, and the matching requirements to meet this spec are very loose, so we have a relatively free choice for the value of device we eventually choose.

1. Temperature Operating Range: 0°C to +70°C.
2. Operating current. The **SLIM** device has a maximum feed current of 43 mA. Modulating this, the worst case longitudinal current, say 20 mArms, gives maximum operating current of 48 mArms. Therefore require a thermistor which must be able to handle 48 mArms at the maximum operating temperature (70°C). Note the use of RMS currents since we are interested in the heating effect of the current.
3. Voltage spec for device: 250 Vrms (min). (Since the resistance of the series element will increase to become much greater than the source resistance.)
4. Peak current handling requirements. Given that the test condition has a 30Ω source impedance, then short circuit current capability of the source is 12 Apeak (8.33 Arms). This suggests a fairly large thermistor to withstand a peak current as high as this. A suitable device which has a current rating close to this is YS960 which has a peak current rating of 10A. This device has a cold resistance of 10Ω, which when added to the source resistance gives a total resistance of 40Ω across the 250 Vrms source. This gives a peak current of 8.83A.

An alternative method is to choose a thermistor with a higher cold resistance. This increases the resistance in series with the source resistance thus reduces the peak current handling requirements. If a thermistor has a cold resistance of 40–50Ω, it only requires to handle a maximum current of 5A in the example given, and has the added advantage that the current flow into the protection ground is also reduced. This tradeoff is dependent on the availability of suitable thermistors. The calculation of this parameter must always be done using this somewhat iterative method to arrive at a suitable device.

The choice of a suitable device is often restricted by the limitations of one of the test requirements, and experience shows that this is often the peak current requirements. After the device has been selected, the predicted performance level can read off the graphs plotted in the results section checking the validity of the selection.

8.0 WORKED EXAMPLE 2

If the longitudinal requirements are much more strict, such as those imposed by the Bell specifications, the value selected becomes more critical. Referring to the results graphs suggests a value of 75–120Ω for the series elements. In the case of the thermistor selected in the first example, this is not so, but can be made very easily. Since the shunt protector device is connected across the junction of the series elements and the module pins, anything behind this node is protected by the secondary protection. In order to improve the longitudinal balance performance of the circuit, it is necessary to place additional resistance in series with the thermistors to increase the combined value of the resistance closer to 100Ω. This can be done with two resistors which would raise the resistance to around 85Ω overall. Care should be taken in the power rating of these resistors since during fault conditions, these must cope with the difference in shunt protector trigger voltage, Vbo, and the battery supply. This can cause a substantial amount of power to be dissipated in this condition. A schematic showing the implementation of this technique is given in *Figure 18.*

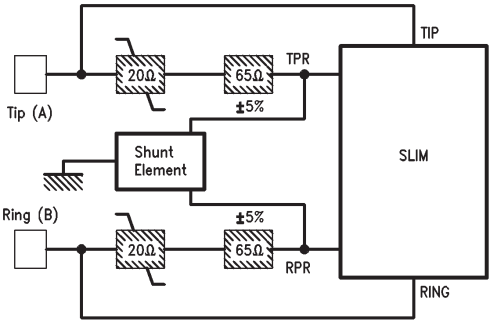

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FIGURE 18. Protection Schematic for Stringent Longitudinal Requirements

9.0 CONCLUSIONS

At the outset of this applications note, the objective was to show the ease of designing protection networks using the **SLIM** module. Due to the philosophy behind the **SLIM** of reducing the cost of the overall application, the protection constraints are much less stringent than in conventional line interface circuits, which allows previously unavailable protection schemes to be employed. Below is a summary of the advantages and disadvantages of the fusible and auto-resetting systems.

Fusible Systems

Advantages

1. Low Installation Cost.
2. Low Power dissipation on board during fault conditions.
3. Total disconnection of subscriber wires when fault occurs.

Disadvantages

1. Relatively high replacement costs.
2. Labor intensive, especially in distributed switching systems.
3. Non-resettable, thus causing unnecessary out of service time for users.
4. Possibility of operating due to transient fault.

Auto Resetting Systems

Advantages

1. Good for remote locations.
2. No unnecessary down time for users.
3. Completely automatic.
4. Low maintenance.
5. Low instances of transient operation.

Disadvantages

1. Increased Installation costs.
2. Small amount of on-card heating due to thermistor dissipation (2–3W).
3. Line not totally disconnected during fault condition.

Given these choices, and bearing in mind the industry moving toward decentralized switches, the auto resetting systems technique is more applicable to the requirements of the market where maintenance costs are at a premium. There are now companies taking advantage of this opportunity and manufacture complete modules containing the thermistors and shunt protectors designed for direct mounting onto the line card. These modules are ideal for applications attempting to minimize the board footprint for compact systems employing 16 lines on a card, but do incur a slight cost penalty.

Finally, included as an appendix to this note is a list of suppliers of shunt protectors, series fuse elements, fusible resistors or fusible links, and a supplier list of thermistors. This list is not intended to be exhaustive, but more a starting point for those who are interested in pursuing the subject further. It is hoped that in writing this note that the author has highlighted the major problems in trying to design protection schemes for line card applications, and helped in dispelling any misconceptions in the application of thermistors in this area.

APPENDIX

Below are listed suppliers of protection components. Suppliers of Fusible series protection components.

1. Welwyn Electronics.
Bedlington, Northumberland NE22 7AA England
Tel. (0670) 822181.

2. International Resistive Company, Inc.
Post Office Box 1860,
Boone, North Carolina, 28607-1860 USA
Tel. (704) 264-8861.

Suppliers of PTC Series Elements.
1. Raychem Corporation,
Polyswitch Products, 300 Constitution Drive
Menlo Park, Calif., 94025-1164 USA
Tel. (415) 361-6900.

2. Mullard Ltd.
Mullard House, Torrington Place
London, WC1E 7HD

3. STC Components
Thermistor Division,
Crown Industrial Estate,
Priorwood Road,
Taunton,
Somerset,
TA2 8QY.
England.
Tel. (0823) 335200.

Suppliers of Shunt Protection Devices.
1. Texas Instruments,
Power Products Division.

2. Teccor Electronics Inc.
1801, Hurd Drive,
Irving, Texas 75038-4385 USA
Tel. (214) 580-1515.

Lucas Semiconductors Ltd.
Garetts Green Lane,
Birmingham.
B33 0YA.
England.
Tel. (021) 784-6855.

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National Semiconductor GmbH
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D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

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Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

Submission X

Type	Reference	Title
Patent	US 7266302	Asymmetric Optical Network Traffic Flow Con
Citations	**2**	

US007266302B2

(12) **United States Patent**
Bremner et al.

(10) **Patent No.: US 7,266,302 B2**
(45) **Date of Patent: Sep. 4, 2007**

(54) **ASYMETRIC OPTICAL NETWORK TRAFFIC FLOW CONTROL**

(75) Inventors: **Duncan J. Bremner**, Lochwinnoch (GB); **Finn Helmer**, Blanefield (GB); **Eivind Johansen**, Horsholm (DK)

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 674 days.

(21) Appl. No.: **10/353,426**

(22) Filed: **Jan. 28, 2003**

(65) **Prior Publication Data**

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(51) **Int. Cl.**
H04B 10/00 (2006.01)

(52) **U.S. Cl.** **398/138**; 398/139

(58) **Field of Classification Search** 398/135–139, 398/87

See application file for complete search history.

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S.L. Woodward and G.E. Bodeep, "A Full-Duplex Optical Data Link Using Lasers as Transceivers," IEEE Photonics Technology Letters, Sep. 1, 1995, pp. 1060-1062, vol. 7, No. 9, IEEE, Inc., USA.

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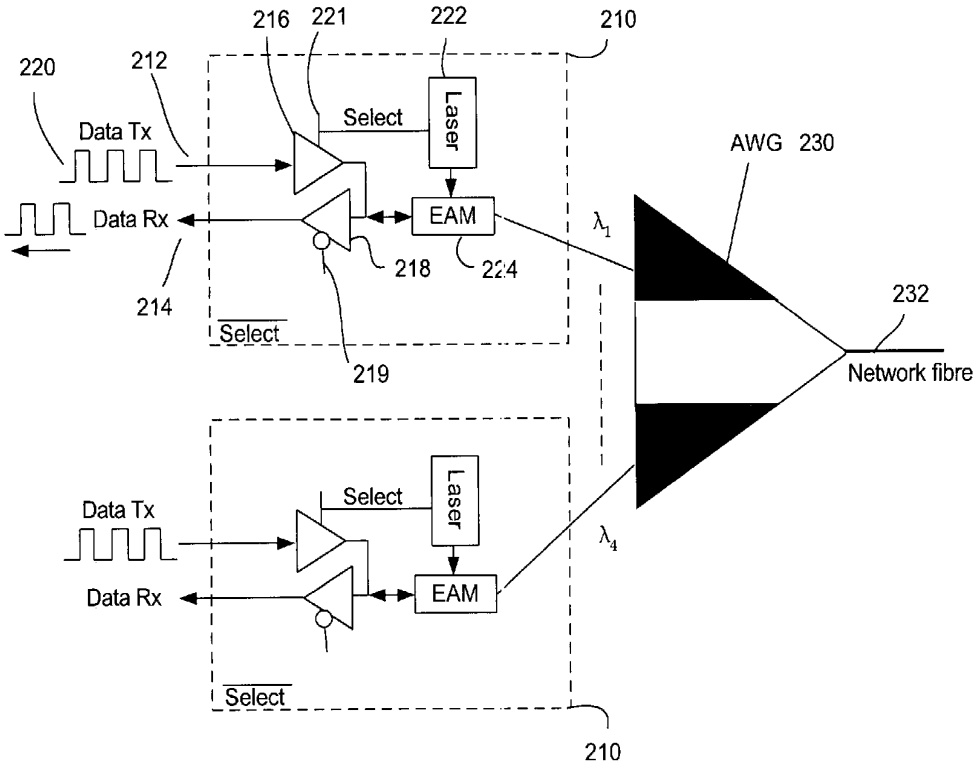
Primary Examiner—Christina Leung
(74) *Attorney, Agent, or Firm*—Kevin A. Reif

(57) **ABSTRACT**

An optical network may be configured dynamically so that a given channel wavelength can operate in either direction over a fiber in a network. Thus, network providers can provision bandwidth according to the traffic characteristics of the network link in question. A plurality of transceiver modules on either side of a fiber may be switched from a transmit mode to a receive mode depending on the desired direction of the channel.

10 Claims, 4 Drawing Sheets



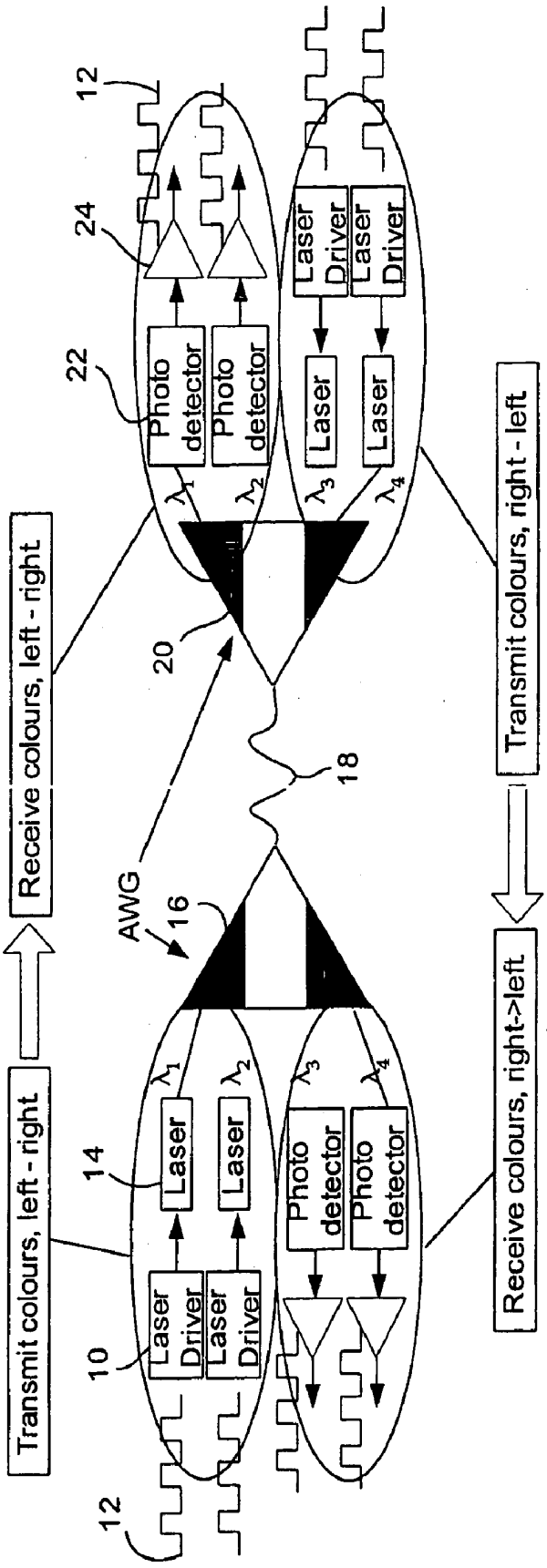


Fig.1
(Related Art)

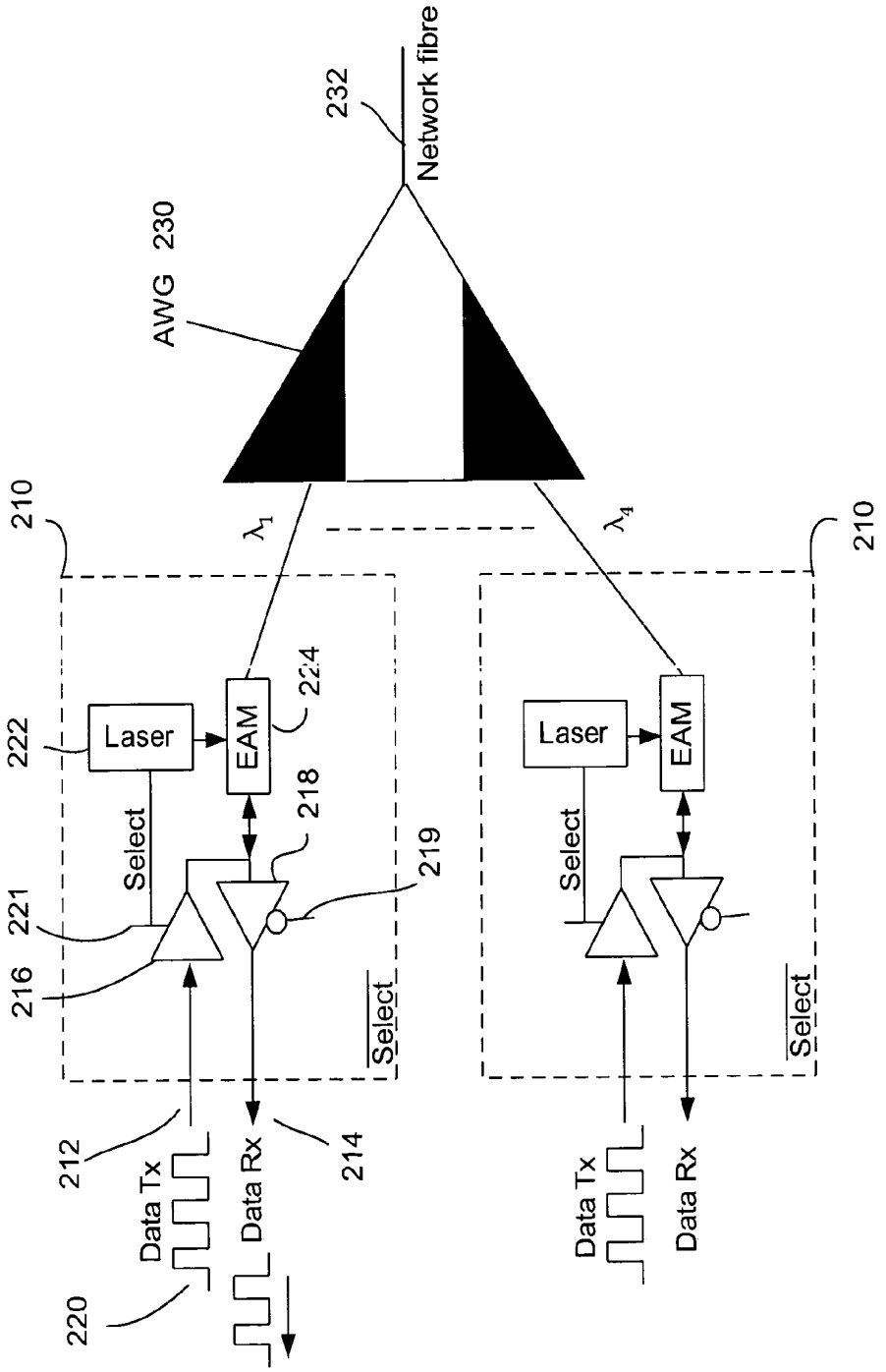

232
Network fibre
AWG 230
210
λ_1
λ_4
210
222
Laser
EAM
224
218
219
Select
221
216
Select
212
Data Tx
Data Rx
214
220
Laser
EAM
Select
Select
Data Tx
Data Rx

Fig. 2

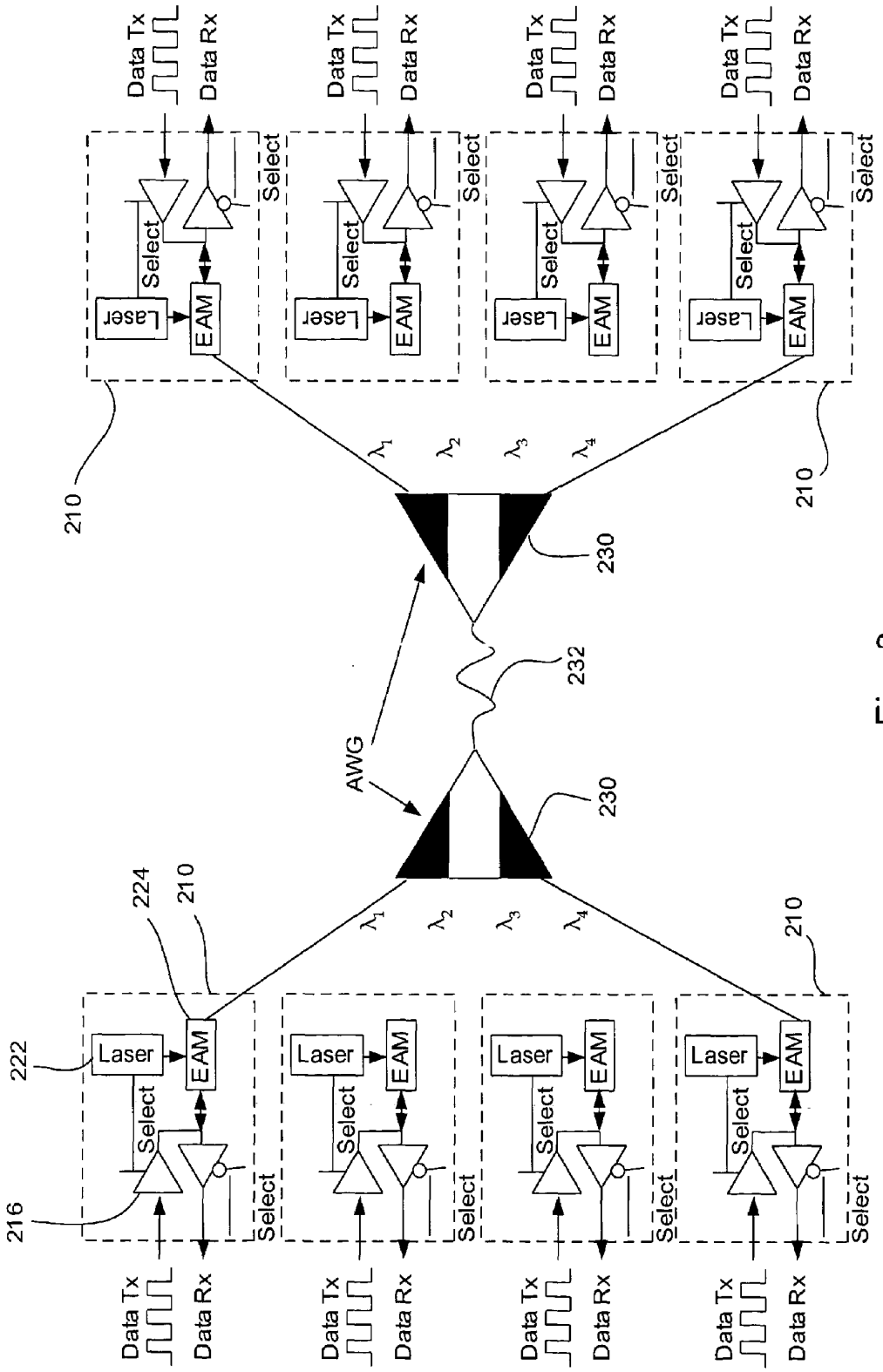

Data Tx
Data Rx
Select
Laser
EAM
210
222
224
216
230
232
AWG
λ_1
λ_2
λ_3
λ_4

Fig. 3

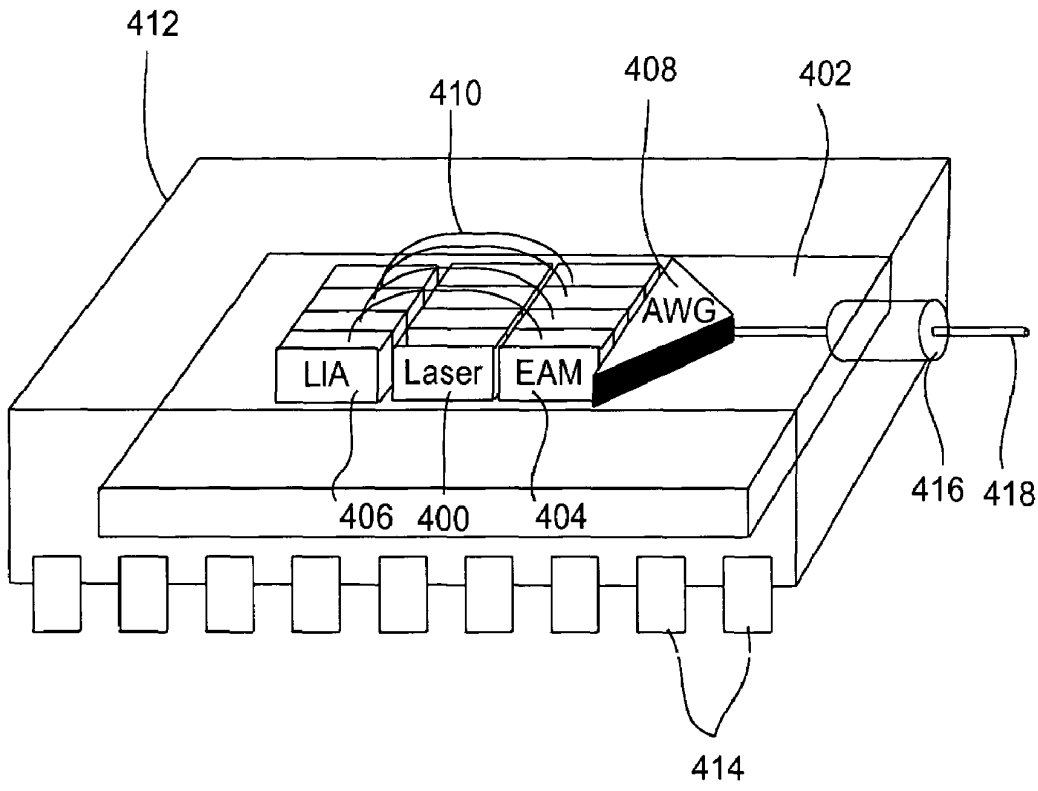


Fig. 4

ASYMETRIC OPTICAL NETWORK TRAFFIC FLOW CONTROL

FIELD OF THE INVENTION

An embodiment of the present invention relates to optical networks and, more particularly, to configurable optical networks where the direction of a particular channel may be dynamically allocated depending on traffic demand.

BACKGROUND INFORMATION

The field of optical communications, that is communication using optical fibers, transmitters, receivers, modulators and amplifiers, is becoming more mature and cost competitive. Additionally, in order to manage the increasing demand for bandwidth over an optical fiber, it has become necessary to introduce a technique know as Wave Division Multiplexing (WDM).

WDM technology comes in two basic forms. These include Coarse WDM (CWDM) and Dense WDM (DWDM). Both work in the optical domain, very similar to frequency division multiplexing in the electronic domain. Instead of using a single laser (i.e., single color or wavelength) to communicate across a fiber optic network, WDM uses several different wavelengths to increase the capacity of a single optical fiber by modulating each color with a different data signal and hence increasing the capacity of a single fiber by the number of colors or channels it can carry simultaneously.

By increasing the number of colors carried by a single fiber the number of channels and hence the bandwidth of the fiber is increased. However the traditional method of increasing capacity involves providing transmission 'pairs', each pair comprising one path or wavelength to transmit and another path or wavelength to receive. In some applications, this may not be the ideal provisioning scheme as it limits the traffic in each direction to be approximately equal.

Referring to FIG. **1** it can be seen that the number of channels going from left-right and those running from right-left are fixed and remain in an assigned direction. In particular, FIG. **1** shows a four wavelength (color) channel communication fiber with two colors (λ**1** and λ**2**) traveling down the fiber in a first direction (i.e., left to right) and a two colors (λ**3** and λ**4**) traveling down the fiber in a second, opposite direction (i.e., right to left).

On the left hand side of FIG. **1**, a laser driver **10** modulates a data stream **12** to drive a laser **14** producing a beam having the wavelength λ**1**. The beam λ**2** is produced in a similar fashion. The beams are wavelength division multiplexed using for example an array waveguide grating (AWG) **16**, and travel as a multiplexed beam across a fiber **18**. A similar AWG **20** on the right hand side of the communication channel **18** demodulates the beam into the individual wavelengths (λ**1** and λ**2**) where they are received by respective photo detectors **22** and amplified by their respective amplifiers **24** to output the original data stream **12**. Data channels λ**3** and λ**4** work in a similar fashion, only traveling in the opposite direction from right to left.

A drawback to the above design is that the direction a particular channel travels is fixed. This means that unless the original network designers anticipated that an asymmetric traffic profile is warranted, the normal implementation involves assigning an equal numbers of channels (wavelengths) in each direction. However, due to local traffic conditions or circumstances, it may be desirable to provide

an asymmetric path between nodes such that, say, the right-left direction can carry more traffic that the left-right direction.

A practical reason for desiring an asymmetric network may be demonstrated by considering the download of a music file or picture file from the World Wide Web (WWW) where the data requesting the song (title, artist, URL etc.) is many times smaller than the downloaded data itself. The effect of this asymmetric demand for bandwidth is that the network provider typically over provisions the upstream paths in order to meet the demands of the downstream paths.

A need may exist to dynamically to permit asymmetrical and programmable bandwidth over an optical fiber in either direction.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram showing a typical symmetrical multiple channel optical communication system having fixed channel assignment in each direction;

FIG. **2** is a block diagram of one side of a multiple channel optical communication system having an asymmetric, bi-directional configuration according to one embodiment of the invention;

FIG. **3** is a block diagram of a multiple channel optical communication system having an asymmetrical, bi-directional configuration according to one embodiment of the invention; and

FIG. **4** is a block diagram of a bi-directional transceiver module according to one embodiment of the invention.

DETAILED DESCRIPTION

Described is an apparatus and method to implement WDM technology such that each wavelength (channel) can be configured dynamically to operate in either direction over a fiber in a network. This may have the advantage that the network providers can provision bandwidth according to the traffic characteristics of the network link in question. Furthermore, it may be used to permit a degree of equipment 'sparing', sometimes referred to as equipment redundancy, by permitting channels to be re-allocated or re-directed to carry traffic previously carried by a faulty channel.

Referring to FIG. **2**, for each channel there may be provided a programmable block **210** that can be configured to either transmit or receive a particular channel. Each programmable block **210** includes an input port **212** and an output port **214**, and a pair of amplifiers **216** and **218**. The amplifiers **216** and **218** comprise select switches **219** and **221** that may be used to activate or disable the respective amplifiers **216** or **218**, depending on whether the programmable block **210** is in a transmit mode or a receive mode.

When configured to act as a data transmitter, an input data stream **220** (Data TX) is supplied to the input port **212**. The transmit switch **221** is selected to transmit the data and the receive switch **219** is deselected to disable the output port **214**. When the transmit switch **221** is selected, a laser **222** is likewise enable to begin lasing at the particular channel's frequency, in this case, λ**1**. The data stream passes through the amplifier **216** and is supplied to a modulator **224** to modulate the beam, λ**1**, from the laser **222**.

As shown, an electro-absorption modulator (EAM) **224** may be used to modulate the beam. EAMs generally include a waveguide core and a waverguide cladding. The EAM **224** modulates the light launched into the waveguide by the laser **222** in response to an applied voltage that varies in accordance with the data stream **220** being transmitted. Of course

this is but one modulation technique suitable for the present application. It can be appreciated that other modulation techniques may be used and still fall within the scope of the invention The modulated beam from the EAM **224** is multiplexed with other channels (e.g., λ**1**-λ**4**) with, for example, an array waveguide grating (AWG) **230**. The modulated channels are thereafter transmitted from the output of the AWG **230** over a network fiber **232**.

When configured to act as a receiver, a signal is received from the fiber **232** which may be multiplexed with other such channels. In this case the AWG **230** demultiplexes the channels, for example λ**1**, and sends it to the programmable block **210** designated for λ**1**. In the receive mode, the transmit switch **221** is deselected thus disabling the input port **212** as well as disabling the laser **222**. The receive switch **219** is selected thus allowing the demultiplexed signal to pass through the EAM **224** and the amplifier **218** to the output port **214** (Data Rx).

FIG. **3** shows a fiber network having programmable or "asymmetric" bandwidth allocation according to an embodiment of the invention. As shown, a plurality of programmable blocks or nodes **210** may be connected on either side of a fiber **232**. Depending on the polarity of the appropriate 'select' pins, the EAM **224** in each block **210** acts as a receiver or as a modulator. If Select is '1', for example, power may be supplied to the modulator driver amplifier **216** and the laser **222**, and the EAM **224** acts as a modulator. If Select is '0', power may be supplied to the receiver amplifier **218** and the EAM **224** acts as a receiver for detecting incoming signals. Traffic flow can be adjusted or programmed by changing the select polarities to change each channel from transmit mode to receive mode and vice-versa. Hence, network traffic with a tidal characteristic (i.e., right to left and then left to right) can be accommodated with the same channel with ease.

Ordinarily, there are many precision interfaces for optical alignment that should be carried out to manufacture optical transceiver modules. These alignments start with the entrance of the fiber to the package that are targeted to be aligned with sub-micron accuracy in six degrees of freedom, to the AWG which, along with the other components on the sub-mount have all been similarly aligned. This is very expensive and time-consuming.

One way to potentially reduce this alignment activity is to reduce the number of alignment procedures. Thus, by manufacturing multiple components in a monolithic manner, for example by manufacturing a number of modulators, equivalent to the desired number of channels as a single component, this reduces the optical alignment challenges considerably. A practical way to produce such monolithic components involves Indium Phosphide (InP) manufacturing techniques. Such techniques may be described by Ronald Kaiser et al., *Optoelectronic/Photonic Integrated Circuits on InP Between Technological Feasibility and Commercial Success,* IEICE Transactions of Electronics, Vol. E85-C, No. 4, April 2002. Due to inherent registration accuracies of the masking process associated with Indium Phosphide (InP) manufacturing, a multi-channel receiver, transmitter, or transceiver can be manufactured very economically.

Referring to FIG. **4**, there is shown a bi-directional "tidal" transceiver module according to an embodiment of the present invention. As shown, the module is compact and components are fabricated together as blocks such that the blocks can be aligned as one unit thus reducing the number of alignment steps. In particular, the module comprises a plurality of tuned laser diodes **400** positioned on a submount **402**. A plurality of Electro-Absorption Modulators (EAM) **404** are aligned in front of the lasers **400**, and a plurality of limiting amplifiers/modulator drivers (LIAs) **406** are aligned in back of the lasers **400**. Bond wires **410** connect the LIA **406** to the EAMs **404** to carry received signals from to EAMs **404** to the LIAs **406** when in receive mode. An array waveguide (AWG) **408** is aligned in front of the EAM **404** and multiplexes or demultiplexes the particular channels on to a fiber **410**. A ferrule **416** or other suitable connector may be used to connect the optical fiber **418**.

All of the components are encased in a housing **412** having external leads **414**. Ones of the leads **414** comprise the select switches **219** and **221** (FIG. **2**) for designating the direction of each channel. In a transmit mode, the LIA **406** acts as a modulator. In a receive mode, the LIA **406** acts as a receiver amplifier. The lasers **400**, the EAMs **404** and the LIAs **406** may be manufactured as single blocks, using for example Indium Phosphide technology. Where each block contains the number of particular components corresponding to the number of channels handled by the module. This greatly reduces the number of alignment steps required to assemble the module.

Embodiments of the present invention are specifically illustrated and/or described herein. However, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and within the purview of the appended claims without departing from the spirit and intended scope of the invention.

What is claimed is:

1. An optical network transceiver, comprising:

an input port to input a transmit data stream;

an output port to output a received data stream;

a laser to produce a transmit channel;

a modulator to modulate the transmit channel with the transmit data for transmission over a fiber in a transmit mode;

a receiver to receive an incoming channel in a receive mode, said transmit channel and said receive channel having a same wavelength; and

a select circuit to select between the transmit mode and the receive mode,

wherein an electro absorption modulator (EAM) includes both said modulator and said receiver, and

wherein said select circuit comprises a select switch on a limiting amplifier/modulator driver (LIA).

2. The optical network transceiver as recited in claim **1** wherein a plurality of said lasers are configured as a block and a plurality of said EAMs are configured as a block, and a plurality of said LIAs are configured as a block.

3. The optical network transceiver as recited in claim **2** wherein said blocks are fashioned in Indium Phosphide (InP).

4. An asymmetric optical network, comprising:

an optical fiber network having a first end and a second end;

at least one first transceiver module at said first end to operate at an assigned channel wavelength;

at least one second transceiver module at said second end to operate at a same said assigned channel wavelength;

switches in said first and said second transceiver modules to cause the channel wavelength to operate in either direction between said first end and said second end;

a plurality of said first transceiver modules at said first end each operating at an assigned wavelength; and

a plurality of said second transceiver modules at said second end, each operating at an assigned wavelength corresponding to one of said plurality of first transceiver modules,

wherein said switches comprise a select switch on a limiting amplifier/modulator driver (LIA) in each of said transceiver modules.

5. An asymmetric optical network as recited in claim **4**, further comprising:

a first array waveguide grating (AWG) between said optical fiber and said plurality of first transceiver modules; and

a second AWG between said optical fiber and said plurality of second transceiver modules.

6. An asymmetric optical network as recited in claim **5**, further comprising an electro absorption modulator (EAM) in each of said transceiver modules.

7. An asymmetric optical network as recited in claim **6** wherein said EAM comprises both a modulator and a receiver.

8. An asymmetric optical network, comprising:

an optical fiber network having a first end and a second end;

at least one first transceiver module at said first end to operate at an assigned channel wavelength;

at least one second transceiver module at said second end to operate at a same said assigned channel wavelength;

switches in said first and said second transceiver modules to cause the channel wavelength to operate in either direction between said first end and said second end;

a plurality of said first transceiver modules at said first end, each operating at an assigned wavelength; and

a plurality of said second transceiver modules at said second end, each operating at an assigned wavelength corresponding to one of said plurality of first transceiver modules,

wherein each of said transceiver modules comprise:

a laser to produce said assigned channel wavelength;

an electro absorption modulator (EAM) to modulate the assigned channel wavelength with data for transmission over a fiber in a transmit mode, and to receive an incoming channel in a receive mode; and

a limiting amplifier/modulator driver (LIA) comprising said switches.

9. An asymmetric optical network as recited in claim **8**, wherein a plurality of said lasers are configured as a block, and a plurality of said EAMs are configured as a block, and a plurality of said LIAs are configured as a block.

10. An asymmetric optical network as recited in claim **9** wherein said blocks are fashioned in Indium Phosphide (InP).

* * * * *

Submission XI

Type	Reference	Title
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Citations	**Not Known**	

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(72) Inventor(s):
Duncan Bremner
Fraser Murray Edwards

(73) Proprietor(s):
ITI Scotland Ltd
(Incorporated in the United Kingdom)
5th Floor, 191 West George Street,
GLASGOW, G2 2LB, United Kingdom

(74) Agent and/or Address for Service:
Haseltine Lake
Redcliff Quay, 120 Redcliff Street, Bristol,
BS1 6HU, United Kingdom

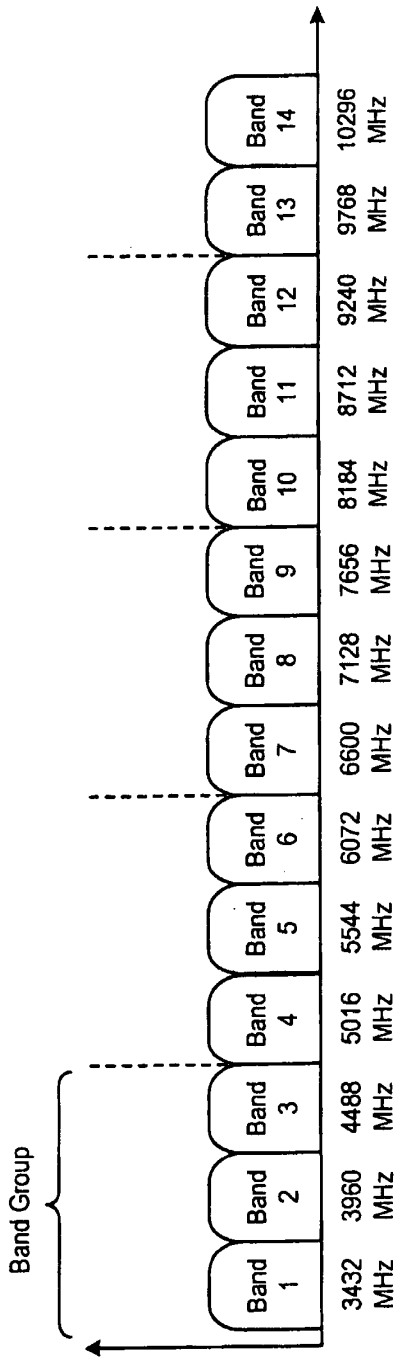
Band Group
Band 1
Band 2
Band 3
Band 4
Band 5
Band 6
Band 7
Band 8
Band 9
Band 10
Band 11
Band 12
Band 13
Band 14
3432 MHz
3960 MHz
4488 MHz
5016 MHz
5544 MHz
6072 MHz
6600 MHz
7128 MHz
7656 MHz
8184 MHz
8712 MHz
9240 MHz
9768 MHz
10296 MHz

Figure 1

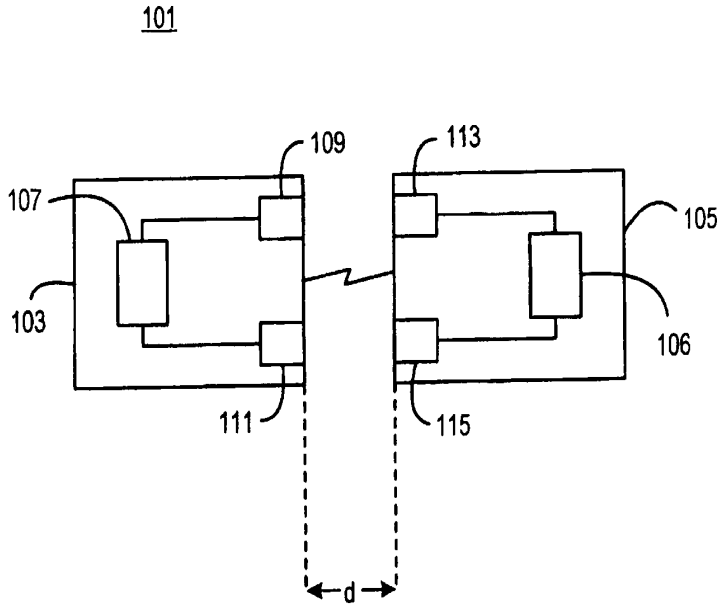

Figure 2

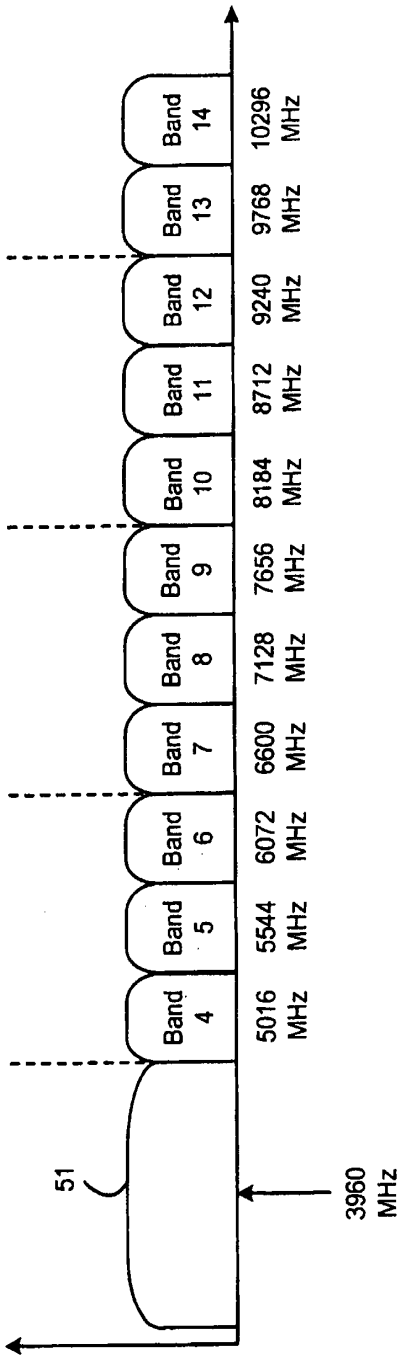
Band 4
Band 5
Band 6
Band 7
Band 8
Band 9
Band 10
Band 11
Band 12
Band 13
Band 14
5016 MHz
5544 MHz
6072 MHz
6600 MHz
7128 MHz
7656 MHz
8184 MHz
8712 MHz
9240 MHz
9768 MHz
10296 MHz
51
3960 MHz

Figure 3

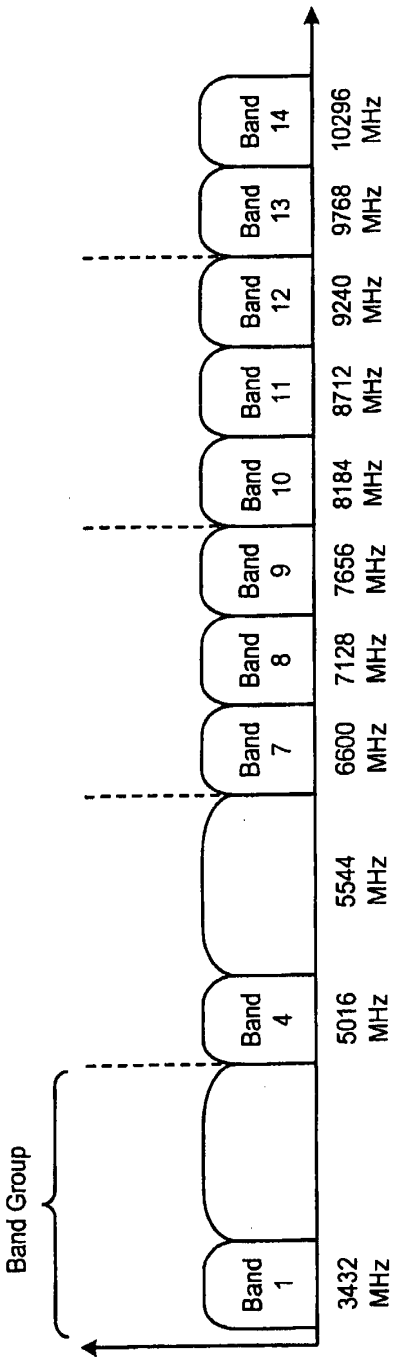
Band Group
Band 1
3432 MHz
Band 4
5016 MHz
5544 MHz
Band 7
6600 MHz
Band 8
7128 MHz
Band 9
7656 MHz
Band 10
8184 MHz
Band 11
8712 MHz
Band 12
9240 MHz
Band 13
9768 MHz
Band 14
10296 MHz

Figure 4

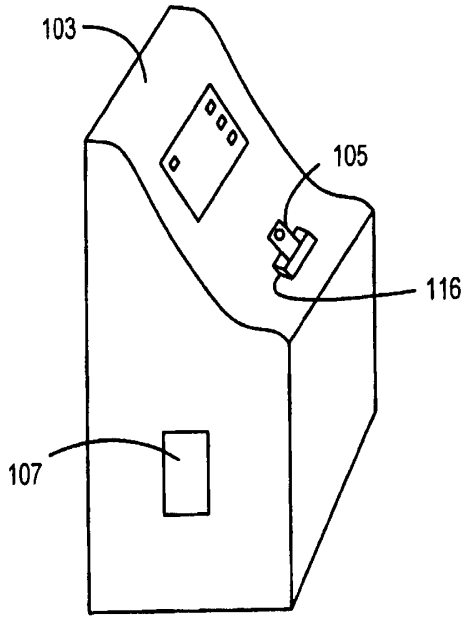

Figure 5

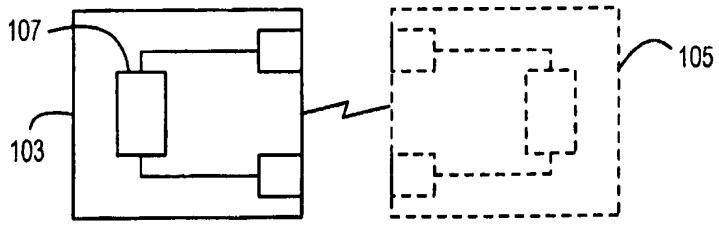

Figure 6a

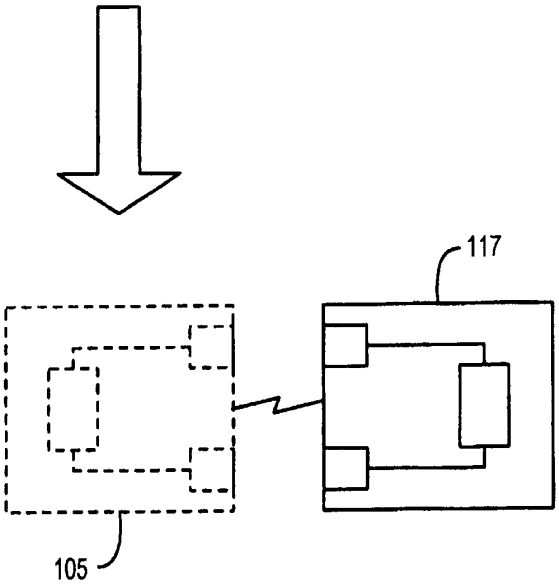

Figure 6b

Communication System and Method

Field of the invention

The invention relates to a communication system and method, and in particular to an ultra wideband (UWB) communication system and method for transferring a large amount of data, typically defined as greater than 1GB, at high speed between a first communication device, such as a host device, and a second communication device, such as a portable device, in a wireless manner.

Background of the invention

Ultra-wideband is a radio technology that transmits digital data across a very wide frequency range, 3.1 to 10.6 GHz. It makes use of ultra low transmission power, typically less than –41dBm/MHz, so that the technology can literally hide under other transmission frequencies such as existing Wi-Fi, GSM and Bluetooth. This means that ultra-wideband can co-exist with other radio frequency technologies. However, this has the limitation of limiting communication to distances of typically 5 to 20 metres.

Ultra-wideband uses very short impulses, often of the duration of nanoseconds (ns) or less, to modulate information across a very wide frequency spectrum (3.1-10.6 GHz is currently approved by Federal Communications Commission (FCC) in the United States). These pulses give rise to spectral components covering a very wide bandwidth in the frequency spectrum, hence the term ultra-wideband, whereby the bandwidth occupies more than 20 percent of the centre frequency, typically at least 500 MHz.

These properties of ultra-wideband, coupled with the very wide bandwidth, mean that UWB is an ideal technology for providing high speed wireless communication in the home or office environment, whereby the communicating devices are within a range of 20m of one another.

Figure 1 shows the arrangement of frequency bands in a Multi Band Orthogonal Frequency Division Multiplexing (MB-OFDM) system for ultra-wideband

communication. The MB-OFDM system comprises fourteen sub-bands of 528 MHz each, and uses frequency hopping every 312ns between sub-bands as an access method. Within each sub-band QPSK coding is employed to transmit data. It is noted that the sub-band around 5GHz, currently 5.1-5.8 GHz, is left blank to avoid interference with existing narrowband systems, for example 802.11a WLAN systems, security agency communication systems, or the aviation industry.

The fourteen sub-bands are organised into four band groups, each having three 528MHz sub-bands, and one band group having two 528MHz sub-bands. As shown in Figure 1, the first band group comprises sub-band 1, sub-band 2 and sub-band 3. An example UWB system will employ frequency hopping between sub-bands of a band group, such that a first data symbol is transmitted in a first 312.5 ns duration time interval in a first frequency sub-band of a band group, a second data symbol is transmitted in a second 312.5 ns duration time interval in a second frequency sub-band of a band group, and a third data symbol is transmitted in a third 312.5 ns duration time interval in a third frequency sub-band of the band group. Therefore, during each time interval a data symbol is transmitted in a respective sub-band having a bandwidth of 528MHz, for example sub-band 2 having a 528 MHz baseband signal centred at 3960MHz.

The technical properties of ultra-wideband mean that it is being deployed for applications in the field of data communications. For example, a wide variety of applications exist that focus on cable replacement in the following environments:

- communication between PCs and peripherals, i.e. external devices such as hard disc drives, CD writers, printers, scanner, etc.
- home entertainment, such as televisions and devices that connect by wireless means, wireless speakers, etc.
- communication between handheld devices and PCs, for example mobile phones and PDAs, digital cameras and MP3 players, etc

Despite ultra-wideband having a large bandwidth that is capable of transmitting large amounts of data in a relatively short time, the ever increasing size of data downloads means that many applications will still experience problems or delays when copying

large amounts of data between devices. For example, the transfer of video or music data between a first device (such as a wireless jukebox) and a second device (such as a personal computer) is sufficiently fast to enable video or music to be experienced wirelessly in real time. However, the transfer speed is less than acceptable for transferring a complete movie file between the first and second devices, which typically comprises transferring 10 to 40GB of data.

It is known to increase the data rate by transmitting data symbols concurrently in a plurality of sub-bands. In other words, the data is encoded, interleaved and divided into two or more parallel bit streams for transmission concurrently in two or more of the sub-bands. However, such a system suffers from the disadvantage of requiring a plurality of transmitters and antennas, one for each of the concurrent sub-bands being used. The receiver also requires a plurality of antennas for receiving the concurrent information. Therefore, the cost of both the transmitting and receiving devices is increased due to duplication of antenna and radio stages.

The aim of the present invention is to provide an improved ultra-wideband communication system and method that is capable of transmitting bulk data over a short time period.

Summary of the invention

According to a first aspect of the invention, there is provided a communication device which in use transmits a data file to a portable device over a wireless ultra-wideband communication system using multi-band orthogonal frequency division multiplexing, the multi-band orthogonal frequency division multiplexing organised as a plurality of frequency sub-bands. The communication device comprises means for concatenating two or more frequency sub-bands during a data transfer operation, and means for transmitting data via the two or more concatenated frequency bands to the portable device. The communication device also comprises means for enabling the portable device to be located in a predetermined positional relationship with respect to the communication device during a data transfer operation.

The concatenation of frequency sub-bands and the predetermined positional relationship between the two devices provides the advantage of enabling large volumes of data to be transmitted in a very short period of time.

According to a further aspect of the invention, there is provided a method of transmitting a data file between a communication device and a portable device in a wireless ultra-wideband communication system using multi-band orthogonal frequency division multiplexing, the multi-band orthogonal frequency division multiplexing system organised into a plurality of frequency sub-bands. The method comprises the steps of concatenating two or more frequency bands, and transmitting data via the two or more concatenated frequency bands to the portable device. The method also comprises the step of positioning the portable device in a predetermined positional relationship to the communication device during the data transfer operation.

According to a further aspect of the invention, there is provided a portable device adapted for use with a communication device as defined in the appended claims. The portable device comprises a receiver for receiving a signal comprising two or more concatenated frequency sub-bands, and processing means for processing the concatenated sub-bands.

Brief description of the drawings

For a better understanding of the present invention, and to show more clearly how it may be carried into effect, reference will now be made, by way of example only, to the following drawings in which:

Figure 1 shows the multi-band OFDM alliance (MBOA) approved frequency spectrum of a MB-OFDM system;

Figure 2 shows an ultra-wideband communication system according to the present invention;

Figure 3 shows the MBOA frequency spectrum of a MB-OFDM system when used in accordance with a first embodiment of the present invention;

Figure 4 shows the MBOA frequency spectrum of a MB-OFDM system when used in accordance with a second embodiment of the present invention;

Figure 5 shows an ultra-wideband communication system according to another aspect of the present invention;

Figure 6 shows a typical application of an ultra-wideband communication system according to the present invention.

Detailed description of a preferred embodiment of the present invention

Figure 2 shows a schematic view of an ultra-wideband communication system 101 according to the present invention. The ultra-wideband communication system 101 comprises a first communication device 103, such as a host device or server, which communicates with a second device 105, such as a portable device. It is noted that the second device 105 can be a "dumb" storage device such as a hard disc, or an "intelligent" device such a media player, mobile phone, or video playing device.

The first communication device 103 comprises a memory 107 for storing data that is to be downloaded to the second device 105. For example, the memory 107 can be adapted to store a catalogue or collection of movie films, audio tracks, photographic images, MP3 files, and so on. The first device 103 includes an ultra-wideband transmitter 109 for transmitting data over an air interface. Optionally, the first device 103 includes an ultra-wideband receiver 111 for receiving data from the second device 105, for example if data is to be uploaded from the second device 105 to the first device 103.

The second device 105 includes an ultra-wideband receiver 113 for receiving data received over the air interface from the first device 103, and a memory 106 for storing the received data. Optionally, the second device 105 includes an ultra-wideband transmitter 115 for transmitting data to the first device 103, for example if data is to be uploaded from the memory 106 of the second device 105 to the first device 103.

According to the invention, the effective data transfer rate between the first communication device 103 and the second device 105 is increased as follows.

Firstly, the transmitter 109 in the first device 103 is configured to concatenate two or more sub-bands during a data transfer operation. For example, as shown in Figure 3, the transmitter 109 in the first communication device 103 can be configured to concatenate sub-band 1, sub-band 2 and sub-band 3 from the first band group, such that a 1584MHz base band signal 51 centred at 3960 MHz is employed for transmitting data. In this manner the data rate can be increased depending on the number of sub-bands that are concatenated. This has the effect of securing a plurality of UWB sub-bands in the immediate vicinity, thus enabling the UWB device of the present invention to secure increased bandwidth for enabling the data throughput to be increased.

Secondly, the first communication device 103 comprises means for enabling the second device 105 to be located in a predetermined positional relationship with respect to the first communication device 103 during a data transfer operation.

In this manner the first communication device 103 and the second device 105 are disposed in close proximity to one another during the data transfer operation, such that the range of the UWB transmission is reduced significantly to a distance "d". In addition, the predetermined positional relationship between the first communication device 103 and the second device 105 enables one or more transmission parameters to be adapted, for example, the data rate to be increased. In addition, the fact that the air interface between the first communication device 103 and the second device 105 is known means that certain communication protocols can be simplified or omitted. For example, channel estimation procedures become simplified because the first communication device 103 will know (or learn to know) the channel characteristics between itself and the second device 105, due to the fact that the second device 105 is located in the predetermined positional relationship. The predetermined positional relationship can also lead to a reduction in error rate, which also contributes to an increase in the effective data rate.

The close proximity of the first communication device 103 and the second device 105, coupled with the concatenation of multiple UWB sub-bands, enables the data throughput to be increased significantly. By "close proximity" it is meant that the

distance "d" is less than 100cm, and preferably less than 30cm, or even touching (without electrical connection).

Thus, according to the invention the first communication device 103 widens the functional bandwidth by concatenating two or more frequency sub-bands. For example, as discussed above the invention can concatenate sub-band 1, sub-band 2 and sub-band 3, which are adjacent frequency sub-bands within a band group of the multi-band orthogonal frequency division multiplexing system. Alternatively, the invention can concatenate sub-bands from adjacent band groups, for example sub-band 2, sub-band 3 and sub-band 4.

Referring to Figure 4, the invention can also make use of band stop or notch filters to concatenate frequency sub-bands from two or more sub-bands that are non-adjacent. For example, the invention can be used to concatenate frequency sub-band 2, sub-band 3, sub-band 5 and sub-band 6. The concatenation of sub-bands can also take place between non-adjacent band groups.

It will be appreciated therefore that, rather than the transmitter 109 securing one UWB sub-band for communicating with a second device in the conventional manner, the invention adapts the operation of the transmitter 109 such that it appears that multiple transmitting devices are communicating in parallel. Normally, this would have a degrading impact on other UWB devices operating in the vicinity, because the multiple sub-bands would be employed by the same transmitting device. However, because the UWB transmission is performed over a very small distance (less than 100cm), or even touching without electrical contact, the first and second devices are able to temporarily fully occupy a plurality of UWB bands in the vicinity, without having a degrading effect on the ability of other devices to use the UWB space. Preferably, the first and second devices temporarily fully occupy most, if not all, of the available UWB bands, adjacent within a band group or channel.

As mentioned above, although the preferred embodiment is adapted to concatenate one or more adjacent sub-bands from within the same band group or channel (for example sub-bands 1 to 3 in the first band group), the invention may also be extended to concatenating UWB bands from more than one band group. Also, although the

preferred embodiment discloses that three sub-bands are concatenated, it will be appreciated that any number of sub-bands can be concatenated, including all fourteen sub-bands.

Preferably, to ease integration with existing systems, the concatenated bands are adjacent to one another since the receiver 113 in the second device 105 will be tuned to search for the 1584 MHz spread with time interleaving frequency hopping (time-frequency codes) of existing hardware specifications. However, rather than processing a 528MHz wide signal as carried out in a conventional receiver, the second device 105 is configured to process a 1584MHz wide signal.

As mentioned above, the data transfer takes place while the first communication device 103 and the second device 105 are located in a predetermined positional relationship with one another, and preferably in contact with each other (without electrical connection). The use of multiple UWB bands and the reduction in the transmission distance enable a large data file, for example a 10GB data file relating to a movie, to be transmitted between the first and second devices in less than 1 minute.

According to a further aspect of the invention, the first device 103 is adapted to concatenate two or more sub-bands after the first device has determined how many frequency sub-bands are available for transmission in the area concerned.

The second device 105 is adapted to receive the concatenated sub-bands, and to decode the data from the wider bandwidth baseband signal, for playback or storage in the second device 105. Preferably, the second device is switchable between a first mode of operation in which the receiver is adapted to receive and process a 528MHz wide signal in a conventional manner, and a second mode of operation in which the receiver is adapted to receive and process a 1584MHz wide signal in an enhanced data rate mode.

It is noted that the memory 107 for storing data can either form part of the first communication device 103, or be located at a remote connection, for example a central server device. Alternatively, the memory 107 may be split between the first communication device 103 and a separate remote location. For example, a memory

107 within the first communication device 103 could be used to store data that is frequently required (such as the latest popular movies), and the remote memory used to store data that is required less frequently (such as a back catalogue of old movies). Preferably, with this split-storage embodiment the data link between the memory in the first device and the memory in the remote location is very fast, for example a single or plurality of fast copper or fibre channels, such that the data transfer speeds for files stored in the remote location is not too slow.

Figure 5 shows a further aspect of the invention, in which the first communication device 103 comprises a cradle 116 for supporting the second device 105 during the data transfer process. The first communication device 103 is shown as a kiosk, such as an automatic teller machine (ATM) or a petrol pump, for transferring data to the second device 105, such as a portable media player or a portable storage device. As with Figure 2, the first device 103 comprises a memory device 107 for storing data that is to be downloaded to the second device 105.

According to this embodiment, the cradle 116 acts to support the second device 105 during the data transfer process, and for ensuring that the first and second devices are located in a predetermined positional relationship with one another during the data transfer process. For example, the cradle can be configured to position the first and second devices so that they are less than a predetermined distance apart, for example less than 30cm apart. Alternatively, the cradle can be configured such that the first and second devices are in physical, but not electrical, contact with one another during the data transfer operation.

This defined proximity permits automatic power control over the wireless interface. For example, the power may be reduced whilst maintaining channel throughput, ultimately enabling a higher density of kiosk installations. In addition, the predetermined positional relationship results in fewer data error correction operations being performed, hence contributing to the increased data transfer rate between the first and second devices.

Although Figure 5 has been shown as an ATM type machine, it is noted that the cradle 116 could form part of any desktop device (for example part of a computer, DVD

player, television or the like), or an independent cradle that is remotely connected to such a device. According to the latter, the cradle houses the transmitter and/or receiver circuitry, and is permanently connected by wire or fibre, or other data channel, to a host device, and accepts the portable device during a data transfer operation.

According to another embodiment, the first communication device 103 can comprise a simple support, for example a pad, for receiving a portable device placed by a user during a data transfer operation. In such an arrangement the support is arranged substantially horizontal, such that the user can simply place the portable device on the support during the data transfer operation. Alternatively, the support can be positioned in some other configuration, such as vertically or sloped, such that the portable device is held by a user against the support during a data transfer operation.

According to yet another embodiment, the first communication device comprises a receptacle or slot into which the portable device slides (without electrical contact).

Figures 6a and 6b show a typical application of the present invention. In Figure 6a a first device 103 stores a catalogue of media files in its memory device 107. The first device 103 could be a kiosk vending machine or ATM type machine located in a convenient public place, such as a shopping mall or a fuel pump at a garage forecourt. A user places a portable device 105 in close proximity to the host device 103 in order to select and download a media file, for example a movie. Once the media file has been saved in the memory 106 of the portable device 105, the media can either be played on that device, or transferred to another device, as shown in Figure 6b. Figure 6b shows how the media file stored in the memory 106 of the portable device 105 can be uploaded to another device 117, such as a DVD player, PC, television, etc.

As can be seen from the above, the invention enables a user to carry a personal media player having a high-speed UWB chipset integrated, which is capable of playing a variety of media types e.g. music and video streams. The user can download data, including a large video data file, without spending a large amount of time at the vending machine. The portable device is then able to play the media in a portable mode, or even use UWB functionality to stream the high-definition sound or video content onto an UWB enabled television or plasma screen, in what is termed a "docked"

configuration. It will be appreciated that in the latter, the portable media player and the UWB enabled television or plasma screen must be in close proximity during the data transfer, if data transfer speed is a priority. If not, for example because the video data is merely being watched on the television or plasma screen, then the portable media player could be configured to transfer data to the other device 117 in a conventional or enhanced data-throughput mode, UWB manner, over greater distances.

The invention is particularly suited for a number of applications where high-speed, short time-span data burst communication is desired. For example, if used in the DVD/ music rental business, the shop floor could be cleared of bulky DVD media and cases, and even of counter staff. The invention enables DVD/music rental to be conducted in an un-manned environment, such as a system that is more like an ATM cashpoint system. In other words, a user would be able to walk-in and choose music or film media from one the ATM-style jukeboxes and download their selections in a short space of time to their portable media device. High speed bulk data transfer is important in such an application, since a user does not wish to spend a disproportionate amount of time at the source machine. The invention enables a typical movie to be downloaded in the time a user would normally spend at an existing ATM cash dispenser, which would be acceptable to a user.

Another envisaged application is a "pod-cast" type application, whereby customers could access a Wi-Fi type ultra-wideband hotspot before boarding a train or airplane, enabling them to make selections of media (music, film, or even radio broadcasts) to last the duration of travel.

It is noted that, although the preferred embodiment has been described in relation to the first device being typically a host or server device, it will be appreciated that the first device could also be a portable or hand-held device. In such an arrangement, the invention can be used to transfer data at high speeds between two portable or storage devices.

Also, although the means for positioning the first device and the second device in a fixed positional relationship during a data transfer operation has been described in the preferred embodiment as comprising a cradle for receiving the second device, the

positioning means could also comprise a surface for supporting the second device in a fixed relationship to the first device. The surface could either be a surface on which a user places the portable device during a data transfer operation, or a surface which the user holds the portable device against during the data transfer operation.

Furthermore, although the preferred embodiments have been described in relation to the MB-OFDM technique, it will be appreciated that the invention is equally applicable to other ultra-wideband techniques.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim, "a" or "an" does not exclude a plurality, and a single processor or other unit may fulfil the functions of several units recited in the claims. Any reference signs in the claims shall not be construed so as to limit their scope.

CLAIMS

1. A communication device which in use transmits a data file to a portable device over a wireless ultra-wideband communication system using multi-band orthogonal frequency division multiplexing, the multi-band orthogonal frequency division multiplexing organised as a plurality of frequency sub-bands, the communication device comprising:

means for concatenating two or more frequency sub-bands during a data transfer operation,

means for transmitting data via the two or more concatenated frequency bands to the portable device; and

means for enabling the portable device to be located in a predetermined positional relationship with respect to the communication device during a data transfer operation.

2. A communication device as claimed in claim 1, wherein the means for enabling is configured to position the portable device within a distance of less than 100cm to the communication device during the data transfer operation.

3. A communication device as claimed in claim 1, wherein the means for enabling is configured to position the portable device within a distance of less than 30cm to the communication device during the data transfer operation.

4. A communication device as claimed in any one of claims 1 to 3, wherein the means for enabling is configured to place the portable device in contact with, but not electrically connected to, the communication device during the data transfer operation.

5. A communication device as claimed in any one of claims 1 to 4, wherein the means for enabling comprises means for retaining the portable device in the fixed positional relationship during a data transfer operation.

6. A communication device as claimed in any one of claims 1 to 4, wherein the means for enabling comprises a cradle for receiving the portable device during a data transfer operation.

7. A communication device as claimed in any one of claims 1 to 4, wherein the means for enabling comprises a surface for receiving the portable device during a data transfer operation.

8. A communication device as claimed in claim 7, wherein the surface is configured to be substantially horizontal such that, during use, the surface receives a portable device placed by a user during a data transfer operation.

9. A communication device as claimed in claim 7, wherein the surface is configured to be vertical or sloped such that, during use, a portable device can be held by a user against or near the surface during a data transfer operation.

10. A communication device as claimed in any one of claims 1 to 4, wherein the means for enabling comprises a receptacle or slot into which the portable device slides without electrical connection.

11. A communication device as claimed in any one of the preceding claims, wherein the means for concatenating is adapted to concatenate two or more adjacent frequency sub-bands during a data transfer operation.

12. A communication device as claimed in claim 11, wherein the means for concatenating is adapted to concatenate two or more adjacent frequency sub-bands from within the same band group of the multi-band orthogonal frequency division multiplexing system during a data transfer operation.

13. A communication device as claimed in any one of the preceding claims, further comprising means for adapting one or more transmission parameters based on the known positional relationship between the communication device and the second device.

14. A communication device as claimed in any one of the preceding claims, wherein the communication device is a server device.

15. A method of transmitting a data file between a communication device and a portable device in a wireless ultra-wideband communication system using multi-band orthogonal frequency division multiplexing, the multi-band orthogonal frequency division multiplexing system organised into a plurality of frequency sub-bands, the method comprising the steps of:

concatenating two or more frequency bands;

transmitting data via the two or more concatenated frequency bands to the portable device; and

positioning the portable device in a predetermined positional relationship to the communication device during the data transfer operation.

16. A method as claimed in claim 15, wherein the step of positioning comprises positioning the portable device within a distance of less than 100cm to the communication device during the data transfer operation.

17. A method as claimed in claim 15 wherein the step of positioning comprises positioning the portable device within a distance of less than 30cm to the communication device during the data transfer operation.

18. A method as claimed in any one of claims 15 or 17, wherein the step of positioning comprises placing the portable device in contact with, but not electrically connected to, the communication device during the data transfer operation.

19. A method as claimed in any one of claims 15 to 18, wherein the step of positioning comprises providing means for retaining the portable device in the fixed positional relationship during a data transfer operation.

20. A method as claimed in any one of claims 15 to 18, wherein the step of positioning comprises providing a cradle for receiving the portable device during a data transfer operation.

21. A method as claimed in any one of claims 15 to 18, wherein the step of positioning comprises providing a support surface for receiving the portable device during a data transfer operation.

22. A method as claimed in claim 21 wherein, during use, the portable device is placed by a user on the support surface during the data transfer operation.

23. A method as claimed in claim 21 wherein, during use, the portable device is held against or near the support surface by a user during a data transfer operation.

24. A method as claimed in any one of claims 15 to 18, wherein the step of positioning comprises providing a receptacle or slot into which the portable device slides without electrical contact during a data transfer operation.

25. A method as claimed in any one of claims 15 to 24, wherein the step of concatenating comprises the step of concatenating two or more adjacent frequency sub-bands during a data transfer operation.

26. A method as claimed in claim 25, wherein the step of concatenating comprises the step of concatenating two or more adjacent frequency sub-bands from within the same band group of the multi-band orthogonal frequency division multiplexing system during a data transfer operation.

27. A method as claimed in any one of claims 15 to 26, wherein the communication device is a server device.

28. A portable device adapted for use with a communication device as defined in any one of claims 1 to 14, the portable device comprising:

a receiver for receiving a signal comprising two or more concatenated frequency sub-bands; and

processing means for processing the concatenated sub-bands.

29. A portable device as claimed in claim 28, wherein the receiver is switchable between a first mode of operation in which the receiver is adapted to receive and

Submission XII

Type	Reference	Title
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Citations	**Not Known**	

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(72) Inventor(s):
Dean Kemp
Duncan Bremner
Mark Norris

(73) Proprietor(s):
ITI Scotland Ltd
(Incorporated in the United Kingdom)
5th Floor, 191 West George Street, GLASGOW, G2 2LB, United Kingdom

(74) Agent and/or Address for Service:
Haseltine Lake LLP
Redcliff Quay, 120 Redcliff Street, BRISTOL, BS1 6HU, United Kingdom

Band Group
Band 1
Band 2
Band 3
Band 4
Band 5
Band 6
Band 7
Band 8
Band 9
Band 10
Band 11
Band 12
Band 13
Band 14
3432 MHz
3960 MHz
4488 MHz
5016 MHz
5544 MHz
6072 MHz
6600 MHz
7128 MHz
7656 MHz
8184 MHz
8712 MHz
9240 MHz
9768 MHz
10296 MHz

Figure 1

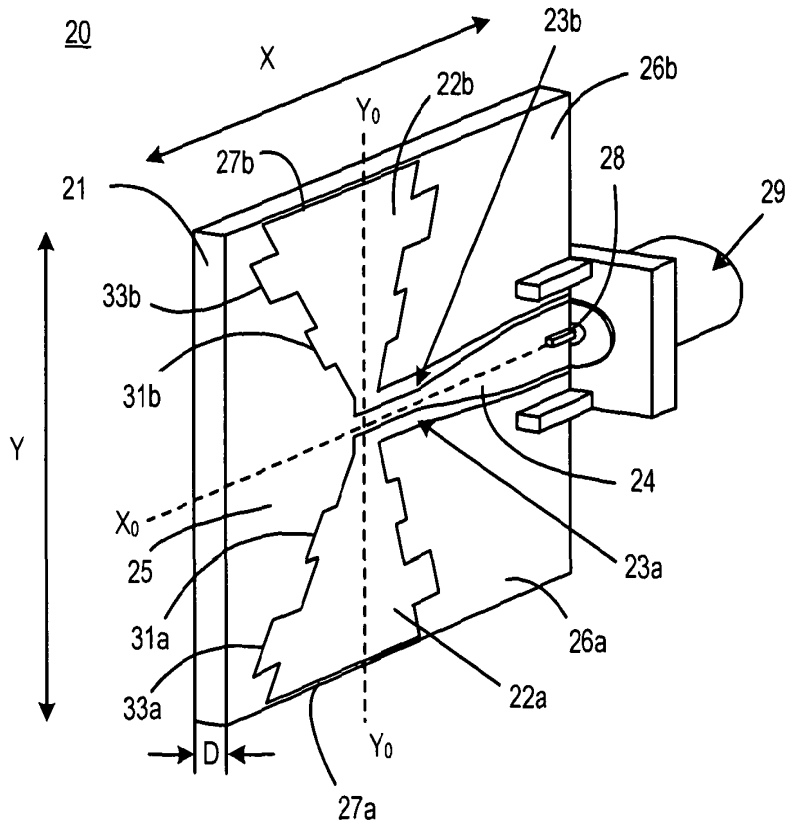
20
X
23b
26b
22b
Y_0
27b
28
29
21
33b
31b
Y
24
X_0
25
23a
31a
26a
33a
22a
D
Y_0
27a

Figure 2

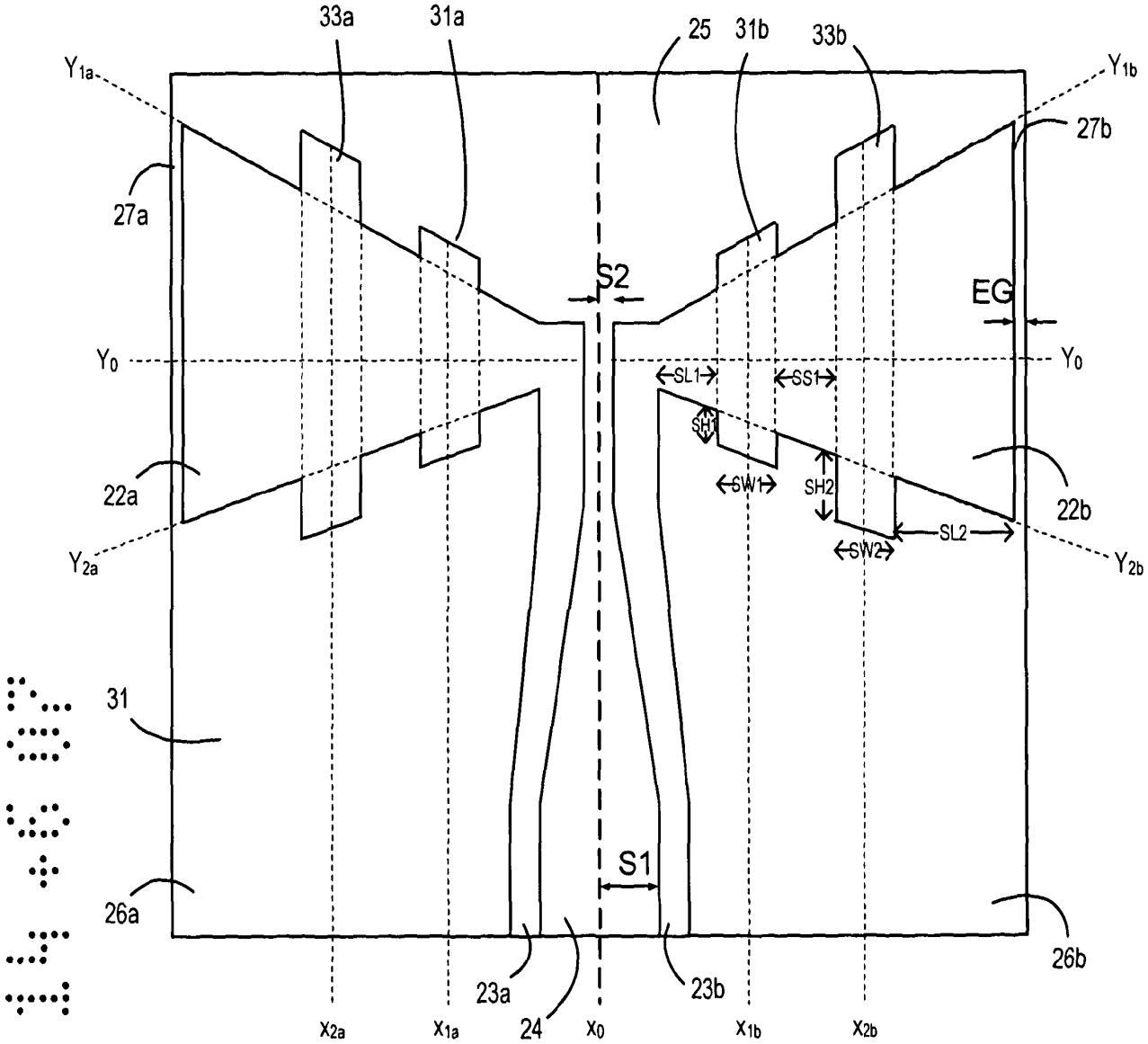
33a
31a
25
31b
33b
Y1a
Y1b
27b
27a
S2
EG
Y0
Y0
SL1
SS1
SH1
SW1
SH2
22a
22b
SL2
SW2
Y2a
Y2b
31
S1
26a
26b
23a
24
23b
X2a
X1a
X0
X1b
X2b

Figure 3

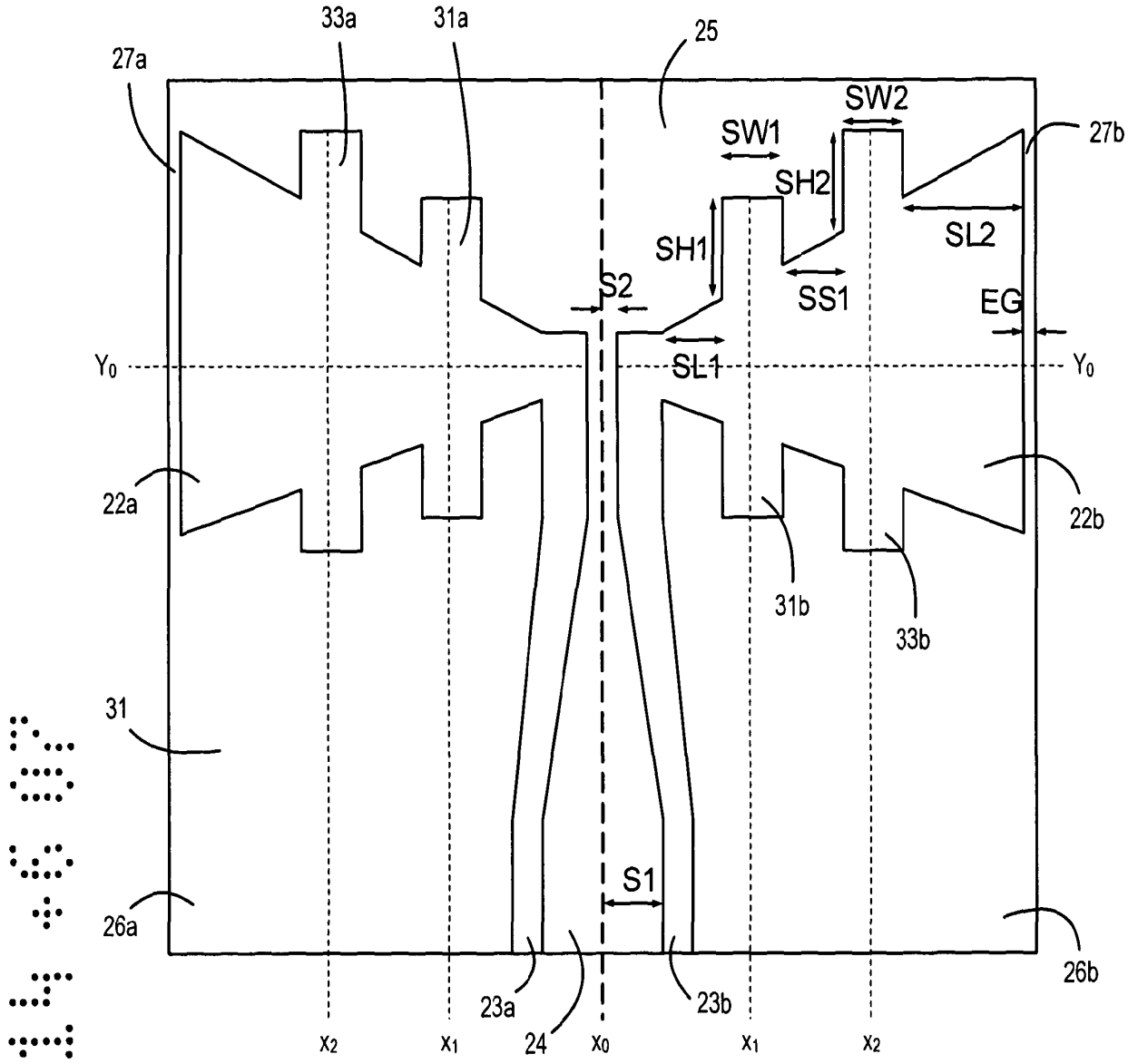
33a
31a
25
27a
SW2
SW1
27b
SH2
SH1
SL2
S2
SS1
EG
Y0
SL1
Y0
22a
22b
31b
33b
31
S1
26a
26b
23a
23b
24
x2
x1
x0
x1
x2

Figure 4

ULTRA WIDEBAND ANTENNA

Field of the invention

The invention relates to an ultra wideband antenna, and in particular to a low cost ultra wideband antenna suitable for use in portable devices.

Background of the invention

Ultra-wideband is a radio technology that transmits digital data across a very wide frequency range, 3.1 to 10.6 GHz. It makes use of ultra low transmission power, typically less than –41 dBm/MHz, so that the technology can literally hide under other transmission frequencies such as existing Wi-Fi, GSM and Bluetooth. This means that ultra-wideband can co-exist with other radio frequency technologies. However, this has the limitation of confining communication to distances of typically 5 to 20 metres.

There are two approaches to UWB: the time-domain approach, which constructs a signal from pulse waveforms with UWB properties, and a frequency-domain modulation approach using conventional FFT-based Orthogonal Frequency Division Multiplexing (OFDM) over Multiple (frequency) Bands, giving MB-OFDM. Both UWB approaches give rise to spectral components covering a very wide bandwidth in the frequency spectrum, hence the term ultra-wideband, whereby the bandwidth occupies more than 20 per cent of the centre frequency, typically at least 500MHz.

These properties of ultra-wideband, coupled with the very wide bandwidth, mean that UWB is an ideal technology for providing high-speed wireless communication in the home or office environment, whereby the communicating devices are within a range of 20m of one another.

Figure 1 shows the arrangement of frequency bands in a multi-band orthogonal frequency division multiplexing (MB-OFDM) system for ultra-wideband communication. The MB-OFDM system comprises fourteen sub-bands of 528 MHz each, and uses frequency hopping every 312 ns between sub-bands as an access method. Within

each sub-band OFDM and QPSK or DCM coding is employed to transmit data. It is noted that the sub-band around 5 GHz, currently 5.1–5.8 GHz, is left blank to avoid interference with existing narrowband systems, for example 802.11a WLAN systems, security agency communication systems, or the aviation industry.

The fourteen sub-bands are organized into five band groups: four having three 528 MHz sub-bands, and one having two 528 MHz sub-bands. As shown in Figure 1, the first band group comprises sub-band 1, sub-band 2 and sub-band 3. An example UWB system will employ frequency hopping between sub-bands of a band group, such that a first data symbol is transmitted in a first 312.5 ns duration time interval in a first frequency sub-band of a band group, a second data symbol is transmitted in a second 312.5 ns duration time interval in a second frequency sub-band of a band group, and a third data symbol is transmitted in a third 312.5 ns duration time interval in a third frequency sub-band of the band group. Therefore, during each time interval a data symbol is transmitted in a respective sub-band having a bandwidth of 528 MHz, for example sub-band 2 having a 528 MHz baseband signal centred at 3960 MHz.

The technical properties of ultra-wideband mean that it is being deployed for applications in the field of data communications. For example, a wide variety of applications exist that focus on cable replacement in the following environments:

- communication between PCs and peripherals, i.e. external devices such as hard disc drives, CD writers, printers, scanner, etc.
- home entertainment, such as televisions and devices that connect by wireless means, wireless speakers, etc.
- communication between handheld devices and PCs, for example mobile phones and PDAs, digital cameras and MP3 players, etc.

The large bandwidths and large data rates associated with such applications require an antenna which has excellent characteristics over the whole ultra wideband range. As a result, many ultra wideband systems adopt complex antenna solutions, such as smart antennas or antenna arrays.

However, antennas of this type are not suited for use in small portable devices, since the smart antennas or antenna arrays tend to be relatively large and expensive.

What is needed is an antenna design that can operate consistently across all current legislated band frequencies, having a small footprint, suitable for mass production, and also having a low-cost.

Summary of the invention

According to a first aspect of the invention there is provided an ultra wideband antenna comprising a substrate; a metal layer deposited on the substrate; wherein the metal layer comprises first and second non-metallic regions defined therein, the first and second non-metallic regions being arranged on either side of a longitudinal axis, the longitudinal axis corresponding to a feed axis of the antenna, the first and second non-metallic regions tapering towards the longitudinal axis to form a bowtie pattern; wherein each of the first and second non-metallic regions comprises at least one tuning slot, the at least one tuning slot being arranged about a respective first axis, the first axis being parallel to the longitudinal axis; and wherein the at least one tuning slot extends along its respective axis to form a non-metallic area outside the non-metallic area defined by the respective first or second non-metallic region.

According to another aspect of the invention, there is provided an ultra wideband antenna comprising a metal layer; wherein the metal layer comprises first and second non-metallic regions defined therein, the first and second non-metallic regions being arranged on either side of a longitudinal axis, the longitudinal axis corresponding to a feed axis of the antenna, the first and second non-metallic regions tapering towards the longitudinal axis to form a bowtie pattern; wherein each of the first and second non-metallic regions comprises at least one tuning slot, the at least one tuning slot being arranged about a respective first axis, the first axis being parallel to the longitudinal axis; and wherein the at least one tuning slot extends along its respective axis to form a non-metallic area outside the non-metallic area defined by the respective first or second non-metallic region.

The antenna according to the invention has the advantage of being able to transmit and receive frequencies over at least the entire UWB frequency range, i.e. at least

between 3.1 to 10.6 GHz. Furthermore, the antenna structure has a compact footprint for integration into consumer equipment.

Preferably the antenna substrate is made from FR4 PCB material. This has the advantage of being low cost, and compatible with major PCB processes and techniques.

Brief Description of the drawings

For a better understanding of the present invention, and to show more clearly how it may be carried into effect, reference will now be made, by way of example only, to the following drawings in which:

Figure 1 shows the arrangement of frequency bands in a multi-band orthogonal frequency division multiplexing (MB-OFDM) system for ultra-wideband communication.

Figure 2 shows a perspective view of an antenna according to an embodiment of the present invention;

Figure 3 shows a plan view of the antenna shown in Figure 2; and

Figure 4 shows a plan view of an antenna according to another embodiment of the present invention.

Detailed description of preferred embodiments of the present invention

Figure 2 shows an antenna 20 according to an embodiment of the present invention. The antenna 20 is a planar antenna formed on a substrate 21. The antenna 20 has a footprint of about 30mm in the "X" direction by about 31mm in the "Y". It will be appreciated that these dimensions, including other dimensions described within the remainder of this application, are provided as examples only, and that the invention is equally applicable to antenna arrangements having different dimensions. The dimensions and tolerances are provided as examples associated with low cost fabrication techniques, yet providing an antenna structure that has robust wideband performance compatible with such mass production techniques.

The substrate 21 is made from a suitable material, for example a PCB material such as FR4. FR4 substrate material has the advantage of being low cost and easy to manufacture. FR4 is a woven glass reinforced epoxy resin laminate and is the usual base material for PCB laminates. FR4 laminate displays a reasonable compromise between mechanical, electrical and thermal properties. The dimensional stability is influenced by construction and resin content. The dielectric constant, typically in the range 4.4 to 5.2, depends on the glass-resin ratio. This value decreases with increasing resin content and increasing frequency. As such, the use of FR4 as an antenna substrate is normally restricted to frequencies in the lower microwave band since dielectric losses usually make FR4 unsuitable for higher frequencies, which

means that other substrate materials are usually used for such applications. However, as will be described hereinafter, the antenna structure and design according to the present invention means that the antenna 20 is suitable for use in the ultra wideband frequency range using a substrate 21 made from FR4 material.

The substrate 21 has a single sided coating of a metal conductor, for example a 1 oz coating of copper. The substrate 21 shown in Figure 2 has a thickness D of about 1.6mm, although it will be appreciated that other thicknesses may also be used, as may other conductive materials such as gold or aluminium. It will be appreciated that the thickness of the substrate will affect the return loss across the frequency band. The structure of the embodiment of Figure 2 is therefore described in relation to the tolerances required for compatibility with commercial off-the-shelf materials such as FR4, and as such the tolerances and dimension may vary when the invention is applied to an antenna using a substrate made from a different material.

The antenna structure is formed by creating non-metallic regions in the metal coating on the surface of the substrate. In particular, the metal coating on the substrate 21 is processed to provide first and second non-metallic regions 22a and 22b, the first and second non-metallic regions 22a and 22b having corresponding first and second non-metallic channels 23a and 23b connecting the first and second non-metallic regions to the edge of the substrate that is nearest the antenna feed.

In the embodiment of Figure 2 the first and second non-metallic regions 22a and 22b are generally triangular in shape with their apexes facing each other, and together with the first and second non-metallic channels 23a, 23b define an antenna structure having a bowtie shaped tuning slot. It will be appreciated by a person skilled in the art that the triangular shaped first and second non-metallic regions 22a, 22b may be replaced by non-metallic regions having other shapes that taper towards an apex, for example a curved shaped profile in place of the triangular one shown in the Figures.

The first and second non-metallic regions 22a, 22b and/or the first and second non-metallic channels 23a, 23b are preferably symmetrical about an axis X_0 (referred to hereinafter as the "vertical axis" or "longitudinal axis" corresponding to a feed axis of the antenna).

As can be seen from Figure 2, each of the first and second non-metallic regions 22a, 22b comprises at least one tuning slot (31a, 33a; 31b, 33b) formed in the generally triangular areas. In Figure 2 each of the first and second non-metallic regions 22a, 22b is shown as having a first tuning slot 31a, 31b, respectively, and a second tuning slot 33a, 33b, respectively. The tuning slots in combination with the tapering of the first and second non-metallic regions enable the antenna to be reduced in size, yet used with the wide range of frequencies required by ultra wideband devices. The tuning slots 31a, 31b, 33a, 33b are described in greater detail below in relation to Figure 3.

The non-metallic areas formed by the first and second non-metallic regions 22a, 22b, the non-metallic channels 23a, 23b and the plurality of tuning slots form the following metallic regions (i.e. metallic regions which remain on the substrate after creation of the various non-metallic regions).

A first metallic region corresponds to a co-planar antenna feed region 24 which, during use, is connected to receive the positive signal from the antenna feed point 28. The antenna feed region 24 is connected to a first radiating portion 25, which is generally triangular in shape and having its apex connected to the antenna feed region 24. The first radiating portion 25 is connected to second and third radiating portions 26a and 26b via respective first and second edge portions 27a and 27b. The second and third radiating portions 26a and 26b are connected, during use, to a ground connection of the antenna signal. In Figure 2 the antenna is shown as being connected to an SMA end launcher feed 29, which is typically used for connecting an antenna signal to an antenna structure (for example using a co-axial cable). The first metallic region 24, i.e. defined by the first and second non-metallic channels 23a, 23b, acts as an impedance changer to interface the higher antenna impedance to the defined 50ohm single ended source.

The metallic coating may be removed to form the first and second non-metallic regions 22a, 22b, the first and second non-metallic channels 23a, 23b and the tuning slots 31a, 31b, 33a, 33b using a PCB milling machine, for example, which is capable of accurately milling the 1oz surface copper of FR4 with an accuracy of 0.1 mm, using cutters with diameters as small as 0.25 mm. The geometry of the antenna may be defined by CAD inputs, either in DXF or Gerber format, and are converted into a

machine readable format for input to the milling machine. It is also possible to accurately cut the substrate material using machine routers that come in a variety of sizes.

Alternative techniques may also be used to create the non-metallic portions, including the possibility of etching the metallic layer using chemicals or processes used for producing printed circuit boards.

It will be appreciated from the above that, in contrast to known antenna designs, the bowtie in the present invention is made from non-metallic material (i.e. compared to traditional bowtie arrangements in which the bowtie itself is made from the conducting material). Tuning of the antenna may be required when enclosed by a structure, for example a radome, or when the antenna is in close proximity to objects. Tuning the antenna may involve minor modification of the complete geometry in view of the interdependency of the various features of the structure.

The antenna described above is suited for use over at least the whole UWB frequency range due to the complementary action of the overall taper of the non-metallic regions 22a, 22b and purposely designed tuning slots 31a, 31b, 33a, 33b. These features help facilitate pure radiation modes, and minimise the amount of residual energy likely to stay within the structure (which set strong standing waves and reduce bandwidth).

Figure 3 shows a plan view of the antenna design according to an embodiment of the present invention.

As described in Figure 2, first and second non-metallic regions 22a and 22b are formed in the metal coating on the surface of the substrate 21, the first and second non-metallic regions 22a and 22b having corresponding first and second non-metallic channels 23a and 23b connecting the first and second non-metallic regions 22a, 22b to the edge of the substrate that is nearest the antenna feed.

The first and second non-metallic regions 22a, 22b and first and second non-metallic channels 23a, 23b are preferably symmetrical about a longitudinal axis X_0 (i.e. the axis corresponding to the axis of the antenna feed).

A first pair of tuning slots 31a and 31b is formed on a respective first pair of axes X_{1a}, X_{1b}. The first pair of tuning slots 31a, 31b are arranged on the first pair of axes X_{1a}, X_{1b}, such that the tuning slots 31a, 31b extend along their respective axes X_{1a}, X_{1b} to form a non-metallic area outside the non-metallic area defined by the respective first and second non-metallic regions 22a, 22b.

A second pair of tuning slots 33a and 33b is formed on a respective second pair of axes X_{2a}, X_{2b}. The second pair of tuning slots 33a, 33b are arranged on the second pair of axes X_{2a}, X_{2b}, such that the tuning slots 33a, 33b extend along their respective axes X_{2a}, X_{2b} to form a non-metallic area outside the non-metallic area defined by the respective first and second non-metallic regions 22a, 22b.

In the embodiment of Figure 3 the respective ends of the tuning slots 31a, 31b, 33a, 33b are shown as being non-parallel to the axis Y_0, resulting in tuning slots having a trapezium or trapezoid shape. However, it is noted that the respective ends of the tuning slots 31a, 31b, 33a, 33b may be arranged such that they are parallel to the axis Y_0, for example as shown in Figure 4, resulting in tuning slots having a rectangular shape.

In the embodiment of Figure 3, the magnitude of the gradient of the upper side of the non-metallic region 22a (i.e. along axis Y_{1a}) is larger than the magnitude of the gradient of the lower side of the non-metallic region 22a (i.e. along axis Y_{2a}). Similarly, the magnitude of the gradient of the upper side of the non-metallic region 22b is larger than the magnitude of the gradient of its lower side. As mentioned above, the ends of the tuning slots 31a, 31b, 33a, 33b may be arranged such that they are non-parallel to the axis Y_0. For example, in Figure 3 the ends of the tuning slots are arranged such that they are parallel with the respective axes Y_{1a}, Y_{2a}, Y_{1b} and Y_{2b}.

The dimensions of the first and second pairs of tuning slots 31a/31b and 33a/33b will now be described. It will be appreciated that these dimensions are only examples, and that other dimensions may be used without departing from the scope of the invention.

Each tuning slot 31a/31b in the first pair has a width SW1 of about 2.83mm ±10%, and a height SH1 of about 1.00mm ±10%. It can be seen that the height SH1 is provided from where the end of a tuning slot 31a/31b meets the edge of the triangular shape defined by the non-metallic regions 22a/22b, respectively. Each tuning slot 31a/31b is positioned a distance SL1 from the respective first and second non-metallic channels 23a, 23b. The distance SL1 is about 2.83mm ±10%.

Each tuning slot 33a/33b in the second pair has a width SW2 of about 2.98mm ±10%, and a height SH2 of about 2.30mm ±10%. It can be seen that the height SH2 is provided from where the end of a tuning slot 33a/33b meets the edge of the triangular shape defined by the non-metallic regions 22a/22b, respectively. Each tuning slot 33a/33b in the second pair is positioned a distance SL2 from the outer edge of the respective first and second non-metallic regions 22a, 22b. The distance SL2 is about 2.14mm ±10%.

A tuning slot 31a/31b in the first pair is separated from a tuning slot 33a/33b in the second pair by a distance SS1 of about 2.70mm ±10%.

Each edge portion 27a, 27b is about 0.33mm wide ±10%. The first and second non-metallic channels 23a and 23b are separated from the axis X_0 by a distance S1 near the point where the antenna feed is provided. The distance S1 is about 4.17mm ±10%. The first and second non-metallic channels 23a and 23 are separated from the longitudinal axis X_0 by a distance S2 near the apexes of the first and second non-metallic regions 22a and 22b. The distance S2 is about 1.28mm ±10%. From the above it can be seen that the feed separation near the antenna feed is greater than the feed separation near the first and second non-metallic regions 22a and 22b. This arrangement defines a co-planar antenna feed region 24 which becomes progressively narrower along the longitudinal axis X_0 away from the antenna feed point, until it reaches the first radiating portion 25.

As mentioned above, the dimensions and tolerances provided above are examples only, and it will be appreciated that other variations are possible without departing from the scope of the invention as defined in the appended claims.

The impact on return loss due to tolerances has been performed numerically on the exemplary antenna dimensions of the above design. It will be appreciated that the antenna consists of a large number of optimised variables that contribute to the overall performance of the design. Table 1 below provides an indication of the performance variance caused by the tolerances of the variables described in relation to Figure 3.

Table 1: Tolerance analysis of bowtie slot antenna

Variable	Description	Value (mm)	Degradation of worst case return loss (dB)
SH2	Tuning slot height 2	2.30 ±10%	1.1
S1	Feed separation 1	4.17 ±10%	1.0
SL2	Tuning slot length 2	2.14 ±10%	0.6
SS1	Slot separation	2.70 ±10%	0.6
S2	Feed separation 2	1.28 ±10%	0.3
EG	Edge gap	0.33 ±10%	0.2
SH1	Tuning slot height 1	1.00 ±10%	0.1
SW2	Tuning slot width 2	2.98 ±10%	0.1
SL1	Tuning slot length 1	2.83 ±10%	0.05
SW1	Tuning slot width 1	2.83 ±10%	0.05

The table provides a worst case degradation in return loss for these values. The parameters are placed in order of their degradation effect on the return loss. As can be seen from Table 1, the critical parameters from this analysis are the tuning slot properties, especially the second pair of tuning slots 33a/33b, and the feed separation S1. The dimensions of the second pair of tuning slots 33a/33b have a significant effect at both the low and high frequencies regions, where changes produce up to a 1 dB reduction in return loss. These changes are due to the resonant behaviour of the second slots 33a/33b being altered and hence having a deleterious effect on the overall performance.

Similar degradation effects also occur if the co-planar antenna feed region 24 is altered, where the return loss can degrade by up to 1.1 dB. This degradation is due to an increased mismatch between the co-planar antenna region 24 and the impedance of the antenna feed, which is normally 50 Ω. The other variables listed in Table 1 have less effect on the performance of the antenna, such as the first pair of tuning slots 31a/31b or edge gaps 27a/27b. It is noted, however, that the tolerance analysis has been limited to ± 10% of the nominal design, and it will be appreciated that increases to this value may produce a higher degree of degradation.

The planar antenna described above in the preferred embodiment has the advantage of being small in size, yet able to transmit and receive frequencies over at least the entire UWB frequency range, i.e. at least between 3.1 to 10.6 GHz. This is achieved by the combination of the tapering of the non-metallic regions 22a, 22b in conjunction with the one or more pairs of tuning slots 31a/31b and/or 33a/33b.

The antenna structure also has the advantages of being fabricated using extremely cheap FR4 PCB material, and of being compatible with major PCB processes and techniques. Furthermore, the antenna structure has a compact footprint and is low profile for integration into consumer equipment.

The antenna design also has the advantage of providing consistent characteristics across the UWB frequency band, while being optimised around the centre-band frequency of 6.85GHz

It is noted that, although the preferred embodiment is described in relation to using FR4 PCB material for the substrate, the invention can be used with other suitable materials forming the substrate, for example materials having a lower loss. It will be appreciated that the use of other materials may require the physical dimensions to be adjusted to compensate for the different electrical properties (for example different dielectric constant) of the different material. It will also be appreciated by a person skilled in the art that the main radiation is at the surface to air interface, with the dielectric playing a secondary role in defining the dimensions, apart from the short section of coplanar waveguide transmission line shown as the channels 23a and 23b.

The invention also contemplates the antenna being fabricated to be free standing on a suitable planar material. The free standing antenna may be formed by fabricating the metal coating on a substrate and then removing the substrate. In addition, the antenna may be constructed on or from a flexible material which may be designed to be "wrapped" around the edge of an enclosure of an UWB device.

It is also noted that the antenna described above could be arranged to operate on top of a screen, for example a CRT/LCD screen or a screen made from fabric or any other material. Such an arrangement provides directivity enhancement. The antenna may also be arranged to operate as a feed of a corner or parabolic reflector.

Although the embodiments shown in Figure 3 and Figure 4 are described as having tuning slots 31a, 31b, 33a, 33b which are shaped as a trapezium, trapezoid or rectangle, it is noted that the tuning slots may have other configurations that extend out from the area defined by the non-metallic regions 22a, 22b, For example, the tuning slots 31a, 31b, 33a, 33b may be triangular or curved in shape. Also, the antenna may have more or fewer tuning slots than the number shown in the embodiments above.

Furthermore, although the described embodiments show the tuning slots extending out from above and below the non-metallic regions 22a, 22b, it will be appreciated that the tuning slots may extend from the non-metallic region 22a, 22b in one direction only, for example either above or below the non-metallic region 22a, 22b.

In addition, although the tuning slots are described as lying on axes that are parallel to the longitudinal axis, the tuning slots may lie of other axes, or lie on axes that are non-parallel with respect to each other.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim, "a" or "an" does not exclude a plurality, and a single unit may fulfil the functions of several units recited in the claims. Any reference signs in the claims shall not be construed so as to limit their scope.

CLAIMS

1. An ultra wideband antenna comprising:

a substrate (21);

a metal layer deposited on the substrate;

wherein the metal layer comprises first and second non-metallic regions (22a, 22b) defined therein, the first and second non-metallic regions (22a, 22b) being arranged on either side of a longitudinal axis (X_0), the longitudinal axis (X_0) corresponding to a feed axis of the antenna, the first and second non-metallic regions tapering towards the longitudinal axis (X_0) to form a bowtie pattern;

wherein each of the first and second non-metallic regions comprises at least one tuning slot (31, 33), the at least one tuning slot (31, 33) being arranged about a respective first axis (X_1, X_2), the first axis (X_1, X_2) being parallel to the longitudinal axis (X_0);

and wherein the at least one tuning slot extends along its respective axis (X_1, X_2) to form a non-metallic area outside the non-metallic area defined by the respective first or second non-metallic region (22a, 22b).

2. An antenna as claimed in claim 1, wherein the first non-metallic region (22a) is a mirror image of the second non-metallic region (22b) about the longitudinal axis (X_0).

3. An antenna as claimed in claim 1 or 2, further comprising first and second non-metallic channels (23a, 23b), the first and second non-metallic channels (23a, 23b) connecting the first and second non-metallic regions (22a, 22b) to an edge of the substrate.

4. An antenna as claimed in claim 3, wherein the first non-metallic channel (23a) is a mirror image of the second non-metallic channel (23b) about the longitudinal axis (X_0).

5. An antenna as claimed in claim 3 or 4, wherein the first and second non-metallic channels (23a, 23b) connect with the first and second non-metallic regions (22a, 22b) near an apex of the first and second non-metallic regions (22a, 22b).

6. An antenna as claimed in any one of claims 3 to 5, wherein the first and second non-metallic channels (23a, 23b) form a co-planar feed region (24) in the metal layer along the longitudinal axis (X_0).

7. An antenna as claimed in claim 6, wherein the co-planar feed region (24) is connected to a first radiating portion (25), the first radiating portion (25) having an apex connected to the co-planar feed region (24).

8. An antenna as claimed in claim 7, further comprising second and third radiating portions (26a, 26b), the second and third radiating portions (26a, 26b) arranged on either side of the longitudinal axis (X_0), and being connected to the first radiating portion (25) via edge portions (27a, 27b) provided along the periphery of the substrate.

9. An antenna as claimed in any one of claims 6 to 8, wherein the co-planar feed region (24) is connected, during use, to a positive antenna signal.

10. An antenna as claimed in claims 8 or 9, wherein the second and third radiating portions (26a, 26b) are connected, during use, to a ground connection of the antenna signal.

11. An antenna as claimed in any of the preceding claims, wherein each of the first and second non-metallic regions (22a, 22b) comprises first and second tuning slots (31a, 31b; 33a, 33b), each of the first tuning slots (31a, 31b) being arranged about a respective first axis (X_{1a}, X_{1b}), and each of the second tuning slots being arranged about a respective second axis (X_{2a}, X_{2b}).

12. An antenna as claimed in claim 11, wherein each of the first tuning slots (31a, 31b) and each of the second tuning slots (33a, 33b) have substantially parallel sides to the respective first axis (X_{1a}, X_{1b}) and the respective second axis (X_{2a}, X_{2b}).

13. An antenna as claimed in claim 12, wherein the width of the second tuning slot (33a, 33b) about the second axis (X_{2a} X_{2b}) is greater than the width of the first tuning slot (31a, 31b) about the first axis (X_{1a}, X_{1b}).

14. An antenna as claimed in claim 13, wherein the width of the second tuning slot (33a, 33b) is in the range of about 2.68mm to about 3.28mm.

15. An antenna as claimed in claim 13 or 14, wherein the width of the first tuning slot (31a, 31b) is in the range of about 2.55mm to about 3.11mm.

16. An antenna as claimed in any one of claims 6 to 15, wherein the width of the co-planar feed region becomes narrower along the longitudinal axis (X_0) away from the edge of the substrate which receives an antenna feed.

17. An antenna as claimed in claim 16, wherein the width of the co-planar feed region at the end near the antenna feed is in the range of about 7.50mm to about 9.17mm.

18. An antenna as claimed in claim 16 or 17, wherein the width of the co-planar feed region at the end away from the antenna feed is in the range of about 2.30mm to about 2.82mm.

19. An antenna as claimed in any one of the preceding claims, wherein the first and second non-metallic regions (22a, 22b) are generally triangular in shape.

20. An antenna as claimed in claim 19, wherein the magnitude of the gradient of an upper side of the first and second non-metallic regions (22a, 22b) is larger than the magnitude of the gradient of the lower side of the first and second non-metallic regions (22a, 22b), the lower side being the side nearest to an antenna feed.

21. An antenna as claimed in any one of claims 1 to 11, wherein the first and second tuning slots (31a, 31b, 33a, 33b) are generally triangular in shape.

22. An antenna as claimed in any one of claims 1 to 11, wherein the first and second tuning slots (31a, 31b, 33a, 33b) are generally trapezoidal or trapezium in shape.

23. An antenna as claimed in any one of claims 1 to 11, wherein the first and second tuning slots (31a, 31b, 33a, 33b) are generally circular in shape.

24. An antenna as claimed in any one of the preceding claims, wherein the substrate is made from FR4 PCB material.

25. An antenna as claimed in claim 24, wherein the substrate is planar.

26. An antenna as claimed in any one of claims 1 to 23, wherein the substrate is made from a flexible material.

27. An ultra wideband antenna comprising:

a metal layer;

wherein the metal layer comprises first and second non-metallic regions (22a, 22b) defined therein, the first and second non-metallic regions (22a, 22b) being arranged on either side of a longitudinal axis (X_0), the longitudinal axis (X_0) corresponding to a feed axis of the antenna, the first and second non-metallic regions tapering towards the longitudinal axis (X_0) to form a bowtie pattern;

wherein each of the first and second non-metallic regions comprises at least one tuning slot (31, 33), the at least one tuning slot (31, 33) being arranged about a respective first axis (X_1, X_2), the first axis (X_1, X_2) being parallel to the longitudinal axis (X_0);

and wherein the at least one tuning slot extends along its respective axis (X_1, X_2) to form a non-metallic area outside the non-metallic area defined by the respective first or second non-metallic region (22a, 22b).

28. An antenna as claimed in claim 27, wherein the first non-metallic region (22a) is a mirror image of the second non-metallic region (22b) about the longitudinal axis (X_0).

29. An antenna as claimed in claim 27 or 28, further comprising first and second non-metallic channels (23a, 23b), the first and second non-metallic channels (23a, 23b) connecting the first and second non-metallic regions (22a, 22b) to an edge of the metal layer.

30. An antenna as claimed in claim 29, wherein the first non-metallic channel (23a) is a mirror image of the second non-metallic channel (23b) about the longitudinal axis (X_0).

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31. An antenna as claimed in claim 29 or 30, wherein the first and second non-metallic channels (23a, 23b) connect with the first and second non-metallic regions (22a, 22b) near an apex of the first and second non-metallic regions (22a, 22b).

32. An antenna as claimed in any one of claims 29 to 31, wherein the first and second non-metallic channels (23a, 23b) form a co-planar feed region (24) in the metal layer along the longitudinal axis (X_0).

33. An antenna as claimed in claim 32, wherein the co-planar feed region (24) is connected to a first radiating portion (25), the first radiating portion (25) having an apex connected to the co-planar feed region (24).

34. An antenna as claimed in claim 33, further comprising second and third radiating portions (26a, 26b), the second and third radiating portions (26a, 26b) arranged on either side of the longitudinal axis (X_0), and being connected to the first radiating portion (25) via edge portions (27a, 27b) provided along the periphery of the metal layer.

35. An antenna as claimed in any one of claims 32 to 34, wherein the co-planar feed region (24) is connected, during use, to a positive antenna signal.

36. An antenna as claimed in claims 34 or 35, wherein the second and third radiating portions (26a, 26b) are connected, during use, to a ground connection of the antenna signal.

37. An antenna as claimed in any one of claims 27 to 26, wherein each of the first and second non-metallic regions (22a, 22b) comprises first and second tuning slots (31a, 31b; 33a, 33b), each of the first tuning slots (31a, 31b) being arranged about a respective first axis (X_{1a}, X_{1b}), and each of the second tuning slots being arranged about a respective second axis (X_{2a}, X_{2b}).

38. An antenna as claimed in claim 37, wherein each of the first tuning slots (31a, 31b) and each of the second tuning slots (33a, 33b) have substantially parallel sides to the respective first axis (X_{1a}, X_{1b}) and the respective second axis (X_{2a}, X_{2b}).

39. An antenna as claimed in claim 38, wherein the width of the second tuning slot (33a, 33b) about the second axis (X_{2a} X_{2b}) is greater than the width of the first tuning slot (31a, 31b) about the first axis (X_{1a}, X_{1b}).

40. An antenna as claimed in claim 39, wherein the width of the second tuning slot (33a, 33b) is in the range of about 2.68mm to about 3.28mm.

41. An antenna as claimed in claim 39 or 40, wherein the width of the first tuning slot (31a, 31b) is in the range of about 2.55mm to about 3.11mm.

42. An antenna as claimed in any one of claims 32 to 41, wherein the width of the co-planar feed region becomes narrower along the longitudinal axis (X_0) away from the edge of the metal layer corresponding to where the antenna feed is received.

43. An antenna as claimed in claim 42, wherein the width of the co-planar feed region at the end near the antenna feed is in the range of about 7.50mm to about 9.17mm.

44. An antenna as claimed in claim 42 or 43, wherein the width of the co-planar feed region at the end away from the antenna feed is in the range of about 2.30mm to about 2.82mm.

45. An antenna as claimed in any one of claims 27 to 44, wherein the first and second non-metallic regions (22a, 22b) are generally triangular in shape.

46. An antenna as claimed in claim 45, wherein the magnitude of the gradient of an upper side of the first and second non-metallic regions (22a, 22b) is larger than the magnitude of the gradient of the lower side of the first and second non-metallic regions (22a, 22b), the lower side being the side nearest to an antenna feed.

47. An antenna as claimed in any one of claims 27 to 37, wherein the first and second tuning slots (31a, 31b, 33a, 33b) are generally triangular in shape.

48. An antenna as claimed in any one of claims 27 to 37, wherein the first and second tuning slots (31a, 31b, 33a, 33b) are generally trapezoidal or trapezium in shape.

49. An antenna as claimed in any one of claims 27 to 37, wherein the first and second tuning slots (31a, 31b, 33a, 33b) are generally circular in shape.

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