Lodhi, Tariq (2001) InP based 77 GHz monolithic millimetre wave integrated circuits. PhD thesis

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InP Based 77 GHz Monolithic Millimetre Wave Integrated Circuits

thesis by

Tariq Lodhi

Submitted for the Degree of Doctor of Philosophy to the Department of Electronics and Electrical Engineering, University of Glasgow

April 2001

Abstract

The aim of this work was to design, fabricate and characterize InP high electron mobility transistor (HEMT) based monolithic millimetre wave integrated circuits (MMIC) which operate at 77 GHz. To achieve this active and passive circuit elements were designed, fabricated and characterized and accurate equivalent circuit models extracted. All circuits were designed with coplanar waveguide (CPW) as the transmission medium. Electron beam lithography was used for most fabrication processes in this work.

A range of passive elements such as CPW discontinuities, series and parallel MIM and interdigital capacitors of different sizes and NiCr resistors were designed fabricated and measured. Equivalent circuit models of these elements were extracted which were shown to be valid to 110 GHz.

Passive circuits such as branch-line coupler, rat-race coupler, Lange coupler and Wilkinson divider were successfully demonstrated at W-band frequencies. In all cases the circuits have equal power splitting characteristics with low insertion losses and very good input and output match over large bandwidth. Equivalent circuits of these circuits were extracted and were used in design of MMICs.

Active devices were fabricated on a lattice matched InAlAs/InGaAs InP HEMT material structure. Two different 0.12 μm T-gate processes were used to make these devices with a UVIII/PMMA based process giving superior high frequency performance when compared to a conventional Copolymer/PMMA based T-gate structure. The end to end gate resistance of UVIII/PMMA T-gate was comparable to the lowest 0.1 μm gate resistance ever reported. The HEMTs fabricated in this work have shown f_T as high as 193 GHz and MAG of 13 dB at 94 GHz. Equivalent circuit models of these HEMTs were extracted and were valid up to 110GHz.

These passive and active circuit models were used to design MMICs, in particular reactively matched single ended, balanced and balanced switching amplifiers at 77 GHz. Direct carrier modulators including BPSK, bi-phase amplitude modulation, QPSK and QAM were designed, fabricated and measured at 77 GHz. These modulators are designed with reflection type topology to perform the different modulation schemes. The Balanced BPSK modulator circuit was used to demonstrate switching operation with ON-OFF isolation better than 25 dB. The

two ON states showed 180±5° phase difference which is almost ideal for BPSK modulation. For all states, the input and output reflections were measured to be better than -17 dB at the design frequency. In the case of QAM and QPSK modulation, the circuits showed non-ideal performance with high insertion loss and phase errors but the input and out put reflections were better than -10 dB.

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Acknowledgments

Over the past three years, a number of people have helped me in my efforts to make MMICs. I am thankful to my supervisor Iain Thayne for letting me work in an exciting area of microwave research and for his invaluable support during the project. All the FET group members have made significant contributions in this work. I am grateful to Susan Ferguson who is responsible for doing air bridging in all the wafer runs. Thanks to Helen Mclelland for showing me the pros and cons of wafer fabrication, sorting out the T-gate mess (copoly 97-98) with help from other group members, for annealing all the HEMT samples in the project and for her unlimited support over the three years. I am grateful to David Edgar, who provided me with the initial HEMT data for small signal modeling, for sharing his wealth of MMIC design and measurement knowledge and for driving the fabrication of joint circuit wafer run with Helen's help.

I am thankful to Yifang Chen for working with me on UVIII T-gate process. Yifang was responsible for developing the initial process, subsequently Helen and I helped him to implement the process on HEMT devices. I would like to thank Khaled Elgaid who not only introduce me to microwave measurements but is also responsible for NiCr resistor development at Glasgow (heavily used in this project). I am also grateful to Gary Ternent, Harold Chong, Fraser Williamson, Xu Li, and Zoltan Borosfoldi for their contributions in stabilization of wafer fabrication processes. Thanks to Alex Ross for introducing me to wafer thinning and helping with many measurement related issues.

I am extremely grateful to Steve Thoms who solved unlimited lithography and resist related problems in this project. Thanks to Douglas McIntyre, Dave Gourlay, Robert Harkins, Leslie Donaldson and Elizabeth Wiley for their unlimited support in the fabrication lab. I am grateful to John Weaver who gave me very good feed back after 1st and 2nd year exams on the potential directions of the project and for sharing his vast technological knowledge.

Thanks to the members of the B-3 coffee club for not only providing the best coffee and doughnuts but also sharing their vast knowledge on all kinds of science and technology related issues. I am grateful to Phil Stopford for helping me sort out many

of the images in this thesis. Thanks to Erik Johanessen and Steven Hamill for saving me from the torture of wire bonding. I am thankful to Kevin Lister for sharing his thesis writing experiences, which in turn made my thesis writing experience quite pleasant. I am grateful to Judy Wilkinson and Jon Cooper for introducing me to the idea of doing a PhD.

On a personal note, I am most grateful to my parents whose love and support is limitless. There are no words that I can use to thank them for what they have done for me. I am extremely grateful to my brothers Ali, Mohammed and sister Ayesha for their friendship and unbelievable support. Finally, I would like to thank all my friends within and outside the department for their support and encouragement over the last three years.

1 Introduction

Devices, circuits and systems operating in the Millimeter wave (MMW) range of the frequency spectrum (30 GHz-300 GHz) are finding various applications in the commercial sector [R1.1]. The demand for wireless systems has caused congestion in the microwave frequency bands (1-10 GHz) which has resulted in more applications moving to the millimeter range. At the higher frequencies the smaller wavelength in the MMW bands results in higher resolution radar and imaging system together with smaller hardware size. Perhaps the most important advantage however is large bandwidth available due to relatively few applications in the band.

MMW communications has been a focus of research in Japan since the early 1970s, supported heavily by both industry and government, leading to mature and widespread 50 GHz radio links today [R1.2]. During the same period MMW research was also pursued in the United States but mostly aimed at military applications, such as smart weapons and adverse weather alternatives to radar guidance system. Recently, the focus of the MMW industry has turned to commercial applications.

MMW communications provides the opportunity to meet the demand of ever smaller and more portable telecommunication equipment for broadband applications like microwave video distribution systems (40-42 GHz) and wireless local area networks (60-62 GHz) [R1.3, R1.4]. The sensor/radar based applications include various automotive safety accessories like intelligent cruise control, lane change aid and backup warning products (76-77 GHz) [R1.5, R1.6]. There are also portable applications like hand held radar for the blind [R1.7].

The technology required for such high volume applications needs to simultaneously satisfy low cost and high reliability requirements. Due to these needs, monolithic millimeter wave (microwave) integrated circuit (MMMIC or MMIC) technology finds a unique opportunity to be inserted into these large volume production programs (MMIC is a microwave circuit in which the active and passive components are fabricated on the same semiconductor substrate).

Indium Phosphide (InP) based high electron mobility transistors (HEMTs) provide an attractive alternative to GaAs based HEMTs at MMW frequencies for MMICs. They have demonstrated high frequency characteristics superior to any other transistor, including highest f_T (362 GHz [R1.8]), highest f_{max} (600 GHz [R1.9]), the lowest noise figure of any three terminal device at room temperature [R1.10] and the highest efficiency at MMW frequencies [R1.11]. InP based Lattice matched HEMTs (53 % indium InGaAs channel) have demonstrated 50 % higher f_T and f_{max} than a GaAs based pseudomorphic HEMTs (the most mature MMW technology) [R1.12].

Coplanar waveguide (CPW) is gaining popularity as an interconnect method at MMW frequencies [R1.13]. It has several advantages over microstrip (the most popular interconnect method) such as no backside processing, elimination of via hole and lower dispersion at MMW frequencies [R1.14]. It currently suffers from having an incomplete set of accurate passive element equivalent circuit models, which are essential for MMIC performance prediction.

Direct carrier modulation is an alternative to standard baseband modulation used in the majority of transceiver systems. In conventional transmitters, the signal is modulated at the Intermediate Frequency (IF) then up-converted using a chain of mixers, filters and amplifiers [R1.15]. In the direct carrier modulation scheme, the RF carrier frequency is modulated, which results in the elimination of sub-component chain for up-conversion. In monolithic millimeter-wave circuits where chip space is of a premium in terms of cost, direct carrier modulation is an attractive solution.

The aim of this work was to design, fabricate and on-wafer test InP based MMICs operating at 77 GHz and using coplanar waveguide as a transmission line medium. To achieve this, passive and active elements were characterized in W-band (75-110 GHz) frequency range. Equivalent circuit models of these elements were extracted which were shown to be valid in W-band. These were subsequently used in design of circuits such as amplifiers and direct carrier modulators.

1.1 Outline of the Following Chapters

Chapter two introduces the fabrication techniques used to produce InP based MMICs. Chapter three describes high frequency measurements along with a description of coplanar waveguide and an introduction to some passive elements. Chapter four describes the operation of InP lattice matched HEMTs including both DC and high frequency performance. Chapter five covers CPW couplers such as branch-line, rat-race, Lange, and Wilkinson dividers. Direct carrier modulators are covered in chapter six including an overview of operation, design and measurements. Chapter seven describes the operation and design of amplifiers. Chapter eight presents conclusions of the thesis along with suggestions for future work.

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2   MMIC Fabrication & Material Characterisation

2.1   Introduction

This chapter describes wafer fabrication techniques of InP based MMICs. It includes an overview of the electron beam lithography system and resists used in this project. The material characteristics of lattice matched HEMTs are presented. Metalisation techniques for deposition of both Schottky and Ohmic contacts are discussed. Two different 100 nm mushroom or T-gate formation techniques are described and their performance compared.

2.2 Electron Beam Lithography

In semiconductor processing, patterning techniques are critical. Lithography is the process of transferring patterns on to a thin layer of radiation sensitive material called resist covering the surface of the semiconductor wafer. Electron beam lithography (EBL) is the most flexible lithography tool for very high resolution processing. The most common lithography tools such as optical steppers or optical contact printers can not compete with electron beam lithography at high resolution as they are limited by the wavelength of the source and diffraction from masking material. Another alternative is x-ray lithography, which has the capability of going down to 30nm feature size [R2.1]. The major problem with this technology is that the x-ray masks and source are expensive [R2.2].

MMICs working in the W-band frequency range require gate technologies with minimum feature size of around 0.1μm. Electron beam lithography is capable of patterns as small as 3nm [R2.3] and can comfortably produce patterns of 30nm [R2.4]. The resolution of the electron beam system is limited by the quality of resists and electron optics. Along with high resolution, electron beam lithography offers very high alignment accuracy. In MMIC fabrication, layers of fabrication need to be aligned with one another, especially critical is the alignment of the gate in the device source-drain gap. Electron beam lithography systems can provide alignment accuracy of around 50nm [R2.5].

Additionally direct write electron beam lithography does not require the use of a mask. This avoids the problems of mask defects and gives flexibility of design modification at any stage of the process cycle. Changes can be incorporated quite easily without requiring new mask sets resulting in savings of both time and money. Most fabrication processing steps during this project were performed by electron beam lithography using 50KV accelerating voltage.

The main disadvantage of electron beam lithography is the low throughput. This is caused by long sequential writing time of samples. It is the best lithography tool when a small number of samples are being processed.

2.3   Electron Beam Lithography System

During this project electron beam lithography was performed using Leica Cambridge Electron Beam Pattern Generator 5 (EBPG5).

Electron Gun

Condenser lenses

Beam blanker

Condenser lenses

Condenser lenses

Scan coils

Pattern Generator 15 bit DAC

to x & y scan coils

Final lens system

Auto focus

Computer

Substrate

Back scatter electron detector

Faraday cup

x-stepper motor

y-stepper motor

Computer controlled stage Movement

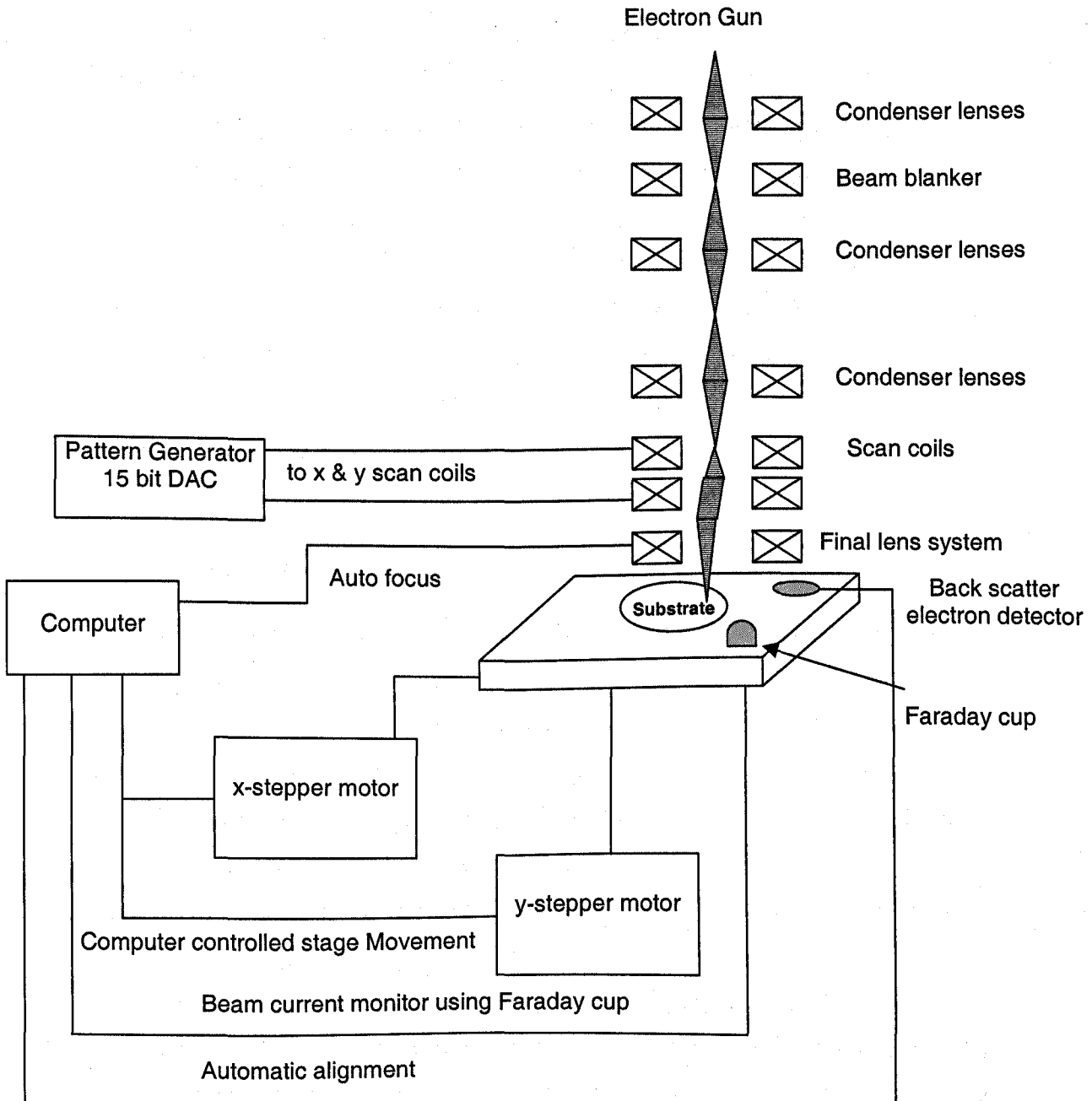Beam current monitor using Faraday cup

Automatic alignment

Figure 2.1: Schematic of Leica EBPG 5 [R2.6]

The commercial EBPG 5 system uses Guassian shaped beam forming system. Three sets of condenser lenses are used to focus the electron beam to a specific spot size on the substrate. The beam blanker acts as an on-off switch for the gun to avoid unwanted exposure of samples. The deflection coils are used to steer the beam to scan the required pattern on the substrate. The final pair of lenses are computer controlled for auto focussing the beam on substrate. The substrate is mounted on a computer controlled stage capable of moving in x-y directions. This is necessary because the scan field of the beam is much smaller than the substrate. The Faraday cup is used to monitor electron beam current (see figure 2.1).

Some of the features of this machine are:

The accelerating voltage can be varied between 20kV, 50kV and 100kV.

The main field size $800\mu m$ x $800\mu m$ at 50kV accelerating voltage

The electron spot can be selected between 12nm to 500nm

Alignment accuracy of 30nm is achievable

2.4   Electron Beam Resist

Electron beam resists allow patterns to be transferred to the substrate using lithography. When exposed by an electron beam, positive electron beam resists can be selectively removed in exposed areas by dissolving in appropriate solvent. Poly-Methyl Methacrylate (PMMA) and the copolymer of Methyl Methacrylate and Methacrylic acid P(MMA/MAA) (will be referred as copolymer) of different concentrations were used as the electron beam resists in all processing steps in this project. In some cases Deep Ultra Violet (DUV) resist was used as an alternative for EBL processing.

PMMA and copolymer are made of long chains of polymers [R2.7]. The chains can be broken by exposure from the electron beam thus making them of smaller molecular weight. These broken chains can be selectively removed in a developer that dissolves chains below a certain molecular weight leaving behind only unexposed regions of resist. The PMMA and copolymer were developed in a mixture of 4-methyl pentan-2-one (MIBK) and Isopropyl Alcohol (IPA).

PMMA is dissolved in a solvent such as chlorobenzene or xylene before use. It is spun on to the substrate at very high speed (typically 5000rpm) to uniformly coat the sample. The coated substrate is baked at a high temperature (180 °C) to disperse the solvent leaving behind only the PMMA resist film. The thickness of the resist film can be controlled by varying the concentration of PMMA in the solvent.

Chemically amplified DUV Shipley Ultra Violet III (UVIII) resist is increasingly being used for electron beam lithography [R2.8]. It is a positive resist consisting of a polymer of Hydroxystyrene and t-butylacrylate. A wide variety of resist thicknesses can be achieved by diluting the resist in ethyl lactate. The resist requires high (120 °C) post exposure bake temperature to increase its resistance to atmospheric contamination that can effect its sensitivity [R2.9]. The electron beam exposure combined with a post exposure bake chemically changes the composition of the exposed region. These exposed regions are dissolvable in Shipley CD-26 developer. The real reaction is controlled by post exposure bake where the electron beam acts like a catalyst. The advantage of the resist is its high sensitivity and low dose requirement; thus short writing time.

2.5 Metalisation & Lift Off

Once the semiconductor has been electron beam exposed and developed, a window is left in the resist film which can be further processed by metalisation or etching. The resists described above dissolve easily in acetone, a property fully exploited in lift off. By depositing metal on a sample with exposed windows of resist then placing it in acetone causes the removal of all the resist leaving behind only the metal on the surface of semiconductor (see figure 2.2).

In this project metalisation and lift off were performed using a bi layer resist process. Here two PMMA resists with different sensitivities are spun on the sample. The sensitivity of resist to the developer depends on the molecular weight of the resist. Resists with higher molecular weight are less sensitive to the developer and thus develop more slowly. Lower molecular weight (mw) resist is spun first followed by higher molecular weight which results in bottom layer being wider than top layer after development due to the difference in sensitivity. This

profile avoids the metal connection between the pattern metal and the spare metal on the top of the resist after metalisation resulting in metal feature which has smoother edges after lift off (see figure 2.2).

PMMA of two different molecular weights used for lift off are

120000 molecular weight referred to as Aldridge (ALD)

360000 molecular weight referred to as Elvacite (ELV 2041)

All metal depositions in this project were carried out using Plassys MEB 450 Electron Beam Evaporator. It has a base pressure of $1x10^{-7}$ mbar and a quartz crystal monitor to measure metal thickness. Before metalisation, samples were oxygen ashed to remove unwanted resist residual in the developed area. This is followed by a clean in diluted hydrochloric acid (HCl) to remove the surface oxide before metalisation.
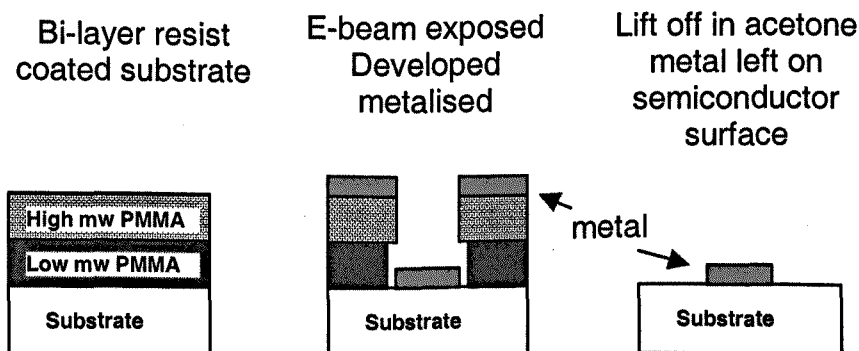
Figure 2.2: Lift off illustration using bi-layer resist

2.6   Pattern Transfer & Electron Beam Exposure

Patterns created in GdsII format with all the hierarchy information are flattened to remove the hierarchy and fractionated into smaller segments using CATS software. This file is transferred to the beam writer in the IWFL format. This IWFL file together with a job file, which contains all the exposure parameters that are to be used for pattern writing are submitted with the sample to the beam writer operator. The important parameters as far as writing is concerned are resolution, spot size

and exposure dose. The resolution defines the pixel size in the pattern and is normally set to 1/6 or less of the smallest feature size. The spot size defines the size of the actual electron beam that is being used and is normally set to 2 times the resolution size [R2.10]. The exposure dose is the number of electrons per unit area (μC/cm^2) that are being used to expose the substrate. A dose is chosen very carefully to enable the removal of all exposed resist without over exposure. Over exposure results in an increase in the size of the developed feature. Normally dose tests are carried out on test samples to determine the optimal dose for a specific feature.

2.7 HEMT & MMIC Fabrication Cycle

The complete MMIC fabrication cycle used in this project contains a minimum of 8 levels of electron beam lithography combined with 3 level of optical lithography for air bridge formation.
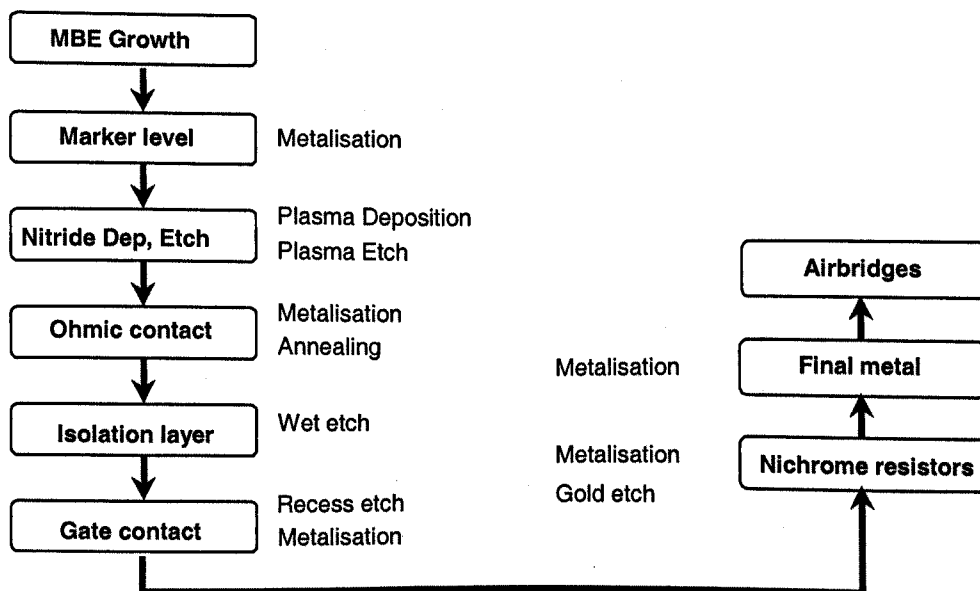
Figure 2.3: InP LMHEMT MMIC fabrication cycle

In the following sections, each level of device fabrication will be described in detail and reasons will be outlined for carrying out fabrication in the order shown in figure 2.3.

2.8 HEMT Layer Growth & Characterisation

The HEMT layer structure was grown in-house by molecular beam epitaxy (MBE) on a 400 μm thick semi-insulating indium phosphide substrate. The electronic quality of the MBE stack is evaluated by measuring the Hall mobility (μ_h) and sheet concentration (n_{sh}) [R2.11]. The typical stack used in this project is shown in figure 2.4 and explained in detail in the next chapter.

7nm 3×10^{18} cm^{-3} Si doped In$_{0.53}$Ga$_{0.47}$As **Cap** layer
20nm In$_{0.52}$Al$_{0.48}$As **Barrier**
5×10^{12} cm^{-2} Si **Delta Doping layer**
6 nm In$_{0.52}$Al$_{0.48}$As **Spacer**
20 nm In$_{0.53}$Ga$_{0.47}$As **Channel**
96 nm In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As **Superlattice Buffer**
250 nm In$_{0.52}$Al$_{0.48}$As **Buffer**
Semi-insulating InP substrate

Figure 2.4: Layer stack of InP lattice matched HEMT

Figure2.5: Images of a Van Der Pauw structure measuring 0.5 μm^2 in size.

Van Der Pauw structures were fabricated on this stack for Hall measurements (see figure 2.5). There are two levels of lithography involved in the realisation of the Van Der Pauw structure. First the Ohmic contacts are defined, metalised and annealed as will be described later in the chapter. The second layer of lithography defines the Van Der Pauw geometry, which 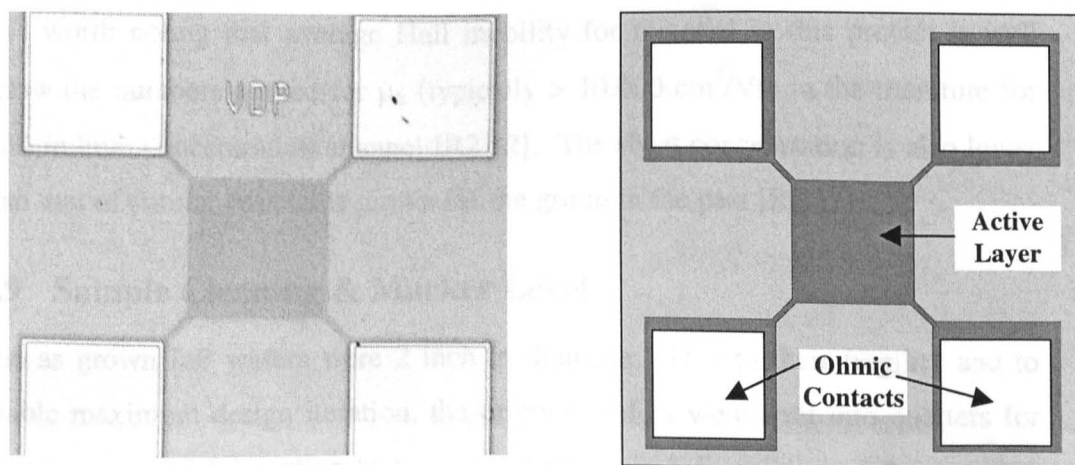enables the removal of the active layers of the sample using wet etching (see isolation section) to form the device. The active area is the darker region in figure 2.5

The Hall mobility and carrier concentration were measured at room temperature with a Bi-Rad Polaron HL5200 measurement system.

Wafer Number	Mobility (cm^2/Vs)	Sheet Concentration(cm^{-2})
A1255	7600	1.9×10^{12}
A1270	7200	2.5×10^{12}
A1276	7500	2.11×10^{12}

Table 2.1: Hall measurements of InP lattice matched HEMT at room temperature with light.

The measured Hall data for all three wafers used in this project is shown table 2.1. It is worth noting that average Hall mobility for material in this project is well below the numbers quoted for μ_h (typically > 10,000 cm^2/Vs) in the literature for 53% indium concentration channel [R2.12]. The sheet concentration is also lower than that of similar structures grown for the group in the past [R2.13].

2.9 Sample Cleaning & Marker Level

The as grown InP wafers were 2 inch in diameter. Due to their fragility and to enable maximum design iteration, the original wafers were split into quarters for fabrication. The fabrication began with cleaning and degreasing of the samples. Five-minute each ultrasonic stirring of the samples in trichlorethylene, acetone and IPA was used for cleaning, before blowing dry the sample with nitrogen.

The first lithography level of any wafer requiring multiple lithography steps involves the definition of alignment markers. High quality registration markers are needed to achieve accurate alignment for good yield circuits. This level is also used for writing identification text for devices, defining the bottom plate of metal-insulator-metal capacitors and probe alignment markers for accurate placement of RF probes during measurements.

(a)   (b)
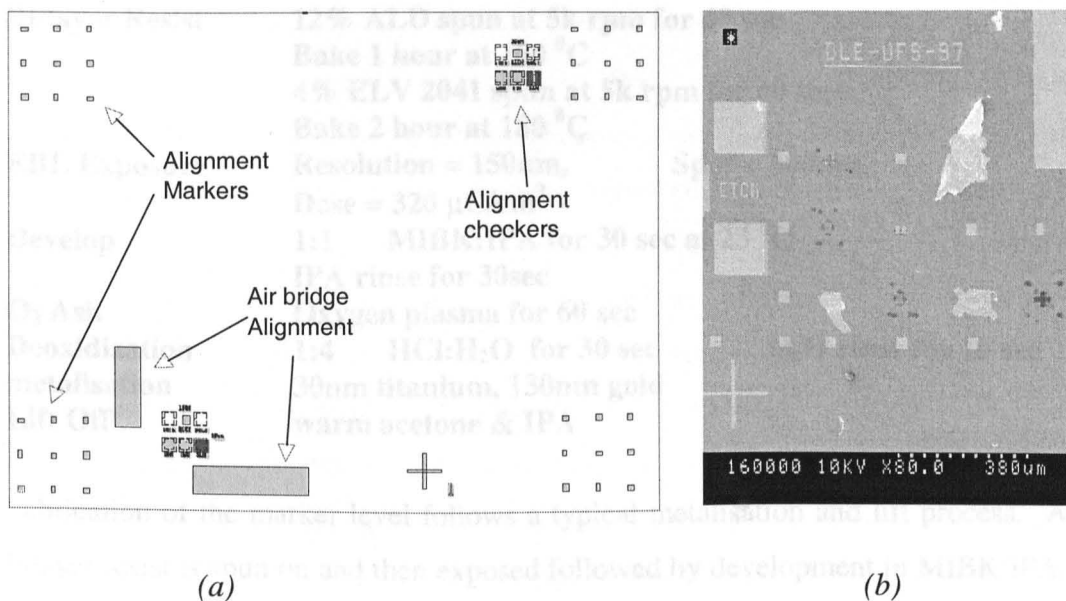
Figure 2.6: (a) Layout of typical cell with different set of markers and alignment checkers. (b) SEM of damaged markers after lithography

On a wafer, cells containing circuits and devices are written in the form of a matrix. Each of the cells have their own set of alignment markers placed at the four corners (see figure 2.6). The marker set comprises an array of squares of size 30 μm^2. The reason for having a group of markers at each corner is that a marker is degraded for each level of lithography as when the marker is being registered, it is exposed by the electron beam. This causes exposure of resist covering the marker and if this is followed by metalisation, this will result in metal covering the marker making it useless for subsequent levels. In an effort to find a marker the beam can expose all the markers that are in the array, destroying them all if metalisation is followed (see figure 2.6b). To avoid this a cross is used which

provides the initial target for the beam then in the job-file mentioned before, the exact distance between cross and the marker being used is provided making it easier for the marker to be found without any damage. The large vertical and horizontal bars are for air bridge alignment. The alignment checkers are a special set of markers designed to check the alignment of each level to the marker level. The complete fabrication process for the marker level is as follows

Bi-layer Resist	**12% ALD spun at 5k rpm for 60 sec**
	Bake 1 hour at 180 ^{0}C
	4% ELV 2041 spun at 5k rpm for 60 sec
	Bake 2 hour at 180 ^{0}C
EBL Exposure	**Resolution = 150nm, Spot = 300nm,**
	Dose = 320 μC/cm^2
Develop	**1:1 MIBK:IPA for 30 sec at 23 ^{0}C**
	IPA rinse for 30sec
O$_2$ Ash	**Oxygen plasma for 60 sec**
Deoxidization	**1:4 HCl:H$_2$O for 30 sec H$_2$O rinse for 10 sec**
metalisation	**30nm titanium, 130nm gold**
Lift Off	**warm acetone & IPA**

Fabrication of the marker level follows a typical metalisation and lift process. A bilayer resist is spun on and then exposed followed by development in MIBK:IPA. It is worth noting that MIBK concentration in the developer depends on the required resolution. For more control in the development process, this concentration can be reduced further. The sample is ashed after development to remove the resist residuals from the exposed region. The deoxidization is done just before the sample is put into evaporator to remove any oxide layer that might have been formed on the surface of the semiconductor. The marker metals are titanium, which provides excellent adhesion to the substrate and gold as the top layer to improve the contrast for EBL alignment.

2.10 Silicon Nitride Deposition and Etching

In MMICs silicon nitride (Si$_3$N$_4$) was used as the dielectric layer in metal-insulator-metal capacitors. As mentioned previously, the marker level was used as the bottom layer of the capacitors. The layer of silicon nitride was deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD). The process of

deposition occurs at 300 ^{0}C and to reduce the time for which the sample sits at this temperature, a "cold load" must be specified. A cold load is one in which the sample was loaded at room temperature and deposition took place immediately after the table temperature was 300 °C. N.Cameron states that if the sample sits at 300 °C for a long period indium migration can occur reducing dramatically the etch rate of the silicon nitride [R2.14].

The required thickness of nitride for capacitors was 150nm and all samples achieved errors of less than 5% from desired thickness. The only potential problem with silicon nitride is pinholes, which cause short circuits within capacitors. After the deposition, the sample is electron beam patterned and all the unnecessary silicon nitride on the sample is removed by dry etching. A damage free reactive ion etching process developed in the department using SF_6 was used [R2.14]. The samples were post baked after development and before etching to increasing the resistance of the resist to the etch process. The etch lasts for 2 minutes after which the resist can be removed with acetone.

The silicon nitride deposition patterning is performed before the Ohmic level for two main reasons. Any failure of the process during deposition and etching requires nitride to be removed using buffered hydrofluoric acid and this rapidly attacks Ohmic metal [R2.15]. Secondly the relatively high deposition temperature can degrade the Ohmic contact performance. The complete silicon nitride process is

Deposition	**PECVD silicon nitride**	
Parameters	**substrate temp. :300 °C**	**RF power :22W**
	chamber pres. :1 Torr	
	Deposition :150 nm	
Gases & Rates	**SiH$_4$:10 sccm NH$_3$:44 sccm**	**N$_2$:170sccm**
Bi-layer Resist	**12% ALD spun at 5k rpm for 60 sec**	
	Bake 1 hour at 180 ^{0}C	
	4% ELV 2041 spun at 5k rpm for 60 sec	
	Bake 2 hour at 180 ^{0}C	
EBL Exposure	**Resolution = 150nm,**	**Spot = 300nm,**
	Dose = 240 µC/cm^2	
Develop	**1:1 MIBK:IPA for 30 sec at 23 ^{0}C**	
	IPA rinse for 30sec	
O$_2$ Ash	**Oxygen plasma for 60 sec**	

Post Bake	Bake at 120 ^{0}C for 30 min	
Deoxidization	1:4 HCl:H$_2$O for 30 sec	H$_2$O rinse for 10 sec
Dry Etch	RIE SF$_6$ for 90 sec	Flow rate 22 :sccm
	Etch pressure 150 :mTorr	Bias : 5V
	RF power :12 W	Temp. :40 °C
Resist removal	warm acetone & IPA	

2.11 Ohmic Contacts

Formation of high quality Ohmic contacts is a key ingredient to good HEMT performance. The source and drain resistances of the HEMT consist of two main parts with one being the semiconductor to metal contact and the second is the access resistance due to finite resistance of the active layer. Fabricating good Ohmic contact results in smaller metal-semiconductor contact resistance. Reducing the source-drain gap causes a reduction in access resistance. In this project all devices were designed with 2μm source-drain, which after fabrication were measured to be in the range 1.6μm to 1.8μm (see figure 2.7 (b)). This gap was chosen to improve the gate yield of the HEMTs as a bigger source-drain gap avoids changes to resist thickness within the gap at gate level [R2.16].

The Ohmic patterns were written with higher resolution and smaller spot to help improve the pattern definition. It is essential to use clean glassware during Ohmic fabrication to avoid any kind to contamination. Nickel (Ni), Germanium (Ge) and Gold (Au) were used to form the contacts [R2.17]. Heating Au-Ge above its melting temperature forms the Ohmic contact to n-InGaAs. At the contact interface Ge forms a heavily doped layer to produce linear I-V characteristics after anealing and Au helps lower the melting temperature [R2.18]. Au-Ge on its own does not wet the semiconductor surface so this can be improved by adding small amount Ni which also improves the contact adhesion.

The samples were annealed in a nitrogen atmosphere at 340 ^{0}C for 30 seconds using Jipilec Rapid Thermal Annealer (RTA). InP Ohmic contacts always have poor morphology due to very thin metal stack as shown in figure 2.7 (a). The Ohmic resistances are measured before and after annealing to check that annealing was successful. Before annealing the Ohmic contact should give a very high

resistive nonlinear response where after annealing a low resistance linear curve is observed. The Ohmic contacts are written before the isolation level to enable an electrical measurement of device isolation to be performed. Annealing can harden organic residuals left on sample after processing and these can interfere with subsequent processing levels. By doing Ohmics early in process cycle, these residuals are going to be in lower numbers [R2.19].
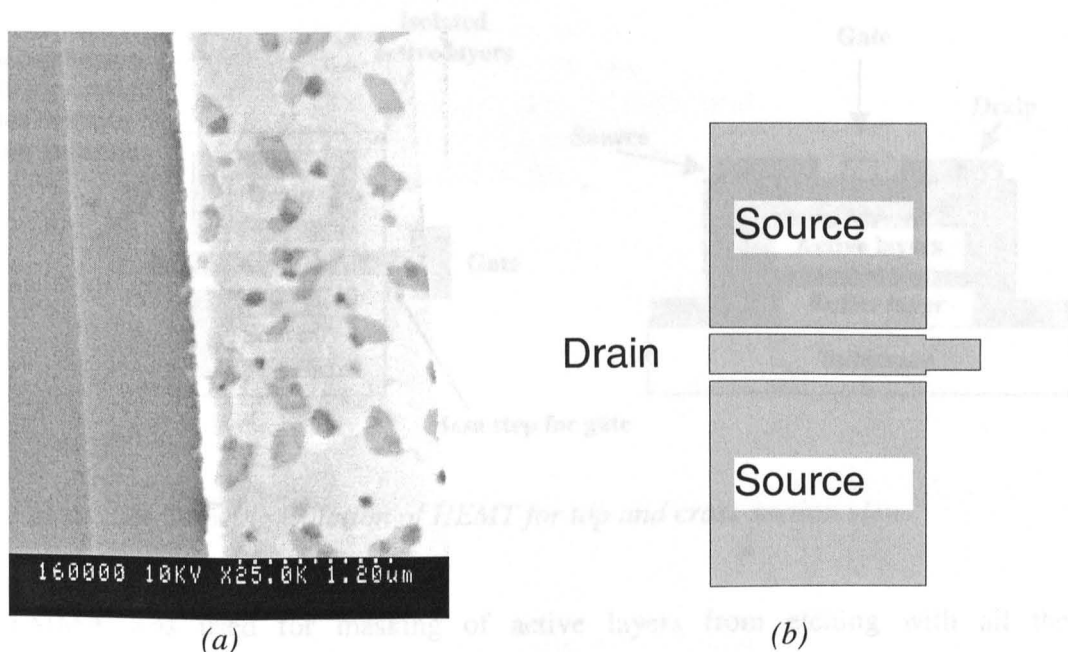

<div align="center">(a)   (b)</div>

Figure 2.7: SEM image of Ohmic contact after annealing and Ohmic layout for 100μm 2 finger device.

The complete Ohmic contact process is

Bi-layer Resist	**12% ALD spun at 5k rpm for 60 sec**
	Bake 1 hour at 180 ^{0}C
	4% ELV 2041 spun at 5k rpm for 60 sec
	Bake 2 hour at 180 ^{0}C
EBL Exposure	**Resolution = 100nm, Spot = 160nm,**
	Dose = 220 μC/cm^2
Develop	**1:1 MIBK:IPA for 30 sec at 23 ^{0}C**
	IPA rinse for 30sec
O$_2$ Ash	**Oxygen plasma for 60 sec**
Deoxidization	**1:4 HCl:H$_2$O for 30 sec H$_2$O rinse for 10 sec**
Metalisation	**Au:80nm-Ge:10nm-Ni:10nm**
Lift off	**Warm acetone & IPA for 30 sec**
RTA	**340 ^{0}C for 30 sec**

2.12 Isolation

The aim of isolation is to confine the current in the HEMT by selectively removing regions of active material. In this project devices were isolated by etching away the active material surrounding the Ohmic pads as shown in figure 2.8.
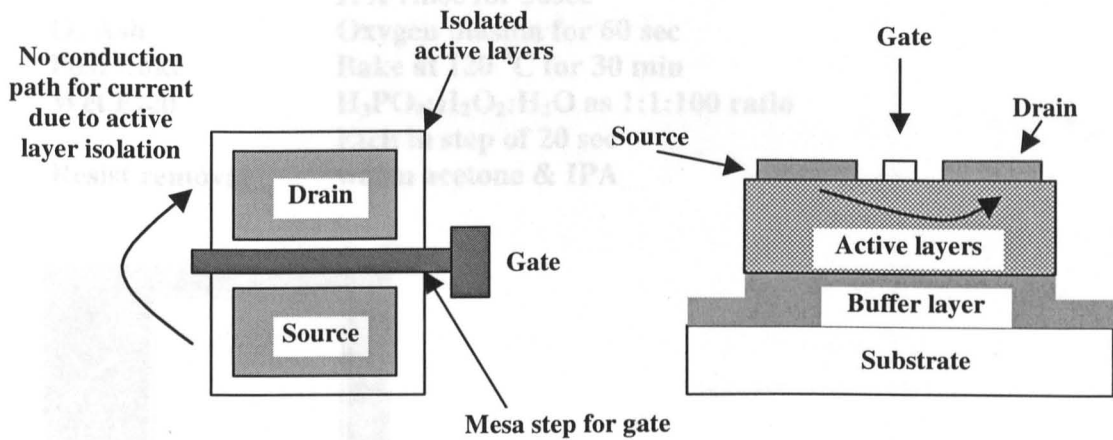

Figure 2.8: Showing isolation of HEMT for top and cross section view.

PMMA was used for masking of active layers from etching with all the surrounding areas exposed and developed. After ashing in oxygen a post exposure bake was carried out to improve the resist adhesion. The surrounding active layer was removed by wet etching using a solution containing orthophosphric acid (H_3PO_4), hydrogen peroxide (H_2O_2) and water (H_2O) in the ratio 1:1:100.

The process has to be monitored very carefully to make sure that etch depth is sufficient for complete isolation. If the etch is too deep in to the buffer layer, this can cause problems with gate fabrication as a large active layer step for the gate can cause metal discontinuity. The isolation etch was performed by monitoring the electrical current between two Ohmic pads separated by material to be removed across the wafer (see figure 2.9 (a)). The current was measured after every 20 seconds in etching solution until a target current of 50 nA/mm typically was reached. On average the isolation etch took around 60 seconds. The isolation can be confirmed by measuring the depth of mesa using a dectak, which typically showed an etch depth of 50 to 60 nm.

The complete process is

Bi-layer Resist	**12% ALD spun at 5k rpm for 60 sec** **Bake 1 hour at 180 ^{0}C** **4% ELV 2041 spun at 5k rpm for 60 sec** **Bake 2 hour at 180 ^{0}C**
EBL Exposure	**Resolution = 150nm, Spot = 300nm,** **Dose = 240 µC/cm^2**
Develop	**1:1 MIBK:IPA for 30 sec at 23 ^{0}C** **IPA rinse for 30sec**
O$_2$ Ash	**Oxygen plasma for 60 sec**
Post Bake	**Bake at 120 ^{0}C for 30 min**
Wet Etch	**H$_3$PO$_4$:H$_2$O$_2$:H$_2$O as 1:1:100 ratio** **Etch in step of 20 sec**
Resist removal	**warm acetone & IPA**

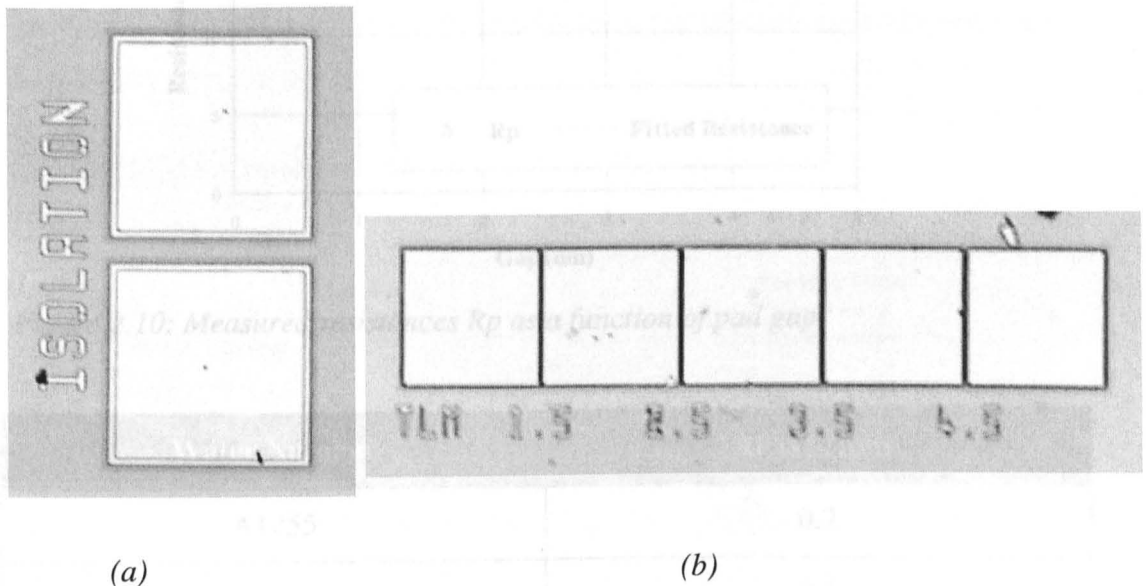*(a)*   *(b)*

Figure 2.9: (a) Isolation process control monitor image

(b) TLM pattern contact assessment

Ohmic contacts were evaluated by Transmission Line Measurement (TLM) after isolation [R2.20]. Test structures shown in figure 2.9(b) were placed across the wafer to assess the contact uniformity. The structure consists of five pads measuring 150 µm^2 separated by gaps of 1.5, 2.5, 3.5 and 4.5µm. DC four probe resistances were measured between adjacent pads using an HP 4145 and needle probes. The contact resistance can be extracted by plotting the resistance as a

function of pad gap as shown in figure 2.10. The linear resistance line fitted to measured data intercepts the y-axis (zero gap) at 2 times the contact resistance per mesa width.

For 150μm mesa

Contact resistance = (13.4/2) x 0.15 = 1 Ω.mm

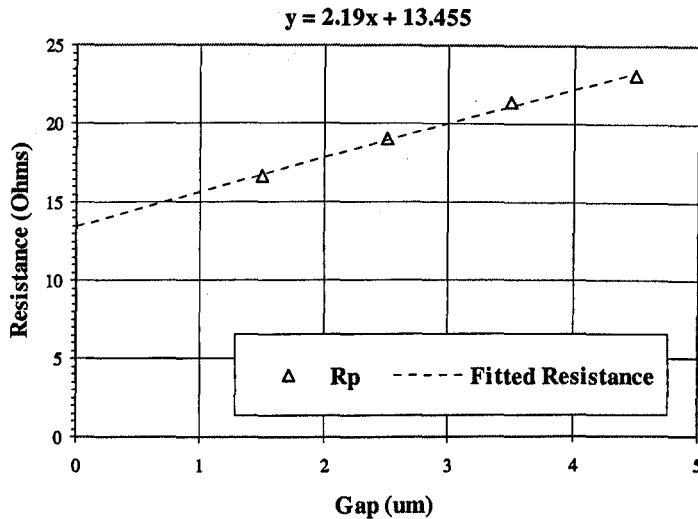*Figure 2.10: Measured resistances Rp as a function of pad gap.*

Wafer Number	Rc (Ω . mm)
A1255	0.2
a1270#1	0.6
A1276#1	0.4
A1276#2	1.1
A1276#3	1

Table 2.2: Contact resistances of some of the wafers used in the project

The average extracted contact resistance of wafers fabricated in this project is summarized in table 2.2. The typical contact resistances in literature for Au-Ge-Ni

on n-InGaAs are in 0.1 to 0.3 Ω.mm range [R2.21]. The initial samples in the project showed quite promising performances but the latter suffered due to lowering of optimum annealing temperature which was experimentally verified by D.Edgar [R2.22].

2.13 Gate Fabrication

The gate level is the most critical and yield limiting step in MMIC fabrication. Mushroom gates were used since they have a small gate resistance because of the large head size and small gate capacitance due to short foot. Two different processes were used to make mushroom gate with a 120 nm foot print. One of them uses a combination of PMMA and copolymer whereas the other one uses a PMMA/UVIII resist stack.

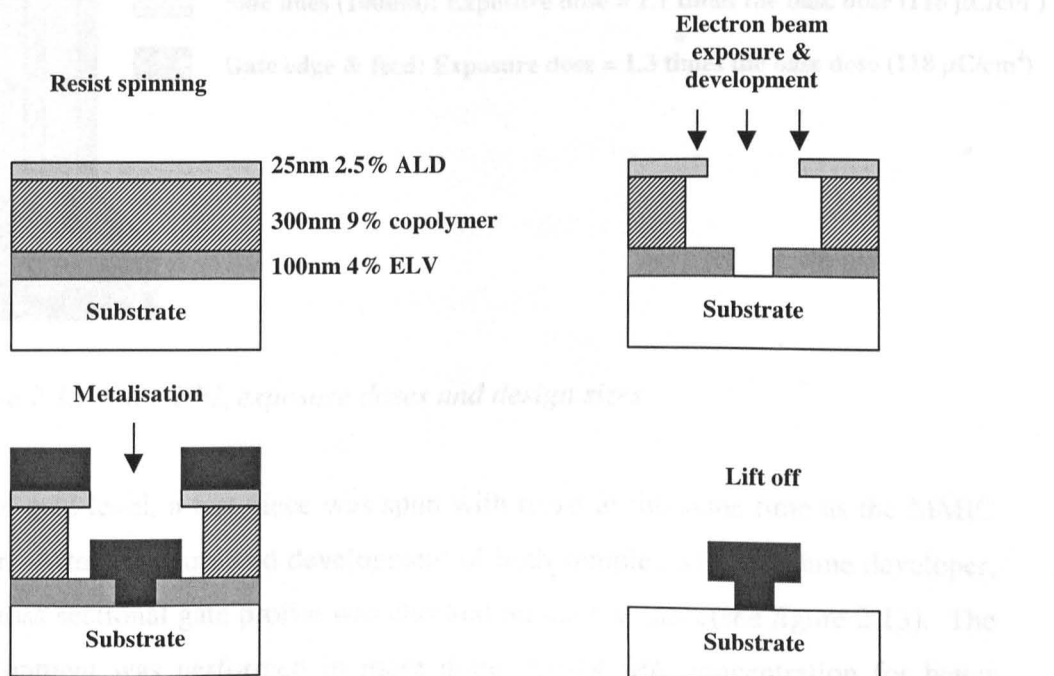### 2.13.1 PMMA-Copolymer Mushroom Gate Procedure

Figure 2.11: PMMA-Copolymer Mushroom gate formation

The wafer is spun with three layers of resist with different sensitivities. The bottom layer is the least sensitive resist consisting of 100nm thick PMMA (ELV 4%) which is used to define the 120nm footprint of the gate. The more sensitive copolymer resist 300nm thick defines the head of the gate. The final layer is 25nm thick PMMA of low molecular weight to improve the gate metal liftoff by providing an overhanging resist profile (see figure 2.11).

Three different electron beam doses are required to expose the gate (see figure 2.12). The highest dose is applied in the middle to define the foot. Low doses are applied to the sides to define the wings of the gate without affecting the size of the footprint. The aim was to achieve the head size of 450nmx160nm. In addition a feed to the gate is defined on the same level to help anchor the gate on the substrate during liftoff. The cross section of gate profile after exposure and the gate sitting in source-drain gap is shown in figure 2.13.
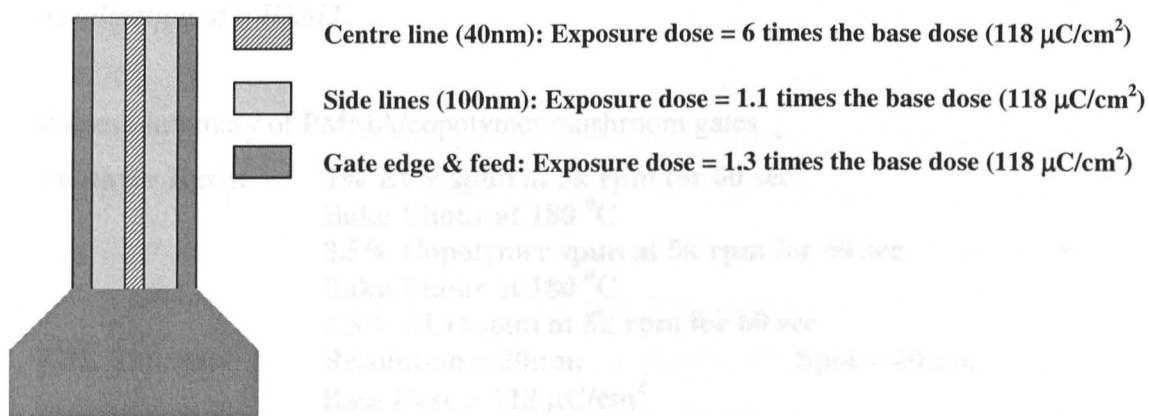

Centre line (40nm): Exposure dose = 6 times the base dose (118 $\mu C/cm^2$)

Side lines (100nm): Exposure dose = 1.1 times the base dose (118 $\mu C/cm^2$)

Gate edge & feed: Exposure dose = 1.3 times the base dose (118 $\mu C/cm^2$)

Figure 2.12: Gate EBL exposure doses and design sizes

At the gate level, a test piece was spun with resist at the same time as the MMIC wafer. After exposure and development of both samples with the same developer, the cross sectional gate profile was checked on the test piece(see figure 2.13). The development was performed in more dilute MIBK:IPA concentration for better control. Subsequently both wafer and the test piece were subjected to recess etching described in the next section.
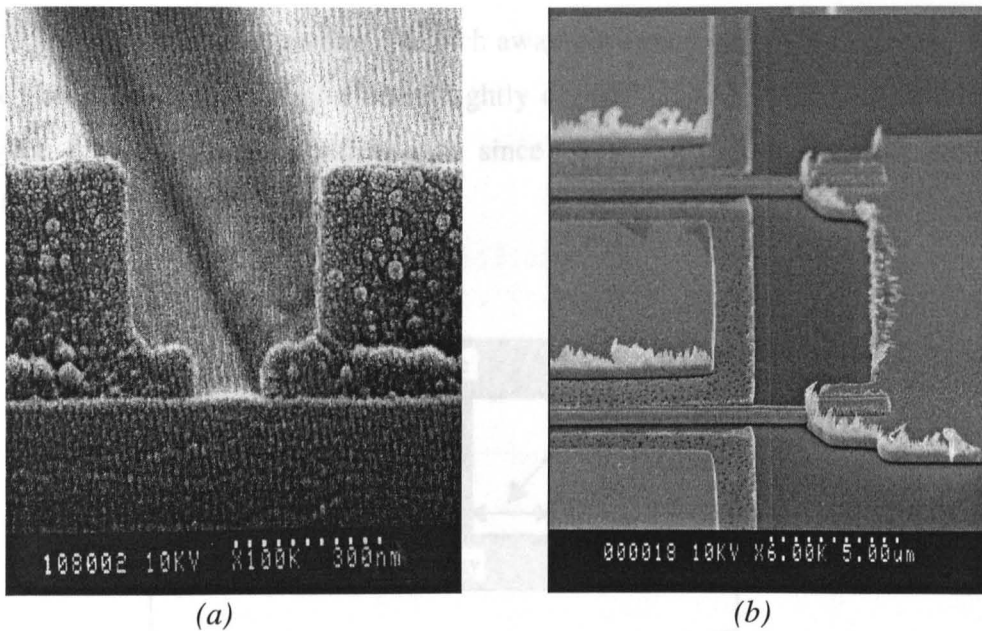
(a)   *(b)*

Figure 2.13: (a) PMMA-Copolymer resist profile before metalisation. (b) Gate metalisation of a HEMT.

Process summary of PMMA/copolymer mushroom gates

Tri-layer Resist	**4% ELV spun at 5k rpm for 60 sec**
	Bake 1 hour at 180 ^{0}C
	8.5% Copolymer spun at 5k rpm for 60 sec
	Bake 1 hour at 180 ^{0}C
	2.5% ALD spun at 5k rpm for 60 sec
EBL Exposure	**Resolution = 20nm,** **Spot = 40nm,**
	Base Dose = 118 µC/cm^2
Develop	**1:2.5 MIBK:IPA for 30 sec at 23 ^{0}C**
	IPA rinse for 30sec
Recess Etch	**1:1:200** **H$_3$PO$_4$:H$_2$O$_2$:H$_2$O & 1% of FC93**
	Etch till target current is reached
Metal	**15nm Ti, 15nm Pd & 160nm Au**
	at pressure of 1x10^{-7} Torr
Resist removal	**warm acetone & IPA**

2.13.2 Gate Recess Etching & Metalisation

The idea behind gate recessing is to etch away the highly doped cap layer to enable the gate contact to be deposited on lightly doped Schottky layer as illustrated in figure 2.14. This is a critical etch since depth and offset achieved strongly influences the HEMT performance.
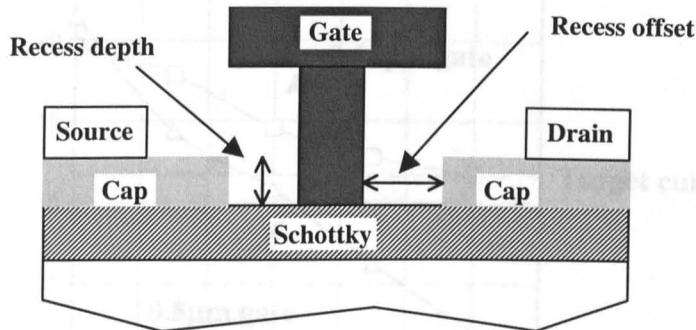

Figure 2.14: Recess etch parameters.

The recess etching was carried out using a mixture of 1:1:200 orthophosphric acid (H_3PO_4), hydrogen peroxide (H_2O_2) and water (H_2O) and 1% of FC 93 a detergent. FC93 is used to improve the uniformity and etch rate of ultra small gap in mushroom gate footprint [R2.23]. The etch was controlled by monitoring the saturation current on single gate finger HEMT test structures. The sample is initially etched for 20 seconds and then repeatedly etched and measured in 10 seconds periods until the target current is reached [R2.24]. A number of test structures are needed across the wafer to check the uniformity of the recess. The non-selective nature of the etch meant that there was often a large spread of saturation currents across the wafer. Samples with large Ohmic contact resistance needed high bias voltage to reach the saturation current and it was causing heating and melting of resist in the gap of the footprint. This was detected during the etch as no etching was occurring at sites which had been measured before. The metalisation of the gates also failed on these sites indicating a collapse of the resist profile [R2.25].

The etch rate also varied with the size of the gate footprint. A test was done to check the etching of 120nm gate and 500nm gate on the same wafer. The results shown in figure 2.15 indicate that the time required to etch 120nm mushroom gate to target current over etches 500nm gate length structures.
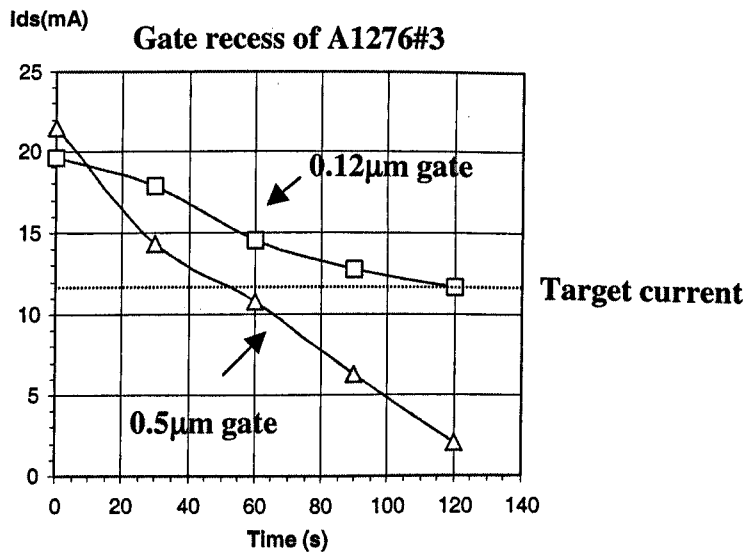

Figure 2.15: Saturation current as a function of gate recess time

After the recess etching, the samples were metalised with titanium (Ti), palladium (Pd) and Gold (Au) at very low evaporator pressure (10^{-7} Torr). Ti forms a relatively inert barrier with the semiconductor and provides a good adhesion layer for the gates, whereas Pd is the diffusion barrier to stop migration of gold into semiconductor at high temperatures. Gold is used as the top metal because of its low resistivity to achieve low gate resistance.

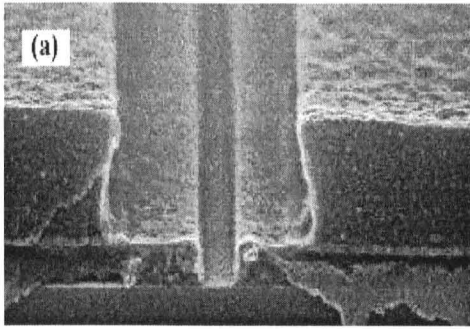## 2.13.3 PMMA-UV111 Mushroom Gate
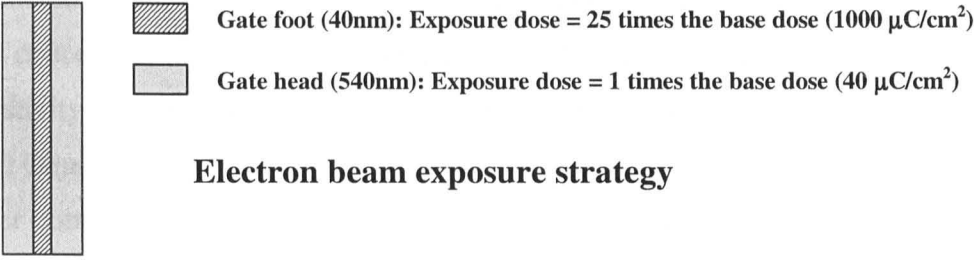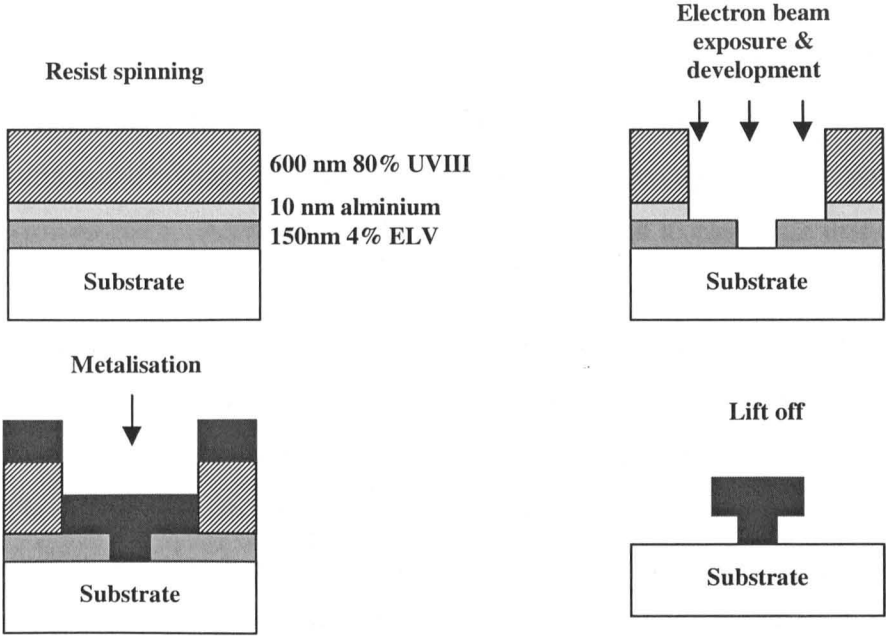
One of the disadvantages of the PMMA/Copolymer gate stack is the small sensitivity difference between the resists, which means the process window for T-gate formation is relatively small. The PMMA/UVIII layer stack offers a very large sensitivity difference and thus a large process window for gate fabrication. The stack used for the mushroom gate is shown in figure 2.16 [R2.26]. The foot is

defined in 150 nm of PMMA (ELV 4%) and the head in 600nm of 80 % UVIII in ethyl lactate. To avoid cross-linking between the resists, a 10nm layer of aluminum is deposited between resist layers. The T-gate exposure strategy is shown in figure 2.16. Here a 40nm design footprint produces an actual size of 120nm in PMMA using a dose of $1000\mu C/cm^2$ at 50 KV. The head was designed to be 550 nm wide and with a dose of $40\mu C/cm^2$ in UVIII resulted in a 600 nm structure (see figure 2.16). After exposure the samples were post exposure baked at 120 °C for 1.5 minutes on a hotplate. In these gates, the feeds were written on a different level, as the gap in doses required for the PMMA and UV3 for development is too large.
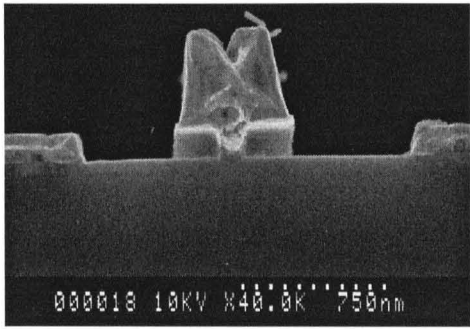
The process uses a two-developer strategy. UVIII is developed first in CD-26, which also dissolves the aluminum layer without affecting the PMMA. PMMA was developed in O-xylene instead of MIBK as it does not attack the UVIII film. The gate recess and metalisation were performed in a similar manner as described above. The DC end to end resistance of this mushroom gate was measured to be $220\Omega/mm$ which is nearly three times lower than PMMA/copolymer gates and is comparable to the lowest DC 100nm gate resistance in the literature [R2.27]. All HEMTs fabricated in this project are made with PMMA/copolymer gates unless otherwise stated.

PMMA Resist	**4% ELV spun at 3.7k rpm for 60 sec**
	Bake 2 hour at 180 ^{0}C
Evaporation	**Aluminum thickness = 10~20 nm**
Primer	**HMDS spun at 3k rpm for 30 sec**
	Bake 20 min at 80 ^{0}C
UV111 Resist	**80% UV111 spun at 4k rpm for 60 sec**
	Hot plate at 120 ^{0}C for 60 sec
EBL Exposure	**Resolution = 12.5nm, Spot = 20nm,**
	Base Dose = 40 $\mu C/cm^2$
Post Bake	**Hot plate at 120 ^{0}C for 1.5 min**
Develop	**UV111 develop in CD-26 for 60 sec at room temp.**
	Water rinse
	PMMA develop in O-xylene for 60 sec at room temp.
	Water rinse
Recess Etch	**1:1:200 H_3PO_4:H_2O_2:H_2O & 1% of FC93**
	Etch till target current is reached
Metal	**15nm Ti, 15nm Pd & 500 nm Au**

Resist removal

**at pressure of 1x10⁻⁷ Torr
warm acetone & IPA**

Resist spinning

Electron beam
exposure &
development

600 nm 80% UVIII

10 nm alminium

150nm 4% ELV

Substrate

Substrate

Metalisation

Lift off

Substrate

Substrate

Gate foot (40nm): Exposure dose = 25 times the base dose (1000 μC/cm²)

Gate head (540nm): Exposure dose = 1 times the base dose (40 μC/cm²)

Electron beam exposure strategy

(a)

000018 10KV X40.0K 750nm

Resist profile after development

Gate after metalisation

Figure 2.16: PMMA\UVIII gate fabrication process (SEM images are provided by Y.Chen)

2.14 Nichrome Resistors

In this project 50 Ohm resistors were used extensively in circuits such as power dividers and vector modulators. They are also used as standards for on-wafer measurement system calibration. Nickel-Chromium (NiCr) was used to produce these resistors. NiCr tends to suffer from surface oxidation and when the NiCr resistors make contact with bond pad level, a parasitic capacitance is generated due to oxidised NiCr. A two level EBL process was used to eliminate this capacitance from the load [R2.28].

In the first level a 30μmx20μm rectangle pattern of 35 nm NiCr and 100nm of Au was evaporated on the sample. Gold was evaporated straight after NiCr in a vacuum condition to avoid oxidation of NiCr. In the second level of lithography gold is etched away to form a square of NiCr with 50 ohm resistance.

One major draw back of NiCr is that it consists of two metals with different vapor pressure. When evaporation is done with new NiCr in the evaporator, the resulting film contains more chromium due to its lower vapor pressure and with time the Nickel concentration increases in the deposited NiCr film. This results in change of resistivity from run to run. For "old" NiCr, a thickness of 35nm was found to give 50 Ohm per square.

To over come the problem of changing resistivity, test resistors were etched first and measured [R2.29]. The data from these resistors was subsequently used to modify the size of remaining resistors to give the required resistance for the evaporated content of NiCr irrespective of its sheet resistance. The gold was etched in diluted potassium iodide (KI/I) solution for 10-15 seconds until all the gold was removed from desired areas. KI was diluted with water in one to one ratio to slow the etch rate and avoid over etching of resistors. In passive wafer runs markers and resistor deposition were combined on the same level. This could not be done with epitaxial wafers since the active layer needs to be removed before passive components can be fabricated. All levels of lithography after gate metalisation were baked at 120 ^{0}C to prevent gold diffusion in to the Schottky layer of the device which results in lowering of the barrier height and higher gate leakage current.

The resistor process can be summarised as

NiCr Deposition

Bi-layer Resist	**12% ALD spun at 5k rpm for 60 sec**
	Bake 1 hour at 120 ^{0}C
	4% ELV 2041 spun at 5k rpm for 60 sec
	Bake 2 hour at 120 ^{0}C
EBL Exposure	**Resolution = 150nm, Spot = 300nm,**
	Dose = 300 μC/cm^2
Develop	**1:1 MIBK:IPA for 30 sec at 23 ^{0}C**
	IPA rinse for 30sec
O$_2$ Ash	**Oxygen plasma for 60 sec**
Deoxidization	**1:4 HCl:H$_2$O for 30 sec H$_2$O rinse for 10 sec**
Metalise	**NiCr 35nm & 100 nm of Au**
Lift off	**Warm acetone & IPA**

Resistor Etch

Bi-layer Resist	**12% ALD spun at 5k rpm for 60 sec**
	Bake 1 hour at 120 ^{0}C
	4% ELV 2041 spun at 5k rpm for 60 sec
	Bake 2 hour at 120 ^{0}C
EBL Exposure	**Resolution = 150nm, Spot = 300nm,**
	Dose = 300 μC/cm^2
Develop	**1:1 MIBK:IPA for 30 sec at 23 ^{0}C**
	IPA rinse for 30sec
O$_2$ Ash	**Oxygen plasma for 60 sec**
Wet Etch	**Etch in KI/I :H$_2$O 1:1**
	Etch for 10 sec
resist removal	**Warm acetone & IPA**

2.15 Final Metal (Bond pad level)

The final metal defines all the interconnects of the circuit, the top plate of metal-insulator-metal capacitors and the probe pad configuration. All components are embedded in coplanar waveguide interconnects thus obviating the need for back-face wafer processing. Special probing pads are fabricated to take account of dimensions of coplanar RF probes (see figure 2.17). Two sets of markers, defined at the marker level, are incorporated into the probe pad for accurate and repeatable probe placement during measurement. The first marker indicates the position where the probe should touch the substrate and the second marker represents the

position to which the probe should be skated for accurate definition of the measurement reference plane.

The fabrication procedure for final metal is similar to the standard liftoff processes described previously for marker and Ohmic levels. To reduce RF losses, gold films of 400nm and 1.2μm were used (see chapter 3). All devices in this work were fabricated with 1.2 μm thick gold except for modulator circuits in chapter 6 and UVIII based HEMTs in chapter 3. NiCr was used as the bottom metal to improve adhesion of the bond pad. A higher concentration of PMMA resist was used to enable the lift off of the thicker low resistance films. The complete process is summarized below.
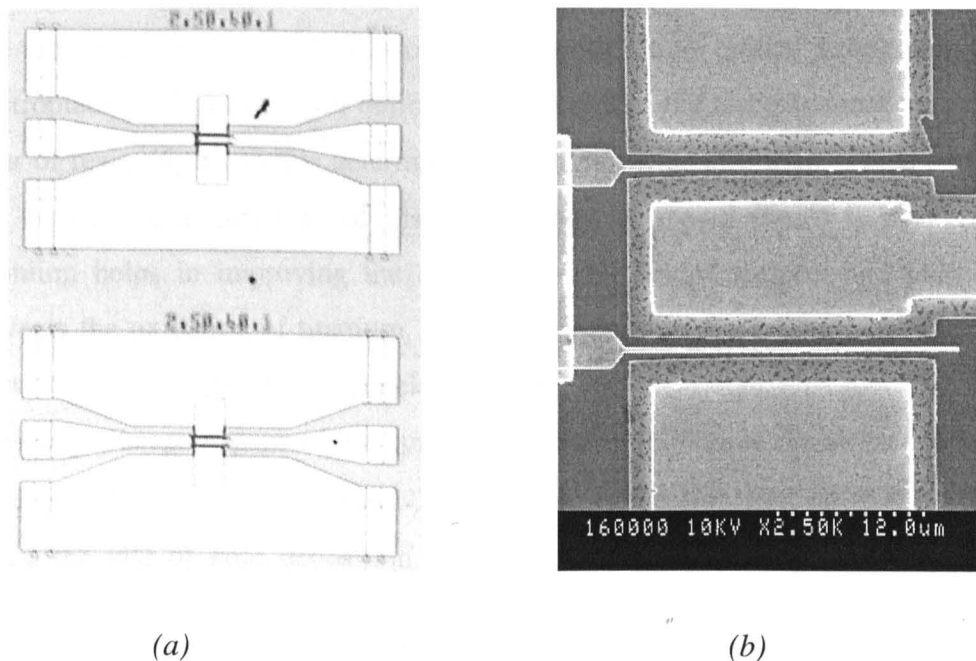

(a)   *(b)*

Figure 2.17: (a) Optical image of HEMT embedded in coplanar waveguide configuration. (b) SEM of HEMT with Ohmic pads cover with final metal

Final metal process summary

Bi-layer Resist	**15% ALD spun at 5k rpm for 60 sec** **Bake 1 hour at 120 ^{0}C** **4% ELV 2041 spun at 5k rpm for 60 sec** **Bake 2 hour at 120 ^{0}C**
EBL Exposure	**Resolution = 150nm,** **Spot = 300nm,**

Dose = 300 $\mu C/cm^2$

Develop   **1:1   MIBK:IPA for 30 sec at 23 ^{0}C**
IPA rinse for 30sec

O$_2$ Ash   **Oxygen plasma for 60 sec**
Deoxidization   **1:4   HCl:H$_2$O for 30 sec**   **H$_2$O rinse for 10 sec**
Metalise   **NiCr 50nm & 400 nm of Au**
Lift off   **Warm acetone & IPA**

2.16 Airbridges

Airbridges are essential in the coplanar waveguide medium as they are used to suppress the parasitic slotline mode (see figure 3.7), which exists with the coplanar mode in the waveguide [R2.30]. Shorting the ground planes on either side of the signal track with air bridges eliminates this parasitic mode. Air bridges have also been used in coplanar waveguide Lange couplers to connect coupling fingers.

The air bridge is made in a two level process using optical lithography and electroplating. The first level defines the supports of the airbridge in a very thick layer of resist (6μm) as this determines the height of the airbridge. Once exposed and developed, a thin film of titanium (50nm) and gold (5nm) is evaporated. Titanium helps in improving the adhesion of air bridge support and gold film prevents the oxidation of titanium. A further 40nm gold is sputtered to form the electrical contacts for subsequent electroplating

The sample is spun again with a 2μm thick resist and this time the air bridge tracks are exposed. After development, 2μm of gold is electroplated on to the sample where the rate of gold deposition is determined by the plating current [R2.31]. Flood exposure and development of the top layer of the resist follows the electroplating. Buffered hydrofluoric acid (4:1) was used to etch titanium and gold was etched with KI/I. The thick bottom layer of the resist was removed using warm acetone. A brief description of the process is shown in figure 2.18 and a more detailed description can be found in [R2.32].

Process summary

Supports of Air bridges
Bi-layer Resist   **S1828 photo resist spun @ 4k rpm for 60 sec**
                            Bake 15 min at 90 ^{0}C
                            S1828 photo resist spun @ 4k rpm for 60 sec

	Bake 15 min at 90 ^{0}C
Mask cleaning	**5 min acetone**
photo Exposure	**120 sec**
Develop	**1:4 Shiply 351:H$_2$O for 60 sec**
	H$_2$O rinse & blow dry
Post bake	**30 min at 120 ^{0}C**
Ash	**60 sec**
Metalise	**Ti 50nm & 5 nm of Au**
Sputter	**40 nm Au**
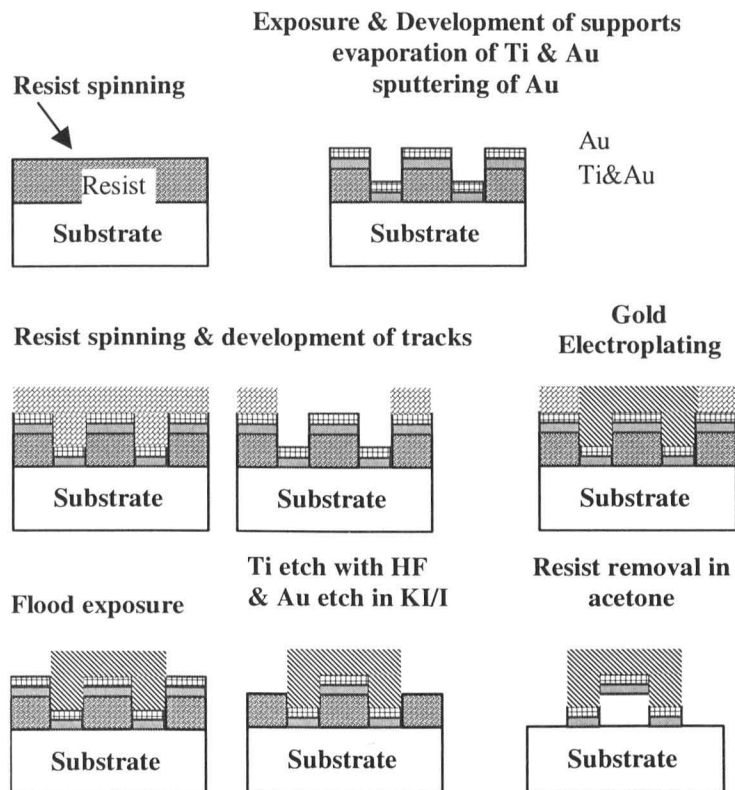
Figure 2.18: *Air bridge fabrication process summary*

Tracks of Air bridges

Bi-layer Resist	**S1818 photo resist spun @ 3k rpm for 60 sec**
	Bake 15 min at 90 ^{0}C
Mask cleaning	**5 min acetone**
photo Exposure	**60 sec**
Develop	**1:1 S1818 developer:H$_2$O for 60 sec**
	H$_2$O rinse & blow dry
Ash	**60 sec**
Gold plate	**2μm of Au layer**
	time: 20min plating temp.: 50 °C spin speed:100rpm

S1818 stripping	**Flood expose for 60 sec**
	Develop 1:1 S1828 developer:H₂O
	Ash 60 sec
Gold etch	**KI/I for 10 sec**
Ti etch	**Buffer HF 4:1 (approx. 20 sec)**
S1828 stripping	**Flood expose: 60sec**
	Develop 60 sec 1:1 S1828 developer:H₂O
	Warm acetone

2.17 Summary

This chapter has covered fabrication techniques used to produce InP based MMICs in this project. The material characteristics of lattice matched HEMT are also presented. The results of the first demonstration of UVIII-PMMA T-gates on InP HEMT devices work performed jointly with Y.Chen, are shown and evaluated.

2.18 References

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[R2.3]   D.Cumming, S.Thoms, S.P.Beaumont, J.M.R.Weaver, "Fabrication of 3nm Wire using 100KV Electron Beam Lithography and Poly(Methyl Methacrylate) Resist", Appl. Phy. Lett., Vol. 68, No. 3, pp322-324, 1996.

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3 MMIC Passive Elements

3.1 Introduction

Characterization of microwave components at high frequencies requires accurate measurement techniques. This section describes on-wafer W-band S-parameter measurements used in this project and system calibration methods used at these frequencies. Also included is a brief introduction to coplanar waveguide and some of its design rules. Operation of various passive elements in coplanar waveguide medium, their characterisation and extraction of accurate equivalent circuit models to be used in circuit design are also covered.

3.2   Scattering Parameters

At high frequencies, scattering or S-parameters are the preferred choice of network parameters for component characterisation.   S-parameters do not require short circuit or open circuit tests used in H, Y and Z parameters, which are difficult to achieve over a broadband range of microwave frequencies and can also cause active devices to oscillate depending on the device stability [R3.1].   S-parameters are defined in terms of voltage travelling waves and are relatively easy to measure. S-parameters of a two port network shown in figure 3.1 are determined by measuring the magnitude and phase of all incident, reflected and transmitted voltage signals when the ports are terminated in the characteristic impedance of the system.
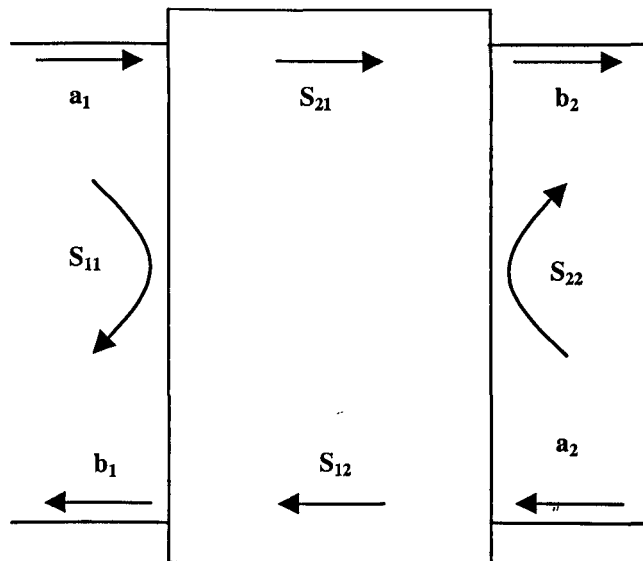
Figure 3.1: S-parameters of a 2 port device

The output and input signals are related by the following

$$b_1 = S_{11}a_1 + S_{12}a_2 \qquad\qquad \textit{Equation 3.1}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \qquad\qquad \textit{Equation 3.2}$$

By placing the source at port 1 and terminating port 2 with a matched load, no signal will be reflected back into the output of the device (i.e. $a_2 = 0$). This condition enables the determination of S_{11} and S_{21}

$$S_{11} = \frac{b_1}{a_1} \qquad \text{and} \qquad S_{21} = \frac{b_2}{a_1}$$

Similarly when the source is at port 2 and port 1 is terminated with a matched load then a_1 equals zero and S_{22} and S_{12} are

$$S_{22} = \frac{b_2}{a_2} \qquad \text{and} \qquad S_{12} = \frac{b_1}{a_2}$$

3.3 High Frequency Measurement System

The complete measurement arrangement used to characterize MMICs in shown in figure 3.2. All S-parameter measurements were carried out using Wiltron 360B network analyzer with two different probe stations. One of the probe stations was used to perform measurements from 24 MHz to 60 GHz using on-wafer
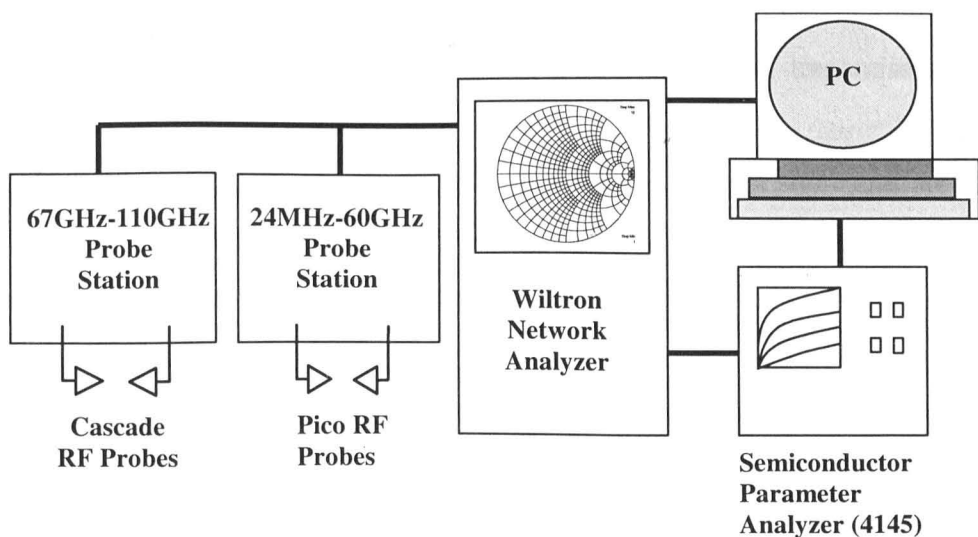
Figure 3.2: RF measurement system

Picoprobes GGB. A second probe station with a separate source was used to cover 67-110 GHz frequency range using Cascade Microtech on-wafer probes. At any one time only one frequency range can be swept with a RF switch present between the probe stations to allow changing of frequency range. The network analyzer is connected to PC for accessing S-parameter data and to semiconductor parameter analyzer for biasing transistors or circuits.

3.4 Calibration of Network Analyzer

For accurate microwave measurements, systematic errors due to imperfections in the vector network analyzer (VNA) and the test setup (cables, probes etc.) have to be de-embedded. Calibration of the VNA removes these systematic errors using measurements of known standards such as short, open, through and load to establish a measurement reference plane (boundary where measurement system ends and device under test (DUT) begins).

A number of on-wafer calibration techniques are available but very few of them have been demonstrated at W-band frequencies [R3.2]. In this project Line, Reflect, Reflect, Load (LRRM) and Line Reflect Line (LRL) calibration techniques were used. Both calibration techniques use 12-term error model correcting for imperfections such as directivity of couplers, imperfect source and load matches looking back into the test set ports, cross talk, transmission and reflection tracking between ports [R3.3].

On-wafer calibration standards are a 50 Ω thin film resistor, a short and an open circuit and 50 Ω transmission lines. The Cascade Microtech impedance standard substrate (ISS) contains all these standards, which are accurately fabricated on an alumina substrate. In this project calibration standards with 1.2 μm gold metalisation were fabricated on the same substrate as the device under test and containing the same probing pads as the DUT (see figure 3.3). The advantage of having the same pad geometry as the DUT is that the reference plane is defined at the end of the probe pad compared to probe tip for ISS standards. This de-embeds the extra parasitics and impedance discontinuity that occur at the pad-probe

transition which are not corrected by the calibration defining the reference plane at the probe tip. The ISS open is also not ideal as it is not substrate based and does not include any losses. The standards made on the same substrate as the DUT do not have very accurate 50 Ω loads.
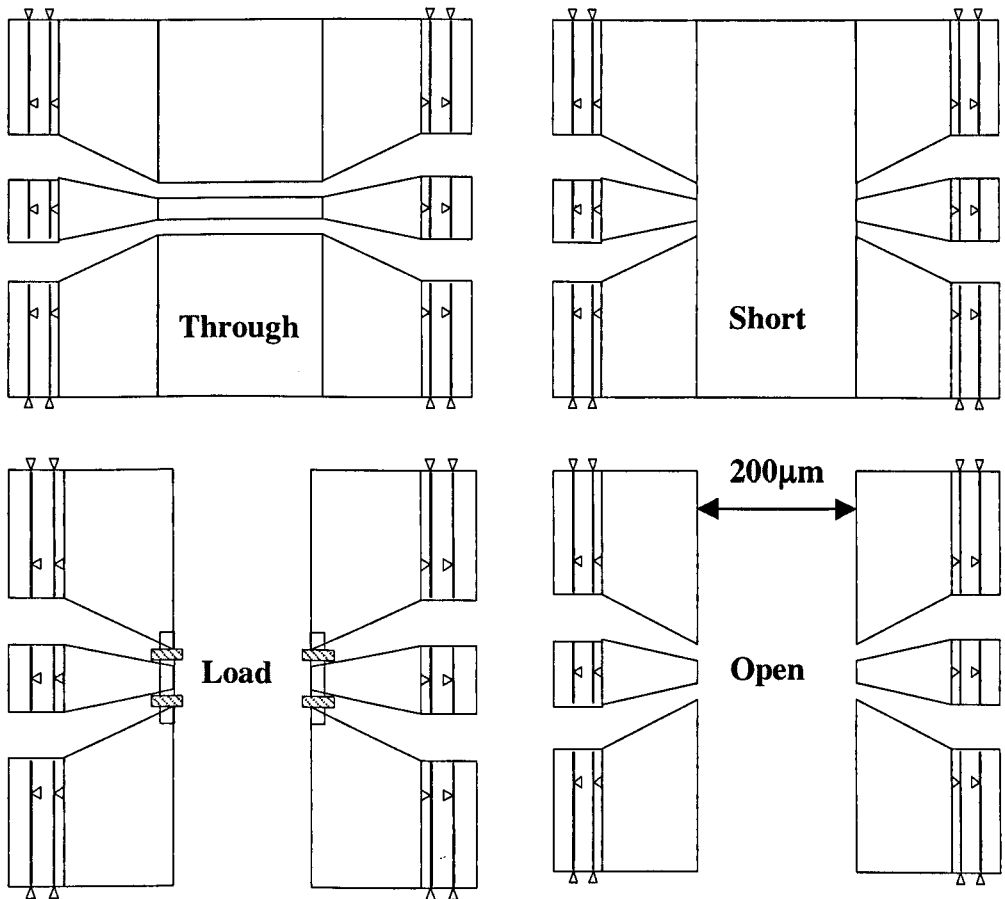

Figure 3.3: On-wafer calibration standards fabricated using processes described in chapter 2.

As the name suggests, an LRL calibration technique requires 2 transmission lines and a reflect standard (short circuit was used as a reflect standard). The reference impedance of the system is set by the characteristic impedance of the transmission lines. To calibrate over a wide band, multiple transmission lines are needed to provide suitable phase differences over the frequency range [R3.4]. At low

frequencies, conductor losses in CPW lines can cause errors in characteristic impedance, which affects the reference impedance of the calibration [R3.5].

The LRL calibration was used primarily to avoid the use of an on-wafer 50 Ω load in the calibration to enable the calibration standards fabricated on InP. It also enabled the exact match of the DUT feed lines to the reference impedance of the system as the calibration standards used exactly the same geometry.

After calibration, the standards are re-measured to verify the quality of calibration. Typically the reflections on a through and a 50 Ω load were measured to be better than -20 dB (see figure 3.4).
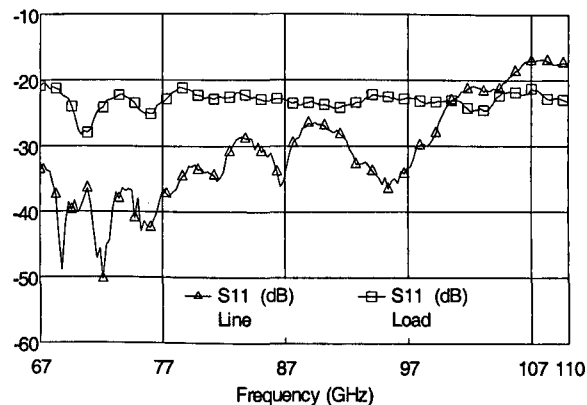
Figure 3.4: Verification of LRL calibration with measurement of 50 Ω load and 3000 μm line.

LRRM calibration technique is available using WinCal software for Cascade Microtech and requires a line, two different reflect standards and a load, which does not have to be exactly 50 Ω [R3.6]. The technique is capable of extracting the inductance of the load standard by using extra information provided to it from the reflect standard. LRRM calibration was performed using the ISS standards and verification of typical calibration is illustrated in figure 3.5 (open and short circuits were used as the two reflect standards).

Calibration and measurements at W-band were always performed with a quartz substrate between metal chuck and the substrate to suppress substrate modes. Collier and Edgar have demonstrated that the introduction of a low dielectric spacer between the substrate and the chuck increases the critical frequency

(frequency where coupling can occur) for the lowest order TM mode from 72 GHz to 130 GHz for a 400μm thick substrate [R3.7, R3.8].
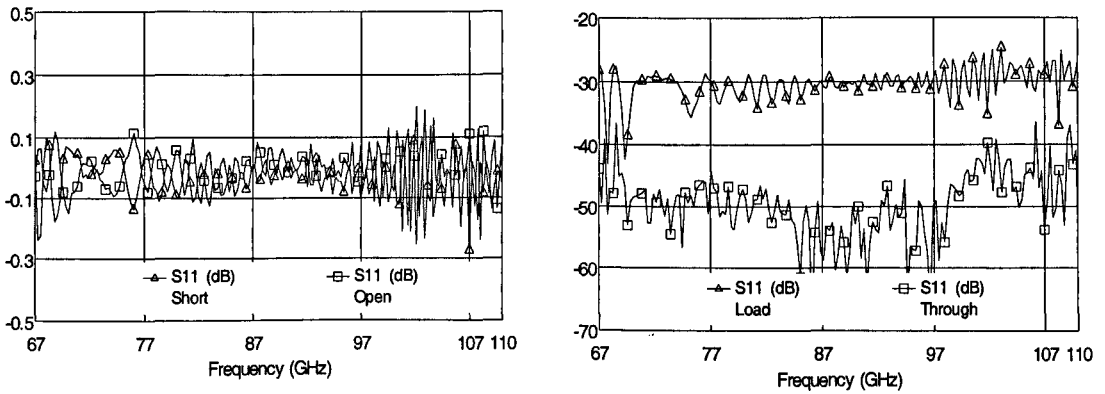
Figure 3.5: Verification of LRRM calibration on ISS standards

3.5 Coplanar Waveguide

Coplanar Waveguide (CPW) which consists of a signal conductor placed in the middle of two ground planes (see figure 3.6), was first demonstrated by Wen in 1969 [R3.9]. The dominant mode of propagation is quasi-TEM, which results in no low frequency cutoff. The characteristic impedance of CPW can be easily defined by changing the ratio of signal conductor width and ground to ground spacing.
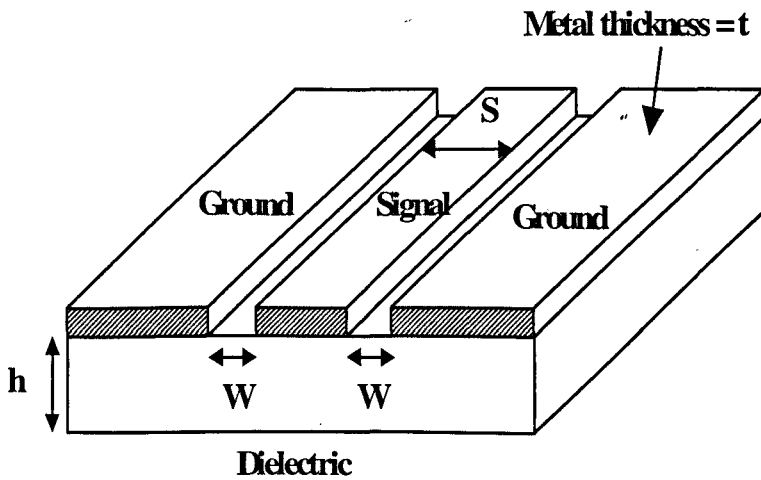
Figure 3.6: CPW physical layout

CPW was used in this project because it offers many advantages over microstrip (the most popular transmission medium) at millimeter wave frequencies. It is easier to fabricate than microstrip since there is no backside processing or via hole technology needed. The grounding of elements is done on the surface with low inductance. In addition the dispersion of CPW at millimeter waves is lower than microstrip. Finally, a considerable increase in packing density is possible in CPW because the ground planes provide shielding between adjacent lines reducing signal cross coupling [R3.10].

CPW has some disadvantages however, such as low power handling capability and poor field confinement when compared to microstrip [R3.11]. The biggest disadvantage is the generation of the slotline mode (see figure 3.7), particularly at discontinuities. This can be suppressed by using air bridges to connect the two ground planes at discontinuities and also at interval of less than a quarter of the guide wavelength $\lambda_g/4$ [R3.12].
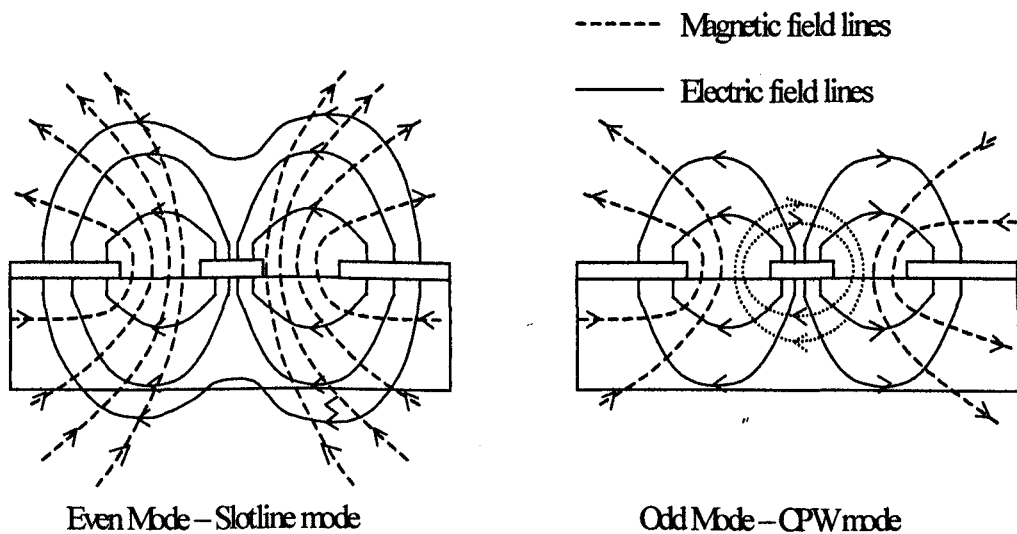
Figure 3.7: Even and odd mode in CPW transmission line

The guide wavelength λ_g is defined as

$$\lambda_g = \frac{c}{f\sqrt{\varepsilon_{eff}}} = \frac{\lambda_0}{\sqrt{\varepsilon_{eff}}}$$

Equation 3.3

where

$$\varepsilon_{eff} = (\varepsilon_{r1} + \varepsilon_{r2})/2 \qquad\qquad\qquad \text{Equation 3.4}$$

$\varepsilon_{r1} = 12.2 \qquad$ *InP permittivity*

$\varepsilon_{r2} = 1 \qquad\qquad$ *air permittivity*

c = speed of light

f = frequency (77GHz)

λ_0 *= wavelength in free space at operating frequency*

The characteristic impedance (Z_0) of the CPW can be calculated using the following expression.

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{eff}}} \frac{K(k')}{K(k)} \qquad\qquad\qquad \text{Equation 3.5}$$

Where $K(k)$ and $K(k')$ are complete elliptic integral of the first kind and its complement

$$\varepsilon_{eff} = (\varepsilon_r + 1)/2 \qquad\qquad\qquad \text{Equation 3.6}$$

ε_r *is the substrate permittivity*

$$k = S/(S+2W) \qquad\qquad\qquad \text{Equation 3.7}$$

$$k' = \sqrt{1 - k^2} \qquad\qquad\qquad \text{Equation 3.8}$$

the ratio $\dfrac{K(k')}{K(k)}$ can be estimated using

$$\frac{K(k')}{K(k)} = \frac{1}{\pi} \log\left(2\frac{1+\sqrt{k'}}{1-\sqrt{k'}} \right) \quad \text{for } 0<k<0.7 \qquad\qquad \text{Equation 3.9}$$

This expression is only valid for h > (S+2W)/2 where h, S and W are as defined in the figure 3.6 and also assumes infinite ground planes and infinitesimally thin metal thickness [R3.13].

CPW used in this project consist of 50 micron ground to ground spacing with 20 micron center conductor to obtain 50 ohm characteristic impedance on a 400 μm InP substrate. The metal thickness t, was chosen to be 1.2 μm, more than 3 times the skin depth to minimize losses in conductor caused by the resistive nature of metal [R3.14]. The signal is concentrated at the surface of conductor at millimeter wave frequencies and falls with depth into conductor. The Skin depth δ is a parameter which defines conductor thickness at which signal falls to 1/e of its surface value.

$$\delta = \frac{1}{2\pi}\sqrt{\frac{\rho}{f\mu_r}}$$

Equation 3.10

μ_r = conductor permeability

ρ = conductor resistivity (gold = 2.44 E-10 ohm/cm)

f = 77GHz
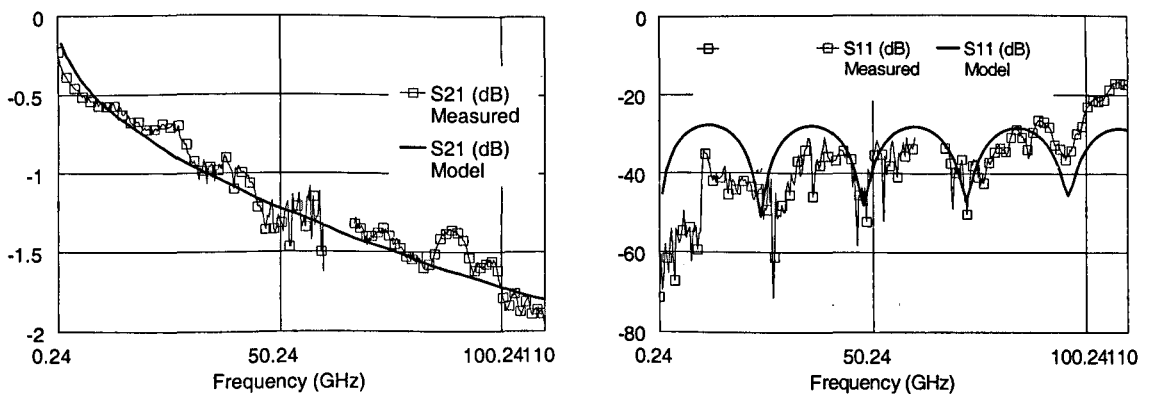
Figure 3.8: Shows measurement of a 3mm CPW line compared to Touchstone physical transmission line model of characteristic impedance of 50.8 Ω and loss 0.4 dB/mm.

A simple Touchstone physical transmission line model was fitted to the measured RF data of transmission lines to extract the loss of the lines (see figure 3.8). CPW lines fabricated with 1.2 μm thick gold metal on 400 μm InP substrate showed losses of 0.4 dB/mm at 55 GHz. In the case of 400 nm thick gold lines, losses of 0.6 dB/mm were observed at 55 GHz.

3.6 Coplanar Waveguide Discontinues

Discontinuities appear in most microwave circuits. In monolithic circuits, it is not possible to tune out unwanted parasitics after fabrication, so it becomes necessary to characterise circuit elements such as transmission line discontinuities and include them in circuit design. A number of CPW discontinuities were characterised for use in circuits. The structures were fabricated and measured, then fitted to equivalent circuit models, which were found to be valid in the frequency range 1-110 GHz. Two port tees and crosses were characterised with extra ports terminated with a full wavelength stub followed by a short or an open circuit (see figure 3.9&310). The full wavelength stub made parasitic extraction simple due to the number of resonances in the measured frequency band.

Figure 3.9 & 3.10 show the models that were fitted to the tees and crosses. The equivalent circuit parameters were extracted by fitting the model to the measured data (see figure 3.11). In all cases the junction capacitance occurs due to abrupt change in the conductor shape which modifies the electric field distribution near the discontinuity causing change in capacitance. A further contribution to the capacitance comes from the air bridges positioned at the junction. The shunt resistor represents the substrate leakage effect. The extracted transmission line values represents the region of the discontinuity within the air bridges represented by shaded region in figure 3.9 & 3.10.
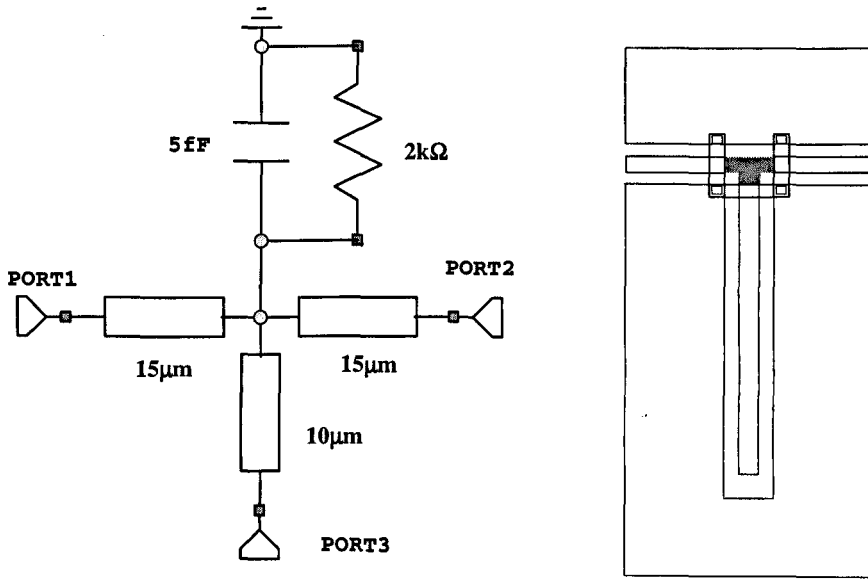
Figure 3.9: Layout of open circuited tee and the equivalent circuit model of the shaded layout
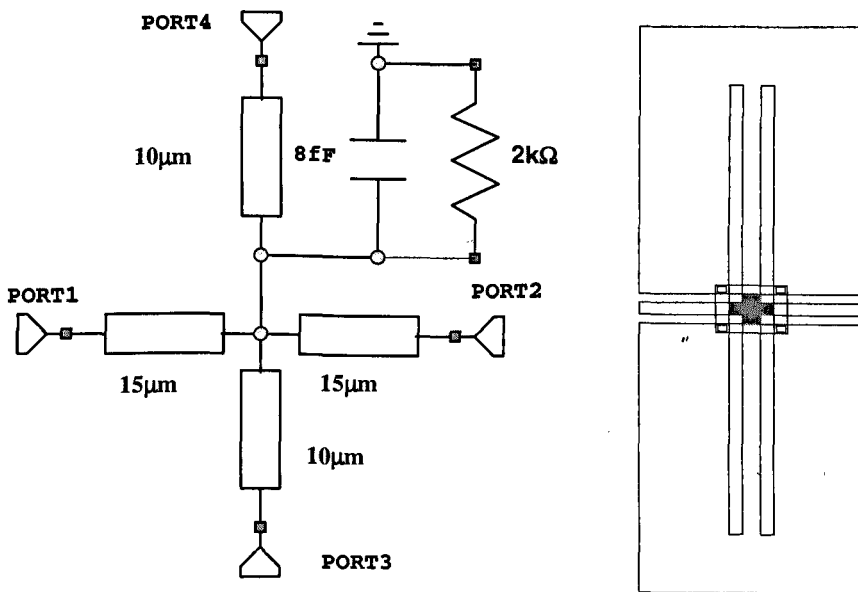

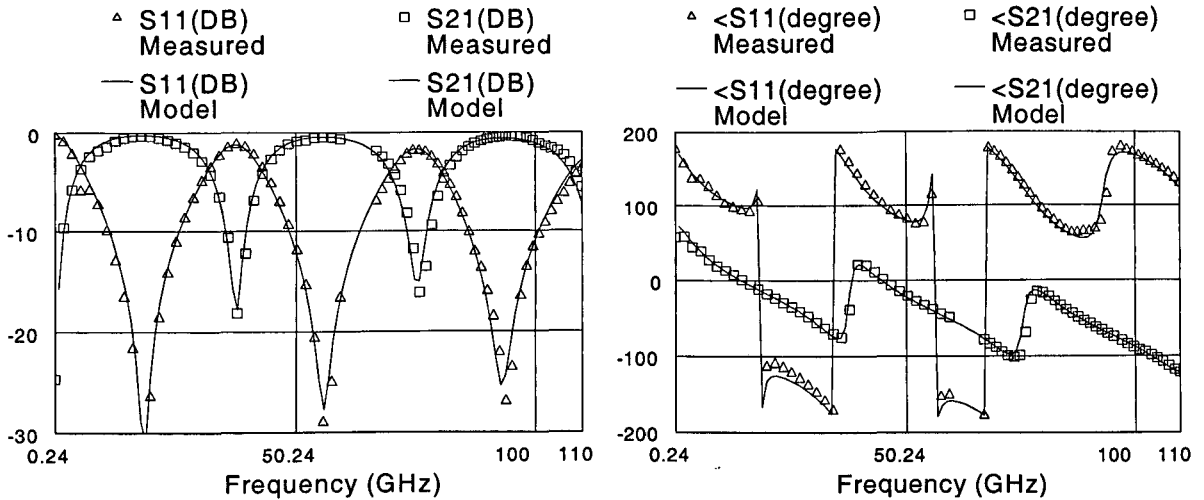*Figure 3.10: Layout and equivalent circuit model of a cross.*

ᐃ S11(DB) Measured	▫ S21(DB) Measured	ᐃ <S11(degree) Measured	▫ <S21(degree) Measured
— S11(DB) Model	— S21(DB) Model	— <S11(degree) Model	— <S21(degree) Model

Figure 3.11: Example of the match between measured and modeled open tee structure with stub length of 1500μm.

3.7 CPW Capacitors

Capacitors are very common in microwave circuits and are used in matching networks, filters and couplers as well as in RF bypassing and DC blocking applications. Two types of capacitors, Metal Insulator Metal (MIM) and inter digital capacitors were designed, fabricated and characterised in this work. The choice of capacitor depends on the size of the capacitance required, the size limits imposed by MMIC design, and the frequency of operation. Normally interdigital capacitors are used when very small capacitance values are required in the circuit. MIM capacitors can be made by sandwiching a thin" low loss dielectric film between two metal plates as illustrated in figure 3.12. Silicon nitride (Si_3N_4) was used as the insulator in the standard MMIC process (see chapter 2). The capacitance of MIM structures can be calculated using

$$C = \varepsilon_0 \varepsilon_r A/d \qquad\qquad\qquad \textit{Equation 3.11}$$

ε_0 = free space permittivity
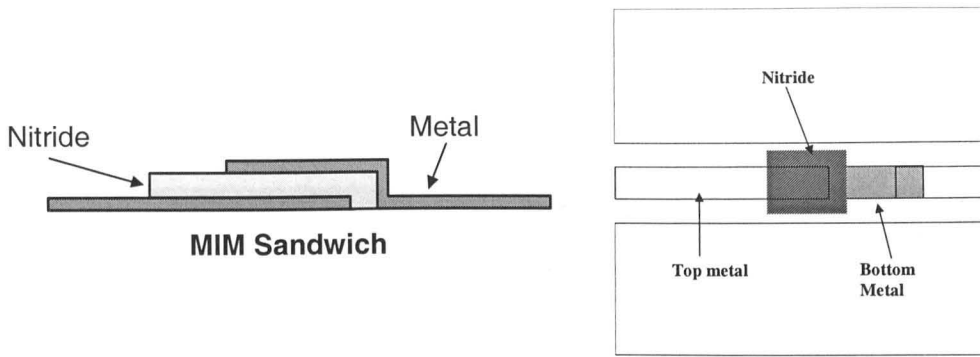
Figure 3.12: Cross section of an MIM capacitor and layout of series capacitor

Where A is the area of the top plate and d is the thickness of silicon nitride. The silicon nitride thickness and relative permittivity are 150nm and 12.2 respectively. A large range of MIM capacitors in both shunt and series form were fabricated and characterized. A shunt capacitor in CPW is achieved by connecting the bottom plate to the CPW ground planes. A range of capacitors and their equivalent circuit values are summarized in table 3.1 & 3.2.
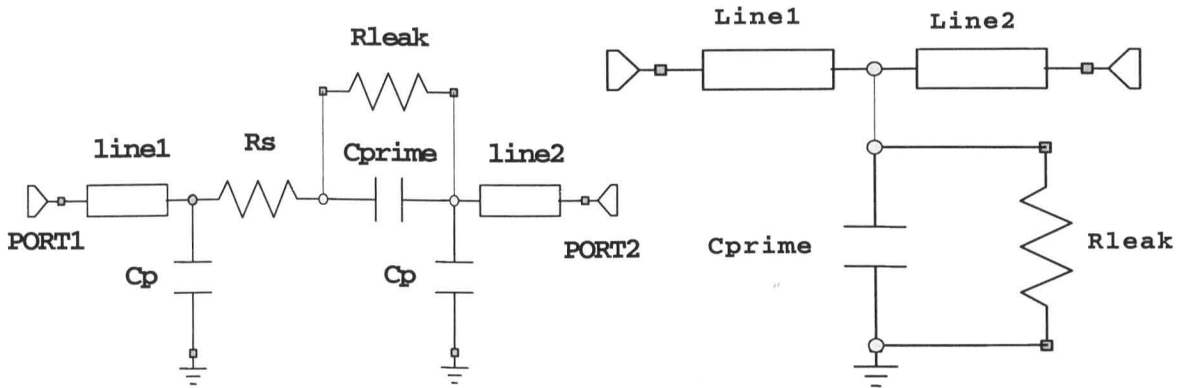
Figure 3.13: Equivalent circuit model for both series and shunt MIM capacitors

The series MIM equivalent circuit model shown in figure 3.13 takes account of the dominant parasitic effects. The transmission lines at either end take account of distributed effects of the capacitor. The dielectric film loss of the capacitor is represented by Rleak. Cprime is the extracted value of the capacitor. The series

resistor Rs represents the loss due to the bottom plate of the capacitor, which is thin compared to skin depth. The fringing capacitance of the top plate is given by Cp in the circuit model.

Design Cap(fF)	Cprime (fF)	Cp (fF)	Rs (ohm)	Rleak (ohm)
38	40	1	2	5k
77	77	1	2	5k
116	110	1	2	3k
154	152	1	2	2.5k
195	188	1	1	1.7k
235	220	1	1	1k
465	415	1	1	700

Table 5.1: Shows values of extracted equivalent circuit parameters of different sized series MIM capacitors.
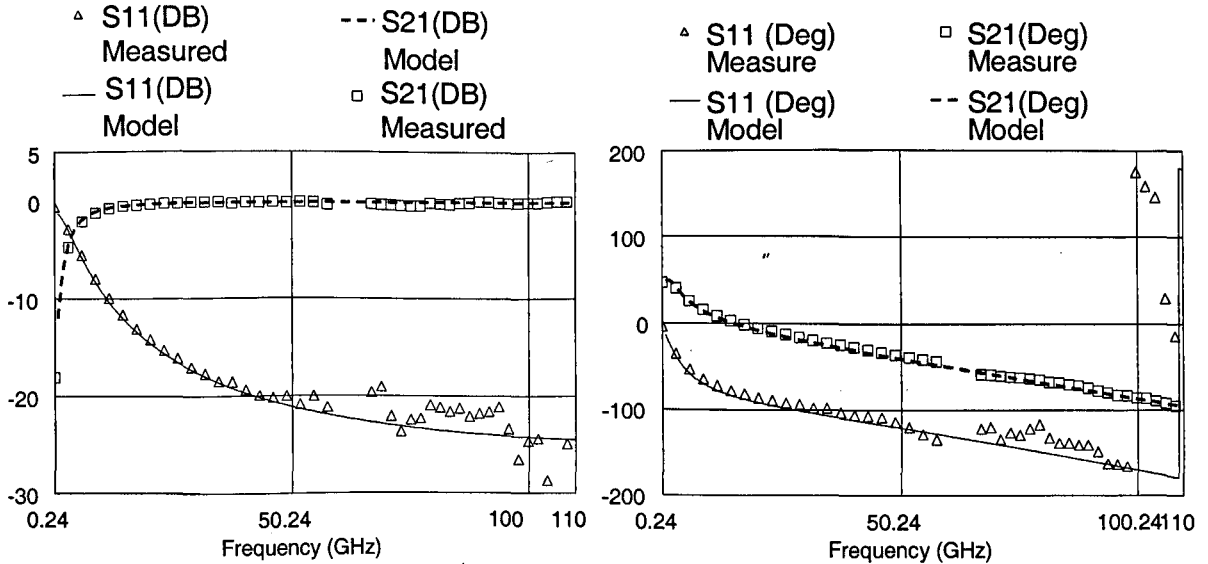
Figure 3.14: Shows the measured and modeled response of a 500fF series capacitor

Cap Design (fF)	Cprime (fF)	Rleak (ohm)
40	45	4000
75	77	3000
100	115	2000
150	145	1000
200	180	1000
250	230	1000
500	420	1000

Table 3.2 Equivalent circuit shunt capacitor data.
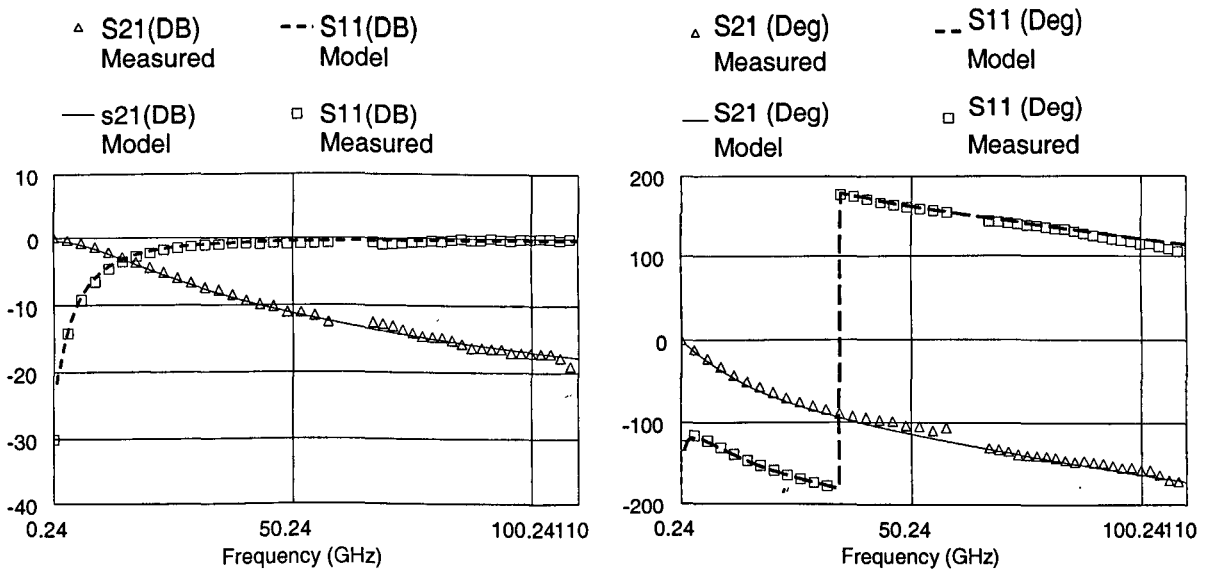
Figure 3.15: Measured & modeled response of 500 fF shunt capacitor

Interdigital capacitors use the coupling of closely placed transmission lines to generate capacitances as shown in figure 3.16. The capacitance can be increased by increasing the number of fingers, the length of the fingers, or decreasing the gap between the transmission lines. They are useful in circuits where small

capacitance values are required and it helps to reduce the number of fabrication steps since there is no need for a dielectric layer.
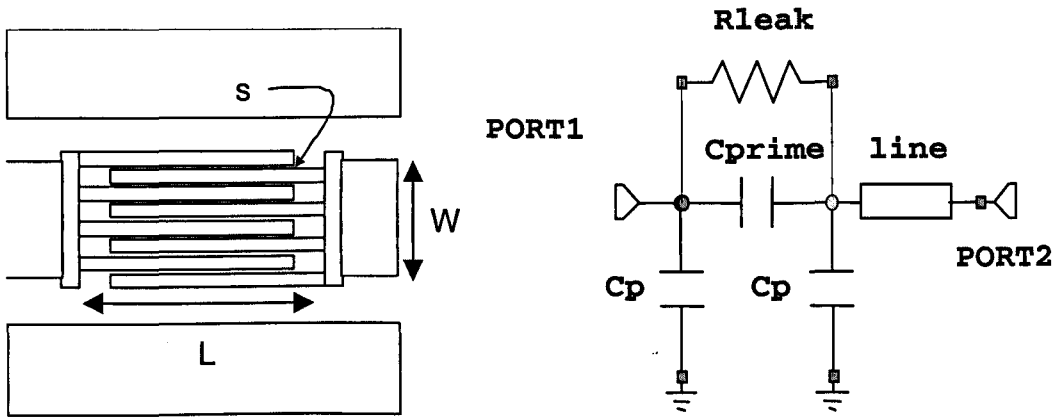
Figure 3.16: Layout and equivalent circuit model of interdigital capacitor

The capacitance of N interdigitated metal strips coupled together of length l and total width w can estimated as following

$$C(pF) = \frac{\xi_r + 1}{w} l\left[(N - 3)A_1 + A_2\right] \qquad \text{Equation 3.12}$$

Where A_1 and A_2 are given by *8.85E-12*w* (pF) and *9.92E-12*w* (pF) respectively [R3.15]. This approximation is valid only when substrate thickness is large compared to spacing of metal strips. The maximum value is limited by the physical size and the maximum useable frequency is limited by the distributed nature of the fingers.

The capacitors characterized in this project had constant lines width, gap and number of fingers. The capacitance was changed by increasing the length of lines. The equivalent circuit model shown in figure 3.16 was fitted to the measured data (see figure 3.17) and the parameters extracted are given in table 3.3.

Design cap(fF)	Cprime (fF)	Cp (fF)	Rleak (Ω)	Line (μm)
2.5	4	1	5000	20
5	5.5	1	5000	45
10	10	1	5000	70
12.5	17	1	5000	100

Table 5.3: Equivalent circuit parameter data for Interdigital capacitor
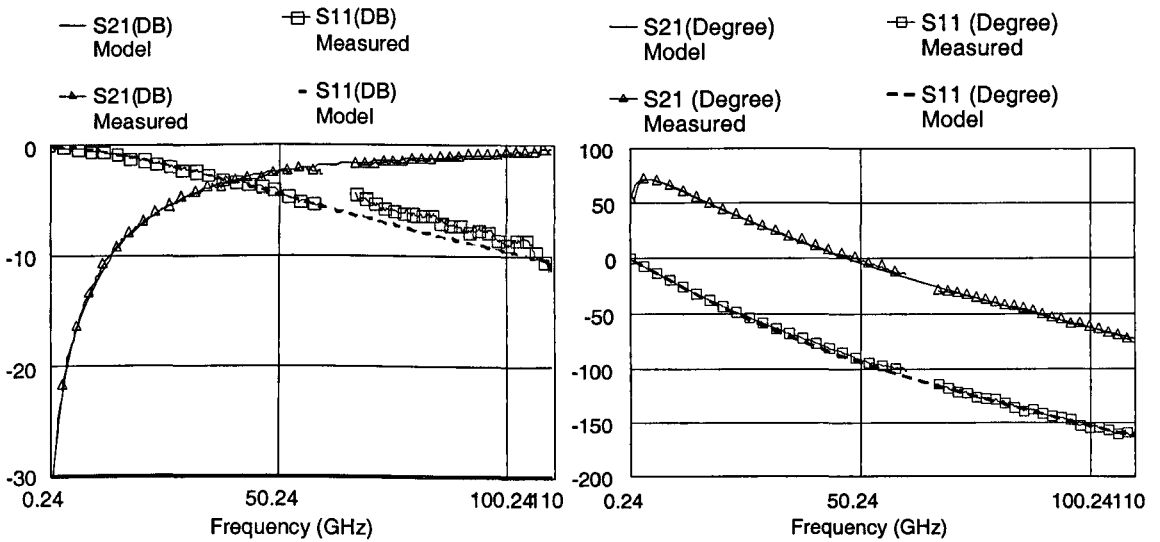
Figure 3.17: Measured & modeled data of 10fF interdigital capacitor

3.8 Thin Film Resistors

Resistors perform a number of tasks in a MMIC chip ranging from matching networks and biasing to power division and termination. NiCr based thin film resistors were characterized and used in passive and active circuits. Figure 3.18 shows the layout of a shunt resistor and equivalent circuit that was used to characterize this resistor. The resistor layout contains two 100 Ω resistors connected in parallel to generate a 50 Ω load. The model consists of a

transmission line, which represents the distributed nature of the resistor and shunt parasitic capacitance.
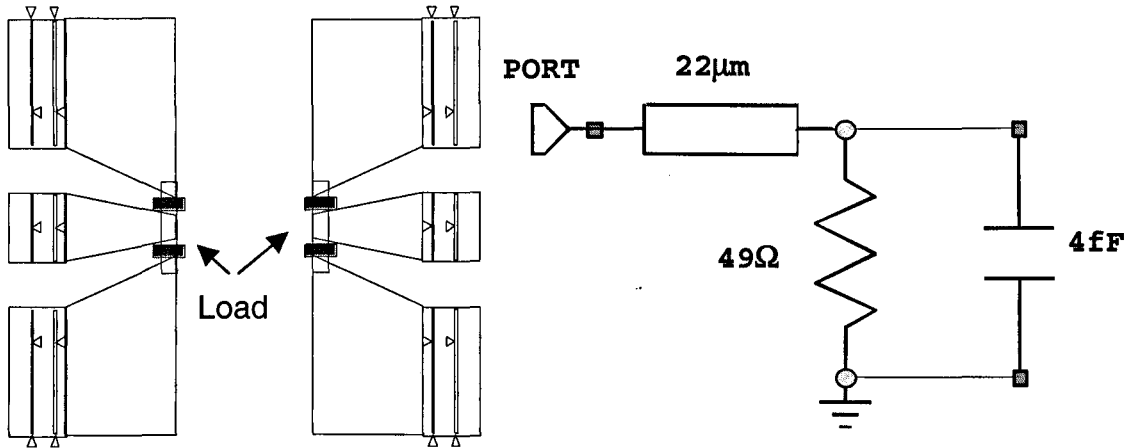
Figure 3.18: Layout and Equivalent circuit model of a shunt NiCr resistor.
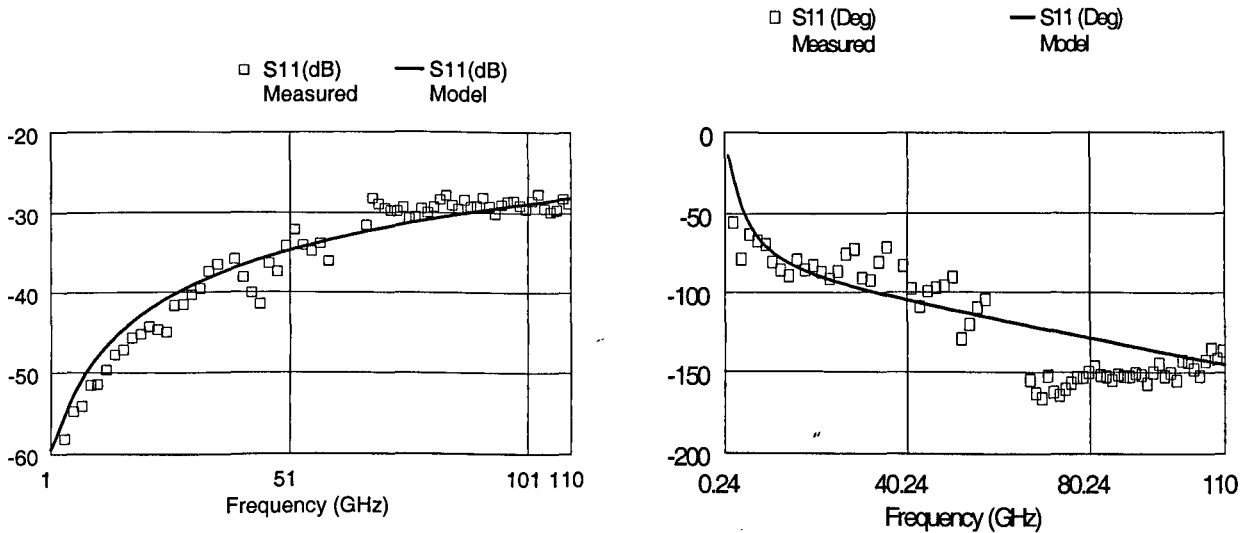
Figure 3.19: Measured & modeled performance of a 50 ohm shunt resistor

3.9 Summary

This chapter has outlined the basic principles of coplanar waveguide. High frequency measurements and calibration techniques are discussed. A number of passive elements are designed and characterized. The extracted equivalent circuit models have been shown to be valid in the W-band frequency range.

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4   MMIC InP based lattice matched HEMT

4.1   Introduction

The High Electron Mobility Transistor (HEMT) has become the most popular active device for MMICs at millimeter-wave frequencies due to its excellent low noise and high gain performance. This chapter outlines the general operating principles of a HEMT before describing in detail the behavior of InP lattice matched (LM) HEMTs, highlighting their relative advantages & disadvantages in terms of DC and RF performance. The RF performance of InP based HEMTs with two different T-gate processes are compared.

4.2 HEMT Structure
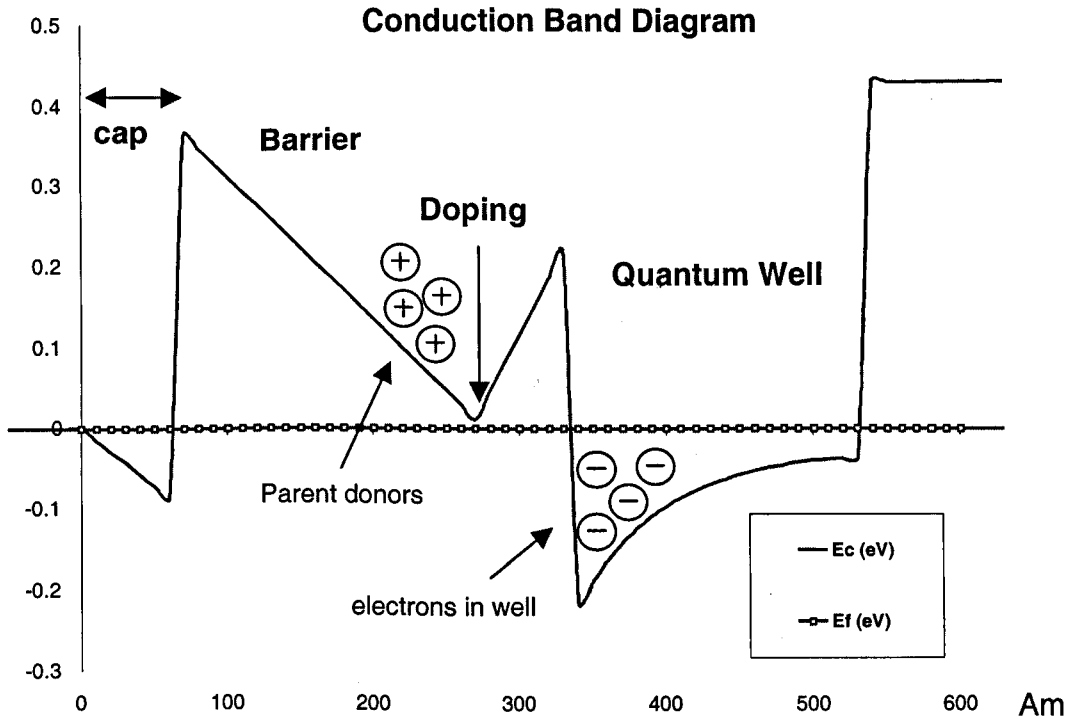
Figure 4.1: 1D Conduction band diagram of InP LM HEMT using Greg Schnieder's band diagram calculator [R4.1]

The High Electron Mobility Transistor (HEMT) belongs to family of field effect transistors (FET) where current flow between two terminals (source and drain) is modulated by a third terminal (gate). The HEMT is very similar in structure to a MESFET but the major difference is that the channel is realised from a sheet of tightly confined charge in a quantum well which is formed by sandwiching a low-bandgap material between two high bandgap materials (see Figure 4.1). The upper high bandgap material is doped while the narrow band gap material is undoped. The potential energy of the conduction band in the quantum well is lower compared to the barrier material allowing the electrons to transfer to the lower energy region (see figure 4.1). This charge transfer is opposed by the electric field formed from the separated electron and donor ions. The electric field however

alters the conduction band potential causing it to bend and confines the mobile carriers in triangular well. The electrons in the quantum well are separated from their parent donors, experiencing reduced ionized impurity scattering, which results in improved mobility. A second high band gap material is situated below the quantum well to confine the carriers in the well. This is illustrated in figure 4.1, which is the calculated conduction band diagram for the InP LM HEMT material used in this project.
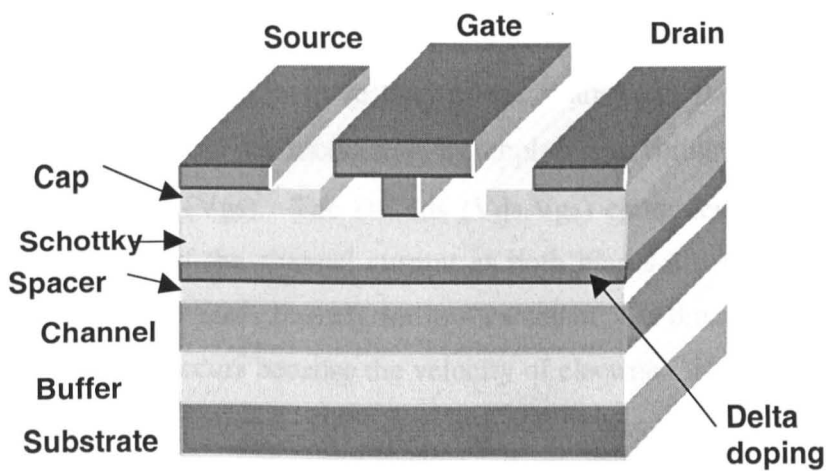
Figure 4.2: Cross section of a generic HEMT Device

A typical HEMT structure showing all MBE grown layers and nano-fabricated contacts is shown in figure 4.2. The top layer of the HEMT vertical architecture is known as the cap, which is highly doped to form the low resistance Ohmic source-drain contacts. The cap must be etched away in the region around the gate before gate deposition to ensure that conduction from source to drain is solely through the charge sheet formed in the high mobility channel. In addition this enables the Schottky gate contact to be formed on relatively low doping concentration material to minimize gate leakage current. The doping layer, which supplies charge to the channel is placed in a very thin layer (δ doping layer) to reduce the gate-channel separation and also provide good charge control. The spacer layer is undoped to provide spatial separation between the δ doped donor layer and the channel. This

reduces the Coulomb scattering, which improves the carrier mobility in the channel.

The buffer layer provides a conduction band discontinuity to the channel, which helps keep the carriers in the channel and offers a clean and defect free interface to the channel. Any carriers escaping to the buffer layer cause an increase in buffer current resulting in lowering the output resistance of the HEMT and reducing the voltage gain [R4.2].

4.3 HEMT Operation

In an n-type depletion mode HEMT, current is driven from source to drain through the channel by applying a positive bias to the drain with the source grounded (Vds). This current can be modulated by applying a voltage to the gate with respect to the source (Vgs). The DC Ids (Vds,Vgs) characteristics in figure 4.3 show the behaviour of the channel current as both biases are varied. The drain-source current, Ids increases linearly for low values of Vds but saturates for higher voltage levels. This occurs because the velocity of electrons in the channel linearly increases with rising electric field but beyond certain electric field strength, complex scattering mechanisms in the device channel cause velocity saturation, which results in current saturation [R4.3].
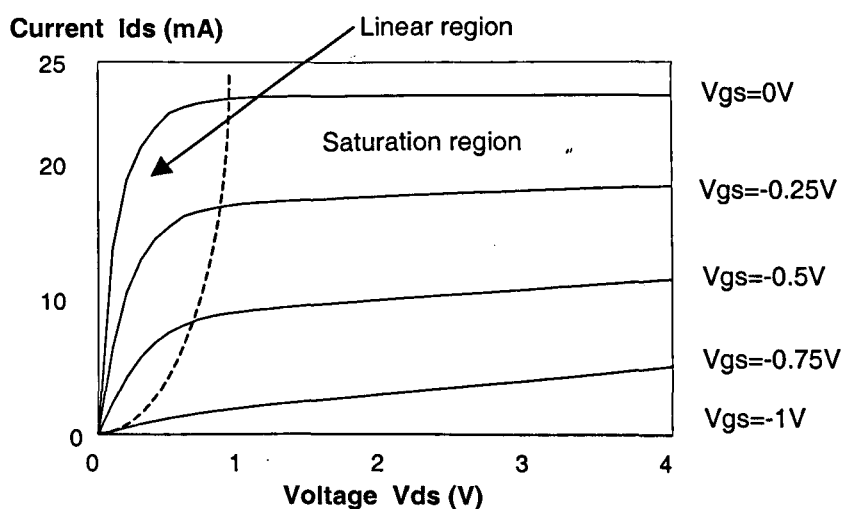
Figure 4.3: I-V characteristics of an ideal HEMT

Negative gate bias causes the depletion of carriers for the channel underneath the Schottky contact. This channel electron concentration is reduced as more negative voltage is applied, until it is completely removed at which time, no current can flow. This is shown in I-V characteristics of figure 4.3, where Ids becomes smaller with increasingly negative gate voltage. When the channel is completely removed by the reverse bias applied to the gate, it is referred to as "pinched off" state of the HEMT.

In the saturation region the drain current is independent of Vds and in a simple 1-dimension approximation, assuming free carriers move with uniform velocity through all parts of transistor, this can be written as

$$Ids = qn_s v_{eff} Z = Q_s v_{eff} / L_g \qquad\qquad Equation\ 4.1$$

Where

$$Q_s = q\, Z\, L_g\, n_s \qquad\qquad Equation\ 4.2$$

q = electronic charge

n_s = electron concentration in the channel

v_{eff} = effective velocity of electrons in the channel

Z = device width

L_g = gate length of HEMT

Q_s = Sheet charge of the channel

The rate of change of drain current with respect to change in gate voltage is an important parameter as it defines the gain of the device. The transconductance gm can be written as

$$gm = \frac{dI_{ds}}{dV_{gs}}\bigg|_{Vds=const} \qquad\qquad Equation\ 4.3$$

The depletion region under the gate can be treated as parallel plate capacitor with capacitance C_g given by

$$C_g = \frac{dQs}{dV_{gs}} = \frac{L_g Z \varepsilon}{d} \qquad \textit{Equation 4.4}$$

Where d is the separation between gate and the electrons in the channel and ε is the dielectric constant of the semiconductor between the gate and the channel. From equation 4.1 and 4.4, the following expression of intrinsic gm results

$$gm = \frac{dI_{ds}}{dV_{gs}} = \frac{Z v_{eff} \varepsilon}{d} = \frac{C_g v_{eff}}{L_g} \qquad \textit{Equation 4.5}$$

These relationships illustrate that to achieve high gm, the gate to channel distance must be reduced. This however, results in an increase in the gate capacitance. The gate capacitance can be reduced by shrinking the gate length.

In reality, when a HEMT is operated in saturation, the drain current is not constant with drain voltage but increases linearly. The rate of change of drain current with drain voltage is the output conductance g_{ds} of the transistor.

$$g_{ds} = \frac{dI_{ds}}{dV_{ds}} = \frac{1}{R_{ds}}\Big|_{Vgs=const} \qquad \textit{Equation 4.6}$$

The relation of gm to gds is the voltage gain of the HEMT which is related to the power gain

$$Av = \frac{g_m}{g_{ds}} = \frac{dV_{ds}}{dV_{gs}} \qquad \textit{Equation 4.7}$$

The measured gm at the device terminals or extrinsic gm is influenced by parasitic resistances, especially by the source resistance. The relationship between the two can easily be arrived at by considering the voltage drop across the source resistance as shown in figure 4.4.
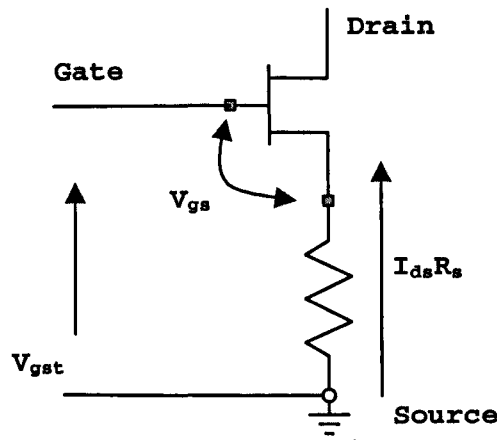
Figure 4.4: Illustration of voltages in external gm measurement.

$$Vgst = Vgs + Ids\ Rs \qquad\qquad Equation\ 4.8$$

Where *Vgst* is the external gate voltage applied, Vgs is the gate source voltage drop. Differentiating equation 4.8 with respect drain current yields

$$g_{mt} = \frac{g_m}{\left(1 + g_m R_s\right)} \qquad\qquad Equation\ 4.9$$

Here gm is the internal device transconductance and g_{mt} is the extrinsic, measured and accessible value, which is always lower than the intrinsic transconductance.

4.4   Lattice matched HEMT Structure

The vertical architecture of the HEMT used in this project is very similar to the one used by Ngyuen to demonstrate 50nm gate devices with good pinch off and uniform transconductance characteristics [R4.4]. The complete structure is shown in Figure 4.5

7nm 3×10^{18} cm^{-3} Si doped In$_{0.53}$Ga$_{0.47}$As **Cap** layer
20nm In$_{0.52}$Al$_{0.48}$As **Barrier**
5×10^{12} cm^{-2} Si **Delta Doping layer**
6 nm In$_{0.52}$Al$_{0.48}$As **Spacer**
20 nm In$_{0.53}$Ga$_{0.47}$As **Channel**
96 nm In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As **Superlattice Buffer**
250 nm In$_{0.52}$Al$_{0.48}$As **Buffer**
InP substrate

Figure 4.5: Layer stack of Lattice matched InP HEMT.

The device stack is built around the In$_{0.53}$Ga$_{0.47}$As channel, which has excellent electron transport properties, including low effective mass, high mobility, and a large energy separation between the lowest two valleys in the conduction band [R4.5]. Along with supreme transport properties, it is lattice matched to both In$_{0.52}$Al$_{0.48}$As, a high bandgap III-V semiconductor that enables the formation of a heterostructure, and to InP. Lattice matching prevents strain in the system, which avoids dislocations that can cause severe damage to the HEMT performance and reproducibility [R4.6]. A 6 nm spacer In$_{0.52}$Al$_{0.48}$As is grown between the channel and upper barrier to separate the free electrons from their parent donors. Nguyen has experimentally optimised the thickness of device layers by following the scaling rule of maintaining the 3:1 ratio of gate length and gate to channel separation [R4.7].

The cap is made from thin low band gap In$_{0.53}$Ga$_{0.48}$As and high Si doping for the formation of low resistance Ohmic contacts. An In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As super lattice is used to provide a smooth interface between the channel and the lower barrier [R4.8]. In$_{0.52}$Al$_{0.48}$As was used as both the upper and lower barrier for the channel confinement. The conduction band discontinuity between the channel and barriers is around 0.5 eV in this lattice matched HEMT, considerably larger than in

Pseudomorphic HEMT on GaAs. The lower barrier is relatively thick to keep the surface defects of the substrate away from the channel. The conduction band diagram of this structure is shown in figure 4.1.

4.5 DC characteristics

Devices with gate lengths of 120 nm and gate widths of 100 μm, fabricated following the process flow described in chapter 2 were characterized using the experimental setup illustrated in figure 3.2 in chapter 3. The I-V characteristics of figure 4.6 are very typical of an InP LM HEMT device. The small source drain saturation voltage indicates the material has high mobility. The linear increase of Ids with Vds in saturation region indicates a finite output resistance. The measured drain saturation current Idss is around 300mA/mm and the output conductance is 200mS/mm.
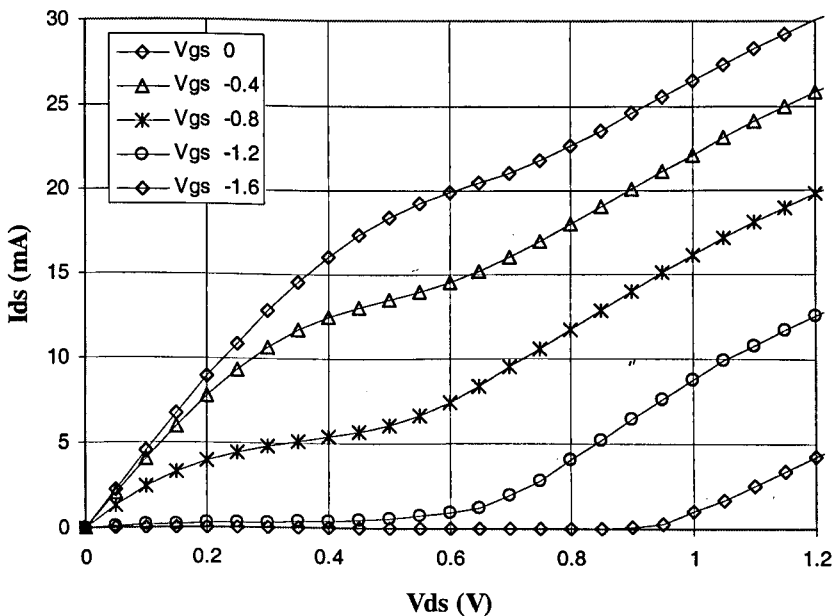
Figure 4.6: I-V characteristics of a InP LMHEMT (wafer no. A1270)

The devices suffer from the "kink effect" in saturation region, where a sudden rise in drain current occurs at a certain drain-source voltage leading to high output conductance, high gm compression and poor linearity. Studies of kink in InGaAs channel HEMTs have suggested that impact ionization is responsible for this phenomenon [R4.9]. Impact ionization is more common in low band gap materials like $In_{0.53}Ga_{0.47}As$ where the electron-hole generation rate is proportional to drain source current and impact ionization coefficient [R4.10]. At the kink voltage, the electric field at the drain end of gate is strong enough to force the holes to tunnel through to the gate contact. The gate leakage current is the combination of this hole current plus electron tunneling current. As the bandgap decreases with increasing indium concentration in the channel, the gate current will become more significant.
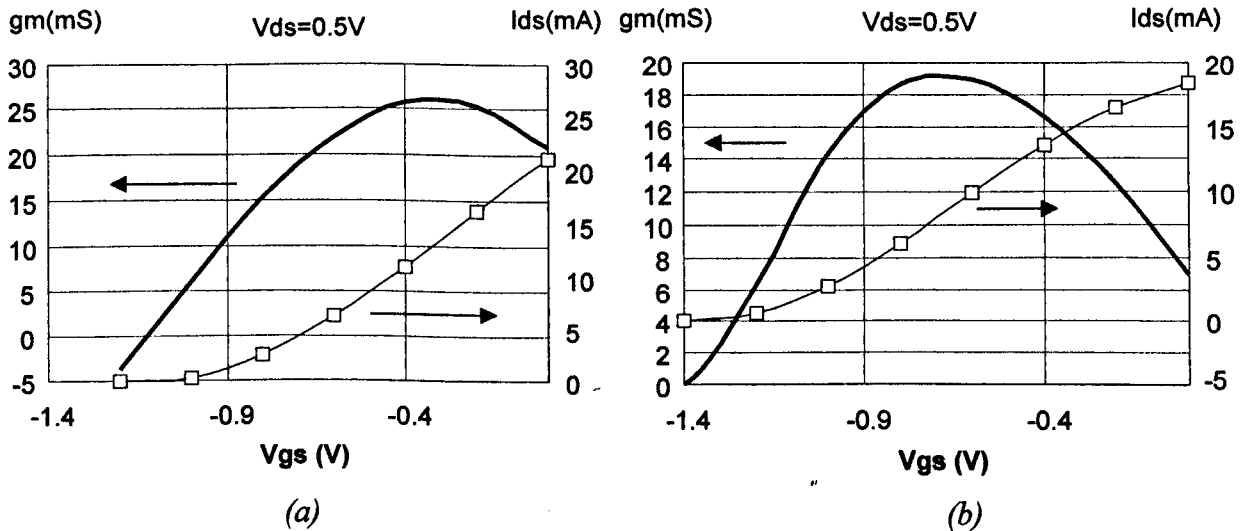
Figure 4.7: Shows gm of two 100 μm devices made on same material but processed at different times. It is believed that graph (a) has a deeper recess compared to (b) because it shows higher gm and more positive peak gm voltage.

DC transconductance of HEMTs is always measured before RF measurements to assess the performance of the device. Typical extrinsic transconductance curves for LM HEMTs are shown in figure 4.7. Transconductance is very much related to the shape of the recess where a deep recess results in higher transconductance.

This relationship is shown in equation 4.6, where the transconductance increases by reducing the gap between the free carriers in the channel and Schottky gate contact. Figure 4.7 illustrates this with gm of two devices etched at different times with different recess depths resulting in different gm. Also the gate voltage at which the peak gm occurs becomes more positive as the recess becomes deeper.

4.6 HEMT High Frequency Behaviour

DC characteristics are useful for analyzing the potential of the transistor but the real advantage of the LM InP HEMT comes at high frequency. Perhaps the most useful function of the LM InP HEMT is the ability to provide very large gain at very high frequencies. When a HEMT is operated in common source mode (i.e. source grounded, gate and drain bias applied with respect to source to set the operating condition), an RF signal applied to the gate will be amplified and output at the drain.
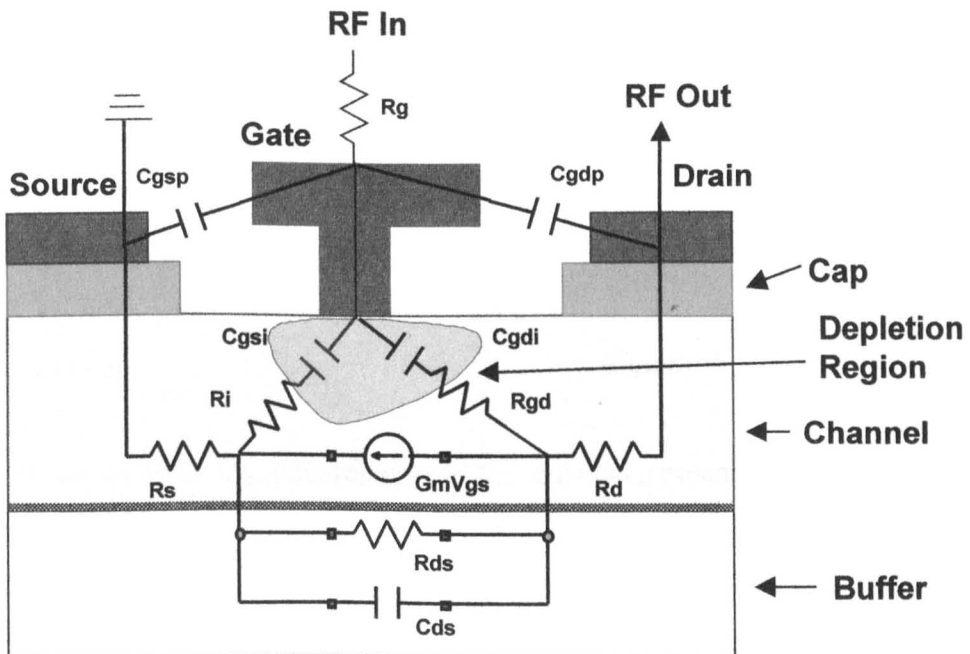
Figure 4.8: Equivalent circuit model superimposed on layer structure of HEMT

The response of the HEMT at microwave frequencies can be modeled by lumped circuit elements, which fall into two categories. One of them is the intrinsic part of HEMT, which is section of the HEMT directly underneath the gate contact that has been briefly mentioned in the previous section. This intrinsic HEMT cannot be electrically connected to the outside environment without incurring losses. These lossy elements are referred to as the extrinsic part of the HEMT or the parasitics and they determine the percentage of intrinsic HEMT performance that can be measured externally. Figure 4.8 shows the equivalent circuit model superimposed onto the HEMT layer structure in such a way that it shows the origin of each circuit element.

4.7 RF Equivalent Circuit Elements

The voltage controlled current source embodies the gain of the HEMT, which is the product of intrinsic gm and voltage drop across the gate source capacitance. The RF gm has been shown to be dependant on the recess shape and is coupled to gate capacitance with deeper recess resulting in high values of both the transconductance and gate capacitance. The only way of achieving high gm with low gate source capacitance is to reduce the gate length of the HEMT. C_{gs} represents the gate source capacitance and consists of contributions from gate to channel capacitance (C_{gsi}) and small fringing capacitance that exists between gate and source (C_{gsp}) shown figure 4.8.

$$C_{gs} = C_{gsi} + C_{gsp}$$ *Equation 4.10*

Ri is in series with C_{gs} and represents the channel resistance. The gate-drain capacitance is the sum of C_{gdi} and C_{gdp} as shown in figure 4.8 where C_{gdi} represents the depletion region capacitance caused by the drain bias beyond the drain end of the gate and C_{gdp} is the fringe capacitance between gate and drain.

$$C_{gd} = C_{gdi} + C_{gdp}$$ *Equation 4.11*

Rds or gds, parallel to the current source is the output resistance of the HEMT. It shows the extent to which drain current is controlled by the drain source voltage, an undesirable effect. The conductance can be suppressed by having good electron confinement in the channel, large conduction band discontinuities at both upper and lower barriers and maintaining the 3:1 gate to channel separation ratio as mentioned by Golio [R4.11]. Contribution to gds coming from the space transfer of carriers from channel into the cap region between gate and drain can be reduced by having a larger recess offset on the drain side of the gate [R4.12]. The capacitance Cds originates from two highly doped source and drain cap regions separated by the depletion region.

The source resistance Rs has contributions from Ohmic contact resistance and the sheet resistance of the semiconductor between source and gate contacts. Rs is minimised by having low resistance Ohmic contacts along with the semiconductor having high mobility and carrier concentration and having a narrow gate recess. Rd representing the drain resistance, similar to Rs in nature but occurs on the drain side of the gate.

Rg is the gate metalisation resistance where a short gate length is required to produce small gate capacitance, and thus a high speed device. However, such a structure would have a large resistance, which would compromise the device performance particularly at high frequencies. To over come this, a T-gate is used which has a small foot print for high gm plus a large head to avoid large gate resistance. An equivalent circuit model with intrinsic and extrinsic elements is shown in figure 4.8.

4.8 RF Figures of Merit

4.8.1 Transition Frequency

The transition frequency (f_T) occurs when the short circuit current gain falls to unity. To calculate the f_T, the output of the equivalent circuit is shorted and current gain I_{out}/I_{in} is evaluated. Equation 4.12 gives an expression for f_T, which has been derived from equivalent circuit model of figure 4.9 [R4.13].
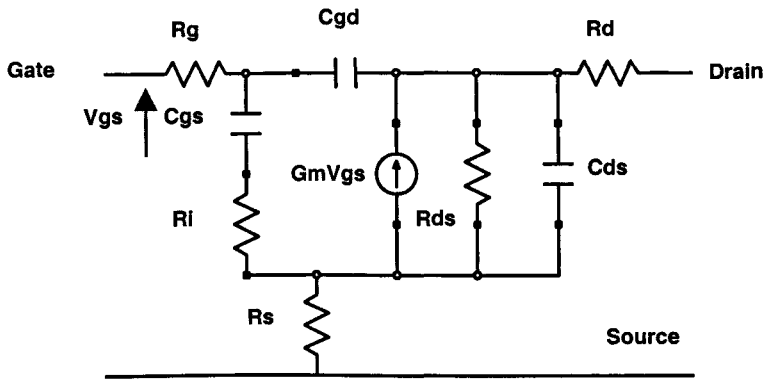
Figure 4.9: Extrinsic equivalent circuit model used for deriving the expression in equation 4.12

$$f_T = \frac{gm}{2\pi\left[\left(C_{gs} + C_{gd}\right)\left(1 + \dfrac{Rs + Rd}{Rds}\right) + gmC_{gd}\left(Rs + Rd\right)\right]}$$ *Equation 4.12*

4.8.2   Maximum Frequency of operation

Maximum frequency of oscillation (f_{max}) is a more relevant figure of merit for design engineers. It is the frequency where the power gain falls to unity. It can be expressed by equation 4.13 derived from equivalent circuit in figure 4.9 [R4.14, 4.15].

$$f_{max} = \frac{f_T}{2\sqrt{\dfrac{Rg + Ri + Rs}{Rds} + 2\pi f_T RgCgd}}$$ *Equation 4.13*

Maximum Available Gain (MAG), is the power gain of a HEMT with both input and output simultaneously matched [R4.16]

$$MAG = \frac{\left(\frac{f_T}{f}\right)^2}{4\left[\left(\frac{Rg + Ri + Rs}{Rds}\right) + 4\pi f_T Cgd(2Rg + Ri + Rs)\right]}$$ *Equation 4.14*

These relationships show that to get high MAG, low parasitic Rg, Ri, Rs and high f_T and Rds are needed. For high f_T, low gate capacitance and high gm is required which implies high effective velocity in the material and short gate length.

4.8.3   Noise Figure

The noise figure of a HEMT (NF) is ratio of signal to noise ratio at the input to the signal to noise ratio at the output. A low frequency approximation for noise figure exists which to some extent indicates the main sources of noise in the HEMT [R4.17].

$$NF(dB) = 10\log[1 + 2\pi K f C_{gs}\sqrt{\frac{R_s + R_g}{gm}}]$$ *Equation 4.15*

K is the correction factor in the expression
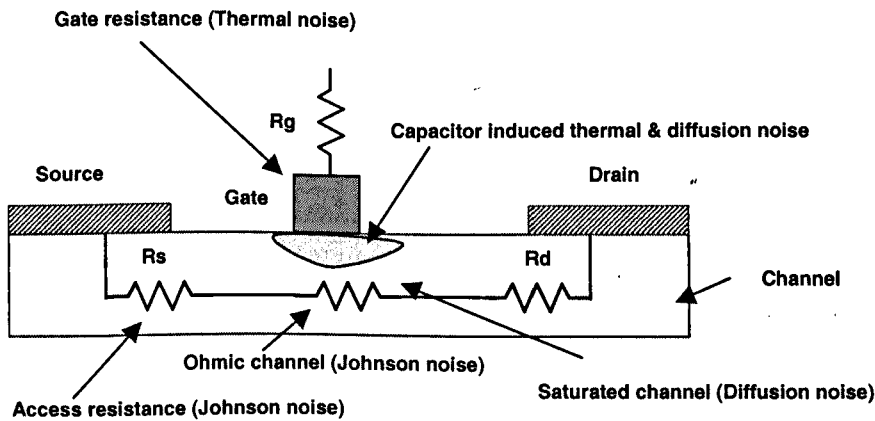
Figure 4.10: Noise sources in a HEMT structure [R4.18]

The InP based HEMT has demonstrated the best noise figure ever reported for a high frequency device. This is possible due to the excellent material properties of

InGaAs. Equation 4.15 illustrates that to achieve low noise figure, the HEMTs require good material transport properties along with short gate length, low gate resistance, small source-drain gap and low Ohmic contact resistances.

4.9   Equivalent Circuit Element Extraction

The complete equivalent circuit model containing all the parasitic effects due to bond pad connections is shown in figure 4.11.

Figure 4.11: Complete equivalent circuit model of an InP HEMT.

The gate inductance L_g, drain inductance L_d and source inductance L_s arise from metal pads. Their typical values are dependent on the size and shape of the pads. Similarly C_{pg}, C_{pd} and C_{pgd} are parasitic capacitance generated because of relatively large areas of metal [R4.19].

In this work equivalent circuit models were extracted using two different software packages. Initially all the models were extracted using Lysander, an in-house bias dependant HEMT small signal model extractor [R4.20]. For more accurate comparison between HEMT devices, equivalent circuits were extracted using methods suggested by Tayrani [R4.21] and Beroth [R4.22] and the final

optimizations were performed using RF simulators such as Microwave Office or EESOF Touchstone.

All the parasitics were extracted using Tayrani's methods of unbiased and pinched-off HEMTs [R4.23]. This method avoids measurements with forward Schottky biasing thus avoiding large gate currents, which can lead to deterioration in HEMT device performance. The equivalent resistances and inductances are extracted at zero bias condition. The equivalent circuit reduces to the following
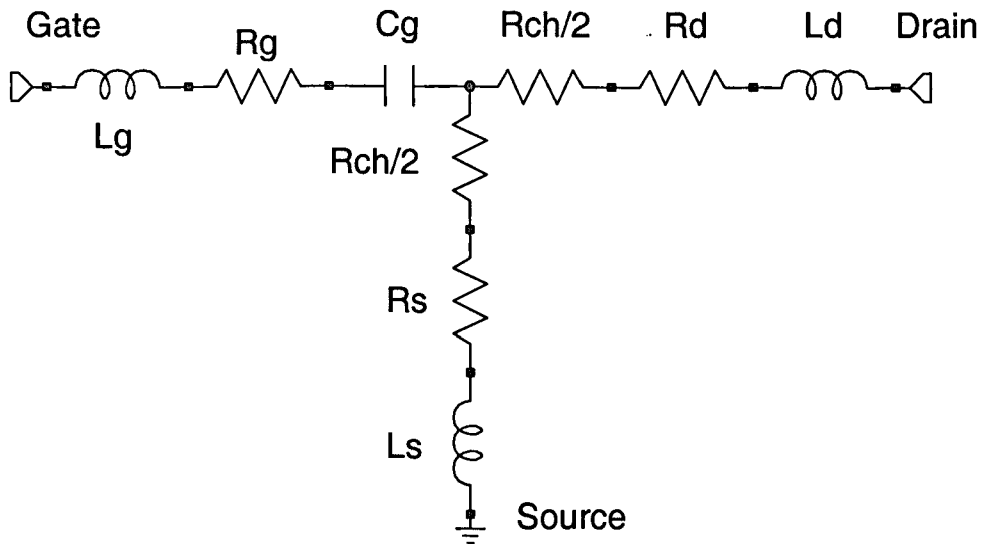
Figure 4.12: Equivalent circuit model at Vds=0 and Vgs=0

The element values can be determined from on-wafer S-parameter measurements. The 2 port S-parameters were measured after an LRL calibration as described in chapter 3. These measurements were converted into z parameters using standard conversion equations [R4.24]. The relationship of equivalent circuit parameters to z parameters are given as follows

$$Z_{11} = Rs + 0.5Rch + Rg + j\left[\omega(Lg + Ls) - \frac{1}{\omega Cg}\right] \qquad \text{Equation 4.16}$$

$$Z_{12} = Z_{21} = Rs + 0.5Rch + j\omega Ls \qquad \text{Equation 4.17}$$

$$Z_{22} = Rs + Rch + Rd + j\omega(Ld + Ls)$$ *Equation 4.18*

The inductances are determined from the imaginary part of unbiased Z-parameters. L_s and L_d can be easily worked out from the equation 4.17 and 4.18 where for Lg, two frequency points are taken to solve for Cg and Lg in equation 4.16. In the pinched-off condition, with zero drain bias, the equivalent circuit reduces to figure 4.13.
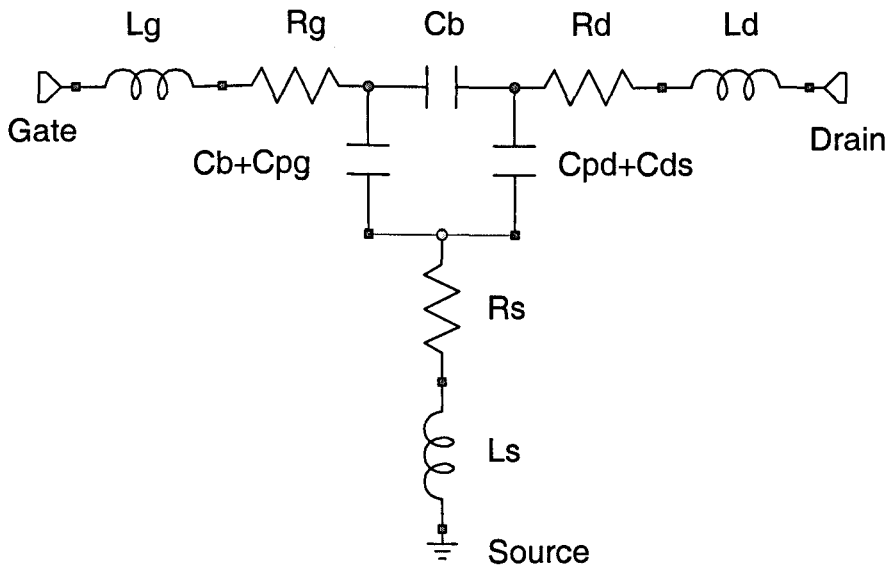
Figure 4.13: Equivalent circuit of pinched-off HEMT

The pinched-off HEMT measurements give us the following parameters

$$\mathrm{Re}\{Z_{11}\} = Rs + Rg$$ *Equation 4.19*

$$\mathrm{Re}\{Z_{12}\} = Rs$$ *Equation 4.20*

$$Cb = -\frac{\mathrm{Im}\{Y_{12}\}}{\omega}$$ *Equation 4.21*

$$Cpg = \frac{\text{Im}\{Y_{11}\}}{\omega} - 2Cb \qquad\qquad Equation\ 4.22$$

$$Cds + Cpd = \frac{\text{Im}\{Y_{22}\}}{\omega} - Cb \qquad\qquad Equation\ 4.23$$

The pinched HEMT data is first converted to Z-parameters then inductances and resistances, which are already known in figure 4.13 from zero bias measurements, are de-embedded from the model. The de-embedded Z-matrix is then converted to Y-matrix to determine the remaining capacitances. Cds and Cpd are normally very difficult to separate with a number of extraction methods available in literature [R4.25]. In this work Tayrani's method of making Cpd=Cds/4 has been followed to be consistent with other parasitic extractions.

Once the parasitic parameters are determined, the bias dependent S-parameters can be de-embedded to determine the intrinsic elements. The first estimate of intrinsic element values was made using the method of Beroth and Bosch [R4.26]. They use parasitic de-embedded data to estimate the intrinsic parameters by using the following expressions.

$$Cgd = -\frac{\text{Im}\{Y_{12}\}}{\omega} \qquad\qquad Equation\ 4.24$$

$$Rgd = \text{Re}\{Y_{12}\} \qquad\qquad Equation\ 4.25$$

$$Cgs = \frac{\text{Im}\{Y_{11}\}}{\omega} - Cgd \qquad\qquad Equation\ 4.26$$

$$Ri = \frac{\text{Re}\{Y_{11}\}}{\omega^2 Cgs^2} \qquad\qquad Equation\ 4.27$$

$$gm = \text{Re}\{Y_{21}\} \qquad\qquad Equation\ 4.28$$

$$Gds = \text{Re}\{Y_{22}\} \qquad\qquad Equation\ 4.29$$

$$Cds = \frac{\text{Im}\{Y_{22}\}}{\omega} - Cgd$$

Equation 4.30

Once the initial value of each element is determined, a better fit to measurement data was achieved by hand tuning and optimizing the model using Microwave Office. Figure 4.14 shows a model fit to measured S-parameters of a 100 micron 2 finger LM InP HEMT with gate length of 120nm fabricated on wafer no. A1270. The biasing conditions are Vds=1.5 V and Vgs=-0.4 V. The device was biased for peak gm and the measured Ids was 26mA.
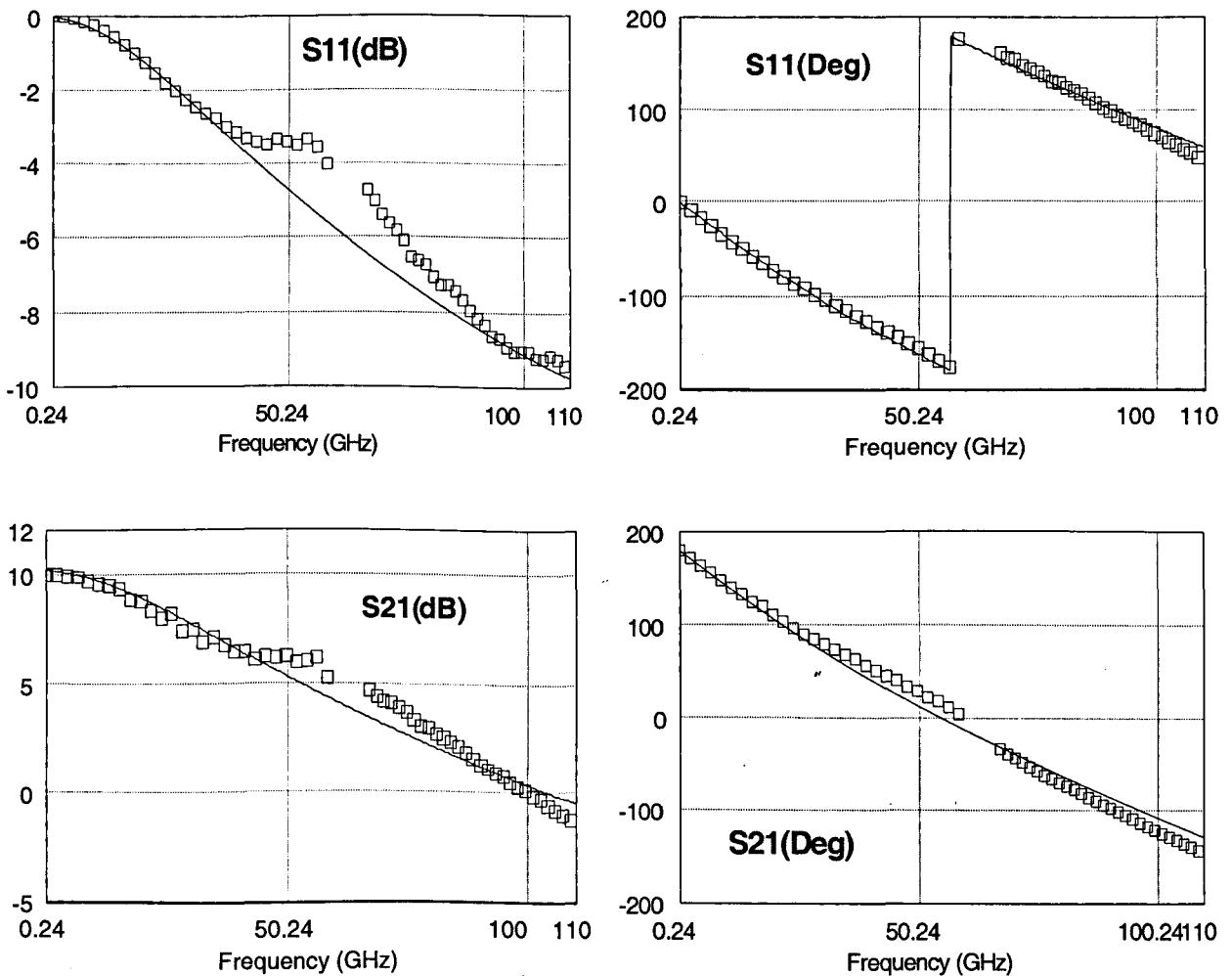
Figure 4.14: Continued next page
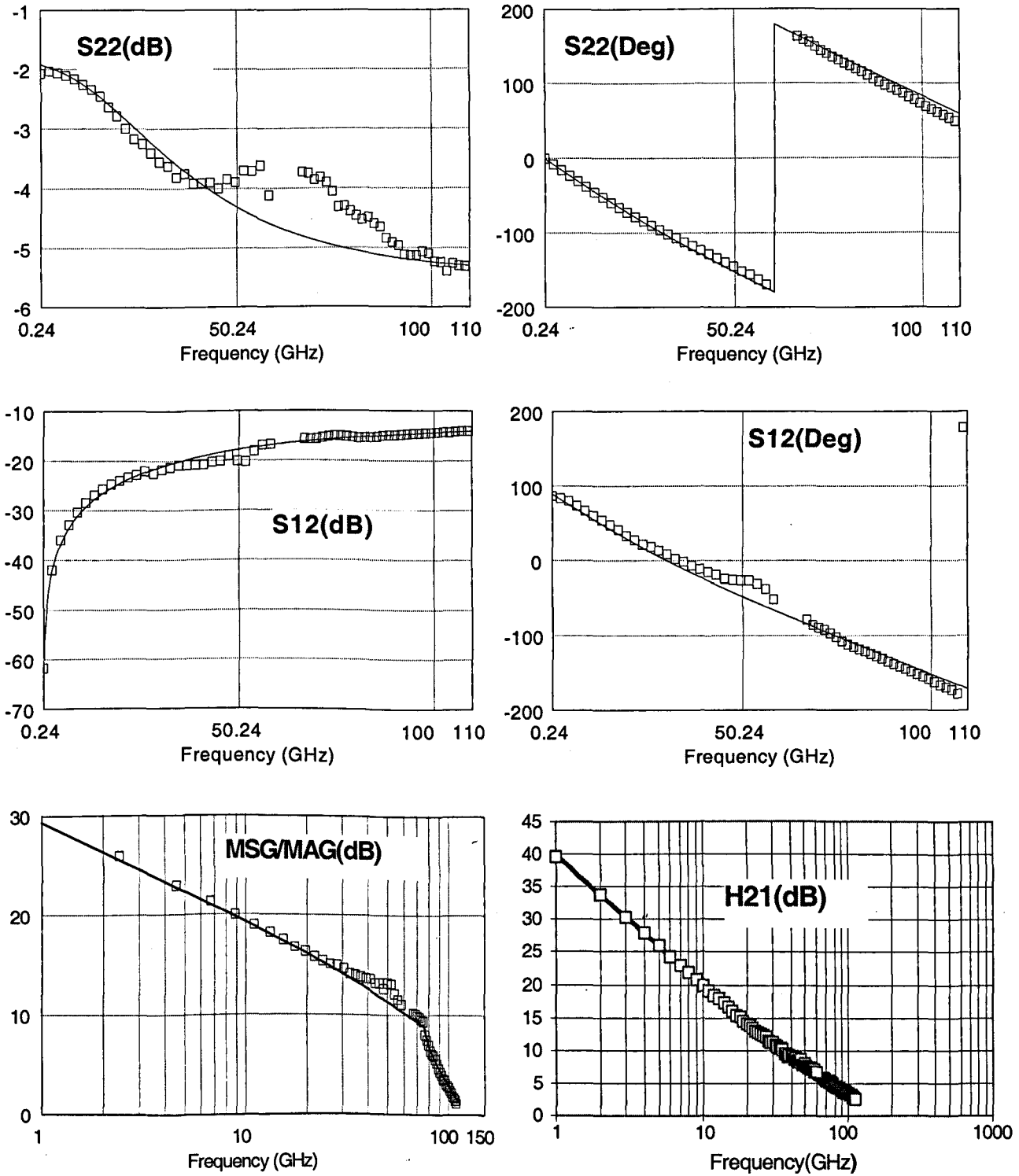
Figure 4.14: Presents measured data of a 100um HEMT (markers) and an equivalent circuit model (solid line) fitted to this measured data.

Cgs	Gm	Cgd	Tau	Cds	Cpgd	Cpg	Cpd	Rs	Ls
66fF	48mS	3.7fF	0.1pS	22fF	2fF	3fF	2.2fF	5.2Ω	3pH
Lg	Rd	Ld	Rg	Rgs	Rgd	Rin	Rds	Gll	Dll
10pH	13Ω	17pH	8Ω	1kΩ	16Ω	3Ω	280Ω	-7μm	20μm

Table 4.1: Equivalent circuit model of A1270 LM HEMT.

The model fitted to this set of data is given in Table 4.1. From the measured data, it can be seen that the maximum available gain at 94 GHz for Vds=1.5V and Vgs=-0.4 is 7 dB. The extracted f_T from measured data at the same bias is 110GHz. The extracted f_T using equivalent circuit model from table 4.1 using equation 4.12 is 104 GHz. This suggests some degree of accuracy in the derived equivalent circuit model. The HEMT pinch off voltage was −1.6V indicating an under etched device, which will result in a lower gm. Under etching will also cause lower gate recess offset, which results in improved Rs.

4.10 UV III/PMMA Mushroom gate HEMTs

To achieve good HEMT performance at millimeter wave frequencies, it is essential to reduce gate resistance. Small gate resistance helps achieve high maximum available gain and lower noise figure [R4.27].

In common source configuration, the input signal is fed into the gate, which can be considered as a distributed network. The signal reduces across the width of the device as it is removed via a distributed capacitor network representing the depletion layer. This reduces the voltage drop across gate width resulting in lower effective gate resistance when compared to DC. Wolf has shown that the microwave gate resistance is one third of the DC end to end resistance [R4.28]. Typically microwave gate resistance can be calculated by the following expression.

$$Rg = \frac{\rho Z_g}{3m^2 h L_g}$$

where p = resistivity of the metal used

h = height of the gate

m = number of gate fingers

L_g = gate length

Z_g = device width or gate width
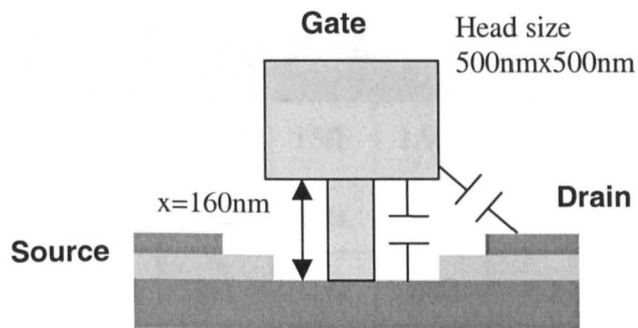
Figure 4.15: UV111 T-gate demonstrates large head size for lower gate resistance and large x for lower parasitic capacitance.

UVIII mushroom gates have been shown to have much lower DC end to end resistance than conventional PMMA/copolymer mushroom gates due to the large head sizes that can be achieved with the bi-layer process as shown in chapter 2. Devices with UVIII gates were fabricated on wafer no. A1276#1 described in chapter 2. The HEMTs showed exceptional RF performance in terms of gain when compared to HEMTs made with PMMA/Copolymer mushroom gates. The maximum available gain of a 100 μm HEMT with 120 nm gate length improved by as much as 3 dB at 94 GHz when compared to PMMA/Copolymer gate HEMT with same dimensions.

Another major advantage of UVIII gate is that its stalk is around 60 nm higher than the convention copolymer gate as shown in figure 4.17. The equivalent circuit model of UVIII gate based HEMT in table 4.2 shows a reduction in Cgd

parameter, which could be due to increased stalk length. This data was extracted from a 2x100μm HEMT with gate length of 120nm. The extracted and measured MAG and H_{21} data is shown in figure 4.18. The maximum attainable gain was measured as 13 dB at 94 GHz at Vds=1.5V and Vgs=0 V. The peak f_T extracted from measured data using 20 dB/decade slope was 193 GHz. Both the MAG and f_T quoted for this device were the best figures of merit achieved during this project. The f_T of this HEMT is quite high when compared to HEMTs made on similar quality material and Ohmic contacts. A possible explanation for this is that the gate length of the device is shorter than 120 nm.

Cgs	Gm	Cgd	Tau	Cds	Cpgd	Cpg	Cpd	Rs	Ls
51fF	60mS	2fF	0.7pS	15fF	1.9fF	1fF	4fF	3Ω	1.2pH
Lg	Rd	Ld	Rg	Rgs	Rgd	Rin	Rds	Gll	Dll
1pH	6Ω	17pH	2Ω	1kΩ	24Ω	4Ω	600Ω	-6μm	-9μm

Table 4.2: Equivalent circuit parameters of a UV111 gate 100μm HEMT.

(a)   *(b)*
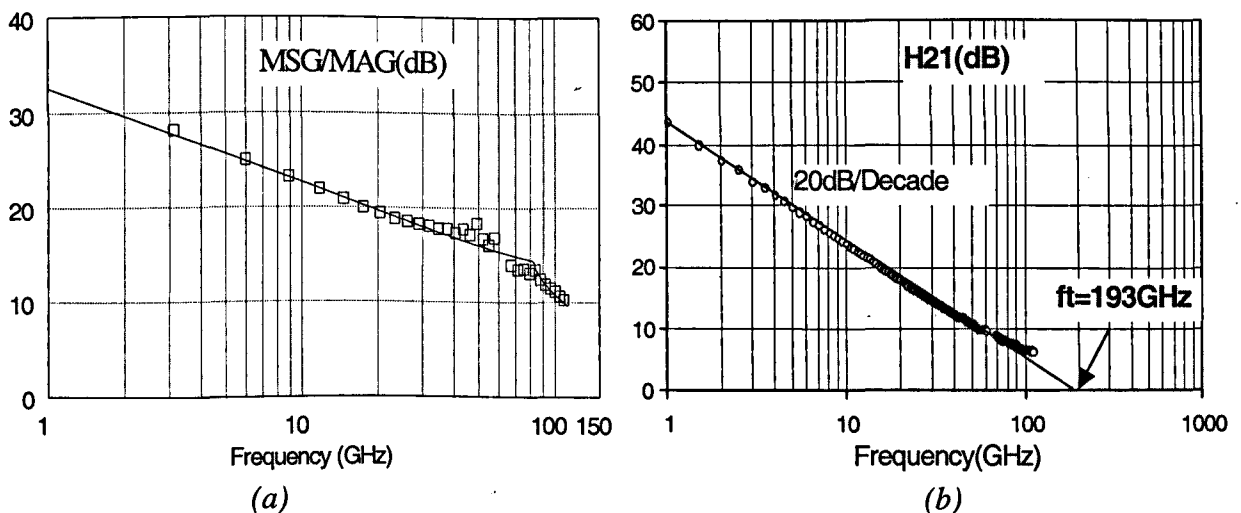
Figure 4.16: (a) The graph is showing the measured and modeled results of maximum attainable gain at VDS=1.5V and Vgs=0. (b) The graph is showing the measured data of the same device biased at Vds=1.2V for Peak f_T.

4.11 Summary

The chapter has outlined brief operating principles of HEMTs. Both DC and RF characteristics of InP LM HEMTs have been shown and discussed. Small signal equivalent circuit models of HEMTs have been extracted and RF performance of HEMTs using different gate technologies has been compared.

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5   CPW Couplers & Power Dividers

5.1   Introduction

Passive circuits such as directional couplers find a wide variety of applications such as power splitting/combining in balanced circuits or are used for separating incident and reflected signals in network analyzers. A number of couplers were designed, measured and modelled in this project.   In some cases accurate equivalent circuit models were extracted and subsequently used in circuit design. Coplanar waveguide based Branch-line, rat-race and Lange couplers together with Wilkinson power divider/combiner were produced in this project.

5.2 Wilkinson Divider/Combiner

The Wilkinson power divider is a three port passive circuit used for splitting or combining signals. It can be designed for an arbitrary power split but in this project the dividers were designed for equal splitting of the signal power. The design conditions are that the signal at the input must equally divide into output ports 1 and 2 and stay in phase. All the ports of the network should also be matched and the two output ports must be isolated from each other (figure 5.1). Pozar has shown by odd-even mode analysis that the Wilkinson circuit shown in figure 5.1 meets all the design requirements [R5.1].
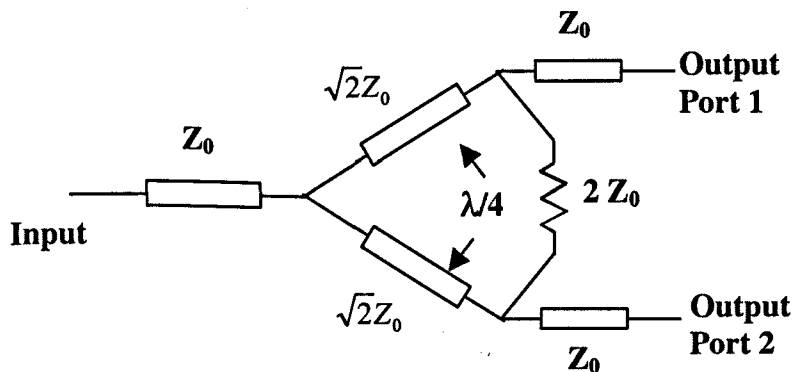
Figure 5.1: An equal split Wilkinson divider

The equal power division (3 dB split) in this circuit is determined by the characteristic impedance of the two arms of the splitter. The quarter wavelength arm length sets the centre frequency of the Wilkinson divider. The resistor between the two output ports absorbs any signal that might occur due to reflection from the output ports.

The circuit was implemented with the following dimensions in 50 Ω coplanar waveguide system for 77 GHz operation

$\lambda/4 = 385\ \mu m$

$\sqrt{2}\ Z_0 = 70.7\Omega$

$2\ Z_0 = 100\ \Omega$

The divider was designed as a two-port device due to availability of only two RF probes. This was achieved by terminating one of the output ports with matching 50 Ohm load at any one time (see figure 5.2). To characterize this circuit two Wilkinson dividers were fabricated with the resistor switching positions at the output in each case.
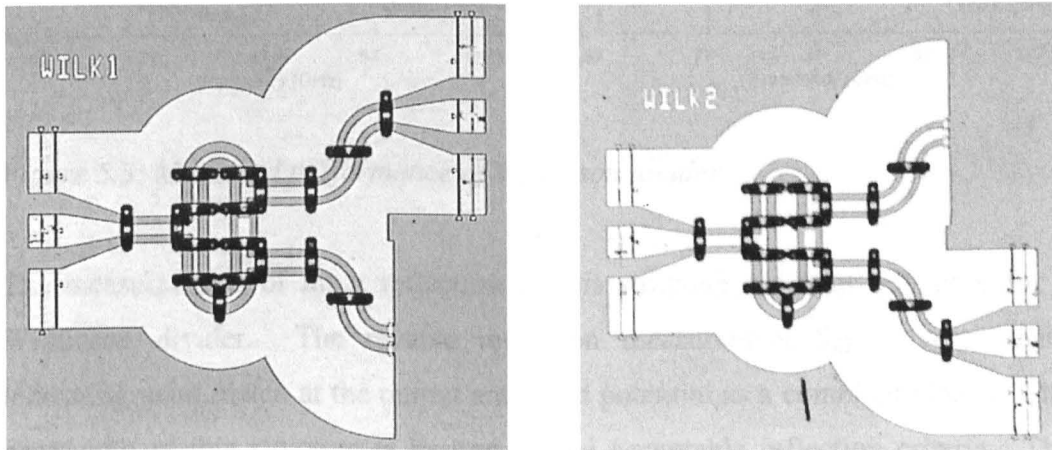
Figure 5.2: Wilkinson divider with alternate port terminated with 50 ohm load

The circuit was measured in the W-band frequency range after an LRL calibration of the network analyzer. The final metal thickness was 1.2μm which resulted in an insertion loss of 1 dB at both output ports (see figure 5.3). The return loss was measured to be -9 dB at the design frequency for both structures. The symmetrical nature of the structure means both outputs are measured in phase. The reverse reflection is better than -20 dB, indicating very good function as a combiner.
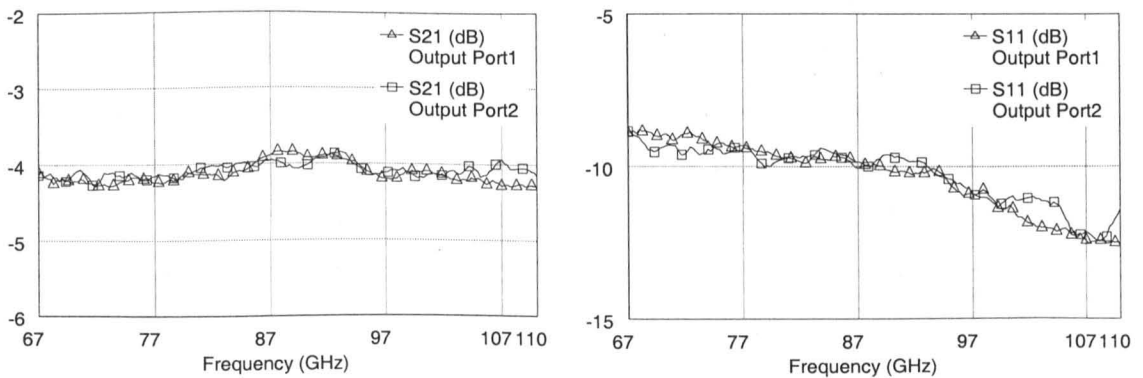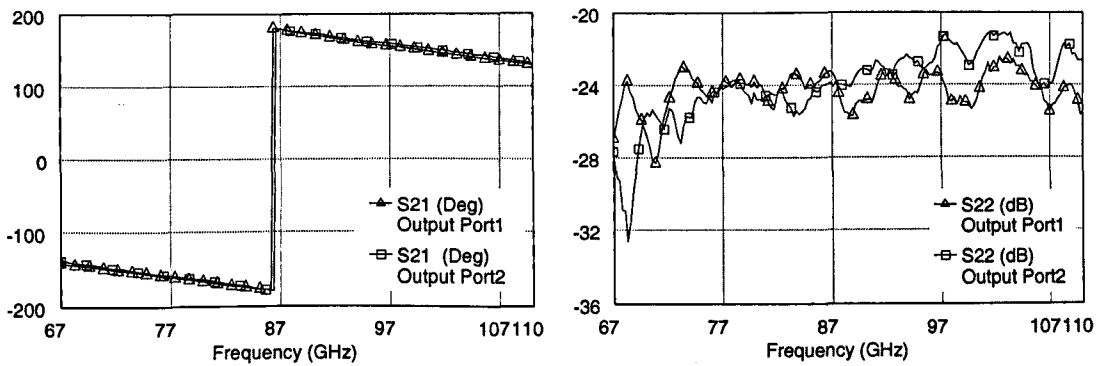
Figure 5.3: Measured performance of Wilkinson divider

The measurements of input reflection of this structure are relatively poor for a Wilkinson divider. The reverse reflection measurement S_{22} is very small, indicating good match at the output and good potential as a combiner circuit. The bandwidth of this structure is limited by the acceptable reflection criteria. The forward transmission and phase are constant with frequency but the reflection is variable.

The input reflection was improved by varying the angle at the input T-junction from 90 degrees to 45 degrees (see figure 5.4). It is believed that right angle T-junction at the input was causing large amount of signal reflection. As a result the angle was reduced and the measured S-parameters of the modified geometry are shown in figure 5.4.

The modified divider in figure 5.4 offers a number of advantages over the original tee geometry. The reflection S11 improves from –9 dB to –16 dB at the design frequency. The S11 reflection could have been smaller with more accurate 50 Ω resistor terminations as shown by reverse modeling (see figure 5.5). It is also demonstrated in the next chapter when these dividers are used in the I-Q modulator circuit. The lower reflection also helps in improving the insertion loss by around 0.7 dB due to more signal entering the divider arms (see figure 5.4). The power division is equal and in phase. The S22 reflection is also measured to be better than –20 dB.

Modified   *Original*
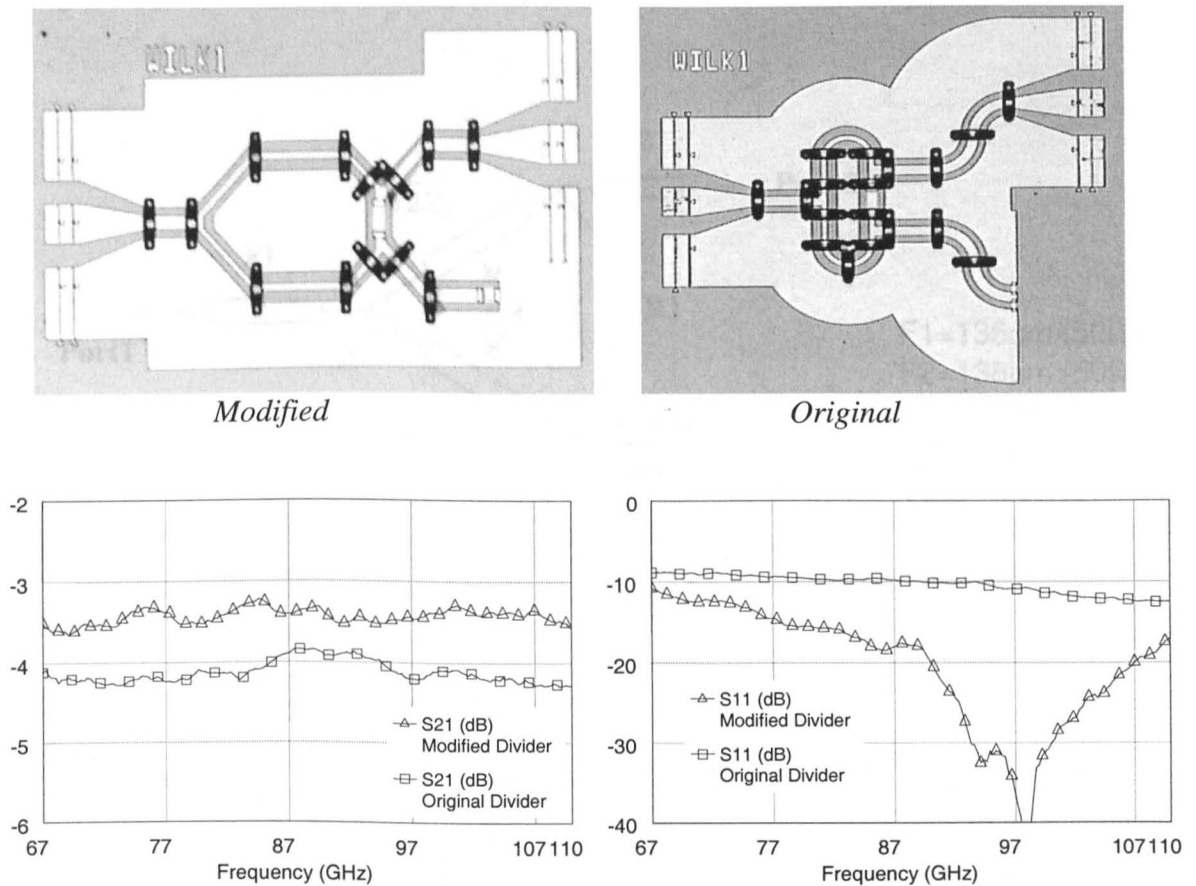
Figure 5.4: Illustrates the visual difference between the two Wilkinson Dividers and compares their measured performance.

5.2.1 Equivalent Circuit Modeling of Wilkinson divider

Equivalent circuit models were extracted for both Wilkinson divider geometries. The modeling strategy was to design, fabricate and measure these devices and fit the measured data to the equivalent circuit model given in figure 5.5. The initial geometry for Wilkinson divider (labeled "original" in Figure 5.4) required additional parasitic capacitors in the equivalent circuit model to account for perpendicular discontinuities [R5.2]. These were not required in the modified geometry as the discontinuity capacitance was too small to be included in the basic

model of figure 5.5. The parameter values in figure 5.5 are quite similar to the original layout dimensions and the extracted resistor values from the device wafer.

F1=135μm (50Ω)
F2=138μm (50Ω)
F3=149μm (50Ω)
λ/4=350μm
√2Z₀ =70.7Ω
R1=120Ω
R2=72Ω
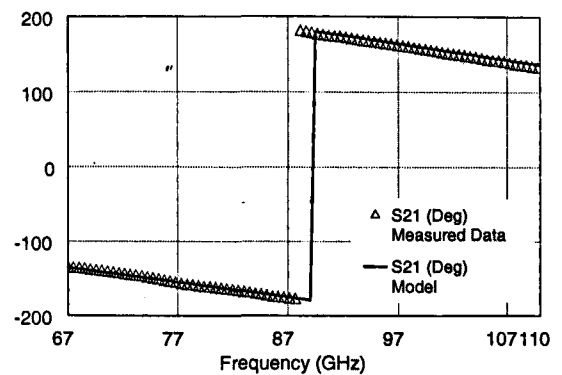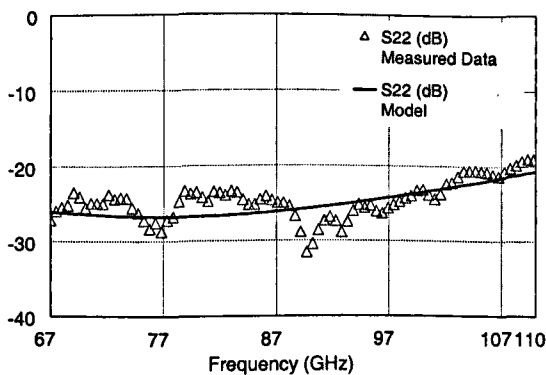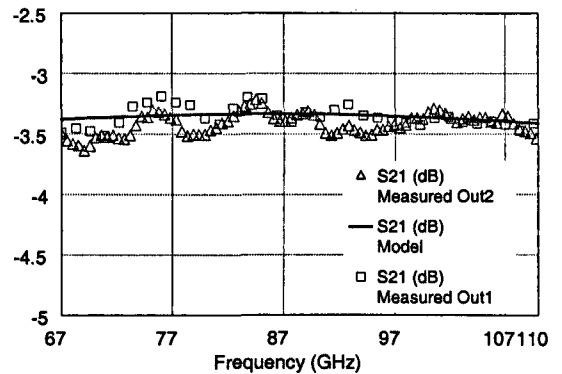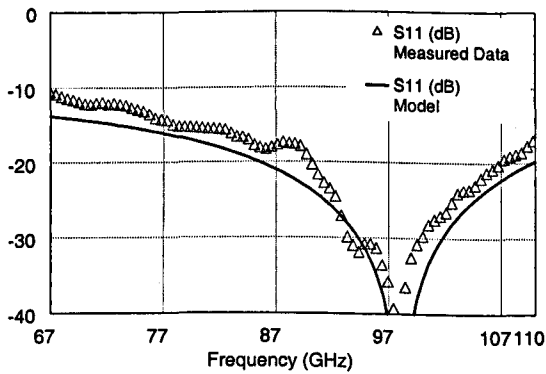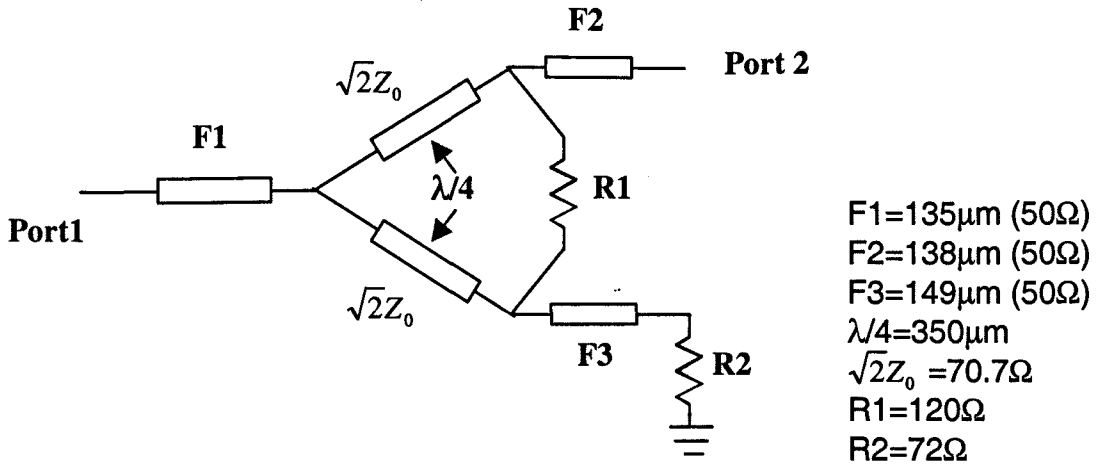
Figure 5.5: Shows the equivalent circuit model for Wilkinson divider and the typical parameter values used to fit the model to data. The plots illustrate the match between the measured and model data for modified Wilkinson divider.

5.3 Branch-line Coupler

The Branch-line coupler is a four port power splitter that divides an input signal into two signals of smaller power. A coupler circuit can be designed to perform any level of power division. Operation of a typical coupler is summarized in figure 5.6 with port definitions.
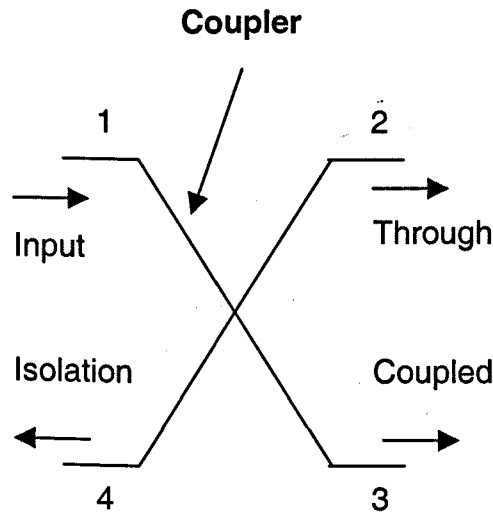
Coupler

Figure 5.6: Commonly used symbol for directional coupler and its port notations

Power supplied at the input couples to port 3 with some coupling factor X and the remainder goes to port 2. If the coupler is matched properly at its ports then there should not be any power delivered to port 4. A four port coupler can be characterized by the following quantities [R5.3]

$$Coupling = C = 10\log\frac{P_1}{P_3} = -20\log X \, (dB)$$

$$Directivity = D = 10\log\frac{P_3}{P_4} = 20\log\frac{X}{|S_{14}|} \, (dB)$$

$$Isolation = I = 10\log\frac{P_1}{P_4} = -20\log|S_{14}|(dB)$$

A Branch-line coupler is a special form of coupler that divides an input signal equally between the two output ports with 90 degrees of phase shift between them. In this case the coupling factor X is $\dfrac{1}{\sqrt{2}}$ for 3dB of coupling. It is completely a symmetrical structure with the extra quality of interchangeable ports. Any one of its ports can be used as an input port where the opposite two ports are the outputs and the port adjacent to input port is the isolation port.

The design conditions for the branch-line coupler are that all ports are to be matched with equal power split at the output and 90 degrees of phase-shift between the output ports. The Y-parameter matrix covering all the design conditions can be derived by direct synthesis [R5.4] and is shown in figure 5.7.

$$[Y] = j\begin{bmatrix} 0 & 1 & 0 & \sqrt{2} \\ 1 & 0 & \sqrt{2} & 0 \\ 0 & \sqrt{2} & 0 & 1 \\ \sqrt{2} & 0 & 1 & 0 \end{bmatrix}$$
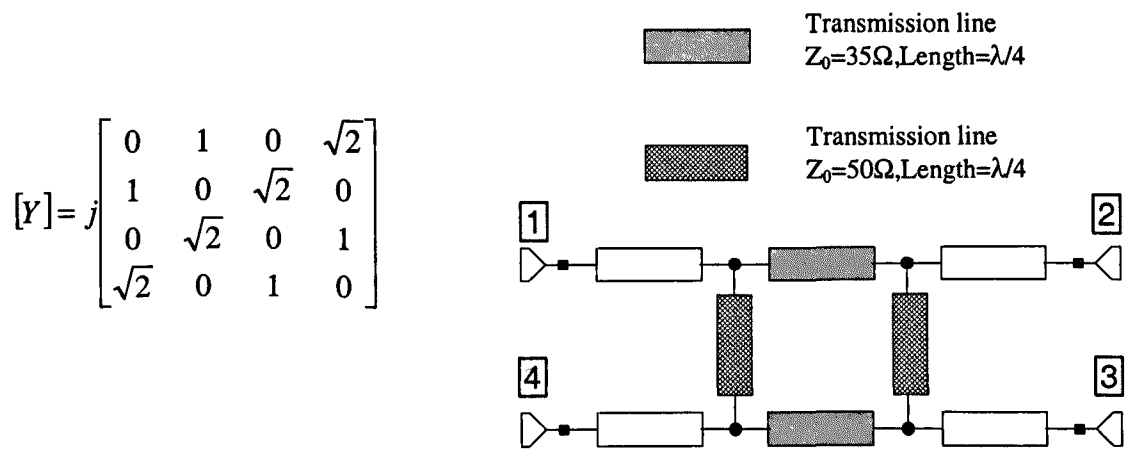
Figure 5.7: Branch-line coupler admittance matrix and circuit diagram.

The branch-line couplers were characterized in the same manner as Wilkinson divider. Firstly 3 couplers were fabricated with two of the ports terminated in 50Ω resistances (see figure 5.8). These couplers were then measured in W-band with LRL calibration and the results are shown in figure 5.8.
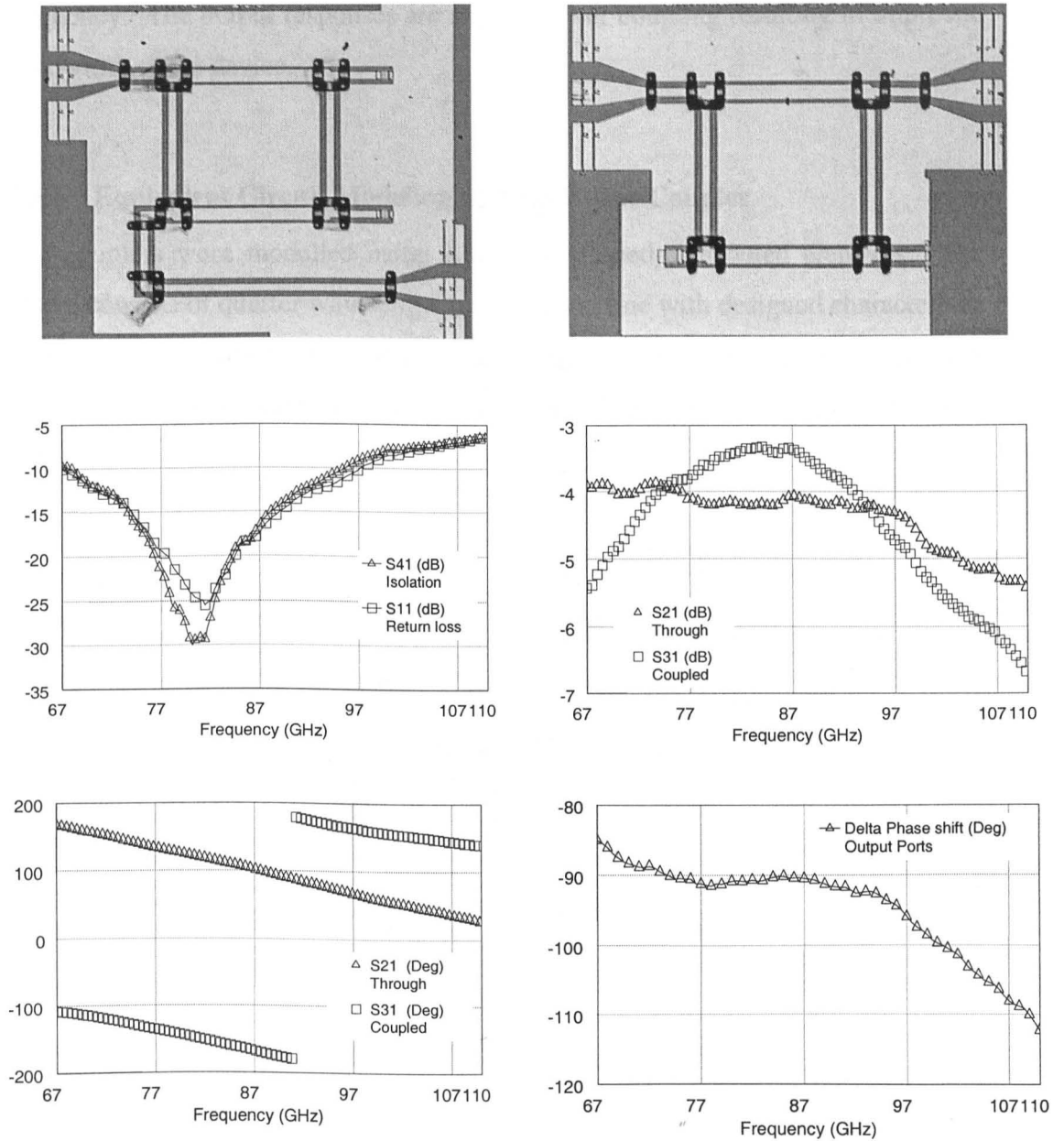
Figure 5.8: shows the layout of the fabricated branch-line coupler along with the measured results.

The input reflection measurements of the coupler are near ideal with return loss measured smaller than –20 dB at the design frequency. The shift in the resonance from the 77 GHz was shown to be due to non-ideal resistors by modeling. The phase shift between the two output ports is around 90 degrees at the design

frequency. The output responses are showing over coupling resulting in improved bandwidth of the device.

5.3.1   Equivalent Circuit Modeling of Branch-line Coupler

The couplers were modelled using a mix of lumped-distributed elements. The model consists of quarter wavelength transmission line with designed characteristic impedance and parasitic capacitance (Cp) showing the discontinuity effect. The complete model and extracted parameters along with data fit are shown in figure 5.9.
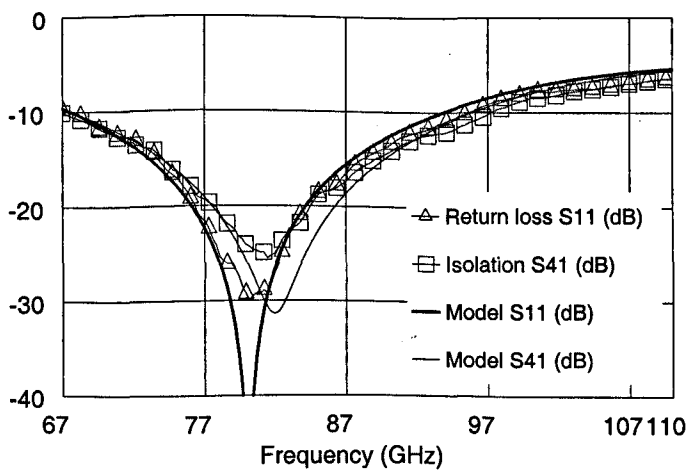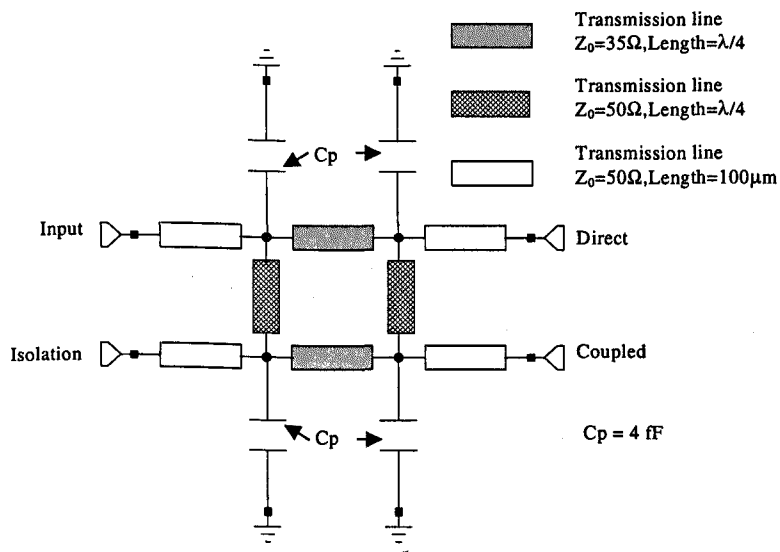
Figure 5.10: continued
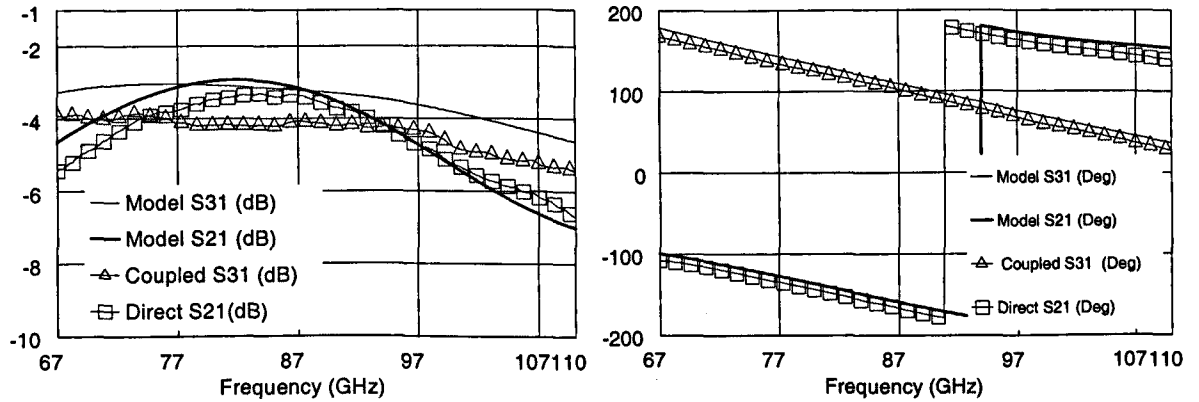
Figure 5.10: Equivalent circuit model of branch-line coupler and graphs showing model to measured data curve fitting.

5.4 Rat-race Coupler

The rat-race coupler is a 4-port power divider with 180 degrees of phase shift between its output ports. The couplers contains a phase inverter network within so depending on which port is used as input, the outputs can either be in phase or out of phase. When port 1 in figure 5.11 is used as the input port, the signal divides equally in-phase at ports 2 & 3 with port 4 as the isolation port. If port 4
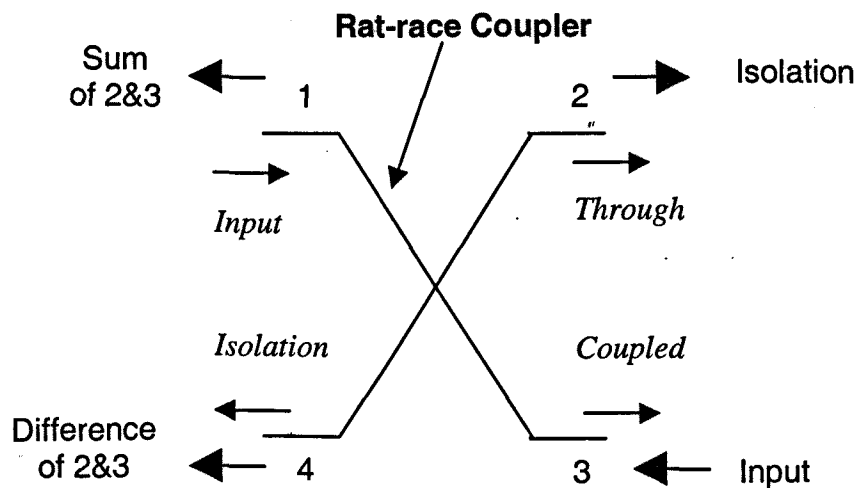
Figure 5.11: Operation of rat-race coupler with inside arrows representing the splitter action and the outside arrows indicating combiner operation.

is used as the input port, then the two output ports 2 & 3 will have equal 3-dB signal with 180 degree of phase shift between them. Port 1 is the isolation port in this case. When the rat-race coupler is used as a combiner with the input signals fed into port 2 and 3, the two signals will add in-phase at port 1 and anti-phase at port 4. Ports 1 and 4 are called the sum and difference ports respectively [R5.5].

The rat-race coupler is designed in a similar manner to the Wilkinson divider and branch-line coupler, where the condition of design are equal signal split with phase inversion and all matching ports. The normalized Y-parameter matrix covering all design conditions of rat-race coupler derived by direct synthesis of S-parameters is shown below [R5.6].

$$[Y] = j\sqrt{\frac{1}{2}} \begin{bmatrix} 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ -1 & 0 & 1 & 0 \end{bmatrix}$$

The couplers were fabricated and measured after an LRL calibration. The anti-phase network was realized by using $\lambda/2$ wavelength transmission line. This shifter has a very narrow bandwidth and limits the ideal performance of the coupler to the frequency defined by the $\lambda/2$ line [R5.7]. The coupler is not often used as an in-phase power splitter due to limited bandwidth compared to other circuits like the Wilkinson divider.

The fabricated coupler and its measured characteristics are shown in figure 5.12. It is clear from measurements that coupler performs ideally in forward transmission operation. The coupled and direct port show near ideal power split with 1 dB of insertion loss. The phase shift between the two output ports is also 180 degree at the design frequency. The return loss at the design frequency is around −16 dB with an isolation of better than -20 dB. The reason for the relatively poor reflection measurements are believed to be similar to the one noticed in Wilkinson

divider. The coupler tends to suffer from right angle junctions at the input of the circuit.
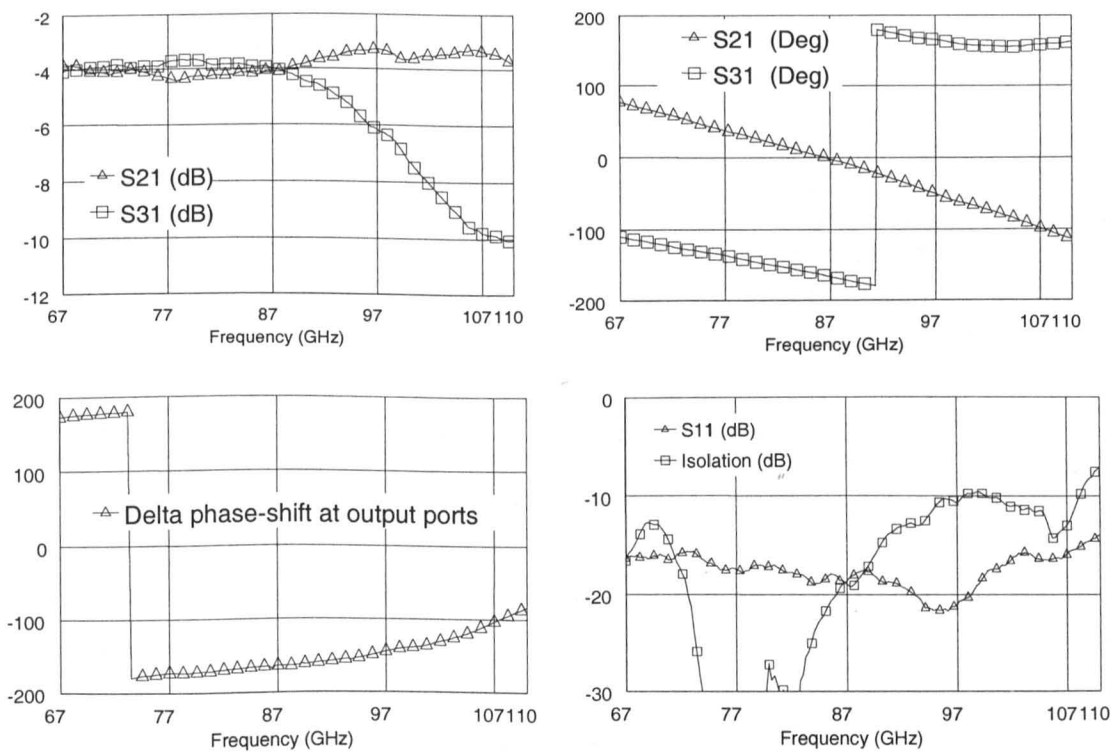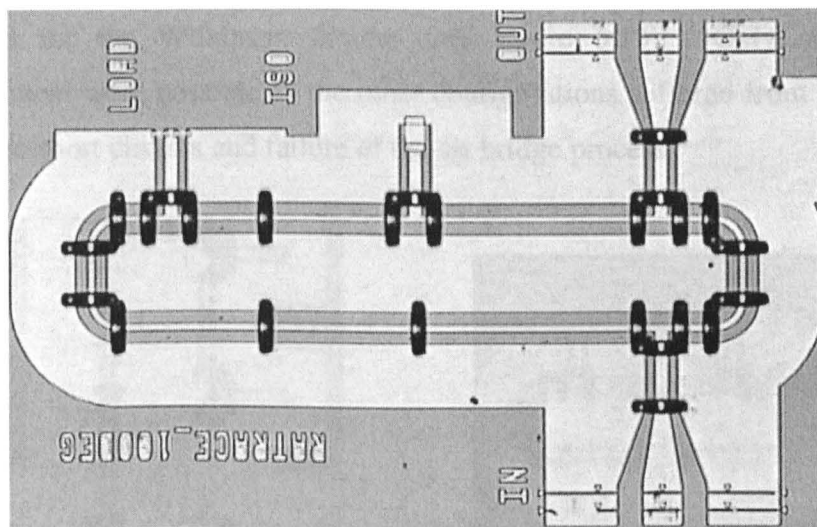

Figure 5.12: Picture of fabricated rat-race coupler along with S-parameter measurements of the structure. The isolation measurements are without air-bridges.

Rat-race couplers with 45-degree junctions were also fabricated but suffered from poor yield. The improvement in the performance was small compared to that observed for the Wilkinson divider (see figure 5.13). Only coupled port measurement were possible as the other configurations suffered from poor lift-off leading to short circuits and failure of the air bridge process.
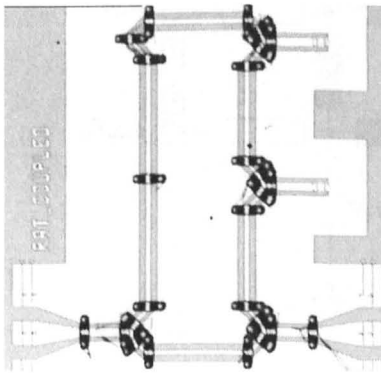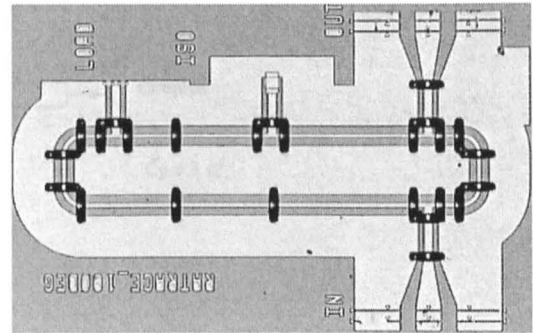
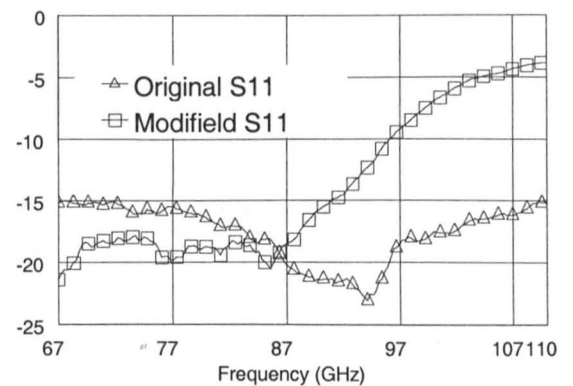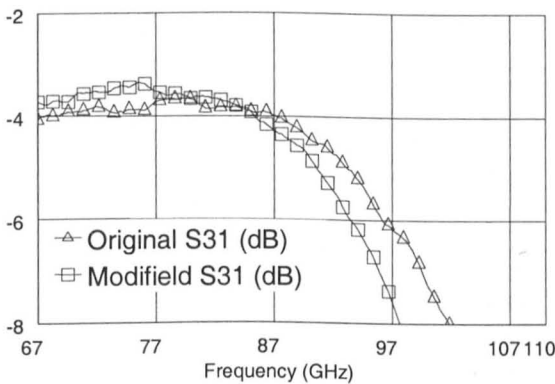*Modified*   *Original*

Figure 5.13: shows the performance difference between the original and modified rat-race geometry.

5.4.1 Equivalent Circuit modeling of Rat-race Coupler

The model was extracted from data of the original rat-race coupler, as a complete set of data was available. A similar model to the branch-line coupler was used with λ/4 transmission lines of designed characteristic impedance and parasitic

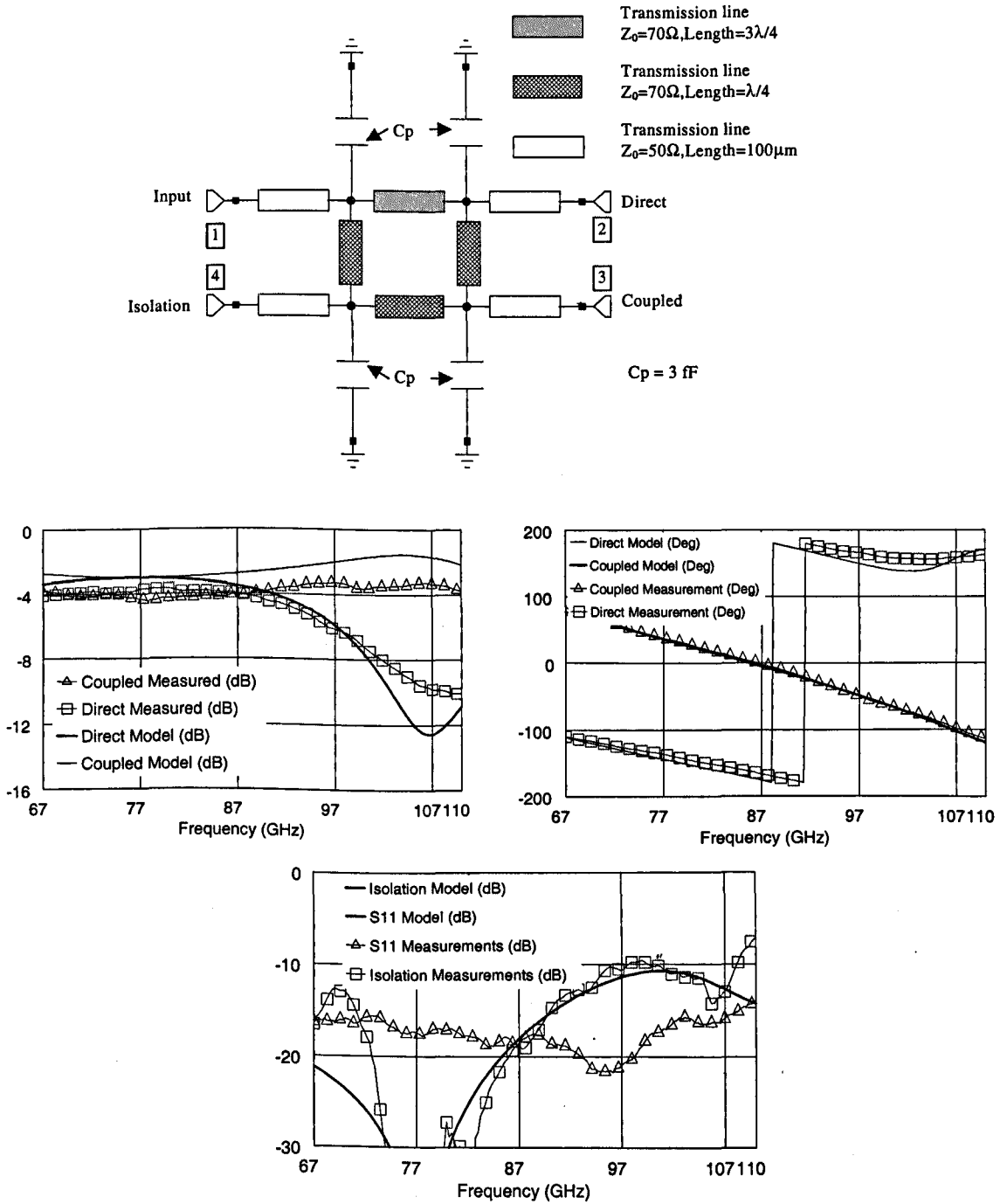capacitance (Cp). The complete model and extracted parameters along with the data fit are shown in figure 5.14.

Transmission line
$Z_0=70\Omega$,Length=$3\lambda/4$

Transmission line
$Z_0=70\Omega$,Length=$\lambda/4$

Transmission line
$Z_0=50\Omega$,Length=100μm

Input   [1]   Direct [2]

Isolation [4]   Coupled [3]

Cp

Cp = 3 fF

Coupled Measured (dB)
Direct Measured (dB)
Direct Model (dB)
Coupled Model (dB)

Frequency (GHz)

Direct Model (Deg)
Coupled Model (Deg)
Coupled Measurement (Deg)
Direct Measurement (Deg)

Frequency (GHz)

Isolation Model (dB)
S11 Model (dB)
S11 Measurements (dB)
Isolation Measurements (dB)

Frequency (GHz)

Figure 5.14: Rat-race model and data fitting plots

5.5 Lange Couplers

A Lange coupler is a power splitter, capable of providing equal power division between the two output ports with 90 degree of phase shift. The coupler is ideally suited for broadband applications as it offers an octave of bandwidth, considerably, more than the branch-line coupler [R5.8]. The layout of the coupler with all 4 ports labeled is shown in figure 5.15.
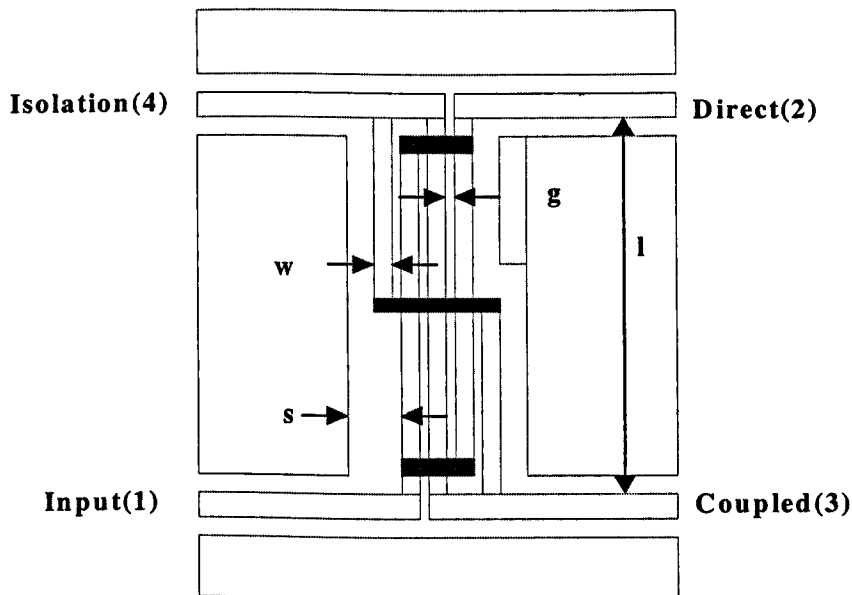

Figure 5.15: Layout of a Lange coupler.

When transmission lines are placed in close proximity, energy from one line can be coupled to the next line. In Lange couplers several parallel transmission lines are placed in closed proximity, as a result fringing fields from both edges of each line contribute to the coupling. In an ideal Lange coupler, the coupling is directional which means that the coupled signal travels in the opposite direction to the wave on the input line. In the ideal structure the direct and coupled ports are 90 degree out of phase across all frequencies, all four ports are matched and no signal is present at isolation port.

5.5.1 Design of CPW Lange Coupler

Most Lange coupler analysis methodology and design data is available for microstrip structures formed on substrates with very low effective dielectric, which are used in hybrid microwave circuits [R5.9]. Recently, Pieters has analyzed CPW based Lange couplers and provides design data but again for low effective dielectric substrates and the coupler dimensions covered are unsuitable for monolithic circuits [R5.10]. Campos-Roca has demonstrated a 40 GHz CPW Lange coupler but with no explanation of design or the coupler dimensions [R5.11].

In the Lange coupler, there are four design parameters shown in figure 5.15 (*s, w, g and l*), which have to be optimized in the design problem. The design equations for Lange couplers, given by Pozar are valid for equal odd and even mode phase velocities [R5.12]. This is not the case in this topology due to the nature of the structure.

The Lange couplers of this project were initially designed using em Sonnet Software, a 2-D electromagnetic simulator [R5.13]. The initial estimate of design parameters was taken from Lo whose demonstrated a 94 GHz Lange coupler in microstrip on GaAs [R5.14] (a valid assumption if ground planes are a certain distance from coupled lines [R5.15]). The coupler was optimized for equal power split and 90 degree phase shift.

To maximize coupling between lines, a small gap *g* was initially chosen. 2-D electromagnetic simulators are limited when it comes to designing coupled line structures with small dimensions as they assume zero metal thickness. In the initial coupler design, the metal thickness of 1.2 μm was as much as 25% of strip spacing *g*. The side-walls of the metal strips influence the electric field and by not including the field due to thick metal, errors are introduced in the simulation results.

l and *s* were optimized for fixed *w* and *g* which were chosen by considering the fabrication limits . For ideal phase shift and power split *l* and *w* were found to be 330 μm and 70 μm respectively. The optimum coupling length of this structure

has shifted from the theoretical optimum of $\lambda/4$ due to the presence of various modes in the coupler.

5.5.2 Fabrication and Measurements

To overcome the uncertainties of the electromagnetic simulator design, a number of Lange couplers were fabricated to study the variation of the coupler performance when *s*, *g*, and *w* of Figure 5.15 were changed. The variations in geometrical parameters were chosen around the designed values. Three different structures were designed and fabricated to measure the coupler response (see figure 5.16).

(a)

(b)

(c)
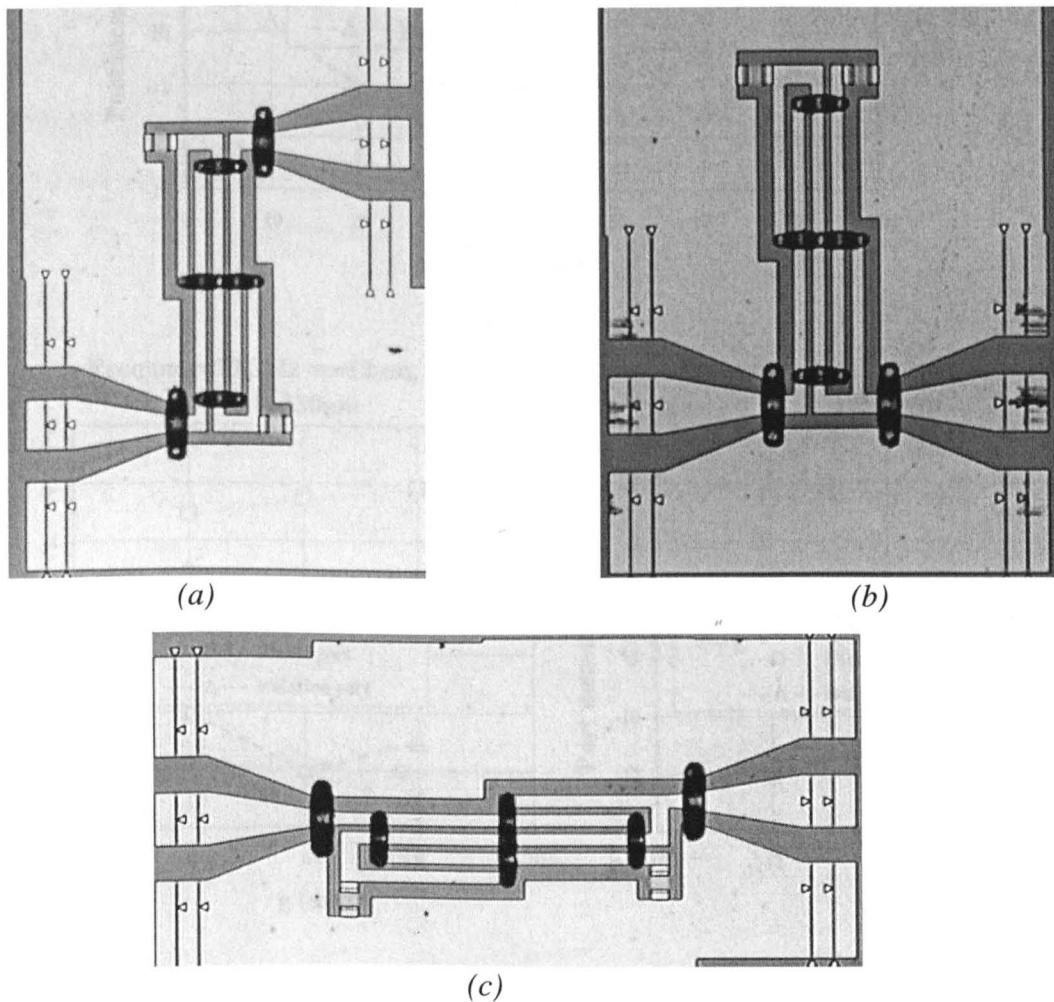
Figure 5.16: Fabricated Lange coupler (a) coupled port test structure (b) direct port test structure (c) isolation port test structure.

The circuits were fabricated on 400 μm semi-insulating InP substrate (ε_r = 12.2) using the standard fabrication process described in chapter 2. The measurements were performed on a quartz substrate after an LRRM calibration using ISS calibration standards.
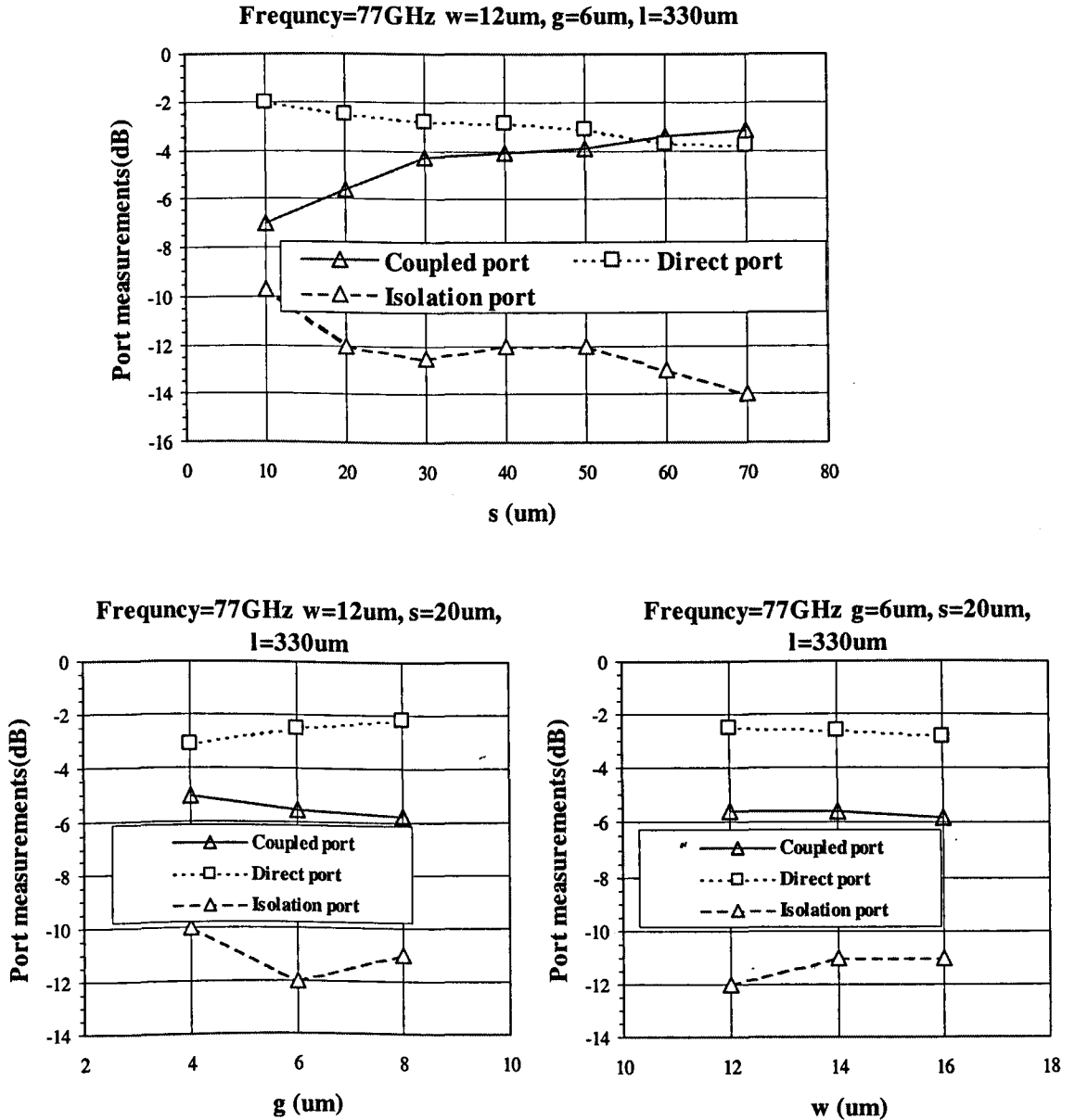
Frequncy=77GHz w=12um, g=6um, l=330um

Frequncy=77GHz w=12um, s=20um, l=330um

Frequncy=77GHz g=6um, s=20um, l=330um

Figure 5.17: shows the response of Lange coupler ports with changes in layout parameters at 77 GHz.

The measurements in figure 5.17 show the trends expected from a Lange coupler. By increasing the distance s, coupling between ground planes and signal strips is reduced which results in higher signal at the coupled port. Reduction in g also results in more coupling between lines. Figure 5.18 compares the measured and modeled (em Sonnet) response of a l=330 μm, s=70 μm, w=12 μm, g=6 μm Lange coupler and shows a relatively good match. The measured data at the coupled port is over coupled when compared to the Sonnet response because the metal thickness of the conductor is not included in Sonnet. The input reflection of simulation and measurement differ significantly reasons for that are unclear.
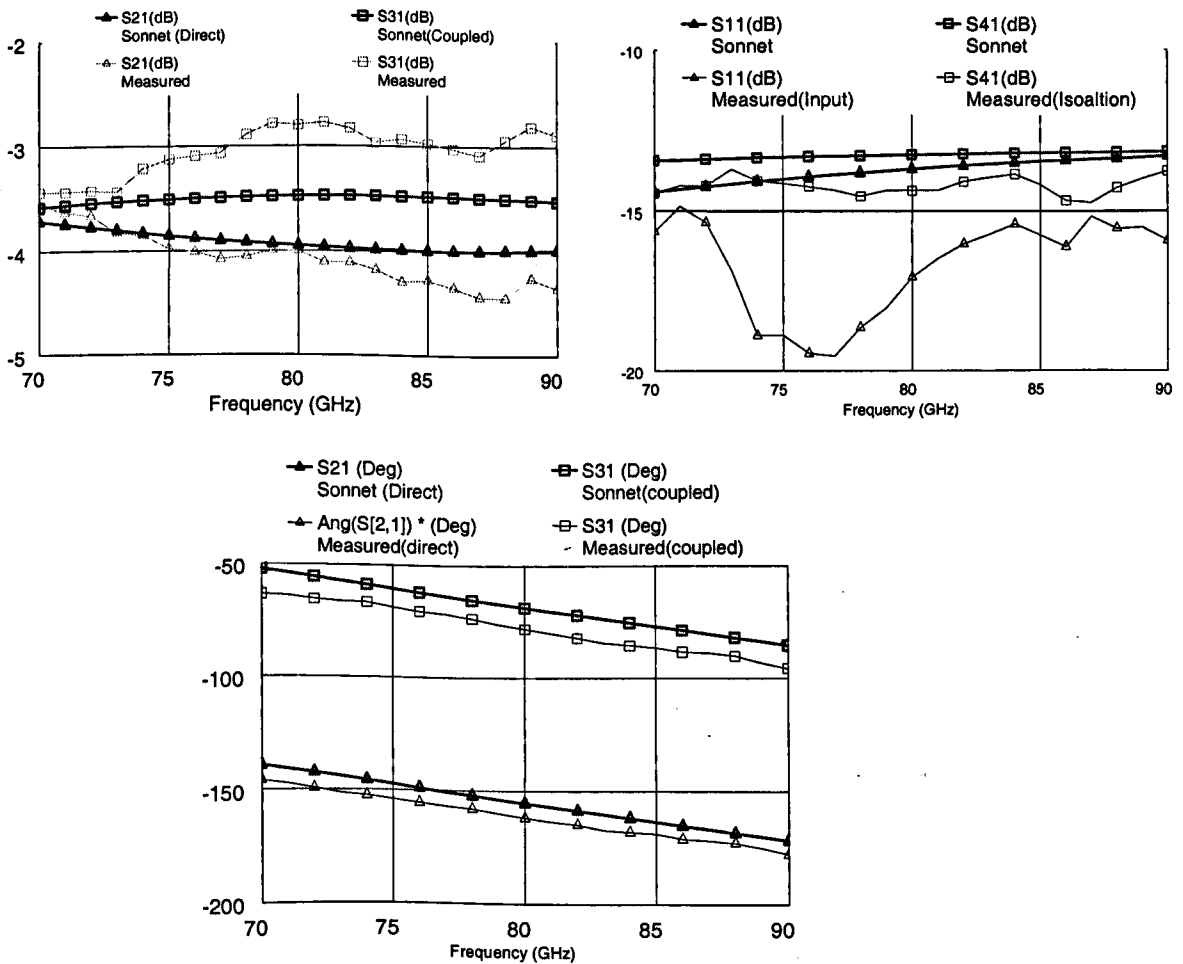
Figure 5.18: Measured and modeled (Sonnet) response of a l=330 μm, s=70 μm, w=12 μm, g=6 μm Lange coupler

A near ideal Lange coupler response was achieved with s=60 μm, w=12 μm, g=6 μm, l=330 μm (see figure 5.19). This structure in figure 5.19 has over coupling of 0.4 dB with insertion loss of less than 1 dB form 67-110 GHz . The input return loss and isolation were measured to be -18 dB and -13 dB at 77GHz. The phase difference between the output ports was measured as 90° ± 3° from 70 GHz to 110 GHz.
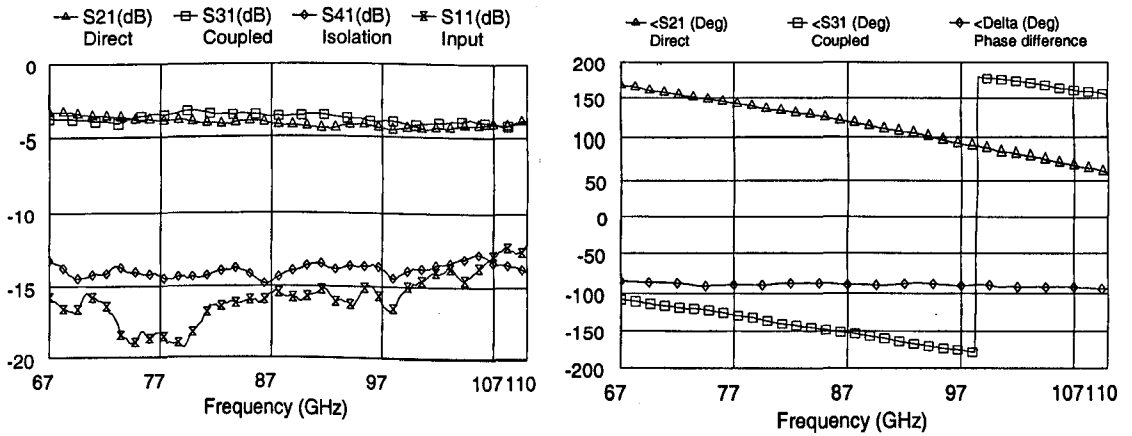
Figure 5.19: Response of a Lange coupler with s=60 μm, w=12 μm, g=6 μm & l=330 μm.
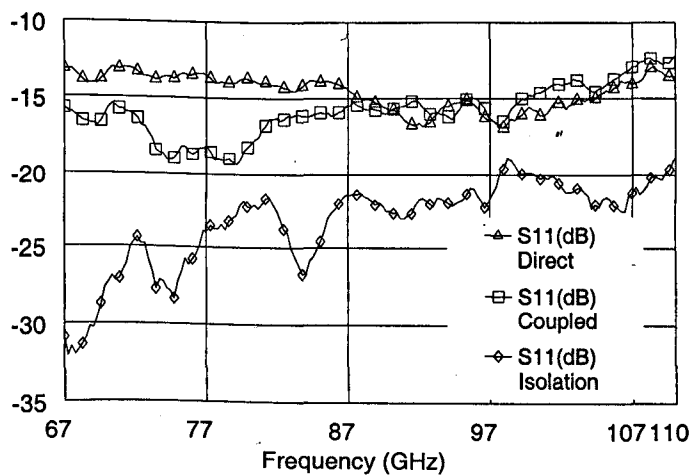
Figure 5.20: Input reflection of Lange coupler with s=60 μm, w=12 μm, g=6 μm & l=330 μm.

The input reflection measurement of each of the three Lange coupler structures shown in figure 5.16 varied, as shown in figure 5.20. It is believed that the input reflection coefficient of the isolation structure was the best because there is no right angle feed-line discontinuity at the structure input. The original feed (designed to simplify the Sonnet simulation) showed a poorer input reflection when compared to a mitred feed (see figure 5.21). The input reflection improved by at least 2dB when a mitred feed was used.
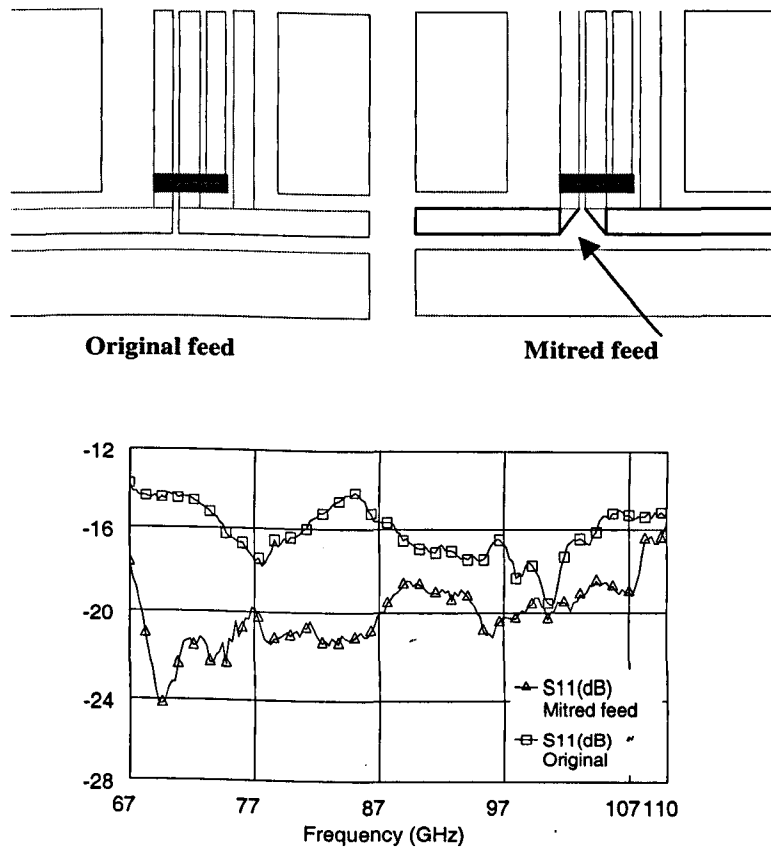
Original feed   **Mitred feed**

Figure 5.21: Comparison between input feeds of the Lange coupler (s=50 μm, w=12 μm, g=6 μm).

5.6 Summary

This chapter has described the design, fabrication and measurements of passive circuits such as branch-line coupler, rat-race coupler, Lange coupler and Wilkinson divider. In all cases coupler couplers have shown good performance at W-band frequency range. In most cases accurate equivalent circuit models have been extracted to be used in the circuit design.

5.7 References

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[R5.15]   P.Pieters, R.Mertens, "Generalized Analysis of Coupled Lines in Multilayer Microwave MCM-D Technology", IEEE Trans. Microwave Theory & Tech., Vol. 47, No. 9, pp. 1863-1872, 1999.

6 CPW Vector Modulators

6.1 Introduction

In this chapter the operation, design and measurements of CPW based vector modulators operating at 77 GHz is discussed. Different digital modulation schemes are explained and comparison between direct carrier modulation and baseband modulation is made. Reflection type circuits are explained including the use of a HEMT as a variable resistor. The principle of a single ended modulator is explained including its use as a switch and a BPSK modulator. The operation of QPSK modulators, realized using parallel BPSK modulator is discussed. Measured results of single ended and balanced BPSK and QPSK vector modulators are presented and analyzed.

6.2 Direct Carrier Modulation

Direct carrier modulation is an alternative to standard baseband modulation used in the majority of transceiver systems. In conventional transmitters, the signal is modulated at the Intermediate Frequency (IF) then up-converted using a chain of mixers, filters and amplifiers (see figure 6.1). In the direct carrier modulation scheme, the RF carrier frequency is modulated, which results in the elimination of the sub-component chain for up-conversion. In monolithic millimeter-wave circuits where chip space is of a premium in terms of cost, direct carrier modulation is an attractive solution.
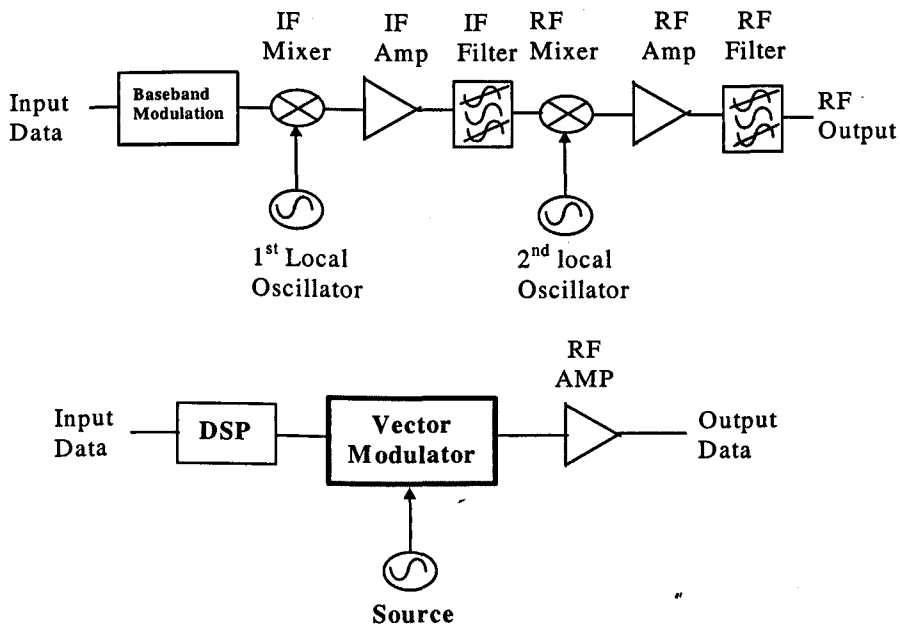

Figure 6.1: Comparison between conventional and direct carrier modulation transmitter

In modern wireless systems digital modulation is preferred to analogue due to increased channel capacity and improved accuracy of transmit-receive information [R6.1]. Phase shift keying (PSK) is a popular form of modulation due to the complexity that can be achieved from this scheme. It is a form of angle modulation with constant amplitude and digital input signal.

Binary phase shift keying (BPSK) is the simplest form of phase shift keying. Two output phases are possible for a single carrier frequency, representing "1" and "0" (see figure 6.1). As the digital input signal changes states, the phase of the output carrier shift between two angles that are 180 degrees out of phase. Quadrature Phase shift keying (QPSK) is another form of angle modulated, constant amplitude digital modulation (see figure 6.1). With QPSK four output phases are possible for a single carrier frequency. The four output conditions require four different input conditions requiring two input signals to generate these. In conventional QPSK modulators, the output states are 90 degrees out of phase of each other. Quadrature Amplitude Modulation (QAM) is a form of digital modulation where both the phase and amplitude of the transmitted carrier contain the digital information. QPSK is special case of 4 State QAM or 4-QAM. The modulation does not require constant phase or amplitude, giving opportunity for more complex modulation design.
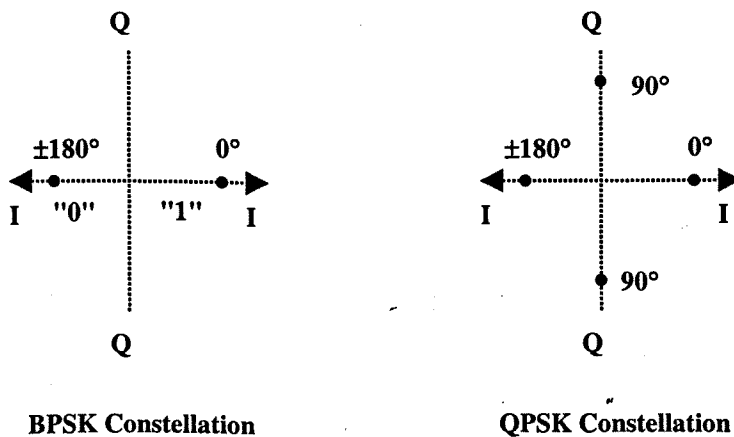

BPSK Constellation   **QPSK Constellation**

Figure 6.1: constellation diagram of BPSK and QPSK modulation.

In recent years considerable effort has been made to exhibit monolithic direct carrier modulators operating up to millimeter wave frequencies (see table 6.1). The modulators demonstrated have shown a variety of modulations ranging from simple ON-OFF switching to very complex phase and amplitude modulations. These modulators have been demonstrated by employing a variety of different

techniques. Each technique has its advantages and disadvantages with the final choice of the design technique depending on the application.

Two main design techniques have gained popularity at millimeter-wave frequencies. These are the tandem modulator and the phase-shifter/attenuator modulator [R6.2]. The phase-shifter/attenuator modulator as the name suggests consist of cascaded phase-shifters and attenuators to achieve the desired modulation. The tandem modulator uses a quadrature splitter to create two channels which amplitude modulate the signal and then combines the signals with an in-phase combiner. Both of these can be realized using reflection type circuits or double balanced mixers. Table 1 gives some recent examples of direct carrier modulators.

Modulation	Frequency	Type
QPSK[R6.3]	8-12 GHz	Reflection Topology with 10 ° of phase error
QPSK[R6.4]	8 GHz	Reflection Topology with 8 ° of phase error
QPSK[R6.5]	1-3 GHz	Double balanced mixer with 4 ° phase imbalance
64-QAM[R6.6]	6-8.5 GHz	Single balanced mixer with 1.5 ° phase error
QPSK[R6.7]	4-18 GHz	Phase shifter/Attenuater
QPSK[R6.8]	16.7-17.8 GHz	Phase shifter/Attenuater with 6.5 dB insertion loss
BPSK[R6.9]	94 GHz	Reflection Topology with 5 ° of phase error
256-QAM[R6.10]	55-65 GHz	Reflection Topology with 2 ° of phase error
64-QAM[R6.11]	77 GHz	Reflection Topology
BPSK[R6.12]	77 GHz	Reflection Topology with 5 ° of phase error

Table 6.1: Recent literature summary of direct carrier modulators

6.3   Reflection Type Modulator

In this project a reflection type topology was used for design of direct carrier modulators. The topology depends on the extensive use of couplers and becomes more effective at millimeter wave frequencies as coupler size shrinks. The other main advantages of this technique are the ease of design when compared to double balanced mixer based topologies together with the large number of modulation schemes that can be realized by using the same hardware circuit.

A typical single stage reflection type bi-phase amplitude modulator is shown in figure 6.2. The signal enters at input of the coupler and divides equally between the direct and coupled ports with 90 ° of phase-shift between them. If the two output ports are not matched but terminated with equal impedance, the signals reflected back from both ports add in phase at the isolation port and add out of phase at the input of the coupler. The input port of the coupler is the input port of the circuit and the isolation port is the output port of the circuit (see figure 6.2). Both amplitude and phase modulation can be achieved by varying the impedance at the direct and coupled ports. In this work branch-line couplers were used as 3 dB quadrature couplers and HEMTs were used as variable resistors at the output ports.
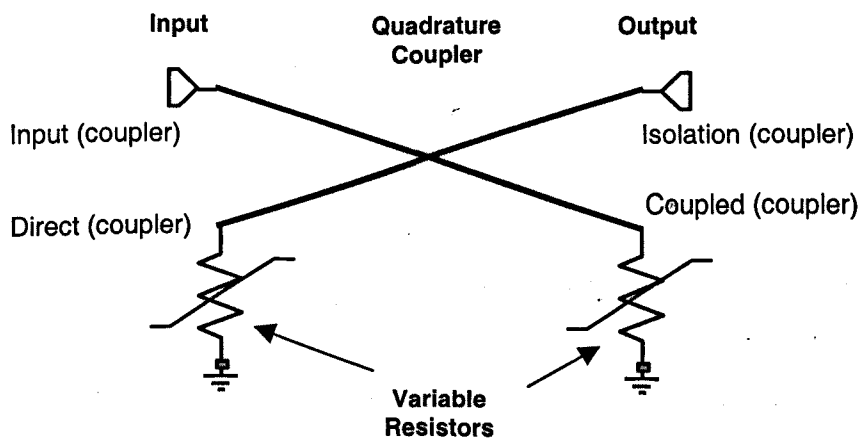

Figure 6.2: Illustration of reflection type topology

6.4 HEMT as a Variable Resistor

Depletion mode transistors in common source mode can be configured as variable resistors when operated without drain bias by varying the gate bias to modulate the channel resistance. The main advantage of using HEMTs instead of more traditional methods such as PIN diodes is the compatibility of the modulator with other sub-system building blocks to enable monolithic integration leading to single chip solution.
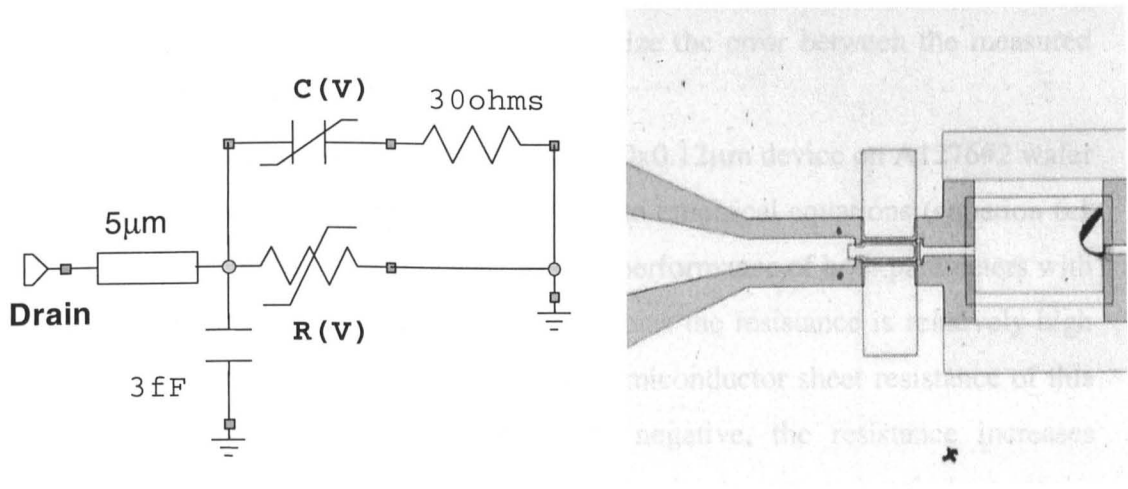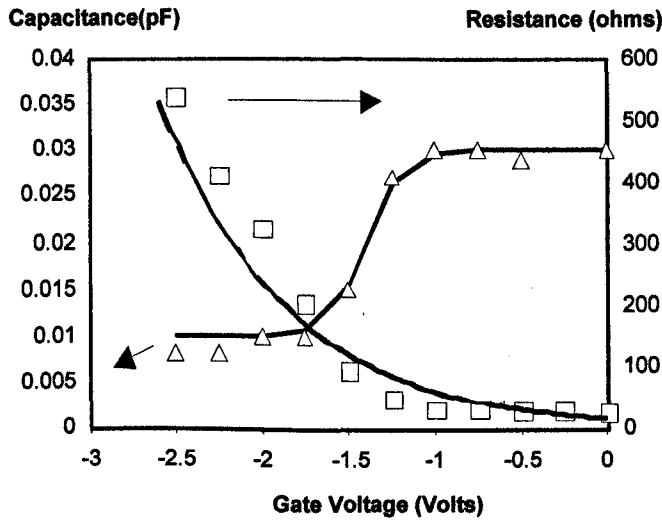

Figure 6.3: Equivalent circuit model and fabricated layout of the cold HEMT.

For ideal operation of reflection type modulator, HEMTs are needed with large source-drain resistance variation coupled with small variation in capacitance. InP based HEMTs with short gate length and reasonably small gate width meet both criteria and were characterized from DC to 60 GHz in cold bias conditions i.e. zero volts applied to the drain and the gate bias varied from open channel to pinch-off typically in the range from 0 V to -2.5 V. A 5 pF shunt capacitor was included on the gate side of the device to ensure good RF isolation and accurate reflection measurements (see figure 6.3). The measured data of a 2-finger 50 μm HEMT was fitted to the equivalent circuit model shown in figure 6.3. In the equivalent circuit R(V) represents the channel resistance and is the most dominant parameter in the circuit. In the ideal situation, the channel resistance would be modulated from short circuit to an open circuit by varying the gate bias. In reality, due to finite

ohmic resistance plus semiconductor sheet resistance and sub-threshold effects, the channel resistance can be varied from 10 Ω to 1500 Ω in a typical InP 2x100 μm HEMT. As the gate bias becomes more negative, the depletion region under the gate increases in size forcing the channel resistance to increase in a nonlinear manner. The other major parameter in the equivalent circuit is C(V) which consist of gate (C_{gs} & C_{gd}) and source-drain (C_{ds}) capacitance. The 3 fF capacitor represents the parasitic pad capacitance of the structure. The 5 μm transmission line was use to match the phase of the model and measured data. All parameters were extracted by tuning the model to minimize the error between the measured and modeled S-parameter data.

The extracted values of R(V) and C(V) of a 100x0.12μm device on A1276#2 wafer are shown in figure 6.4. This data was fitted to empirical equations (equation 6.1 & 6.2) to characterize the gate bias dependant performance of both parameters with all other parameters being constant. At zero bias the resistance is relatively high due to rather poor ohmic contacts and high semiconductor sheet resistance of this wafer. As the bias becomes increasingly negative, the resistance increases nonlinearly but does not reach a very high value due to reverse break down of the Schottky gate contact.

At zero bias the capacitor C(V) provides a larger resistance to current than R(V) as a result the current will flow through the resistor R(V) but at high negative bias the capacitor provides the low resistance path for the current and will shunt the large value resistor. Figure 6.4 shows the fit of measured S-parameters to the model of figure 6.3 at open channel (Vg=0V) and closed channel (Vg=-2.5V) bias conditions.
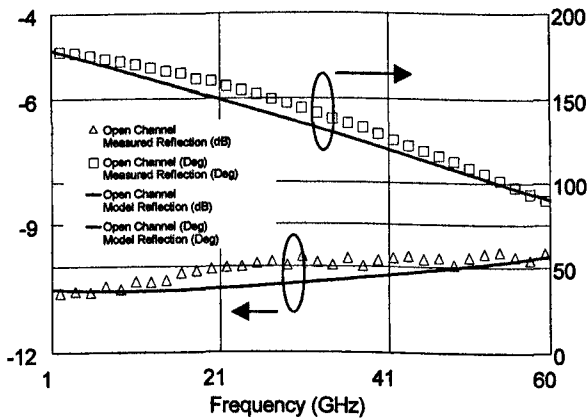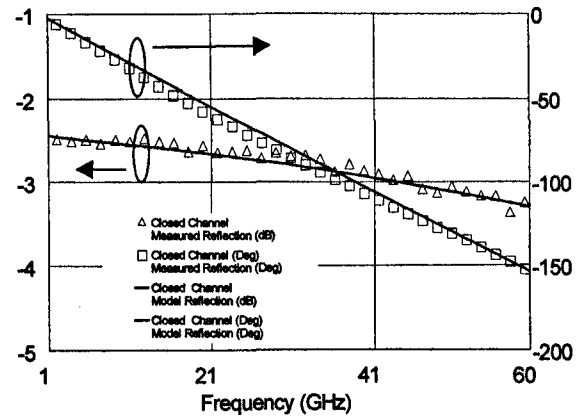
Figure 6.4: (a) Measured and empirical equation fitting of R(V) & C(V)

(b) Measured and equivalent circuit model data at open channel condition

(c) Measured and equivalent circuit model data at closed channel condition.

$$R(V) = 26 + 0.05 * \exp\left(\frac{-0.45V}{0.12}\right) \; ohms \qquad\qquad \textit{Equation 6.1}$$

$$C(V) = 0.01 * [2 + \tanh(5V + 7)] \; pF \qquad\qquad \textit{Equation 6.2}$$

6.5 Single ended Reflection type Modulator

A branch-line coupler in combination with cold HEMTs can be used to realize a bi-phase amplitude modulator. When the two HEMTs are operated in open or closed channel condition, the circuit has the lowest attenuation, as most of the signal is reflected back from the HEMT and appears at the isolation port of the coupler. These two states are referred as the two ON states of the circuit and are 180 ° out of phase. The BPSK modulation can be achieved by biasing the circuit in these states as they provide low attenuation in combination with 180° phase shift. The OFF-state of the Modulator can be achieved by biasing the HEMTs in such a way that they are providing around 50 Ω impedance. This will cause the incident signal to be absorbed by the HEMTs; hence a very small signal will be available at the output of the circuit. Between the ON-state and OFF-state, a number of other amplitudes can be achieved by varying the HEMT impedance. The circuit has the potential of working as BPSK modulator, amplitude modulator, a switch and a bi-phase amplitude modulator. The complete circuit is shown in figure 6.5. The bias resistors on the gates of the HEMTs are used to prevent RF leakage. One major problem with this circuit is that in closed channel operation, the HEMT channel resistance is shunted by the C(V) capacitance causing phase and amplitude errors in modulation.
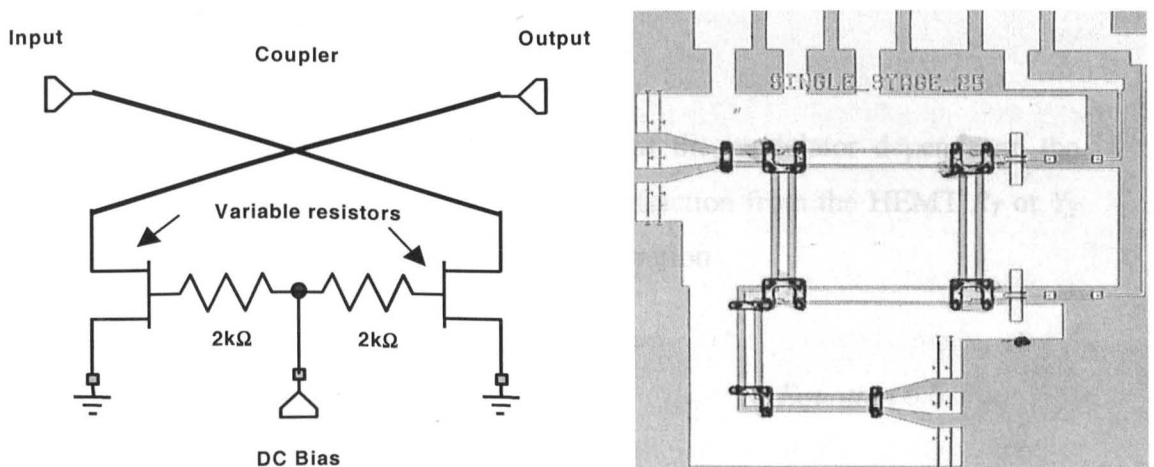

Figure 6.5. Single stage reflection type modulator

The dependence of the single ended modulator response on the parasitic capacitance is shown by Lusyszyn [R6.13]. For an ideal coupler with identical reflection terminations, the output at isolation port is given by

$$S_{21} = 2R_T S_c S_d \qquad\qquad \textit{Equation 6.3}$$

Where R_T is the reflection coefficient of reflection termination and S_c & S_d coupled and direct voltage coefficients of the coupler. This also shows that voltage wave immerging at isolation port has the same amplitude as input voltage wave but extra reactance due to reflection terminations.

The phase shift of the circuit is given by

$$\angle S_{21} = \angle S_c + \angle S_d + \angle R_T = \angle R_T + \angle S_c + 90° \qquad \textit{Equation 6.4}$$

The reflection coefficient can simply be written as

$$R_T = \frac{Y_0 - Y_T}{Y_0 + Y_T} \qquad\qquad \textit{Equation 6.5}$$

Where Y_0 is $1/Z_0$ and Z_0 is 50Ω

It is evident from above that the phase shift of the modulator depends on the reflection coefficient of the termination. The reflection from the HEMT R_T or Y_T can be approximated by resistor/capacitor combination

$$Y_T = G_T + jB_T \approx \left(\frac{1}{R(V)} + j\omega C(V) \right) \qquad \textit{Equation 6.6}$$

Substituting this into R_T

$$R_T = \left(\frac{Y_0^2 - G_T^2 - B_T^2}{(Y_0 + G_T)^2 + B_T^2} \right) - j \left(\frac{2B_T Y_0}{(Y_0 + G_T)^2 + B_T^2} \right) \qquad \textit{Equation 6.7}$$

The magnitude and phase are

$$|R_T| = \sqrt{\left(\frac{Y_0^2 - G_T^2 - B_T^2}{(Y_0 + G_T)^2 + B_T^2} \right) - j \left(\frac{2B_T Y_0}{(Y_0 + G_T)^2 + B_T^2} \right)} \qquad \textit{Equation 6.8}$$

$$\angle R_T = \tan^{-1}\left(\frac{-2B_T Y_0}{\left(Y_0^2 - G_T^2 - B_T^2\right)} \right) \qquad \textit{Equation 6.9}$$

These circuits were fabricated using the standard MMIC process where the large 2kΩ resistors were created by using semiconductor resistors. The circuits were fabricated on the wafer A1276#2 for which the cold HEMT characteristics are presented in the previous section. Figure 6.6 illustrates the measured response of the circuit as described in table 6.2. The insertion loss of the two ON-states depends on the range of the variable resistor formed by the HEMTs. For low insertion loss, a very small open channel resistance and very high pinch off resistance is required. In the case of this circuit the open and closed channel resistances were 26 Ω and 600 Ω respectively, resulting in rather high insertion loss of -10 dB at the design frequency. The phase-shift between the two ON-states is far from ideal due to parasitic capacitance of the HEMT. The rapidly changing phase difference with frequency is probably caused by unequal impedance provided by the two HEMTs. The input reflection is close to ideal for both ON states, indicating accurate operation of the coupler. The output reflection of all states is slightly shifted from ideal response due non-optimized biasing of the HEMTs but is still around -20 dB. If the circuit is operated as an attenuator then the attenuation range is around 8 dB. For BPSK operation, the phase difference between the two ON-states is 130 degrees at the design frequency.

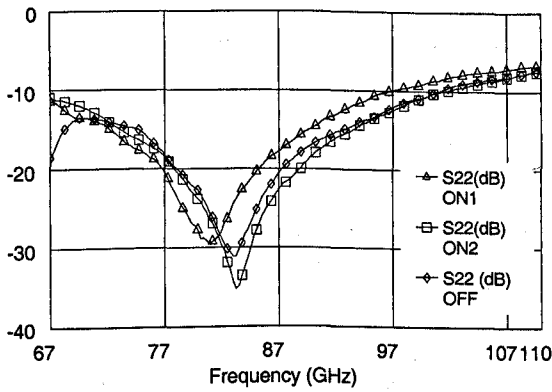| DC Bias (V)	State of HEMT	State of Circuit	Phase (°)
0	open channel	ON1	X
-2.5	closed channel	ON2	X+130
-1.5	~ 50 Ω	OFF	

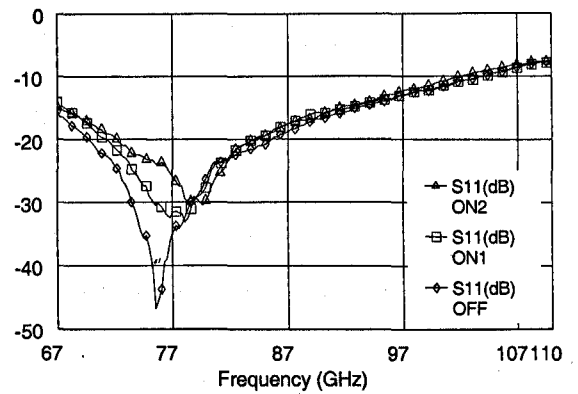Table 6.2: States of single stage modulator
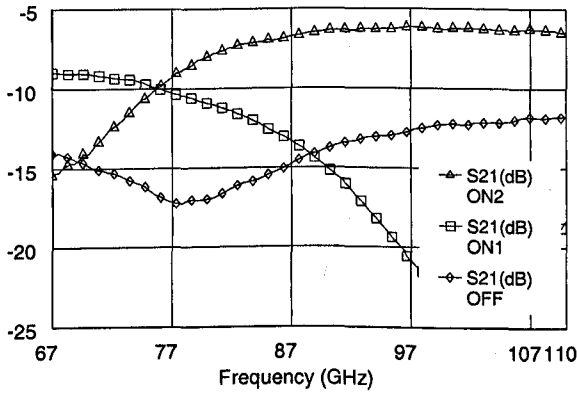
(a)
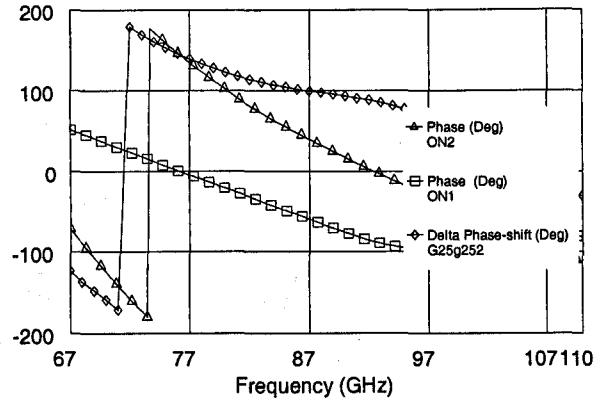
(b)

(c)

(d)

Figure 6.6: Showing the measured response of the modulator

6.6 Balanced Bi-phase Amplitude Modulator

The phase and amplitude errors of a single ended modulator can be eliminated by using a balanced modulator topology. It consists of two single ended modulators connected in parallel with branch-line couplers at both input and output (see figure 6.7). The input and output couplers ensure that the circuit will have good input/output match. The circuit theoretically has infinite number of phases and amplitudes at the output depending on the biasing of the HEMTs.
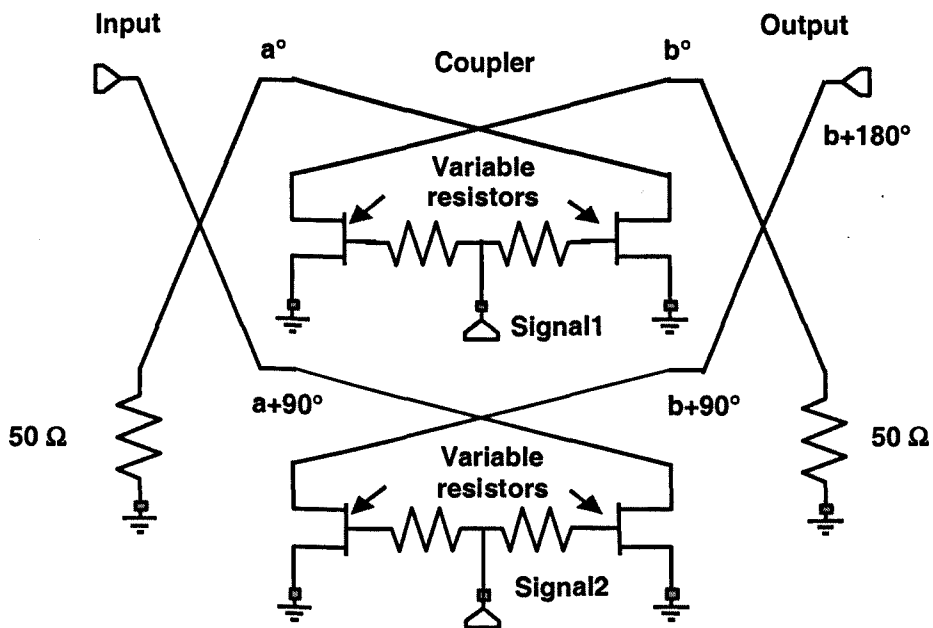

Figure 6.7: Circuit diagram of balanced bi-phase amplitude modulator
The phase labels are in the case when all 4 HEMTs have the same bias

Signal 1 (V)	Signal 2 (V)	Circuit State	Circuit Phase (°)
0	0	OFF1	
0	-2.5	ON1	X
-2.5	0	ON2	X+180
-2.5	-2.5	OFF2	

Table 6.3: Summary of BPSK and switching operation of balanced modulator.

To simplify the biasing of the circuit, it is desirable that each pair of HEMTs connected to a coupler are matched. In this ideal situation when both signal 1&2 in figure 6.7 are zero Volts (i.e. all four transistors are open channel), then the RF signal at the input coupler divides equally between the two arms with 90 degree of phase shift (phases are labeled in figure 6.7). As both single ended modulators have the same state, they perform the same phase-shift. The input signals to the output coupler combine at the output port but with a further 90° of phase-shift, resulting in cancellation of the input signals at the output. This is referred to as the OFF State of the circuit. In all cases where all four HEMTs have the same reflection coefficient, the circuit will be in an OFF-state because the balanced topology causes the single ended modulators to add in 180-degree phase difference. The ON state of the circuit can be achieved by having Signal1=-2.5V (both HEMTs in closed channel state) and Signal2=0V. The signal again divides equally between the two arms of input coupler before passing to the two modulators. In this case the single ended modulators have different phases as shown in the last section, resulting in the signals at the output to add in phase (ON1). The same response can be achieved by using Signal2=-2.5V and Signal1=0V (ON2). There is natural 180 ° phase-shift between the two ON states because of the 180 phase difference between the two arms. These states are summarized in table 6.3.

The circuit was fabricated on A1276#2 and measured after LRRM calibration using an ISS wafer. The measured characteristics are shown in figure 6.8. The ON states are within 0.5 dB of each other over 10 GHz frequency range. The high insertion loss in the ON states is due to small channel-resistance variation of HEMTs in this wafer mainly caused by non-ideal Ohmic contacts, high sheet resistance and poor schottky contacts . The OFF State is measured to be greater than –40 dB at the design frequency giving an ON-OFF isolation of better than 25 dB. This circuit therefore provides ideal characteristics for an attenuator. The phase difference between the two ON states was measured to be 172°. To enable the biasing of all four HEMTs, circuit was rotated during the measurements of the ON states. It is expected that at least ±5° of phase error might due to change of

probe positioning between measurements. Both input and output reflections of the circuit have shifted from design frequency. The main cause for these shifts are non-ideal 50Ω isolation resistors and unmatched HEMT pairs. The OFF state shift is most likely due to isolation resistors as unbiased HEMTs across the wafer were found have very similar responses. The ON-state shifts are combination of the impact of the isolation resistors and lack of matching of HEMTs providing unequal reflection coefficient. In all cases, the reflections at the design frequency were measured to be better than −17 dB.
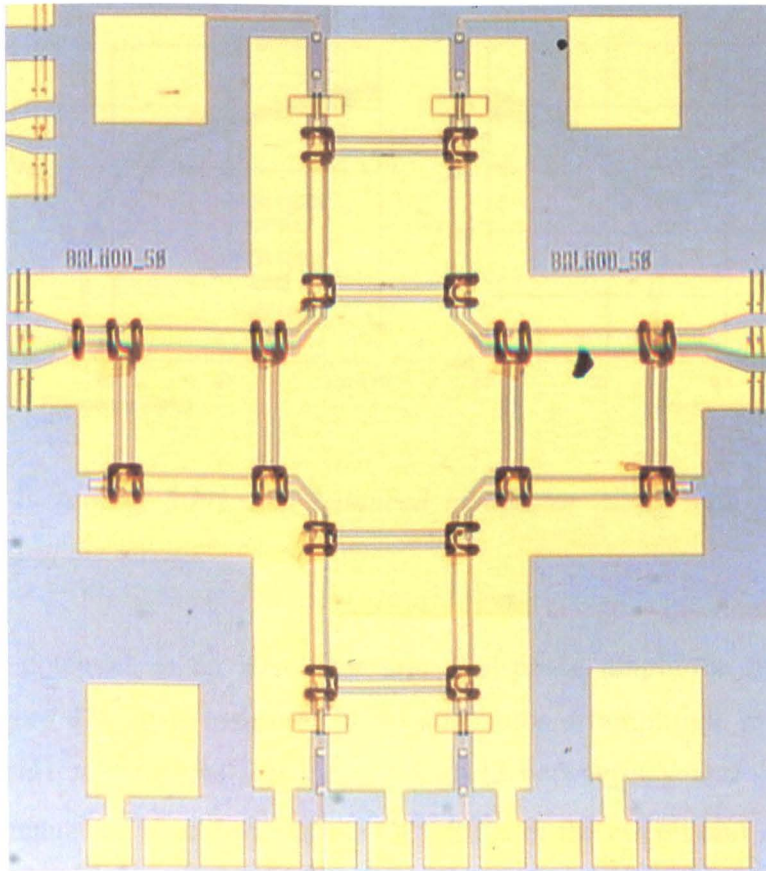

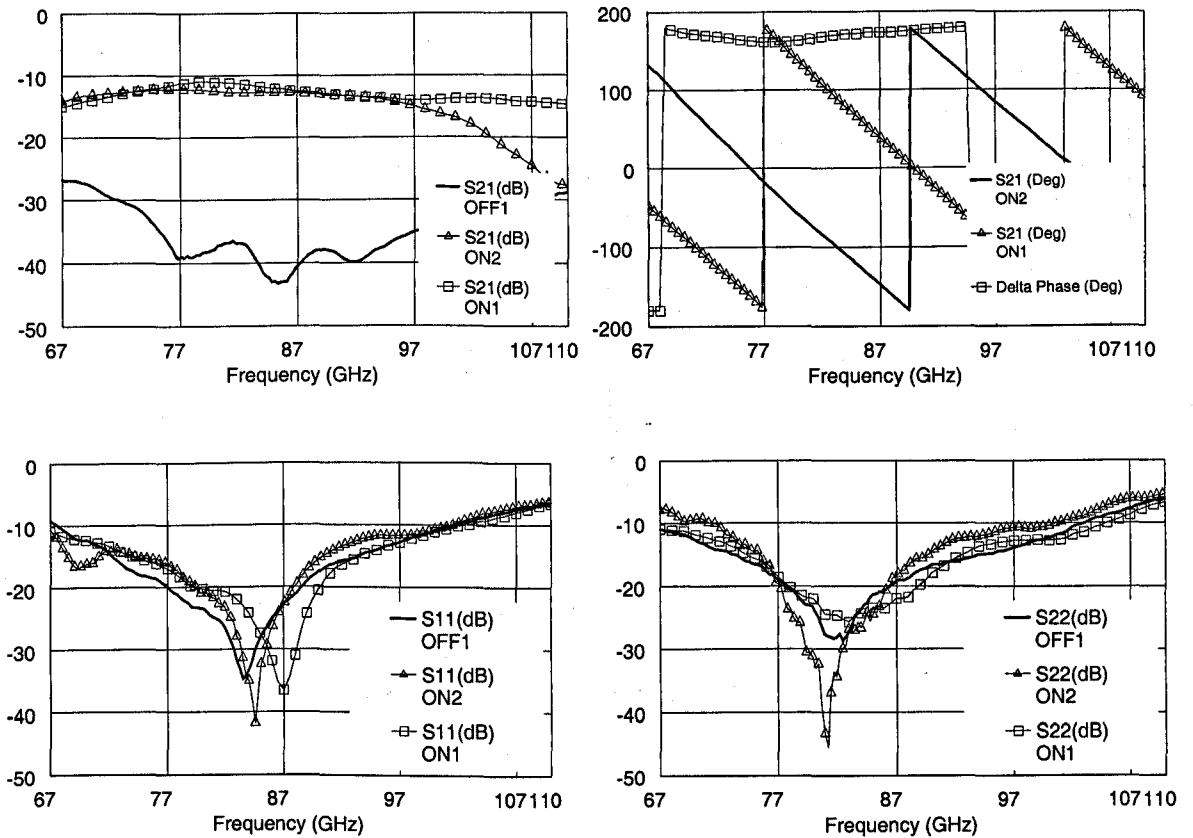
Figure 6.8: continued on next page

Figure 6.8: Picture of fabricated balanced modulator along with S-parameter measurements of the circuit.

The circuits potential as an attenuator and a bi-phase amplitude modulator is shown in figure 6.9. It is measured as an attenuator or amplitude modulator by keeping Signal1 at zero bias and varying Signal2 between 0V and –2.5V. The maximum attenuation is achieved at the OFF State of the circuit and minimum at the ON-states of the circuit. By varying Signal1 in a similar fashion and keeping Signal2 constant at zero bias gives approximately the same attenuation but a 180 ° phase shift. This gives the complete spectrum of a bi-phase amplitude modulator, which is demonstrated on a polar plot. On the polar plot each point represents phase and magnitude of the circuit at 77 GHz with a certain level of bias applied.
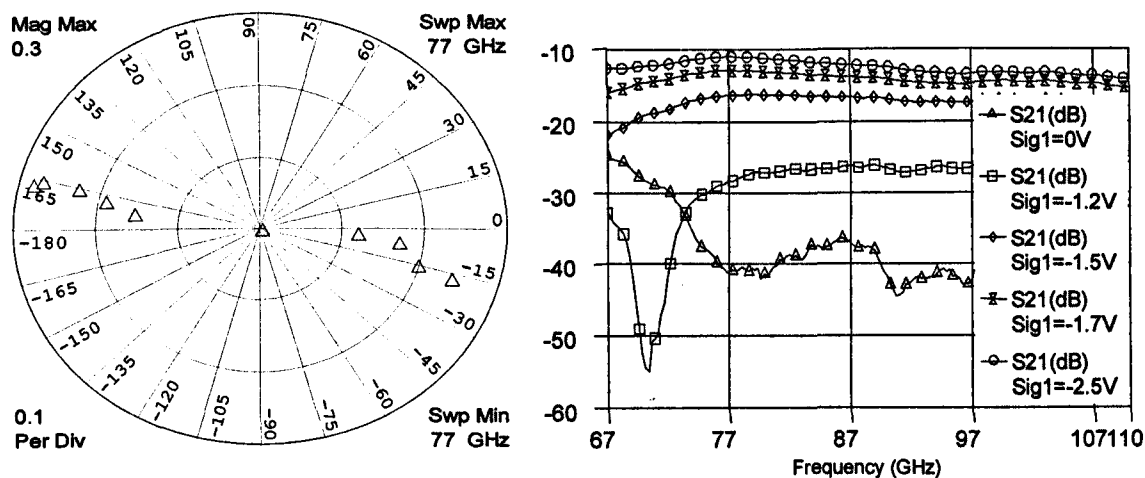
Figure 6.9: Polar plot is of a bi-phase amplitude modulator where the left data points represents varying Signal2 and right data is varying Signal1. The centre point is representing OFF state. The rectangular graph is giving the attenuation with varying signal1 and zero bias Signal2.

6.7 I-Q Vector Modulator

I-Q vector modulators can be realized by using two BPSK modulators in parallel with a branch-line coupler at the input and an in phase combiner at the output. The branch-line coupler creates two orthogonal channels as shown in figure 6.10, which contain bi-phase amplitude modulators. The output signals from these modulators are combined using an in-phase combiner. " Although single ended modulators can be used to realize an I-Q modulator but their non-ideal performance makes them unsuitable for complex digital modulation schemes such as heavy QAM schemes. Balanced modulators have been used to demonstrate 256-QAM at 60 GHz because of their near perfect BPSK constellation and large attenuation range to allow more amplitude modulation states to occur [R6.14]. The circuit diagram for an I-Q vector modulator is shown in figure 6.11. QPSK modulation achieved by using this circuit is summarized in table 6.4.
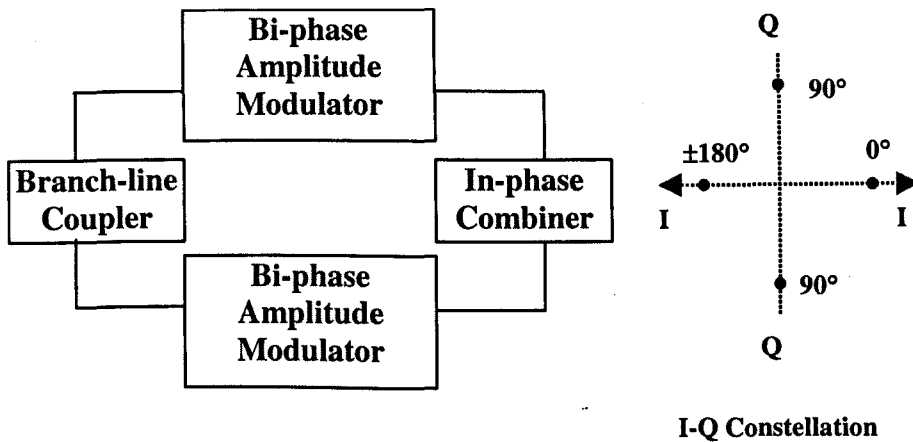
Figure 6.10: Block diagram of I-Q vector modulator

In the circuit, a Wilkinson divider was used as power combiner as it provided better performance than rat-race coupler as described in chapter 5. A completed I-Q vector modulator circuit fabricated in this project is shown in figure 6.12. The circuit was measured for QPSK response after an LRRM calibration. The data is shown in figure 6.12 at the design frequency of 77 GHz. The OFF state was measured to be better than −35 dB which is similar to balanced BPSK modulator. The input and output reflection coefficients for all states were measured to be better that −14 dB. The minimum reflection at the input is shifted from design frequency due to isolation resistor. The ON state insertion loss was between −17 to −20 dB again primarily due small resistance variation of cold HEMTs. Another possible reason for high insertion loss could be the 400 nm thick bond pad metal which was used to improve yield of circuits by simplifying the liftoff process for the final metal. This thin metal probably contributes more to insertion loss in physically big circuits such as I-Q modulator. There is significant amplitude variation in the ON states mostly due to non-ideal behavior of the transistors. Ideally a phase difference of 90 ° should exist between the ON states but this is only the case for ON3 & ON4. The other two ON-states (ON1 and ON2) are more lossy and have non ideal phase response due to varying transistor behavior.

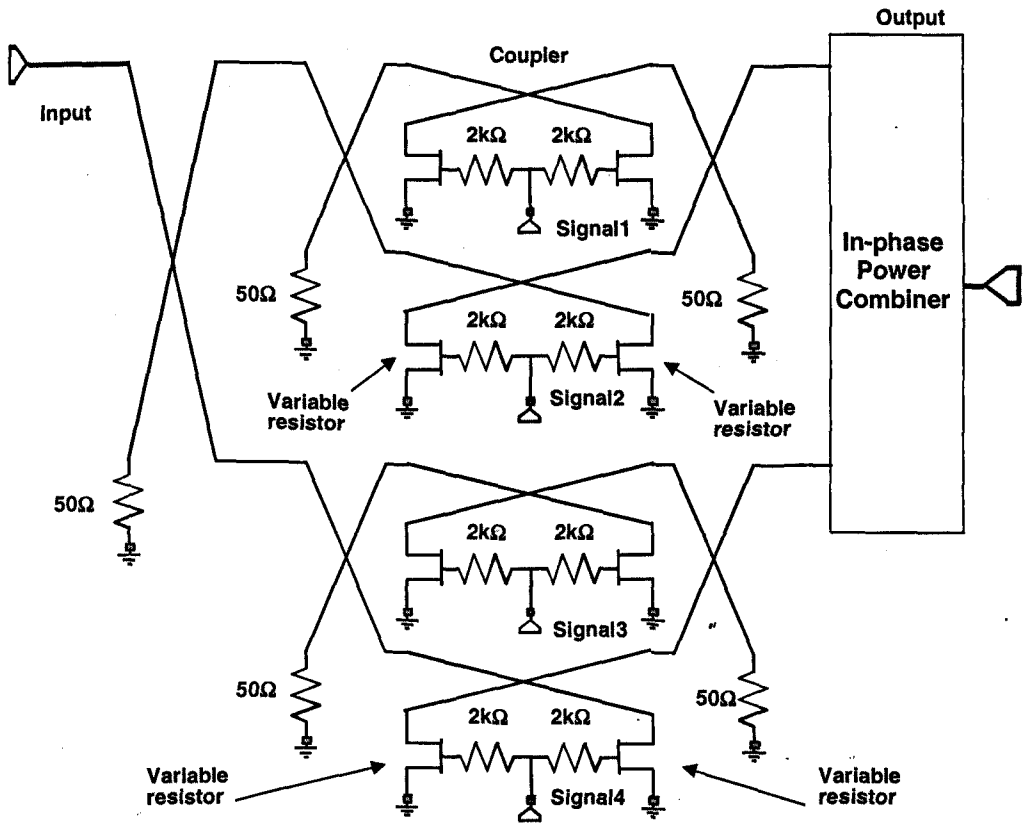| Signal1(V)	Signal2(V)	Signal3(V)	Signal4(V)	State	Phase shift
0	-2.5	0	-2.5	On(1)	X
0	-2.5	-2.5	0	On(2)	X+90
-2.5	0	-2.5	0	On(3)	X+180
-2.5	0	0	-2.5	On(4)	X+270
-2.5	-2.5	-2.5	-2.5	Off1	
0	0	0	0	Off2	

Table 6.4: Summarization of QPSK operation

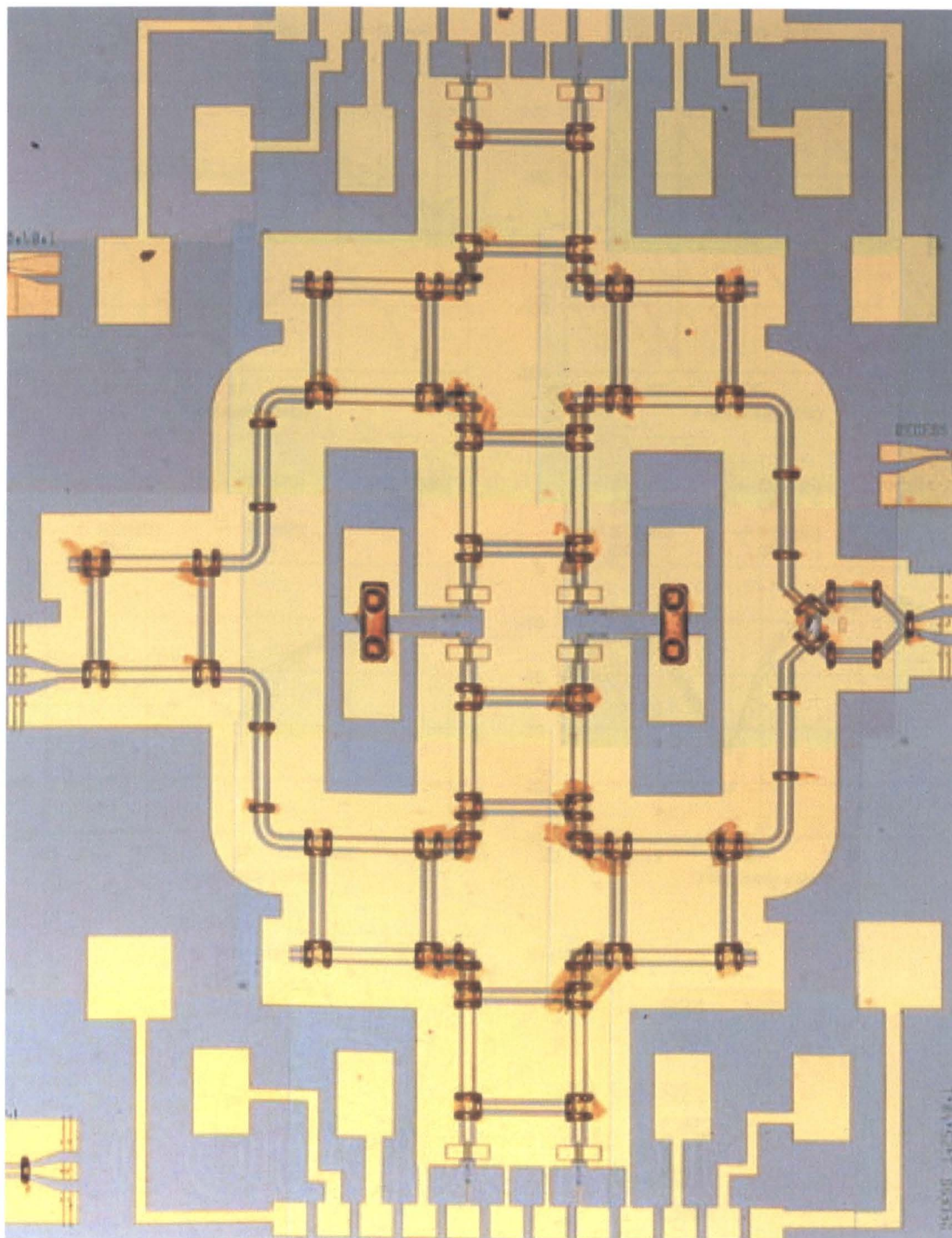Figure 6.11: Circuit diagram of I-Q vector modulator
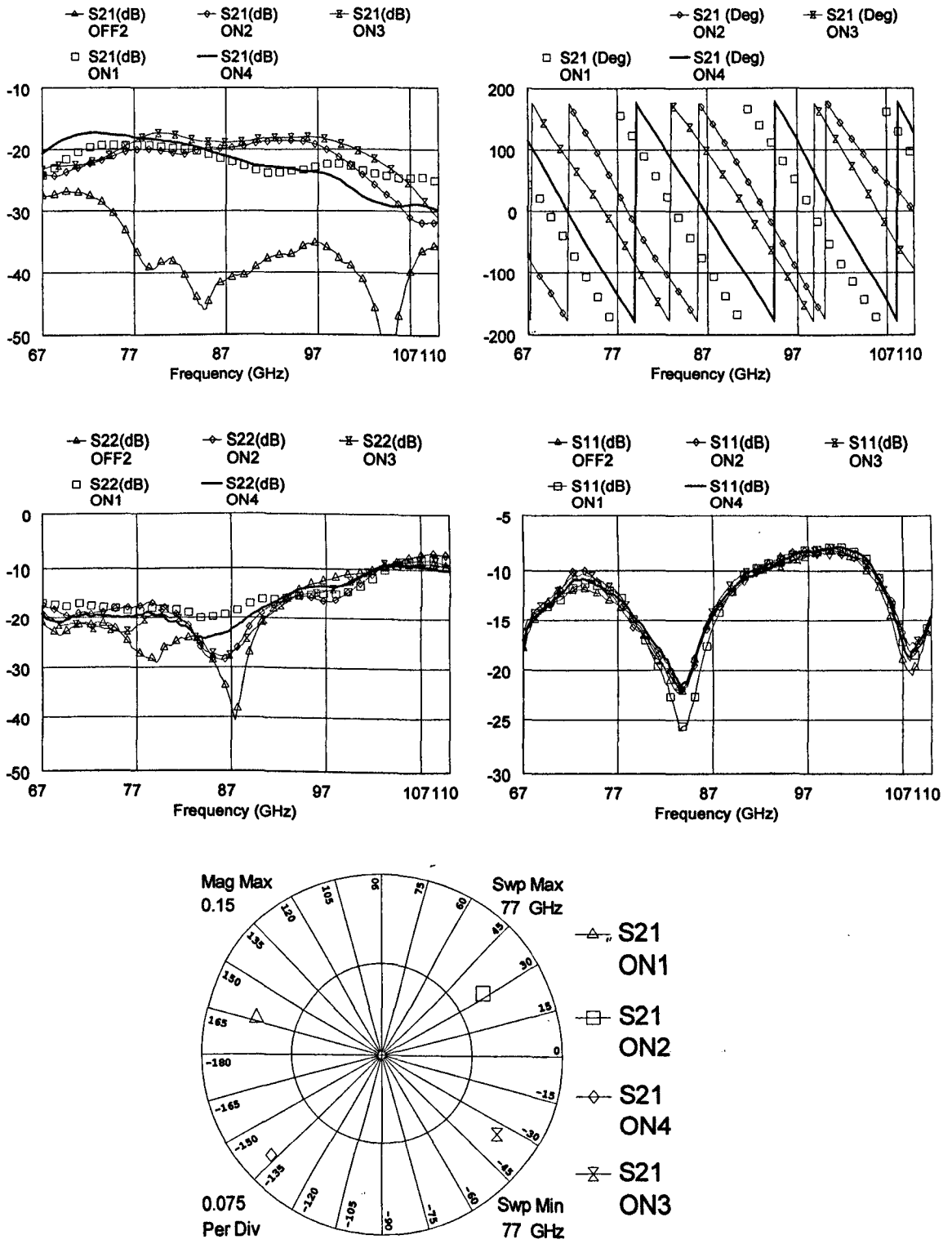
Figure 6.12: Fabricated I-Q vector modulator

Figure 6.13: Measured data of I-Q vector modulator when operated as in QPSK scheme as shown in table 6.4.

The same circuit was biased to achieve 16-QAM modulation. To maintain low input/output reflections, it is necessary to maintain the same biasing strategy as the QPSK scheme. Operating the HEMTs at different bias levels rather than the open and the short channel conditions can gain extra states. There are potentially four signals that can be biased to give 16 states (see figure 6.11).

Signal1(V)	Signal2(V)	Signal3(V)	Signal4(V)	State
-2.7	0	-2.8	0	A9
-2.6	0	-2.6	0	A8
-2.4	0	-2.4	0	A7
-2.2	0	-2.2	0	A6
-2.8	0	0	-2.8	B8
-2.6	0	0	-2.6	B6
-2.4	0	0	-2.4	B4
-2	0	0	-2	B1
0	-2.6	0	-2.6	C2
0	-2.3	0	-2.3	C5
0	-2.5	0	-2.8	C6
0	-2	0	-2	C7
0	-2.3	-2.3	0	D6
0	-2.4	-2.4	0	D5
0	-2.6	-2.6	0	D2
0	-2.5	-2.5	0	D1
0	-2.5	0	0	E2
0	-2.7	0	0	E3
0	0	0	-2.5	E8
0	0	0	-2.7	E9
-2.5	0	0	0	E11
-2.7	0	0	0	E12

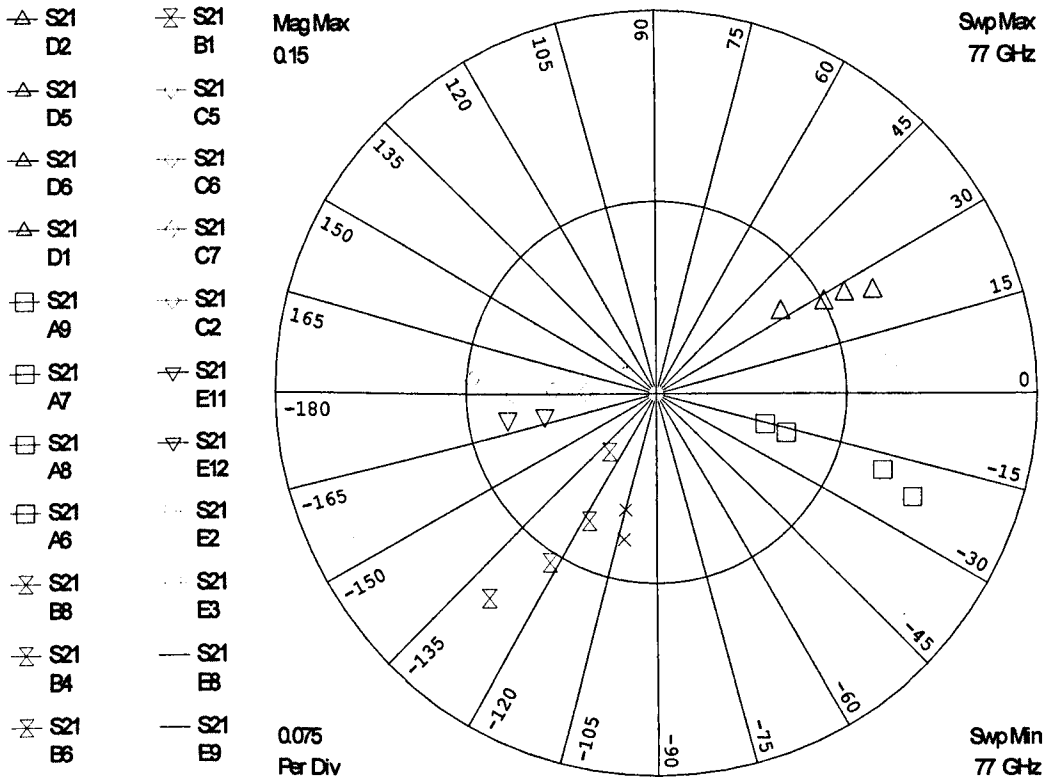*Table 6.5: Summary of 16-QAM biasing*

Figure 6.14: show 22 possible states that can be used for 16-QAM modulation at 77 GHz.

All the states in table 6.5 are shown on the polar plot in figure 6.14. The amplitude modulation was achieved by reducing the bias on the pinched off HEMTs from QPSK modulation biasing. Phase shift with constant amplitude was very difficult to achieve as one of the transistors was not working as expected.

6.8 Summary

This chapter has illustrated design, operation and measurements of CPW based direct carrier modulators. Reflection type circuits in combination with HEMTs as variable resistors have been used to demonstrate the modulator circuits. Different modulation schemes are explained and modulators made have demonstrated BPSK, QPSK, QAM modulations.

6.9 References

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[R6.9] D.Lo, "Noval Monolithic Multifunctional Balanced Switching Low Noise Amplifier", IEEE Trans. MTT, vol. 42, pp.2629-2634, 1994.

[R6.10]   S.Nam, et al., "A 60 GHz 256 QAM Balanced Modulator for Short Range LOS Communication Application", IEEE MTT-S Digest, pp.215-218, 1998.

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[R6.13]   S.Lucyszyn et al., "Analogue Reflection Topology Building Blocks for Adaptive Microwave Signal Processing Applications", IEEE Trans. Microwave Theory & Tech., Vol 43, NO.3, pp601-611, 1995.

[R6.14]   S.Nam, et al., "A 60 GHz 256 QAM Balanced Modulator for Short Range LOS Communication Application", IEEE MTT-S Digest, pp.215-218, 1998.

7 CPW Amplifier

7.1 Introduction

Amplifiers are used in any microwave system where enlarging of power or amplitude of the signal is needed. Amplifiers are commonly used in transmitters after up-conversion to increase the power of the signal. They are also used in receivers to increase the amplitude of a weak signal to extract information from it. This chapter covers practical design of a small signal amplifier. It covers single ended and balanced amplifier designs including integration of these with modulators to produce switching amplifiers.

7.2 Amplifier Topologies

Amplifiers are probably most researched component in the millimeter wave frequency range. Like all other microwave components its design is dependent on the application and specification requirements. There are four main amplifier topologies regularly used at millimeter-wave frequencies. Each of them has advantages and disadvantages where the final topology choice depends on the application (see table 7.1).

Amplifiers	Noise Figure	Bandwidth	I/O match	Stability
Reactive match	Good	Narrow	Poor	Poor
Lossy match	Poor	Wide	Good	Good
Balanced	Good	Wide	Good	Good
Feed back	Good	Wide	Good	Good

Table 7.1: Performance comparison of amplifier circuit topologies

Reactively matched amplifiers use purely reactive matching to achieve amplification and have been shown to provide the best gain and noise figure of all amplifiers but they suffer from instability, non-flat gain response and narrow bandwidth [R7.1]. The lossy matched amplifier use resistors as matching elements and tend to suffer from poorer gain and noise figure when compared to reactively matched amplifier. They have however shown excellent gain flatness over large bandwidth combined with excellent stability. Feedback amplifiers have the smallest chip size and provide excellent overall performance all round. The gain of the amplifier is lower than the reactively matched amplifier due to the feedback [R7.2]. The balanced amplifier tends to give the best overall performance but requires a large chip area. The match in a balanced circuit is good because of the input/output couplers. This gives extra freedom in optimizing other design parameters such as gain, bandwidth and noise figure. The paper by Nam compares

some of these topologies in millimeter-wave frequency range on the same substrate [R7.3].

7.3 Amplifier Figure of Merits and Specification

In this project, the aim was to design a small signal amplifier using an InP lattice matched HEMT technology. The most important parameters in the design of the small signal amplifier are the power gain, bandwidth, stability, input / output match and noise figure. The power gain is defined as the ratio of power dissipated in the load to the power supplied from the source. In MMIC small signal amplifiers, transistors are used as gain elements and the gain of the overall system depends on how the active devices are matched.

Amplifier bandwidth is the range of frequency over which the gain is constant and input/output reflections are very low. In all circumstances to improve the bandwidth of the amplifier, power gain is reduced.

The stability of an amplifier is a measure of its resistance to oscillation. An amplifier is unconditionally stable if its input and output impedance are positive for any passive terminations. Input / output match is essential for MMIC subsystems as good matching ensures that very little input/output signal is reflected, potentially effecting the performance of other components being used in the system. Amplifier noise figure is the ratio of input and output signal to noise ratio.

All these parameters of the amplifier are inter-dependant and to improve one parameter, some others degrade. It is the job of the designer to balance these parameters mentioned above for the desired application. In this project the small signal amplifiers were designed without optimization of noise figure as no transistor noise figure data was available. The typical specification of millimeter-wave small signal amplifier is summarized in table 7.2 [R7.4].

Amplifier parameters	Specification
Gain	Better than 20 dB
I/O match	Better than 10 dB
Stability	Stable across all frequencies
Bandwidth	≈ 4 GHz

Table 7.2: Amplifier specification [R7.4]

7.4   Active Device in Amplifier Design

The amplifier was designed around a 2 x 0.12 μm x 50 μm InP lattice matched HEMT. The model for this device is shown in table 3. The HEMT model has been successfully used in past to design a 94 GHz low noise amplifier [R7.4]. The device has a f_T of 180 GHz and MAG of 11 dB at 77 GHz. The operating bias of the transistor is zero volts on the gate and 1.5 volts at the drain.

Equivalent Circuit Parameters at Vds=1.5V & Vgs=0V									
Cgs	Gm	Cgd	Tau	Cds	Cpgd	Cpg	Cpd	Rs	Ls
60 fF	55 mS	5 fF	0.42 p	21 fF	2 fF	2.2 fF	1.8 fF	3.4Ω	0.1 pH
Lg	Rd	Ld	Rg	Rgs	Rgd	Gll	Glz	Dll	Dlz
7.8 pH	1.3Ω	0.1 pH	6.7 Ω	1 MΩ	25Ω	10μm	10 Ω	50μm	20Ω

Table 7.3: Equivalent circuit model of LM HEMT (S-parameter data for the HEMT was courtesy of D.Edgar)

The MAG of the HEMT can be calculated from measured S-parameters by the following equation

$$MAG = \frac{S_{21}}{S_{12}}\left(K + \sqrt{K^2 - 1}\right)$$ Equation 7.1

Where

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} \quad \textit{Equation 7.2} \quad \Delta = S_{11}S_{22} - S_{21}S_{12} \quad \textit{Equation 7.3}$$

K is Rollet's stability factor, which if greater than unity indicates, the HEMT is unconditionally stable irrespective of the input/output matching network, or if less than 1, implies the HEMT can be made stable by suitable matching load and source impedance [R7.5]. Another figure of merit for the stability of a 2 port network are the geometric stability parameters MU1 and MU2. The condition for unconditional stability can be determined by verifying whether MU1 or MU2 are greater than unity [R7.6].

$$MU1 = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta| + |S_{21}S_{12}|} \qquad \textit{Equation 7.4}$$

$$MU2 = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^* \Delta| + |S_{21}S_{12}|}$$
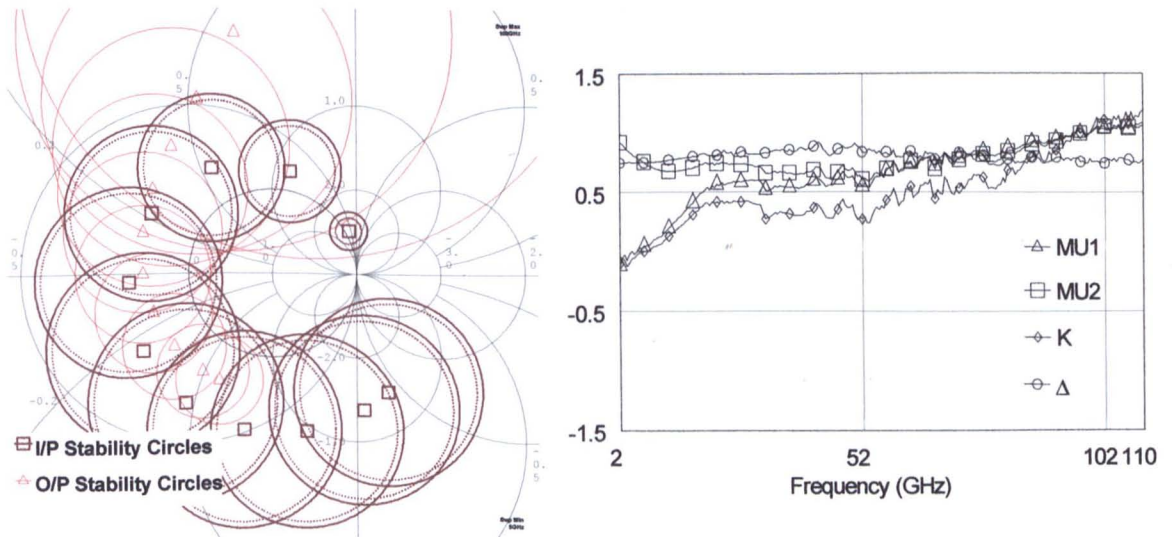

Figure 7.1: The Smith chart shows the input & output stability circles of the HEMT from 5-110GHz, where stable match is available outside the circles. The rectangular graph shows all 4 stability parameters of the unmatched HEMT.

7.5   Circuit Design of single ended amplifier

The specification of the amplifier required a three-stage amplifier to achieve the desired gain. A reactively matched topology was used because it has been successfully used in demonstrating a W-band InP HEMT amplifier and in addition it has the potential to offer low noise characteristics [R7.7]. The reactively matched amplifier only uses purely reactive elements for matching networks. For W-band design, distributed elements are preferred to lumped elements because these offer lower parasitics and are compact. The circuit design was performed in Touchstone, using extracted small signal equivalent circuit models for transistors, discontinuities, capacitors and resistors. The complete circuit is shown in figure 7.2.
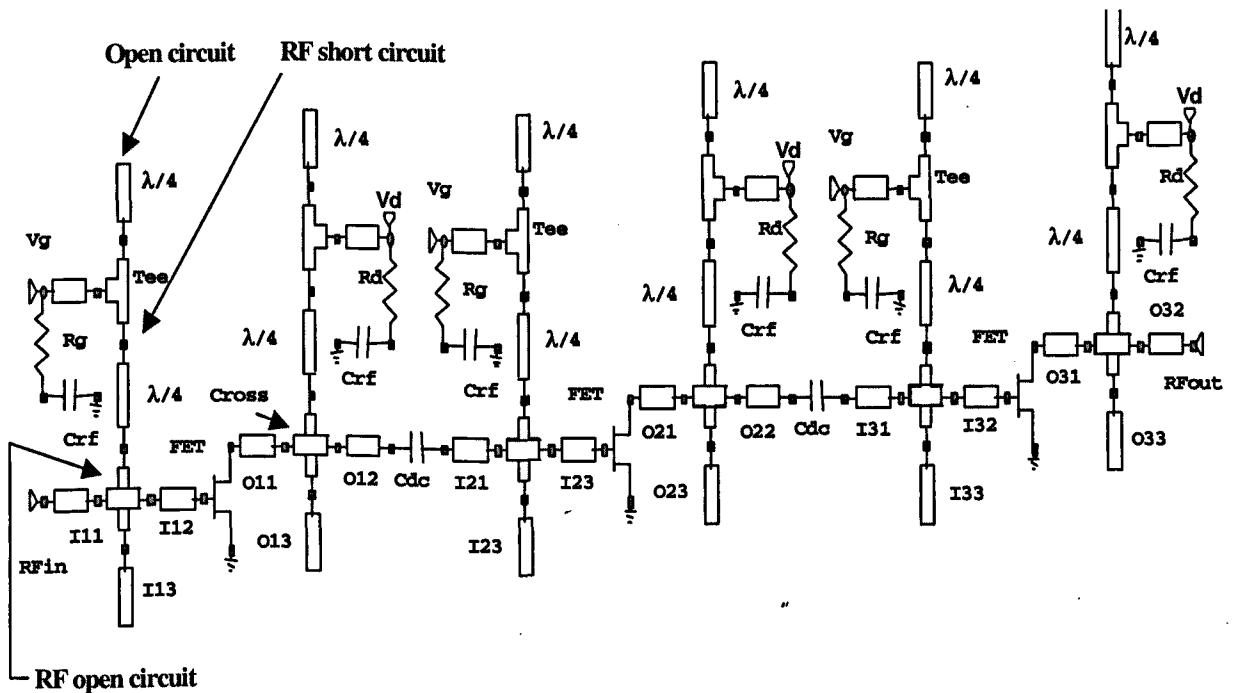

Figure 7.2: Schematic of a three stage reactively matched amplifier

Each HEMT is matched at input/output with 50 Ω stubs (I13, O13, I23 etc.). The DC bias to the transistor is applied through a high impedance (80 Ω) λ/4 stub. This stub provides a DC supply path to voltage source and presents an open circuit to the RF signal at the design frequency. The high impedance line is used to avoid any RF coupling and is shorted at the design frequency by an open circuited λ/4

transmission line [R7.8]. There is a shunt capacitor for RF short-circuiting and a stabilizing resistor in the path to the bias supply. The resistor provides out of band stability to the transistors without effecting the in-band performance. This is required as the InP HEMTs have very large gain at very low frequencies, which can cause instability. At low frequency the reactance of loss less networks is very low, as a result the transistor is loaded with the resistor which lowers its gain thus improving stability. During designing the input of the first transistor and output of third transistor are matched to provide very low reflections at both input and output of the circuit. All other matching networks are optimized for maximum gain with stability.
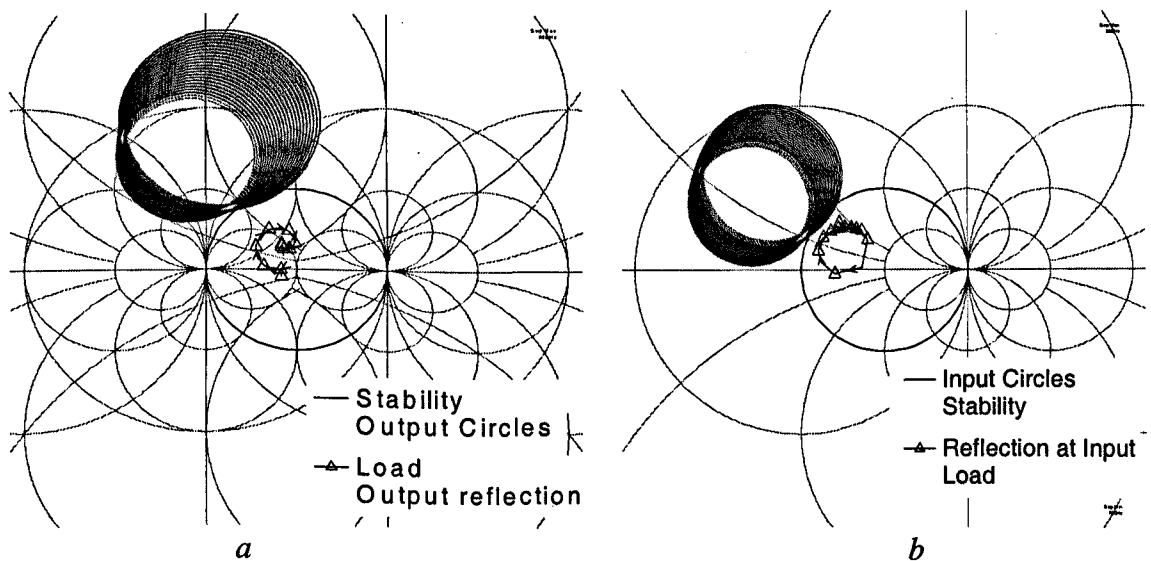

Figure 7.3: (a) Shows output stability circles of HEMT and the reflection at the output of the HEMT in stage 1. (b) The input reflection of the HEMT in stage 3 and the input stability circles of the device.

Most of the effort in amplifier design was spent on making the amplifier stable across all frequencies. Making the three stage circuit stable is a relatively easy task but ensuring that all the HEMTs are properly terminated to avoid internal oscillations is quite difficult and time consuming. Figure 7.3a shows the output stability circles of the HEMT and output reflection the first stage HEMT faces

from all the circuitry present at its output. The match is clearly in the stable region of the Smith chart and should not suffer from internal oscillation. Similarly figure 7.3b is shows the reflection seen by the third HEMT at input from all the circuitry and it is also in stable region of Smith chart.

The final optimized response of the circuit is shown in figure 7.4(a). It meets the specifications of gain, stability, and input / output match. The design gain was found to be 24 dB at 77 GHz. The S22 and S11 are better than −15dB at the design frequency. The measurements in figure 7.4(b) show the stability of each stage represented by amp1, amp2 and amp3 and the stability of the total amplifier. All the component values of the amplifier are listed in table 7.4.

Component	Value	Component	Value
$\lambda/4$	385 μm	I11	300μm
Rg	50 Ω	I12	440μm
Rd	100 Ω	I13	160μm
Crf	3 PF	O11	300μm
Cdc	125 fF	O12	140μm
I21	10μm	O13	10μm
I22	160μm	I31	10μm
I23	450μm	I32	160μm
		I33	500μm
O21	250μm	O31	380μm
O22	10μm	O32	230μm
O23	460μm	O33	300μm

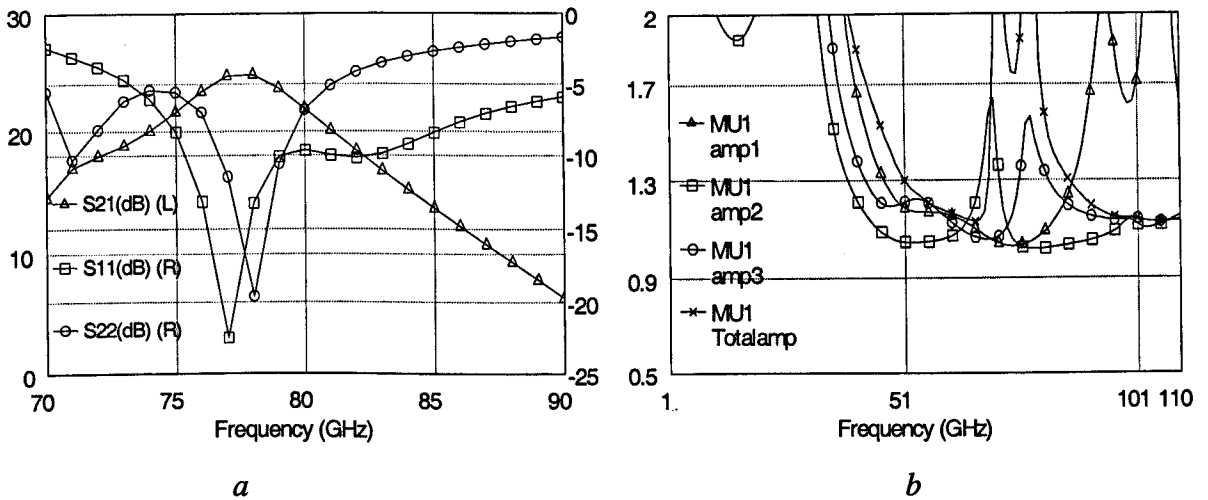*Table 7.4: Component values of amplifier*

Fig.7.4: (a) Gain and matching of 3-stage amplifier, (b) Stability performance of all amplifier stages.

7.6 Sensitivity Analysis

Sensitivity analysis is an essential part of the MMIC design cycle. There are many parameters involved in design of an amplifier and it is essential to know how each effects the response of the circuit due to changes in them caused by tolerances in the fabrication process.

The amplifier response is not effected significantly by small (< 1 μm) changes in the size of transmission lines. The design can tolerate 25% change in resistor value and still keep the amplifier stable. Semiconductor resistors are used in the amplifier and variations arise due to contact and sheet resistance changes. The capacitors are very much likely to change due to unpredictable nitride deposition thickness. The shunt capacitor (Crf) is quite large and insensitive to changes but a 100 % change in the DC block capacitor value degrades the input/output match. Another possible variation in passive elements can arise from air bridging where extra metal can increase capacitance at discontinuities. This will cause a slight shift in input and output match but does not effect the gain significantly.
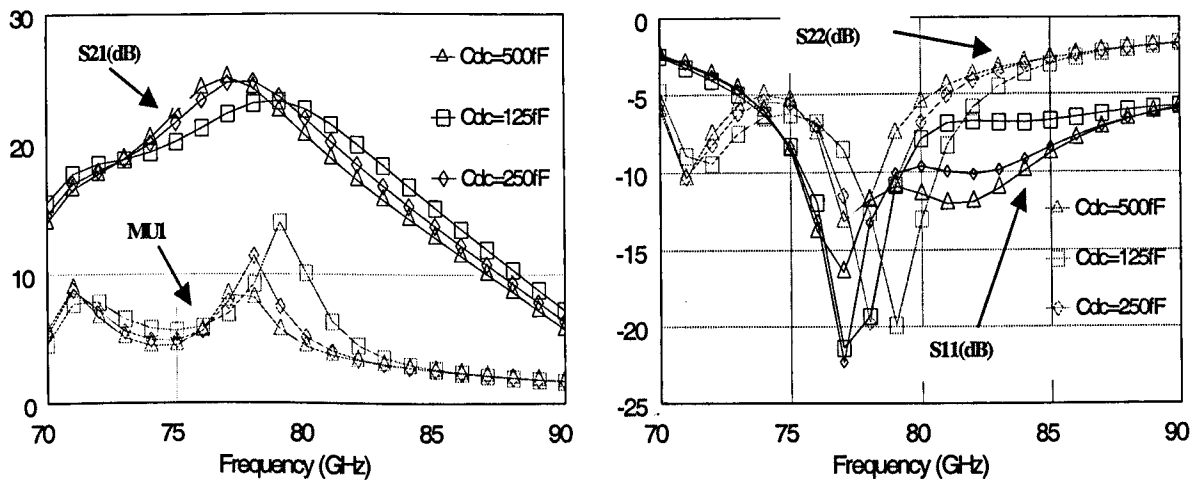
Figure 7.5: Effect of DC Block capacitor on amplifier response

The performance of the amplifier is most sensitive to the properties of the HEMTs. Clearly for the amplifier to meet specification, the intrinsic HEMT must have good characteristics and these are dependent on the quality of semiconductor material and fabrication processes. Virtually all elements of the HEMT equivalent circuit effect the gain, stability and input/output match of the amplifier. Table 7.5 shows the sensitivity of HEMT equivalent circuit parameters for the amplifier specification. The HEMT parameters that are most likely to change are Cgd, Cgs, gm, Rs and Ri since these depend on the shape of the gate recess which is difficult etch to control with the process used. Figure 7.6 shows the effect of varying the transconductance, gate resistance, gate-drain capacitance on amplifier performance.

HEMT Parameters and their sensitivity to amplifier design									
Cgs	Gm	Cgd	Rd	Cds	Ri	Rg	Rds	Rs	Lg
60 fF	55 mS	5 fF	1.3Ω	21 fF	6.4 Ω	6.7 Ω	393Ω	3.4Ω	7.8 pH
21%	15%	37%	200%	15%	70%	100%	25%	41%	250%

Table 7.5: Shows the variation in equivalent circuit parameter values before amplifier is out of specification.
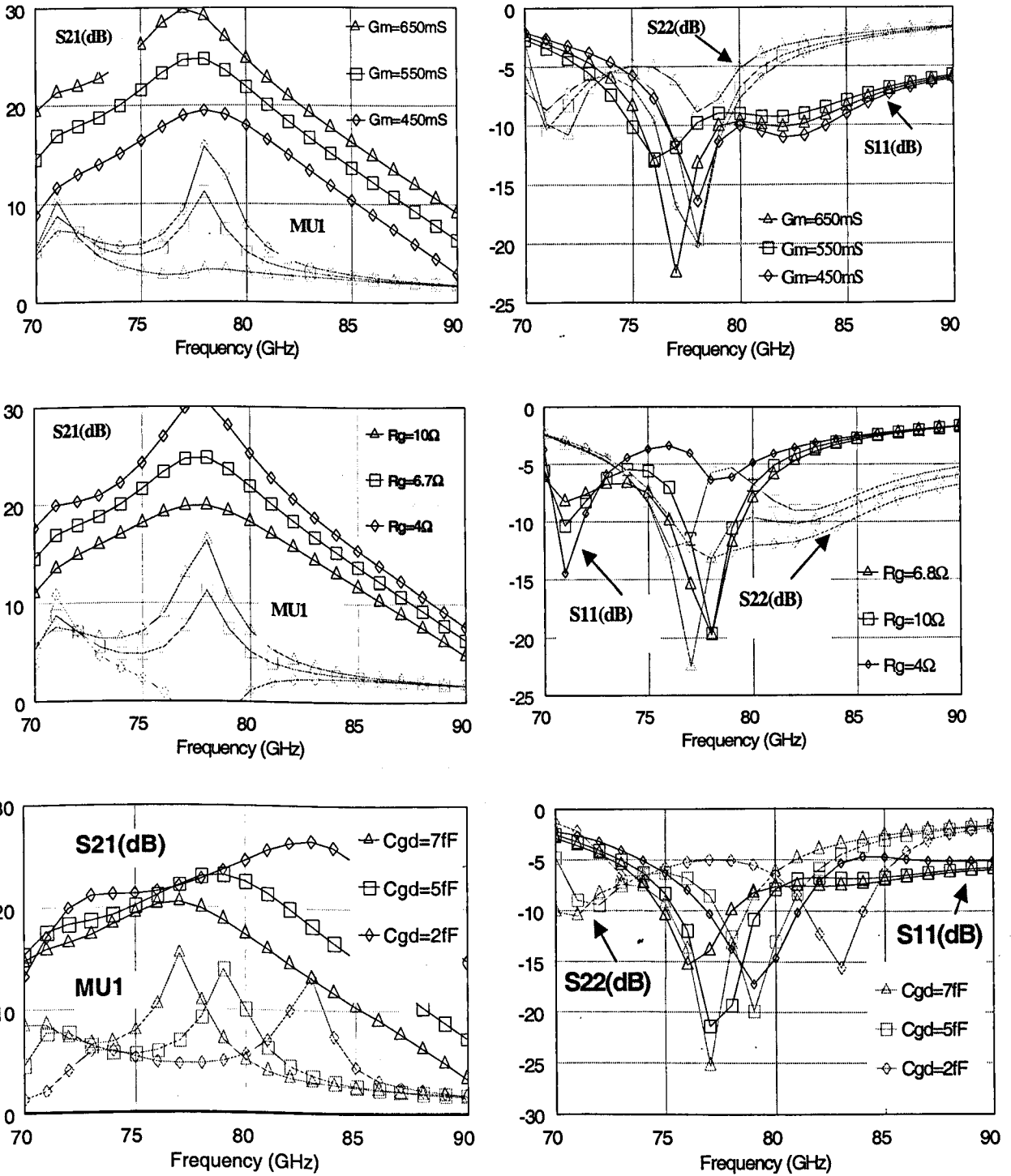
Figure 7.6: Variation in amplifier response due to changes in FET equivalent circuit parameters

7.7 Amplifier Fabrication & Measurements

The amplifier was fabricated using the standard processes shown in chapter two (see figure 7.7). The measurements of the circuit revealed that two of the HEMTs in the amplifier were non-functioning. The probable cause was short-circuiting of HEMT pads during the air-bridging process. The measurements of the circuit at zero gate and drain bias is shown in figure 7.8. The input match of the circuit is not bias dependant and falls outwith the specification of the amplifier.
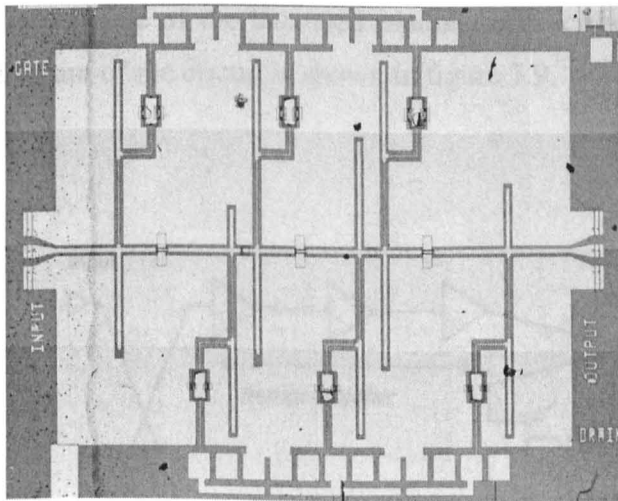

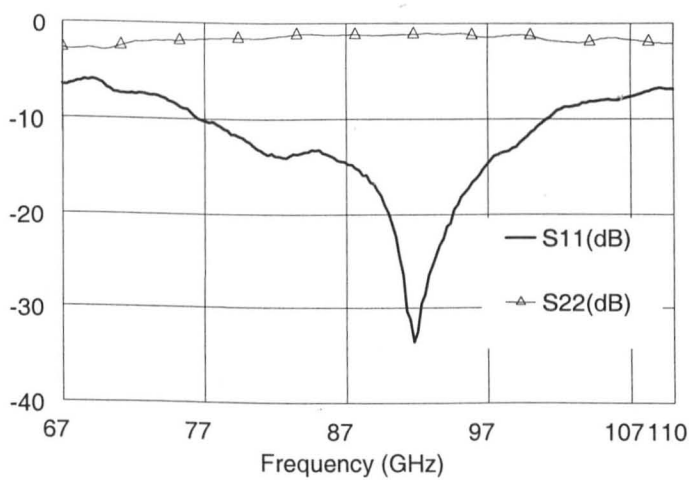*Figure7.7: A fabricated 3-stage single ended amplifier.*

Figure 7.8: Input & output match of amplifier at zero gate and drain bias

7.8 Balanced Switching amplifier

A switching amplifier consists of an amplifier integrated with a modulator. It combines the advantages of both circuits including switching, phase shifting and signal amplification. In this project a balanced switching amplifier was designed as it uses a combination of a balanced amplifier and a BPSK modulator. The advantages of this circuit include good input/output match and near ideal switching performance of the balanced modulator described in the last chapter. The block diagram of the circuit is shown in figure 7.9.
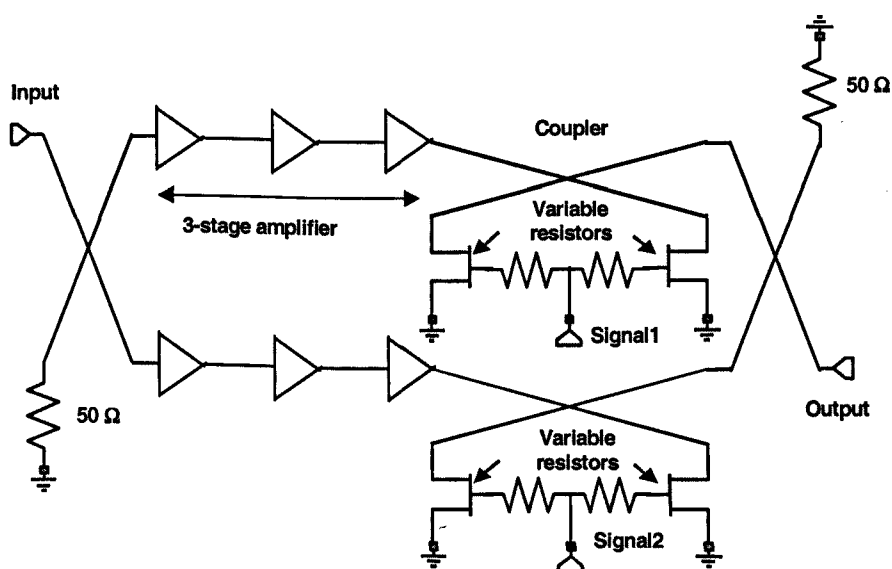

Figure 7.9: Balanced switching amplifier circuit.

This circuit was first demonstrated by TRW who used a 2-stage amplifier to achieve the desired performance at 94 GHz using GaAs technology [R7.9]. In this project a three stage balanced amplifier topology was chosen to compensate for the high insertion loss of the modulator.

Initially a balanced amplifier circuit was designed to be integrated with the modulator. This circuit was designed by re-optimizing the single ended amplifier design. The balanced topology insures good input/output match so more effort can

be put into optimizing the gain and stability. The schematic of the balanced amplifier is shown in figure 7.10.
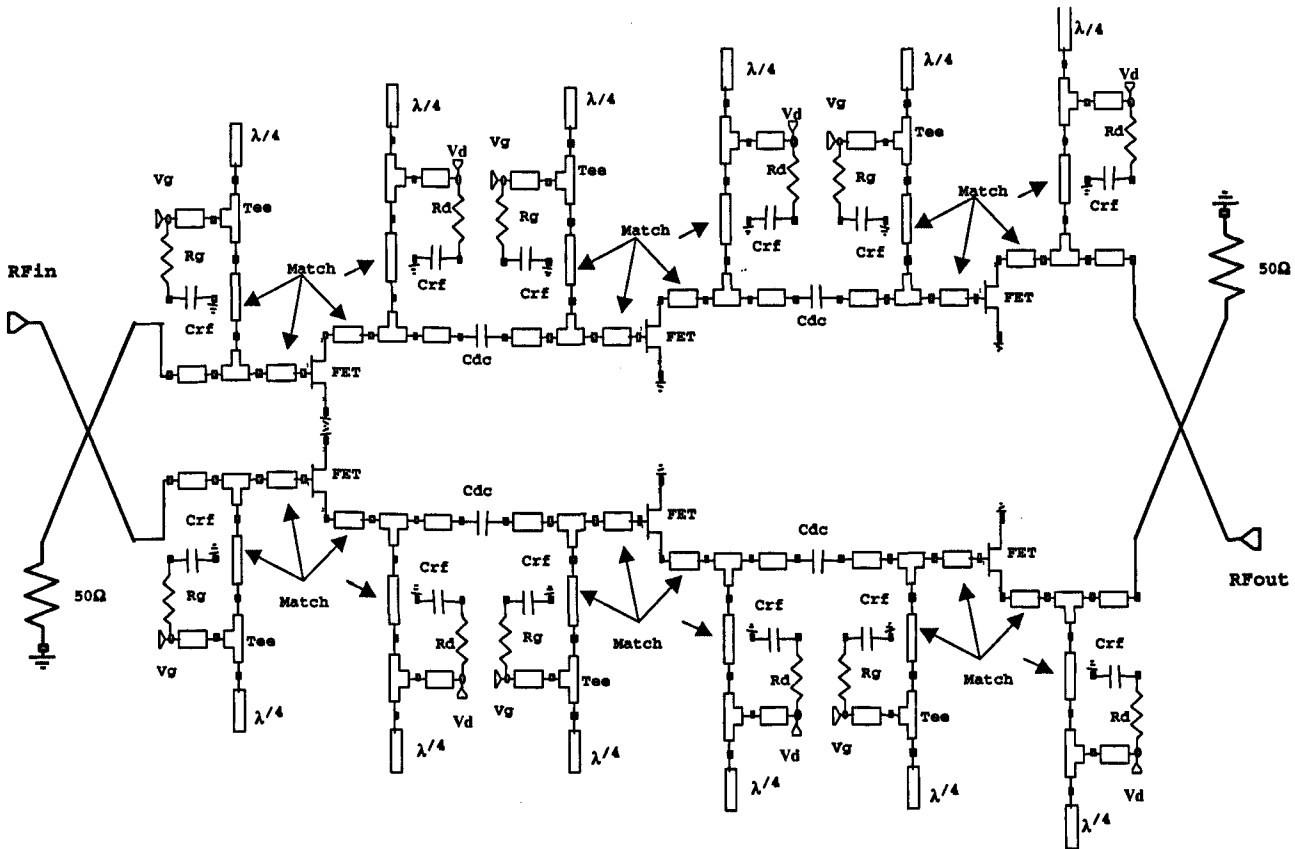

Figure 7.10: Complete balanced amplifier circuit.

The circuit consists of two identical three stage amplifiers with quadrature couplers at the input and output of the circuit. The input coupler has the same impedance at each of its output ports. The reflected signal from these output ports will add in anti-phase at the input of the coupler after passing through the coupler ensuring a very low input reflection of the whole amplifier circuit. Similar cancellation of reflection occurs at the output coupler. The matching and biasing strategy of the balanced circuit is the same as the single ended amplifier. The response of the circuit is shown in figure 7.11. The bandwidth of the input/output match is the same as bandwidth of the coupler, which in this case is a branch-line coupler. The

gain at the design frequency is 26 dB and the stability margin is also improved for this circuit compared to a single ended amplifier.
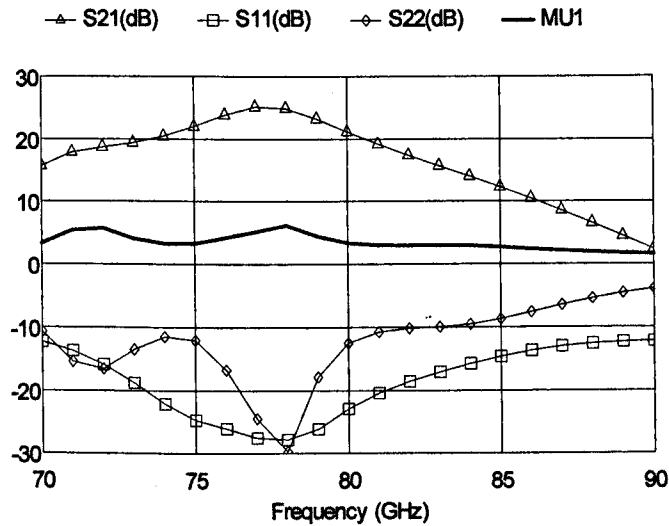

Figure 7.11: Simulated response of a balanced amplifier

This circuit was then combined with the balanced modulator and the complete schematic of this circuit is shown in figure 7.12. The modulator design shows quite lossy performance mainly due to high open channel resistance of the cold HEMT model. This results in low gain for the switching amplifier. The response of the complete switching amplifier is shown in figure 7.13. The states of the switching amplifier are shown in table 7.6.

Signal 1 (V)	Signal 2 (V)	Circuit State	Circuit Phase (°)
0	0	ON1	X
0	-2.5	OFF1	
-2.5	0	OFF2	
-2.5	-2.5	ON2	X+180

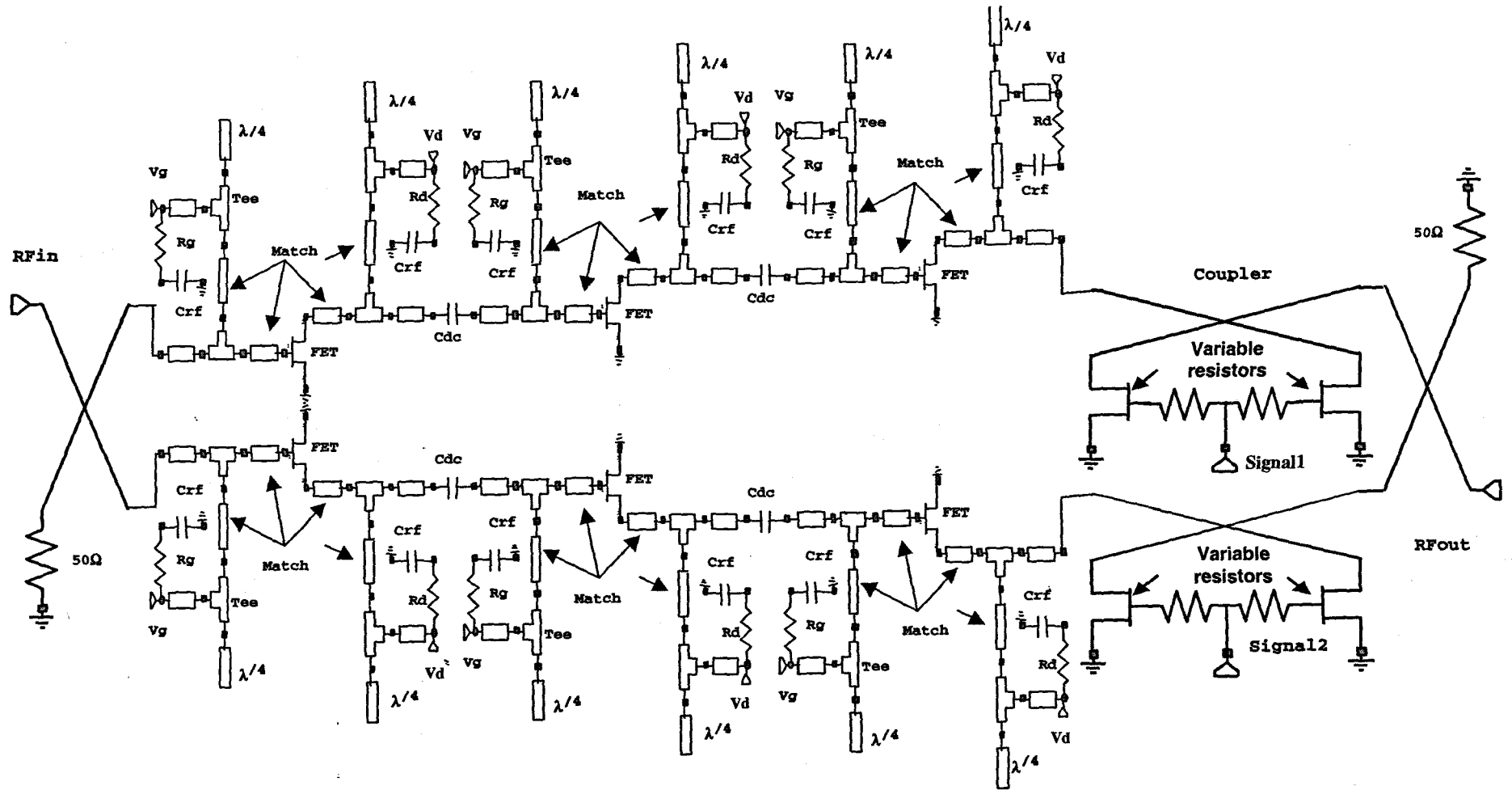*Table 7.6: Summary of switching amplifier states.*

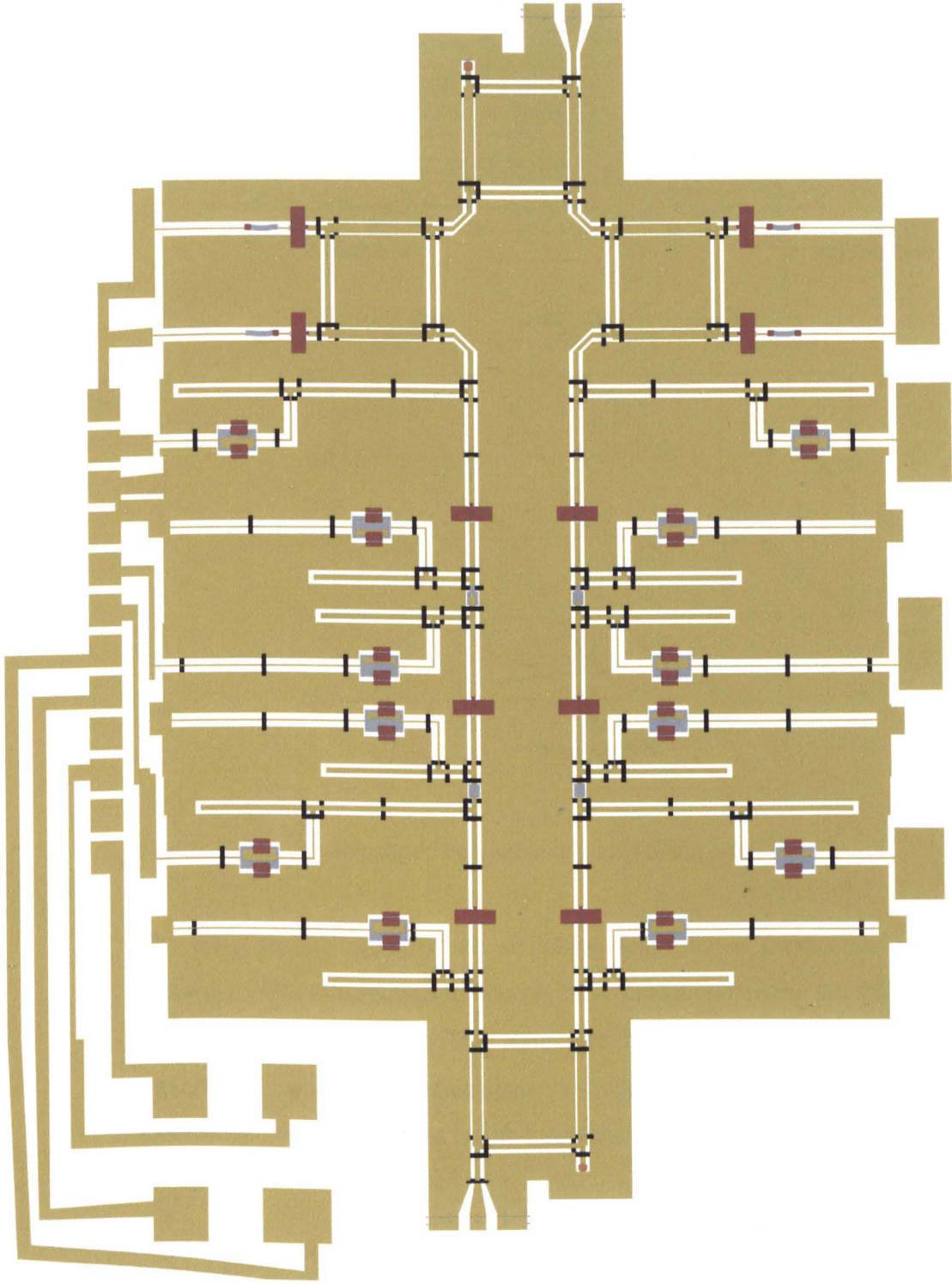*Figure 7.12: Circuit diagram of switching amplifier*

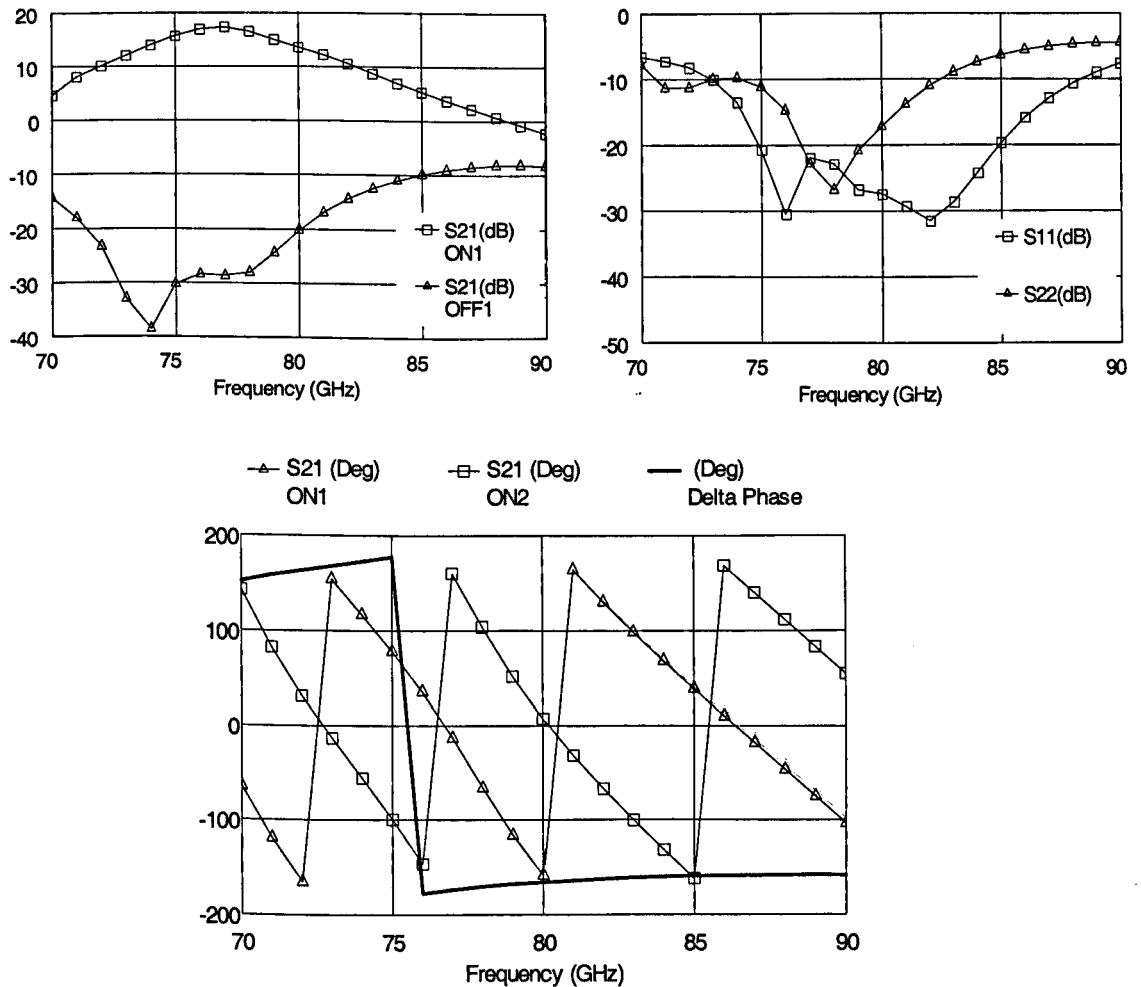Figure 7.13: layout of switching amplifier

Figure 7.14: The simulated response of a switching amplifier

The input/output match of the switching amplifier is good due to the balanced topology. The ON state of the circuit is achieved by biasing the cold HEMTs with same potential. The two ON states are 180 degree out phase because of the modulator characteristics described in chapter 6. In the OFF state, the amplifier transistors are left unbiased as the amplifier gain reduces the ON-OFF isolation of the circuit.

7.9 Summary

In this project MMIC 77 GHz single ended, balanced and switching amplifier were designed. The amplifier designed showed high gain and reasonable input/output match with good stability across all frequencies. Only single ended amplifiers were fabricated and characterized. Regrettably the fabricated amplifiers showed no gain as active devices in the amplifiers were found to be non-working.

7.10 References

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8   Conclusion & Future Work

8.1   Conclusion

The aim of this work was to design, fabricate and on-wafer test InP based MMICs operating at 77 GHz and using coplanar waveguide as a transmission line medium. To achieve this, passive and active elements were characterized in W-band (75-110 GHz) frequency range.

A range of passive elements such as CPW discontinuities, series and parallel MIM and Interdigital capacitors of different sizes and NiCr resistors were designed fabricated and measured. Equivalent circuit models of these elements were extracted which were shown to be valid to 110 GHz. Passive circuits such as branch-line coupler, rat-race coupler, Lange coupler and Wilkinson divider were successfully demonstrated at W-band frequencies. In all cases the circuits have shown insertion losses of around 1 dB and very good input and output match over large bandwidth. Equivalent circuits of these circuits were extracted and were used in design of MMICs.

Active devices were fabricated on lattice matched InAlAs/InGaAs InP HEMT. Two different 0.12 μm T-gate processes were used to make these devices with UVIII/PMMA based process giving superior high frequency performance when compared conventional Copolymer/PMMA based T-gate. The end to end gate resistance of UVIII/PMMA T-gate was comparable to the lowest 0.1 μm gate resistance ever reported. The HEMTs fabricated in this work have shown f_T as high as 193 GHz and MAG of 13 dB at 94 GHz. Equivalent circuit models of these HEMTs were extracted and were valid up to 110GHz.

These passive and active circuit models were used to design MMIC such as reactively matched single ended, balanced and balanced switching amplifiers at 77 GHz. Direct carrier modulators including BPSK, QPSK and QAM were designed, fabricated and measured at 77 GHz. The modulators have demonstrated relatively large insertion losses mainly due to poor HEMT performance in combination with thin metal used for bond-pad. The input and output match of the circuits in all cases is good over large bandwidth.

8.2 Future Work

The future work from this project spreads into two main areas.

Optimization of circuits in this work

Most MMIC results reported in this work are first pass designs and wafer runs. The modulator circuits need to be fabricated again with better ohmic contacts to see whether the insertion losses are reduced. The amplifier circuits need re-fabrication to check validity of the designs. Considerable work based on electromagnetic simulation is needed on Lange couplers to gain better understanding of the power divider structure.

Advances on this project

The UVIII/PMMA T-gate based HEMTs should give very good noise figure with reasonable material quality and Ohmic contacts. The amplifiers can be redesigned with UVIII/PMMA T-gate based HEMTs and should give a much better performance.

One of the main problems with lattice matched HEMT technology is the non-selective gate recess etch process which create significant HEMT parameter variations across the wafer. A selective gate recess etch process will make the HEMT performance more repeatable.

The vector modulators can also be redesigned with Lange couplers instead of the branch-line coupler. This should result in improved bandwidth of the circuit and will also result in shrinking the circuit size.

8.3 List of Publications From This Work

T.Lodhi, H.McLelland, S.Ferguson, K.Elgaid, D.Edgar, I.Thayne, "W-Band Coplanar Waveguide Passive Element Library", <u>IOP PREP'99</u>, January 1999, p165-168

T. Lodhi, H. McLelland, S. Ferguson, K. Elgaid, D.L. Edgar, I.G. Thayne, "InP-based W-band Coplanar Waveguide Couplers", <u>29th European Microwave Conf.</u>, Oct.1999, pp. 250-253

T. Lodhi, D.L. Edgar, H.McLelland, S.Ferguson, K.Elgaid, C.R. Stanley, I.G. Thayne, "A 77 GHz Coplanar Waveguide MMIC BPSK Vector Modulator realised using InP Technology", <u>GaAs IC Symposium</u>, Seattle WA USA, 5-8th November, 2000

Y.Chen, T.Lodhi, H.McLelland, D.L. Edgar, D.Macintyre, S.Thoms, I.G.Thayne, "First Demonstration of InAlAs/InGaAs HEMTs using T-gates Fabricated by a Bi-layer of UVIII & PMMA Resists", IEEE EDMO Symposium, Glasgow Scotland, 13-14 November, 2000.