# Germanium on Silicon Photonics

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- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
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# Abstract

Silicon photonics technologies have the potential to overcome the bandwidth limitations inherent in electrical interconnect technology. Modulation technology which is efficient both in terms of size and energy is required if silicon photonics are to replace electronics for interconnect communications. Silicon germanium technologies have the potential to not only improve the performance of current semiconductor devices but to also extend the reach of semiconductor technology into new areas such as development of a room temperature THz laser. A novel process that allows easy fabrication of Ohmic contacts to moderately doped n-type Germanium has been developed. This process has the potential to allow the realization of new devices which have been previously hampered by non-Ohmic contacts or dopant segregation problems. This work reported in this thesis also includes the design and fabrication of Ge/SiGe QCSE devices. Thin barrier QCSE designs have been put forward as a potential way to produce a more energy efficient modulator. Simulations of the devices show that a design with 16 nm Ge QWs and 8 nm SiGe barriers can provide effective modulation covering the entire optical communications C band with less than 3 V DC offset and achieve a contrast ratio across the band of over 3 dB. It was also shown that despite the thin barriers the wavefunctions remain well confined to the QWs suggesting that even thinner barriers are possible. MQW structures with thin barriers were grown and photodiodes fabricated from them. While the wafers did not have barriers as thin as designed they were thinner than devices previously demonstrated. From photocurrent measurements it was shown that these MQW structures were able to effectively modulate light near the 1550 nm wavelength with better performance than devices found in the literature.

# Publications

## Journal Papers

**D.C.S. Dumas**, K. Gallacher, S. Rhead, M. Myronov, D.R. Leadley and D.J. Paul, "Ge/SiGe Quantum Confined Stark Effect Electro-absorption Modulation with Low Voltage Swing at $\lambda$= 1550 nm." Optics Express 22.16 (2014): 19284-19292.

**D.C.S. Dumas** and K Gallacher, R Millar, I MacLaren, M. Myronov, D.R. Leadley, and D.J. Paul, "Silver Antimony Ohmic Contacts to Moderately Doped n-type Germanium". Applied Physics Letters, 104, 162101 (2014)

## Conference Papers

**D.C.S. Dumas**, K. Gallacher, S. Rhead, M. Myronov, D.R. Leadley and D.J. Paul, "Ge/SiGe Quantum Confined Stark Effect Modulators with Low Voltage Swing at $\lambda$ = 1550 nm". Group IV Photonics 2014

P. Velha, **D. Dumas**, K. Gallacher, R. Millar,M. Myronov, D. Leadley, and D.J. Paul, (2013) "Strained Germanium Nanostructures on Silicon Emitting at >2.2 $\mu$m Wavelength". 2013 IEEE 10th International Conference on Group IV Photonics (GFP), 23-30 Aug 2013, Seoul, South Korea.

P. Velha, **D. Dumas**, K. Gallacher, R. Millar, M. Myronov, D. Leadley, and D.J. Paul,"Tuning the Electroluminescence of n-Ge LEDs Using Process Induced Strain". Group IV Photonics 2012

Robert W. Kelsall, Viet Thanh Dinh, Pavlo Ivanov, Alex Valavanis, Leon J.M. Lever,

Zoran Ikonic, Philippe Velha, **Derek Dumas**, Kevin Francis Gallacher, Douglas J. Paul, John Halpin, Maksym Myronov, and David R. Leadley, (2013) "Germanium/Silicon Heterostructures for Terahertz Emission". ECS Transactions

P. Velha, K. Gallacher, **D. Dumas**, D. Paul, M. Myronov, D.R. Leadley. (2013) "Long Wavelength > 1.9 um Germanium for Optoelectronics Using Process Induced Strain". ECS Transactions.

P. Velha, K. Gallacher, **D. Dumas**, D.J. Paul, M. Myronov, D.R. Leadley. (2013) "Direct Band-gap Electroluminescence from Strained n-Ge Light Emitting Diodes". ECS Transactions.

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# Chapter 1

# Introduction

## 1.1 Introduction

Moore predicted in 1965 that the complexity of the most cost effective to manufacture integrated circuit (IC) would increase exponentially over the next 10 years [3]. This trend has continued with the number of transistors per dollar doubling approximately every two years. This trend has become known as 'Moore's Law'. The main contribution to cost reduction on a per transistor basis has been due to the reduction in the size of each transistor allowing more transistors to be fabricated on the same amount of silicon. The smaller transistors also require less power to operate and can operate at higher frequencies. The rapid increase in functionality at a given cost has been fuelled by a virtuous cycle where the increase in functionality leads to more demand which leads to more investment which leads to an increase in functionality. The increased investment is required to continue to improve the functionality because while the cost per device has decreased exponentially the cost of the lithography tools required for fabrication has increased exponentially (Fig. 1.1) [4].

## 1.2 Decreasing Size

While the power required per transistor decreases there is an increase in total power dissipation from the smaller and more abundant passive metal interconnect layers which are used for data transmission, signalling and clocking. As the clock speed is increased this leads to more heating in the IC. As the chip features are scaled down,

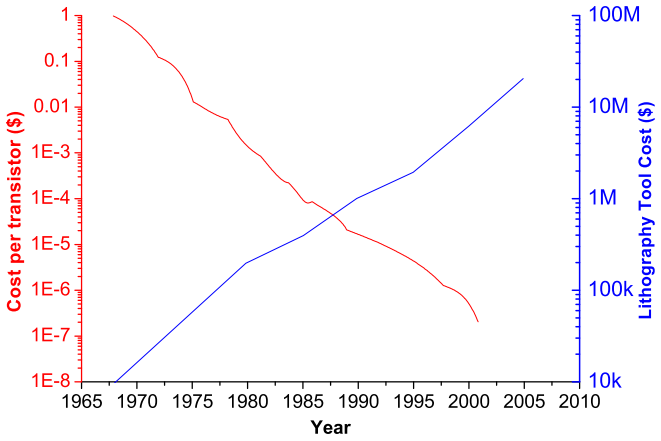


**Figure 1.1:** Decrease in cost per transistor over time and the increase in cost for associated lithography tools required for fabrication. The decrease in cost per transistor has lead to increased demand, allowing for the increased investment in more advanced production tools and research required to drive down cost per transistor.

the number of transistors is increased and the total size tends to stay constant. The propagation delay per unit length will increase as the wires get smaller in cross-section [5]. The propagation delay in a single large processor will begin to cause problems as the frequency is increased. In order to limit the impact of propagation delay processor fabrication has now shifted from a single large processor running at high clock speeds to multiple independent cores running at moderate clock speeds. Increases in performance required for continued expansion are found through the addition of more cores to a processor.

## 1.3 Multi Core

Multi core processors are computing components with two or more independent processing units within a single chip[6]. Having multiple smaller independent processors instead of one large processor lowers the maximum distance a signal needs to travel within a clock cycle reducing the length of interconnects. While the shift towards multi core processors alleviates the interconnect problems in the short term, as more and more cores are added the interconnect problem will return. The interconnect problem will shift from being between transistors within a core to being between cores and other components such as memory. A potential solution is optical chip-to-chip and intra-chip interconnects which would provide much higher data throughput while not suffering from the RC propagation delay that affects electronic interconnects.

## 1.4 Optical Communications

Optical communications is dominant in the field of long distance communications. Optical signals over optical fibres have a much lower attenuation compared to electrical signals over copper wires, as low as 0.2 dB/ km [7]. The attenuation in optical fibres is wavelength dependent. There are windows of extremely low attenuation at 1300 nm and 1550 nm. Most optical communications equipment is therefore designed to operate at or near one of these two wavelengths. Optical fibres have many advantages that allow for much higher information density than copper wires. Optical fibres are many times thinner than copper wires and do not require bulky shielding to prevent crosstalk within a bundle of fibres. In optical fibres light of different wavelengths will not interact, allowing wavelength division multiplexing where multiple wavelengths of light are used to carry independent signals through the same fibre, vastly increasing the information carrying capacity of a single optical fibre. Optical fibres currently in use can stretch for thousands of kilometres with amplification every 100 km or more and carry 100 Gbit/s per wavelength using upwards of 128 wavelengths equating to Tbit/s speeds over a single fibre. Currently the transmitters and receivers are based on III-V InP technologies and can provide 40+ wavelengths detection or transmission within a single chip [8].

## 1.5 Optical Interconnects

While long distance optical communications is a mature technology, the requirements for on chip or chip to chip communications are substantially different. The density required for chip to chip or on chip optical interconnects requires lower power dissipation, small latency, small physical size and to be integrated with Si electronics, none of which are required for or satisfied by current long distance optical communications technologies. In order to achieve optical interconnects at the chip scale, integration of all the required optical components into standard Si electronics is required. The required components are detectors, light sources, waveguides, and modulators. High quality waveguides can be fabricated from silicon on insulator (SOI) wafers using complementary metal-oxide-semiconductor (CMOS) compatible processes [9]. Compatible photodetectors can be fabricated from Ge or SiGe to operate at various wavelengths. Light sources are one of the main challenges to optical integration on Si. An electrically driven Ge laser has been demonstrated that promises to be compatible with standard CMOS processes [10]. Many different types of modulators such as the ones

demonstrated in this work have the potential to work with an optical interconnect system and will be discussed in more detail in the following chapters.

## 1.6 Integration

Integration of components refers to the fabrication of multiple devices within a single discrete package. Integration has many benefits including increased performance, smaller size, lower cost, and greater utility. Components that are monolithically integrated are made on the same substrate with common processing steps. While for hybrid integration, multiple substrates are processed separately and the components are assembled afterwards [11].

To be monolithically integrated with standard electronic processors, photonic devices must be fully compatible with CMOS. CMOS compatibility requires that devices can be fabricated in CMOS fabrication facilities [11]. This restricts the materials and processes available for use in the fabrication of CMOS compatible photonic devices. The main CMOS compatibility requirement is the use of a Si wafer as the substrate. Metals such as gold and III-V semiconductors are incompatible with CMOS fabrication.

Hybrid integration allows completely different processes and materials to be used for the fabrication of different components. At the back end of fabrication the components on the two or more separate substrates are combined using integration processes such as flip chip bonding [12]. This allows greater flexibility in the processes available for different components. With hybrid integration III-V materials could be used with Si photonics, but would not benefit from the high volume fabrication processes developed for CMOS production.

## 1.7 Silicon Photonics

Guided wave components on Si were first investigated by Soref and colleagues [13, 14]. Both passive and active components such as waveguides and modulators were investigated. Si photonics has since become a promising potential solution to the problem facing electrical interconnects as device sizes shrink. Integration of Si photonics components with electrical CMOS components has been actively pursued by a number of companies. Optical data transceivers with data rates of 100 Gbit/s using silicon pho-

tonic devices are readily available and are in use for short range communications such as with server clusters and data centres. Generally these photonic integrated circuits make use of monolithically integrated Si modulators and Ge photodetectors and III-V lasers integrated via hybrid integration. One of the key components preventing full monolithic integration is a compatible Si based light source

### 1.7.1 Silicon Waveguides

Optical waveguides can be readily fabricated from SOI wafers. An SOI wafer contains an insulating layer sandwiched between two Si layers. Any thickness for the layers can be chosen. A standard material for the insulating layer is $SiO_2$ which has a refractive index of 1.47 for 1550 nm light (much lower than Si which is 3.48 at 1550 nm). A simple mesa structure of the correct dimensions on the surface will create a high index core which will guide light. The high index contrast allows the fabrication of small waveguideing structures. The small waveguides allow high density photonic circuits to be produced improving the economics of integration with CMOS electronics.

### 1.7.2 Silicon Detectors

While pure silicon photodetectors can be fabricated from a simple pin structure, due to the large bandgap Si is transparent to wavelengths greater than 1100 nm [15]. The Si pin detectors are therefore not compatible with the communications wavelength bands at 1300 nm and 1550 nm. Si Schottky-barrier photodetectors are based on the absorption of light in a silicide region generating carriers which are excited across the interface into the semiconductor. With the use of a CMOS compatible metal such as Ni, devices have been fabricated which demonstrate detection across the entire communications band of wavelengths [16]. These devices show good potential for integrated detectors at 1550 nm for silicon photonics.

### 1.7.3 Silicon Based Lasers

Several techniques for lasing on Si have been demonstrated but they are not compatible with monolithic integration. Optical pumping of a Si waveguide can produce lasing through stimulated Raman scattering processes. A pin structure is required to sweep out carriers from the waveguide to lower the free carrier absorption to allow gain [17].

The requirement for optical pumping is not compatible with large scale integration into Si CMOS. Light amplification in Er doped silicon fibres is widely used for optical communications and has been investigated for use to achieve lasing in Si. Er doped Si is highly inefficient due to strong Er carrier interaction. Er doped Si nanocrystals within $SiO_2$ matrix prevent the Er carrier interaction and allow optical gain near 1550 nm [18]. While devices of this type have demonstrated both photoluminescence and electricaluminescence, the optical gain is limited by the low solubility of Er. Injection of carriers into the Er doped Si nanocrystals requires very high electric fields which are not suitable for an efficient electrically pumped laser integrated with Si electronics.

### 1.7.4 III-V Lasers on Si

Direct gap semiconductors have demonstrated that they can be used to produce efficient electrically pumped lasers. The vast majority of semiconductor lasers are of this type. Direct gap III-V materials can be directly grown on Si but the large lattice mismatch results in misfits and dislocations which increase optical loss. An alternative is to grow the III-V materials on a lattice matched SiGe alloy buffer grown on Si [19]. The most advanced III-V lasers make use of hybrid integration techniques. This allows the III-V lasers to be grown on an SOI wafer separately from the rest of the components then bonded together at the back end of the fabrication process. The disadvantage of these methods which make use of III-V semiconductors is that the processes are incompatible with CMOS fabrication.

## 1.8 Germanium on Silicon

The possible design parameters for a wafer are greatly expanded by introducing Ge while still maintaining CMOS compatibility. Unlike other group IV elements the miscibility of Ge with Si is complete, allowing stable SiGe alloys with any ratio of Si to Ge. While Ge is still an indirect bandgap material the difference between the lowest indirect (0.66 eV) and the direct band gap (0.8 eV) is quite small. An energy of 0.8 eV corresponds to a wavelength of 1550 nm which allows the creation of optical devices which can use the communications wavelength. SiGe heterostructures can be engineered by changing the elemental ratios which can affect the electrical and optical properties of the material. Another dimension added to the design toolbox is the ability to control the strain by using different Ge fractions. Ge has already been incorporated into Si electronic CMOS processes; source and drain regions of p-MOSFETs use SiGe

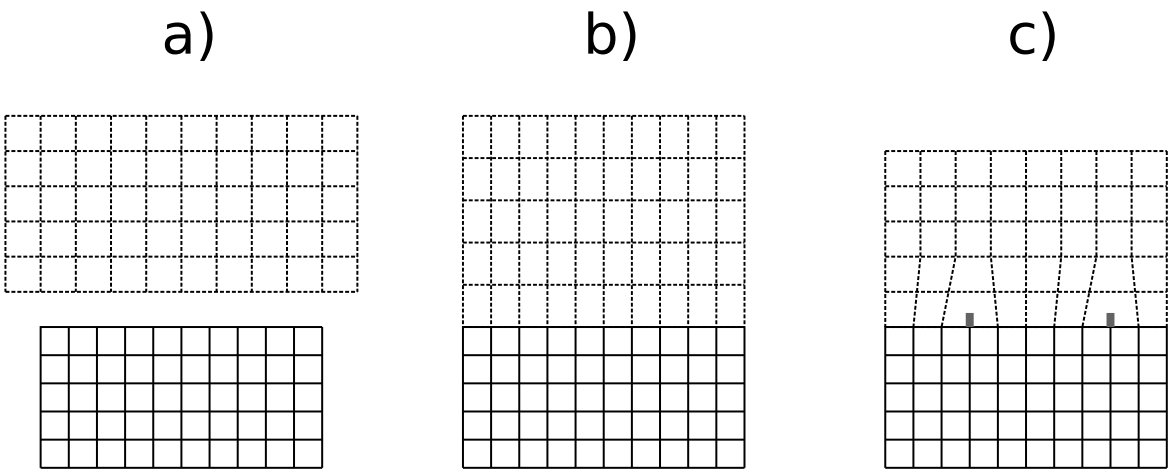


**Figure 1.2:** Diagram of accommodation of lattice mismatch for a film with higher lattice constant then the substrate. a) Lattice constant for each material in bulk, b) film accommodating lattice mismatch by strain; compression parallel to surface leads to expansion orthogonal to surface, and c) film accommodating lattice mismatch by misfit dislocation; missing columns allows film to relax towards bulk lattice.

alloys to improve the mobilities in Si transistors by the addition of strain [20].

Despite the issued associated with the lattice mismatch, using Si wafers as a base for Ge technology has many benefits even for high Ge content heterostructures. Si wafers are less expensive, more durable, and of a higher purity than Ge wafers [21], and using Si wafers allows one to take advantage of some of the mature CMOS foundry technology which has been developed for Si electronics. Currently SiGe wafers cannot easily be created with any Ge concentration directly from a melt due to the differences in Si and Ge solidus liquidus curves. Some small scale experiments have shown a possibility for directly growth but only for crystals of 2 mm diameter and a ratio of 1:1 [22].

### 1.8.1 Lattice Mismatch

In general there will be a lattice mismatch between two different materials such as Si and Ge or SiGe alloys of different Ge concentrations (Fig. 1.2). For the growth of a single crystal film on a substrate the mismatched lattice constant will be dealt with in one of several ways depending on what is more energetically favourable. For growth of Ge on top of Si the underlying substrate is assumed to be much thicker than the film and retain its bulk properties. Since Ge has a larger lattice constant than Si, the Ge film will be deformed in one of the following ways to accommodate the lattice difference [23]:

- Film accommodation by strain. The film grows pseudomorphically, matching the in-plane lattice constant but with an increased lattice constant normal to the surface. The strain will break the symmetry of the normal crystal structure of the film resulting in the splitting of normally degenerate energy bands.
- Film accommodation by misfit dislocations at the interface. Some atomic planes in the substrate do not have matching planes in the film. This allows the film to relax towards its bulk lattice constant. A film can be partially relaxed by misfit dislocations and be partially strained. A higher density of misfit locations will increase the relaxation of the film.
- Morphological relaxation. Surface undulations create an uneven surface and non-uniform crystal orientation.
- Cracks. Large breaks in the material can form, rendering the material unsuitable for device fabrication.

Any thin film with a higher lattice constant than the substrate will accommodate the mismatch in one or more of these ways. If the lattice constant of the film is less than that of the substrate accommodation by strain will result in a decrease in the lattice constant normal to the surface, and accommodation by misfit dislocations will result in some atomic planes in the film not having matching planes in the substrate. Morphological relaxation and cracking will still be possible forms of mismatch accommodation.

The form that the accommodation takes depends on the thickness of the film, the lattice mismatch between the film and the substrate, and the temperature at which the film is grown. For a given set of substrate and film materials there will be a critical thickness below which the material will be fully strained and above which relaxation can occur. A meta-stable region of lattice mismatch and thicknesses exists in which unrelaxed layers beyond the critical thickness can be grown at low temperatures. An unrelaxed layer grown in the meta-stable region can relax if the temperature is increased sufficiently. For $Si_{(1-x)}Ge_x$ alloys grown on a Si (001) substrate the critical thickness is ∼600 nm for $x = 0.10$, ∼300 nm for $x = 0.20$, ∼150 nm for $x = 0.32$, ∼50 nm for $x = 0.40$ and ∼20 nm for $x = 0.52$ [24]. The exponential decrease in critical thickness as a function of Ge content means that higher Ge content heterostructures will have significant dislocation densities for even extremely thin layers if grown directly on Si substrates.

When a series of thin layers of different lattice constants are grown on a thick substrate there is another critical thickness which is the critical thickness of the heterostructure

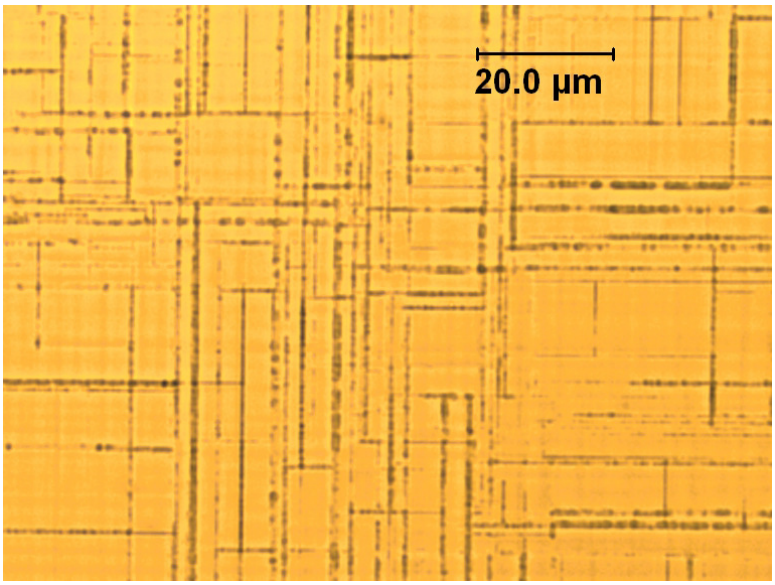


**Figure 1.3:** Example of crosshatching from Ge on Si wafers. Optical microscope image of surface of wafer. The lines of the crosshatching that are visible are depressions that are the result of misfit dislocations.

as a whole [25]. The critical thickness of the entire heterostructure is roughly equal to the critical thickness of a layer with a Ge content equal to the average Ge content of the heterostructure. Therefore, if the average Ge content of the entire heterostructure is equal to the Ge content of the fully relaxed substrate or virtual substrate, then as long as each individual layer is less than its own critical thickness, the entire structure will not relax. Designing a structure in this way is known as strain symmetrization or strain balancing.

A misfit dislocation is not a single missing atom but a line segment of missing atoms across the surface of the interface. If the line does not reach the edge of the wafer it will at some point create threading dislocations which thread upwards towards the surface at 60° angles on the (111) plane. The misfit dislocations due to strain relaxation form lines of misfits along the two <110> directions. This leads to a cross hatch pattern on the surface of the wafer [26] (Fig. 1.3). The roughness due to the crosshatching can be detrimental to devices and device fabrication [27]. Crosshatching can be suppressed by growth techniques that confine dislocations to buffer layers [28]. A high density of threading dislocations is detrimental to electronic and optoelectronic devices since they leave dangling bonds which alter the electrical properties of the material, leading to, for example, higher dark currents in photodiodes.

## 1.9 Germanium Epitaxy on Silicon

In order to produce Ge on Si wafers the Ge is epitaxially grown on to a Si wafer. While the Si wafer is sliced from a cylinder formed from molten Si in a standard and inexpensive process, the Ge and SiGe layers must be grown layer by layer in a precisely controlled chamber. Two major techniques are available for growth of Ge on Si wafers.

### 1.9.1 Molecular Beam Epitaxy

In molecular beam epitaxy (MBE) the layers are grown by producing a beam of molecules which impinges and sticks to the surface of the wafer [29]. MBE is performed in an ultra clean chamber at an ultra high vacuum. Temperature controlled effusion cells are used to create uniform beams of the desired material. Shutters are used to start and stop the beam without changing the temperature to allow precise control over deposition thicknesses. Independent molecular beams for Si, Ge, and dopants allow the growth of doped and intrinsic SiGe of any composition. Deposition rates for MBE can be varied arbitrarily depending on the maximum flux of material from the sources and layers as thin as two atomic monolayers can be grown. A major disadvantage of MBE is the build up of wall deposits which can peel off as fine particles which would be detrimental to high precision growth [30].

### 1.9.2 Chemical Vapour Deposition

Chemical vapour deposition (CVD) uses gaseous compounds as the source of the material for growth. As the gases are released into a chamber containing the wafer they adsorb onto the surface. The molecules react with the surface, building up the layers and releasing volatile molecules which desorb from the surface [31]. Gases used include $SiH_4$, $GeH_4$ for Si and Ge respectively and $PH_3$ and $B_2H_6$ for n-type and p-type dopants. Different pressures and temperatures can be used which effect the quality of the structures grown. The growth rate and elemental ratio of the layers are dependent on the pressure, gas ratios, and temperature during growth and cannot be independently varied.

Reduced pressure CVD (RPCVD) ($\approx$ 20 mTorr) was the method used for the growth of the wafers used in this work. In the RPCVD method the chamber pressure is reduced allowing lower temperature growth while maintaining an oxygen free surface to allow

high quality growth. The wafers used in this work were grown using an Epsilon 2000E commercial CVD tool operated by collaborators at Warwick University. Using a two temperature growth method thick layers of pure Ge are grown directly on top of a Si wafer. This is followed by a reverse graded layer down to the virtual substrate alloy concentration. Since the thick layers of Ge and the virtual substrate ($> 1\mu$m) are well beyond the critical thickness of Ge on Si, the layers fully relax during the growth process [32]. The process produces a fully relaxed virtual substrate of the chosen alloy concentration. The alloy concentration of the virtual substrate is chosen to minimize the strain in the active layers above to allow fully strained growth of thick structures.

### 1.9.3 Reduction of Threading Dislocations

Ge layers well beyond the critical thickness for Ge growth on Si will be fully relaxed due to misfit formation. Each threading dislocation that reaches the surface will cause a defect in the surface. Therefore, reducing the number of threading dislocations that reach the surface will produce a higher quality surface on which to grow the active layers. Threading dislocation densities for thick Ge grown directly on Si can be as high as $10^8$ to $10^9$ per cm. Threading dislocations can be prevented from reaching the surface if they reach the edge of the wafer or they can be annihilated through interaction with another thread. Annealing of a wafer at high temperature and increasing the thickness can reduce the density of dislocations reaching the surface [21]. Using selective growth techniques can decrease the dislocation density by decreasing the lateral distance a thread can travel before reaching an edge. Two temperature growth processes have been developed which improve the surface quality of a wafer. A thin layer grown slowly at a low temperature is followed by a thicker and faster high temperature growth. This process has been shown to produce a low threading dislocation density ($3 \times 10^6$ per cm) [33].

## 1.10 Thermal Mismatch Between Ge and Si

Ge epitaxial growth on a Si substrate occurs at high temperature ($> 500$ °C). A Ge layer that is fully relaxed on Si at 500 °C will have tensile strain at room temperature. As the wafer is cooled from growth temperature to room temperature the number of misfit dislocations will not change but the natural lattice constant of both the Si and the Ge will change due to thermal expansion. The thermal expansion coefficients of Si and Ge are not equal and the Ge lattice will shrink by a higher percentage than

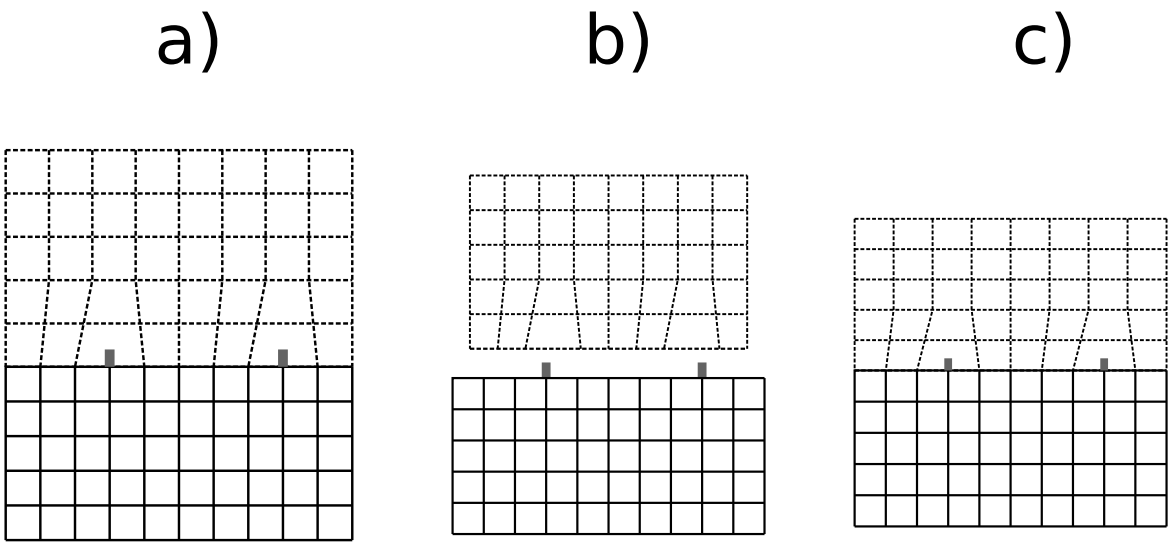


**Figure 1.4:** Diagram of accommodation of lattice mismatch for a film with higher lattice constant then the substrate. a) Ge film accommodating lattice mismatch by misfit dislocation is fully relaxed at growth temperature, b) Shrinkage of lattice constants due to thermal expansion when reducing temperature from growth to room temperature, Si substrate shrinks less than Ge film, c) Ge layer on Si at room temperature is tensile strained due to different thermal expansion coefficient between Si substrate and Ge film.

the Si lattice constant. The effect of thermal mismatch on a virtual substrate is that the parallel lattice constant will be larger than expected if a fully relaxed layer was assumed. This extra tensile strain should be taken into account when designing devices since, for example, in a Ge/SiGe QCSE device the extra tensile strain will shift the absorption peak to higher wavelengths.

A simple example of a thick Ge layer grown on Si at 800 K is used to explain the effect. The Ge will be fully relaxed at 800 K and its lattice constant will be 5.67684 Å the lattice constant of the Si substrate will be 5.44096 Å [34]. This difference will be compensated for by a number of misfit dislocations. As the sample is cooled to 300 K (room temperature), the lattice constant of the Si substrate will shrink to 5.43109 Å a decrease of 0.18 %, while the Ge lattice constant will want to shrink to 5.65795 Å a decrease of 0.34 %. This difference will be accommodated by the Ge film becoming tensile strained (Fig. 1.4).

## 1.11 Ge/SiGe Devices

Many different high performance devices can benefit from incorporating Ge or SiGe alloys into the design. One of the first major applications for SiGe heterostructures was the heterostructure bipolar transistor. SiGe alloys have a lower bandgap than Si

does; therefore, replacing the base of a Si bipolar transistor with SiGe allows one to control the relative barrier for holes and electrons. The first patent on this technology was issued in 1977 and the first device fabricated in 1987 [23].

Si transistors can take advantage of the increase in carrier mobilities when the Si layer is epitaxially grown on relaxed a SiGe layer. Due to the lattice mismatch the Si layer will experience biaxial tensile strain which will reduce carrier scattering which increases the mobility [35]. Investigations revealed that uniaxial process induced strain provide better performance than the biaxial strain from the relaxed SiGe layer. Compressive uniaxial strain which is utilized in modern n-channel transistors can be created by using SiGe embedded into the source and drain of the transistor. p-channel transistors require tensile strain which is induced by a capping layer [36].

While resonant tunneling diodes have demonstrated improvement in logic and memory operations when integrated with transistors compared to CMOS technology, most of the demonstrations have been with III-V technology which is incompatible with Si CMOS. Recently, resonant tunneling diodes fabricated from Si and SiGe have been shown to operate as random access memory. Operation was shown at a temperature of 77 K since these device were unable to operate at room temperature. With improvements to the passivation and etching processes to allow room temperature operation they have the potential for improved performance over current memory technology due to low power operation [37].

## 1.12 Ge on Si Photonics

Ge on Si photonics is an active field of research and many devices have been demonstrated. Ge detectors have been created using a p-type region - intrinsic region - n-type region (pin) structure that operate well between 650 nm and 1300 nm with decreasing efficiency above 1500 nm. Ge on Si photodetectors have high response times due to the high carrier drift time in Ge. Ge on Si avalanche photodetectors (APD) have also been demonstrated and provide improved sensitivity compared to pin structures. APD devices combine the excellent optical absorption properties of Ge in the telecommunications wavelengths (1300 nm, 1550 nm) with the carrier multiplication ability of Si. In the high electric field gain region of the Si the carriers photogenerated in the Ge undergo a series of impact ionizations which multiply the current generated from each photon. The benefits of using a Ge on Si structure is that a pure Ge single photon avalanche diode would suffer from much higher dark current in the high field carrier

multiplication region due to the smaller bandgap relative to Si, but without the Ge absorber region 1550 nm light would not be absorbed. Ge on Si avalanche diode detectors capable of detecting single photons at the communications wavelength of 1550 nm have been demonstrated. The structure consists of a three layer pin structure in Si with an intrinsic Ge layer capped with a p-type Ge layer [38]. The device is operated at reverse bias with an extremely high electric field across the Si region and a lower electric field across the Ge region.

Due to the absorption depth of 1550 nm light in Ge, surface normal devices require a thick absorption region in order to increase the total absorption of a device. A thicker absorption region increases the distance between anode and cathode which decreases the electric field for a given bias. The lower electric field lowers the carrier drift velocity, decreasing the maximum operating frequency. Fortunately, these devices can be incorporated into a waveguide structure where the absorption can be increased by increasing the length without increasing the thickness. The detectors can be incorporated into a waveguide either by being butt coupled to the end of the waveguide or directly alongside the waveguide. In a butt coupled configuration the light directly enters into the detector. If the detector is directly alongside the waveguide the evanescent tail of the light couples into the detector.

Photonic integrated circuits currently utilize III-V lasers integrated on to Si. Recent progress has been made in the fabrication of Ge on Si lasers. In 2010 Liu *et al.* [39] reported on the first demonstration of a laser from the direct gap of Ge on Si. Tensile straining and n-type doping of the Ge allowed laser operation through optical pumping. The tensile strain lowers the difference between the direct ($\Gamma$) and indirect (L) conduction valleys while the high n-type doping increases the electron population in the $\Gamma$ valley, enhancing direct gap light emission. Electrically pumped lasers have additional sources of loss making their realization more difficult. Camacho-Aguilera *et al.* demonstated in 2012 [10] an electrically pumped Ge on Si laser was possible by increasing the dopant concentration. This design is not suitable as an on-chip source due to the very large threshold current.

Integration of optical modulators onto integrated circuits is another area currently being researched. Many different technologies are being investigated including Ge/SiGe MQWs as investigated in this work. As QCSE modulators are the main focus of this work, the various modulator technologies will be discussed in more detail in the following chapter.

## 1.13 Aims of this Thesis

One of the goals of this thesis is the development of an Ohmic contact process for moderately doped n-type Ge. Previous processes demonstrated for Ohmic contacts to n-type Ge rely on either high *in-situ* doping, ion implantation of dopants, or ultra thin insulator layers between the Ge and metal layers. For potential technologies based on Ge which rely on intrinsic active layers between n-type contact layers (nin), the high *in-situ* doping or ion implantation methods are detrimental to the performance of the device and the quality of ultra thin insulator method is highly dependent on layer thickness. The process developed will allow Ge nin devices to be fabricated with Ohmic contacts without the issues associated with other Ohmic n-type Ge contact methods.

The main focus of this thesis is the development of improved QCSE modulator technology. Integrated Si photonics has the potential to revolutionize processor interconnect technology by removing the current roadblock faced with electrical interconnects. While integrated Si light sources still require development, improvements to the efficiency of integrated modulators are an important area of research heading towards large scale integration of Si photonics. The absorption characteristics of low voltage QCSE designs are simulated and devices based on the designs are fabricated. This work has shown the potential for low voltage QCSE modulation based on thin barrier MQW designs.

The following is a brief outline of the remaining chapters of this thesis.

**Chapter 2: Modulation Technologies**

This chapter consists of a discussion of modulation technologies. These include the two main modulation types, electro-optic refractive and electro-optic absorptive, as well as a variety of other types of modulation. This chapter provides necessary background information required to understand and evaluate the potential of modulation technologies such as the QCSE designs investigated in this thesis.

**Chapter 3: Fabrication**

This chapter details the techniques and tools required for the fabrication of the devices and structures. It includes an overview of the different processes used during fabrication followed by detailed descriptions of some of the more complex fabrication processes and tools. The structures and devices discussed in the following chapters required precision processing.

**Chapter 4: Silver Antimony Ohmic Contacts to n-type Ge**

This chapter describes the development and analysis of Ohmic contact to moderately doped n-type Ge. The reason behind the difficulty encountered when producing Ohmic contacts to n-type Ge is discussed, current methods are compared, and the need for an alternate method is explained. The development of the AgSb Ohmic contact process is detailed and the quality of the contacts are analysed. The use of these contacts has the potential to allow the fabrication of novel devices which require low doped n-type Ge bottom contact layers.

**Chapter 5: Simulation of Low Voltage QCSE Designs**

This chapter details the work on simulating low voltage MQW QCSE designs in order to calculate the effect of the QCSE on the absorption. It includes discussion of the physics required for understanding the quantum confined stark effect as well as demonstrations and analysis of the results from simulations of SiGe/Ge MQW structure designs. The simulation results show the potential for low voltage QCSE devices which can operate as modulators near 1550 nm.

**Chapter 6: Fabricated Low Voltage QCSE Devices**

This chapter details the fabrication and testing of the low voltage QCSE devices. First, the wafer structure is described, followed by a detailed description of the fabrication process. Next, the measurement techniques are discussed and the measured results analysed. The results of the measurements of these devices show that thin barriers can provide sufficient confinement for the QCSE, allowing more energy efficient QCSE designs to be realized.

**Chapter 7: Conclusions**

The conclusions about the results achieved from this work are presented and future work which could follow from this research is discussed.

# Chapter 2

# Modulation Technologies

A optical modulator is a device that allows a control signal to impart information on to a light wave by temporarily varying one of its properties. A number of different technologies exist which allow one to modulate an optical signal. Two main categories of electrically controlled modulation exist: electro-optic refractive which, works by directly changing the phase; and electro-optic absorptive, which directly changes the amplitude of the light at the output of the component. Other technologies include all-optical techniques, in which an optical signal is used to control the transmission, grating technologies, which use refraction to control the angle of the output light, thermo-optical refractive index changed by heating, and acoustic modulation, which uses vibrations to modulate the signal. The main focus in this chapter will be on electro-optic absorption technologies including the QCSE modulator technology used in this work.

## 2.1 Direct Laser Modulation

Conceptually the simplest method to modulate a light beam is direct laser modulation. In this method the laser is directly modulated such that a signal controls the frequency or amplitude of the laser output. Amplitude modulation of the laser is performed by having a current equal to the threshold current of the laser and imposing the control signal on top. The small change in current due to the control signal switches the laser from slightly above to slightly below the threshold for lasing. The frequency of the laser can be modulated by changing the optical size of the cavity in which the laser is operating. A change in the refractive index of the gain medium will change the optical

distance between the two ends of the laser cavity, changing the optical modes of the cavity and resulting in a different frequency of light from the laser.

## 2.2 Modulation Technologies

A major disadvantage of using direct modulation of the laser is that it will introduce chirp to the signal. Chirp is the effect in which the frequency of the light changes as the laser is turned on and off. As the modulation frequency increases the distortion due to the chirp becomes increasingly destructive. Chirp in the signal can be avoided through the use of an external modulator. The two main forms of external modulation used to modulate optical signals are electro-optic refractive, and electro-optic absorptive techniques. There are other methods that have been shown to be able to modulate a light. A sampling of them is discussed here.

### 2.2.1 Bragg Gratings

A Bragg grating is a surface or volume with a periodic variation in optical path length. With a Bragg grating if light is incident on the grating at the Bragg angle $\theta_B$ the angle of maximum reflection or refraction is equal to $2\theta_B$. The angle $\theta_B$ depends on the spacing and phase difference between the two parts of the grating.

#### Acoustic Bragg Grating

An acoustic Bragg grating uses an acoustic wave to setup a periodic strain in the semiconductor material. Since the index of refraction in the material will vary with the strain in the material, the acoustic wave will create a periodic index of refraction. The acoustic wave can be modulated to modulate the Bragg angle of the grating or to turn the grating on and off. A thick grating with a period of $\Lambda$ (thickness $\gg \frac{\lambda^2}{\Lambda}$ where $\lambda$ is the wavelength of light) is modulated by turning on and off an acoustic wave. Light incident on the grating at an angle $\theta_B = \frac{\lambda}{2\Lambda}$ will be refracted by an angle of $2\theta_B$ when the grating is active (Fig. 2.1). When the grating is removed by stoping the acoustic wave the light will not be Bragg refracted and will exit at the same angle it entered.

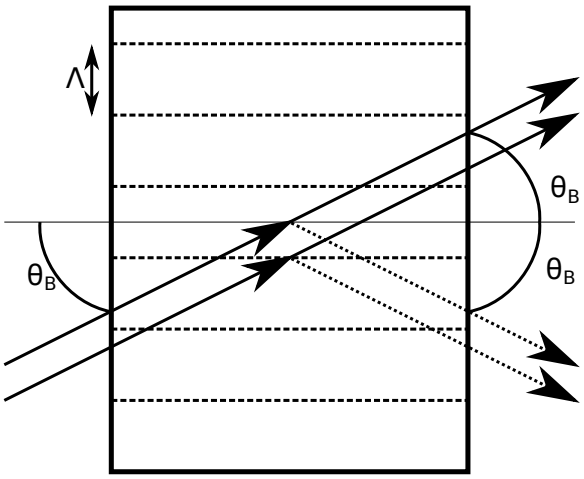


**Figure 2.1:** Diagram of an acoustic Bragg grating modulator where the Bragg grating is turned on and off by turning on and off an acoustic wave. When Bragg grating is off the incident light is not refracted (solid arrows). When the Bragg grating is on with a period of $\Lambda$ the light is refracted by an angle of $2\theta_B$.

### Electro-optic Bragg Grating

Interdigitated contacts can be used to periodically modify the index of refraction of the semiconductor underneath the contacts. Changing the voltage difference between the two contacts will change the refractive index in the semiconductor. In this technique the period of the Bragg grating is fixed during fabrication by the periodicity of the contacts and the relative phase shift will be determined by the magnitude of the refractive index difference.

### Micro-mechanical Bragg Grating

A Bragg grating can also be modulated using micro-mechanical techniques. An array of grating lines are fabricated that can be moved perpendicular to the surface as a function of applied voltage using electrostatic actuators [40]. As they are moved the phase difference between light reflected off the grating and the surface between the gratings is modified, changing $\theta_B$. Modulation of over 100 kHz was demonstrated using electrostaticly actuated gratings.

### 2.2.2 Thermo-optical

A variation of the refractive index of a material with temperature is known as the thermo-optical effect. A thermo-optical modulator has been demonstrated using a Si Fabry-Perot etalon with resistive heaters to control the refractive index in the etalon and therefore the transmission. Due to the inherently slow process of heating and cooling a device, this method would only be useful for applications where a high modulation speed is not required [41].

### 2.2.3 All Optical Modulation

A variety of different all optical methods have been developed. These techniques allow the modulation of a light beam to be controlled by a second light beam. The ability to modulate a light power using a second light source opens up the possibility of all optical information processing.

### 2.2.4 Organics

Non-linear processes in organic photonic crystals change the bandgap of the material, resulting in large changes in transmission of light near the bandgap energy. Modulation of a light at a wavelength of 1620 nm using a 532 nm laser as the control was demonstrated using dye-doping of a liquid crystal [42]. The dye is highly absorbent at 532 nm allowing the control laser to be used to heat the liquid crystal. The absorption spectrum of the liquid crystal is temperature dependent with an absorption edge near 1620 nm. When heated by the pulse the absorption edge of the liquid crystal shifts to higher wavelengths allowing the 1620 nm light to be transmitted.

A second method which utilizes organics is gain switching. A polymer laser operating at 650 nm has been modulated using pulses of 1300 nm light. The laser operates normally before a pulse arrives and on arrival of a pulse the polymer is excited into higher energy states. The excited polymer is absorptive at the operating wavelength which quenches the gain, effectively turning the laser off. After the pulse the polymer laser returns to its normal operating state [43].

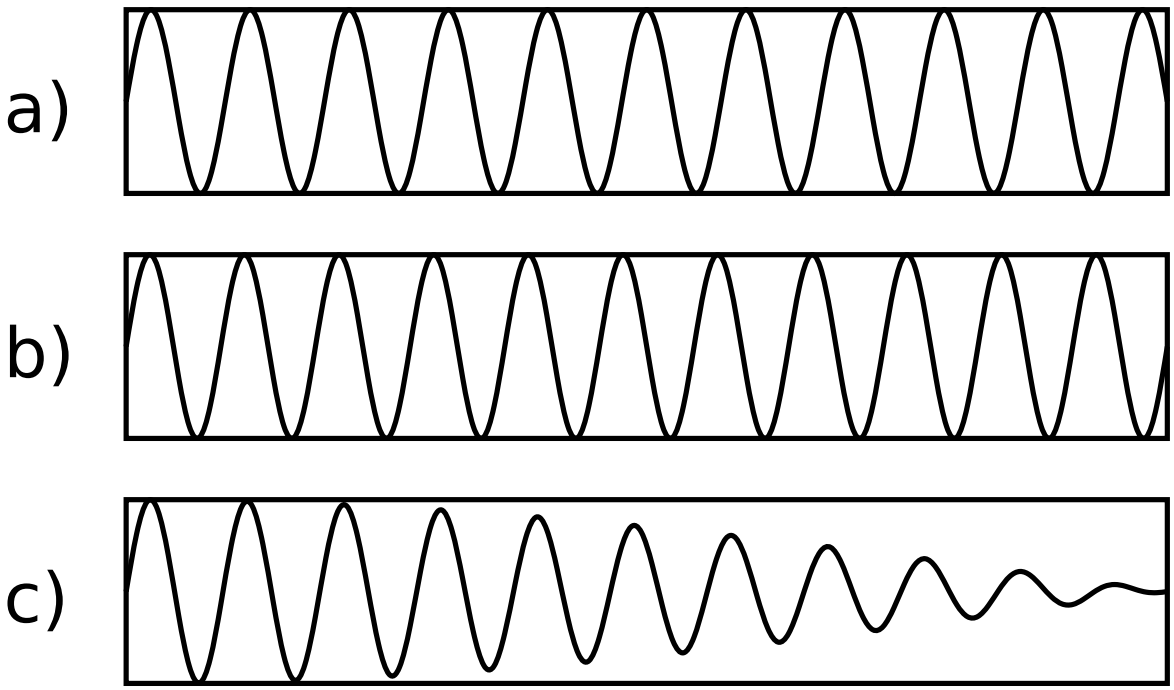


**Figure 2.2:** Schematic of the effect of a change in refractive index on the propagation of a light wave. An applied voltage changes the refractive index in the material as seen between a) and b) In this case b) has a slightly higher refractive index than a). This slight change in refractive index leads to a change in phase along the length of the material. c) shows the sum of the two waves at each point along the material. The peak to peak amplitude of c) is related to the phase shift between a) and b).

### 2.2.5 Plasmons

All optical modulation has also been achieved using plasmonic excitation of CdSe quantum dots [44]. The infrared light beam to be modulated is incident on a metal surface with a slit and a grove separated by an area filled with CdSe quantum dots. The transmission of the infrared beam through the slit is controlled by a visible light beam. The beams each create surface plasmon polaritons which interact, decreasing the transmission of the infrared beam.

## 2.3 Electro-optic Refractive

With electro-optic refractive technologies the refractive index of a material is controlled using an electrical signal. This imparts a phase shift onto the light (Fig. 2.2) which can be used directly to encode information on to the phase or polarization or used within other components to modulate the amplitude of the light.

The main electro-optic refraction effects that are useful in semiconductors are the Pockel's effect and the Kerr effect. Many different materials can be used which take advantage of the Pockel's effect including $LiNbO_3$, polymers and III-V semiconductors. With the Pockel's effect the refractive index of a material changes linearly as a function of an applied electric field [45]. The geometry of the crystal structure of the Group IV semiconductors prevents the Pockel's effect so it is not an option for Si electro-optic refraction [14]. With the Kerr effect the change in refractive index is proportional to the square of the change in the applied electric field. While this effect is present in Si it is much weaker than the free carrier density effect. In devices which use these effects the refractive index is modulated by modulating an applied voltage which controls the electric field across the material.

The refractive index of Si can be modulated by modulation of the free carrier density [46]. Both the real and the imaginary parts of the index of refraction will depend on the free carrier density. As the number of carriers is increased the refractive index will decrease and as the number of carriers is decreased the refractive index will increase. The change in the real part of the refractive index $\Delta n$ at a wavelength of 1550 nm is related to the change in electron $\Delta N_e$ and hole carriers $\Delta N_h$ by [13]:

$$\Delta n = -[8.8 \times 10^{-22} \Delta N_e + 8.5 \times 10^{-18} (\Delta N_h)^{0.8}] \tag{2.1}$$

Si devices that take advantage of this effect are constructed out of a pn junction, a pin junction, or a capacitive structure formed by a pin junction with an insulating barrier in the centre of the intrinsic region [47]. Designs based on the pin junction are referred to as carrier injection devices. The intrinsic region in which the light travels is initially free from carriers and the carrier injection devices increase the free carrier density by continuously injecting carriers into the junction. In capacitive structure designs the carrier concentration is increased by applying a forward bias to the device which increases the free carrier density by charging up the capacitive structure. This allows faster switching speeds than the carrier injection method which is limited by the relatively long minority carrier lifetimes. Carrier depletion methods make use of a pn junction design which is also not limited by minority carrier lifetimes. The application of a reverse bias across the junction will create a depletion zone in the junction which lowers the carrier density. In all of the methods the change in the free carrier density creates a change in refractive index which can be used with one of the following methods to create an optical amplitude modulator.

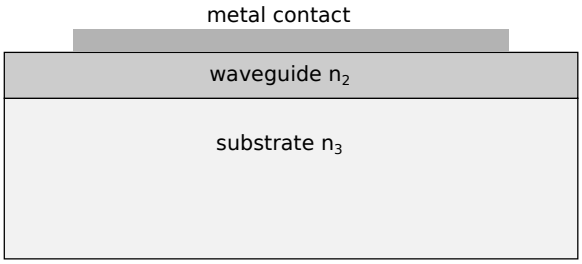


**Figure 2.3:** Diagram of a waveguide using electro-optic refractive effect to modulate the signal via cutoff frequency method. As voltage is applied to the top contact, $n_2$ approaches $n_3$ and confinement of optical mode decreases.

### 2.3.1 Mode Extinction

For the mode extinction technique a waveguide is fabricated using electro-optic refractive material. The waveguide is designed so that the frequency of the light to be modulated is just above the cutoff frequency of the waveguide. The refractive index of the waveguide $n_2$ is higher than but close to $n_3$, the refractive index of the substrate (Fig. 2.3). This allows the light to be guided through the waveguide when no voltage is applied. When a voltage is applied to the electro-optic material the index of refraction of the waveguide will decrease, changing the cutoff frequency [48]. The refractive index change is large enough that the frequency of the light is now below the new cutoff frequency and therefore the light will not propagate along the waveguide. The changing cutoff frequency imposes an amplitude modulation on the light wave. If the waveguide is not fully guiding at zero voltage a negative voltage can be applied to increase the refractive index of the waveguide to increase transmission for the on state. Kawabe *et al.* [49] demonstrated an ion beam etched $LiNbO_3$ ridge waveguide that was able to modulate 633 nm light using the cutoff frequency technique with an on voltage of -10 V and off voltage of +10 V. The following issues with this type of modulator mean it is not commonly used [45]:

1. The small change in refractive index ($\Delta n$) obtained by the electro optic effect means that high voltages are required. With $LiNbO_3$ and contacts separated by 10 $\mu$m, 100 Volts applied yields only a $\Delta n$ of $1.6 \times 10^{-4}$.

2. The small $\Delta n$ achievable means that the waveguide must be very close to mode cutoff in the on state in order to switch the signal off. This means the losses will be high in the on state.

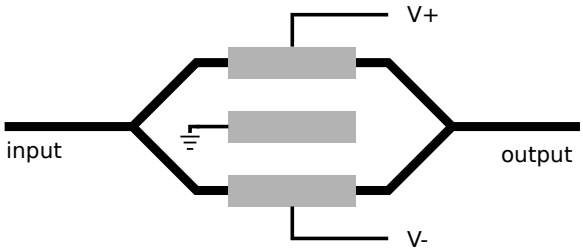


**Figure 2.4:** Diagram of an integrated Mach-Zehnder interferometer using electro-optic refractive effect to modulate the signal. Each arm contains electro reflective material and electrical contact. As opposite voltages are applied to the arms each path is phase shifted in opposite directions. When the light recombines at the output the phase shift difference leads to destructive interference.

### 2.3.2 Mach-Zehnder Interferometer

In a Mach-Zehnder interferometer optical modulator the waveguide carrying the light wave splits into two paths with equal amplitude which recombine at the output. Each path contains a section of electro-optic refractive material and either one or both contains a contact to apply voltage. Ideally, at zero applied voltage the optical path difference between the two paths will be equal and the signal will recombine constructively. The signal voltage is used to impart a relative phase shift on to the two paths. The optical path difference between the two paths determines whether the light combines constructively or destructively at the output. In general, the two paths are not exactly equal and therefore there will be some loss of power when no voltage is applied. This can be compensated for by having a non-zero applied voltage for the transmission setting or through the use of a balanced bridge approach [50].

State of the art silicon Mach-Zehnder interferometers have been recently demonstrated by Streshinsky *et al.* [51]. The modulators were fabricated from a standard SOI wafer of 220 nm Si on top of 2 $\mu$m $SiO_2$ above a high resistivity Si substrate. Doping was added during fabrication by implantation and rapid thermal annealing. Operating at 1300 nm with a contrast ratio of 3.4 dB, they have a modulation frequency of 50 Gbps using a swing voltage of 1.5 V and a bias of 0 V. In addition to the 3 mm long electro-optic phase shifters on each of the arms the design also uses thermal phase tuners on each of the arms to align the zero optical path difference point with the zero applied bias point. A cross section of the waveguide and electro-optic phase shifters is shown in figure 2.5.

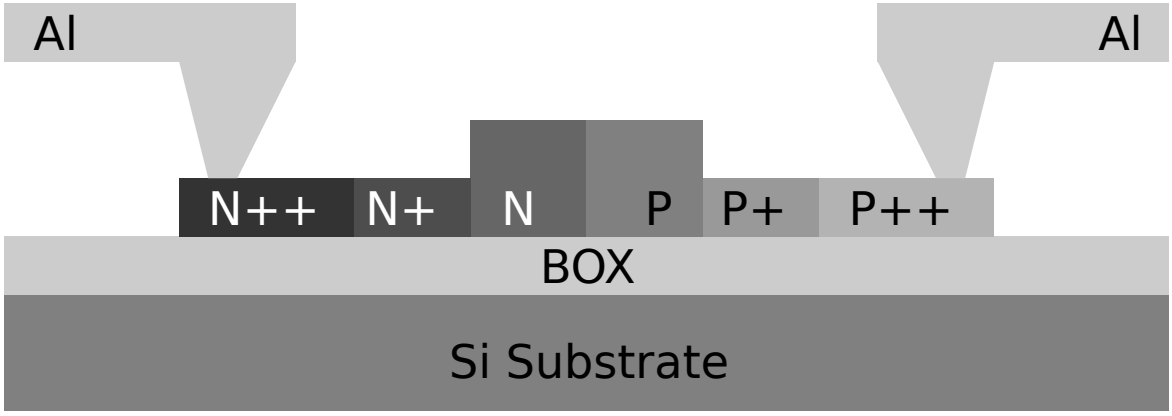


**Figure 2.5:** Cross-section of an integrated Si Mach-Zehnder interferometer using electro-optic refractive effect to modulate the signal. Waveguide is composed of n-type ($N_D \approx 5 \times 10^{17}\text{cm}^{-3}$) and p-type ($N_A \approx 7 \times 10^{17}\text{cm}^{-3}$) doped Si connected through higher doped (N+ and P+) Si to highly doped Si contact areas (N++ and P++), on top of a buried oxide (BOX) layer.

### 2.3.3 Dual Channel

Another method to modulate the intensity of the light is to use a dual channel waveguide setup. When two waveguides are closely spaced the light energy will periodically switch between waveguides. The distance required for the light to completely transfer from the first waveguide to the second depends on the spacing between and the refractive index of the waveguides. The dual channel waveguide is designed so that when no voltage is applied the light will complete an even number of transfers and be completely within the original waveguide. When a voltage is applied the refractive index of one of the waveguides is changed and the period for light to make a single transfer changes. If the refractive index change is such that there is an odd number of transfers the light will be completely in the second waveguide. This design is essentially a controllable power splitter and can also be used for fabrication of optical switches.

## 2.4 Electro-optic Absorption

An applied voltage can be used to directly modify the absorption spectrum of a material using the Franz-Keldysh or the quantum confined Stark effect.

### 2.4.1 Franz-Keldysh

The Franz-Keldysh (FK) effect manifests as a change in minimum absorption energy as a function of applied electric field for a bulk material. The absorption in a material has an exponential tail towards lower energies due to electric field induced ionization of the exciton [45]. The FK effect is due to the dependence of this exponential tail on the applied field. For wavelengths slightly below the wavelength of the bandgap the absorption can be modulated by changing the electric field in the material. The magnitude of the FK effect decreases for wavelengths further from the bandgap. The bandgap in Si is near 1.1 $\mu$m and therefore the FK effect in Si is quite weak for the important communications wavelengths of 1300 nm and 1550 nm [52]. Ge has a direct band gap at the energy of a 1550 nm photon and therefore the FK effect in Ge or high Ge content SiGe should be able to better modulate the absorption near 1550 nm. The effect has shown potential for modulation when using SiGe alloys in place of Si. SiGe devices have recently been demonstrated showing 3dB bandwidths of $>$ 40 GHz using the FK effect at 1550 nm but requiring 2.8 V swing voltage [53].

### 2.4.2 QCSE III-V

Electro-optic absorption based on the quantum confined Stark effect was demonstrated and theoretically explained by Miller *et al.* using GaAs/AlGaAs multiple quantum well structures [54]. While it was demonstrated using III-V materials it was acknowledged that the effect should be reproducible in any material system which provides type I band alignment. Devices fabricated from III-V materials have shown the ability to modulate optical signals in the communications bands. In 1994 Ido *et al.* demonstrated an InGaAs/InAlAs MQW structure showing good modulation at 1550 nm [55]. High speed operation in InGaAlAs/InAlAs MQW structures has been demonstrated producing $>$ 50 Ghz modulation of 3 dB with voltage swing of 1.1 V [56]. Efficient integrated laser and modulation has been demonstrated using InGaAlAs MQW structures for both laser diodes (LD) and QCSE modulators. The two devices can be monolithically integrated on InP substrates by epitaxial growth of the LD structure followed by selective removal and replacement of the LD structure by etching and growth of the QCSE structure [57]. Since III-V materials are not CMOS compatible they cannot take advantage of CMOS fabrication facilities. Monolithic integration with Si CMOS electronics is therefore not possible and while hybrid integration is a possibility they cannot take advantage of the CMOS facilities which are required for high volume production [58].

### 2.4.3 QCSE SiGe

Ge and SiGe alloys are compatible with and are currently in use in CMOS production facilities. The compatibility allows for the potential monolithic integration of Ge/SiGe optical components with CMOS electronics. Ge/SiGe hybrid integration solutions would benefit from the high volume production possible in CMOS production facilities.

In 2005 Kuo *et al.* demonstrated the first Ge/SiGe QCSE (2005) which showed modulation near a wavelength of 1450 nm [59]. The shift from a wavelength of 1550nm which is seen in bulk Ge is due to confinement of the wavefunctions in quantum wells and compressive strain in the material.

#### 1300 nm

To operate at the 1300 nm low loss optical fibre window it is required that the absorption edge is shifted to shorter wavelengths. This can be achieved during growth by having a higher level of compressive strain in the QW, thinner QWs, or GeSi wells in place of Ge wells [60]. Lever *et al.* experimentally demonstrated 1300 nm modulation from $Ge/Si_{0.4}Ge_{0.6}$ MQW structures grown on $Si_{0.22}Ge_{0.78}$ [61]. This design uses increased compressive strain to shift the absorption edge. Later improved electro-optic absorption at 1300 nm using QCSE structure was demonstrated using $Ge/Si_{0.35}Ge_{0.65}$ on $Si_{0.21}Ge_{0.79}$ [62].

#### 1550 nm

In 2006 Kuo *et al.* demonstrated the QCSE in SiGe at 1550 nm wavelengths [63]. This was achieved by a decrease in compressive strain, confinement energy and using a substrate temperature of 90 °C. Using selective area growth of a $Ge/Si_{0.15}Ge_{0.85}$ MQW structure Ren *et al.* demonstrated QCSE close to 1550 nm at room temperature with 8.0 V applied bias [64]. It has been demonstrated that the absorption wavelength in Ge QWs can be shifted to longer wavelengths by tensile strain induced reduction of the direct band gap energy [65].

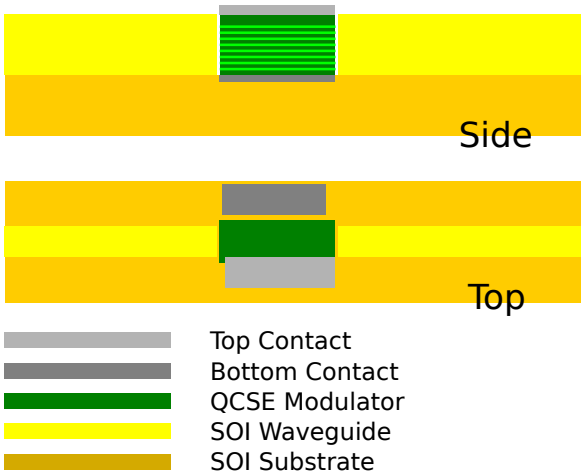


**Figure 2.6:** Side and top view of a QCSE modulator butt coupled to a SOI waveguide on a SOI wafer.

### Waveguide Integration

Monolithic integration of modulators coupled on chip to waveguides allows integration with other optical functions such as detection, propagation, and emission. Options to integrate waveguides and QCSE modulators include butt coupling the two components and evanescent coupling.

Integration of QCSE optical modulators with silicon on insulator (SOI) waveguides via butt coupling (Fig. 2.6) using selective area growth has been proposed [66] and demonstrated [67]. A SOI wafer is patterned and etched using a dual layer spacer approach leaving a protective oxide layer on the side walls of the etched areas. The Ge/SiGe MQW structure is epitaxially grown in the etched areas only. The oxide prevents growth from the side walls. The active layers of the MQW structure are now at the same height as the SOI layers so that after fabrication they are butt coupled together.

For modulators that are grown above the level of the waveguides, evanescent coupling can be used to transfer light into and out of the modulator. When the evanescent tail of the optical mode in the waveguide overlaps with the QCSE modulator evanescent coupling occurs [68]. Tapering of the QCSE modulator is used to improve insertion and extraction losses between the waveguide and modulator (Fig. 2.7). Edwards *et al.* have shown through optical simulations that this effect can provide efficient waveguide integration for QCSE modulators [2].

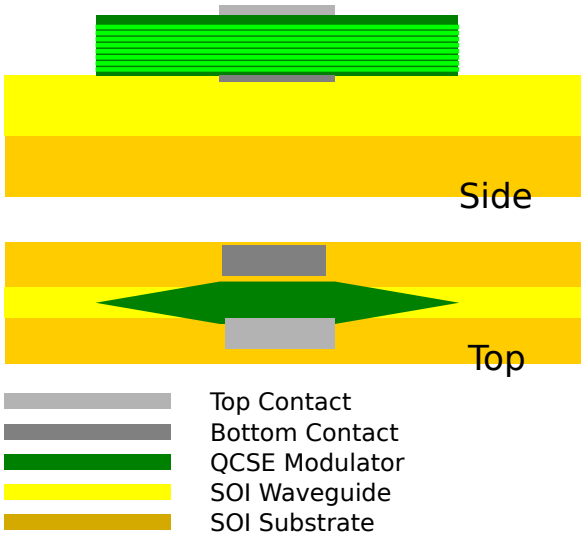


**Figure 2.7:** Side and top view of a QCSE modulator coupled evanescently to a SOI waveguide on a SOI wafer. Taper length and shape should be optimized to lower coupling losses.

## 2.5 Si Modulator Review

For the benefits of silicon photonics to be realized modulators which are compatible with Si CMOS fabrication processes are required. In Si the only potential mechanism for optical modulation for light at the communications bands is carrier depletion / injection. The Pockel's effect is non-existant and the Kerr and Franz-Keldysh effects are weak in Si at 1300 nm and 1550 nm wavelengths. The addition of Ge and SiGe alloys into the design allows more options for modulation while maintaining Si compatibility.

### 2.5.1 Carrier Density Modulation

Manipulating the carrier density of Si will alter its refractive index, allowing modulation when incorporated into one of the designs mentioned in the electro-optic refractive section. Designs for carrier injection devices on Si predicted modulation speeds of up to 5 GHz as early as 2004 [69]. Modulators based on the capacitive structure design were the first Si modulators to demonstrate $> 1$ GHz modulation monolithically integrated onto Si [70]. A Mach-Zehnder interferometer design was used and required a 10 mm long phase shifting segment on each arm to modulate a 1540 nm signal. Optimizations of this design have produced modulators that require phase shifter lengths of only 480 $\mu$m and a modulation frequency of 10 GHz.

Carrier depletion designs were proposed in 2005 which offered a potential modulation

frequency of 50 GHz. Devices similar to the proposed design were realized in 2007 which could operate at a modulation frequency of 20 GHz. This device used a 3 mm long phase shifter in a Mach-Zehnder interferometer to achieve modulation using a 6.5 V swing voltage [71].

### 2.5.2 Electro-optic Absorption Modulation

While both the FK effect and the QCSE allow modulation of the absorption edge of a material, the QCSE is more abrupt and stronger changes in the absorption spectra occur due to the discretization of the density of states and the stronger exciton effects [72]. The strong absorption of the QCSE requires very small thickness on the order of 1 $\mu$m which enables vertical devices to be effective. The weaker FK effect requires waveguide structures in order to achieve the required interaction lengths. Efficient optical modulation near 1550 nm via the FK effect was demonstrated using high Ge content SiGe in place of Si for the modulation region of the waveguide. A FK modulator with a small 55 $\mu$m long active region was demonstrated which showed modulation at 1550 nm with a modulation frequency $> 40$ GHz with a swing voltage of 2.8 V [53].

The much higher absorption shift due to the QCSE as compared to the FK effect allows much higher contrast ratios with lower requirements for swing voltage. In 2005 Kuo *et al.* [59] demonstrated the first Ge/SiGe QCSE which showed modulation near a wavelength of 1450 nm. A MQW structure with 10 Ge QW ($Si_{0.15}Ge_{0.85}$ barriers) with a thickness of 10 nm (16 nm) were grown on a $Si_{0.1}Ge_{0.9}$ fully relaxed virtual substrate. A 3 V change in applied voltage resulted in a contrast of 5 dB in absorption at 1438 nm. A design using a similar MQW structure was reported in 2012 demonstrating a high contrast ratio of 9 dB between applied biases of 3 V and 4 V [73]. Using the same alloy composition but with wider 12 nm QWs grown by selective area growth, modulation in the communications band near 1550 nm was demonstrated in 2011. The modulator demonstrated a contrast ratio of 3 dB at 1525 nm between 7 V and 8 V applied bias [67]. Most recently Edwards *et al.* have demonstrated a Ge/SiGe QCSE modulator with the ability to cover the entire communications band with a 6 dB contrast ratio and a 1 V swing [2]. This design used 5 Ge QWs 14 nm wide with 18 nm wide barriers $Si_{0.19}Ge_{0.81}$ on a $Si_{0.12}Ge_{0.88}$ virtual substrate. The low swing voltage modulation was achievable due to the small intrinsic region due to having only 5 QWs in the structure, and thinner spacer regions between the contacts and the QWs. Table 2.1 shows a summary of some of the features of the various Si based modulator technologies.

**Table 2.1:** Comparison of Si modulators demonstrated in the literature.

| Reference | $\lambda$ ($\Delta\lambda$) | $f$ | $\Delta V$ | Contrast | notes |
|---|---|---|---|---|---|
| CD[74] | 1550nm | 50 Gbit/s | 6 V | 5 dB | 1 mm long phase shifter |
| FK[53] | 1550 nm (35 nm) | 40.7 GHz | 2.8 V | 6 dB | 55 $\mu$m long waveguide |
| QCSE[59] | 1438 nm (10 nm) | | 3 V | 5 dB | |
| QCSE[73] | 1435 nm | 23 GHz | 1 V (3 V) | 9 dB | 1 V swing contrast ratio much less for other offsets |
| QCSE[67] | 1425 - 1540 nm | 3.5 GHz | 1 V (0 V-7 V) | 3 dB | |

## 2.6 Summary

There are multiple methods available for the modulation of optical signals. The main ones that are compatible with Si are free carrier modulation of the refractive index, which requires long waveguide to produce sufficient phase shift, and Franz-Keldysh absorption modulation, which is extremely weak near the communications bands. The incorporation of Ge onto Si extends the options for modulation in the communications bands. SiGe FK modulators have been shown to work at 1550 nm and require relatively short waveguides. Ge/SiGe QCSE devices have demonstrated the potential to allow modulation at both 1300 nm and 1550 nm. This work investigates QCSE using Ge/SiGe MQW structures designed to operate near 1550 nm. The benefits of these structures are that they use CMOS compatible materials which would allow the production to benefit from the high volume and low cost fabrication currently utilized in Si CMOS processor production. It also opens up the possibility of monolithic integration of these devices onto Si electrons, creating a potential solution to the electric interconnect problems facing the Si electronics industry. Compared to other Si compatible technologies QCSE have the promise of small physical size and low swing voltage requirements. The potential of the QCSE designs used in this work for use as modulators is investigated using computer simulations and photocurrent measurements of fabricated devices. Photodiode devices are used to measure the change in absorption of the structures under an applied bias. The photodiodes are fabricated from QCSE wafers grown by collaborators at Warwick University. The QCSE devices used in this work are fabricated in a cleanroom environment at the James Watt Nanofabrication Centre at the University of Glasgow. The techniques and processes used during device fabrication are described in the following chapter.

# Chapter 3

# Fabrication

## 3.1 Introduction

Fabrication of devices is explained in this chapter, including process flow and explanations of the reasons for various steps and any changes required during the development of the processes.

Fabrication processes are required in order to transform wafers into devices that can be characterized both electrically and optically. The devices are created by removing and adding different materials in a controlled manner. While each type of device uses a different fabrication process, a generalized overview of device fabrication is useful. The particular processes for fabricating AgSb contacts and QCSE photodiodes will be detailed separately.

## 3.2 Fabrication

### 3.2.1 Facilities

The majority of the work in fabricating devices was done in the James Watt Nanofabrication Centre (JWNC). The JWNC is a cleanroom facility which houses state of the art nanofabrication tools within a mixture of class 1000, class 100 and class 10 cleanrooms. The cleanroom level is the equal to the maximum number of particles

larger than 0.5 $\mu$m in diameter per cubic foot of air. For comparison purposes a typical clean indoor environment can contain 500000 particles larger than 0.5 $\mu$m per cubic foot of air [75]. As particles in the environment can contaminate the surface of a sample during fabrication, therefore potentially ruining devices, a clean room facility was essential for fabrication of the devices used in this work.

### 3.2.2 Cleaving

Each wafer used for fabrication in this work consists of epitaxially grown layers of SiGe and Ge on top of 525 $\mu$m thick Si (001). Each wafer is cleaved or diced into a number of small samples approximately 1 cm square. Each sample can then be processed separately. The small sample sizes means that many samples can come from each wafer. Before cleaving the wafer is covered with a resist on the top surface in order to protect the surface from particles created during the cleave. The wafers can either be diced into a uniform pattern of squares using an automated wafer dicer, or cleaved by hand as needed using a scribe pen. The scribe pen makes a small nick in the edge of a wafer and the wafer is placed over an edge and pressed down until it cracks along an atomic plane. The atomic planes of Si (001) wafers in the vertical direction are at right angles to each other allowing square samples to be cleaved.

### 3.2.3 Cleaning

In order to improve the quality and yield of each process step the sample needs to be as clean as possible. The standard two solvent cleaning process for a newly cleaved sample is an ultrasonic clean in acetone followed by 2-Propanol (IPA). The sample is then blown dry using nitrogen gas. While the acetone removes oils and organic residues from the surface, acetone residue is left on the surface after drying. The two solvent process is used because IPA dries clean without leaving residue but does not clean the surface as well as acetone. For subsequent cleaning processes the ultrasonic bath is avoided to prevent destruction of already fabricated structures.

### 3.2.4 Patterning

Patterning is used to determine which areas of the sample will be exposed to a later processing step. Both photolithography and electron beam lithography (EBL) can be

used to define a pattern onto the surface of a sample. A combination of resist and developer solution is used such that the areas that are exposed to ultraviolet (UV) light or high energy electrons will dissolve in the developer at a different rate then the unexposed areas.

### 3.2.5 Metal Deposition

Metal deposition is used to create a thin layer of metal on the exposed surface of the sample. There are two main types of metal deposition: evaporation and sputtering. Evaporation applies a non-conformal layer of the chosen metal or metals straight down on to the sample. Sputtering of metal is more conformal and therefore has better step coverage due to the wider range of delivery angles of the metal atoms.

### 3.2.6 Dry Etching

Dry etching is used to remove material from exposed areas of a sample in a controlled manner. A patterned sample is loaded into a dry etch tool and a specific recipe and time are chosen. The dry etch tool processes include high energy ions for physical bombardment of the surface, chemical reactions to create volatile molecules from the atoms on the surface, and protection layers in various ratios to control the speed and sidewall angle of the etch. The etch can be monitored *in-situ* by a laser reflectometer which can be used to determine etch stop times. The individual dry etch tools and recipes used will be detailed with their specific device processes.

### 3.2.7 Silicon Nitride Deposition

Silicon nitride deposition applies a conformal layer of $Si_3N_4$ over the surface of the sample. This provides a protective and insulating layer which allows larger bond pads to be deposited for the top contact without electrically contacting the bottom contact layer. The deposition parameters can be modified to deposit a nitride film with a chosen level of stress. The compressive stress in the nitride layer will apply tensile stress to the semiconductor layer beneath.

## 3.3 Photolithography

### 3.3.1 Photoresists

Photolithography utilizes light sensitive polymers know as photoresists in order to transfer a pattern from a photomask to the substrate. The two main categories of photoresist are distinguished by their tone which can be either negative or positive. The tone is determined by how the chemicals that makes up the resist react when exposed to UV light. With positive resists the exposed areas become more soluble in the developer solution while with negative resists the exposed areas become less soluble in the developer solution. The solubility of the resists can also be affected by exposure to heat. A schematic of the difference between positive and negative photoresists exposed to the same pattern is shown in figure 3.1. After exposure, development, and metal deposition the negative resist produces the inverse pattern to that of the positive resist. Both types of resist were used for the fabrication of devices, primarily Shipley Microposit S1818 positive photoresist and AZ2070 negative photoresist.

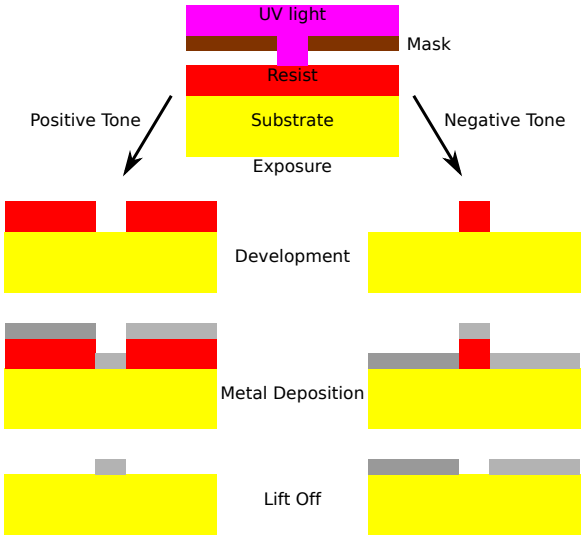


**Figure 3.1:** Difference between negative and positive tone demonstrated by metal deposition.

### 3.3.2 Dehydration Bake

In order to promote adhesion of the resist to the substrate a dehydration bake is performed. This drives off solvents or moisture that could be on the sample. The sample is placed in a 120°C oven for 10 minutes, after which the sample is allowed to cool before the resist is spun on.

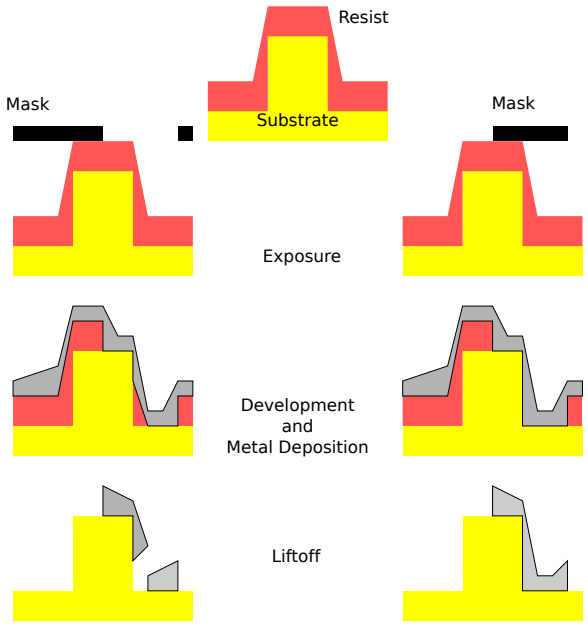


**Figure 3.2:** Comparison of negative and positive resist choices when creating bond pads connected to mesa tops. Resists are much thicker immediately beside a tall mesa structure. Positive resists are not fully exposed, leaving resist at the corner after development, while negative resists simply require slightly longer development time to be cleared.

### 3.3.3 Resist Spinning

Resist is applied to the substrate though a process call spin coating. The sample is placed onto a spinner and held in place by a vacuum. Resist is applied by dropper on to the sample and then the sample is spun at a high rate of speed. The length of time and the speed of the spin can be varied to change the thickness of resist after the spin is complete. Lower viscosity resists require a longer spin in order to have the same uniformity of thickness. The S1818 resist uses a spin rate of 4000 RPM and a time of 30 s in order to produce a resist thickness of 1.8 $\mu$m, while AZ2070 resist uses a spin rate of 4000 RPM and a time of 60 s in order to produce a resist thickness of 10 $\mu$m. Multiple layers of resist or of different resists can be applied to the sample same with a soft bake between spinnings.

### 3.3.4 Soft Bake

After spinning is complete a soft bake is required to prepare the resist for exposure. The samples are placed on a temperature controlled hot plate to evaporate the solvent that is in the resist and solidify the resist. For S1818 the soft bake is 120 s at 85 °C and for the AZ2070 it is 90 s at 110 °C.

### 3.3.5 Exposure

The exposure of the resist is performed using a Karl Suss Microtech MA6 mask aligner / exposure tool (MA6). The MA6 allows the operator to position the sample underneath a photomask and align with micrometer precision. The sample is then brought in to contact with the photomask and illuminated through the windows in the mask with UV light for a set exposure time. The exposure time required depends on the thickness and type of resist used. The S1818 resist requires 4.4 s exposure, while the AZ2070 requires a 20 s exposure.

### 3.3.6 Post Bake

After exposure some resists require an additional bake before development known as a post bake. The S1818 resist does not require a post bake, but one is required for AZ2070. The post bake hardens the exposed areas in the AZ2070 preventing them from being dissolved in the developer.

### 3.3.7 Development

In order to remove the resist from selected areas on the sample a specific developer is required. The developer will preferentially dissolve the exposed (unexposed) resist for positive (negative) photoresists. The side wall shape will depend on the exposure profile and the resist type. The choice of which resist to use will depend on what process is required for the pattern.

### 3.3.8 Mask Design

The photolithography masks are quartz plates with patterned chromium on one surface. The chromium is opaque to UV light while the quartz is transparent. To create the pattern in the chromium it is covered with an electron beam resist and exposed using a 100 keV electron beam from a Vistec VB6 electron beam lithography tool. The pattern is then developed and the exposed chromium etched away. The pattern written by the VB6 is controlled using computer data files that contain the patterns required. The patterns required for the fabrication of a device are designed using com-

puter aided design (CAD) software such as L-edit by Tanner EDA. Each lithography step tends to require a different pattern.

### 3.3.9 Alignment

In order to create a device with multiple lithography steps, which most devices require, all other exposures need to be precisely aligned to the first exposure. In order to align multiple layers the first layer creates alignment markers on the sample. All other patterns have matching alignment markers on the photomask. There are three degrees of freedom for the position of the sample relative to the photomask, $x$, $y$, and $\theta$, which can be manually adjusted using the MA6. Each marker contains a cross for coarse alignment ($\approx$5 $\mu$m) and vernier markers for fine alignment ($<$ 1 $\mu$m) (Fig. 3.3). To allow accurate alignment in $\theta$, alignment markers are placed on both the left and right of the sample and photomask. The further apart the markers are the more accurate the angular alignment can be. The maximum angular misalignment ($\phi$) can be calculated using equation 3.1.

$$\phi = (\delta y_1 + \delta y_2)/\Delta x \tag{3.1}$$

Where $\delta y_i$ is the maximum error in the alignment in the $y$ direction for the $i$th marker and $\Delta x$ is the distance between the two markers. For a 1 cm$^2$ sample the markers can easily be 8 mm apart. By aligning the vernier markers an accuracy of better than 1 $\mu$m for each marker can be achieved yielding a maximum angular misalignment of $2.5\times10^{-4}$ radians. Once the angle of the photomask is aligned to the sample a single marker can be used for alignment in the x and y directions.

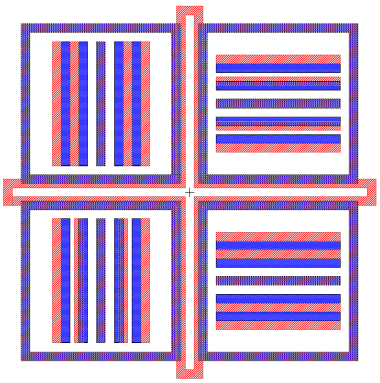

**Figure 3.3:** An photolithographic alignment marker as designed in L-edit. Blue areas correspond to the first layer which corresponds to metalized areas during alignment. Red areas correspond to second layer which will be transparent areas on the mask. Purple areas are areas of overlap. The large central cross is used for course alignment ($\approx$5 $\mu$m) while the vernier marks are used for fine alignment ($<$ 1 $\mu$m).

## 3.4 Electron Beam Lithography

Electron beam lithography (EBL) is the process of patterning a substrate using a beam of high energy electrons to expose a resist that is coating a substrate. The patterned resist is then developed leaving resist only where required. The high energy electron beam has a much lower wavelength than the UV light used in photolithography, allowing much smaller features to be patterned. Unlike photolithography, which exposes the entire pattern simultaneously, EBL is a serial process where only one point is exposed at a time and therefore requires longer write times for exposing larger areas. Similar to photomasks, patterns to be written using the EBL tool are designed using the L-edit CAD software. In addition the design needs to be fractured into trapezoidal shapes that can be written by the EBL tool. Write settings such as dose per area, beam size, and grid spacing need to be chosen depending on resist type and pattern feature size. Incorrect choice of settings can result in unnecessarily long write times or poor reproduction of the designed pattern.

### 3.4.1 Electron Beam Lithography Tool

The electron beam lithography tool available in the JWNC facility is a Vistec VB6 UHR EWF [76] (Fig. 3.4). The electron source is a Schottky emission gun, which uses a zirconium oxide coated tungsten cathode heated to 1800 K. The electrons are accelerated up to 100 keV by an electrostatic lens C1. Magnetic deflection coils are used to tilt and shift the beam to align it to the electron optical axis of the following lenses. Apertures are used at various positions in the column to limit divergence of the beam. The C2 lens is a magnetic condenser lens which allows a zoom lens function by C1 and C2. The final lens C3 provides the main focus for the beam onto the substrate. The beam is turned off and on during writing by use of a beam blanker, which turns the beam off by electrostatic deflection of the beam into an aperture. Between the final lens and the condenser lenses is the deflection unit assembly. It is comprised of sets of magnetic coils which create fields transverse to the beam to shift the beam in the x and y axis. The assembly consists of two sets of deflectors: main deflectors for large scale movements, and subfield deflectors for fine control. The deflectors can cover an area of 1.3mm by 1.3 mm. For patterns beyond that size the stage holding the substrate is moved during the writing process. The apertures can be adjusted to control the current and beam size used for writing the patterns. Large areas can be written quickly using large currents and beam sizes of up to 45 nm at 131 nA, while small features can be produced using small currents and beam sizes as low as 4 nm at 1

nA. Alignment between layers is controlled by use of alignment markers. The position of each marker is recorded in the data file used to write the pattern and the position on the substrate is measured automatically using a built-in electron microscope function of the VB6.

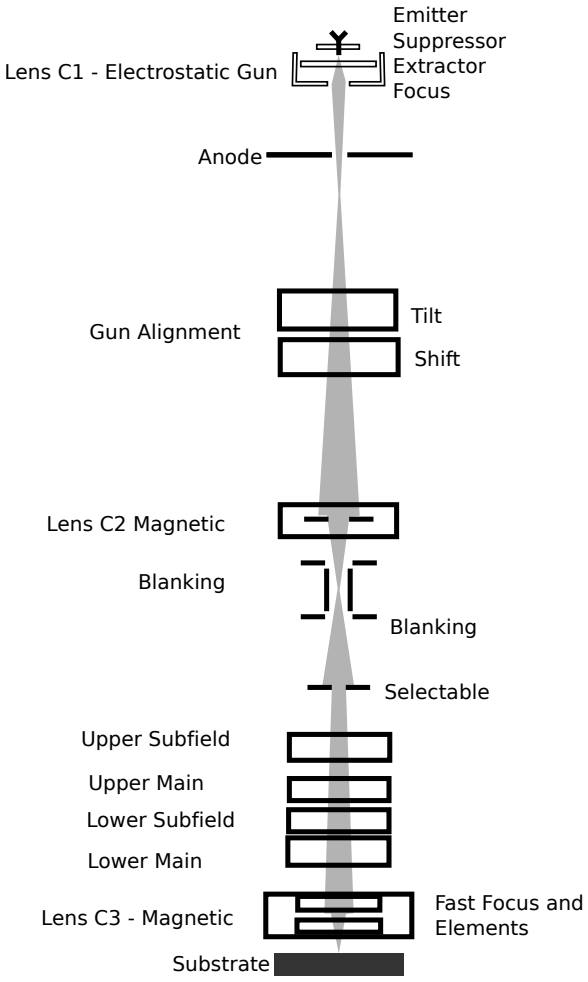


**Figure 3.4:** Diagram of the beam column of the VB6 electron beam lithography tool available in the JWNC. The magnetic and electrostatic lenses focus the beam while the magnetic deflectors control the position on the sample.

### 3.4.2 Electron Beam Resists

Like photoresists, electron beam resists also can be of negative or positive tone. The resists used in this work were poly-methyl methacrylate (PMMA) a positive tone resist and hydrogen silsesquioxane (HSQ) a negative tone resist.

### PMMA

PMMA is a positive tone electron beam resist which, due to the serial nature of electron beam exposure, is ideal for patterns that require large areas of the substrate covered after development. PMMA is applied to the substrate by spin coating in a similar process to photoresist with a spin speed of 5000 rpm for 60 s. In the JWNC PMMA is available in two types and various dilutions. The two types are 2010 and 2041 and have different sensitivities to electron beam exposure. The 2041 resist is less sensitive than the 2010 resist. The different dilutions allow different thicknesses of resist to be applied to a substrate. After a layer of resist is spin coated the sample is soft baked on a temperature controlled hotplate for 120 s at 154 °C to evaporate the solvent and solidify the resist.

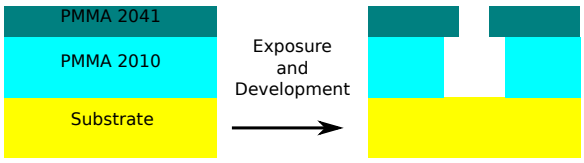


**Figure 3.5:** Illustration of PMMA bilayer using PMMA 2041 on top of PMMA 2010. After exposure and development an undercut profile is created, improving metal liftoff reliability for small features.

The 2010 and 2041 resist can be sequentially applied to a sample in order to create a bi-layer of PMMA. With the 2041 resist on top of the 2010 an undercut is created after development that is more reliable for metal liftoff than a single layer of PMMA (Fig. 3.5). The ideal thickness of PMMA depends on the subsequent process that utilises the pattern. Thinner PMMA layers require less exposure and allow higher resolutions but limit the amount of metal that can be reliably lifted off. PMMA is developed, which removes the exposed resist, using a 1:1 solution of methyl isobutyl ketone (MIBK) and iso-propanol (IPA). The solution is temperature controlled to 23 °C in a water bath during development. After 60 s of being lightly agitated in the solution the sample being developed is placed into a beaker of IPA to stop the development process and then blown dry in $N_2$.

### HSQ

HSQ is a negative tone electron beam resist and therefore is ideal for patterns that require large areas of the substrate to be free from resist. HSQ also has a higher selectivity for etching most materials than PMMA. HSQ is spun coated in a similar process to the other resists using a spin speed of 3000 rpm for 60 s. The thickness of

the HSQ layer can be controlled by dilution with methyl isobutyl ketone (MIBK). A 1:1 ratio was used throughout this work which results in a resist thickness of 300 nm. After spin coating the resist is soft baked on a temperature controlled hotplate for 120 s at 90 °C.

### 3.4.3 Proximity Effect

The proximity effect in electron beam lithography is the effect by which the exposure of an area of resist causes nearby areas of resist to also receive some exposure [77] (Fig. 3.6). This effect is due to forward scattering of the electrons in the resist and back scattering of electrons from the substrate back into the resist [78] and can be modelled by two Gaussians or more accurately through Monte Carlo simulations [79]. In order to correct for the proximity effect a process called proximity error correction is used. This process changes the relative exposure dose at each point so that the total dose received on areas that are required to be exposed will be equal. In general, the dose is increased for areas of low density and decreased for areas of high density. The relative doses are then multiplied by a constant factor to get the actual exposure dose which is determined by doing a dose test.

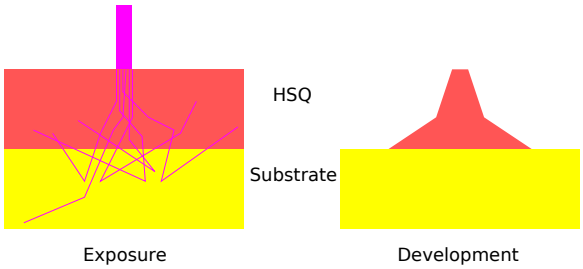


**Figure 3.6:** Illustration of forward and back scattering that leads to the proximity effect during electron beam exposure of a resist. Proximity effect causes the exposed area of the resist to be wider than designed if not properly taken into account during exposure.

### 3.4.4 Dose Testing

The correct dose to fully expose an area of resist will depend on many different factors, including the substrate below the resist, the thickness and type of resist, the density of the pattern, the developer solution, development time and temperature, and temperatures and times of soft bake and post bake. In order to determine the best dose to use for a new pattern a dose test is required. The new pattern or a large part of the new pattern is repeated multiple times on a single sample. Each copy of the pattern is exposed at a higher dose then the previous pattern. After development the sample

can be examined to determine which dose provided the best pattern as in figure 3.7. This dose can then be used for exposure of the pattern for device fabrication.

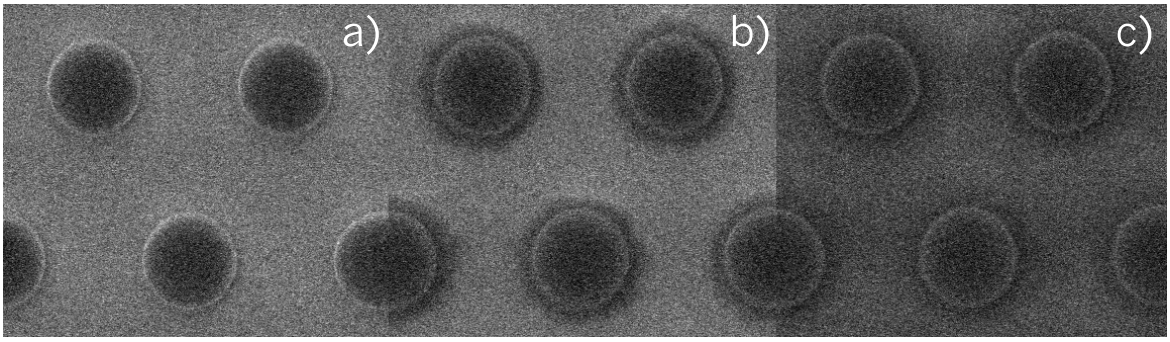


**Figure 3.7:** Dose test for 2D array of 1 $\mu$m radius circles patterned in HSQ. Scanning electron microscope image of circle arrays with three different doses after development. a) correct dosage, b) slightly overexposed, and c) highly overexposed.

## 3.5 Metal Deposition

Metal deposition is the process of creating a layer of metal on the surface of a sample. The metal can be patterned by etching or liftoff. Metal patterning was done throughout this work by the liftoff process. With metal etching the metal is first deposited over the entire surface of the sample. It is then coated with resist and patterned by photo- or electron beam lithography. After development of the resist the exposed metal is removed by wet or dry etching. The metal liftoff process begins with lithographic patterning of resist on the surface and is followed by the metal deposition. In the exposed areas the metal contacts and adheres to the surface while in the unexposed areas the metal lies on top of the resist. When the resist is removed the unwanted metal is removed as well.

### 3.5.1 Thermal Evaporation

In the JWNC the thermal evaporator is used to deposit metals that are not available in the electron beam evaporation systems. It was exclusively used in this work for the evaporation of a silver-antimony alloy (99% Ag 1% Sb). In the thermal evaporator the sample is placed upside-down above the metal target and the chamber is pumped down to high vacuum. The metal target is a thin wire coil of the desired material placed into a tungsten boat. A current is passed through the tungsten boat and it is heated through Joule heating. The metal target is heated through contact with the tungsten

boat. The evaporated metal travels from the target to the sample where it cools down on contact and adheres to the surface. The metal film created by thermal evaporation is non-conformal. The metal thickness is controlled by monitoring a crystal frequency. As metal is evaporated onto the sample, some is also evaporated onto the crystal. As the crystal accumulates metal the resonant frequency of the crystal decreases allowing accurate measurement of deposition rates and totals. The deposition rate is controlled manually by adjusting the current through the tungsten boat.

### 3.5.2 Electron Beam Evaporation

Like metal deposition by thermal evaporation, metal deposition by electron beam evaporation produces a non-conformal layer of metal with little to no sidewall coverage. Inside a vacuum chamber an electron beam is used to heat the surface of a metal target which vapourizes. The metal atoms travel to the sample, hitting the surface, cooling down, and sticking to the surface. The use of an electron beam to heat the target is an improvement over the thermal evaporation method. The electron beam causes a more localized heating which allows the crucible holding the metal target to be water cooled, preventing contamination from the heating of non-target metal. This allows a highly pure film to be deposited on to the sample.

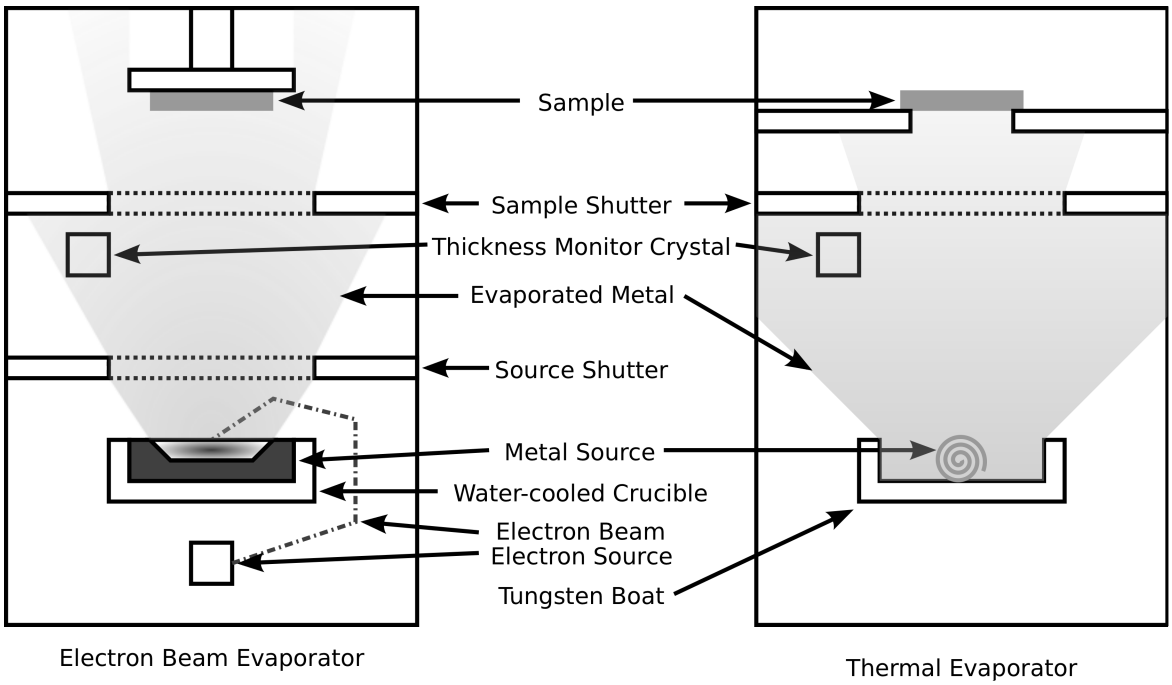


**Figure 3.8:** A schematic diagram of an electron beam metal evaporator and a thermal evaporator.

### 3.5.3 Metal Sputtering

Another method used to deposit metal was metal sputtering. A DC sputtering system like the one used in this work is composed of two planar electrodes. The target to be sputtered is placed on the cathode and the substrate on the anode. Argon gas is fed into the system and ionized and accelerated towards the cathode, striking the metal target and displacing metal atoms which can hit the substrate and adhere [80]. Metal sputtering creates a conformal layer of metal on the sample. This is useful when creating bond pads that are connected to the tops of mesas. The sputtering tool was exclusively used in this work to deposit aluminum bond pads. Figure 3.9 illustrates the difference between metal films deposited by sputtering and evaporation.

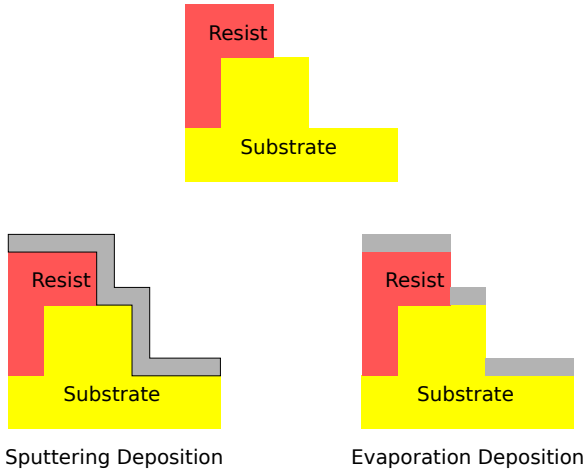


**Figure 3.9:** Comparison of metal deposition by electron beam or thermal evaporation vs sputtering. Sputtering creates a conformal layer of metal covering the sidewalls while evaporation deposits mainly on the top surface of a sample.

## 3.6 Etching

The removal of material from a sample is referred to as etching. There are two main types of etching: wet etching, in which a sample is placed in a liquid which chemically attacks the surface which tends to etch isotropically, and dry etching, which is done in specialized tools using plasma to chemically and physically etch the surface.

### 3.6.1 Wet Etching

To wet etch a surface a chemical etchant is chosen that has a high selectivity between the material to be removed and the underlying material or patterned resist. Due to the

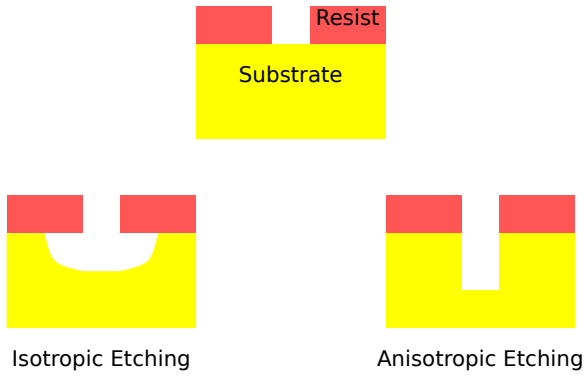


**Figure 3.10:** Illustration of isotropic and anisotropic etching. Isotropic etches such as wet etches remove material in all directions at the same rate, while anisotropic etching can etch vertically.

purely chemical nature of wet etching, the etch is usually isotropic. One of the most common etchants used in the work is hydrogen fluoride (HF). HF is used before metal deposition onto Si or Ge to remove the native oxide that grows on the Si or Ge surface. HF etches silicon oxide and germanium oxide at very high rates while having virtually no interaction with Si or Ge surface. For a detailed study of the etch rates for many combinations of etchant and material please refer to [81] and [82]. The correct choice of etchant can quickly etch away the unwanted material without damaging underlying material.

### 3.6.2 Dry Etching

When high aspect ratio features or precise etch depths are required dry etching is the preferred method. Dry etching tools can use chemical etching, chemical passivation, and physical etching to control the etch results. Anisotropic etches allow high aspect ratio features while computer control and fast switching allow precise control of etch depths. Two main types of dry etch tools are available in the JWNC: reactive ion etching (RIE) and inductively coupled plasma (ICP) machines.

#### RIE

In RIE tools a single power source is used for both plasma generation and for creating a bias. RF power is applied to two parallel plates generating a plasma of reactive ions and the table bias that accelerates the ions towards the sample. Therefore, any increase in plasma power to increase the etch rate will also increase the ion energy which lowers selectivity and increases damage.

#### ICP

ICP tools have a loop outside the chamber that inductively creates an e-field within the chamber, as well as an RF generator to control the table bias, allowing separate control over the plasma density and e-field. This allows for separate control over the ion density and ion energy. Higher etch rates are achievable with low damage and high selectivity since the ion density can be high and ion energy low.

#### Reflectometry

Etch depth can be monitored *in-situ* by laser reflectometry. A 632.8 nm laser is reflected off the surface being etched and the returned power is monitored. Prior to etching the sample an in-house Matlab program is used to simulate the reflectivity as a function of etch depth. During the etch the reflectivity is monitored to determine when the etch should be stopped. The reflectivity of the surface for 632.8 nm oscillates as a function of etch depth, $d$, following equation 3.2.

$$d = \lambda/2n \tag{3.2}$$

where $\lambda$ is the laser wavelength (632.8 nm) and $n$ is the refractive index of the material being etched. For Ge with a refractive index of 5.47 at 632.8 nm [83] this equates to one oscillation every 58 nm. Another effect that is more relevant for multiple quantum well structures is periodic change in reflectivity due to the change in Si and Ge content as the wells and barriers are etched through (Fig. 3.11).

### 3.6.3 Dry Etching Recipes

Different recipes are available depending of the material to be etched, the underlying material and the resist used for patterning. The chosen recipe effects the selectivity, the etch rate, and the side wall angle.

#### Si/Ge Etches

For the QCSE devices created in the work a mesa structure is etched into the sample to define the active area of the device. AZ2070 was used as an etch mask and a Surface

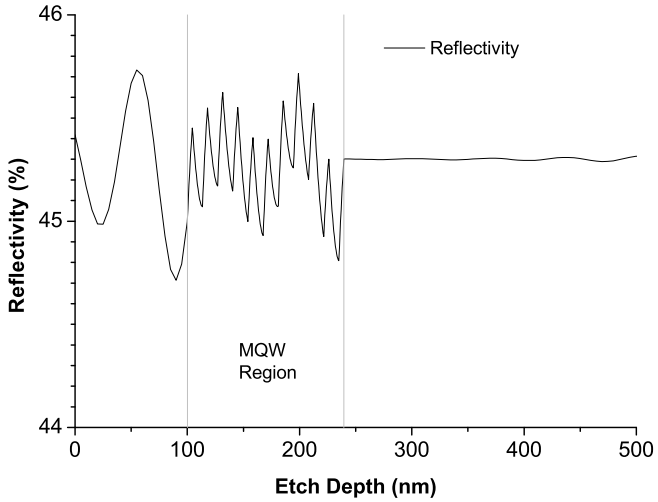


**Figure 3.11:** Plot of the calculated reflectometry data from Matlab simulation of QCSE device. Smooth oscillations during etch though upper layers of constant composition correspond to equation 3.2 while sharp oscillations correspond to transitions between barrier and quantum well regions.

Technology Systems (STS) ICP-RIE etch tool was used to etch the material. A mixture of $SF_6$ and $C_4F_8$ gasses was used with an etch rate of 130 nm/min. The $SF_6$ etches the Si and Ge while the $C_4F_8$ produces a non-volatile film which protects the sidewalls but is removed from the bottom surface by the physical etching of the plasma. This combination produces an anisotropic etch with a slight undercut profile. The etch is required to stop once the bottom contact region has been reached. The QCSE devices do not have an etch stop layer so the etch is monitored using reflectometry to determine the correct etch time.

### Silicon Nitride Etches

Silicon nitride is etched using an 80+ RIE etch tool. The gases used are $CHF_3/O_2$ which etches silicon nitride at a rate of 50 nm/min. The silicon nitride etches are used to create via holes to allow contact to the top and bottom contact layers from the bond pad. The underlying material for the QCSE devices during the via hole etch is Pt which acts as an etch stop for the silicon nitride etch. The Pt etch stop allows the etch time to be increased to ensure the silicon nitride is completely removed without fear of over etching negating the need for reflectometry.

## 3.7 Dielectric deposition

Dielectric deposition is used to create a protective insulating layer on the substrate. Silicon nitride films are deposited with an ICP tool using precursor gases $SiH_4$ and $N_2$ [84]. The insulating layer allows for the deposition of large bond pads to allow wire-bonded connections to top contact layers on small devices. Silicon nitride deposition can also be used for process induced strain. Silicon nitride layers that are compressively strained on top of the substrate will impart tensile strain into the substrate. The strain imparted will affect the electrical and optical properties of the material, opening up another method for controlling device properties.

## 3.8 Summary

In order to create useful devices from wafers various fabrication techniques are required. The device is built up using both additive and subtractive processes. Each process is comprised of many steps, each of which is important to be able to repeatably produce working devices. The following chapter will discuss the development and analysis of a metal contact process, which utilizes a number of the techniques discussed in this chapter, that was developed for creating Ohmic contacts to moderately doped n-type Ge layers.

# Chapter 4

# Silver Antimony Ohmic Contacts to n-Ge

## 4.1 Introduction

An important part of Ge-on-Si photonic devices is creating electrical contacts to semiconductor layers. High quality electrical contacts improve the power efficiency of fabricated devices. There is an increasing interest in using Ge for both electronic and optical devices on Si substrates to expand the functionality of Si technology. Ge is an attractive material for use in many different technologies including end-of-roadmap complementary metal-oxide semiconductor (CMOS), where its higher carrier mobilities compared to Si would potentially allow for reduced power operation[85]. Ge integration has benefits for Si photonics devices[86] such as photodetectors[87], single photon avalanche detectors[38], modulators[59] and Ge lasers[10]. Ge has also been used for spintronic devices[88] along with thermoelectrics[89] and there have been proposals for Ge/SiGe quantum cascade lasers (QCLs) [90]. Poor electrical contacts to n-Ge are a potential roadblock to the majority of these applications. Since non-Ohmic contacts require electrons to be thermally excited to overcome the barrier they result in 'hot' electrons entering the semiconductor. n-type Ge/SiGe QCLs are precisely designed such that the path of the electrons through the quantum wells leads to population inversion allowing gain via stimulated emission [91]. The 'hot' electrons from non-Ohmic contacts are detrimental to such devices since the higher energy electrons lead to excess current not along the prescribed path. With Ohmic contacts the number of high energy electrons is reduced since the electrons do not require excess energy to overcome a barrier.

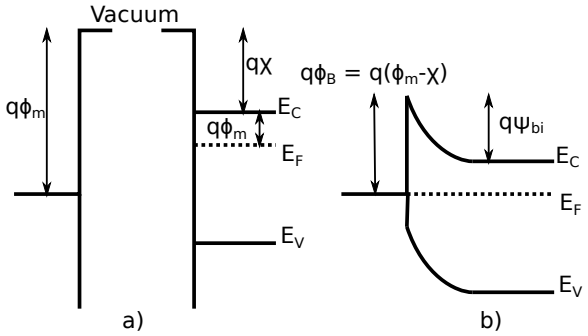


**Figure 4.1:** A schematic diagram of an ideal metal-semiconductor contact. a) Energy levels for metal and semiconductor before contact. b) Energy levels for metal and semiconductor after contact in ideal case.

Low resistive Ohmic contacts to n-Ge are difficult to achieve because of strong Fermi level pinning at the charge neutral level (0.08 to 0.09 eV), [92, 93] just above the valence band. This produces a large Schottky barrier height at the metal-Ge interface [94], which is relatively independent of the metal work function (pinning factor S=0.02 to 0.05) [92, 93]. While the cause of the Fermi level pinning is not fully understood, multiple methods to overcome the pinning and form an Ohmic contact have been suggested. Degenerately *in-situ* P doped n-Ge can support Ohmic contacts to annealed Ni [95, 96]. The large dopant concentration required to achieve Ohmic behaviour results in segregation of the n-type dopants during chemical vapour deposition (CVD) which is detrimental for many vertical devices since any other epitaxial layers subsequently grown will be unintentionally doped [97]. Other methods investigated include lowering the barrier height by ion implantation [98, 99, 100], inserting an interfacial layer, [94, 101, 102, 103] and the deposition of Yb capped with $SiO_2$ [104]. AgSb alloys have been shown to form Ohmic contacts to low Ge concentration n-type $Si_{1-x}Ge_x$ alloys, [105] leading to the investigation of AgSb for this moderately doped n-Ge layer.

### 4.1.1 Theory of Contacts

To connect a circuit to a semiconductor device electrical contacts are required. This requires a metal-semiconductor junction. According to Schottky theory [106] the barrier height will be equal to the difference in the work function in the metal ($\phi_m$) and the electron affinity ($\chi$) in the semiconductor (Fig 4.1). Therefore ideally it should be possible to create an Ohmic contact to an n-Ge layer simply by choosing a metal with the correct work function such that the barrier height is zero. Experimentally it has been seen that the barrier height is actually relatively independent of the metal work function. This effect is known as Fermi level pinning.

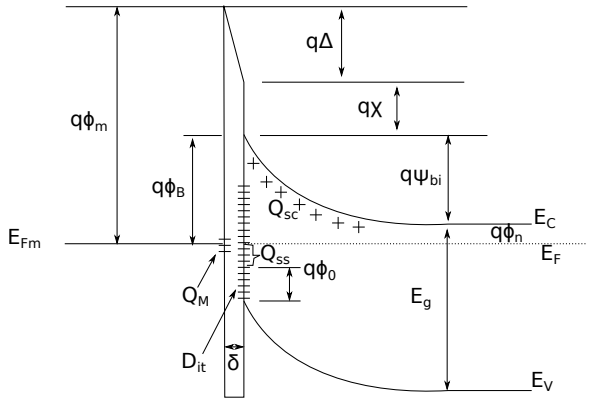


**Figure 4.2:** Energy diagram of metal-semiconductor interface with interface states for n-type semiconductor.

### Fermi Level Pinning

There are two main competing theories for the cause of Fermi level pinning: surface interface states, and metal induced gap states (MIGS).

### Surface Interface States

In surface interface state theory it is assumed that there is an interface layer between the semiconductor and the metal which is an intrinsic part of the semiconductor and therefore independent of the metal. The charge neutral level (CNL) is the energy level ($q\phi_0$ above the valence band) within the semiconductor band gap above which the states are acceptor like and below which the states are donor like. If the semiconductor is acceptor type then the Fermi level is above the CNL as shown in figure 4.2. The interface is assumed to be thin enough that it is transparent to electrons, *ie.* electrons can tunnel through with 100 percent probability, but able to support a potential drop. The interface trap charge $Q_{ss}$ and the depletion layer charge in the semiconductor $Q_{sc}$ are given by [107]

$$Q_{SS} = -qD_{it}(E_g - q\phi_0 - q\phi_b) \tag{4.1}$$

and

$$Q_{SC} = \sqrt{2q\epsilon_s N_D \left(\phi_B - \phi_n - \frac{k_B T}{q}\right)} \tag{4.2}$$

where $D_{it}$ is the interface trap density and $N_D$ is the dopant concentration. For thin interfacial layers where space-charge effects are negligible an equal and opposite charge $Q_M$ develops on the surface of the metal.

$$Q_M = -(Q_{SS} + Q_{SC}) \tag{4.3}$$

The potential $\Delta$ across the interfacial layer from Gauss' law is:

$$\Delta = -\frac{\delta Q_M}{\epsilon_i} \tag{4.4}$$

where $\epsilon_i$ and $\delta$ are the permittivity and thickness respectively of the interfacial layer. From the energy band diagram (Fig. 4.2) and using the fact that the Fermi level must be constant throughout the system at thermal equilibrium $\Delta$ can be equated with other energies in the system.

$$\Delta = \phi_m - (\chi + \phi_B) \tag{4.5}$$

The barrier height $\phi_B$ can be solved for by equating the right hand sides of equations 4.5 and 4.4 then substituting in equations 4.3, 4.2, and 4.1. Rearranging the equation, introducing $C$, and making some simplifying assumptions gives:

$$\phi_B = C(\phi_m - \chi) + (1 - C)\left(\frac{E_g}{q} - \phi_0\right) \tag{4.6}$$

$$C = \frac{\epsilon_i}{\epsilon_i + q^2 \delta D_{it}} \tag{4.7}$$

The two limiting cases are when $D_{it} \to \infty$ which leads to $C = 0$

$$\phi_B = \frac{E_g}{q} - \phi_0 \tag{4.8}$$

or when $D_{it} \to 0$ which leads to $C = 1$

$$\phi_B = \phi_m - \chi \tag{4.9}$$

In the first case, where the interface trap density goes to infinity, corresponds to a barrier height which is completely independent of the metal work function. The Fermi level is completely pinned. In the second case, where the interface trap density is zero, the barrier height is equal to the difference between metal work function and semiconductor electron affinity. This is the ideal case with no Fermi level pinning. In this model, the interface trap density determines the level of pinning. The Fermi level pinning of a semiconductor is quantified using the pinning factor $S$.

$$S = \frac{\delta \phi_B}{\delta \phi_m} \tag{4.10}$$

The pinning factor is the rate of change in barrier height with change in metal work function, where $S = 0$ corresponds to a completely pinned semiconductor, and $S = 1$ corresponds to the ideal case of no pinning.

### Metal Induced Gap States

According to MIGS theory, electron states in the metal have exponentially decaying tails in the band gap of the semiconductor [108]. The states that are above the CNL will be empty while the states below will be filled, leading to either a positive or negative net charge at the interface which has qualitatively the same effect as the surface interface states as discussed above. The Fermi level is then pinned at the CNL, creating a barrier height which is independent of the metal work function.

### Experimental Barrier Height of Metal-Ge Contacts

It has been shown experimentally that metal-Ge contacts have a near zero pinning factor ($S = 0.02$ to $0.05$) [92, 93]. In Ge the CNL is just (0.08 to 0.09 eV)[92, 93] above the valence band, leading to large Schottky barrier heights (around 0.55 eV) for n-type Ge contacts and low barrier heights for p-type Ge contacts.

### Conduction Mechanisms

The conduction across a barrier is categorized into three different regimes which depend on the dominant emission. Which regime the conduction is in depends on the size of the barrier between the metal and semiconductor. For a semiconductor with a low doping concentration the conduction will be in the thermionic emission regime. In the low-doped regime the carriers are unable to tunnel through the barrier and require enough energy to overcome the barrier. The total current density in the thermionic regime ($J_{TE}$) for a forward bias $V$ can be expressed as follows:

$$J_{TE} = A^* T^2 \exp\left(\frac{-q\phi_B}{k_B T}\right) \exp\left(\frac{-qV}{k_B T}\right) \tag{4.11}$$

where $A^*$ is the Richardson constant which is 143 $\mathrm{Acm^{-2}K^{-2}}$ for n-Ge[93]. In this regime the current density is effectively independent of the doping density. As the doping increases the barrier becomes thinner and because the band edge is curved the barrier is thinner near the top than at the bottom. At moderate doping densities the conduction transitions into the thermionic field emission regime ($J_{TFE}$). In this regime carriers with sufficient energy are able to tunnel through the barrier.

$$J_{TFE} = \frac{A^* T \sqrt{\pi E_{00} q(\phi_B - \phi_n - V_F)}}{k_B \cosh\left(E_{00}/k_B T\right)} \exp\left(\frac{-q\phi_n}{k_B T} - \frac{q(\phi_B - \phi_n)}{E_0}\right) \exp\left(\frac{qV_F}{E_0}\right) \tag{4.12}$$

where

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{m^*\epsilon_s}} \tag{4.13}$$

$$E_0 \equiv E_{00}\coth\left(\frac{E_{00}}{k_BT}\right) \tag{4.14}$$

At extremely high doping levels the carriers are able to tunnel through the barrier without requiring any energy above the conduction band. When this happens the conduction enters the field emission regime in which the dominant conduction mechanism is the tunnelling of carriers through the barrier. There is therefore very little temperature dependence relative to the other regimes. When the contact is in the field emission regime the conduction will be Ohmic.

$$J_{FE} \approx \frac{A^*T\pi\exp(-q(\phi_B - V_F)/E_{00})}{c_1k_B\sin(\pi c_1k_BT)} \tag{4.15}$$

where

$$c_1 \equiv \frac{1}{2E_{00}}\log\left(\frac{4(\phi_B - V_F}{-\phi_n}\right) \tag{4.16}$$

Comparing $E_{00}$ to $k_BT$ allows one to determine the conduction regime. If $E_{00} \gg k_BT$ then the conduction will be in the field emission regime, if $E_{00} \ll k_BT$ then the conduction will be in the thermionic emission regime. Otherwise the conduction will not be dominated by either field emission or thermionic emission and therefore be in the thermionic field emission regime. The regime therefore depends on both the temperature and the doping density. The difference in the three regimes can be seen in figure 4.3 where the thermionic and field emission current densities are plotted for each of the three regimes as a function of doping concentration.

### 4.1.2 Ohmic Contacts to n-Ge

Previous work done in this group has shown that degenerately *in-situ* P doped n-Ge can support Ohmic contacts to annealed Ni [95, 96]. The large dopant concentration required to achieve Ohmic behaviour results in segregation of the n-type dopants during chemical vapour deposition (CVD) which is detrimental for many vertical devices since any other epitaxial layers subsequently grown will be unintentionally doped [97]. Other methods which have been investigated include lowering the barrier height by ion implantation [98, 99], inserting an interfacial layer [94, 100, 102, 103], and the deposition of Yb capped with $SiO_2$[104].

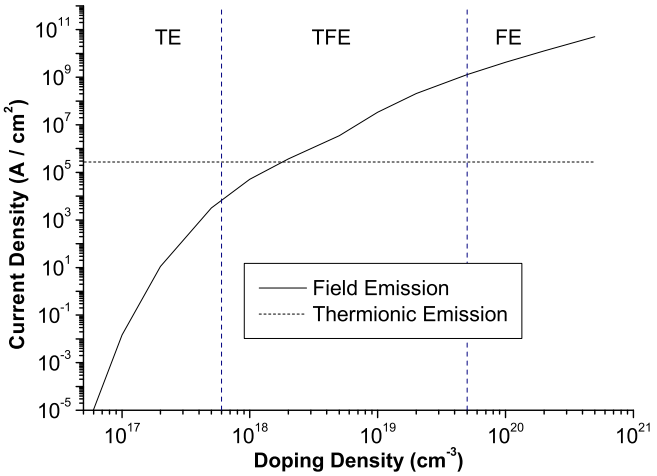


**Figure 4.3:** A comparison of the three conduction regimes in a Ge contact. As doping level is increased field emission increases to the point where it is dominant over thermionic emission. Regimes of thermionic (TE), thermionic field (TFE), and field emission (FE) are shown.

### 4.1.3 Growth Issues

Ideally an n-type Ohmic contact in Ge would be created by highly doping [95] ($N_D > 1 \times 10^{19}$ cm$^{-3}$) the semiconductor contact layers during epitaxial growth. A high enough dopant level such that electron transport between the metal and the semiconductor would be in the field emission regime would allow low resistivity NiGe contacts to be used. While this is useful for top contact layers, this is not possible for contacts layers that are below active regions that are required to be intrinsic. The n-type dopants in germanium will diffuse due to the high temperatures [109] experienced during growth. The high level of dopants required for standard n-type Ohmic contacts below the active layers will cause these layers to be unintentionally doped due to the high diffusivity of the n-type dopants in Ge which increases with higher doping concentrations [97, 110, 111].

### 4.1.4 Characterization of Contacts

To determine the quality of the contacts, test structures are fabricated and measurements are made. Test structures fabricated to characterize the contacts consist of circular transfer length method (CTLM) structures [112] to determine contact resistivity, lines of contacts for structural characterization, and two terminal wirebonded contacts for low temperature measurements.

### Low Temperature Measurements

As conduction by field emission has a low temperature dependence, and thermionic emission has high temperature dependence, the resistance of the contacts as a function of temperature can be used to determine the conduction regime. As the temperature is decreased the average energy of the electrons will decrease and less electrons will have enough energy to surmount the barrier. This results in less conduction due to thermionic emission. Field emission, on the other hand, has comparatively less dependence on temperature as the energy distribution of the electrons has very little effect on the tunnelling probability. Therefore, if the dominant conduction mechanism at room temperature is field emission there will be little change in conduction as the temperature is decreased, if the dominate conduction mechanism is thermionic emission the conduction will decrease exponentially as the temperature decreases.

### Specific Contact Resistivity

The specific contact resistivity is a standard metric for the quality of a Ohmic contact which is independent of contact size. A lower specific contact resistivity contact process results in a lower total resistance when comparing contacts of equal size. Test structures are required to extract the specific contact resistivity for a contact. Test structures that can be used to determine the specific contact resistivity include cross bridge Kelvin resistors structures, transfer length method structures and circular transfer length method structures.

### Cross Bridge Kelvin Resistor

A cross bridge Kelvin resistor (CBKR) is a four probe technique used to measure the contact resistance. Two adjacent arms of the cross are formed by a mesa in the semiconductor, and the opposite two arms are formed by metal with contact between them forming a square in the centre (Fig. 4.4). The measurement is setup so that the current flows in one semiconductor arm through the contact and out the opposite metal arm, while the voltage is measured from the remaining arms. Since ideally no current flows through the voltage arms the voltage difference measured will be the voltage difference of the contact, eliminating parasitic resistances from the measurement. The

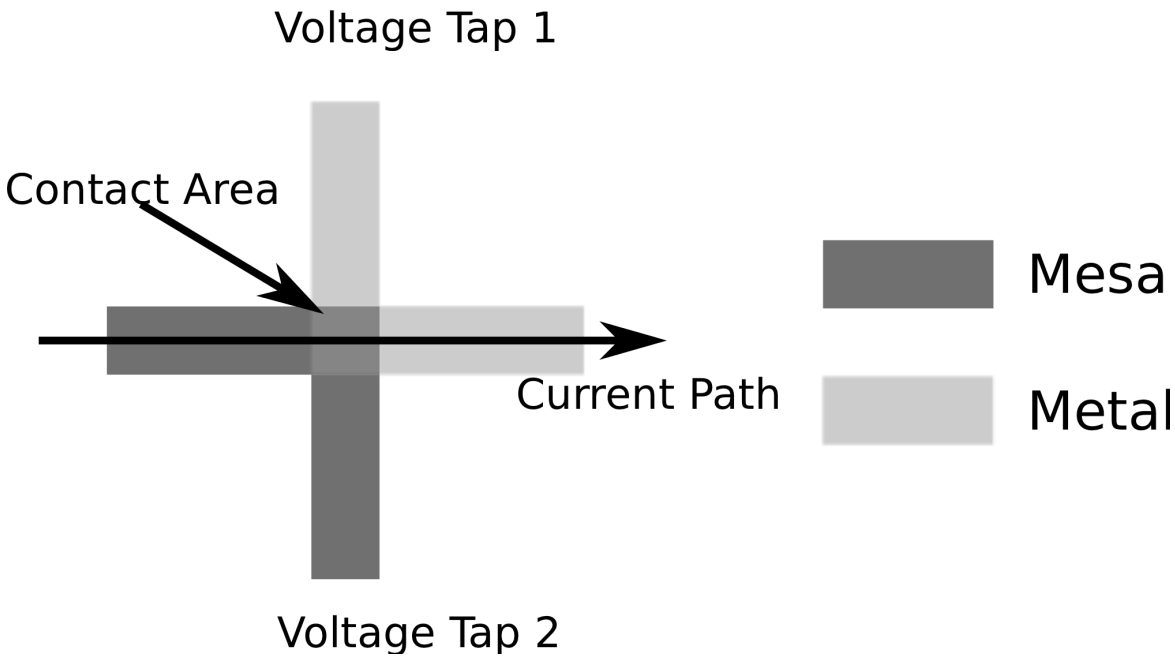


**Figure 4.4:** A schematic diagram of a CBKR structure. Probes are placed on the ends of each arm with the current flowing left to right while the voltage difference is measured between the upper and lower arms.

contact resistance $R_C$ for a current $I$ will therefore be

$$R_C = \frac{V_1 - V_2}{I} \tag{4.17}$$

where $V_1 - V_2$ is the voltage difference between the two voltage measurements. The specific contact resistivity $\rho_c$ can then be calculated from $R_C$ and the contact area $A$.

$$\rho_c = R_C \times A \tag{4.18}$$

This calculation for the contact resistivity assumes that the arms are perfectly aligned and the contact area covers the entire centre area. For real devices there will be a non-zero misalignment between the two layers which will lead to some current flow within the voltage arms. This causes the voltage difference between the arms to be higher than the voltage drop across the contact. The misalignment will cause the resistivity to be over estimated by this method. Another factor is that fabrication of a CBKR requires four lithography steps: a mesa layer, a contact layer, a via hole layer, and a layer for the metal arms. A passivation layer is also required. Contact pads for all four arms can be deposited simultaneously with the metal arms.

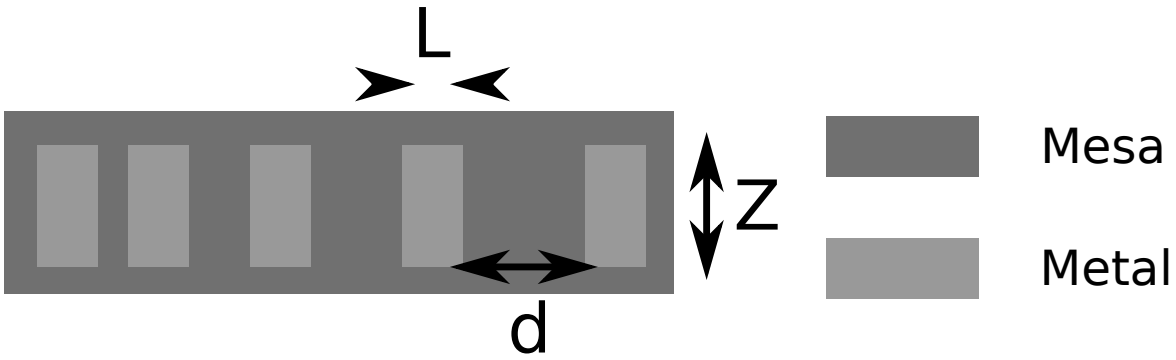


**Figure 4.5:** A schematic diagram of a TLM structure. $L$ is the length of each contact, $Z$ is the width, and $d$ is the gap spacing, shown for one of the pairs of contacts.

### Transfer Length Method

Another type of structure used to determine the specific contact resistivity of a contact is known as a transfer length method (TLM) structure. A series of identical rectangular contacts of width $Z$ and length $L$ is fabricated with increasing gap spacing $d$ between each pair of contacts (Fig 4.5). The area is isolated electrically by a mesa etch surrounding the series of contacts. TLM structures have a simpler fabrication process than CBKR structures requiring only one metal deposition step and one mesa etch. The total resistance ($R_T$) between contacts with spacing $d$ is

$$R_T(d) = \frac{R_{\text{sh}} d}{Z} + 2R_C \tag{4.19}$$

Therefore the contact resistance is equal to half the measured resistance for a gap spacing of zero. While this cannot be measured directly it can be extrapolated by measuring $R_T$ for multiple gap spacings and using a linear fit. The specific contact resistivity can then be calculated using equation 4.18 where $A = LZ$.

While TLM structures do not suffer from the accuracy problems for low specific contact resistivity values [113] that CBKR structures do, they still suffer from alignment issues. If there is a gap between the edge of the contact and the edge of the mesa there will be some spreading of current which will effect the measurement.

Both of these methods have the disadvantage of requiring multiple lithography steps. Having multiple lithography steps adds to the time and complexity of the fabrication. It also introduces alignment errors which lead to errors in the extracted specific contact resistivity. CTLM structures require only a single lithography step, eliminating layer to layer alignment issues. They can also be easily added as test structures within a device fabrication process (ideally in the same steps as the device contacts).

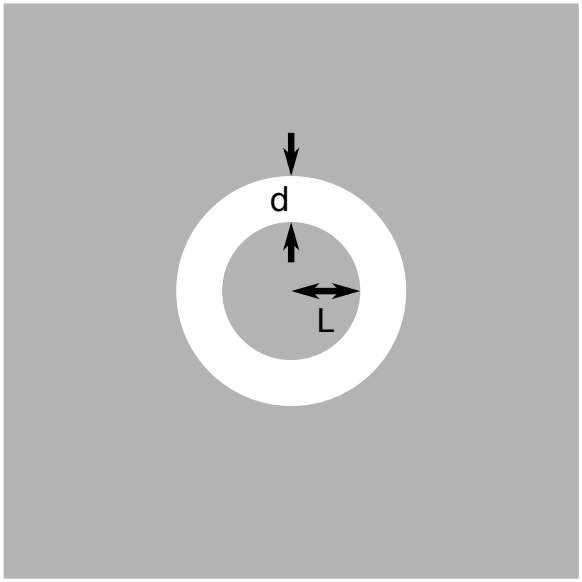


**Figure 4.6:** A schematic diagram of a CTLM structure $L$ is the radius of the inner contact while $d$ is the gap spacing.

A CTLM structure consists of an inner circular contact surrounded by an annular gap within a larger contact area. Each measurement set contains multiple CTLMs with varying gap sizes. In order to measure the contact resistivity, the resistance due to the contact must be isolated from the other components of the measured resistance. To remove any resistance in the wires or probes from the measured resistance the four-point measurement technique is used. One pair of probes supplies a voltage and measures the current while the second pair are current limited to measure the difference in voltage between the two contact areas. The total resistance measured ($R_m$) can be expressed as [114]

$$R_m = \frac{R_{\text{sh}}}{2\pi}\left(\ln\left(\frac{L+d}{L}\right) + \frac{L_T I_0(L/L_T)}{L I_1(L/L_T)} + \frac{L_T K_0((L+d)/L_T)}{(L+d)K_1((L+d)/L_T)}\right) \tag{4.20}$$

where $I_0$, $I_1$, $K_0$ and $K_1$ are the modified Bessel functions, $L_T$ is the transfer length, $L$ and $d$ are the radius and gap spacing as shown in figure 4.6. When $L > 4L_T$ then $\frac{I_0(L/L_T)}{I_1(L/L_T)}$ and $\frac{K_0((L+d)/L_T)}{K_1((L+d)/L_T)}$ can be approximated by unity, simplifying equation 4.20 to

$$R_m = \frac{R_{\text{sh}}}{2\pi}(d + 2L_T)C \tag{4.21}$$

where

$$C = \frac{L}{d}\ln\left(1 + \frac{d}{L}\right) \tag{4.22}$$

For each contact resistivity measurement the resistance of multiple CTLM structures with different gap spacings ($d$) is measured. $R_m$ is a non-linear function of $d$ but $R_m/C$ will yield a linear function of $d$ with a slope of $\frac{R_{\text{sh}}}{2\pi}$ and with $d = -2L_T$ when

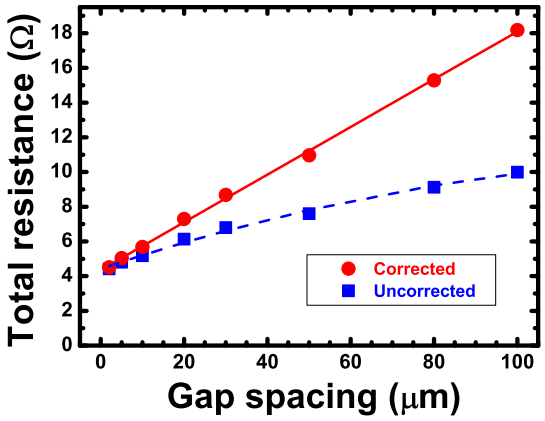


**Figure 4.7:** An example of the measured and corrected resistance values for a CTLM structure with the linear fit used to calculate the contact resistivity and sheet resistance. The example is a Ag/Sb (99%/1%) alloy on n-Ge CTLM structure with 50 $\mu$m radius annealed at 400 °C.

$R_m/C = 0$. The sheet resistance and transfer length can then be extracted from the linear fit to $R_m/C$. Figure 4.7 shows an example of measured resistance data as a function of gap spacing, the corrected data ($R_m/C$) and a linear fit to the corrected data. From the linear fit the values of $L_T$ and $R_{\mathrm{sh}}$ can be extracted, and the contact resistivity ($\rho_c$) can be calculated:

$$\rho_c = \mathrm{L}_T^2 \times \mathrm{R}_{\mathrm{sh}} \tag{4.23}$$

### Structural Characterization

Analysis of the physical structure of the contact is performed using scanning transmission electron microscopy (STEM) and atomic force microscopy (AFM). STEM work was performed with the help of Dr Ian McLaren of the physics department at the University of Glasgow.

For STEM thin cross sections of the contact are removed from the sample using a focused ion beam (FIB) lift-out process. Samples to be measured with a STEM must be less than 40 nm thick. They are then able to be placed into the STEM. In a STEM an electron beam is used to scan across the surface of the sample. High-angle annular dark-field (HAADF) images and dual electron energy loss spectroscopy are used to characterize the sample. HAADF images are constructed by collecting the electrons that have been scattered at high angles from the sample. The scattering is dependant on the atomic mass of the atoms. Dual electron energy loss spectroscopy gives information about the elemental composition of the sample at the beam location.

When a beam of electrons with a narrow range of energies is focused onto a small area of the sample, some of the electrons will interact with the sample and lose some energy. Each element creates a unique set of energy loss edges at known energies. The edges are named by the initial state of the atomic electron involved and is the minimum energy needed to remove an electron. If the first shell is involved the edge is K; for the second shell the edge is $L_i$, where $i$ is 1, 2 or 3 for the 2s, $2p^{1/2}$ and $2p^{3/2}$ orbitals respectively. M, N, and O are for shells 3, 4 and 5. For some initial orbitals the transition energy is too closely spaced to differentiate so the labels are combined. For example, for the $3d^{3/2}$ and $3d^{5/2}$ orbitals the edge is $M_{4,5}$. The energies, shapes, and relative intensities for most atoms are well known; for example, Ge $L_{2,3}$ (the $L_{2,3}$ of Germanium) is 1217 eV [115]. This information can be used to determine the composition of a given volume of the sample. The electron beam is moved along the surface of the cross section to create a map of the composition.

With AFM a height map of the surface of a sample can be made. The AFM tool uses an atomically sharp tip to precisely measure the height of the surface at a given point. As the tip scans across the surface the height of the tip is controlled in order to keep the force between the tip and the surface constant using a feedback mechanism. The applied force that is required to maintain the required height is the signal that is used to measure the height [116].

## 4.2 Silver Antimony Ohmic Contacts

Wafers with Ge/SiGe QCL designs and highly doped n-type top and bottom contacts have been investigated and showed no signs of the resonance tunnelling expected from the designs. The diffusion of dopants from the bottom contact through the active layer was believed to have contributed to the failure of the design, so designs with moderately doped bottom contacts were designed and fabricated. As the bottom contact layer was not highly doped enough to support NiGe Ohmic contacts another process was required. Since AgSb contacts have been shown to work in low Ge content SiGe the alloy was investigated for use with an n-type Ge contact layer.

### 4.2.1 Wafer for Contact Development

To develop and test AgSb contact processes with a moderately phosphorus doped Ge contact layer samples with a similar structure to a QCL but without the active layers

above the bottom contact were used. The n-Ge was epitaxially grown using an ASM Epsilon 2000E low pressure CVD tool on a $p^-$ Si(001) wafer [21]. The Ge layer was 2 $\mu$m thick and a phosphane precursor produced an *in-situ* P doping of $1 \times 10^{18}$ cm$^{-3}$. The Mott criteria for Ge:P is $2.5 \times 10^{17}$ cm$^{-3}$ [117], indicating that the sample is metallic with a doping level that is a factor of 4 above the metal-insulator transition.

### 4.2.2 Fabrication of Contacts

The wafer was first cleaved in to a number of 15 mm$^2$ chips. The chips for electrical measurements were prepared by first cleaning in acetone, followed by a rinse in IPA, and then blown dry in $N_2$. Circular transfer length method (CTLM) structures [112] as well as linear contact regions were then patterned in PMMA using a Vistec VB6 electron beam lithography tool to produce devices with a placement accuracy of $\sim$1 nm. The samples were developed using a 1:1 solution of (MIBK): (IPA) for 60 s followed by a rinse in IPA and then blown dry in $N_2$. The samples were then dipped in a 5:1 buffered HF solution to remove any native oxide before immediately being placed into a metal evaporator which is then pumped down to $< 1 \times 10^{-6}$ mbar, where 90 nm of a mixed Ag/Sb (99%/1%) alloy was deposited by thermal evaporation. The standard process for thermal evaporation had to be modified to ensure antimony deposition. In the standard process for thermal evaporation the sample shutter is closed while the metal warms up until a deposition rate of around 0.30 nm/s is obtained. Due to the differing melting points between Ag and Sb this process resulted little to no Sb deposited onto the sample. Instead the sample shutter was open during the metal warm up phase of the thermal evaporation resulting in sufficient Sb deposition. Following lift-off, the samples were annealed for 5 minutes in $N_2$ in a rapid thermal annealer at temperatures from 300-550 °C.

#### Low Temperature Measurement

In order to measure the resistance of the contacts at cryogenic temperatures samples were fabricated that consisted of two AgSb contacts wirebonded to a leadless chip carrier (LCC). The LCC was placed on the cold head of a cryostat. The devices were connected through the cryostat to an Agilent B1500A semiconductor device analyser. The cryostat chamber was placed under a vacuum of $< 1 \times 10^{-7}$ mbar and had a minimum temperature of 6.5 K. The IV characteristics of the contact were measured as a function of sample temperature; this is shown in Fig. 4.8. It is clear that the

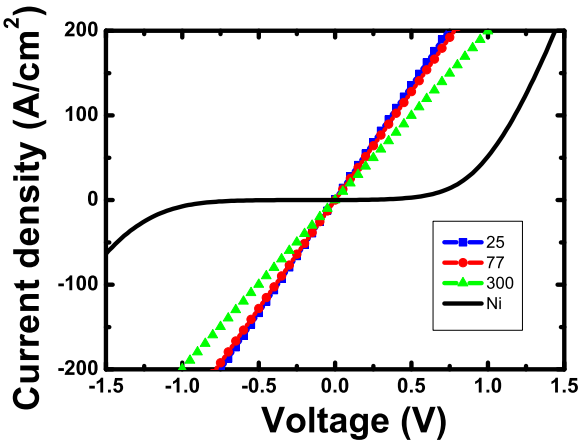


**Figure 4.8:** The current density versus voltage characteristics measured at different temperatures for a 90 nm AgSb alloy on n-Ge contact annealed at 400 °C for 5 min. For comparison the room temperature IV for the NiGe contact annealed at 340 °C is displayed (black line).

contact remains Ohmic down to the base temperature of the measurement cryostat of 6.5 K. There is noticeable improvement in the current conduction for the IVs at 6.5 K and 77 K compared to room temperature, which can be explained from an increase in conductivity for the as-grown n-Ge at lower temperatures [118]. The Ohmic behaviour at 77 K and below and the minimal temperature dependence is an indication that field emission is the dominant conduction mechanism at 300 K.

### CTLM Measurements

Each chip contained multiple CTLM structures with inner radii ranging from 50 to 100 $\mu$m, more than four times the transfer length [112] (around 7.5 $\mu$m), with gap spacings ranging from 2 $\mu$m to 100 $\mu$m, comparable in size to others[119], the outer contact was contained within an 800 $\mu$m $\times$ 800 $\mu$m square. The CTLM structures were characterised using a four connection (separate force and sense for voltage and current) DC configuration with a voltage sweep from -2 to 2 V using an Agilent B1500 semiconductor parameter analyser. When a contact is Ohmic the voltage sweep shows a linear relation between the voltage difference and the current applied. Contacts annealed at 350 °C and below showed non-Ohmic behaviour, contacts annealed at 400 and 450 °C showed Ohmic behaviour (Fig. 4.9), and contacts annealed at 500 °C and above where unable to be measured due to poor surface quality.

For each of the CTLM measurements from the Ohmic contacts the resistance was calculated by taking the slope of a linear fit to the current as a function of voltage. The specific contact resistivity was then calculated using equation 4.23. Table 4.1

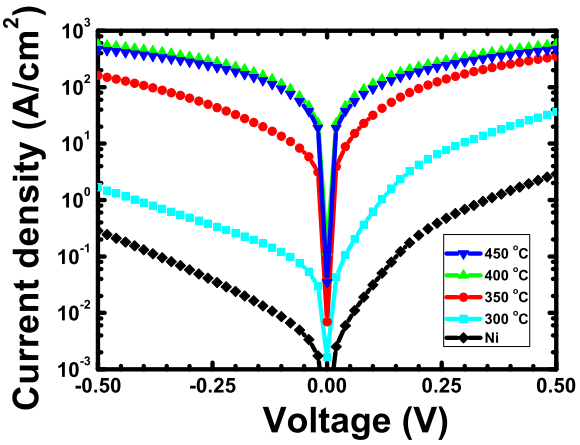


**Figure 4.9:** The semi-log current density versus voltage characteristics for a 90 nm 99% Ag / 1% Sb alloy on n-Ge annealed at 300-550 °C. The NiGe sample annealed at 340 °C is also shown (black line). The AgSb on n-Ge contacts annealed at 400 and 450 °C for 5 min are clearly Ohmic.

| Anneal (°C) | Contact | $\rho_c$ ($\Omega$-cm$^2$) |
|---|---|---|
| $\leq$350 | Schottky | - |
| 400 | Ohmic | $(1.1 \pm 0.2) \times 10^{-5}$ |
| 450 | Ohmic | $(1.7 \pm 0.3) \times 10^{-5}$ |
| $\geq$500 | Agglomerated | - |

**Table 4.1:** The contact type that arises for a AgSb alloy on moderately doped n-Ge annealed at different temperatures. The specific contact resistivity is included for the Ohmic contacts.

summarizes the results of the CTLM measurements.

### Structural Characterization

The agglomerated surfaces of the samples annealed at 500 and 550 °C were investigated using an AFM. From the height map of the surface of the contacts it can be seen that instead of the continuous surface the unannealed and lower anneal temperatures contacts had, the metal film is broken up with areas where there is no metal (Fig. 4.10). The 500 °C sample shows that mounds of metal have formed and the 550 °C sample shows much smaller and more numerous peaks of metal. These anneal temperatures are unable to provide good contacts for a device due to the poor surface morphology.

Linear contacts of AgSb annealed at 400 °C were fabricated to allow structural characterization of the contact. With the help of Dr Ian McLaren of the physics department at the University of Glasgow, cross sectional samples were prepared by the focused

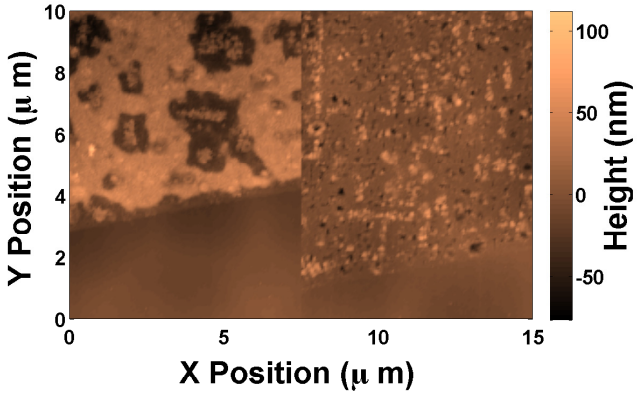


**Figure 4.10:** Surface roughness map of the AgSb on moderately doped n-Ge contact annealed at 500 °C (left) and 550 °C (right) measured with an atomic force microscope. The smooth surface in the bottom of the figure corresponds to an area of blank Ge.

ion beam (FIB) lift-out process using a FEI Nova Nanolab 200 Dualbeam FIB microscope. STEM characterisation was then performed on the resulting sections using a JEOL ARM200F microscope equipped with a cold field emission gun electron source and a Gatan GIF Quantum electron energy loss spectrometer. Characterisation was performed using electrons accelerated to 200 kV, with images recorded using the high-angle annular dark-field (HAADF) mode and dual electron energy loss spectrum (DualEELS) images recorded over an energy range up to 2100 eV covering the edges for Ag $M_{4,5}$, Sb $M_{4,5}$ and Ge $L_{2,3}$, as well as C K. Quantification was performed using a new convolution-based approach provided by Gatan Inc. (Pleasanton, USA) based on earlier work by Verbeeck *et al.*[120, 121] which fits the fine structure at the absorption edges based on the low loss spectrum and thus accounts for multiple scattering explicitly through the use of the whole DualEELS dataset.

The HAADF image of figure 4.11 shows a cross-section of a contact annealed at 400 °C for 5 minutes. The distribution of the Ag, Sb, and Ge are shown both separately and as a multicoloured overlay map. In both the image and the maps, it is clear that, unlike $Ni_xGe_y$ contacts [95], the AgSb forms a predominately flat contact on the surface, with just the occasional dip into the Ge. It is also observed that the Sb has diffused to a depth of ∼5 nm at a concentration of a few percent. This corresponds to a doping density of $\sim 5 \times 10^{19} \mathrm{cm}^{-3}$. This is significant enough to consider the Ge highly doped. The top surface of the contact is rougher. This is most likely due to the fact that the contact is polycrystalline with nanosized grains. The estimates from the DualEELS quantification suggest an approximate 75% Ag / 25% Sb composition, confirming that Sb is preferentially evaporated from the target, enriching it significantly in the film.

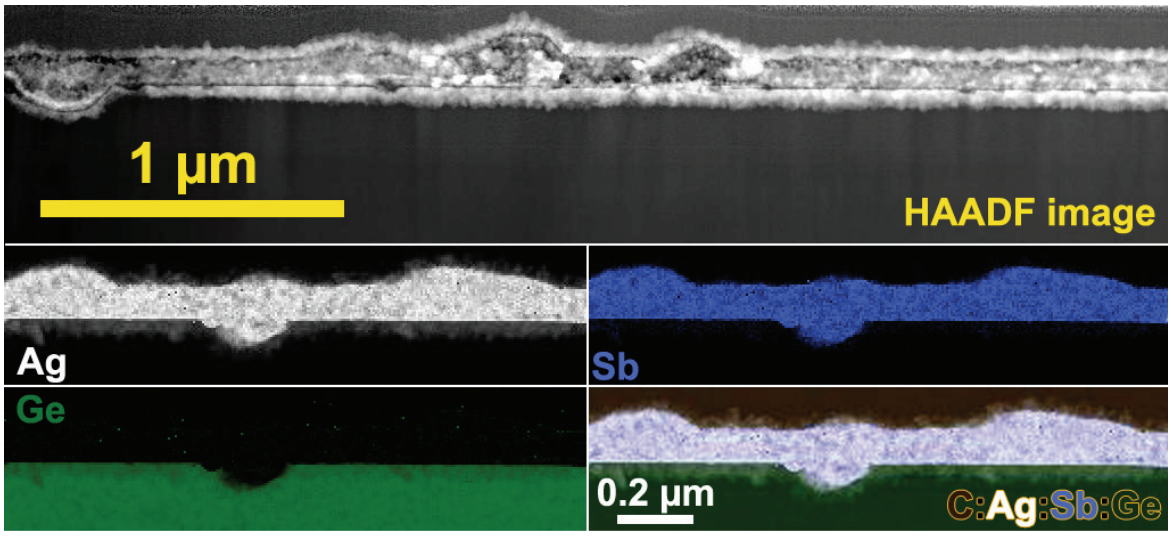


**Figure 4.11:** HAADF images of a AgSb on n-Ge contact annealed at 400 °C for 5 minutes.

## 4.3 Comparison with Literature

YbGe contacts to low doped n-type Ge ($N_D \approx 1 \times 10^{15}\text{cm}^{-3}$) have been demonstrated that produce a contact resistivity of $2.4 \times 10^{-5}$ $\Omega-\text{cm}^2$[104]. This technique requires Yb which is highly reactive with oxygen and therefore requires an additional protective layer.

Interfacial layers such as $TiO_2$ have been used to reduce the electron barrier height, but also introduce addition tunnelling resistance. Specific contact resistivies as low as $1.3 \times 10^{-6}$ $\Omega-\text{cm}^2$ have been demonstrated[101], but with highly doped n-type Ge ($N_D \approx 3 \times 10^{19}\text{cm}^{-3}$). ZnO has been used as well and has better specific contact resistivies, as low as $1.4 \times 10^{-7}$ $\Omega-\text{cm}^2$ [94] on n-type Ge ($N_D \approx 2.5 \times 10^{19}\text{cm}^{-3}$). The resistivity depends greatly on the thickness of the interfacial layers which adds to the difficulty of the method as compared to AgSb co-deposition.

Ion implantation can also be used to highly dope a contact layer, allowing Ohmic contact through conventional metal deposition and annealing techniques. Two disadvantages of ion implantation is the damage caused by the ions and the diffusion of the dopants during the required activation anneals. Laser annealing can be useful for high dopant activation [99] with low diffusion of dopants. Again this technique has addition complexities compared to the AgSb co-deposition process.

NiGe contacts annealed using a rapid thermal annealer on highly doped epitaxially grown n-Ge ($N_D > 1 \times 10^{19}\text{cm}^{-3}$) have shown specific contact resistivities as low as $2.3 \times 10^{-7}$ $\Omega-\text{cm}^2$. The requirement of highly doped epitaxial layers makes this

process incompatible with wafer designs requiring an Ohmic n-type bottom contact with intrinsic regions above.

## 4.4 Future Techniques

A fuller analysis of AgSb contacts to n-type Ge could be achieved by investigation into the minimum *in-situ* doping required for Ohmic contacts. All the contacts fabricated so far have been on n-type Ge with a doping density of $N_D = 1 \times 10^{18}$ cm$^{-3}$. Fabrication of AgSb contacts on a series of wafers with varied doping densities would allow determination of the effect of the *in-situ* dopant concentration on the contact resistivity.

Controlling the amount of Sb deposited proved challenging. The difficulty is due to the different melting points between Ag and Sb. The evaporation of a AgSb alloy results in preferential evaporation of the Sb which enriches the Ag content of the target during the evaporation. Initial processes resulted in no Sb being deposited on the sample because the small amount that was in the target was evaporated during the outgassing phase before the shutter was opened. Another issue is that the small amount of Sb being evaporated is less than can be measured via the crystal monitor used in the evaporation chamber. Improved results could be obtained by optimizing the ratio and thicknesses of Ag and Sb. Use of separate Ag and Sb targets could allow better control of the ratio to be deposited and allow optimization of the evaporation process.

While AgSb was able to produce Ohmic contacts the specific contact resistivity was relatively high. Substituting the Ag in the alloy with other metals could make use of Sb to increase the dopant concentration while forming lower resistivity contacts. To date NiGe contacts have been shown to produce one of the lowest specific contact resistivities, but only on highly doped layers which are incompatible with epitaxially grown active layers above due to dopant diffusion during growth. The process used for NiGe Ohmic contacts could be modified to include a co-deposition of Sb during the Ni deposition. A co-deposition of Ni and Sb followed by an anneal could potentially allow for an Ohmic contact to moderately doped n-Ge with extremely low contact resistivities. Finding the optimal anneal time and temperature would require experimentation. Dopant segregation during NiGe formation, known as the snowplough effect, could potentially increase the dopant concentration and lead to better contacts.

## 4.5 Summary

To reduce n-type dopant diffusion during epitaxial growth, n-type Ge Ohmic contact layers grown below nominally undoped active layers require lower doping concentrations than those required to produce low $\rho_c$ Ohmic contacts. The NiGe Ohmic contacts to n-type Ge requires a highly doped layer ($N_D > 1 \times 10^{19}$ cm$^{-3}$), otherwise a Schottky contact forms. Other processes that have been demonstrated require additional steps, adding to the complexity of the contact scheme. A process for the creation of Ohmic contacts to moderately doped n-type Ge ($N_D = 1 \times 10^{18}$ cm$^{-3}$), which requires only a AgSb alloy deposition and an anneal, has been demonstrated. A deposition of a AgSb alloy followed by a 400 °C anneal for 5 minutes can produce an Ohmic contact with a $\rho_c$ of $(1.1 \pm 0.2) \times 10^{-5}$ Ω-cm$^2$ on n-type Ge layers doped to a factor of four above the metal insulator transition. The contacts remained Ohmic down to 6.5 K, indicating that field emission is the main electrical conduction mechanism. As this contact process can produce Ohmic contacts to moderately doped n-type Ge they could prove useful for the fabrication of Ge photonic devices such as n-type Ge/SiGe THz QCLs.

The main work in this thesis is on quantum confined Stark effect (QCSE) devices made from Ge/SiGe MQW pin structures which use a p-type bottom contact, and n-type top contact both of which can be highly doped without significant dopant diffusion into the intrinsic region. Simple NiGe deposition allowed Ohmic contact to both the top and bottom contact layers for these devices. The following chapter will introduce the physics of QCSE with a focus on the SiGe material system and discuss results based on numerical simulations of QCSE designs.

# Chapter 5

# Simulation of Low Voltage QCSE Designs

## 5.1 Introduction

The quantum confined Stark effect (QCSE) is the effect on the absorption of light in a quantum well due to a change in electric field. The QCSE can be used in semiconductor devices to modulate the optical absorption using an applied voltage. As well as optical modulators as mentioned in the previous chapter, wavelength tunable photodetectors can be fabricated from MQW structures in which the detection edge is switchable by an applied voltage due to the QCSE [122]. This chapter will begin with an overview of the physics required to understand the QCSE with details focused on the Ge and SiGe material system. This will be followed by discussion and analysis of the results from numerical simulation of low voltage Ge/SiGe MQW QCSE designs.

## 5.2 Physics of QCSE

The QCSE is an effect that changes the absorption spectra of a QW as a function of the electric field across the QW. An understanding of the physics of QW confined wavefunctions is required to understand the QCSE. Designing these QW structures requires knowledge of the band structures of Ge and SiGe and how they are affected by strain. How to relate the wavefunctions and energy levels to the optical absorption is critical to understanding how the QCSE can be used to modulate the amplitude of

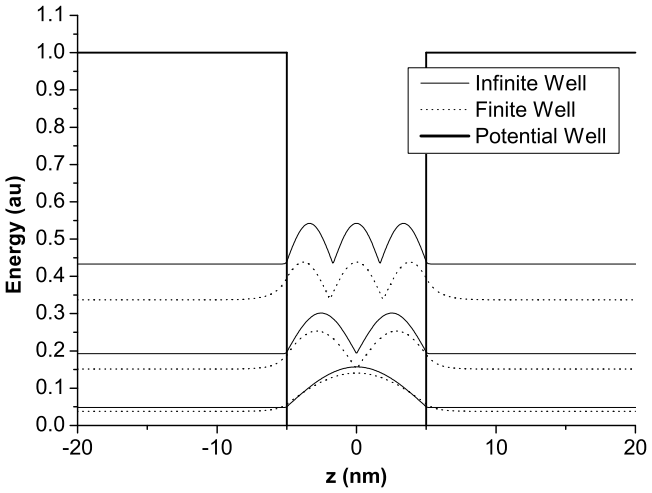


**Figure 5.1:** First three wavefunctions calculated for infinite and finite (1V deep) 10 nm quantum wells. In the infinite quantum well the wavefunctions are completely confined to the well, while in the more realistic finite quantum well the wavefunctions extend into the barriers. Due to the extended size of the finite wavefunctions the energy level is lower than the energy level of the infinite well wavefunctions. The difference between corresponding wavefunctions increases as the energy approaches the top of the barrier.

a light wave. This section will detail the physics of QWs, band structures, and optical absorption to provide the background knowledge required for QCSE device design and simulation.

### 5.2.1 Quantum Wells

A quantum well is a potential well with dimensions that are small enough to quantize the allowed energies of electrons within the well. The ideal well is known as a one-dimensional infinite square well (1DSW) and provides a good understanding of more complicated, realizable wells. The potential $V$ as a function of position $z$ for a 1DSW is:

$$V(z) = \begin{cases} \infty, & \text{if } z < 0 \\ 0, & \text{if } 0 < z < a \\ \infty, & \text{if } z > a \end{cases} \tag{5.1}$$

where $a$ is the width of the quantum well. This is a quantum well surrounded by barriers with an infinite height. To determine the allowed wavefunctions ($\psi(z,t)$) of an electron in the well the Schrödinger equation can be solved.

$$i\hbar\frac{\partial}{\partial t}\psi(z,t) = -\frac{\hbar^2}{2m}\frac{\partial^2}{\partial z^2}\psi(z,t) + V(z)\psi(z,t) \tag{5.2}$$

where $\hbar$ is the reduced Plank's constant and $m$ is the mass of the electron. Since there is no force on the electron in the well its wavefunction inside the well is the same as a free particle

$$\psi(z,t) = [A\sin(kz) + B\cos(kz)]\mathrm{e}^{-\mathrm{i}\omega t} \tag{5.3}$$

where $A$ and $B$ are arbitrary complex numbers, $k$ is the wavenumber and $\omega$ is the angular frequency. As the potential is infinite outside of the well the wavefunction must be equal to zero outside the boundaries. The wavefunction must not have discontinuities so the wavefunction must also be zero at the boundaries. Solving for the boundary conditions leaves the following for $\psi(z,t)$;

$$\psi(z,t) = \begin{cases} A\sin(kz)\mathrm{e}^{-\mathrm{i}\omega t}, & \text{in the well} \\ 0, & \text{outside the well} \end{cases} \tag{5.4}$$

where

$$k = \frac{n\pi}{a}, \text{where } n = \{1,2,3,4...\} \tag{5.5}$$

$k$ is quantized, it can only take on certain discrete values. The energy of the electron can be calculated from the dispersion equation:

$$E = \frac{\hbar^2 k^2}{2m} \tag{5.6}$$

Substituting in the discrete values for $k$ gives a set of discrete values for energy.

$$E = \frac{\hbar^2 n^2 \pi^2}{2ma^2} \tag{5.7}$$

These are the energy levels that are allowed within an infinite square well. Figure 5.1 shows a comparison of the wavefunctions and energy levels between a 10 nm 1DSW and a 10 nm quantum well with a finite barrier height. For holes in the valence band a well has a higher potential than the barriers. This is due to holes having a negative mass.

When the barrier height surrounding the quantum well is finite the wavefunctions will be non-zero in the barrier region. For non-ideal potentials the wavefunction and energy levels are calculated by solving the Schrödinger equation numerically.

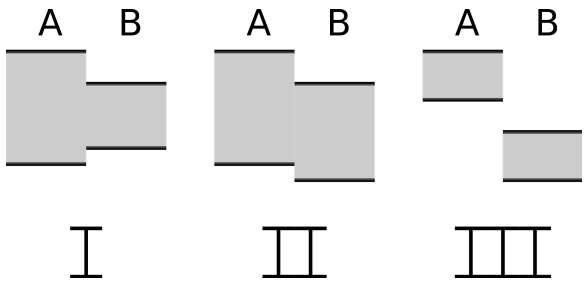


**Figure 5.2:** Types of band alignment between two materials A and B, type I straddling, type II staggered, and type III broken. With type I alignment, if material B has a smaller bandgap than A and is between two layers of A, there will be a quantum well in both the valence band and conduction band in material B

### 5.2.2 Heterojunctions

When different semiconductor materials are in contact there will be a discontinuity in the valence and conduction bands. This is known as a heterojunction. There are three different types heterojunctions based on the alignment of the bands (Fig. 5.2): straddling (type I), staggered (type II) and broken (type III).

When two materials have type I alignment, that allows the creation of quantum wells in the valence band and conduction band in the same location. If the wells are not in the same location the matrix element (overlap integral) between the valence and conduction band wavefunctions will be negligible.

### 5.2.3 Crystal Structure

The unit cell of a crystal structure is the smallest volume that when repeated in space forms the full crystal structure. Each atom in a Si, Ge, or SiGe alloy crystal requires four nearest neighbours to support the four covalent bonds required. These elements therefore form crystals with a cubic diamond structure (Fig. 5.3). The diamond structure is equivalent to two face centred cubic (FCC) lattices which are offset by 1/4 of the lattice constant. The crystal structure is highly symmetric being invariant under many different rotations, any permutation of the x, y, and z axes, and mirroring of the x, y, and z axes. The lattice constant is the length of an edge of the unit cell. For unstrained bulk crystals at room temperature the lattice constant of Si is 5.431 Å, Ge is 5.658 Å, and SiGe is function of the Ge content. A similar crystal structure known as zinc-blend is used by III-V materials such as GaAs. In a zinc-blend crystal each FCC sub-lattice is limited to a single element.

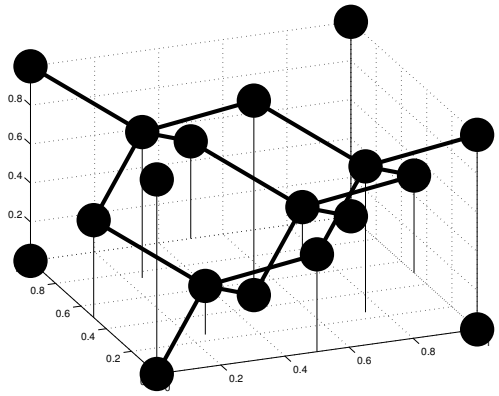


**Figure 5.3:** Unit cell showing the position of atoms in a diamond crystal, such as Si, Ge or SiGe crystals.

### 5.2.4 Band Structures

The periodic structure of a semiconductor crystal leads to a periodic Coulomb potential that is felt by electrons. The periodicity of the potential requires wavefunctions that are also periodic. The nearly free electron model is useful for calculating the theoretical band structure of a semiconductor. While free electrons are free from external forces, nearly free electrons are influenced by the crystal's periodicity and, due to Bragg reflections, there are energies in which they cannot exist, creating an energy gap.

A simple one dimensional model can be used to demonstrate the origin of the band gap. We shall consider an electron in a potential $V(x)$ which is periodic with a period $d$ such that $V(x+d) = V(x)$ such as;

$$V(x) = 2U\cos(gx) \tag{5.8}$$

where $g = 2\pi/d$. Solving the stationary Schrödinger equation

$$-\frac{\hbar^2}{2m}\frac{\partial}{\partial x^2}\Psi(x) + V(x)\Psi(x) = E\Psi(x) \tag{5.9}$$

In order to normalize the wavefunction, we consider a finite crystal of length $Nd$ and use periodic boundary conditions on the wavefuncion $\Psi(x) = \Psi(x+Nd)$. The wavefunction can then be expanded in a discrete Fourier series

$$\Psi(x) = \sum_q a_q \mathrm{e}^{\mathrm{i}qx} \tag{5.10}$$

where $q$ is an integer multiple of $2\pi/Nd$. The periodicity introduced by the finite crystal length can be eliminated by taking $N \to \infty$. Substituting equation 5.10 into

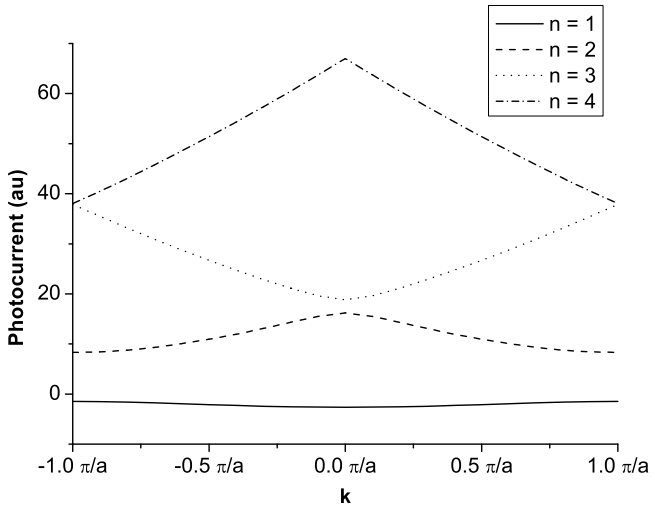


**Figure 5.4:** Calculated energy as a function of $k$ for a 1D crystal structure. The band gap is noticeable between bands 1 and 2, and 2 and 3, while the band gap between 3 and 4 exists but is barely noticeable on this plot. $U = 5$ eV , $d = 0.3$ nm, $l_{\max} = 5$. For $l_{\max}$ values greater than three there was no noticeable change in the energies calculated for the first four energy bands.

the stationary Schrödinger equation yields

$$\sum_q \left( \frac{\hbar^2 q^2}{2m} \mathrm{e}^{\mathrm{i}qx} + U\mathrm{e}^{\mathrm{i}(q+g)x} + U\mathrm{e}^{\mathrm{i}(q-g)x} \right) a_q = E \sum_q \mathrm{e}^{\mathrm{i}qx} a_q \tag{5.11}$$

For non-trivial solutions of this equation to be true for all $x$, terms with equal complex exponents must be equal

$$\frac{\hbar^2 q^2}{2m} a_q + U a_{q-g} + U a_{q+g} = E a_q \tag{5.12}$$

The $q$ values can be grouped into $N$ sets in which each $q$ value is separated by an integer multiple of $g$. Each set can be written as $q = k + lg$ where $l$ is an integer and $k$ is chosen to be the element in the set between $-\pi/d$ and $\pi/d$. This $k$ is known as the wavevector of the electron. Setting $a_q = a_{k+lg} = a_l^{(k)}$ we have

$$\frac{\hbar^2 (k+lg)^2}{2m} a_l^{(k)} + U a_{l-1}^{(k)} + U a_{l+1}^{(k)} = E a_l^{(k)} \tag{5.13}$$

which is an infinite set of equations for each $k$. It can be solved as a standard eigenvalue problem if it is assumed that $a_l^{(k)} = 0$ for $|l| > l_{\max}$. The solution to the eigenvalue problem will provide $(2l_{\max}+1)$ energies for each $k$ corresponding to a different energy band. When solved for each value of $k$ the energies form a smooth band (Fig. 5.4). For certain energies there are no solutions, forming energy gaps between the energy bands.

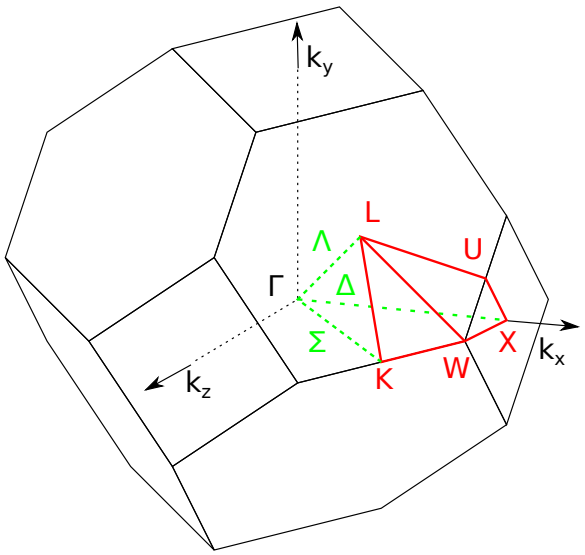


**Figure 5.5:** Brillouin zone is a face centre cubic structure for diamond crystal structures such as Ge, SiGe and Si. Energy minima points for the conduction band in Ge are Γand L points as well as on the Δ line.

Semiconductor materials are in reality three dimensional (3D) crystal structures. This requires 3D versions of the above equations to calculate the band energies. Furthermore, the $k$ values are now a 3D vector and, instead of being limited to a line segment, they are confined to a volume in reciprocal space known as the Brillouin zone. Each point in the volume of the Brillouin zone (Fig. 5.5) represents a $k$ value which has a corresponding energy for each band. In order to visualize the data, the energies along certain lines through the Brillouin zone which connect points of high symmetry are plotted. A common way of representing the data is to plot the energies as a function of position along a line that is composed of the line segment from the L point to the Γ point and from the Γ point to the X point.

When a semiconductor film is grown on a substrate with larger (smaller) lattice constant below the critical thickness, the film becomes strained and the crystal structure will be compressed (expanded) in the plane parallel to the interface and expanded (compressed) normal to the interface. As the strain changes the periodicity of the crystal lattice it will also change the energy of the bands. Strain will also lower the symmetry of the crystal which can cause bands that are degenerate in an unstrained crystal to split in energy.

### 5.2.5 Strain Effects

Diamond cubic semiconductor crystals such as unstrained Si, Ge, or SiGe are highly symmetrical. The symmetry in the crystal structure leads to symmetry in the energy bands in the Brillouin zone. The symmetry results in multiple bands with the same energy. The number of bands depends on the degree of symmetry. A crystal that is expanded or contracted uniformly in all directions is hydrostatically strained. For cubic crystal semiconductors hydrostatic strain will not break the symmetries and therefore will not lift the band degeneracies. If compressive hydrostatic strain is applied to a cubic crystal the unit cell will shrink but the shape will still be cubic (Fig. 5.6a). As the crystal lattice shrinks the periodicity of the crystal will decrease which will increase the separation between the energy bands. If tensile hydrostatic strain is applied the distance between the atoms is increased and the separation between the energy bands will decrease.

A general strain induced into crystal structures is a combination of hydrostatic and shear strain. When shear strain is applied to a crystal structure the shape of the crystal is deformed. Shear strain can be biaxial, in a plane, or uniaxial, along a line. For a cubic crystal structure under biaxial strain in the $xy$ plane the cell edge along the $z$-axis will shorten or lengthen relative to the $x$ and $y$ edges. This will change the shape of the unit cell of the crystal reducing the degree of symmetry in the structure (Fig. 5.6b). The conduction band energies which were previously degenerate due to the symmetry of the system may no longer be degenerate. This will cause a splitting of the energy bands in the semiconductor. Biaxial strain will split the six fold degenerate conduction band minimum at the $\Delta$ valley in Si into two groups with two and four fold degeneracy known as the $\Delta_2$ and $\Delta_4$ valleys respectively. In Ge the biaxial strain will not split the conduction band minimum which is the four fold degenerate $L$ valley since the strain affects each of them identically. From figure 5.5 it can be clearly seen that despite a reduction in symmetry a compression or expansion in the xy plane will affect all the L points in identical ways. In the valence band the heavy hole and light hole valleys are both at the $\Gamma$ point which is a single point unlike the $\Delta$ and L points which are multiple points in reciprocal space. While the HH and LH valleys are degenerate in energy they are from separate bands which are affected to different degrees by the change in crystal shape. Uniaxial strain can also be applied to a crystal; if it is along one of the primary axes the effect will be the same as with biaxial strain. An example of uniaxial strain would be compression along the [110] axis. This deforms the unit cell such that the top and bottom faces are no longer rectangular and they become rhombic. In this case the effect will not be identical at the L points. The L point valleys will be split into two doubly degenerate pairs [123]. The uniaxial strain

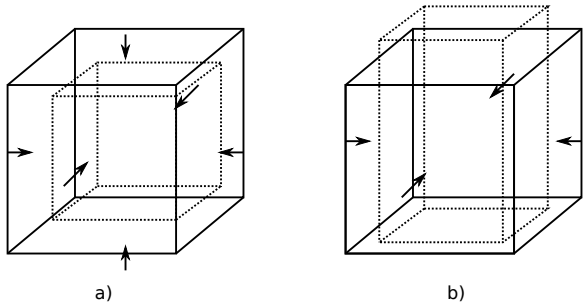


**Figure 5.6:** Diagram of the unit cell of a crystal showing the effects on its shape of a) hydrostatic strain, and b) biaxial strain.

will also cause splitting of the $\Delta$ valleys and between the HH and LH valleys. The minimum $\Gamma$ valley in the conduction band consists of a single band. Since there is no degeneracy due to symmetry, because there is only one $\Gamma$ point, there will be no splitting of the conduction band $\Gamma$ valley.

### 5.2.6 Ge and SiGe Band Structure

The band structure of Ge has three conduction band minima, the $\Gamma$ point, the L point, and along the $\Delta$ line near the X point (Fig. 5.7). SiGe alloys have the minima at the same three points but at different energies which depend on the Ge fraction. The valence band maxima is at the $\Gamma$ point and contains two bands that are degenerate in energy at the $\Gamma$ point but with different curvatures called the heavy (HH) and light hole (LH) bands. In unstrained pure Ge the band gap is 0.66 eV between conduction band minimum at the L point and the valence band maximum. The direct band energy gap is 0.80 eV. In a SiGe alloy, if the Ge fraction is below about 0.85 then the material is Si like with the conduction band minimum along the $\Delta$ line near the X point. As Ge content decreases the direct band gap increases as the valence bands decrease and the $\Gamma$ point conduction increase in energy. SiGe and Ge heterojunctions therefore have a type I alignment at the $\Gamma$ point allowing electron and hole QWs to be coincident in space.

### 5.2.7 Band Structure Engineering

By controlling the Ge fraction of SiGe during the growth of a wafer different heterostructures can be realized. The strain in the different layers can also be used to engineer the properties of the layers and heterostructure. The problem of energy bands in semiconductors is simplified by looking only at a few local extrema near the bandgap

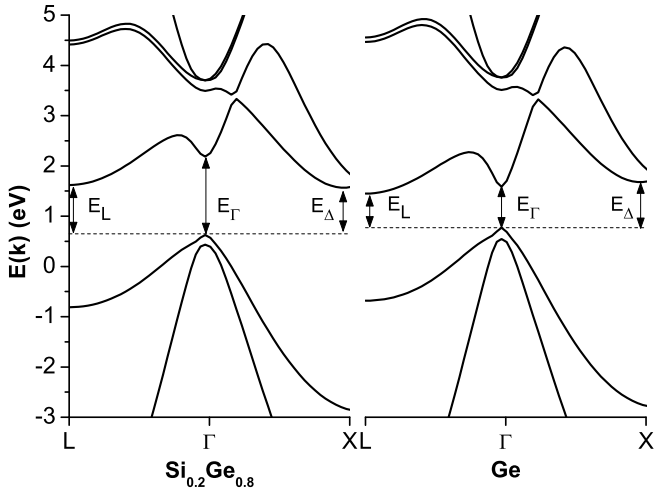


**Figure 5.7:** Band structure for bulk (unstrained) SiGe and Ge as calculated using nanohub's Band Structure Tool [1]. An increase in Si content increases the energy of the conduction band minimum at the Γ point and decreases the valence band maximum leading to type I alignment between Ge and SiGe.

and utilizing an effective mass for the electron or hole. The energy at the extrema are used to define the band edges used to calculate wavefunctions. The effective mass which replaces the electron mass in the calculations is a function of the curvature of the band at the extrema. For the light hole and heavy hole the differences in effective mass leads to differences in energy levels as shown by substituting effective mass for mass into equation 5.7. Strain in the semiconductor will also lift the degeneracy in the energies of the light and heavy hole maxima.

### Calculated Band Structure Values

The band valley extrema have been calculated as a function of Ge content and parallel lattice constant using nextnano software. The calculation used a thin $Si_{1-y}Ge_y$ film which was fully strained to a substrate with a lattice constant equal to a fully relaxed bulk $Si_{1-x}Ge_x$. The band edges were calculated as the Ge content in both the substrate, $x$, and the film, $y$, was varied from 0 to 1 by steps of 0.05. Figure 5.8 shows the calculated direct band gap and valence band splitting as a function of Ge content of the film and substrate. The diagonal of the plots corresponds to unstrained values while for the top left and bottom right halves the film is under compressive and tensile strain respectively. Since relaxation would be detrimental to the quality of the active layers, all layers grown above a virtual substrate will be fully strained to have parallel lattice constants equal to that of the virtual substrate. Therefore a heterostructure design can only make use of the band edges which are calculated for the same parallel lattice value.

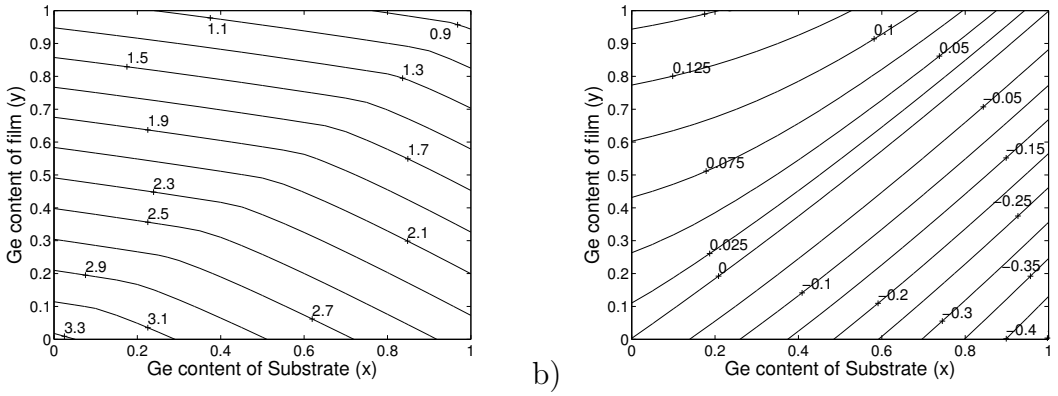


**Figure 5.8:** Contour plot of the calculated effect on the band structure of biaxial strain for $Si_{1-y}Ge_y$ alloys. The $Si_{1-y}Ge_y$ alloys are fully strained on a fully relaxed $Si_{1-x}Ge_x$ substrate. a) shows the direct band gap between the Γ valley in the conduction band and the maximum of the valence band. b) shows the difference in energy between the heavy hole (HH) valley and the light hole (LH) valley. Positive values correspond to HH being higher than LH in energy. For compressive biaxial strain the LH band edge is higher in energy than the HH band edge while for tensile strain the HH is higher in energy than the LH.

### 5.2.8 Optical Absorption

When a photon is absorbed by a material, the energy of the photon is transferred to an electron in the material [124]. In a quantum well the discretization of electron energies means that only photons with specific energies can be absorbed. When a photon is absorbed in a quantum well an electron is moved from the valence band to the conduction band, effectively creating a hole state in the valence band and an electron state in the conduction band. The difference in energy between the hole state and the electron state must be equal to the photon energy. In a quantum well an exciton can also be created which is a particle that is composed of an electron and hole bound to each other [125]. The creation of the exciton requires less energy than moving an electron from the valence band to the conduction band and therefore allows for the absorption of light with slightly less energy than without excitons.

### 5.2.9 Quantum Confined Stark Effect

When a potential is applied across a quantum well an electric field is created perpendicular to the wells and the band edges are angled due to the potential (Fig. 5.9). While the centre of the quantum wells remain the same distance apart the minimum of the conduction band and maximum of the valence band move closer together in energy. This change in the quantum well will naturally change the energy and wavefunction of the confined states. Hole states will be shifted up in energy and electron

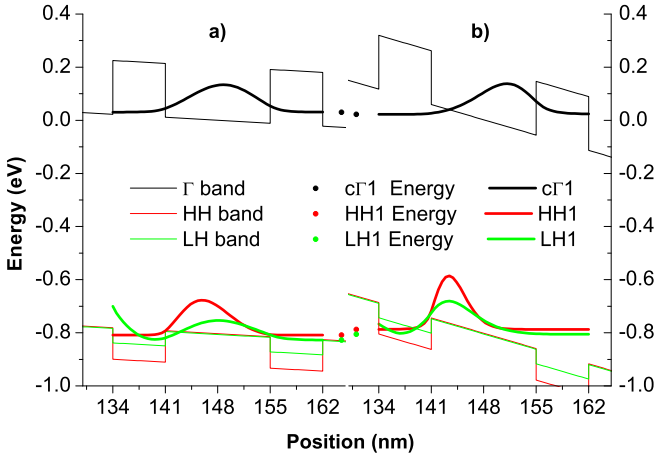


**Figure 5.9:** The calculated wavefunctions and energy levels confined to a 14 nm Ge quantum well between 7 nm $Si_{0.05}Ge_{0.95}$ barriers in a 10 quantum well device. a) at zero applied bias, electric field is due to built-in voltage, and b) with an additional applied bias of 1 V. Conduction and valence band wavefunctions shift closer together in energy while moving further apart in space.

states will be shifted down in energy. The transition between the two states requires less energy and therefore light of a longer wavelength can be absorbed. As well as shifting in energy, the shape of the wavefunction also changes due to the change in the QW shape. The peak amplitude of the wavefunctions will shift in opposite directions, lowering the overlap between the first energy state in the two bands. The decrease in overlap will decrease the absorption efficiency of the transition. These two processes are known as the quantum confined Stark effect (QCSE). While the overlap between the first confined wavefunctions decreases, the overlap between wavefunctions that normally have minimal overlap as enumerated by selection rules will increase. Simulation software is utilized to accurately account for all of these effects on the optical absorption spectrum.

## 5.3 Simulation of QCSE

In order to calculate the absorption spectra for a QCSE device design, the structure is simulated. Specialized semiconductor simulation software called *nextnano* [126] is used to calculate the wavefunctions and energy levels within the quantum wells, as well as the absorption spectrum.

### 5.3.1 Numerical Simulation

The *nextnano* software simulation is controlled through use of input files in which the material geometry is defined and the simulation program flow is controlled. Many options are available allowing many different semiconductor devices to be simulated. For the simulation of a QCSE device the following process flow is used. An in-plane lattice constant for the virtual substrate is chosen and the heterostructure is strained to match. From the strain in the structure the approximate band-edges are calculated and used as a starting point for the next step. A self-consistant Poisson-Schrödinger equation is solved for the strained structure using an 8 band $k.p$ Hamiltonian to determine the wavefunctions and band-edges. Finally, the absorption spectrum is calculated from a 961 k-point discretization of the Brillouin zone. The software then outputs the absorption spectrum for a given polarization of light, band edges, and electron and hole wavefunctions and energies. When the simulation is repeated for the same structure using different applied electric fields the effect of the QCSE can be seen in the change in absorption spectrum, band edges, and wavefunctions.

### 5.3.2 Simulation of QCSE Structures

QCSE structures were simulated using *nextnano* in order to determine the expected absorption spectrum of devices fabricated from wafers with the structure. The time required for a simulation is proportional to the square of the number of grid points used to describe the structure to be used in the calculation. To maintain sufficient accuracy the number of grid points per quantum well or barrier is fixed. To simulate a full 10 QWs and 11 barrier device, the simulation time will be $(21/3)^2 \approx 49$ times that required to simulate a single QW between two barriers. As a single simulation for a single bias voltage of one QW and two barriers requires approximately 8 hours of processing time on a modern computer a full simulation was impractical. While the wavefunctions are not completely confined to a single quantum well the extent of the wavefunction will not be significant beyond the nearest neighbour quantum wells. Therefore accurate results should be obtained using a three (or less) QW simulation.

#### Simulation Parameters

In order to accurately simulate the QCSE structures accurate values for the physical properties of the material are required. The *nextnano* software contains a large

database of parameter values for many different materials. The parameters define the physical properties of the material used for calculations performed during the simulation. The default values contained can be modified by the user and some of the physical properties were modified for this work. The input parameters used for the simulation in this work were obtained from published sources and where possible are values that have been experimentally derived or measured directly [127].

For each simulation it is assumed that the epitaxially layers are fully strained to match the in-plane lattice of an underlying substrate layer. For QCSE wafers grown on virtual substrates the lattice constant of the virtual substrate is used. This is calculated from the Ge content $x$ and the residual strain $\epsilon$ expected or measured for the virtual substrate. The in-plane lattice constant $a$ for SiGe is calculated using

$$a = (0.5431 + 0.01992x + 0.002733x^2)(1 + \epsilon) \tag{5.14}$$

where a positive $\epsilon$ corresponds to tensile strain in the layer. The lattice constant can be modified by changing either the strain or the Ge content or both.

#### Effect of Virtual Substrate Strain

The in-plane lattice constant of the virtual substrate will determine the strain in the MQW region. The in-plane lattice constant is a function of the alloy concentration and the strain in the virtual substrate. An increase in tensile strain will increase the in-plane lattice constant and shift the absorption peak to higher wavelengths. It will affect the light hole (LH) transitions to a higher degree than heavy hole (HH) transitions (Fig. 5.10). This is due to the LH band edge having a larger shift in energy with strain then the HH band edge. The in-plane lattice size can also be increased by increasing the Ge concentration in the virtual substrate.

### 5.3.3 Simulation of Edwards Device

In order to confirm the accuracy of the simulation a design from Edwards *et al.* [2] was simulated using the *nextnano* software. The published paper had experimental absorption spectra for the QCSE design as well as a TEM measurement of the structure. The structure to be simulated was the QCSE structure which was taken from the TEM measurements.

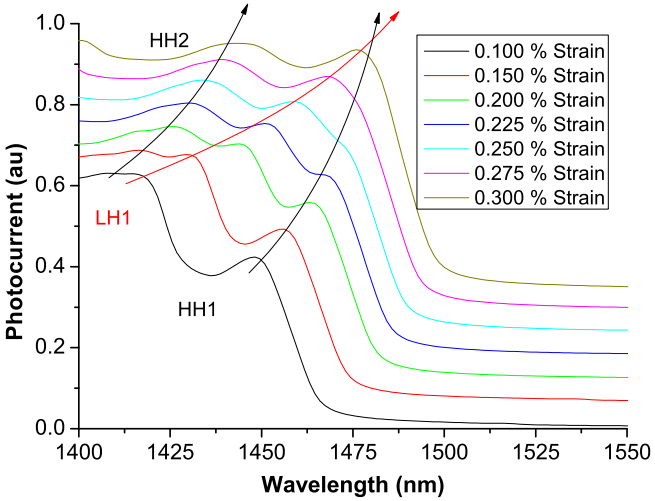


**Figure 5.10:** An example of the change in spectrum as tensile strain in virtual substrate is increased. Transitions shift to higher wavelengths (lower energies) with the light hole (LH) transition changing more than the heavy hole (HH).

The structure was simulated using a single QW simulation region and the calculated spectra was compared to the spectra in the Edwards paper. While the simulated absorption edge for low applied voltages matches the measured spectrum quite accurately, as the voltage is increased the simulated spectra shifts further than the measured spectra (Fig. 5.11). The accuracy of the low voltage absorption edge is evidence of the accuracy of the physical parameters chosen for Ge and Si used in the simulation. The difference in peak shift as a function of voltage can be explained by the details of how the potential drop across the QWs is calculated for the simulation. The potential drop is calculated by adding the applied voltage directly to built in voltage and dividing by the size of the intrinsic region. Any resistance in the contacts is not taken into account, leading to a larger QCSE shift in the simulation than would be measured. Due to the limited precision of the measurements there will also be a difference between the reported widths of the layers measured using the TEM and the true widths. This will lead to slight changes in the spectra and QCSE between simulation and measurement.

The comparison between the spectra measured by Edwards *et al.* and the simulations performed shows that the simulated absorption spectra are sufficiently accurate to allow the design of SiGe/Ge MQW QCSE modulators. The material and calculation parameters used in this simulation were kept constant for subsequent simulations. The changes made for different simulations was limited to the applied voltage and number of QWs and barriers in the simulation region, and parameters that are determined by design and growth such as the alloy concentrations, virtual substrate strain, and well and barrier thicknesses.

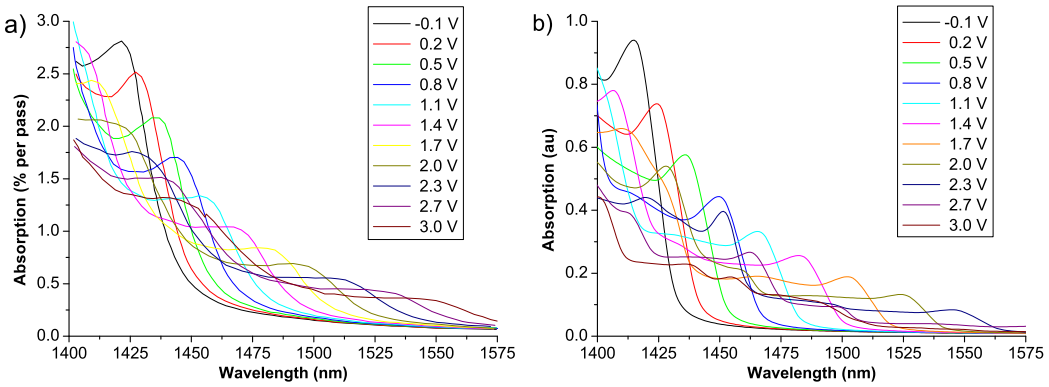


**Figure 5.11:** Absorption spectra for QCSE devices in the Edwards paper. a) Measurement spectra replotted from Edwards [2]. b) 1 QW simulation spectra using TEM measured structure from Edwards.

### 5.3.4 Simulation of Designs

The energy efficiency of a QCSE modulator can be improved by lowering the voltage swing required to switch the modulator on and off. A low voltage SiGe/Ge MQW QCSE device has been designed which should improve on the efficiency of QCSE modulators. The lower voltage requirement is achieved by decreasing the width of the barriers between the quantum wells. With thin barriers a higher fraction of the potential drop across the device will be across a quantum well and therefore contribute to shifting the absorption peak. The designs are based on the SiGe/Ge MQW system where the wells are pure Ge and the barriers are $Si_{0.15}Ge_{0.85}$. The designed structure uses a virtual substrate of $Si_{0.05}Ge_{0.95}$ which is assumed to be tensile strained at 0.18% due to full relaxation at growth temperature followed by tensile strain due to thermal expansion. This results in an in-plane lattice equivalent to the bulk lattice of $Si_{0.01}Ge_{0.99}$. Each of the active layers above are grown below their critical thickness and are of the same average Ge content as the virtual substrate for strain balancing. As such they will be fully strained to the virtual substrate. The Ge wells will be slightly compressively strained while the barriers will be tensile strained.

The design is a pin structure with the MQW within the central intrinsic region with highly doped p-type layer below and n-type layer above. The intrinsic MQW region comprises 11 barriers and 10 QWs. The barrier and well thickness for the MQW region are shown in table 5.1. For each design the barrier width is half the thickness of the QW. This means that 66 percent of the potential drop across the MQW region is across the QWs. The design also incorporates intrinsic spacer layers to prevent dopant diffusion into the MQW region. Since the spacers, like the MQW region, are intrinsic, part of the potential drop will be across the spacers.

**Table 5.1:** Well and Barrier widths of QCSE as designed.

| Wafer | QW Design | Barrier Design |
|---|---|---|
| 13-307 | 9 nm | 4.5 nm |
| 13-308 | 12 nm | 6 nm |
| 13-309 | 14 nm | 7 nm |
| 13-310 | 16 nm | 8 nm |

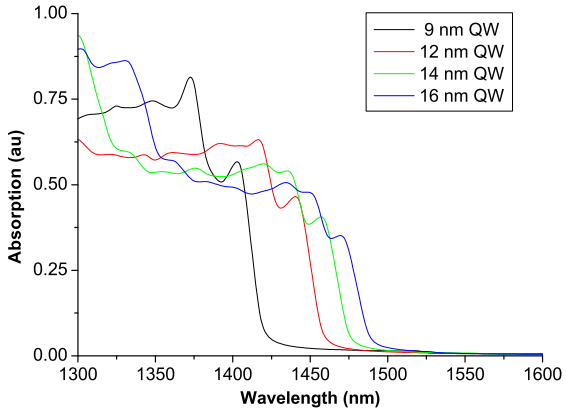


**Figure 5.12:** Calculated absorption spectra for MQW QCSE SiGe/Ge structures as designed, using a simulation of a single quantum well at an applied bias of 0 V .

Simulations of the designed QCSE structures was performed focusing on a single quantum well within the device. The pin structure creates a built-in voltage of ∼0.756 V across the intrinsic region of the device. The applied voltage to be simulated is added to the built-in voltage before the electric field is calculated. The electric field is calculated assuming a linear potential drop across the intrinsic region. As the QW width is increased the wavelength of the absorption peak shifts to higher wavelengths (Fig. 5.12). As the calculation of the absorption spectrum of a single QW is relatively quick it can be easily calculated for multiple bias voltages to see how the QCSE affects the absorption. The absorption spectrum for a few applied voltages for one of the designs (14 nm QWs) is also calculated for a three QW simulation to confirm that a single QW simulation is sufficient to understand the physics. Any perturbation from the single QW calculation due to wavefunctions extending into neighbouring wells is seen to be small and will not qualitatively change the understanding (Fig. 5.20).

The shift in the wavefunctions position and energy due to the changing electric field can be seen from the simulations (Fig. 5.13). Due to the difference in the overall size of the intrinsic region for the designs with wider QWs a given applied voltage will result in a lower electric field across the wider QWs. As a function of electric field the QCSE will cause a smaller shift in thin QW than in wide QWs. Which of these two effects will be dominant depends on the thicknesses of the intrinsic layers. With the current designs the wider QW designs show a faster shift in energy with change in applied

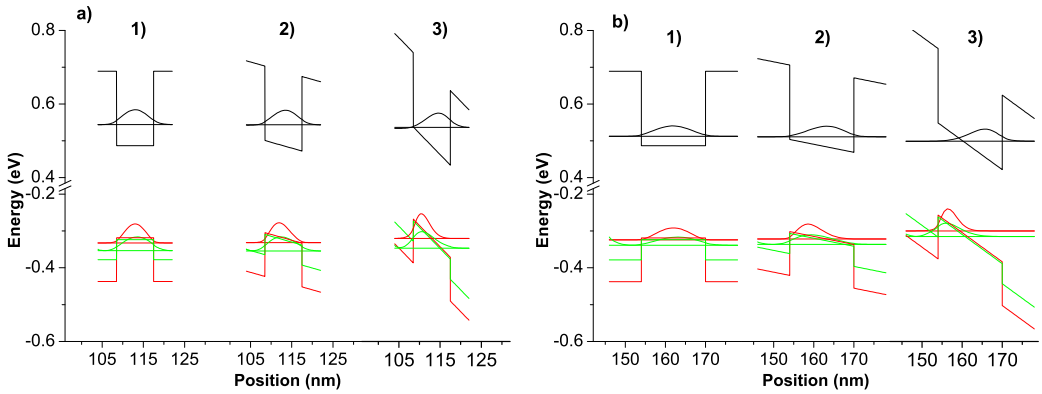


**Figure 5.13:** Wavefunctions for a) 9 nm QW and b) 16 nm QW designs shown at 1) flat band, 2) built-in voltage and 3) with 2 V applied bias. As can be seen from the slope of the band edges, designs with thinner QW and barriers have a higher electric field for the same voltage across device. Despite having a smaller electric field the larger devices have a larger energy shift and less overlap between the hole wavefunctions and the electron wavefunctions.

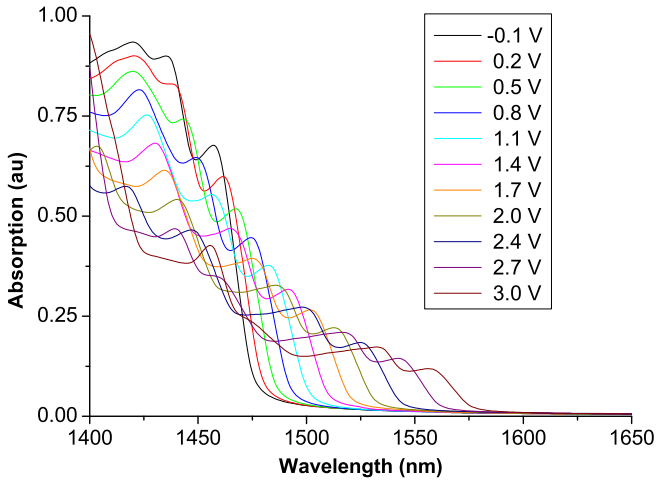


**Figure 5.14:** Calculated absorption spectra for 14 nm QW MQW QCSE SiGe/Ge structures as designed with multiple applied biases using a simulation of a single quantum well region.

bias than the thinner QWs. As the electric field is increased the barrier between the QW and the continuum decreases lowering the confinement. At high enough electric fields the wavefunctions are no longer well confined to the QW.

While the calculation of the wavefunctions of the structures at the Γ point allows for a qualitative understanding of the change in optical absorption, a more detailed calculation is used to determine the full absorption spectrum. The absorption spectra are calculated using a 961 point discretization of the Brillouin zone near the Γ point to include absorption by electrons with non-zero $k$ values. A separate spectrum is calculated for each applied bias which shows the QCSE in action (Fig. 5.14). As the applied bias increases the low energy absorption peak will shift to lower energies since the HH1 to Γ1 transition energy is decreasing. The total absorption from the HH1-

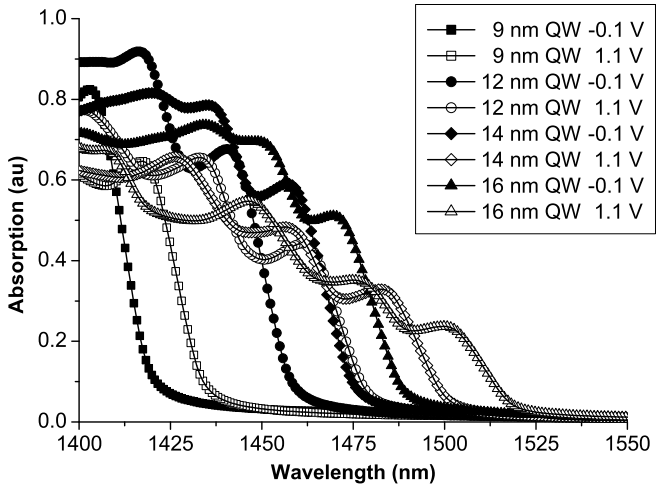


**Figure 5.15:** Calculated absorption spectra for QW MQW QCSE SiGe/Ge structures as designed at -0.1 V and 1.1 V (1.2 V swing) applied, using a simulation of a single quantum well region. The shift in absorption wavelength increases for larger QW structures.

Γ1 transition will decrease since the overlap between the two wavefunctions decreases with applied voltage.

Despite a lower electric field for a given applied bias the QCSE is more pronounced for the larger QW structures (Fig. 5.15). The calculated absorption peak shifts for the 9 nm, 12 nm, 14 nm, and 16 nm QW designs are 15 nm, 23 nm, 28 nm, and 32 nm respectively. The relative height of the peak between -0.1 V and 1.1 V also decreases as the QW width is increased. The absorption contrast ratio as a function of wavelength for the above calculated absorption spectra is shown in figure 5.16. Despite the differences in the absorption shift due to QW and intrinsic region thickness, the contrast ratios for the different are quite similar in shape and height. Simulations show that these designs can provide good absorption contrast with low voltage swing. The 16 nm QW design shows that full coverage of the C wavelength band (1535 nm to 1565 nm) with a contrast ratio $> 3$ dB is possible with a swing voltage of only 0.3 V and DC offset $< 3$ V (Fig. 5.17). Devices with 12 nm or slightly smaller QW designs could cover the L wavelength band (1460 nm to 1530 nm) with a contrast ratio $> 3$ dB with a swing voltage of only 0.3 V and DC offset $< 3$ V (Fig. 5.18).

### 5.3.5 Simulation of Grown Structures

The designs above were sent to be grown by collaborators at Warwick University using a reduced pressure CVD tool. After growth the wafers were examined at Warwick University using transmission electron microscopy (TEM) and measurements for the

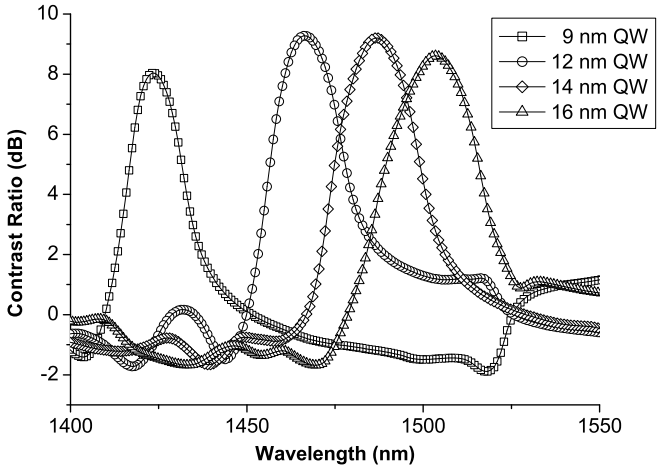


**Figure 5.16:** Contrast ratio as a function of wavelength calculated from the simulated absorption spectra for QW MQW QCSE SiGe/Ge structures as designed at -0.1 V and 1.1 V (1.2 V swing) applied using a simulation of a single quantum well region. The shift in absorption wavelength increases for larger QW structures.

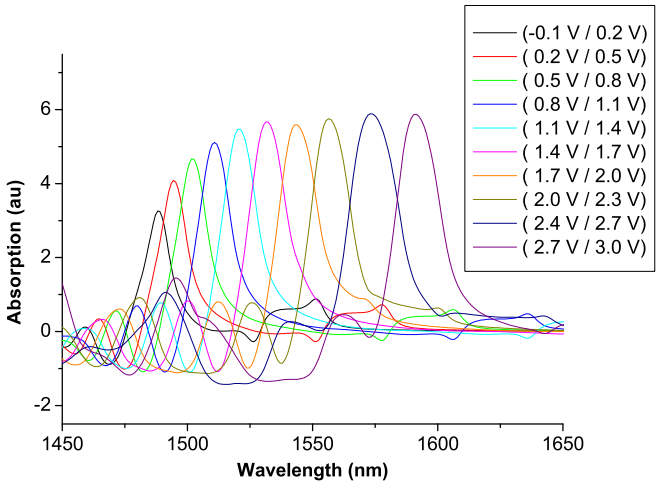


**Figure 5.17:** Calculated contrast ratio from the absorption spectra for 16 nm QW MQW QCSE SiGe/Ge structures as designed with 0.3 V swing voltage with DC offset from -0.1 V to 2.7V a using a simulation of a single quantum well region.

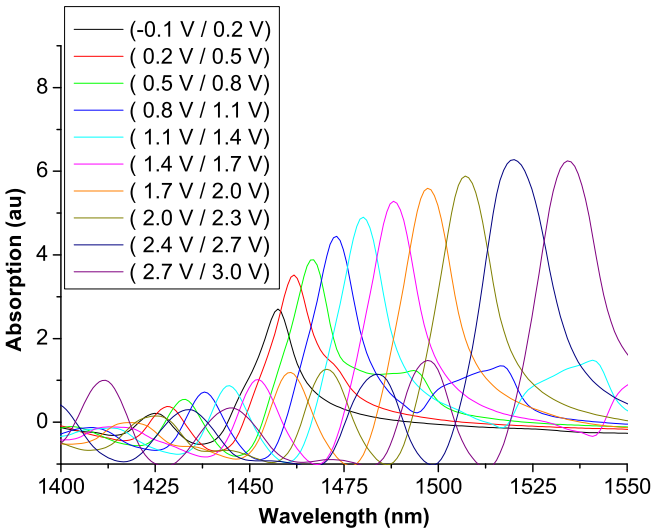


**Figure 5.18:** Calculated contrast ratio from the absorption spectra for 12 nm QW MQW QCSE SiGe/Ge structures as designed with 0.3 V swing voltage with DC offset from -0.1 V to 2.7V a using a simulation of a single quantum well region.

as grown structure were taken. The devices fabricated from the wafers grown at Warwick University will be examined in more detail in the following chapter. Results from the simulation of the as grown structures as measured by TEM will be discuss here.

The differences between the design structure and the as grown wafers are as follows. The virtual substrate had a slightly higher Ge content at $Si_{0.04}Ge_{0.96}$ still with 0.18% strain, the barriers had a lower Ge content at $Si_{0.18}Ge_{0.82}$, and the well and barrier widths were different. The lower Ge content in the barriers should increase the barrier height which would increase the confinement, while the virtual substrate is now of the same in-plane lattice constant as bulk Ge, meaning the wells should be fully relaxed, and the barriers strained higher than in the design. The QW thicknesses of the structures as grown are smaller than designed and the barriers are thicker. The absorption edge will be shifted to lower wavelengths due to the thinner QWs and the electric field across the intrinsic region will be smaller for a given applied bias due to the MQW region being wider overall.

**Table 5.2:** Well and barrier widths of the QCSE wafers from measurements made by collaborators at Warwick University.

| Wafer | QW Measured | Barrier Measured |
|---|---|---|
| 13-307 | 6.6±0.9 nm | 8.2 nm±0.7 nm |
| 13-308 | 9.7±0.7 nm | 10.3 nm±0.2 nm |
| 13-309 | 11.3±0.3 nm | 11.5 nm±0.6 nm |
| 13-310 | 13.6±0.3 nm | 12.5 nm±0.4 nm |

Simulations using the measured wafer structure were performed, again focusing on

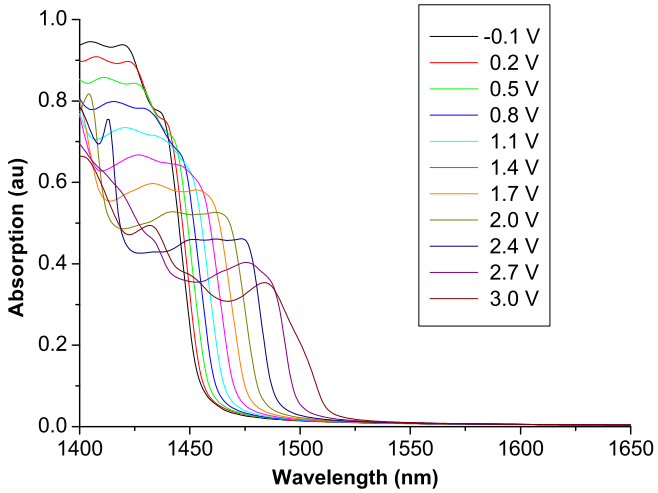


**Figure 5.19:** Calculated absorption spectra for 11.3 nm QW structure from a single QW simulation. Shift in absorption peak position and decrease in height from increase in applied bias shows the QCSE.

a single QW to calculate the absorption spectra for the structures as a function of applied bias. The absorption spectra for the 11.3 nm QW structure for multiple biases is shown in figure 5.19. The spectra for one of the structures (13.6 nm QW) was also calculated using a 3 QW region simulation for a few applied biases to determine the effect of a neighbouring QW on the wavefunctions. A comparison between the absorption spectra of a single QW simulation and that of a three QW simulation is shown in figure 5.20. The single and three QW absorption spectra of the 14 nm design structure and the 13.6 nm as grown structure were calculated for both 0 V and 2 V applied bias. Increasing the simulation to include three QW slightly changes the absorption spectra without appreciably changing the absorption edge.

Due to the differences between the structure as designed and as grown a direct comparison for each design is not useful. Instead the two wafers which are most similar (the 14 nm design and the 13.6 nm as grown wafers) will be compared. For each bias voltage the wavefunctions are calculated using the 8x8 $k \cdot p$ method calculated at only the $\Gamma$ point of the Brillouin zone. From this calculation the wavefunctions for the HH, LH, and c$\Gamma$ valleys are calculated. While the difference in QW size is only 0.4 nm the difference in barrier thickness is 5.5 nm. The wavefunctions of the as grown structure should therefore be less perturbed by neighbouring QWs. Another difference which will have an effect on the wavefunctions is that the height of the barriers is higher in the as grown structure. The wavefunctions for the two structures are compared in figure 5.21. The effect of the higher barriers is that there is less penetration of the wavefunction into the barrier region. The lower strain in the Ge well means that the LH and HH bands are nearly degenerate in the well.

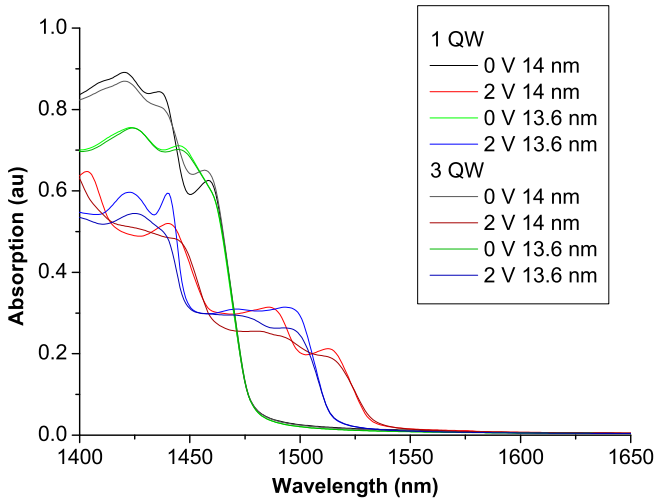


**Figure 5.20:** Comparison of the calculated absorption spectra from the 14 nm design structure and the 13.6 nm as grown structures for both a single QW simulation and a three QW simulation.

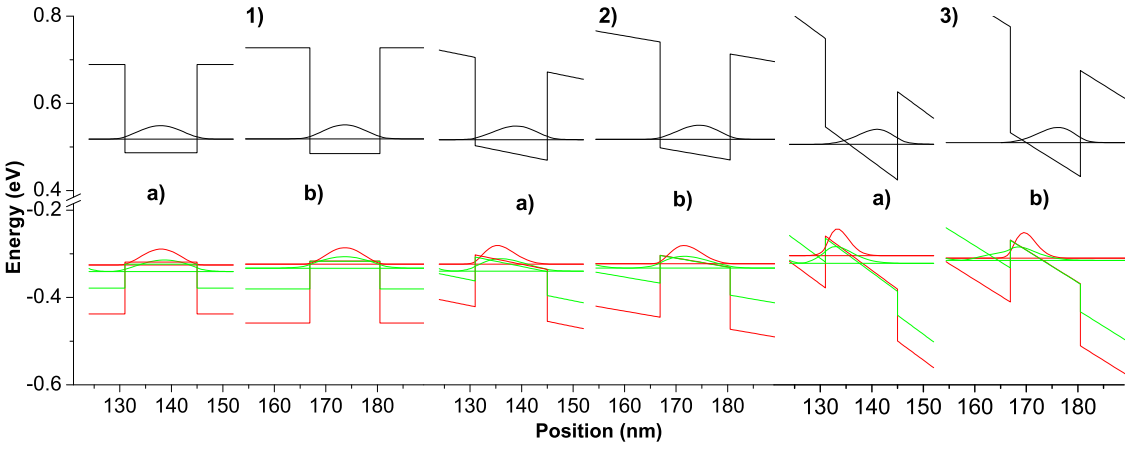


**Figure 5.21:** Comparison of the wavefunctions for a) the 14 nm design and b) the 13.6 nm as grown structures at 1) flat band, 2) built in voltage, and 3) 2 V applied.

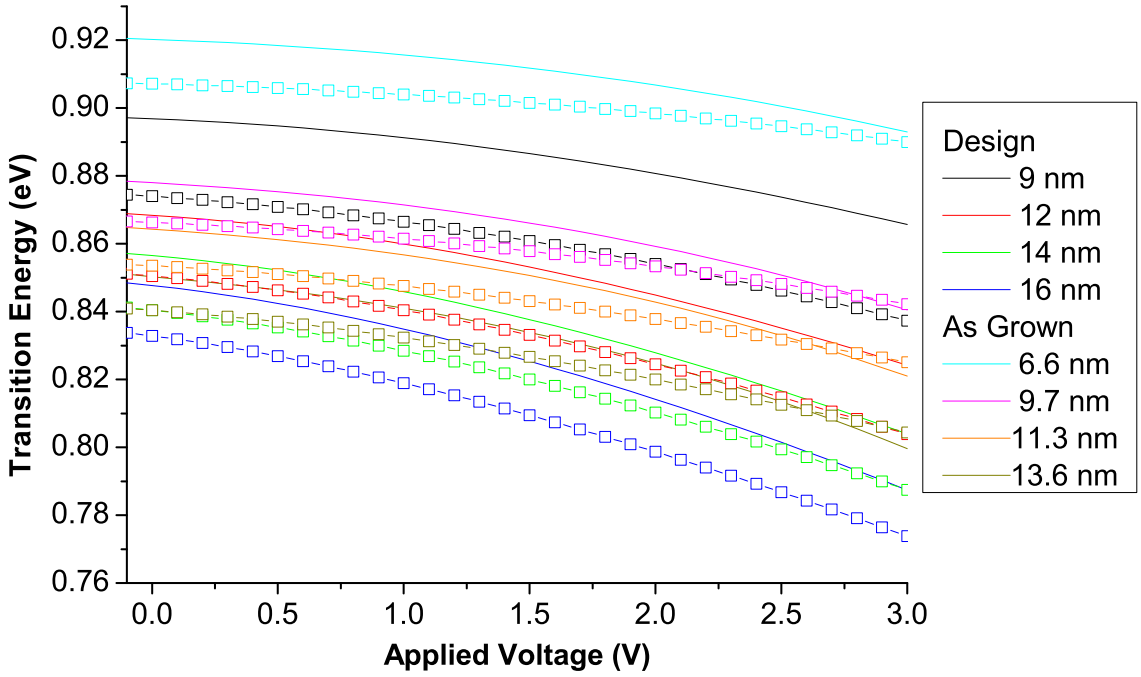


**Figure 5.22:** Energy difference between 1st Γ energy level and either 1st heavy hole (HH1) energy level (squares) or 1st light hole (LH1) energy level (solid lines) calculated for QCSE structures from -0.1 applied bias to 3.0 applied bias using single QW simulation. The as grown 13.6 nm LH1 transition line is hard to distinguish due to being nearly overlapped by the design 12 nm HH1 transition line.

The difference in energy between the highest valence band energy level and the lowest conduction band energy level at the Γ point determines the energy of the absorption edge. The transition energy between the HH1 and Γ1 energy levels and the LH1 and Γ1 energy levels has been calculated as a function of bias for each of the different QW widths. The energy levels of the valence and conduction band states are calculated near the Γ point using the 8x8 $k \cdot p$ method. The transition energy is the difference between Γ1 energy level and the HH1 or LH1 energy level and is seen to be a quadratic function of the bias voltage. Figure 5.22 shows the transition energies for both the designed and as grown structures. Both the Γ1-HH1 and the Γ1-LH1 transitions are shown. The HH1 transitions in the as grown structures show a lower dependence on the applied voltage compared to the LH1 transitions and both the transitions in the design structures. For the as grown structures the Γ1-HH1 and the Γ1-LH1 energies cross near 3 V. For the designed structures the Γ1-HH1 transition is at a lower energy than the Γ1-LH1 transition over the entire simulated voltage range.

## 5.4 Future Work

Despite the accuracy seen in the absorption edge peak of the simulations as compared to the measured spectra from the Edwards paper, the higher energy part of the spectrum and the size of the low energy tail do not match. When the as grown simulated spectra are compared to the spectra of the measured devices a greater discrepancy is seen. One possible source of difference between the simulated and measured results would be absorption in the device from outside of the quantum well region. Another possible source of discrepancy between the simulated spectra and the measure spectra is due to uncertainty in the measurement of the layer thicknesses and variation in the layer thicknesses (especially the thicknesses of the QWs). Variation in the QW thicknesses in the devices would lead to a superposition of different spectra from all of the QWs. The simulation calculates the absorption from a single well. This would result in a spreading of the absorption peaks not taken into account in the simulation. Since there is uncertainty in the measurement of the layers the true layer thickness could be much larger or smaller than the layer thickness. The nominally 6.6 nm QW structure has an uncertainty of $\pm 0.9$ nm. The difference between the absorption edge of a 5.7 nm QW and a 7.5 nm QW will be quite substantial. The thickness of the intrinsic region of the device also has an effect on the simulated absorption since the electric field across the device depends on both the applied voltage and the size of the intrinsic region. Improved simulation results could be obtained by taking into account the absorption outside of the QW region. A better match between the simulated spectra and the measured spectra could be obtained by changing the structure parameters while staying within the uncertainty of the measurement. If the variation in thickness in the structure as grown is sufficiently low it should be possible to determine the parameters by matching multiple features in the spectra.

Another potential avenue of investigation would be to determine the minimum barrier thickness which is able to confine the wavefunctions sufficiently to allow absorption modulation via the QCSE. This could lead to designs that have the minimum swing voltage required while maintaining good absorption and contrast ratios. For the designed structures to be realizable they must take into account the requirements of strained epitaxial growth to prevent relaxation of the active layers. Another option to investigate would be MQW structures in which small groups of wells with thin barriers are separated from other groups by larger barriers or asymmetric QWs. This could result in QCSE devices which have an increased peak shift near voltages in which alignment between adjacent wells occurs.

## 5.5 Summary

The comparison of the absorption and QCSE from the simulations of the structures published in the Edwards paper to the published experimental results shows the results of the simulations are useful for predicting the absorption edge and QCSE for SiGe/Ge MQW designs. Having shown that the absorption spectra for SiGe/Ge MQW devices can be accurately calculated using the simulation, novel designs were simulated.

Low voltage QCSE devices have been designed by using thin barriers to separate the QWs. The designs were all based on the same $Si_{0.05}Ge_{0.95}$ virtual substrate with Ge wells and $Si_{0.15}Ge_{0.85}$ barriers. The barriers were chosen to be half the width of the wells which provides strain balancing allowing large heterostructures to be grown without relaxation. From simulations of the structure of a three quantum well region it has been shown that the thin barriers provide for wavefunctions that are mostly confined to a single quantum well; therefore, there should be little interaction between wavefunctions in neighbouring quantum wells. The computational resources required to perform a simulation of a single QW region is significantly lower than that of a multiple QW region. The accuracy of a one QW simulation was compared to a three QW simulation in order to determine if the simulation was reasonably accurate. It was shown that a single QW calculation of the absorption spectra of SiGe/Ge MQW structures with barriers half the width of the QWs provides an accurate picture of the QCSE. While the shape of the absorption spectrum between a one QW simulation and a three QW simulation differed, the absorption edge was nearly coincident. The structure of the wafers received from Warwick University varied significantly from the design so the absorption spectra of the as grown structures were also simulated. The structure of the wafer was measured by collaborators at Warwick University using TEM and the measured parameters used for the as-grown simulations. From the simulations it was seen that the shift in the absorption peak as a function of applied bias should be less than for the designed structures. It was also revealed that the LH and HH transition are much closer in energy and move closer as the applied voltage is increased. In the next chapter the calculated spectra for the as grown structures will be compared to the experimentally measured spectra from photodiodes fabricated from the wafers.

# Chapter 6

# Fabricated Low Voltage QCSE Devices

## 6.1 Introduction

Integration of optical communications monolithically into Si electronic chips requires CMOS compatible processes. Ge and SiGe alloys are currently in use within CMOS production for the fabrication of electrical transistors. One requirement for on chip optical communications is an optical modulator. CMOS compatible SiGe/Ge MQW QCSE modulators have the potential to be incorporated into an integrated optical communications system. The SiGe/Ge MQW QCSE modulators rely on the electo-optic absorption effect where a change in applied voltage changes the absorption edge of the material. The absorption spectra of a QCSE device can be measured by using a pin structure, fabricating a photodiode, and measuring the photocurrent spectrum as a function of applied bias.

## 6.2 pin Photodiode

A semiconductor device with an intrinsic layer sandwiched between heavily doped n-type and p-type layers is known as a pin diode. The p-type layer has majority hole carriers while the n-type layer has majority electron carriers. When no bias is applied the built-in bias will form due to the diffusion of carriers into the intrinsic region. When a positive voltage is applied to the p-type side holes in the p-type region and electrons

in the n-type region travel to the intrinsic region and combine, allowing current to flow, this is known as a forward bias. When a negative voltage is applied to the p-type side holes in the p-type region and electrons in the n-type region travel away from the intrinsic region, increasing the size of the depletion region and preventing current from flowing, this is known as reverse bias. In reverse bias there is still a small amount of current flow due to minority carriers and non-idealities; this is known as the leakage or dark current (Fig. 6.1).

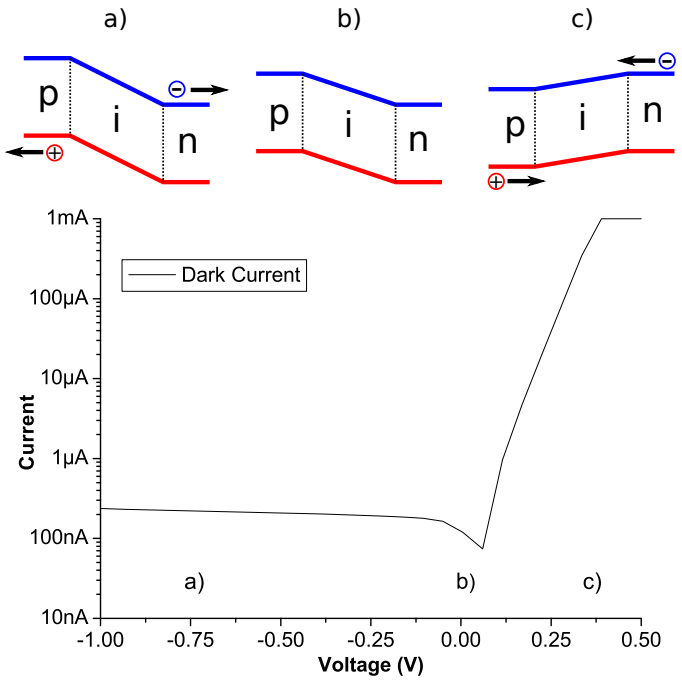


**Figure 6.1:** Top: diagram of ideal pin diode with hole rich p, electron rich n and carrier depleted i regions. Bottom: current-voltage plot of diode measured with 1 mA current limit in forward bias. The three different regimes are shown: a) reverse bias where electron and holes are pulled apart by the electric field and current is low, b) unbiased where built-in potential sets up a small electric field, and c) forward bias where electrons and holes are pulled together and recombine in the intrinsic region allowing a current to easily flow.

A pin diode is operated in reverse bias when used as a photodiode. When a photon is absorbed in the intrinsic region of the photodiode it will create an electron-hole pair. In reverse bias the intrinsic region is devoid of holes and electrons and there is a potential gradient which will sweep holes and electrons apart [128]. This creates a current that is dependent upon the number of photons absorbed, called a photocurrent.

## 6.3 Wafer Growth

The wafers used for the fabrication of the QCSE devices were grown by collaborators at Warwick University. The MQW structures were grown on Si wafers using an ASM Epsilon 2000E low pressure chemical vapour deposition tool. The structures are grown by chemical reaction between precursor gases and the wafer surface within a reaction chamber. The Ge is grown using germane ($GeH_4$) precursor gas and Si using dichlorosilane ($SiH_2Cl_2$). Dopants are added *in-situ* by the addition to the reaction chamber of phosphane ($PH_3$) gas for P doped n-type, or diborane ($B_2H_6$) gas for B doped p-type layers. The ratio of gases and wafer temperature determine the quality of the growth structure and the Ge fraction. A change in gas ratio will not only change the Ge fraction in the layer but also the growth rate of the layer. The gas ratios and growth temperature must be carefully calibrated to achieve the desired wafer structure [32].

A 1 $\mu$m thick Ge seed layer was first deposited on a 200 mm p-Si(001) wafer using the two temperature growth method [129]. This was followed by a 250 nm thick reverse graded $Si_xGe_{1-x}$ from $x = 0$ to $x = 0.04$ buffer grown at 850 °C. Next a virtual substrate of 500 nm thick $Si_{0.04}Ge_{0.96}$ was grown. The active structure was grown on top of the virtual substrate in a pin structure with the quantum wells within the intrinsic region. Figure 6.2 shows a schematic of the structure as grown. The MQW region consists of 11 SiGe barriers and 10 Ge quantum wells. The thicknesses of the layers for the different wafers are tabulated below (Table 6.1).

The actual thicknesses of the layers were measured by collaborators at Warwick University using cross-sectional transmission electron microscopy (Fig. 6.3). The relaxation and composition was measured by x-ray diffraction using reciprocal space maps. The Ge seed layer was measured to be 104.5 percent relaxed relative to the Si(001) substrate, the $Si_{0.04}Ge_{0.96}$ buffer layer was fully relaxed relative to the Ge seed layer, and the active layers were fully strained to the $Si_{0.04}Ge_{0.96}$ buffer. The residual strain in the Ge and $Si_{0.04}Ge_{0.96}$ layers is therefore $\sim$0.18 percent tensile strain. The layer thicknesses and Si content of SiGe layers in the as grown structure differed from the designed structure and the differences are tabulated in tables 6.1 and 6.2.

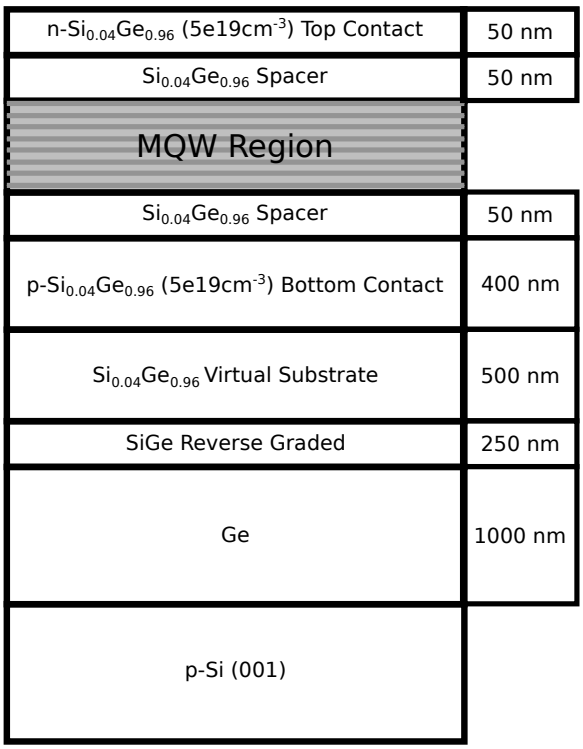


**Figure 6.2:** Structure of the QCSE devices as grown and measured by Warwick University collaborators.

**Table 6.1:** Well and barrier widths of QCSE as designed and as grown from measurements made by collaborators at Warwick University.

| Wafer | QW Design | QW Measured | Barrier Design | Barrier Measured |
|---|---|---|---|---|
| 13-307 | 9 nm | 6.6±0.9 nm | 4.5 nm | 8.2 nm±0.7 nm |
| 13-308 | 12 nm | 9.7±0.7 nm | 6 nm | 10.3 nm±0.2 nm |
| 13-309 | 14 nm | 11.3±0.3 nm | 7 nm | 11.5 nm±0.6 nm |
| 13-310 | 16 nm | 13.6±0.3 nm | 8 nm | 12.5 nm±0.4 nm |

## 6.4 Fabrication

A photodiode device fabricated from the QCSE wafers is required to have a mesa structure which defines the active area and connections to the top and bottom contact layers. As the light will be normal to the surface, the top contact must allow the transmission of light into the active area. The device will be wirebonded to a chip carrier to allow easy connection to external power supply and current measurement. The contacts must be connected to a bond pad which provides an area large enough to support wirebonding.

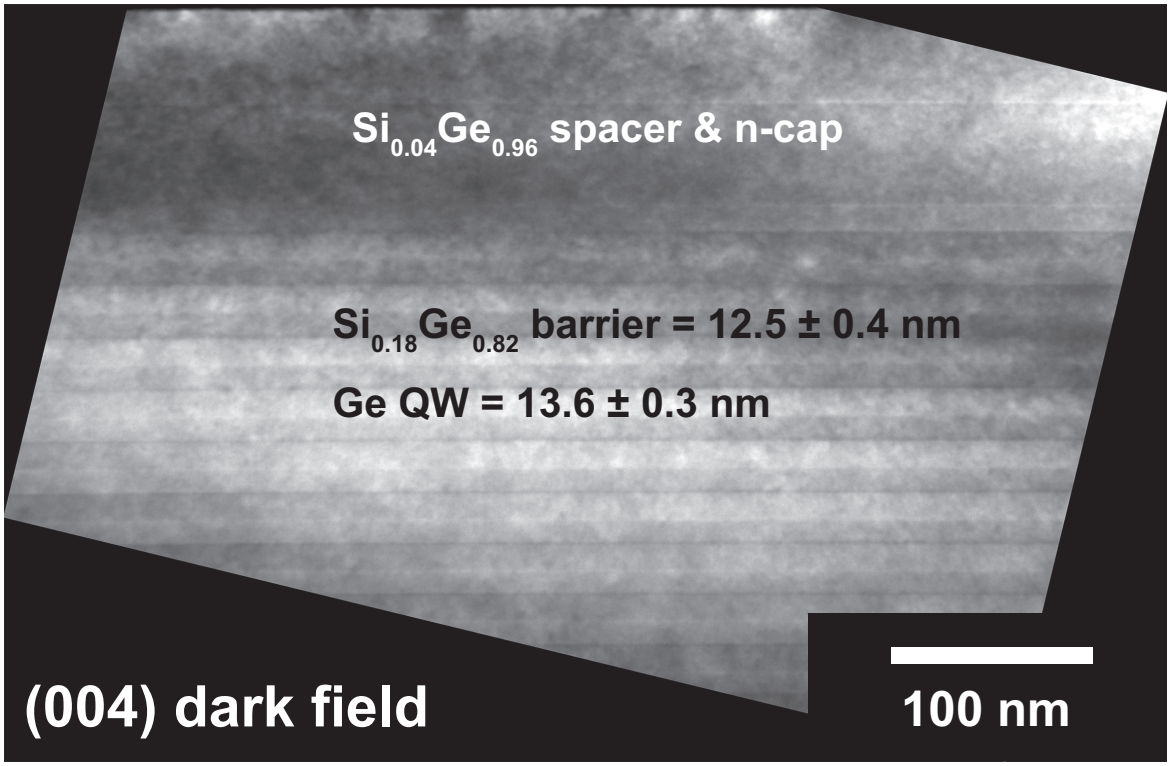


**Figure 6.3:** TEM image of the structure of the 13.6 nm QW QCSE wafer measured by Warwick University collaborators.

**Table 6.2:** Layer composition of QCSE as designed and as grown from measurements made by collaborators at Warwick University.

| Layer | Design | Measured |
|---|---|---|
| Buffer | $Si_{0.05}Ge_{0.95}$ | $Si_{0.04}Ge_{0.96}$ |
| Barriers | $Si_{0.15}Ge_{0.85}$ | $Si_{0.18}Ge_{0.82}$ |
| Wells | Ge | Ge |

### 6.4.1 Mask Design

A photomask was designed and produced containing patterns to fabricate the photodiodes. The photomask contains patterns to produce 21 small (100 $\mu$m radius) photodiodes, 12 medium sized (200 $\mu$m radius) photodiodes and 9 large (300 $\mu$m radius) photodiodes. There are four layers in total, one each for the mesas, contacts, via holes, and bond pads. The mesa layer contains three sets of alignment markers, that match up with a set of alignment markers on each of the other layers. The photomask which was designed using L-edit CAD software (Fig. 6.4) also contains CTLM structures to test the contacts.

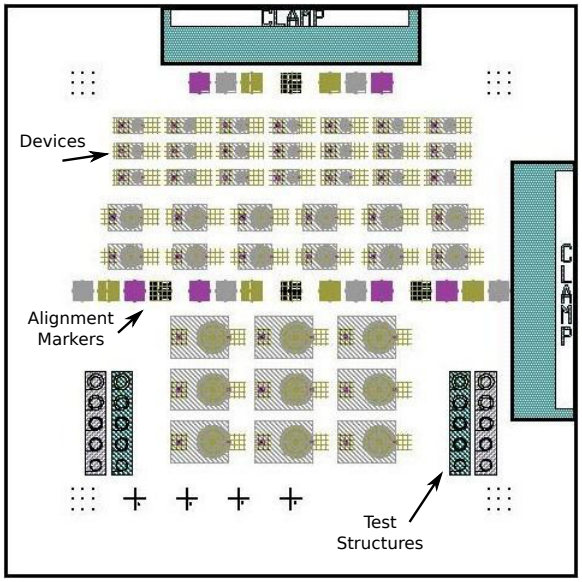


**Figure 6.4:** Design of photodiode mask from L-edit, showing alignment markers, and test structures alongside the photodiodes. A marker layer, which contains clamp areas, alignment markers, and alignment crosses for use with e-beam lithography processes is shown but was not transferred to the photomask.

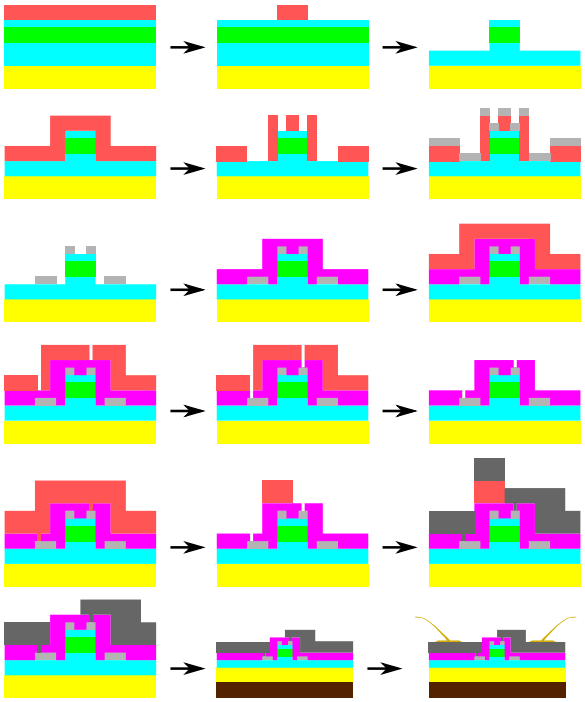

**Figure 6.5:** Schematic diagram of the steps required to fabricate a QCSE photodiode.

### 6.4.2 Process

The process flow used for the fabrication of QCSE photodiodes is diagrammed in figure 6.5. Before the fabrication process is started a 15 $cm^2$ sample is cleaved from the wafer. The first step is to clean the sample and spin coat it with a layer of AZ2070 resist. The resist is then patterned by exposure using the mesa layer of the photomask and

development of the unexposed areas. The sample is then dry etched to create the mesa structure. Dry etch is performed with an ICP dry etch tool utilizing $SF_6$ and $C_4F_8$ for a nearly vertical etch. The etch depth is monitored using laser reflectometry to determine the correct etch stop time. The etch removes material down to slightly below the top of the bottom contact layer. After etching the resist is removed and sample cleaned using acetone and IPA. Again the sample is spun coated, this time with a layer of S1818 resist. The contacts layer of the photomask is used to expose the sample which is then developed to remove the exposed areas. Immediately after a 30 s dip in HF to remove any oxide on the contact layer due to exposure to atmosphere, a layer of 10 nm of Ni and 50 nm of Pt is deposited using an electron beam metal deposition tool. The unwanted metal is removed via liftoff of the resist using acetone in a 50 °C bath. The devices are now working photodiodes which can be tested using needle probes to contact the diode. The CTLM test structures are used to confirm good quality Ohmic contacts have been made to both the top and bottom contact layers.

The size of the top contact layer is much smaller than the size of the mesa in order to allow light into the device. This makes directly probing the devices difficult and directly wirebonding impractical. Large pads of aluminium are required for wirebonding but do not fit on the top of the mesa. In order to use the devices in the FTIR setup to measure the absorption spectrum the devices are required to be wirebonded to a chip carrier. This provides reliable contact to a device which can be easily switched between devices. To prepare the devices for wirebonding further steps are required.

After the contacts have been tested the sample is cleaned in acetone and IPA and then a 200 nm layer of $Si_3N_4$ is deposited using an ICP nitride deposition tool. This insulates the surface to prevent the top contact bond pad from shorting to the bottom contact layer. This thickness of $Si_3N_4$ also provides an anti-reflection coating for wavelengths around 1550 nm. Again a layer of S1818 resist is spun onto the sample. Small via holes are patterned above the contacts by exposure and development. The $Si_3N_4$ in the patterned areas is then etched using $CHF_3$ / $N_2$ gases in a RIE dry etch tool. The Pt on top of the contacts acts as an etch stop preventing overetching. A final layer of resist is spun. AZ2070 is used here due to its thickness and as it gives a large under cut when developed. The bond pad layer is patterned by exposure and the unexposed resist is developed away. A layer of Ti (10 nm) and a thick layer of aluminium ($> 300$ nm) is sputtered over the surface, filling the via holes and creating large pads for wirebonding connected to the contacts. The excess metal is lifted off as the resist is removed. Each device is tested electrically to ensure only devices with good rectifying behaviour are wirebonded. The sample is then cleaved into small ($< 5$

mm × 5 mm) chips and adhered to leadless chip carriers (LCCs) before the chosen devices are wirebonded to the LCC (Fig. 6.6).

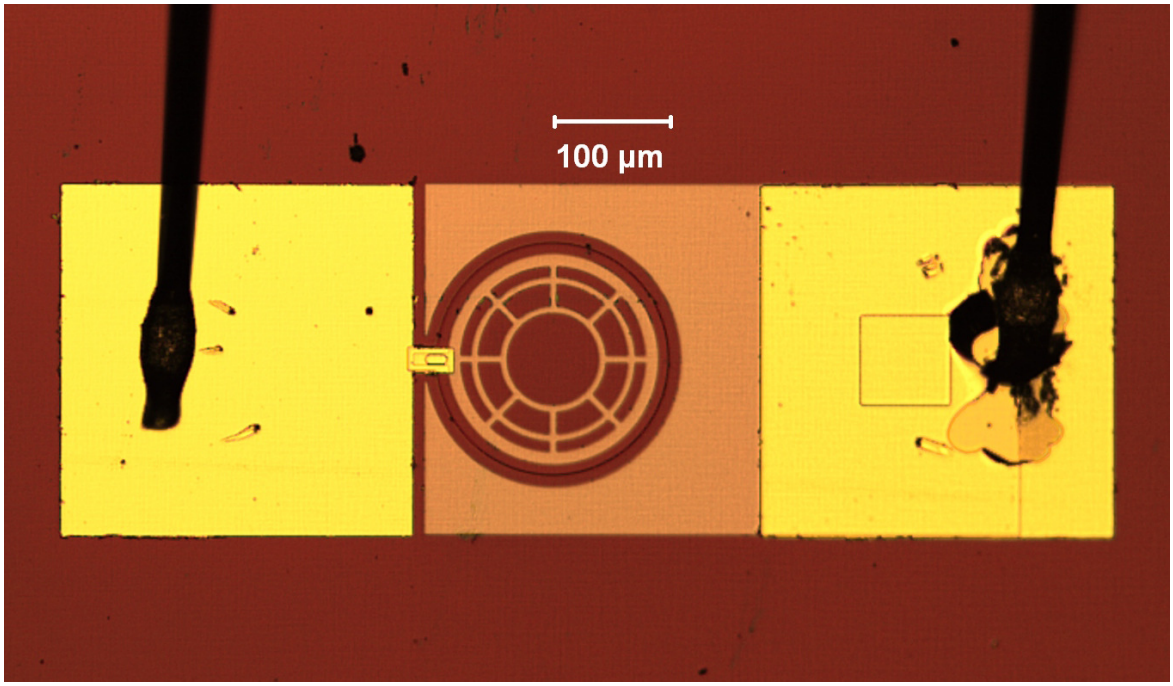


**Figure 6.6:** Optical microscope image of a completed 100 $\mu$m radius SiGe/Ge QCSE photodiode. Diode has been wirebonded to a leadless chip carrier.

## 6.5 Measurements

Once a device has been fabricated, measurements of the electrical and electro-optical properties can be made. The electrical and electro-optical properties of each device will depend on both the properties of the wafer and the quality of the fabrication process.

### 6.5.1 Contact Quality

Along with the photodiodes, CTLM structures are fabricated for both the top and bottom contacts. Electrical measurements are made using the CTLM structures before the layer of $Si_3N_4$ is deposited. This allows for characterization of the contacts to the top and bottom contact layers. Four-point probe measurements are made for each gap spacing on the CTLM structures for both top and bottom contacts. This determines whether the contact is Ohmic or not and the specific contact resistivity. Since the CTLM structures are fabricated during the same process used to fabricate the top and

bottom contacts of the devices, the specific contact resistivity of the CTLM structures can reasonably be expected to be the same as the device contacts.

### 6.5.2 Dark Current

Electrical measurements of the dark current is performed before wirebonding to ensure only functioning devices are wirebonded. After fabrication of the bond pads each photodiode is probed in the probe station and the current is measured as the voltage is swept between 1 V forward to 5 V reverse. The current is limited to 1 mA to prevent heating effects during forward bias from damaging the photodiode. A good diode will show rectifying behaviour with very little current during reverse bias and will reach 1 mA around 0.3 V forward bias. Defects in the wafer that coincide with the device can negatively effect the dark current behaviour of the device, leading to higher reverse current or even Ohmic behaviour. The dark current can also be affected by poor contact or bond pad fabrication.

### 6.5.3 FTIR

A Fourier transform infrared spectrometer (FTIR) was used to measure the photocurrent spectrum of the QCSE devices. The spectral response of a device or material can be accurately measured using an FTIR over a broad spectrum. Unlike dispersive spectrometers, where a single wavelength is measured at a time, an FTIR measures the collective response to multiple wavelengths providing a higher signal to noise ratio measurement. An FTIR uses a Michelson interferometer and a broadband infrared light source to create a beam of infrared light which contains a controllable spectrum. When the light enters the Michelson interferometer it is split into two paths by a beamsplitter. Both paths reflect the light back to the beamsplitter where it coherently recombines before traveling to the device under test. A movable mirror allows one of the path lengths to be modified. The optical path difference between the two paths will determine if the interference is constructive or destructive for each wavelength of light. As the mirror moves the light from each path will move in and out of phase, changing intensity sinusoidally. The period of the sinusoid will be different for each wavelength of light. The measurement from the detector as a function of mirror displacement is called an interferogram. The interferogram is simply Fourier transformed to recover the spectrum [130]. For a photocurrent measurement the device is used in place of the detector and the current through the device is the measured signal.

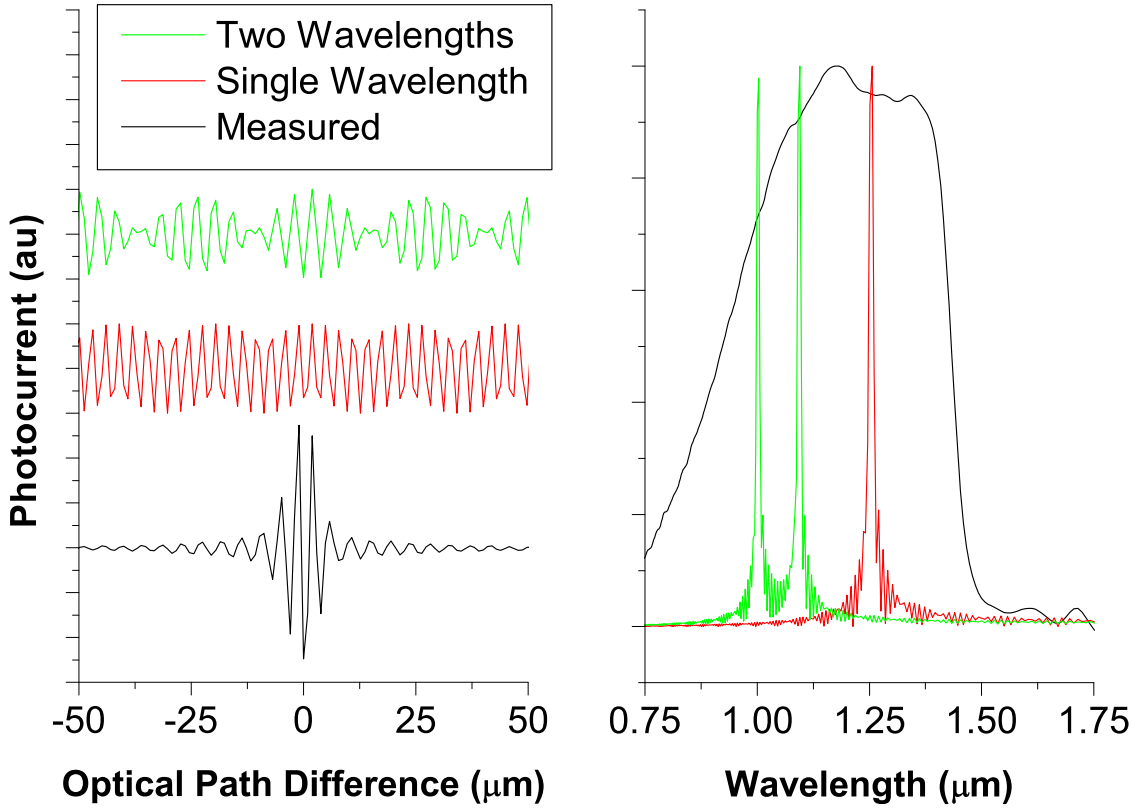


**Figure 6.7:** Calculated spectrum and interferogram of a photocurrent measurement for one and two wavelengths of light, and an example of a measurement from an FTIR. Measured spectrum and interferogram are from an QCSE photocurrent measurement. The one and two wavelength interferograms are sampled from one and two cosine functions respectively and Fourier transformed into spectra using MATLAB.

### Rapid Scan Measurement

In a rapid scan measurement the mirror in the interferometer is continuously moving back and forth during the measurement and the interferograms are averaged together. A full spectrum is available immediately and the signal to noise ratio decreases as more interferograms are measured. To measure the photocurrent using the rapid scan method the current from the photodiode is amplified using a transimpedance amplifier to provide the FTIR with a voltage proportional to the photocurrent. The measurement setup did not provide for isolation of the diode from extraneous light sources such as the room light which if switched on or off during a measurement could ruin a data set. Another way to measure the photocurrent spectrum which is immune to these issues is to use a step scan method. This is the method used in this work when measuring the photocurrent with the FTIR.

### Step Scan Measurement

The step scan method isolates the photocurrent due to the light from the interferometer during a photocurrent spectrum measurement using the FTIR. Any other sources of current in the device, such as stray light photocurrent or dark current will not contribute to the measurement. In a step scan measurement the mirror in the interferometer is held still while each point in the interferogram is measured before stepping to the next mirror position. The measured signal comes from a lock-in amplifier (LIA) which extracts the amplitude of the photocurrent at a reference frequency. If the source light is chopped at the referenced frequency before hitting the diode the LIA will extract the current due to the light from the source. A schematic of the FTIR step scan setup used for photocurrent spectrum measurements is shown in figure 6.8.

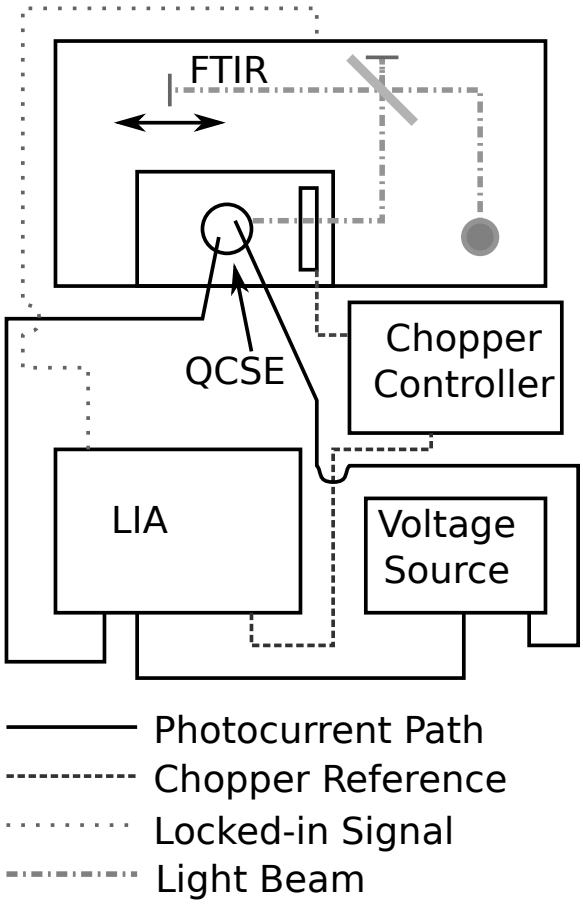


**Figure 6.8:** Schematic diagram of the setup of the FTIR system used to measure the photocurrent of the QCSE photodiodes.

### 6.5.4 Measuring Absorption Efficiency

The absorption efficiency of a photodiode can be accurately measured using a tunable laser setup. The tunable laser setup allows light of a known power to be focused on to a single device while the photocurrent is being measured. This allows an accurate absorption efficiency to be calculated. The light from a wavelength tunable laser diode source (TLS) is focused down to a small spot size using a lensed optical fibre. The optical fibre can then be aligned with the photodiode such that all of the light from the fibre is incident on the photodiode. The total light exiting the fibre can be measured using a calibrated optical power meter. The total light entering the photodiode can be calculated by taking into account the reflected light from the anti-reflection coating, which should be designed to be small over the wavelengths required. For a current $I$ measured at a wavelength $\lambda$ with incident power $W$ the absorption efficiency $\gamma$ is calculated, assuming one electron of current per photon absorbed, by

$$\gamma = \frac{\text{number of electrons in current}}{\text{number of photons in light}} = \frac{I}{q} \times \frac{\lambda}{Whc} \tag{6.1}$$

where $h$ is Plank's constant, $q$ is the electron charge, and $c$ is the speed of light.

## 6.6 Electrical Analysis

### 6.6.1 Contacts

The quality of the contacts is tested after contact deposition using the CTLM test structures. CTLM test structures are fabricated during the same process step as the contacts. Both top and bottom contact CTLMs are fabricated. Since both the top and bottom contacts are Ohmic, the specific contact resistivities and sheet resistance can be extracted from the test structures (Fig. 6.9). The top contact gives a specific contact resistivity of $1.0 \times 10^{-5}$ $\Omega$-cm$^2$ while the bottom contact give a specific contact resistivity of $3.5 \times 10^{-5}$ $\Omega$-cm$^2$. While both top and bottom contact layers are highly doped with similarly low resistivities the sheet resistances (proportional to slope in Fig.6.9) are quite different due to the difference in thicknesses of the layers. Since the contacts are Ohmic with a low resistance a higher fraction of the voltage drop across the device will be across the MQW region. This will allow a lower applied voltage for the same shift in absorption compared to devices with poorer quality contacts.

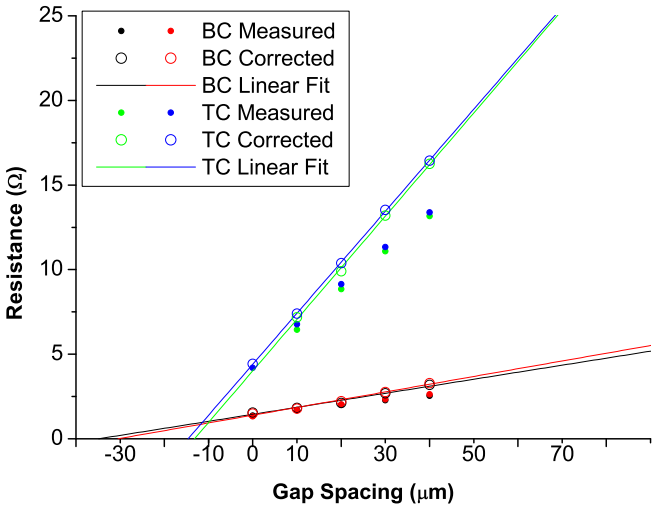


**Figure 6.9:** Measured and corrected resistance values from top and bottom contact CTLM test structures on QCSE photodiodes.

### 6.6.2 Diode Current-voltage

The current-voltage characteristics of the photodiodes are greatly affected by the presence of defects in the structure of the wafer (Fig. 6.10). The surface of the wafers contain a random pattern of pits which are over 400 nm deep (Fig. 6.11). The effect of a pit on the device's current-voltage characteristics has been examined.

#### Pit Distribution

Three randomly chosen small areas of a wafer (4 $mm^2$) were examined and the number of pits counted. An average of 9.2 pits per $mm^2$ was found. Assuming each pit is randomly and independently placed, a Poisson distribution, and measuring the average number of pits in a given area, the probability of a diode of a given size containing a pit can be calculated. The Poisson distribution assumes a random distribution of pits with a known mean density of pits $D_{\text{pits}}$. The probability $P$ of finding exactly $n$ pits in an area $A$ is [131]

$$P(n = x) = \mathrm{e}^{-\lambda}\frac{\lambda^x}{x!} \tag{6.2}$$

where $\lambda = D_{\text{pits}} \times A$. The probability of a diode having at least one pit is the same as not finding zero pits within a device will be

$$P(n > 0) = 1 - P(0) = 1 - \mathrm{e}^{-\lambda} \tag{6.3}$$

The probability of a device having a pit in the mesa will depend on the size of the mesa and the density of pits. For these wafers $D_{\text{pits}} = 9.2\ \text{mm}^{-2}$ and the mesas have a circular area with radius 100 $\mu$m, 200 $\mu$m, or 300 $\mu$m. The expected fraction of devices which will contain a pit for each size is listed in table 6.3.

**Table 6.3:** Probability that a device with a mesa structure of the given size will contain a pit in the mesa structure.

| Radius | Area | Probability |
|---|---|---|
| 100 $\mu$m | $3.14 \times 10^{-2}$ mm$^2$ | 25.1 % |
| 200 $\mu$m | $1.26 \times 10^{-1}$ mm$^2$ | 68.5 % |
| 300 $\mu$m | $2.83 \times 10^{-1}$ mm$^2$ | 92.6 % |

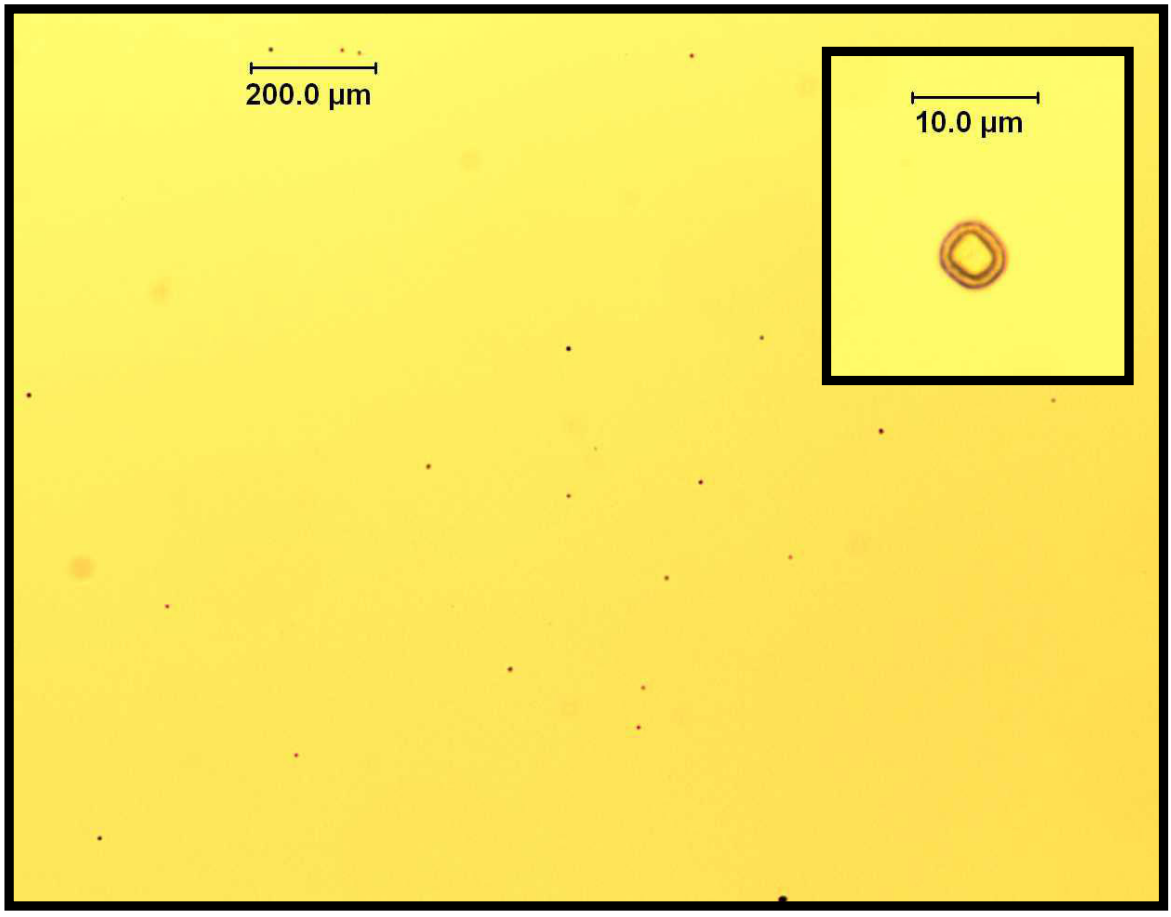


**Figure 6.10:** Optical microscope image of surface of QCSE wafer showing pits. Inset shows single pit at higher magnification.

In order to fabricate a working device a large number of small devices were fabricated. Devices with and without pits were examined and the effect of pit location on the current voltage characteristics was investigated.

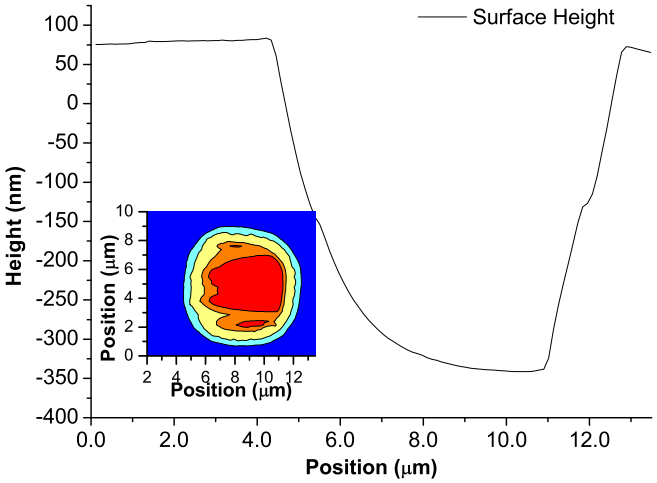


**Figure 6.11:** Trace of height across pit on surface of QCSE wafer before processing, using an atomic force microscope (AFM), inset shows contour map of pit also from AFM measurement. Pit depth of >400 nm is comparable to the height of the active layers of the QCSE wafers.

### Effect of Pit on Dark Current

The current voltage characteristics of the diodes were measured by probing the bond pads and measuring the current as a function of applied bias. Three distinct groups of diode behaviour were found which depend on the absence or position of pits within the photodiode structure (Figs. 6.12, 6.13). The first group were photodiodes that showed rectifying behaviour and currents as low as a few nA at 5 V reverse bias. This first group did not contain any pits within the mesa area. The next group of photodiodes showed rectifying behaviour with much higher current levels. Currents as high as 1 mA at 1 V reverse bias were observed. These were the diodes that contained pits within the mesa structure but not in contact with the metallic top contact. The final group showed Ohmic behaviour for both forward and reverse biases. These diodes had pits which were in physical contact with the top contact layer.

### Effect of Parasitic Resistances

The potential drop across the MQW region contributes to the peak shift via the QCSE. Any extra resistances outside of the MQW region will lower the observed QCSE for an applied voltage. The parasitic resistances will include the contact resistance and the resistance of the contact layers. The resistivity of the intrinsic spacer regions is assumed to be equal to the MQW region and taken into account by adding their thickness to the thickness of the MQW region when calculating the electric field. The

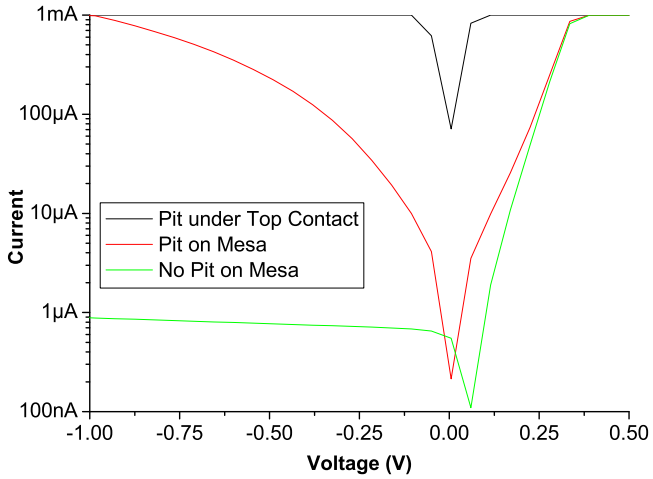


**Figure 6.12:** Comparison of current for diodes without pits, with pits on mesa and with pits under top contact.

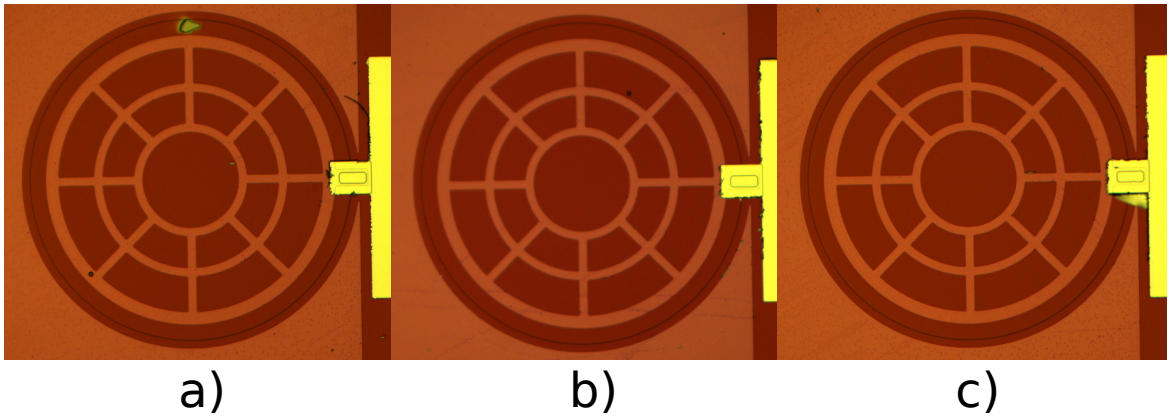


**Figure 6.13:** Microscope image of diodes a) with pits under top contact, b) on mesa but not under top contact, c) and without pits on mesa.

contact resistances can be calculated from the contact area and the contact resistivity. The contact resistances will be compared to the total resistance of the device in reverse bias. For a 100 $\mu$m radius photodiode the area, $A$, of the top contact is 0.0103 mm$^2$ while the bottom contact area is 0.115 mm$^2$. The total contact resistance for each contact $R_C$ is

$$R_C = \rho_c / A \tag{6.4}$$

The resistance $R_{cl}$ through the top and bottom contact layers can be approximated by multiplying the thickness, $t$, of the contact layers by their respective resistivities, $\rho$, and dividing by the area.

$$R_{cl} = \rho \times \frac{t}{A} \tag{6.5}$$

This results in a resistance due to contacts and contact layers of ~127 m$\Omega$ and ~130 $\mu\Omega$ respectively. The total resistance across the device can be calculated from the measured current voltage characteristics. For a dark current measurement of a 100

$\mu$m radius device at 1 V reverse bias, the measured resistance is ~4.23 MΩ. Therefore, the voltage drop across the contact and contact layers is negligible, resulting in efficient use of the applied voltage.

## 6.7 Electroabsorption Analysis

### 6.7.1 Quantum Well Width

The absorption spectra will be different for devices with different quantum well widths. The larger quantum well designs have a thicker structure between the top and bottom contacts, leading to a lower electric field across the MQW region at a given applied bias as well as a lower change in electric field for a given change in applied bias. The energy levels in the larger quantum wells will be closer to the band edge than the corresponding energy level in a thinner quantum well. This leads to a shift to higher wavelengths for the absorption edge as the quantum well width is increased. The difference in absorption between the three different quantum well thicknesses measured is shown in figure 6.14.

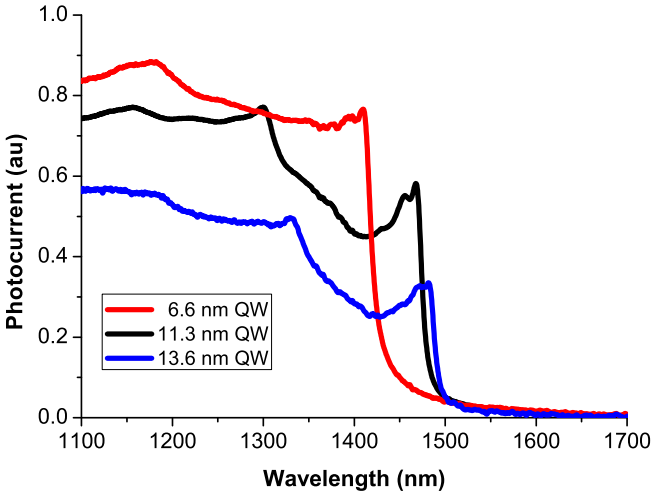


**Figure 6.14:** Photocurrent absorption spectrum for QCSE diodes at zero applied bias as measured with a FTIR.

### 6.7.2 Spectral Shift with Applied Bias

#### FTIR

The photocurrent spectra of the QCSE photodiodes were measured using a Fourier transform infrared spectrometer (FTIR). The resultant spectrum from a measurement is a combination of the output spectrum of the source, the transmission spectrum of the beamsplitter, the transmission spectrum of the air, and the absorption spectrum of the device. The source and beamsplitter are chosen so that in the area of interest the output and transmission spectrum are fairly flat (Fig 6.15). Since the main source of absorption in the air at the wavelengths of interest is from water vapour, the majority of the beam path is kept within a sealed compartment which is desiccated to remove water from the air.

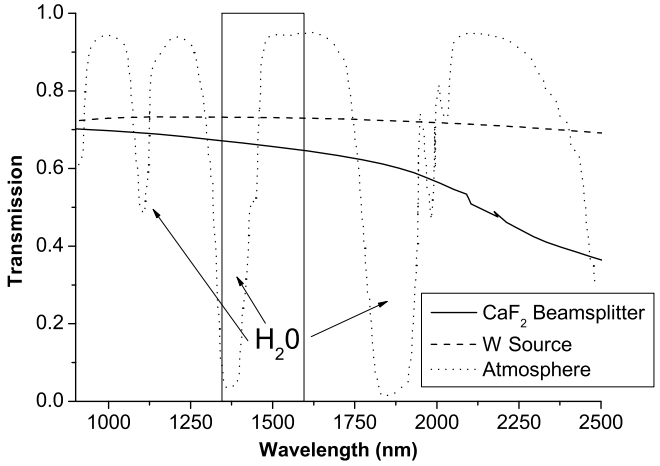


**Figure 6.15:** Transmission spectrum of normal air, $CaF_2$ beamsplitter and output spectrum of tungsten source. Peaks due to water vapour and wavelength range of interest to this work are highlighted. With water vapour removed spectrum is flat over the wavelength range of interest.

The spectra were measured as a function of bias voltage using unpolarized light at normal incidence at 293 K. The diodes were positioned in the sample chamber of a Bruker Vertex 70 FTIR. The FTIR was set up using a tungsten near-infrared source and a $CaF_2$ beamsplitter. A lock-in amplifier (LIA) and mechanical chopper were used to allow step-scan measurements which eliminated the dark current from the measurement. A Keithley 230 programmable voltage source was used to set the applied bias on the device. A schematic of the setup used for the photocurrent spectrum measurement is shown in figure 6.8. A spot size of 2 mm was used to allow easy alignment of a diode under the beam. The mechanical chopper was placed in front of the diode and modulated the light at a rate of 1 kHz. The bottom contact from the photodiode was connected to the current measurement port on the LIA while the

positive terminal on the voltage source was connected to the top contact. The grounds between the LIA and the voltage source where connected. The output signal from the LIA was connected to the detector input of the FTIR. For each bias voltage applied the FTIR ran once, measuring an interferogram and calculating the spectrum. The QCSE could be seen as a shift in the spectrum between measurements with different applied voltages (Fig. 6.16). The peak both shifts to higher wavelengths and broadens as expected due to the change in the electron and hole wavefunctions. The shifts as measured by the peak absorption nearest the absorption edge for the measured devices are show in figure 6.17. For these devices the shift in energy as a function of applied voltage is larger for the wider QWs than for the thinner QWs. The rate of the peak shift depends on both the thickness of the entire intrinsic region as well as the width of the QWs. The absorption peak of wider QWs will have a larger energy shift for a given electric field, while the electric field will be lower for a given applied voltage due to the increased width of the intrinsic region.

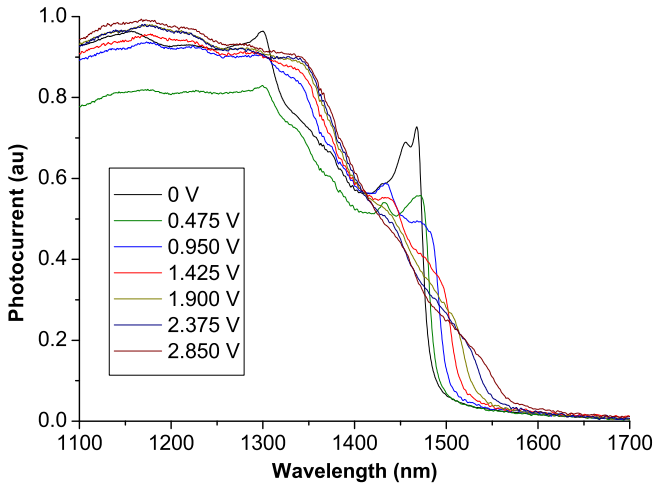


**Figure 6.16:** Spectra for various applied biases for a QCSE device (11.3 nm QW) as measured using FTIR setup.

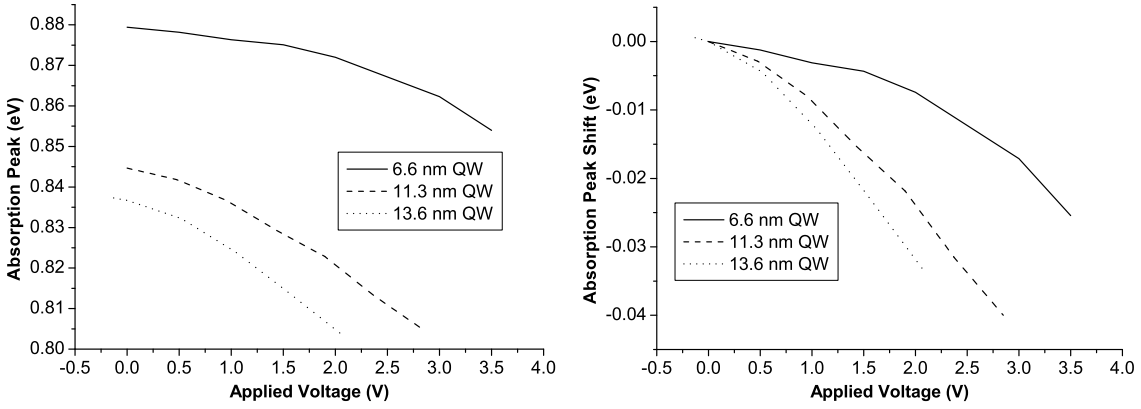


**Figure 6.17:** Shift in absorption peak with applied bias for QCSE devices as measured using FTIR setup.

### 6.7.3 Absorption Efficiency

Although the FTIR allowed measurement of the photocurrent spectrum over a large bandwidth, the absorption coefficients were not calculated due to not knowing the incident optical power at each wavelength at the device. To accurately measure the absorption efficiency a known amount of incident power is required. In order to obtain values for the absorption efficiency, a TLS setup was used to measure the photocurrent of the devices.

#### TLS Setup

The photodiode to be characterized was connected in series with a Keithley 230 programmable voltage source and a Keithley 2000 digital multimeter with GPIB capabilities. The laser source, a Photonetics TUNICS-PRI tunable laser diode source (TLS), was wavelength controllable through GPIB. The TLS was set to 0.20 mW of output power, which was directed through a lensed fibre and aligned at normal incidence to the diode. The fibre was aligned with mirco-manipulators by maximizing the photocurrent at 0 V applied bias and at 1460 nm wavelength. The photocurrent was then measured as a function of applied bias and wavelength. The measurement process was automated using LABview software to step the laser wavelength between each current measurement and step up the applied voltage between each full wavelength sweep. The TLS allowed measurements over a narrow wavelength range (1460 to 1560 nm) and therefore was unable to measure the peak photocurrent of the 6.6 nm QW diodes. The output power from the lensed fibre was measured as a function of wavelength and the Fresnel reflection at the anti-reflection coating ARC was calculated to determine the maximum power reaching the QWs.

At 0 V bias for the 11.3 nm QW device the peak current, after subtracting the dark current, was 6.17 $\mu$A at 1471 nm. The calculated reflectance from the ARC at this wavelength was 1.2% and the measured output at 1471 nm was 0.12 mW. Assuming that each electron in the current is due to one photon being absorbed, an absorption efficiency of 4.4% has been calculated. This value is nearly twice the maximum value obtained by Edwards *et al.* at 1425 nm [2].

#### Well Efficiency

It has been demonstrated that optical absorption normal to the plane of MQW structures should be specified as a fraction of light absorbed per well $\gamma_{\text{well}}(\lambda)$ which is independent of well thickness. This can be calculated from the photocurrent ($I_{\text{ph}}(\lambda)$) at each wavelength ($\lambda$) by: [132]

$$I_{\text{ph}}(\lambda) = \frac{eI_0 N \gamma_{\text{well}}(\lambda)\lambda}{hc} \tag{6.6}$$

under the assumption that $\gamma_{\text{well}}(\lambda) \ll 1$, where $I_0$ is the incident power, $N$ is the number of quantum wells, $e$ is the electron charge, $h$ is Plank's constant, and $c$ is the speed of light.

#### Absorption Coefficient

Light propagating down a waveguide will be parallel to the plane of the MQW layers and therefore the well efficiency will not be a useful metric. In the case of light propagating in the plane of the MQW with the electric field also in the plane of the MQW layers (TE polarization) the absorption coefficient can be calculated from the well efficiency. The absorption coefficient of a QCSE photodiode ($\alpha$) can be defined by: [61]

$$\frac{I_L}{I_0} = \mathrm{e}^{-\alpha L} \tag{6.7}$$

where $\frac{I_L}{I_0} = 1 - \gamma$ is the fraction of light remaining after propagating through a QW and barrier, a length of $L$. If $\frac{I_L}{I_0} \approx 1$ then the absorption coefficient can be calculated using $L$ equal to the total MQW region and $\frac{I_L}{I_0}$ the fraction of light remaining after propagating through the MQW region. In this way the absorption coefficient for waveguided TE polarized light can be calculated from the normal incident absorption.

### 6.7.4 Contrast Ratios

The contrast ratio between the on and off state is an important figure of merit for an electroabsorption modulator [67]. For a QCSE device the contrast ratio is the absorption ratio between two applied voltages. This can be calculated for each wavelength by dividing the two spectra. The difference in voltage between the two biases is known as the swing voltage and the lower of the two voltages is known as the DC offset or bias

voltage. A device which requires a higher DC offset has higher excess energy dissipation from photocurrent and leakage current compared to one with a low or zero DC offset. A higher swing voltage also contributes to excess energy loss. When switching between the low and high voltages the energy dissipated is proportional to the square of the voltage swing [133]. Therefore a device that can operate at a low DC offset with a low swing voltage will be more energy efficient for use as a modulator.

The contrast ratio for a voltage swing of 1 V has been calculated using the measurements from the TLS setup. The 11.3 nm QW devices show a contrast ratio of over 6 dB at 1495 nm for a 0 V DC offset and decreases as the DC offset is increased with a ratio of 4.0 dB at 1550nm for 1.85 V DC offset (Fig. 6.18) above the minimum useful ratio of 4 dB [47] over a range of 65 nm. Trend in the shape and position of the contrast ratio spectrum is directly related to the trend in the shape of the absorption spectra. As the applied bias increases the absorption edge shifts faster and the peak lowers and broadens. While these two effects both lead to increasing the width of the contrast ratio peak, they have opposite effects on the height of the contrast ratio peak as a function of DC offset. The increase in peak shift leads to a higher contrast ratio while the peak lowering and broadening leads to a lower contrast ratio. For this device the overall effect is that the peak contrast ratio increases until around 0.4 V when the effect of the broadening on the peak contrast ratio becomes greater than the effect of the peak shift and the peak contrast ratio begins to decrease.

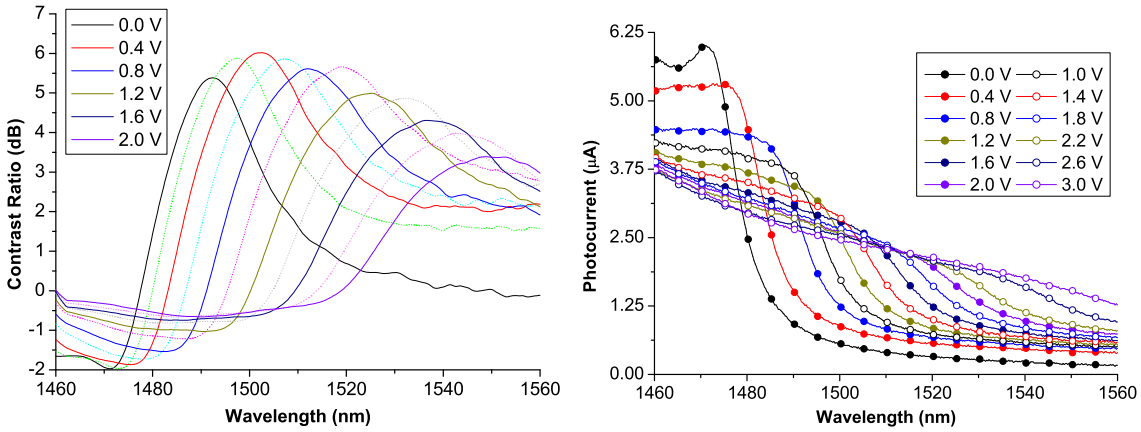


**Figure 6.18:** (Left) Contrast ratios for a voltage swing of 1.0 V for DC bias voltages from 0.0 V to 2.0 V, measured using the TLS setup with 200 mW power and a 11.3 nm QW QCSE photodiode. (Right) Measurement data used to calculate contrast ratios.

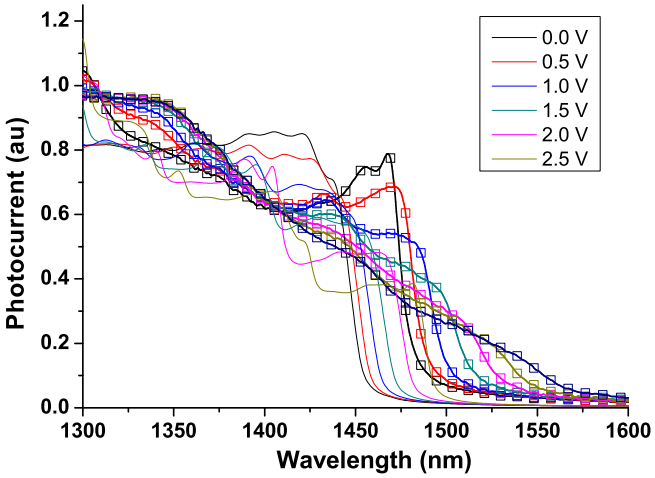


**Figure 6.19:** Comparison between simulated absorption spectra (no marker) for 11.3 nm QW QCSE and measured absorption spectra (square markers) as measured using FTIR.

## 6.8 Comparison to Simulated Results

The absorption spectra as measured was compared to the absorption spectra from the simulations of the as grown structure. The absorption edge for the measured devices is at a higher wavelength then the absorption edge found in the simulations (Fig. 6.19). For the 11.3 nm QW structure a difference of ∼30 nm which is equal to 18 meV (1467.5 nm = 844 meV vs 1437.5 nm = 862 meV) was calculated between the absorption edges at 0 V applied bias. This small difference could be accounted for by the uncertainty in the measurement of the QW and barrier thicknesses. The uncertainty in the strain and Ge content of the virtual substrate could lead to differences in the absorption edge measured versus calculated. The simulations were run using the centre of the uncertainty band only. The absorption spectra could be recalculated using other values within the uncertainty. As the difference is only 18 meV a combination of larger QWs and a slightly higher Ge content or strain in the virtual substrate would lead to a better fit with the experimental data. The LH and HH transitions shift at different rates when the strain is increased, providing another parameter in addition to the absorption edge to match when fitting the strain and QW width.

## 6.9 Comparison to Literature

The devices fabricated in this thesis have shown the best results at 1550 nm for SiGe/Ge MQW QCSE devices. Most devices demonstrated have required high bias voltages (7 V)[67] or high operating temperatures (90°C)[63] in order to operate near

1550 nm and showed lower contrast ratios at 1 V than the devices demonstrated here. In terms of operation near 1550 nm the best SiGe/Ge MQW QCSE modulators demonstrated previous to this work have shown a contrast ratio of 6 dB for a voltage swing of 1V[2]. The comparable low voltage swing contrast ratio was achieved by a reduction in the number of QWs, five QWs instead of ten leading to lower absorption for the design. The decrease in intrinsic region width leads to a higher electric field for a given applied voltage. The devices demonstrated here show a similar contrast ratio with nearly twice the absorption compared to the previous state of the art.

QCSE electro-absorption modulators working at 1550 nm have been fabricated using III-V material systems much earlier than in the SiGe/Ge material system. The flexibility in terms of band edge engineering afforded by III-V systems made realisation of QCSE devices which can operate at a chosen wavelength relatively straightforward. Modulation of light had been demonstrated as early as 1987 using InGaAs/InP MQWs[134]. These devices demonstrated a 17 dB contrast ratio at 1640 nm wavelengths at a bias of 7 V at a modulation frequency of 3 GHz. InGaAs can be lattice matched to InP allowing high quality defect free growth of thick MQW regions. In 1994 InGaAs/InP MQW devices with 200 QWs were grown which showed 9 dB contrast ratio at 1550 nm using high voltages[135]. By 1996 InGaAs/InAlAs MQW devices had demonstrated contrast ratios at 1550 nm of 25 dB with a 1 V swing and a bias voltage of 1.5 V [136].

While there is an increase in performance when using the III-V materials for electro-absorptive modulation over SiGe/Ge, they suffer from lack of CMOS compatibility. The possibility of monolithic integration and the potential of mass fabrication associated with CMOS compatibility gives the SiGe/Ge QCSE designs an advantage over the more mature III-V QCSE designs.

## 6.10 Future Work

Fabrication issues resulted in many devices being unsuitable for photocurrent measurements. Many devices failed during the wirebonding stage which resulted in one of the wafer designs not having a photocurrent measurement. Some of the devices which showed good rectifying behaviour before wirebonding showed Ohmic behaviour afterwards, preventing their use for photocurrent measurements. An investigation into the causes could help prevent further wasted fabrication time and allow more devices to be measured.

The top contact on the devices was a spider web pattern which was used to provide even distribution of the voltage across the top contact and ensure even electric field across the device. This was not an issue for the FTIR measurements in which the total power was unknown. Measuring the absorption coefficient using a lensed fibre to focus a beam onto the top surface the contact pattern made alignment of the fibre difficult and even with perfect alignment blocked a fraction of the light, leading to under reporting of the absorption coefficient. The larger devices had larger openings in the centre of the top contact but, due to the density of pit defects, few of the larger devices were defect free and were unable to be used for photocurrent measurements. These two issues could be resolved by changing the design by removing the larger photocurrent diodes and replacing them with small diodes which contain a larger open window in the top contact. The large windows would allow easier alignment with little or no light missing the photodiode. Comparison between the absorption spectra of the different top contact designs would reveal if there is a difference in electric fields due to the different contacts.

Improvement in the contrast ratio for QCSE devices would be possible if wafers are grown with thinner barriers. The thinner the barrier, the lower the required swing voltage will be for the same contrast ratio. The confinement will also decrease and it is expected that thinner barriers will also have the absorption edge shifted to higher wavelengths. The effects of thinner barriers could be demonstrated by fabricating devices from a series of wafers in which within the MQW region only the barrier thickness is changed. In order to keep the Ge content of the barriers and virtual substrate the same across the series of wafers, the Ge content of the spacer and contact regions may need to modified in order to keep the structure strain balanced. Other novel designs could be grown and devices fabricated based on the results of new simulated structures.

The simulations suggested that the LH and HH to c$\Gamma$ transitions have similar energies. Surface normal illumination has the electric field polarized in the x or y direction which allows absorption between the LH or HH valley and the c$\Gamma$ valley, where z is the direction normal to the surface and layers, and x and y directions are parallel to the layers. Due to the selection rules, the HH to c$\Gamma$ transition is forbidden for light that is polarized along the z direction [124]. Fabrication of waveguide structures using the QCSE wafers would allow one to measure the absorption due to LH transitions separately.

Process induced strain has the potential to shift the operating frequency of a QCSE design. High stress silicon nitride can be used to add tensile strain to the structure.

Silicon nitride has been shown via photoluminescence to shrink the bandgap of Ge nano pillars and ridges [137]. A similar process could be used on thin QCSE structures with the additional requirement of electrical contacts.

## 6.11 Summary

Quantum confined Stark effect structures epitaxily grown on top of Si wafers have the potential to allow efficient modulation of infrared light in the communications wavelength bands. These can potentially be integrated into Si CMOS fabrication processes as modulators for an integrated optical communications on chip system. Ge/SiGe MQW structures with thin barriers have been shown to be able to support confinement of electrons and holes to allow the absorption peak to be shifted by the QCSE. While surface normal photodiodes were fabricated with radii of 100 $\mu$m, 200 $\mu$m, and 300 $\mu$m, due to the density of surface defects only the smaller devices had a reasonable chance of being defect free. Measured absorption spectra and calculated contrast ratios show that the structures have the potential for efficiency modulation of optical signals in the communications bands. Comparison of the measured results to the simulation results showed the absorption edges of the measured results were at a higher wavelength then expected from simulation using the measured layer thicknesses. The difference can be explained by the uncertainty of the measured layer thicknesses and compositions.

# Chapter 7

# Conclusions

Monolithic integration of photonic devices onto a Si chip is a potential solution to the problems created by electrical interconnects to the continued development of high speed processors. Chip to chip or core to core communications using optical signals provides a way to overcome the bottleneck faced with current metal interconnects. The ability to produced photonic devices in a way that is compatible with current CMOS fabrication processes would allow one to take advantage of the large infrastructure developed for CMOS electronics and could substantial reduce fabrication costs. Integration of epitaxially grown germanium on silicon substrates expands the potential for fabrication of active optical devices operating at the low loss optical fibre wavelengths used in long haul communications within a CMOS compatible fabrication process. A major issue with Ge on Si substrate technologies is the misfit dislocations which occur due to the large lattice mismatch between Ge and Si. For photonics using high Ge content the layers are required to be much thicker than the critical thickness. Lowering the surface defects due to the lattice mismatch is an active area of research. Growth techniques that have been developed using chemical vapour deposition, which lower the defect density substantially include growing on a fully relaxed SiGe buffer, the two-step growth technique, and selective area growth. The growth techniques have allowed the demonstration of high performance Ge on Si photodetectors and modulators.

## 7.1 Conclusions and Future Work

One issue with Ge on Si devices is the combination of the Fermi level of Ge being pinned near the valence band and the high diffusion rate of n-type dopants. Due to

the Fermi level pinning of Ge, Ohmic contacts to n-type Ge require high levels of n-type doping ($N_D > 1 \times 10^{19}\text{cm}^{-3}$). For *in-situ* doped structures the high doping of bottom contact layers will lead to dopant diffusion into higher layers of the structure. This will greatly increase the leakage current through a device and change the electrical and optical properties. Therefore in these cases a process which does not rely on high *in-situ* doping is required. The use of ion-implantation to produce Ohmic contacts to n-type Ge does not require high *in-situ* doping but introduces a large number of unwanted defects into the material. Inserting an interfacial layer can also produce Ohmic contacts to n-type Ge but requires higher *in-situ* doped layers. Yttrium has been demonstrated to be able to produce Ohmic contacts to low doped n-type Ge layers but is less stable, requiring a protective cap layer before exposure to atmosphere. In this work an Ohmic contact to moderately doped ($N_D > 1 \times 10^{18}\text{cm}^{-3}$) n-type Ge was fabricated by the deposition and annealing of a AgSb alloy. The AgSb alloy produces a contact resistivity ($\rho_c$) of $(1.1 \pm 0.2) \times 10^{-5}$ $\Omega$-cm$^2$, which is lower than reported for Yttrium based contacts. The resistivity is higher than other techniques mentioned but benefits from using a simple fabrication process which does not introduce defects or require a highly doped n-type Ge layer.

Precise control of the Ag:Sb ratio and thicknesses was not possible using the tools and materials available. Further research could use sequential deposition of Sb followed by Ag from separate targets without exposure to atmosphere in between to allow independent control of the thicknesses of Sb and Ag that are deposited. Optimization of the thicknesses could lead to improved contact quality and repeatability. Another route that could lead to better contact quality would be an investigation into replacing the Ag with other metals such as Ni which has been shown to form low resistivity NiGe alloys. The contact process was developed for use with n-type Ge contact layers with a doping concentration of $N_D = 1 \times 10^{18}\text{cm}^{-3}$. Investigation of the effect on contact quality of lowering the dopant concentration would allow one to determine the minimum dopant concentration required. Knowing the minimum required dopant concentration in n-type Ge for bottom contact layers would allow one to minimize the issue of dopant segregation during wafer growth and allow for the fabrication of devices requiring Ohmic bottom contacts such as n-type SiGe THz QCLs.

An important component required for integration of photonics onto Si chips is a CMOS compatible modulator. A modulator that operates near 1550 nm would have the benefit of compatibility with existing communications infrastructure which utilize the low loss wavelength region of optical fibres. The QCSE allows the modulation of the absorption spectrum of a quantum well and this effect can be used to design and produce electro-optic absorption modulators. Ge/SiGe MQW QCSE modulators can operate

at lower voltages and with smaller sizes than other previously demonstrated Si compatible modulators. Lower voltage DC offset and swing voltages allow device operation with better energy efficiency. The accuracy of the absorption edge calculations was confirmed by simulating structures that have been presented in the literature. QCSE structures were designs with 10 QWs ranging from 9 nm to 16 nm separated by 11 barriers with widths equal to half the QW width. The barriers are designed to allow the QCSE structures to operate with lower voltages than previously reported designs by reducing the total size of the intrinsic region without reducing the number of QWs. The simulations of the design show that the 16 nm QW structure will provide useful modulation across the entire optical communications C band with a low voltage swing and low DC offset voltages.

The structures of the wafers that were grown differed from the design structures. The structures as grown were measured using TEM and the layer thicknesses were used in simulations to determine the expected absorption of devices with the as grown structure. It was shown that the differences in the as grown structures led to a shift of the absorption to lower wavelengths and a higher voltage requirement.

While the spectra from the simulation accurately matched the absorption edge of the measured spectra for the devices from the literature, the devices fabricated during this study did not match as well. The discrepancy could be resolved by improvements to the simulation which would take into account the uncertainty in the measured layer thicknesses. The measured spectra for both the literature and this thesis show stronger tails in the low energy side of the absorption than found in the simulated spectra. This could be due to absorption in other parts of the device such as the spacers and contacts. This requires further investigation in order to allow a more accurate spectrum calculation.

Photodiode devices were fabricated using the wafers grown by collaborators from Warwick University. The surface of the wafer showed pits which were detrimental to the operation of any device that contained one. Due to the density of the pits only devices with an active area with a diameter less than 100 $\mu$m could be reasonably expected to be free of pits. A number of devices were able to be fabricated which showed good rectifying behaviour. The good devices were wirebonded and an FTIR was used to measure the absorption spectra for various applied voltages by measuring the photocurrent. A QCSE shift was able to be seen from the FTIR measurements and, in order to determine absolute values for the absorption, the photocurrent was also measured using a TLS setup. Contrast ratios over 6 dB at 1495 nm and 4 dB at 1550 nm for 1 V swing voltage were measured with an 11.3 nm QW device.

The fabrication issues did not allow for a full characterization of all of the different wafers. Further research with these wafers could include a complete characterization of each of the designs in both TLS setups and FTIR measurements. Replacement of the large and medium sized devices with smaller devices would allow a higher yield of devices per sample. Creation of devices with larger windows in the top contact would allow for a more accurate measure of the absorption coefficient. Another avenue would be the growth of new wafers which more accurately reflect the original design structure. The thinner barriers and larger QW widths should provide a better contrast ratio at 1550 nm.

In conclusion I believe that the results demonstrated in this work show both a novel method for Ohmic contacts to low doped n-type Ge and advancement in the design and realization of QCSE devices. The Ohmic contact technology developed has the potential to allow previously unrealized technologies such as n-type Ge/SiGe THz QCL to be successfully developed. The improvements made by the QCSE devices in this work increase the possibility of the full integration of Si photonics with Si CMOS electronics.

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