Impact of Intrinsic Parameter Fluctuations in Ultra-Thin Body Silicon-On-Insulator MOSFET on 6-Transistor SRAM Cell

Khairulmizam Samsudin

Submitted to the Faculty of Engineering, Department of Electrical and Electronics in full fulfilment of the requirements for the degree of Doctor of Philosophy in Electronics Engineering

September 2006

Abstract

As CMOS device dimensions are being aggressively scaled, the device characteristic must be assessed against fundamental physical limits. Nanoscale device modelling and statistical circuit analysis is needed to provide designer with ability to explore innovative new MOSFET devices as well as understanding the limits of the scaling process. This work introduces a systematic simulation methodology to investigate the impact of intrinsic parameter fluctuation for a novel Ultra-Thin-Body (UTB) Silicon-on-Insulator (SOI) transistor on the corresponding device and circuits. It provides essential link between physical device-level numerical simulation and circuit-level simulation. A systematic analysis of the effects of random discrete dopants, body thickness variations and line edge roughness on a well scaled 10 nm, 7.5 nm and 5 nm channel length UTB-SOI MOSFET is performed. To fully realise the performance benefits of UTB-SOI based SRAM cells a statistical circuit simulation methodology which can fully capture intrinsic parameter fluctuations information into the compact model is developed. The impact of intrinsic parameter fluctuations on the stability and performance of 6T SRAM has been investigated. A comparison with the behaviour of a 6T SRAM based on a conventional 35 nm MOSFET is also presented.

List of Publications

1. K. Samsudin, B. Cheng, A. R. Brown, S. Roy, and A. Asenov. Impact of body thickness fluctuation in nanometre scale UTB SOI MOSFETs on SRAM cell functionality. In *6th European Conference on Ultimate Integration of Silicon (ULIS)*, pages 45-48, April 2005.

2. K. Samsudin, B. Cheng, A. R. Brown, S. Roy, and A. Asenov. UTB SOI SRAM cell stability under the influence of intrinsic parameter fluctuation. In *35th European Solid-State Device Research Conference (ESSDERC)*, pages 553-556, September 2005.

3. K. Samsudin, B. Cheng, A. R. Brown, S. Roy, and A. Asenov. Impact of random dopant induced fluctuations on sub-15nm UTB SOI 6T SRAM cells. In *IEEE International SOI Conference*, pages 61-62, October 2005.

4. K. Samsudin, B. Cheng, A. R. Brown, S. Roy, and A. Asenov. Integrating intrinsic parameter fluctuation description into BSIMSOI to forecast sub-15nm UTB SOI based 6T SRAM operation. *Solid State Electronics*, 50(1):86-93, January 2006.

5. K. Samsudin, B. Cheng, A. R. Brown, S. Roy, and A. Asenov. Sub-25 nm UTB SOI SRAM cell under the influence of discrete random dopants. *Solid State Electronics*, 50(4):660-667, April 2006.

6. K. Samsudin, F. Adamu-Lema, A. R. Brown, S. Roy, and A. Asenov. Impact of body thickness fluctuation in nanometre scale UTB SOI MOSFETs on SRAM cell functionality. In *7th European Conference on Ultimate Integration of Silicon (ULIS)*, pages 93-96, April 2006.

Acknowledgments

I wish to gratefully acknowledge the enthusiastic supervision of my supervisor, Professor Asen Asenov. His continuous guidance and enthusiasms for semiconductor devices is an inspiration to all. I would also like to thank Dr. Scott Roy, my second supervisor for his comments and useful discussions. I am also grateful for the aid and support from our research group throughout this work, particularly Andrew R. Brown for his support with the 'atomistic' simulator and Dr. Binjie Cheng for his help with compact-level modelling.

I would also like to acknowledge Universiti Putra Malaysia and Malaysia Ministry of Science, Technology and Innovation for support and grant to pursue this research program. The work presented in this thesis, conducted during the last four years would never be possible without their study leave approval and scholarships.

It is a pleasure to thank my wife, Syamsiah Mashohor and my daughter, Amatullah Nazirah Khairulmizam for their understanding and support as I work to complete this thesis. Without their love and patience, this research work would be impossible. Finally, I am also grateful for the encouragement and support from my family back home in Malaysia.

Contents

List of Figures

List of Tables

Acronyms and Abbreviations

6T	6-Transistor
BSIM3	Berkeley Short-channel Insulated-gate field-effect-transistor model version 3
BSIMSOI	Berkeley Short-channel Insulated-gate field-effect-transistor Silicon-On-Insulator model
BTV	Body Thickness Variation
DIBL	Drain Induce Barrier Lowering
EDA	Electronic Design Automation
FD-SOI	Fully Depleted Silicon-On-Insulator
IPF	Intrinsic Parameter Fluctuations
ITRS	International Technology Roadmap for Semiconductors
LER	Line Edge Roughness
LWR	Line Width Roughness
MOSFET	Metal Oxide Semiconductor Field-Effect-Transistor
NMOS	N-channel Metal Oxide Semiconductor
PD-SOI	Partially Depleted Silicon-On-Insulator
PMOS	P-channel Metal Oxide Semiconductor

RDD	Random Discrete Dopants
RDD+BTV+LER	Combination of Random Discrete Dopants, Body Thickness Variation and Line Edge Roughness
RDT	Read Discharge Time
RMS	Root Mean Square
SNM	Static Noise Margin
SoC	System on Chip
SOI	Silicon-On-Insulator
SPICE	Simulation Program with Integrated Circuits Emphasis
SPV	Switch Point Voltage
SRAM	Static Random Access Memory
TCAD	Technology Computer Aided Design
UTB	Ultra-Thin Body
UTB-SOI	Ultra-Thin Body Silicon-On-Insulator
WT	Write Time

List of Symbols

$I_{\text{bit-line}}$	SRAM bit-line leakage current
I_{cell}	SRAM cell leakage current
I_{D}	Drain current
$\langle I_D \rangle$	Average drain current from atomistic devices
I_{D0}	Drain current from ideal device
I_{off}	Off-current
I_{on}	On-current
L	Channel length
L_{a}	Access transistor channel length
L_{d}	Driver transistor channel length
N_a	Channel doping
$N_{s/d}$	Source/Drain doping
r	Cell ratio
S	Subthreshold slope
Si	Silicon
$\mathbf{SiO_2}$	Silicon dioxide

t_{box}	Buried oxide thickness
t_{ox}	Gate oxide thickness
t_{Si}	Body thickness
t_{Si}	Body thickness
V_{D}	Drain voltage
V_{dd}	Supply voltage
V_{G}	Gate voltage
V_{T}	Threshold voltage
$\langle V_T \rangle$	Average threshold voltage from atomistic devices
V_{T0}	Threshold voltage from ideal device
W	Channel width
W_{a}	Access transistor channel width
W_{d}	Driver transistor channel width

Chapter 1

Introduction

1.1 Motivation

The concept of device scaling has been consistently applied over the past three decades, increasing the density, the performance, and reducing cost per function of the corresponding integrated circuits and systems [1]. However, the scaling of conventional device architectures such as bulk MOSFETs are approaching fundamental physical limits. As device dimensions shrink to nanometre regime, the limits of conventional bulk MOSFETs are becoming more pronounced due to increasing short-channel effects causing threshold voltage roll-off, lack of performance due to increasing access resistance, material limitations of conventional gate stack and technological difficulties [2]. Extremely high channel doping is required to control short-channel effects in conventional bulk MOSFET. This presents a challenge in terms of devices fabrication and yields degradation of device performance due to strong ionised impurity scattering [3]. It is therefore necessary to consider new device architectures that can be scaled to smaller dimensions compared to the conventional bulk MOSFETs in order to sustain the growth of the VLSI industry in the forthcoming nano-scale CMOS generations.

One of the most challenging by-products of feature scaling that is proving extremely difficult to manage are the increasing variations of the transistor characteristics due to intrinsic parameter fluctuations. This problem is associated with the fundamental discreteness of charge and matter [4, 5] and cannot be

removed by better processing steps or improved equipment [6]. Important sources of intrinsic parameter fluctuations includes random discrete dopants [5, 6, 7, 8], gate line edge roughness [9, 10, 11] and oxide thickness variations [12]. It has been experimentally demonstrated at device and circuit level that with the continuing scaling of the conventional MOSFETs, the random variation in numbers and positions of discrete dopant atoms in the channel region induce threshold voltage and drain-current fluctuations which adversely affect the circuit performance [13, 14]. These atomic-scale intrinsic fluctuations cannot be eliminated by tighter manufacturing process control and have already become one of the major stumbling blocks to scaling and integration.

The International Technology Roadmap for Semiconductors (ITRS) [1] introduces several novel device architectures to secure the continuation of the MOSFET scaling near the end of the roadmap. Ultra-thin body silicon-on-insulator (UTB-SOI) MOSFETs are one of the promising emerging devices that offer better control of short-channel effects compared to conventional bulk MOSFET. In SOI devices, short-channel effects are controlled by the thickness of the silicon film, thus allowing for gate length scaling below 10 nm [15]. Tolerating low doped or intrinsic channels, UTB devices have negligible depletion charge and capacitance, which yields a steep subthreshold slope. In addition, by dielectrically isolating the active region from the substrate, the SOI technology significantly reduces the junction capacitance contribution to the device capacitive load. Working UTB-SOI transistors with a channel length of 6 nm [15] and body thickness down to 3 nm [16] have already been successfully demonstrated. However, the optimal scaling of the UTB-SOI MOSFETs to such dimensions requires a body thickness in the range of deca-nanometres. At such body thicknesses, and device dimensions local variations in body thickness, geometry variations, due to line edge roughness and random discrete dopants in the source and drain region, will have a dramatic impact on the device parameter variations. Although UTB-SOI transistors can tolerate very low doping concentration in the channel region and therefore are more resistant to intrinsic parameter fluctuations induced by random discrete dopants compared to the conventional MOSFETs, there are unavoidable discrete random dopants in the source/drain regions. While UTB-SOI devices offer potential solution to the ultimate MOSFET scaling, a

reliable early estimate for the magnitude of the corresponding intrinsic parameter fluctuations becomes extremely important. From an integration and systems perspective, an in-depth investigation of realistic UTB-SOI MOSFET behaviour in the presence of intrinsic parameter fluctuations is also important to understand at which technology node such fluctuations will affect the UTB-SOI circuit robustness yield and performance. The increasing device variability is especially critical for SRAM due to the use of minimum geometry devices to minimize cell area in combination with the requirement of adequate stability and high performance.

Until now, six-transistors (6T) SRAM cell sizes have benefited in full from the technology ground rules and device dimension scaling [1]. However, it is now well recognized that the increasing variability in device parameters with scaling due to intrinsic parameter fluctuations [17, 18], can lead to less aggressive scaling of the SRAM cell in future technology nodes. This is bad news since microprocessors and System-on-Chip (SoC) applications require large SRAM arrays occupying an increasing fraction of the chip real estate.

Around the 65 nm technology node, intrinsic parameter fluctuations start to eliminate much of the available noise margin and erode the overall speed in SRAM based on conventional MOSFETs [19]. In general it is expected that UTB-SOI MOSFET SRAMs will outperform conventional MOSFETs due to superior electrostatic integrity. The steeper subthreshold slope permits also a better trade-off between power consumption and performance in the SRAM cell design. The significant reduction in junction capacitance of UTB-SOI MOSFETs also reduces a major component of bit-line capacitance, which is a critical parameter limiting SRAM performance [20]. UTB-SOI transistors can operate without dopant within the channel region, which improves the variability compared to conventional MOSFETs and will have beneficial impact on SRAM yield. However at nanoscale dimensions the discreteness and randomness of the dopants in the source/drain regions together with atomic scale interface roughness and body thickness characteristics fluctuations in combination with LER will introduce variations in the UTB-SOI transistor.

From a circuit and systems point of view, the intrinsic transistor variability must be captured in compact models which can be used in circuit simulators

like SPICE [21]. This will ensure the very important information related to the intrinsic parameter fluctuations is communicated to the circuit and system designers. On the other end, circuit designers must understand what range of variances the device will have to ensure that the circuit will function properly and deliver reasonable yield.

1.2 Aim and Objectives

The aim of this thesis is to investigate the impact of different sources of intrinsic parameter fluctuations in next generation UTB-SOI MOSFETs on the functionality and the performance of the corresponding 6T-SRAM cells. Thus, the first objective of this research is to study, using statistical three-dimensional (3D) numerical simulations, the impact of different sources of intrinsic parameter fluctuations in a family of well scaled UTB-SOI MOSFETs near the end of the ITRS [1] and beyond. The simulations are carried out by the 3D "atomistic" device simulator [6] developed in the Device Modelling Group at the University of Glasgow. The study focuses on the effect of different sources of IPF on important electrical characteristics of the scaled devices. The sources of intrinsic parameter fluctuations which can be separated in simulations will occur simultaneously within a single MOSFET. Thus, their combined effect has also been investigated. This allows to identify the dominant sources of intrinsic parameter fluctuations limiting the scaling of next generation UTB-SOI MOSFETs.

A very important application of the result from 3D statistical simulation is the extraction of parameters for statistical SPICE compact models, which can be used in the statistical analysis and designing of integrated circuits. Therefore, the second objective of this research is to develop a statistical compact model circuit simulation framework which takes into account the intrinsic parameter fluctuations in UTB-SOI MOSFETs. The statistical circuit modelling framework will be able to capture the impact of intrinsic parameter variations in SPICE compact-model parameters in order to study the circuits operating uncertainty. The carefully designed methodology, specifically tailored to capture the impact of different sources of intrinsic parameter fluctuations in standard compact models like BSIMSOI would enable their investigation separately and in combination

without the need for a development of a new statistical compact-model. This methodology which bridges the gap between device-level and circuit-level modelling of intrinsic parameter fluctuations is important for understanding of their impact on the next generation circuits and systems and the development of fluctuation resistant design.

Finally the third objective of this work is to study, using the statistical compact-level circuit simulation methodology, the behaviour of UTB-SOI based 6T SRAM cells under the influence of different sources of intrinsic parameter fluctuations. The comprehensive investigation should lead to a more detailed understanding of the stability and performance of 6T SRAM cell of aggressively scaled UTB-SOI MOSFETs with channel lengths ranging from 10 to 5 nm. The study would also evaluate the advantages and drawback of SRAM cell ratio tailoring as a means for reducing the negative impact of IPF. This study helps to identify key areas for device mismatch optimisation based on future technology trends.

1.3 Thesis Outline

Chapter 2 provides the background for different research areas covered in this thesis. The chapter starts by describing the scaling limitation associated with conventional MOSFETs, and the need for migration to UTB-SOI MOSFETs. In addition, several factors limiting the success of UTB-SOI MOSFET scaling are also discussed. The main sources of intrinsic parameter fluctuations in UTB-SOI MOSFET are then laid out, including random discrete dopants, body thickness variation and line edge roughness. The next section of the chapter gives an overview of the physical device modelling aspects of this thesis. It describes the Glasgow 3D "atomistic" device simulator which has been used in this study of intrinsic parameter fluctuations including the use of quantum corrections. Then, the compact modelling aspects are discussed. Berkeley BSIMSOI [22] SPICE compact models which has been choosen for this work is presented. Finally an overview of the existing SRAM architectures with an emphasis on 6T SRAM cells is presented. The cell structure and operations are discussed as well as issues related to transistors mismatch.

Chapter 3, entitled "UTB-SOI MOSFETs Design and Modeling" contains the results of the physical simulation of intrinsic parameter fluctuations for next generation UTB-SOI MOSFETs. It begins by describing in detail the implementation of each individual source of intrinsic parameter fluctuations available in the Glasgow 3D "atomistic" device simulator. Next the structure and the geometry of the well scaled UTB-SOI MOSFETs with 10 nm, 7.5 nm and 5 nm channel length which will be used throughout this work is presented. These generic device correspond to the 25 nm, 20 nm and 14 nm technology generations. The electrical properties of the scaled devices are investigated. The chapter concludes with statistical investigation of the impact of different sources of intrinsic parameter fluctuations on these UTB-SOI MOSFETs. The three sources of fluctuations considered individually and in combination are random discrete dopants, body thickness variations and line edge roughness.

Chapter 4 entitled "Statistical Circuit Simulation Framework" focuses on developing a methodology to incorporate intrinsic parameter fluctuations information into BSIMSOI [22] compact model. This includes compact model extraction strategy and statistical circuit simulation for the scaled UTB-SOI MOSFETs investigated earlier. The two stage statistical extraction strategy which has been used to build the generic devices compact model library are explained in detail. The quality of the extraction strategy for all of the generic UTB-SOI MOSFETs will be presented. The chapter concludes with the presentation of the extracted compact model parameters correlation.

Chapter 5 entitled "Intrinsic Parameter Fluctuations in 6T SRAM Cells" investigates using SPICE circuit simulation, the impact of random discrete dopants, body thickness variations and line edge roughness on UTB-SOI based 6T SRAM cells with different cell ratio. The compact model library built earlier, which incorporates the electrical characteristic information of intrinsic parameter fluctuations will be used extensively to measure the stability and performance of the 6T SRAM cells. Additionally, the stability of 6T SRAM cells based on conventional 35 nm bulk MOSFETs [19] and the generic UTB-SOI MOSFETs with different cell ratio are also investigated and compared. Analysis of the projected UTB-SOI SRAM cell leakage and static power dissipation are also discussed

Chapter 6 summarises the findings of this research and suggests possible future work that can extend the understanding of the effects of intrinsic parameter fluctuations in next generation MOSFETs devices and circuits.

Chapter 2

Background

The microelectronic industry has benefited enormously from MOSFET miniaturization. Due to the advancement of MOSFET technology and the increase of number of transistors per chip, diverse functions have been incorporated into integrated circuits. As the scaling of device size continues due to the market's demand of high chip-density and reduction of production cost, the physical dimension of transistors such as channel length and gate oxide thickness have also been rapidly scaled down. At the same time the process sequence to build an IC has become very complex, demanding stringent process control to minimize the variations in the transistor parameters. These parameter variations traditionally caused by process variation are now also caused by variations in the atomic structure of the present deca-nanometer CMOS devices.

Therefore one of the challenge of advanced CMOS manufacturing lies in TCAD modelling and simulation of the intrinsic parameter fluctuations for accurately assessing the performance and the yield of the corresponding ICs. The main relevant areas of modelling and simulation includes front-end process simulation, physical device simulation, compact-level models and parameter identification, circuit-level and system level simulation [1, 23]. However, a detailed discussion of all these simulation techniques and the corresponding tools is not the main aim of this chapter. The scope has been limited to cover only the modelling and simulation of device and compact models related to the aim and objectives of this thesis. The subsequent sections in this chapter provide

background and literature review on research aspects covered by this thesis.

This chapter has six main sections. Section 2.1, examines some of the fundamental limitations that that will eventually slow down the scaling of conventional MOSFETs. Section 2.2 provides an overview of the ultra thin-body (UTB) SOI MOSFETs. The structure, advantages and limiting factor of this novel device will be discussed. Section 2.3 introduces the concepts of intrinsic parameter fluctuations (IPF) and the sources of IPF investigated in this work. A brief description of the physical device modeling strategy and simulation tool used in this research will be presented in section 2.4. Section 2.5 provides an overview of the compact modelling strategy and introduces the Berkeley BSIMSOI [22] SPICE compact models used for the circuit simulation of UTB-SOI MOSFET in this work. Finally, section 2.6 will present different designs of SRAM cells with an emphasis on 6T SRAM cells. Discussion of performance advantages that UTB-SOI transistors can provide as well as issues related to transistors mismatch in SRAM cell will also be presented.

2.1 Limitation of Conventional MOSFET Scaling

Over the past three decades, by scaling MOSFET design parameters (voltage, doping concentration, and physical dimensions) with each new generation of manufacturing technology, steady improvements in circuit performance and cost per function have been achieved. However, continued transistor scaling will not be as straightforward in the future as it has been in the past because fundamental materials and process limitations are rapidly being approach. Many reviews have been written about the current state and future prospects for MOSFETs and CMOSs [3, 16, 24, 25, 26]. In particular, many different scaling limitation factors for MOSFETs have been examined and innovations to circumvent fundamental physical barriers have been proposed and discussed. In this section, the current state of understanding of these scaling limits is presented. The result at the end is a growing consensus among the industry and research communities alike, that around the 45 nm technology node and beyond, despite the wide application of technology boosters such as process induced strain for carrier transport enhancement, high-k gate stack and metal gates [1], it will become necessary

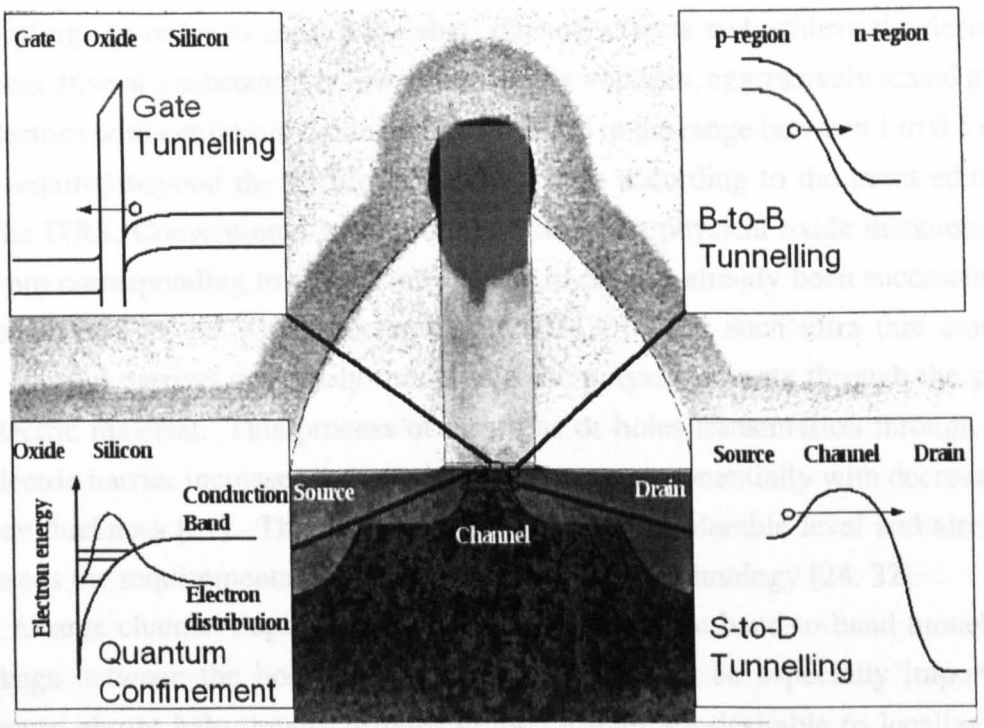


Figure 2.1: Visual illustrations of quantum effects near the Si/SiO_2 interface. Reference [27].

to replace the conventional MOSFETs with novel device architectures such as UTB-SOI and double gate MOSFET.

Conventional MOSFETs scaled down to 15 nm gate lengths have been successfully demonstrated [28]. Scaling below this milestone involves intolerably thin gate dielectrics, unacceptably high channel doping and may require a departure from the conventional MOSFET concepts. This presents a challenge in terms of device fabrication because of a heavy halo implant must be localized close to the surface underneath the gate edge. However, even if this is achievable, the combination of thin gate oxides and heavy doping in conventional MOSFETs, will result in substantial quantum mechanical gate and band-to-band tunnelling [29]. The quantum confinement effects and the three main quantum mechanical tunnelling phenomena, which affect the MOSFET scaling are illustrated in figure 2.1.

Tunneling current through the gate dielectrics is one of the most acute limits

to scaling. In order to control the short channel effects and achieve the desired current drive at a substantially low power supply voltages, aggressively scaled gate dielectrics with equivalent oxide thickness (EOT) in the range between 1 to 0.5 nm are required beyond the 65 nm technology node according to the latest edition of the ITRS. Conventional gate insulator, SiO_2 with physical oxide thickness of 1.2 nm corresponding to four atomic layers of Si, has already been successfully implemented in the 90 nm technology node [30]. For such ultra thin oxides the channel carriers can easily tunnel into the polysilicon gate through the gate dielectric material. This process of electrons or holes transmission through the dielectric barrier increases the gate leakage current exponentially with decreasing oxide thickness [31]. This leakage has reached an intolerable level and already exceeds the requirements of high-performance logic technology [24, 32].

A large channel doping will also inevitably enhance band-to-band tunneling leakage between the body and drain [33]. This will be especially important because abrupt halo doping profiles in the channel are desirable to localize the heavy channel doping whereas abrupt drain doping profiles are desirable for the reduction of series resistance. Together, these requirements will greatly increase band-to-band tunneling, which also contribute to the off-state leakage current in the transistor [16]. Apart from quantum tunneling effects, carrier mobility of bulk device with a heavily doped channel will be severely degraded by impurity scattering. This is particularly noticeable above channel doping concentration of 2e18 cm^{-3} [3].

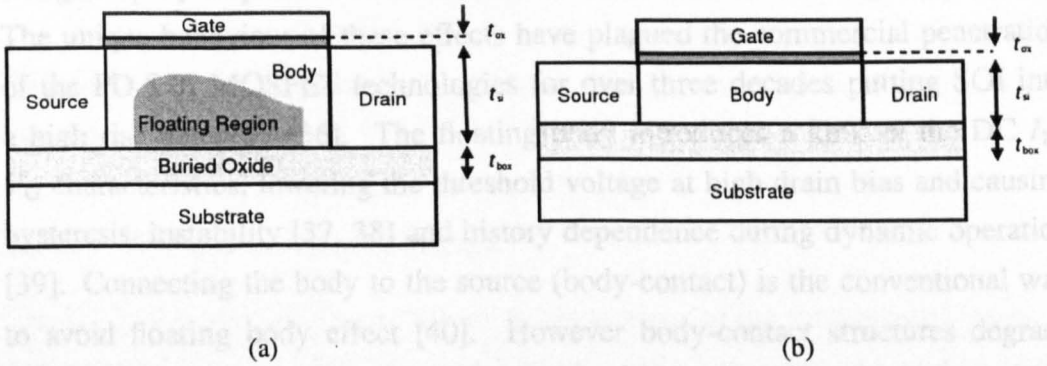
The other possible tunnelling mechanism that can affect the operation of nanometre scale MOSFETs is the source-to-drain tunnelling. The proximity of the source and drain junctions may lead to quantum mechanical tunnelling that will increase the overall transistor leakage current. The effect of source to drain tunnelling current in an 8 nm gate length MOSFET corresponding to the 20 nm technology node has been experimentally demonstrated [34]. According to the technology roadmap such devices will be in production around year 2018.

Aside from fundamental physical limitations, power dissipation will become one of the major factors hampering the integration of the scaled devices and therefore limiting the usefulness of continued scaling [35]. From a VLSI circuits application point of view, the main power dissipation mechanisms are dynamic or

switching power and static power dissipation. The dynamic power is associated with the switching of circuit logic states and is in direct proportion to the rate of computation. Therefore it can be adjusted to meet application power requirement by adjusting the computation rate. Static power dissipation is associated with leakage mechanism within device or circuit and therefore difficult to control. The severity of the problem rapidly increases as scaling proceeds. As a result of subthreshold slope degradation including source-to-drain tunnelling for a given off-state leakage current specification, the threshold voltage must be raised. However, increasing the threshold voltage while scaling the power-supply voltage reduces the drive current of the device. A feasible way of addressing the power issue is to improve the sub-threshold gradient of the transistor. However, as the conventional transistor scales, and the channel doping increases to support the electrostatic integrity, the sub-threshold slope is degraded. Intrinsic parameter fluctuations due to the high channel doping are also among the main limitations to scaling.

2.2 UTB-SOI MOSFET Devices

In the previous section, the fundamental physical limitation of conventional bulk MOSFET have been presented. It was highlighted that conventional transistors with gate length below 10 nm are increasingly difficult to design due to severe short channel effects, quantum tunnelling, power dissipation and the resulting loss of performance. Therefore, it is very important to consider alternative device architectures that do not have some of the limitations of conventional MOSFETs and that may be manufactured with minimal changes to process technology. Novel MOSFET structures such as UTB-SOI and double-gate MOSFET can be scaled more aggressively than the conventional bulk structure and, hence, may be adapted for high performance logic technology production as early as the 65 nm technology node [2]. That is why the latest edition of the ITRS expects that UTB-SOI MOSFET will phase out bulk MOSFET below 22 nm gate length while double-gate MOSFET is expected to be introduced below 16 nm gate length [1]. This work concentrates solely on the modelling and simulation of UTB-SOI MOSFET. In this section a brief description of the basic properties, the



(a) (b)

Figure 2.2: Schematic diagram of (a) partially-depleted SOI and (b) fully-depleted SOI MOSFET.

generic structure and the significant advantages of SOI MOSFETs is presented. Further design considerations necessary to circumvent scaling limitations will be presented.

2.2.1 SOI Basic Properties and Structure

The structure of the classical SOI transistor is similar to the structure of a conventional MOSFET with the exception of the insertion of a buried oxide in the silicon substrate. The SOI technology dielectrically isolates components and in conjunction with the lateral isolation, reduces the effective area capacitance between the diffusion junction and the substrate compared to bulk MOSFET. This is mainly due to the buried oxide layer which is much thicker than the depletion regions and has lower dielectric constant than silicon. As a result, at identical dimensions SOI circuits are faster than bulk MOSFET circuits because of the reduced junction capacitance.

There are two flavours of the SOI transistors, partially depleted (PD) and fully depleted (FD). Typical PD-SOI and FD-SOI device structures are shown in figure 2.2(a) and figure 2.2(b) respectively. PD-SOI have thicker silicon body than the maximum gate depletion width while FD-SOI transistor use a thin silicon body so the depletion layer extends through the entire body film.

The initially electro neutral floating region in PD-SOI MOSFET can be charged up by impact ionization currents which leads to floating body effects. The unique behaviour of these effects have plagued the commercial penetration of the PD-SOI MOSFET technologies for over three decades putting SOI into a high risk category [36]. The floating body introduces a kink in the DC I_D-V_G characteristics, lowering the threshold voltage at high drain bias and causing hysteresis, instability [37, 38] and history dependence during dynamic operation [39]. Connecting the body to the source (body-contact) is the conventional way to avoid floating body effect [40]. However body-contact structures degrade packing density and forces redesigning when remapping bulk chip design to SOI technology [41]. The design of PD-SOI MOSFETs is similar to the design of bulk MOSFETs and faces the same scaling limitations [42] and shifts the interest towards FD-SOI.

Advances in SOI process manufacturing and demand for higher integration density, a smaller die area and a better performance directed the trend toward fully-depleted SOI. The advantages include virtually undoped channel, improved subthreshold slope and reduced random dopant induced parameter variations, reduction of floating-body effect and dynamic stability without body-contact [43]. FD-SOI MOSFETs are promising devices for low-voltage, low-power and high-speed application due to better suppression of short-channel (SCE) and floating-body effects.

Ultra-thin body (UTB) SOI is an extension of FD-SOI. The main difference between the two is the silicon layer thickness. The silicon layer thickness for UTB-SOI transistors is usually less than 10 nm [44]. However, the scaling of the UTB single and double gate transistors beyond 10 nm channel length will require body thickness below 5 nm [45]. UTB-SOI transistors are expected to deliver a solution to the difficult challenge facing the scaling of conventional MOSFETs to deep nano-scale dimensions [46]. The salient features of the UTB-SOI MOSFET are control of short-channel effects by device geometry, as compared to conventional bulk, where the short-channel effects are controlled by doping (channel doping and/or halo doping). The reduced short-channel effects allow scaling to shorter channel lengths for identical gate oxide thickness compared to bulk MOSFET [47], a better subthreshold slope which allows for

a larger gate overdrive at the same power supply and the same off current, better carrier transport since UTB-SOI devices operates at lower vertical field and Coulomb scattering is negligible as the channel is virtually undoped [29]. Reduction of channel doping also reduces the drain-to-body and band-to-band tunneling leakage current.

2.2.2 Design Considerations

The UTB-SOI MOSFETs provide solutions to some of the fundamental issues of conventional bulk MOSFET scaling. Unfortunately, the aggressive scaling of the gate dielectric and the small silicon film thickness needed at short channel length to maintain the electrostatic integrity are prohibitively difficult to manufacture. New approaches to gate stack engineering, source/drain engineering and channel engineering are needed for the alleviation of these problems and will be discussed in this subsection.

UTB-SOI devices require advanced gate stack to reduce the gate tunneling current and the gate capacitance degradation due to polysilicon depletion [2]. With the SiO_2 gate dielectric thickness approaching scaling limits, researchers have been exploring several alternative gate stacks for UTB-SOI MOSFET, including the use of high permittivity gate dielectric (high-k) and metal gate [2, 24, 48]. Successful introduction of high-k depends upon achieving high layer uniformity stability, integration with other Si processes, minimal/controlled reactions with Si and the gate electrode [2], and low fixed-charge, defect, and trap densities in the insulator and at the interface between the insulator and the Si substrate [49]. The incompatibility of high-k dielectric materials with the polysilicon traditionally used for the gate electrode also require alternative gate materials [50]. The use of a metal gate material opens up the opportunity to choose the work function of the gate. In UTB-SOI MOSFET, where the short-channel effects are controlled by the device geometry, the threshold voltage is determined mainly by the gate work function. Therefore, the choice of the gate electrode is particularly important. The use of a lightly doped channel requires the gate work function to be tunable in the range between 4.4 and 5.0 eV to provide means for adjusting the threshold voltage [16].

In the UTB-SOI device structure, the body thickness is reduced with scaling to suppress short channel effects. However, the increasing access resistance of the source and drain regions could limit the transistor drive current [15, 29]. Continued scaling of channel length decreases the channel resistance and increases the impact of access resistance on saturation current. A significant part of the access resistance is associated with the contact resistance which is not scalable [51]. The solution to the drive current reduction due to access resistance is to use raised source/drain, which increase the effective thickness of the junctions and hence the junction conductance [52]. Devices with raised source/drain exhibit superior drive currents, up to 50 percent larger compared to the non-raised source/drain counterparts [29]. An alternative approach is to reduce the series resistance in the thin body by introducing salicide (self aligned silicide) source/drain region [53].

Apart from the increase in series resistance arising from ultra-thin junctions discussed above, the fabrication of uniform thin body layers is extremely difficult. There is a lot of scepticism about UTB-SOI MOSFET ability to be manufactured in a large-scale production. However, experimental result shows relatively good control of body thickness in the range between 6 to 10 nm [54]. While MOSFET scaling can be extended with the UTB-SOI device structures, innovative design considerations and improve processing technology, an ultimate limit associated with intrinsic parameter fluctuations will eventually be reached. In the following section the main sources of intrinsic parameter fluctuations in UTB-SOI MOSFET will be presented.

2.3 Intrinsic Parameter Fluctuations

In the past, the mismatch in the characteristic of transistors in integrated circuits were associated with macroscopic manufacturing process fluctuations. These are mostly related to the process equipment used in various processes such as oxidation, ion implantation, annealing, deposition and etching. As the devices are scaled to nanometre regime, the intrinsic variations associated with the discreteness of charge and matter start to play a fundamental role even with perfect processing conditions. The atomistic nature of the deca nanometer and

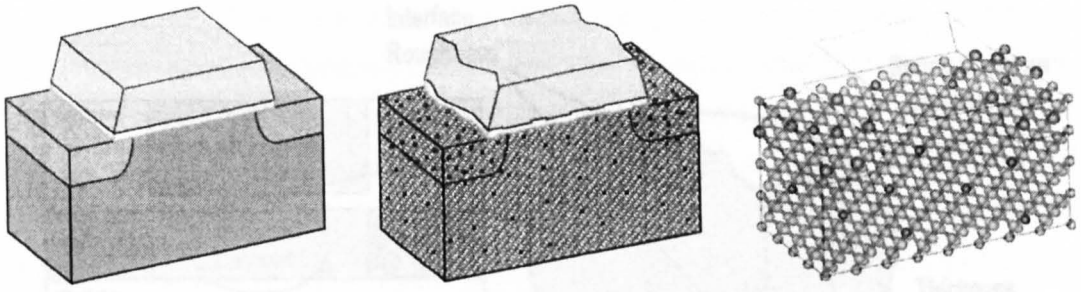


Figure 2.3: The evolution towards atomistic devices concepts. (a) MOSFET with continuous ionised dopant charge, smooth boundaries and Si/SiO_2 interfaces. (b) Sketch of 22 nm MOSFET required for 45 nm technology node with random discrete dopants, rough interface and line edge roughness (c) Impression of 5 nm MOSFET with the silicon crystal lattice superimposed. Reference [55].

nanometer scale MOSFETs is illustrated in figure 2.3. The transistor with sub-50 nm dimensions in figure 2.3(b) and the transistor with sub-10 nm dimensions in figure 2.3(c), can no longer be described, modelled or simulated based on the traditional assumptions of continuous dopant distribution, smooth interfaces and straight gate edges, illustrated in figure 2.3(a). The three main sources of intrinsic parameter fluctuation that are considered in this work include random discrete dopants (RDD), body thickness variations (BTV) and line edge roughness (LER). Ultimately, scaling of UTB-SOI MOSFETs is susceptible to the above sources of intrinsic parameter fluctuations

2.3.1 Random Discrete Dopants

According to the ITRS [1], MOSFETs with 7 nm gate lengths are expected to be in mass production around 2018. Such devices, similar to the one in figure 2.3(c), will have approximately 10 to 15 silicon atoms along the channel length and the position of each silicon, dopant or insulator atom is likely to have significant microscopic impact on the device characteristics. Conventional MOSFETs at such dimensions require a high doping concentration in the channel in order to suppress short channel effects. These dopants are introduced by implantation process and activated using annealing. The overall effect is a random distribution of position

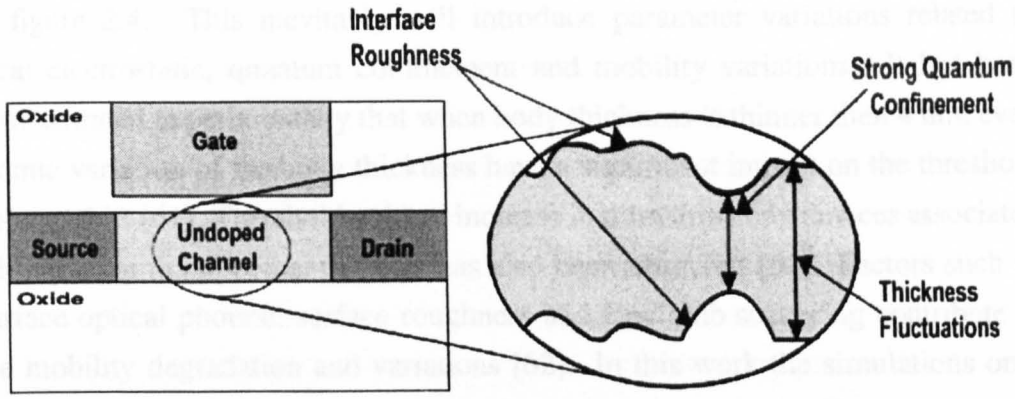


Figure 2.4: Body thickness fluctuations due to interface roughness between the silicon and oxide layers.

and number of dopant atoms for each device. Aside from its adverse effect on device performance the high doping concentration will introduce intolerable IPF. Random discrete dopants of conventional MOSFETs are one of the source of IPF that have been experimentally demonstrated [5] and studied theoretically [8, 56, 57]. However, the impact of random discrete dopant has a different nature in UTB-SOI devices as they are more tolerant to low doping concentration in the channel. The use of virtually undoped channel in UTB-SOI MOSFETs reduces threshold voltage sensitivity and proved to be advantageous even at very short channel lengths [58], but the effect of unavoidable random dopants in the source/drain region has not been well understood. RDD simulation in this work only considers dopants in the source/drain regions of the UTB-SOI MOSFETs.

2.3.2 Body Thickness Variations

The scaling of the UTB-SOI MOSFET to nanometer regime near the end of the ITRS involves aggressive reduction of the silicon body thickness (t_{si}). This is a concern from a manufacturing stand point because of the sensitivity of threshold voltages to variation in the body thickness across the wafer [59, 60]. At the same time, atomic scale roughness of the Si/SiO_2 interface will introduce significant intrinsic parameter fluctuations in UTB-SOI MOSFETs resulting in a unique pattern of the body thickness in each individual device as illustrated

in figure 2.4. This inevitably will introduce parameter variations related to local electrostatic, quantum confinement and mobility variations. It has been demonstrated experimentally that when body thickness is thinner then 4 nm, even atomic variation of the body thickness have a significant impact on the threshold voltage shift [61]. Threshold voltage increase in ultra thin body devices associated with quantum confinement effects has also been observed [61]. Factors such as surface optical phonon, surface roughness and Coulomb scattering contribute to the mobility degradation and variations [62]. In this work the simulations only capture fluctuations induced by the electrostatics and quantum effects.

2.3.3 Line Edge Roughness

Ideal MOSFETs are considered to have a straight gate edges as illustrated in figure 2.3(a). However in real devices, the gate is prone to line edge roughness (LER) caused by tolerances inherent to materials and tools used in the lithography processes. As a result of gate LER, gate geometry will vary from transistor to transistor. Since the drain current is related to the gate geometry the overall current may vary resulting also in threshold voltage variation from transistor to transistor [11]. At the same time, the doping distribution near the p-n junctions which closely follows the gate shape introduces variations in the effective channel length. In the past, LER had little impact on device operation because the gate length was much larger compared to the roughness of the gate edges. However, with UTB-SOI transistors gate length scaled to 10 nm, the contribution of LER to overall IPF is becoming significant.

2.4 Physical Device Modeling

A proper understanding of the electrical properties of advanced semiconductor devices requires adequate device simulations. The ability to predict the electrical device characteristic reduces design cost and manufacturing delay and provides an opportunity to assess capability of devices and circuits using technology computer aided design (TCAD) and compact model extraction. Device simulation is also an important tool in the investigation of new materials and their impact on device

performance.

The intrinsic parameter fluctuations are three dimensional (3D) in nature, and therefore, to correctly capture their effects full scale 3D simulation should be carried out. In this work, the Glasgow 3D "atomistic" device simulator has been employed [10, 56, 63, 64] to investigate random discrete dopants, body thickness variations and line edge roughness in UTB-SOI MOSFETs. The simulator is based on the drift diffusion (DD) approach, self-consistently solving the Poisson and the current continuity equations at room temperature. The Poisson equation describes the charge distribution and the boundary conditions in the solution domain, while the continuity equation determines the current and carrier concentration distributions. The DD system only works in quasi equilibrium where the electric field varies slowly and the velocity is locally related to the electric field. Therefore DD approach is perfectly adequate to analyze fluctuations in threshold voltage and in the subthreshold slope which are dominated by device electrostatics.

Quantum mechanical effects have a big influence on the operation of nanometer scale MOSFETs and on their parameters and electrical characteristics. The quantum mechanical effects affecting the MOSFET operations are mainly the quantum confinement and tunneling. The quantum mechanical tunneling effects have been discussed previously in section 2.1. The quantum confinement effects occur when the carriers in a semiconductor are confined by a potential well in a constrained region. Quantum confinement in the channel has a profound impact on both the amount of charge which can be induced by the gate electrode through the gate oxide and the profile of channel charge in the direction perpendicular to the surface. The quantum confinement effects are included in our 3D simulations using the density gradient formalism [56]. The simulations of intrinsic parameter fluctuation in this work will only consider electrostatic and quantum confinement and do not include variations introduce by quantum confinement scattering and quantum tunneling.

The extremely small body thickness considered in this work results in strong quantization in the direction normal to the interface. This quantization influences the device behaviour by increasing the threshold voltage and decreasing the drive current. In the Glasgow "atomistic" simulator, quantum mechanical effects are

included using quantum corrections based on the Density Gradient approach [56]. The quantum corrections significantly improve the accuracy of the drift diffusion simulation of nanoscale MOSFETs when quantum confinement effects influence the threshold voltage and the overall device performance.

2.5 Compact Circuit Modeling

In circuit design, engineers cycle between design and verification, searching for a design that complies with a set of specifications by performing circuit simulations that rely upon compact models. The purpose of compact modeling is to provide simple, fast and accurate analytical representations of the MOSFET terminal electrical characteristic. The models are desired to be physical in order to capture and reflect the real process and device characteristics with good accuracy and to be able to reasonably project the device behaviour. With a solid physical foundations, a compact model coupled to physically meaningful extraction strategy can be used for device understanding, evaluation, optimization and scaling prediction. Compact models are characterized using data measured from manufactured test chips or simulated using process and/or device simulators. Consequently such compact models are a critical link in the translation of MOSFET process properties into integrated circuit performance.

2.5.1 BSIMSOI

Compact models for SOI MOSFET devices have been developed by the microelectronic industry and in academia over the past few decades [66, 67, 68]. However, among the reported models, BSIMSOI [22] has been of great interest [69, 70] and has played an important role in the semiconductor manufacturing companies [40, 65]. BSIMSOI is built on top of the BSIM3 [71], a well known accurate and predictive bulk MOSFET model, that allows important MOSFET device physics to be shared. However, BSIMSOI is designed as a unified compact model that could model both fully-depleted and partially-depleted SOI devices. Figure 2.5 illustrates the circuit elements of BSIMSOI. When an ideal FD mode for BSIMSOI is enabled, a body-source built-in potential lowering term which is

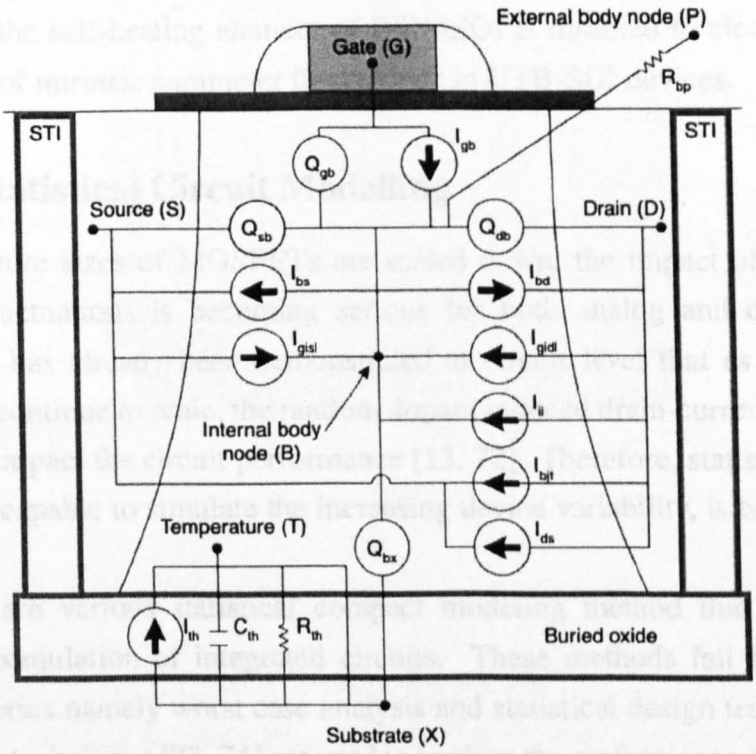


Figure 2.5: Schematic diagram of an SOI transistor, ilustrating the elements present in BSIMSOI for both partially-depleted and fully-depleted SOI MOSFET. Model is shown without source and drain parasitic elements. Reference [65].

a measure of the floating-body behavior of SOI devices is introduced [22]. At the same time, calculation of body node and body current/charge (i.e., heating-free impact ionization current, diode current, gate induced drain leakage and gate-to-body tunneling), which is essential to the partially-depleted model is skipped. Self-heating element in BSIMSOI exists for both FD and PD mode. Self-heating refers to the temperature rise that can occur if excessive heat energy builds up in the SOI body before being dissipated through the buried layer in the substrate. In this work, the self-heating element of BSIMSOI is disabled to clearly illustrate the impact of intrinsic parameter fluctuations in UTB-SOI devices.

2.5.2 Statistical Circuit Modelling

As the feature sizes of MOSFETs are scaled down, the impact of process and intrinsic fluctuations is becoming serious for both analog and digital circuit design. It has already been demonstrated at circuit level that as conventional MOSFET continue to scale, the random dopant induced drain-current fluctuations adversely impact the circuit performance [13, 72]. Therefore, statistical compact modeling, capable to simulate the increasing device variability, is becoming very important.

There are various statistical compact modeling method that are used for statistical simulation of integrated circuits. These methods fall broadly under two categories namely worst case analysis and statistical design techniques. The worst-case techniques [73, 74] are used to explore the performance at the nominal, best and worst case process corners. Previously, this analysis is the industry's de facto standard in statistical modelling that can only be use to verify circuit design at the extremes of manufacturing process variation. The statistical design techniques perform parameter extraction procedure for many individual sample devices, then statistically analyzing the resulting sets of the parameters obtained [75, 76, 77, 78]. This approach could create unrealistic device behaviour and may not capture all aspects of the impact of intrinsic parameter fluctuation sources on the device behaviour. Moreover, compact model parameter inter-correlations are completely neglected, and produces circuit performance predictions that are either overly pessimistic or optimistic.

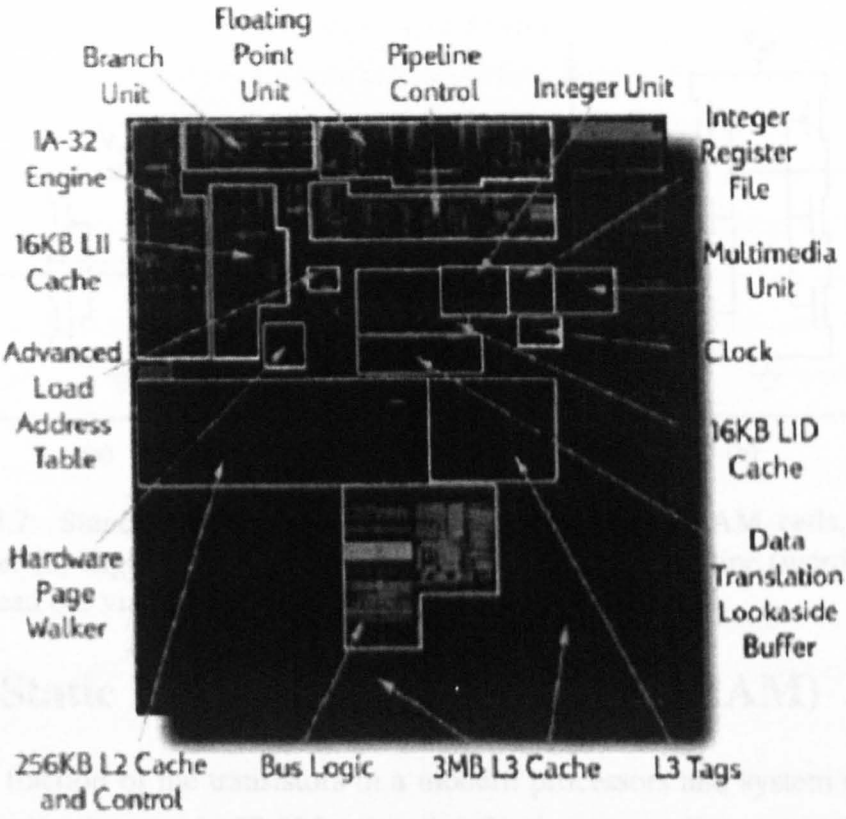


Figure 2.6: Intel Itanium 2 processor overview. Courtesy of [81].

For the design of UTB-SOI circuits that are efficient and remain robust in the presence of intrinsic fluctuations, a new statistical circuit simulation methodology is required. The methodology should be able to transfer the results of the Glasgow 3D atomistic simulator into current EDA tools so that an accurate impact of intrinsic parameter fluctuations on circuit can be investigated. This integration improves the accuracy of BSIMSOI for modelling UTB-SOI devices since its native parameters do not capture the intrinsic parameter fluctuations induced device behavior very accurately in the nanometre regime [79, 80].

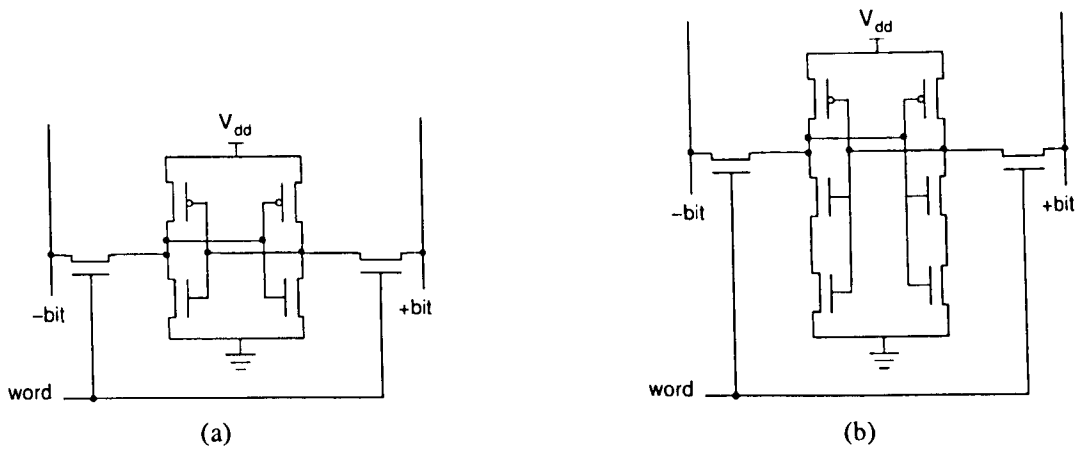


Figure 2.7: Standard configuration of high-performance SRAM cells. (a) Six transistor. (b) Eight transistor. Cell is addressed by the word-line (word) and the data is read out via the bit-line pair (±bit).

2.6 Static Random Access Memory (SRAM)

A large fraction of the transistors in a modern processors and system on a chip (SoC) applications are in SRAM, impacting the density, performance and standby power of the entire chip. Figure 2.6 illustrates that the cache structures constitute a large portion of the Intel Itanium 2 microprocessor real estate. The key to the microprocessor cache market is high performance, high stability and small area. There are several different configuration of SRAM in use in these systems, with different structure and features.

The basic SRAM cell is made up of two cross coupled inverters with several variations. Two SRAM frequently investigated for high performance applications are depicted in figure 2.7. A typical high-performance application SRAM uses the standard six-device (6T) cell configuration illustrated in figure 2.7(a) [82, 83, 84]. Although, the eight-transistors SRAM illustrated in figure 2.7(b), provides a much greater enhancement in stability by eliminating cell disturbs during a read access, the accommodation of two additional transistors causes an area penalty of 30 percent compared to 6T configuration [85]. With excellent performance and stability the six-transistors SRAM has been dominant even though the area has been comparatively very large [24, 86, 87].

SOI based 6T SRAM outperforms conventional bulk ones due to significant reduction of collective device junction capacitance. Its benefit is most exemplified in the differential pair bit-line topology illustrated in figure 2.7(a) as the bit-lines is connected to millions of source/drain junctions and the corresponding capacitance constitutes a sizable portion of the total bit-line nodal capacitance [20]. Improvement in the range between 10 to 30 percent for PD and FD SOI have been observed [82, 83], while 16 percent reduction of chip area has been achieved [82]. Recently a UTB-SOI based 6T SRAM cell with 50 nm gate length transistors has been successfully demonstrated [88].

As memory begins to dominate chip area in high performance applications, SRAM has become the focus of technology scaling [89]. Traditionally, SRAM cell size has scaled in accordance with technology ground rules; however, with the growing importance of variability, it is feared that this may no longer be possible. As minimum gate length and width devices are used to minimize cell area, SRAM is most susceptible to both process induced variations in device geometry and intrinsic parameter fluctuations [90]. These can result in mismatch between the neighboring transistor in a cell. Any mismatch between the devices within a cell degrades the stability of the cell and might as well cause failure. As the scaling of MOSFETs is pushed into the nanoscale regime, the issue of intrinsic parameter fluctuations induced device mismatch is becoming an equal concern for both analog and digital circuits [13, 72].

The impact of random discrete dopants on SRAM cell have been widely investigated for conventional bulk MOSFET using analytical models [17, 18, 19, 79] as well as experimental [13]. However, the impact of each source of IPF on UTB-SOI device and circuit has not been thoroughly investigated. This investigation will be one of the main focus of this thesis.

Chapter 3

UTB-SOI MOSFET Design and Modelling

3.1 Introduction

Conventional MOSFETs are becoming increasingly difficult to design and manufacture due to severe short channel effects, gate oxide tunnelling, power dissipation and intrinsic parameter fluctuations. The continued aggressive scaling of leading edge MOSFETs driven by the increasing density, performance and cost per function expectations, pushes the CMOS technology into an increasingly difficult manufacturing domain below the 65 nm technology generation [1]. Therefore, it is very important to consider alternative device architectures that are more tolerable to some of the limitations of conventional MOSFETs, and that may be realised with minimal change to process technologies. To meet these challenges, both industry and academic communities are pursuing non-classical CMOS technologies with new materials and new device architectures; including ultra-thin body silicon-on-insulator (UTB-SOI) devices after the 65 nm generation and double gate (DG) devices towards the 40 nm generation, according to the 2005 edition of the ITRS.

Working UTB-SOI MOSFETs with a gate length of 6 nm [15] and body thickness down to 3 nm [16] have already been successfully demonstrated. However, it is predicted that at such channel lengths intrinsic parameter

fluctuations will become the critical source of device characteristic mismatch and therefore of profound industry importance. In this chapter the sensitivity of several important electrical parameters (V_T, I_{off} and I_{on}) to intrinsic parameter fluctuations (IPF) has been studied using numerical device simulation. The UTB-SOI MOSFETs are designed to closely match the requirements of the International Technology Roadmap for Semiconductors (ITRS) for high-performance devices in the 25 nm, 20 nm and 14 nm technology generation, which correspond to 10 nm, 7.5 nm and 5 nm channel length devices respectively. The simulation results will be used in the following chapters to predict the impact of IPF on 6-transistors UTB-SOI SRAM cells via circuit simulation. The simulated devices have a simple generic structure with continuously adjustable work functions. Three sources of IPF are taken into account in the analysis: Random Discrete Dopants (RDD), Body Thickness Variation (BTV), and Line Edge Roughness (LER). RDD fluctuations are associated with the discrete nature of the dopant atoms and their location in the crystalline lattice. BTV is associated with the atomic structure of the thin-body Si and the top and bottom oxide layer interfaces, LER is introduced into fabricated devices though the lithographic and etching processes.

This chapter has four main sections. Section 3.2 discusses the overall structure of the device simulation strategy implemented using the three-dimensional (3D) Glasgow atomistic device simulator, and the principal concepts for each source of IPF simulated. Section 3.3 provides a brief description of the generic UTB-SOI structure used throughout this work. Results describing the impact of each individual and combined source of IPF on UTB-SOI device parameters are presented in section 3.4. The chapter summaries are presented in section 3.5.

3.2 Simulation Approach

In order to investigate the impact of intrinsic parameter fluctuations on UTB-SOI MOSFETs, the Glasgow device simulator has been employed [55, 63]. This three-dimensional atomistic device simulator is based on the drift diffusion approach to solution of the semiconductor equations (Poisson and current continuity), employing density gradient quantum corrections. The simulations only capture

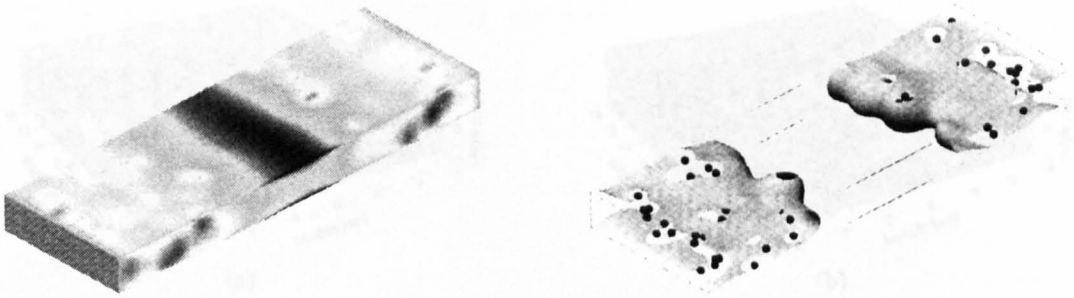
fluctuations induced by electrostatics and quantum confinement effect, and do not include transport variation due to scattering from different impurity and body thickness configurations effects or tunnelling through the gate oxide.

The simulation of IPF shifts the paradigm of traditional device simulation into the statistical domain. In the presence of "atomistic" variations it is inadequate to simulate a single device in order to characterise all macroscopically identical but microscopically different devices realisations. It becomes necessary to simulate a statistically significant sample of devices. The simulation results in general follow closely a normal distribution. This allows a meaningful statistical analysis by estimating and comparing the mean values and standard deviations of basic design parameters such as threshold voltage, off-current and on-current for the whole ensemble of devices of a particular ITRS technology node. The UTB-SOI MOSFET device structure and design will be discussed in section 3.3. In this section, the simulation concepts for including each source of IPF in the 3D Glasgow device simulator will be presented.

3.2.1 Random Discrete Doping

One major advantage of UTB-SOI is the tolerance to very low doping concentrations in the channel. This minimises the impact of intrinsic parameter fluctuations caused by random discrete channel dopants. However, unavoidable random discrete dopants in the source/drain regions will still result in nanometer scale variations of the effective channel length [6] and variation in the source/drain access resistance both contributing to variations in drive current. Thus, the impact of RDD has a different nature in UTB-SOI devices compared to their bulk counterparts.

RDD simulation in this work only considers dopants in the source/drain regions of the UTB-SOI MOSFETs. Although the most realistic way for introducing the random source/drain doping distributions into the atomistic simulations would be the use of the output from a Monte Carlo process simulations [91, 92], here we apply a simpler approach. Given the continuous doping distribution obtained from conventional process simulation tools, the probability that there is a dopant in each cell of the 3D simulation mesh is



(a) (b)

Figure 3.1: A typical simulation domain for a 10×10 nm channel UTB-SOI MOSFET due to random discrete dopants at threshold. The gate and buried oxide is removed to show the fluctuations in (a) electrostatic potential and (b) carrier concentration contour at the source/drain and channel interfaces. The actual location of random discrete dopants in the source/drain regions is also illustrated.

calculated. Then, using a rejection technique, the dopants are placed randomly in the source/drain regions [6]. The doping concentration in the channel region has a continuous distribution with a doping concentration of 10^{14} cm^{-3}.

A typical potential distribution obtained from RDD simulation of a 10 nm UTB-SOI MOSFET is illustrated in figure 3.1(a). The heavily doped source and drain regions are clearly visible in the potential landscape. Strong potential fluctuations at the source/drain and channel interface associated with the discrete dopants can be observed. The equi-concentration contour in figure 3.1(b) highlights the basic features of the discrete dopants in the source/drain region. The discrete dopants render unusable the concept of a metallurgical junction introducing variation of effective channel length across the width of each simulated UTB-SOI MOSFET. Although the fluctuations in a conventional bulk MOSFET parameters are dominated by the randomness of dopants in the channel region [6], atomistic doping in the source and drain of UTB-SOI will introduce variations in the effective length of the channel, even for a perfectly defined gate pattern.

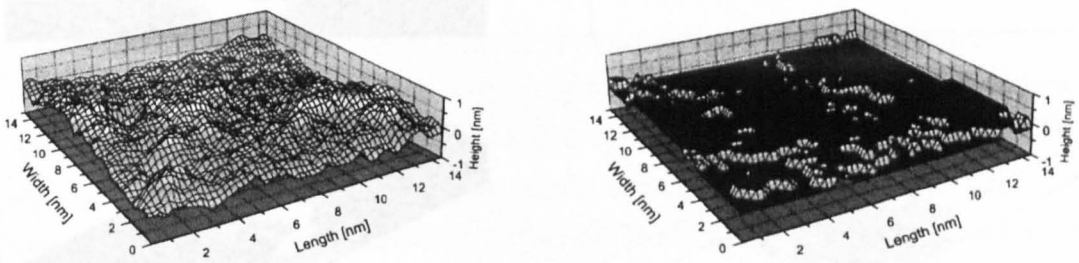
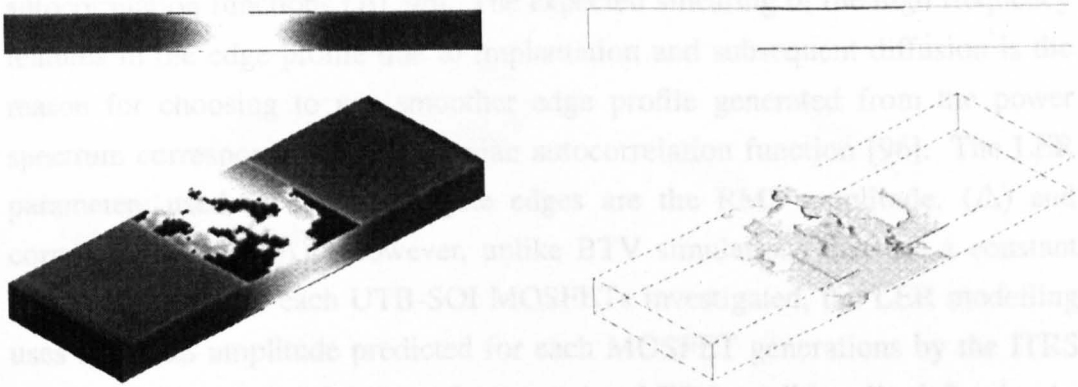


Figure 3.2: (a) Rough surface generated from the Fourier synthesis technique ($\triangle$=0.3 nm, Λ=3 nm) and (b) the surface quantised to $\pm$0.15nm to give the actual interface used in simulations. Reference [64].

3.2.2 Body Thickness Variation

It has been experimentally demonstrated [61] that when silicon body thickness is reduced below 4 nm, slight (even single atomic layer) body thickness variation have a significant impact on the threshold voltage and carrier mobility of UTB-SOI MOSFETs. At such thickness, the atomic scale roughness of the top and bottom Si/SiO_2 interfaces, on the scale of $\pm$1 atomic layer ($\approx$0.3 nm), will introduce appreciable variation in the silicon body thickness. Body thickness variation is introduced into simulations using statistically generated interface roughness patterns with RMS amplitude, ($\triangle$) of 0.3 nm and correlation length, (Λ) of 1.8 nm for the top and bottom Si/SiO_2 interfaces. The Fourier synthesis technique used to generate the random interfaces [12] utilises a power spectrum which corresponds to an exponential autocorrelation function [64]. Figure 3.2 shows a typical rough interface generated using this approach, and the same surface digitised to $\pm$0.15 nm in respect of the originally position of the smooth interface in the simulations.

When studying the impact of body thickness variations, it is important to include quantum confinement effects which push the inversion layer away from the rough interface and also introduce variations in the position of the ground state depending on the local body thickness [93, 94]. In this work the simulations only capture fluctuations induced by the electrostatics and quantum effects, and do not include variations in the quantum confinement scattering introduced



(a) (b)

Figure 3.3: A typical simulation domain for a 10×10 nm channel UTB-SOI MOSFET with t_{si}=2.5 nm due to body thickness variations at threshold. The gate and buried oxide is removed to show the fluctuations in (a) electrostatic potential and (b) carrier concentration contour at the top and bottom Si/SiO_2 interfaces. The silicon body thickness is also illustrated at the top of the images.

by variations in the effective quantum potential. Typical potential and carrier concentration distributions obtained in the simulation of a 10×10 nm channel UTB-SOI MOSFET are illustrated in figure 3.3 with the gate and buried oxide removed. The silicon body thickness is 2.5 nm and illustrated in the same figures. The potential fluctuations associated with the body thickness variations are visible in figure 3.3(a). The variation in carrier concentration near the top and bottom interface due to the surface roughness and the corresponding body thickness variation is clearly depicted in figure 3.3(b).

3.2.3 Line Edge Roughness

The contribution of line edge roughness in the gate pattern definition to the variation of electrical parameters will be significantly increased below the 80 nm technology generation [95]. In this work the investigation of LER is carried out by device simulation where the nominally straight edges gate is replaced by randomly generated rough line pattern. The LER modelling approach used to generate random junction patterns is based on a Fourier synthesis technique and generates gate edges from the power spectrum corresponding to Gaussian

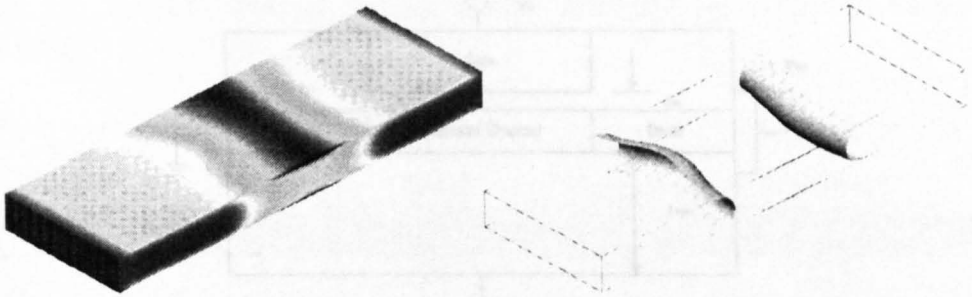
autocorrelation functions [10, 96]. The expected smearing of the high frequency features in the edge profile due to implantation and subsequent diffusion is the reason for choosing to use smoother edge profile generated from the power spectrum corresponding to a Gaussian autocorrelation function [96]. The LER parameters used to define the gate edges are the RMS amplitude, (Δ) and correlation length, (Λ). However, unlike BTV simulations that use a constant RMS amplitude for each UTB-SOI MOSFETs investigated, the LER modelling uses the RMS amplitude predicted for each MOSFET generations by the ITRS [1]. It should be noted that the value quoted as LER is traditionally defined to be 3σ RMS amplitude. Starting from the 2003 ITRS edition, a new LER definition has been introduced. The term LER has been replaced by line width roughness (LWR) defined by the relationship:

$$LER = LWR/\sqrt{2} \tag{3.1}$$

Table 3.1: ITRS 2005 edition LWR and LER guidelines.

Year of Production	2015	2017	2020
DRAM 1/2 Pitch [nm]	**25**	**20**	**14**
MPU Physical L_g [nm]	10	8	5
Line Width Roughness (3σ) [nm]	0.8	0.6	0.5
Line Edge Roughness (3σ) [nm]	0.56	0.42	0.35

The ITRS lithography guideline for LER corresponding to the 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs are given in table 3.1. The other parameter needed to characterise the gate LER is the correlation length. In contrast with the numerous values of RMS amplitude published in the literature for different lithography processes, significantly less is known about the corresponding correlation length [96], which is reported to vary between 10 nm and 50 nm. For the LER simulations presented in this thesis, the correlation length is assumed to be 30 nm. The potential and carrier concentration distributions for a 10×10 nm UTB-SOI MOSFET with randomly generated gate edges are illustrated in figure 3.4. The LER parameters are Δ=3 nm and Λ=30 nm. The potential in this



(a) (b)

Figure 3.4: A typical simulation domain for a 10×10 nm channel UTB-SOI MOSFET due to gate line edge roughness at threshold. The gate and buried oxide is removed to show the fluctuations in (a) electrostatic potential and (b) carrier concentration contour at the source/drain and channel interface.

MOSFET approximately follows the metallurgical pn junction as shown in figure 3.4(a).

3.3 The Simulated UTB-SOI Device

Most simulation studies of IPF have been restricted to devices corresponding to one particular technology node. In this work, the study of IPF has been extended to UTB-SOI MOSFETs corresponding to three technology generations near the long-term end of the current edition of the ITRS [1]. This follows in detail both of the magnitudes and the trend of parameter fluctuations in next generation MOSFETs technology. The process technologies required to manufacture these devices will be developed in the future. However, the availability of the 3D Glasgow numerical device simulator allows us to study in advance the electrical behaviour of these future devices and under the influence of IPF.

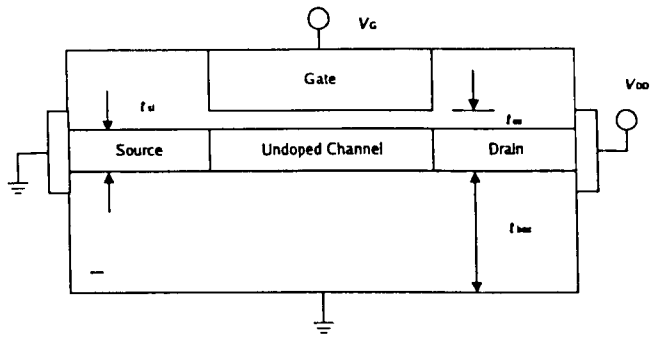


Figure 3.5: Diagram of the generic UTB-SOI MOSFET simulated in this work.

This work only considers high performance devices, which are typical for microprocessor cache and System on Chip (SoC) applications. As mentioned in chapter 2, the ITRS roadmap predicts that double-gate MOSFETs will be required towards the 40 nm technology node. However, much of the work in this thesis was performed prior to these updated guidelines, hence the study presented here only focuses on UTB-SOI MOSFETs. This subsection introduces the structure and the critical design parameters for the devices simulated in this work. The generic structure of the simulated devices is illustrated in Figure 3.5. The 3D Glasgow numerical device simulator initially designed for conventional MOSFETs has been modified to handle UTB-SOI [64] and DG [97] transistors. The simple UTB-SOI MOSFET structure considered here has been selected to clearly illustrate the impact of IPF and to simplify the interpretation of the results.

The scaling of the UTB-SOI MOSFETs from 15 nm down to 5 nm channel lengths have been investigated by Fikru Adamu-Lema and are covered in detail in his PhD dissertation [98]. In this work, a brief description of the scaling approach and the electrical characteristic for the 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs will be presented.

Table 3.2: Investigations of various scaling scenarios for UTB-SOI MOSFET. After [98].

L_C [nm]	t_{ox} [nm]	t_{si} [nm]	$\triangle V_T$ [mV] V_{T850}-V_{T50}	S [mV/dec]	I_{on}/I_{off}
15	1.0	3.0	111	88	42600
10	1.0	3.0	272	125	2280
	0.7	3.0	196	104	8170
	1.0	2.0	146	93	8080
	0.7	2.0	101	82	32200
	0.7	2.5	136	89	9270
5	1.0	3.0	923	240	207
	0.3	3.0	452	133	1520
	1.0	1.0	199	86	6420
	0.3	1.0	57	77	107000
	0.3	2.0	204	88	12400

The starting point in the scaling investigation is a 15 nm device with silicon body thickness of t_{Si}=3 nm and gate oxide of t_{ox}=1 nm selected as reference device parameters. Table 3.2 shows the simulation results including key electrical characteristics for the three devices with channel lengths of 15 nm, 10 nm and 5 nm and various scaling schemes for t_{Si} and t_{ox}. The device scaling study is performed using 2D classical simulations with the commercial simulator Medici^{TM}, which is computationally efficient and sufficiently accurate in the subthreshold regime controlled primarily by the device electrostatics. The linear scaling of both t_{Si} and t_{ox} (the fourth option shown for 10 nm and 5 nm) provides best on/off current ratio, however this results in a body thickness of only 1 nm for the 5 nm channel length device. Aside from the issues involved in fabricating such a thin device, when quantum mechanical confinement in the channel is considered the resultant threshold voltage shift (~700 mV) is prohibitively large [64]. This leads to the adoption of the scaling scheme highlighted in table 3.2, where the oxide thickness scales linearly with channel length but the body thickness scales in a sub-linear fashion, resulting in t_{Si}=2 nm for the 5 nm device. As 7.5 nm channel length device is not included in the scaling study of [98], the t_{Si} and t_{ox}

for 7.5 nm device are obtained from interpolating between the 10 nm and 5 nm channel length devices.

Table 3.3: UTB-SOI MOSFETs physical parameters considered.

Channel length/width [nm]	10/10	7.5/7.5	5/5
Gate oxide thickness, t_{ox} [nm]	0.67	0.5	0.33
Body thickness, t_{Si} [nm]	2.5	2.25	2.0
Buried oxide thickness, t_{box} [nm]		50	
Channel doping, N_a [cm^{-3}]		10^{14}	
Source/Drain doping, $N_{s/d}$ [cm^{-3}]		2×10^{20}	

The summarised device parameters for the investigated family of UTB-SOI MOSFETs are depicted in table 3.3. The 10 nm, 7.5 nm and 5 nm channel length UTB-SOI MOSFETs correspond to the 25 nm, 20 nm and 14 nm technology generations respectively. Another simplification of the presented simulation is the use of silicon dioxide (SiO_2) thickness and dielectric constant to achieve the electrostatic requirement. However, it is believed that such equivalent oxide thickness (EOT) with the application of high-k gate dielectric will become feasible in the near future [2]. Simulation results in sub-section 3.4.2 show that the replacement of SiO_2 with high-k gate dielectric while considering IPF only contributed to approximately 5 percent increase in the threshold voltage standard deviation. The 3D Glasgow device simulator have been calibrated to match the Medici^{TM} simulation result and a metal gate electrode is assumed with the workfunction adjusted to approximately 4.6 eV in each case.

The I_D-V_G characteristics for the 10 nm, 7.5 nm and 5 nm devices simulated are plotted in figure 3.6. The simulations were performed using the 3D Glasgow device simulator assuming continuously doped and uniform devices. The increasing current curvature at shorter channel lengths, clearly indicates increasing problems associated with the access resistance. One of the very important needs in order to retain performance in scaled down MOSFETs and the corresponding circuits is the introduction of raised and silicidised source/drain junctions [99, 100]. The subthreshold behaviour of the three devices is illustrated in figure 3.7 using drift-diffusion simulations with and without density gradient

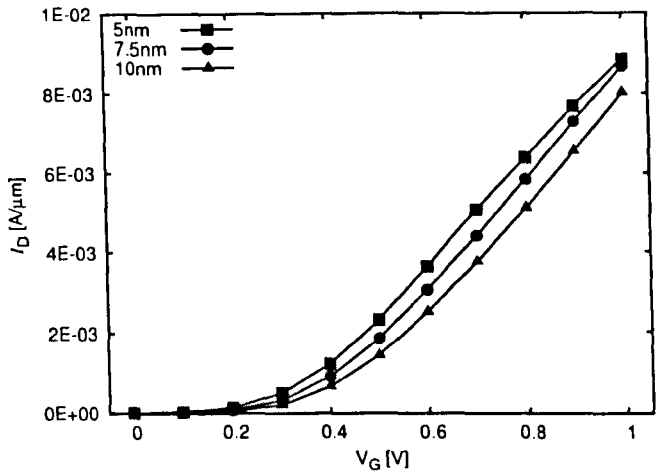


Figure 3.6: Plot of linear scale I_D-V_G characteristics for 10 nm, 7.5 nm and 5 nm channel length UTB-SOI MOSFET.

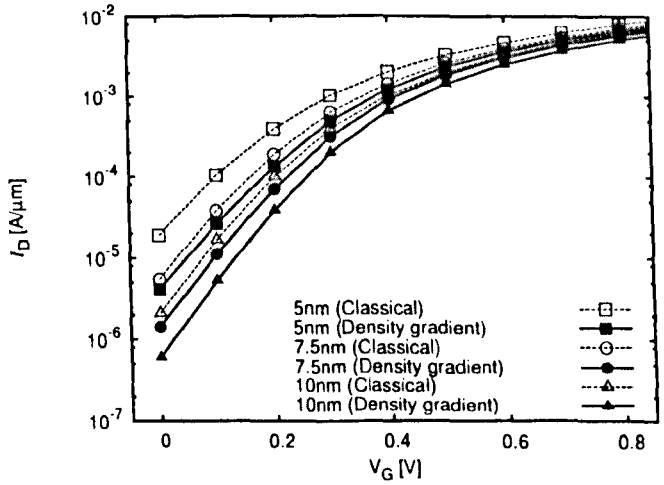


Figure 3.7: I_D-V_G characteristics for 10 nm, 7.5 nm and 5 nm channel length UTB-SOI MOSFET for both classical simulations and simulation with quantum corrections using density gradient approach.

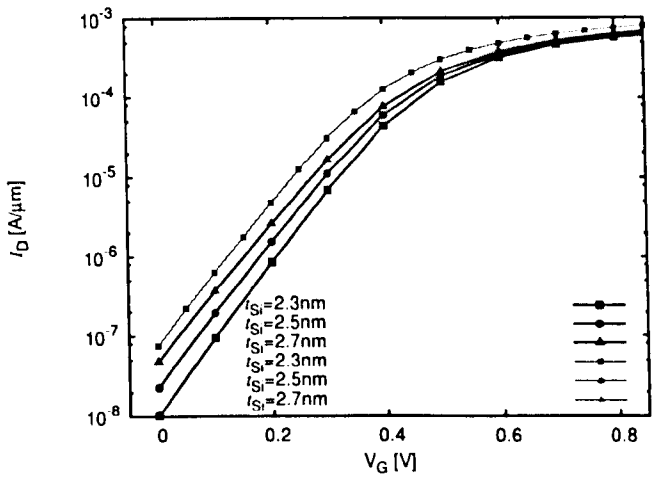


Figure 3.8: The impact of uniform variation of the body thickness (i.e. with no roughness) on the I_D-V_G characteristics of a 10×10 nm channel SOI MOSFET in the classical simulations and quantum corrections with the density gradient approach.

quantum corrections.

In order to clearly illustrate the importance of quantum mechanical confinement effects in the next generation UTB-SOI MOSFETs, the 10 nm channel length UTB SOI MOSFET has been simulated with body thickness, t_{Si} of 2.3 nm, 2.5 nm and 2.7 nm. The I_D-V_G characteristics obtained from drift-diffusion simulations with and without density gradient quantum corrections are illustrated in figure 3.8. The classical simulations show no dependence of the threshold voltage on the body thicknesses. The inclusion of quantum corrections results in much larger change in threshold voltage with the reduction of the body thickness, due to the shift in position of the electron ground state which is approximated by the density gradient solution.

Figure 3.9 shows channel length dependence of the threshold voltage, V_T of the three UTB-SOI MOSFETs. For the purpose of this analysis V_T is determined using a current criteria of $10^{-7}W_{eff}/L_{eff}$ A at V_D=50 mV. The off-current, I_{off} and on-current, I_{on} for the 10 nm, 7.5 nm and 5 nm transistor are plotted in figure 3.10. The values of I_{off} and on-current, I_{on} are extracted at the points where I_D (V_G=0 V) and I_D (V_G=V_D=V_{dd}) respectively. Higher I_{on} values observed in the

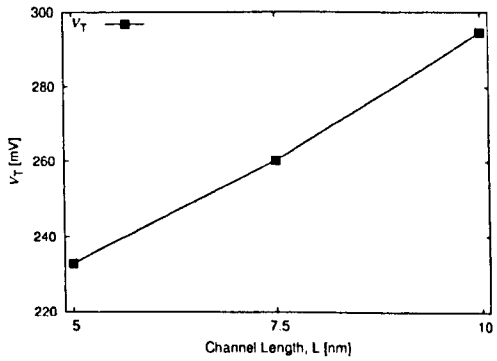
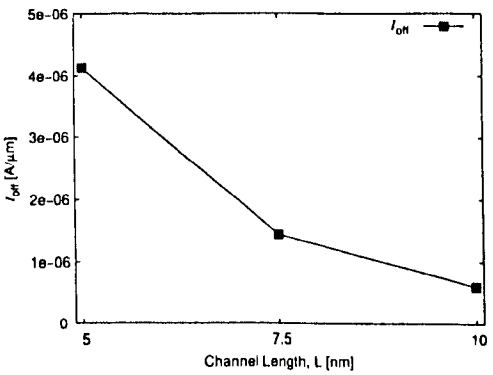
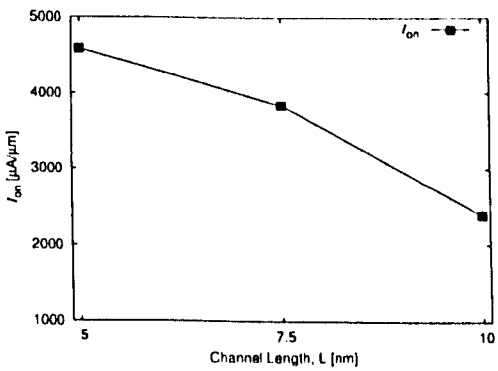


Figure 3.9: Threshold voltage, V_T for 10 nm, 7.5 nm and 5 nm channel length UTB-SOI MOSFETs. V_D=50 mV.



(a)



(b)

Figure 3.10: (a) Off-current, I_{off} and (b) on-current, I_{on} for 10 nm, 7.5 nm and 5 nm channel length UTB-SOI MOSFETs.

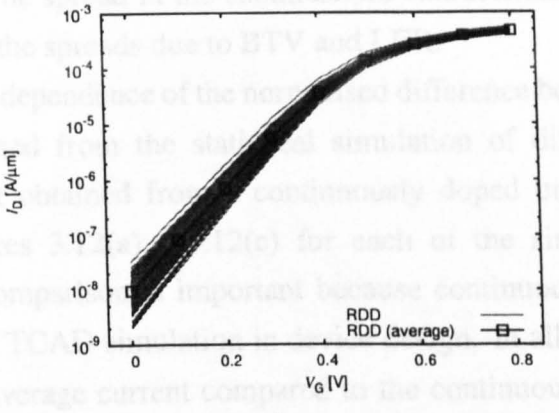
"atomistic" simulation compared to the results from UTB-SOI MOSFETs scaling work are caused by the constant mobility model used to represent the transport in the MOSFET channel. Such simple mobility models do not take into account the mobility reduction in the highly doped source and drain regions, nor the effects of the lateral and perpendicular electric fields in the channel.

3.4 Intrinsic Parameter Fluctuations in UTB-SOI MOSFETs

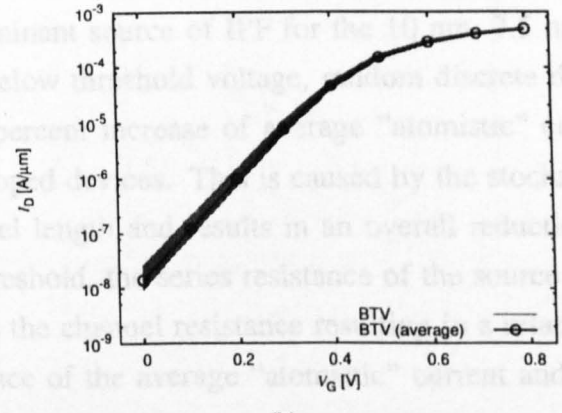
The magnitude of intrinsic parameter fluctuations due to random discrete dopants, body thickness variations and line edge roughness using simulations of statistical samples of 200 UTB-SOI MOSFETs for each device design are presented in this section. The sources of intrinsic parameter fluctuations which can be separated in simulations, will occur simultaneously within a single MOSFET. To understand the magnitude of IPF in an actual device simulations with all sources of intrinsic parameter fluctuations simultaneously present have also been performed. The I_D-V_G simulations have been performed at both low and high drain voltage. Results for both V_D bias conditions are necessary for SPICE compact model parameter extraction and eventually for the SRAM cell simulation in the following chapters. In the following sub-section, the impact of the different sources of IPF on I_D-V_G characteristics, threshold voltage V_T, off-current I_{off} and on-current I_{on} are presented.

3.4.1 I_D-V_G Characteristic

Figure 3.11 illustrates I_D-V_G characteristics obtained from the simulation of statistical samples of 200 macroscopically different 10 nm UTB-SOI MOSFETs in the presence of different sources of IPF. The simulations show that each microscopically different UTB-SOI MOSFET has different characteristics in the presence of random discrete dopants, body thickness variations and gate line edge roughness. Each source of IPF has a marked effect in the subthreshold regime leading to current fluctuations with large magnitude, but has a smaller impact



(a)



(b)

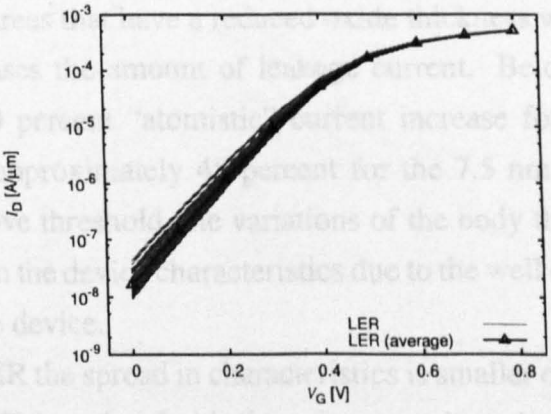


Figure 3.11: I_D-V_G characteristics from an ensemble of 200 macroscopically different 10 nm UTB-SOI due to (a) random discrete dopants (b) body thickness variations and (c) line edge roughness, along with the average I_D, $\langle I_D \rangle$. V_D=50 mV.

on the on-current. The spread in the subthreshold characteristics due to RDD is largest compared to the spreads due to BTV and LER.

The gate voltage dependence of the normalised difference between the average current, $\langle I_D \rangle$ obtained from the statistical simulation of different sources of IPF and the current obtained from a continuously doped uniform device, I_{D0} is depicted in figures 3.12(a) - 3.12(c) for each of the simulated UTB-SOI MOSFETs. This comparison is important because continuously doped devices are still the basis of TCAD simulation in device design. In all cases, we observe an increase in the average current compared to the continuously doped uniform device. The difference between the average current and the current from the continuously doped uniform device is reduced at higher gate voltage.

RDD is the dominant source of IPF for the 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs. Below threshold voltage, random discrete dopants result in an approximately 60 percent increase of average "atomistic" current compared to the continuously doped devices. This is caused by the stochastic shortenings of the physical channel length and results in an overall reduction of the threshold voltage. Above threshold, the series resistance of the source and drain becomes larger compared to the channel resistance resulting in a relative reduction in the percentage difference of the average "atomistic" current and the current from a continuously doped device.

BTV in UTB-SOI MOSFETs also results in an increase in the leakage current. This is due to local areas that have a reduced oxide thickness which facilitates the inversion and increases the amount of leakage current. Below threshold, there is approximately 40 percent "atomistic" current increase for the 10 nm and a further increase of approximately 45 percent for the 7.5 nm and 5 nm channel length devices. Above threshold, the variations of the body thickness have a less pronounced effect on the device characteristics due to the well developed inversion layer throughout the device.

In the case of LER the spread in characteristics is smaller compared to the case of RDD and BTV. Below threshold, there is approximately 30 percent increase in average current for the 10 nm devices and approximately 35 percent and 40 percent increase for the 7.5 nm and 5 nm channel length devices respectively. Although LER also causes shortening of the physical channel length similar to

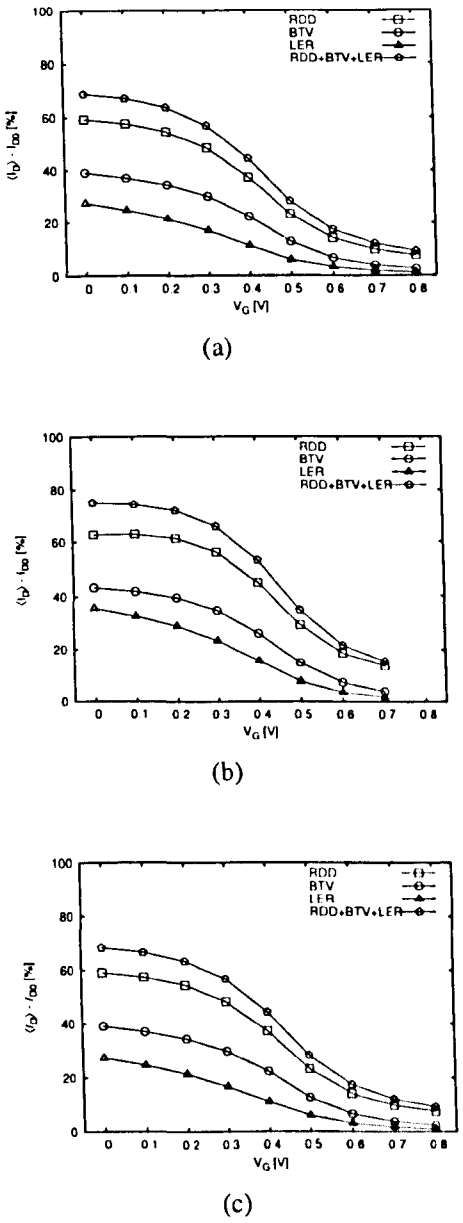


Figure 3.12: I_D percentage difference for (a) 10 nm, (b) 7.5 nm and (c) 5 nm UTB-SOI MOSFETs between the average device characteristics and the continuously doped uniform device. The average current, $\langle I_D \rangle$ are obtain from simulation of different sources of intrinsic parameter fluctuations individually and in combination.

the case of random discrete dopants, the magnitude of the difference is smaller as the RMS amplitudes are reduced according to the ITRS requirement. Similar to the case of body thickness variation, the effect of LER becomes less pronounced above threshold.

The impact of the three sources of IPF occurring simultaneously in an actual device is also illustrated in figures 3.12(a) - 3.12(c). As expected, the combined effect is larger compared to the effect of each individual source of IPF. Below threshold, the combined sources of IPF (RDD+BTV+LER) cause an approximately 70 percent average current increase for the 10 nm devices. As illustrated in figure 3.12(b) and 3.12(c) the increase of average current further rises to 75 percent and 90 percent for the 7.5 nm and 5 nm UTB-SOI MOSFETs respectively for combined sources of IPF.

3.4.2 Threshold Voltage

Threshold voltage V_T, is an important parameter in MOSFET design. In concert with the subthreshold slope it determines the off-state leakage current. A well defined, steady and stable threshold voltage is crucially important for analogue and digital circuits, i.e., less variation of V_T is highly desirable. Therefore, it is important to keep V_T within an acceptable degree of tolerance in order to deliver a reliable integrated circuit and properly working systems. However in real nano-scale MOSFETs, the different sources of IPF introduce V_T fluctuations. Moreover, the fluctuations increase significantly as the gate length decreases.

The simulated average threshold voltage, $\langle V_T \rangle$ as a function of channel length with different sources of IPF is depicted in figure 3.13. The combined sources of IPF has the largest $\langle V_T \rangle$ for the 5 nm, 7.5 nm and 10 nm UTB-SOI MOSFET channel length compared to other individual sources of IPF. This is followed by RDD, BTV and LER. The statistical average effect from the simulation results give a false notion that the combined source of IPF effects is less severe than the individual source of IPF. This observation is important during SRAM simulation in chapter 4, as the static noise margin of SRAM cells is a function of threshold voltage, supply voltage and cell ratio [101].

Figure 3.14 illustrate the channel length dependence of the shift in the average

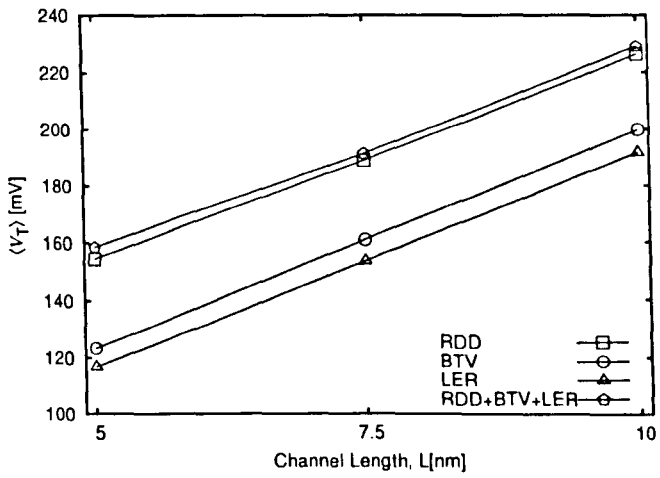


Figure 3.13: Average threshold voltage, $\langle V_T \rangle$ of 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs due to different sources of intrinsic parameter fluctuations.

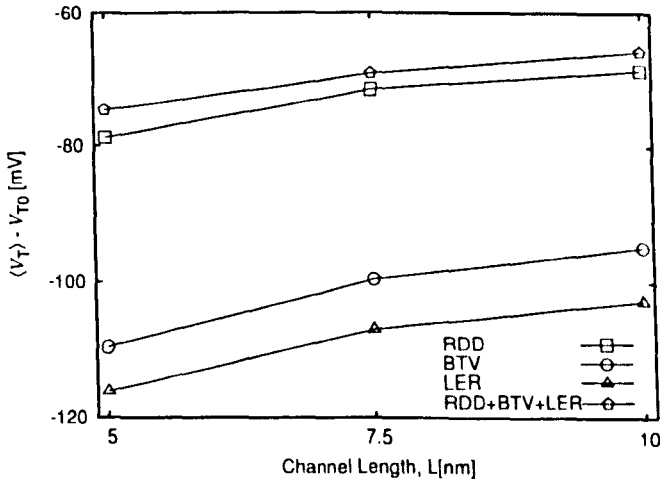
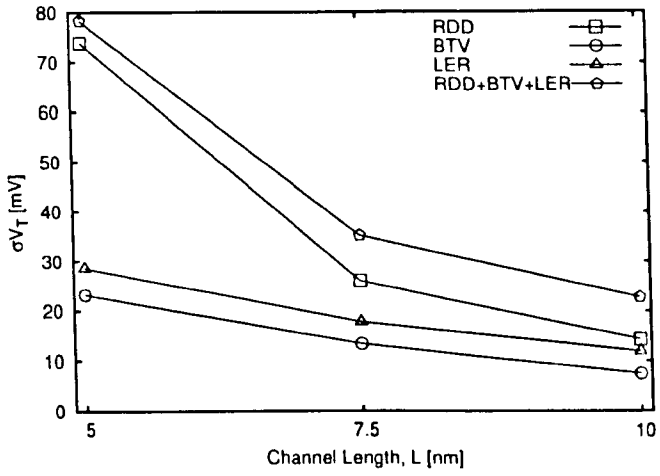


Figure 3.14: Threshold voltage shift, ($\langle V_T \rangle$ - V_{T0}) in 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs due to different sources of intrinsic parameter fluctuations.



(a)

Figure 3.15: Standard deviation of threshold voltage in an ensemble of 200 distinct 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs due to different sources of intrinsic parameter fluctuations.

threshold voltage, $\langle V_T \rangle$ corresponding to different IPF sources compared to the threshold voltage of a continuously doped uniform device, V_{T0}. Each source of IPF individually or in combination cause threshold voltage lowering compared to a continuously doped uniform device. The shift in the average threshold voltage increases almost linearly with the reduction in the channel length for all sources of IPF. In the case of combined sources of IPF, the average threshold voltage for 10 nm UTB-SOI MOSFETs is reduced by 68 mV, while the 7.5 nm and 5 nm devices have a threshold voltage shift of 72 mV and 79 mV respectively. The results, along with the effects of each single source of fluctuations is shown in detail in figure 3.14.

Figure 3.15 compares the standard deviation in the threshold voltage (σV_T) introduced by different sources of IPF for all UTB-SOI MOSFETs investigated in this work. The results follow an intuitively expected trend as the fluctuations increase with decreasing channel length. BTV and LER cause a standard deviation increasing from approximately 10 mV to 30 mV as the channel length is scaled from 10 to 5 nm. However, in the RDD case the standard deviation of threshold voltage increases non-linearly from 14 mV in the 10 nm devices to approximately

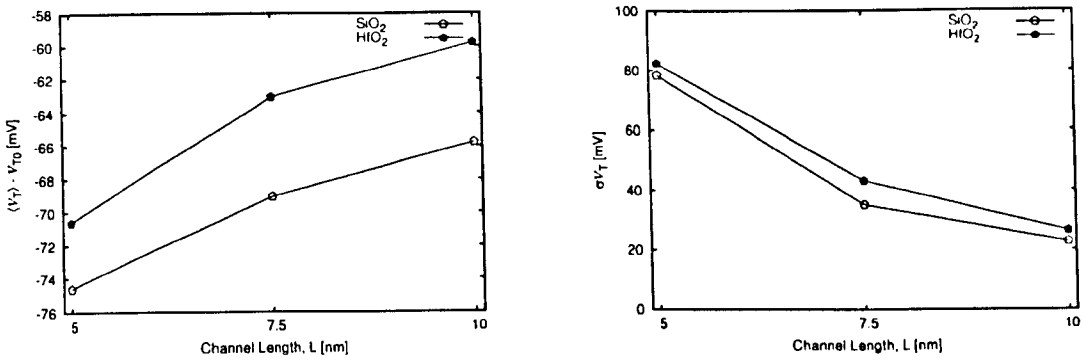
Table 3.4: Summary of the standard deviations of threshold voltage, σV_T for the case of individual and combined sources of intrinsic parameter fluctuations. Calculated σV_T from the individual sources of intrinsic parameter fluctuations are also included.

Intrinsic Parameter Fluctuations	10 nm	7.5 nm	5 nm
RDD σV_T [mV]	14.2	26.0	73.9
BTV σV_T [mV]	7.4	13.4	23.2
LER σV_T [mV]	11.9	17.6	28.6
Calculated σV_T [mV]	20.0	34.1	82.5
RDD + BTV + LER σV_T [mV]	22.8	35.2	78.5

75 mV in 5 nm one. Assuming the 6σ spread of a normal distribution, often used for industrial yield calculation [102] gives approximately a 450 mV range of threshold voltages bearing in mind an expected target V_T of 200 mV. Such variations will significantly affect the SRAM cells and peripheral circuit noise margins. It is also evident that the magnitude of fluctuations resulting from RDD in the source/drain regions will become a dominant source of intrinsic parameter fluctuations, especially for the 5 nm UTB-SOI MOSFETs compared to characteristic fluctuations due to BTV and LER in the gate pattern definition. The results for combined sources of IPF for each of the UTB-SOI MOSFETs investigated are included in the same figure.

The combined effect of three statistically independent variables on the standard deviation is given by the relationship $\sigma_{1+2+3} = \sqrt{\sigma_1{}^2 + \sigma_2{}^2 + \sigma_3{}^2}$. Table 3.4 compares the standard deviation in the threshold voltage (σV_T) from their addition as statistically independent entities to the results of simulations combining all three sources of intrinsic parameter fluctuations. The statistical summations of the standard deviations from individual sources of IPF are very close to the value obtained from the simultaneous simulation of the three fluctuation sources. This provides some evidence that these sources of fluctuations are uncorrelated.

As mention earlier, the simulations use SiO_2 thickness and dielectric constant to secure the electrostatic integrity of the devices. The SiO_2 thickness of 0.67 nm, 0.5 nm and 0.33 nm for the respective 10 nm and 7.5 nm and 5 nm channel length



(a) (b)

Figure 3.16: (a) Average threshold voltage shift and (b) standard deviation of threshold voltage in 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs from simulation of combined source of intrinsic parameter fluctuations with different gate dielectric.

devices are unrealistic due to exponential increase of tunnelling current through the gate dielectric with decreasing physical thickness [103]. Tunnelling currents in SiO_2 layers thinner than 0.8 nm cannot be tolerated, even for high-performance devices [24].

To understand better the impact of intrinsic parameter fluctuations in the next generation UTB-SOI MOSFETs, a statistical simulation of the three devices with physically thicker high-k layers are necessary. Simulations with HfO_2 gate dielectric were carried out keeping the same equivalent oxide thickness. A dielectric constant k=20 was assumed in this case [2] and the thickness of the gate dielectric of the 10 nm and 7.5 nm and 5 nm have been increased by the ratio of the HfO_2 on the SiO_2 dielectric constants to 3.35 nm, 2.5 nm and 1.65 nm respectively. Figure 3.16(a) and 3.16(b) shows the average threshold voltage shift and standard deviation of threshold voltage for the three UTB-SOI MOSFETs with SiO_2 and HfO_2 as gate insulators. The simulations are performed considering all source of intrinsic parameter fluctuations in combination. Figure 3.16(a) shows a reduction between 5 and 10 percent average threshold voltage shift for devices with HfO_2 gate insulator compared to devices with SiO_2 gate insulator. This is caused by proximity effects associated with the five times increase of the HfO_2 physical

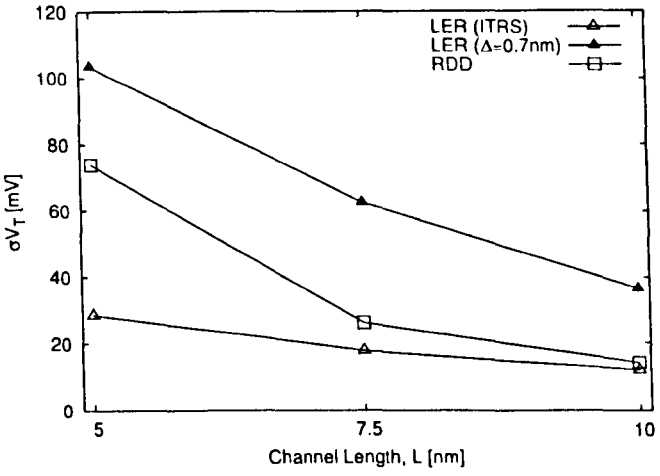
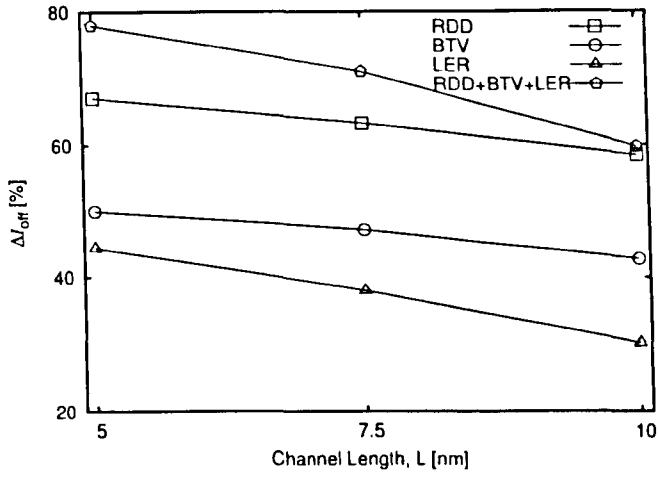


Figure 3.17: Standard deviation of threshold voltage for 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs due to different line edge roughness criteria. Simulation result considering RDD in the source/drain region as source of IPF is also included for comparison.

thickness. It should be noted that the physical thickness of the high-k insulator becomes more important as k increases [104] and has to be taken into account in the simulations. Figure 3.16(b) indicates approximately 5 percent increase in σV_T of devices with HfO_2 gate insulator compared to devices with SiO_2 gate insulator. The results show that, without considering the gate leakage effects, the use of SiO_2 as gate insulator gives reasonably accurate results for the purpose of this work.

The LER simulations carried out in this work follow the values prescribed by the ITRS according to the 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs technology generations given in table 3.1. As shown in figure 3.17, the LER induced threshold voltage standard deviation for this scenario is well controlled, increasing from 11 mV for the 10 nm channel length, rising to 23 mV for the 5 nm UTB-SOI MOSFET. However, the reduction of the LER in accordance to the ITRS requirements will be a very difficult task due to the molecular structure of the photoresist the corpuscular nature of the light and the limitation of optical lithography. Therefore as a second scenario simulations with a constant value of $\triangle$=0.7 nm at all channel lengths were carried out keeping the correlation length 30 nm. In this case, the LER threshold voltage standard deviation becomes worse



(a)

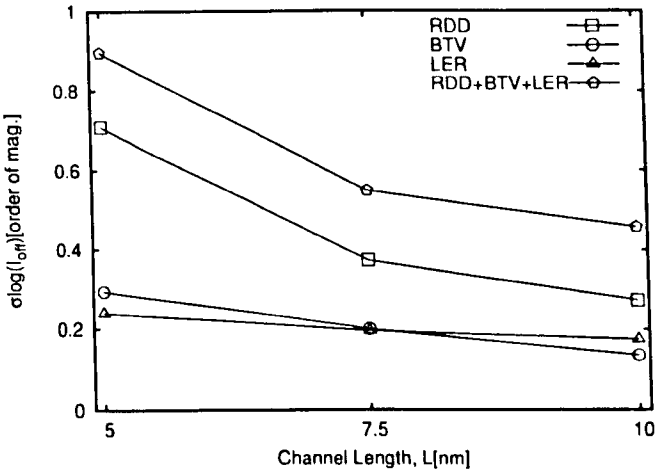
Figure 3.18: Off-current shift for 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs with different sources of intrinsic parameter fluctuations.

than that of RDD. In this second scenario the LER results in a standard deviation of 36 mV at 10 nm channel length which increases to 103 mV at the 5 nm channel length.

3.4.3 Off-Current

The off-current is another important parameter in MOSFETs, and to a great extent determines the standby leakage current in integrated circuits. For SRAMs, the off-current fluctuations are also important as they degrade read operation performance by affecting the precharged bitlines [105] as well as contributing to the total standby power dissipation.

Its illustrated in figure 3.18 that the different sources of IPF result in a substantial increase in the average subthreshold leakage current with the reduction of the channel length. Even the "ideal" LER scenario, where the magnitude of the line edge roughness follows the ITRS requirements there is a considerable average increase in subthreshold leakage for the UTB SOI MOSFETs. This is highly undesirable from the static power dissipation point of view. However, the ideal LER scenario causes the smallest off-current increase from approximately



(a)

Figure 3.19: Standard deviation of off-current, $\sigma\log(I_{off})$ for 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs with different sources of intrinsic parameter fluctuations.

33 percent at 10 nm channel length to 42 percent at 5 nm channel length. The corresponding results for the rest of the individual and the combined sources of fluctuations are also shown in figure 3.18.

Unlike the distributions of the threshold voltage, which are close to normal distributions, the I_{off} distribution is a log-normal distribution. This is due to the exponential dependence of the subthreshold current on gate voltage. The channel length dependence of the standard deviation of $\log(I_{off})$ is shown in figure 3.19. The magnitude of the I_{off} fluctuations corresponding to each source of IPF increases as the UTB-SOI devices are scaled to shorter channel lengths. Figure 3.19 clearly shows that RDD remains the main source of I_{off} fluctuations in UTB-SOI MOSFETs at all investigated channel lengths. BTV and LER result in a standard deviation of less than 0.3 orders of magnitude for all three UTB-SOI MOSFETs. In these cases, line edge roughness dominates at longer channel lengths, but there is a crossover for devices smaller than 7.5 nm channel length. However the magnitude of the standard deviation in the case of RDD increase non-linearly and more sharply.

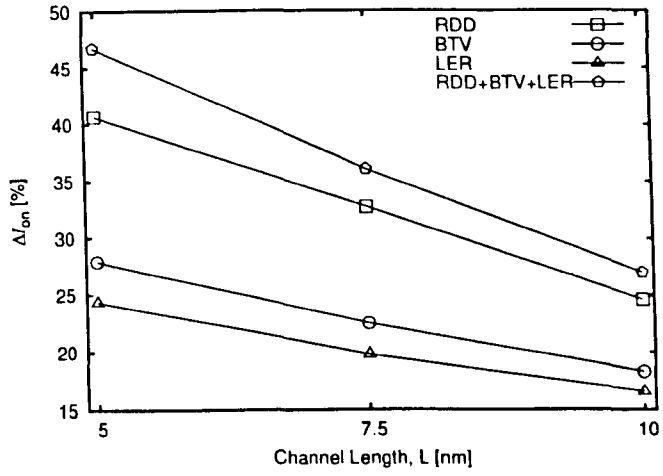


Figure 3.20: On-current shift for 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs with different sources of intrinsic parameter fluctuations.

3.4.4 On-Current

The on-current is key measure for the performance of MOSFETs. One of the motivations of scaling transistors is to achieve high relative drive current in order to boost circuit performance. However variations in the drive current may result in mismatch in analogue applications and variation in the signal propagation times of digital circuits.

The normalised shift in average on-current from atomistic simulation compared to the on-current from a continuously doped uniform interface device as a function of channel length is depicted in 3.20. Similar to the results for the off-current shift, LER causes the smallest on-current shift followed by BTV, while RDD causes the largest shift. For the 10 nm devices, LER and BTV cause approximately between 16 to 18 percent I_{on} shift respectively. The shift in I_{on} increases linearly as the channel length is scaled down, to approximately between 24 to 28 percent for the 5 nm UTB SOI MOSFETs. RDD results in a larger on-current I_{on} shift compared to the other IPF sources, starting from approximately 25 percent for the 10 nm devices and increasing to 41 percent for the 5 nm devices.

As expected, there is a trend of increasing I_{on} fluctuation magnitude with the reduction of the channel length as illustrated in figure 3.21. BTV and LER result in an on-current standard deviation of less than 5 percent for all three UTB-SOI

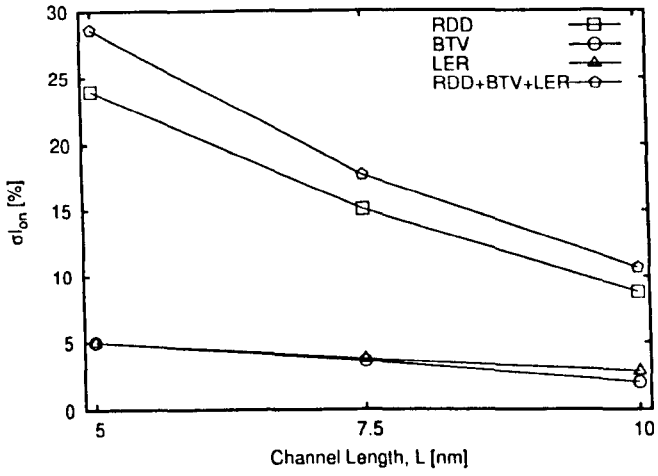


Figure 3.21: Standard deviation of on-current for 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs with different sources of intrinsic parameter fluctuations.

MOSFETs. In both these cases, LER dominates at longer channel lengths but causes a similar to BTV standard deviation of on-current below 10 nm channel length. The results and effects associated with the combined source of IPF is also shown in the same figure.

3.5 Chapter Summary

We have shown that the next generations of UTB-SOI MOSFETs are affected by different sources of intrinsic parameter fluctuations, which can become a major factor limiting further scaling and integration. As expected, for each investigated electrical characteristic the combined sources of IPF cause the worst fluctuations, compared to each individual source of IPF. Random discrete dopants in the source/drain region of UTB-SOI MOSFETs are the dominant individual source of intrinsic parameter fluctuations. When comparing the impact of line edge roughness and body thickness variations, the geometry and scale of the devices will determine which of these two sources of fluctuations dominates and it is therefore important to investigate each source individually, and all combined to obtain the full picture.

Below threshold voltage, simulation of combined sources of IPF caused

between 70 and 90 percent increase in average current of the simulated sample of devices. The impact of the combined sources of IPF on threshold voltage is dramatic starting from 22 mV standard deviation for the 10 nm devices which increases to 79 mV for 5 nm device. Simulation results also show that switching the gate dielectric from SiO_2 to HfO_2 causes less than 5 percent additional increase of threshold voltage standard deviation for the UTB-SOI MOSFET investigated in this work. Assuming a scenario in which LER does not scale according to the ITRS, but stays close to current technology magnitudes, simulations demonstrate that fluctuations caused by this LER become more critical compared to the fluctuations induced by RDD in the source/drain regions. In this case LER causes a standard deviation of 36 mV for the 10 nm device, increasing to 103 mV for the 5 nm devices.

The sources of IPF also result in a substantial increase in the average subthreshold leakage current which becomes larger with the reduction of the channel length. The standard deviation of the off-current, considering all sources of fluctuations in combination, is 0.28 orders of magnitude for the 10 nm UTB-SOI MOSFETs, rising to 0.9 orders of magnitude for the 5 nm devices. Although the 3D Glasgow simulator underestimates non-equilibrium transports effects, it still predicts that the investigated sources of IPF will cause serious on-current fluctuation problems. Combined sources of IPF cause between 11 to 28 percent standard deviation of on-current for the UTB-SOI MOSFETs investigated in this work.

From the perspective of intrinsic parameter fluctuations, scaling down UTB-SOI MOSFETs to 10 nm and below will be extremely difficult. Although, there will be an inevitable transition from single-gate UTB-SOI to double-gate or multi-gate MOSFETs resulting from electrostatic constraints, impact of intrinsic parameter fluctuations would still exist.

The next step, in this research will be to capture the results of the 3D statistical simulations in statistical SPICE compact modelling which will allow to study the impact of the intrinsic fluctuations on circuit and systems operation. This will help to develop circuit design methodology that could cope better with the device variability.

Chapter 4

Statistical Circuit Simulation Framework

4.1 Introduction

The semiconductor industry is constantly striving to increase product yield and to reduce product development time. One of the integral component of IC design and manufacturing activity is the prediction of both nominal circuit behaviour and the likely statistical circuit performance spreads. Hence there is a dire need for a very good understanding of the impact of intrinsic parameter fluctuations in MOSFET on resulting variation in corresponding circuit.

In chapter 3, the impact of intrinsic parameter fluctuations on UTB-SOI MOSFETs behaviour have been investigated. Fluctuation of transistor characteristic reduces the reliability and operating margin of circuit with the continuous scaling down of device feature size and power supply. This requires the development of statistical circuit simulation methodology taking into account the variability in the device characteristic at present and future MOSFET generations. In this chapter, a new statistical circuit simulation methodology that realistically takes into account the impact of intrinsic parameter fluctuations in transistors on the corresponding circuits is presented. The methodology incorporates intrinsic parameter fluctuations information into Berkeley BSIMSOI [22], a SPICE [21] compact model and is applied to the 10 nm, 7.5 nm and

5 nm channel length UTB-SOI MOSFETs simulated in the previous chapter. The compact model library built in this chapter will be employed in chapter 5 to investigate the impact of intrinsic parameter fluctuations in UTB-SOI MOSFET based SRAM cell.

In section 4.2 of this chapter, the overall statistical circuit simulation methodology that bridges the device-level and circuit-level simulation aspect of this thesis is presented. The methodology consists of a statistical compact model parameter extraction and statistical circuit simulation strategy. In section 4.3, the statistical parameter extraction strategy, which is essential in achieving highly accurate modeling of the fluctuation effects will be discussed. The statistical parameter extraction is used to build a compact model library for the 10 nm, 7.5 nm and 5 nm channel length UTB-SOI MOSFETs simulated in chapter 3. The quality of the compact model and analysis of the extracted parameters is presented. In section 4.4, a statistical circuit simulation strategy for utilising the compact model library built in section 4.3 is described.

4.2 Statistical Circuit Simulation Methodology

Statistical circuit simulation analysis consists of a series of statistical device-level and circuit-level simulations. The robust statistical circuit simulation methodology that has been developed for this work is depicted in figure 4.1. Critical ingredients of any statistical circuit modelling approach are the device data sets employed for parameter extraction, the MOSFET compact model and the parameter extraction process itself. The reliability and accuracy of the statistical circuit spread prediction scheme is ultimately determined by the suitability of these three components.

The accuracy of MOSFET parameter extraction is determined by the quality of the collected electrical data sets coming from either simulations or from measurements. Current-voltage characteristic data sets for different bias condition enable the extraction of the core model parameters and estimates for the drain and source access resistances. In this work, data sets required for the compact model parameter extraction are obtained from the simulation of the previously described 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFET presented in chapter 3. These data

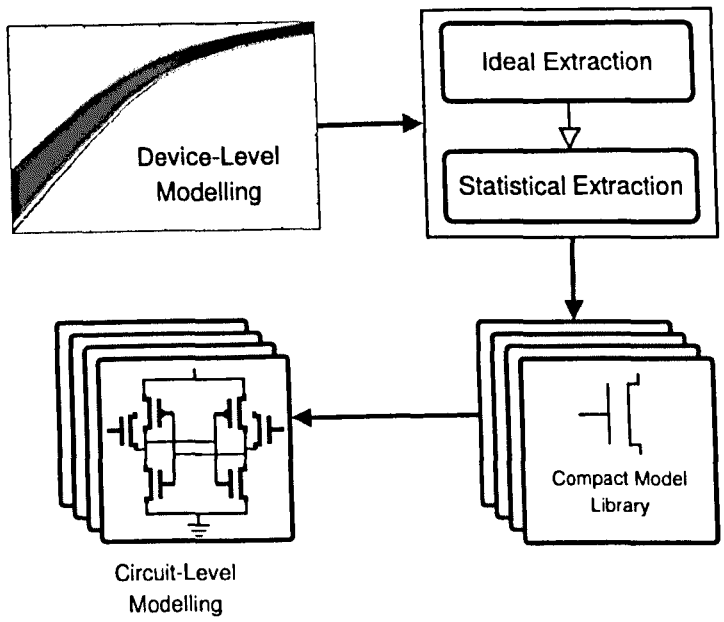


Figure 4.1: Flowchart of statistical circuit simulation methodology.

sets comprise of current-voltage characteristics from ideal devices simulation and devices with different sources of intrinsic parameter fluctuations individually or in combination.

The selected MOSFET compact model must be capable of accurately reproducing the characteristics of the devices. In this work Berkeley BSIMSOI [22] which is an accurate and computationally efficient industry standard SOI MOSFET compact model has been chosen. BSIMSOI is a derivative of the industry-standard bulk MOSFET compact model BSIM3 [71] with SOI specific features including floating-body model, body-contact model and self-heating model. However, because of the chosen UTB-SOI architecture, it is safe to initially focus on extraction of basic MOSFET parameters as UTB-SOI structure is less affected by history effects, unlike its PD-SOI [39] counterpart. However, UTB-SOI MOSFETs are still susceptible to the local thermal heating generated in the channel because of the low thermal conductivity of the buried oxide. Extracting model parameter without considering 'self heating' will overestimate circuit speed in SPICE simulation. However, under dynamic operation conditions (e.g. digital circuit), the self-heating effect is generally insignificant, since the

average power consumption per device is low and its switching time, is much shorter than the thermal time constant [84, 106]. A small difference between 3 to 6 percent delay for inverter circuit has been observed [106].

Compact models used in circuit simulation comprise of equations with associated parameters that need to be determined using parameter extraction procedures. Without a good parameter-extraction strategy a compact model is not complete and useful. Due to the device physics based nature of BSIMSOI, extraction is not merely a curve fitting process compared to some of the earlier generation SPICE compact models. Parameter extraction routes must be chosen carefully to prevent unphysical MOSFET device parameter identification and to capture completely the behaviour of the DC current characteristic observed at the device-level modelling stage. In general, the applicability of DC current-voltage characteristics to characterize device mismatch introduced by intrinsic parameter fluctuations is widely accepted [107]. The compact model parameter extraction was carried out using Aurora^{TM}[108], a general purpose optimisation program for fitting SPICE compact models such as BSIMSOI to device electrical data. The program fits a model to a set of data points by adjusting one or more parameters of the model. The complete set of optimisation steps constitutes the parameter extraction strategy. Not only the extraction steps but also their order is very important. The accuracy of the parameter extraction procedure is limited only by the accuracy of the model and the correct choice of parameters. The parameters are extracted by minimizing the root mean square (RMS) error between each point of data and corresponding compact model value as defined in (4.1).

$$RMS = \sqrt{\triangle I_0 + ... + \triangle I_n} \tag{4.1}$$

Two different strategies are available for extracting parameters: the single device extraction strategy and group device extraction strategy. Group device extraction strategy requires simulation or measurement data from devices with different channel length and width geometries of a certain process. Data sets from each devices will be used during extraction strategy to capture geometry dependence parameters. The resulting model parameters might not be absolutely perfect for any single device but cover the whole range of channel length and

Table 4.1: Prerequisite process parameters prior to compact model extraction.

Parameter	Physical Meaning
L	Channel length
W	Channel width
t_{ox}	Gate oxide thickness
t_{Si}	Silicon film thickness
t_{box}	Buried oxide thickness
X_j	Source/Drain junction depth
n_{ch}	Channel doping concentration
n_{sub}	Substrate doping concentration
Ngate	Polysilicon gate doping concentration

widths under consideration. In a single device extraction strategy, data from a single device is used to extract a complete set of model parameters. The resulting parameters fit well the single device, but will not fit other devices with different geometries. In this work, single device extraction strategy is carried out to obtain compact model parameters as circuits simulated will only use the same geometry device. In addition, the strong source/drain resistance observed in chapter 3 and the sensitivity to electrostatic effect resulting in large current characteristic mismatch between long and short channel devices prevents the use of group device extraction strategy as suggested by [71].

It is possible to perform a global optimisation to find model parameters that will fit the available data set, with minimum RMS error between data sets and BSIMSOI calculated data point. However, this optimization treats each parameter as fitting and often has severe problems and can result in nonphysical parameter values. Using local optimization, parameters are extracted independently of each other from bias condition which correspond to dominant physical mechanism. A good optimisation strategy ensures that the results of a preceding steps are not affected by succeeding steps. Different sets of parameters are suitable for fitting in the linear region of operation or in saturation region. Some parameters are directly measurable while others can only be found indirectly by least squares fit. In this work, a local optimization strategy has been adopted.

Basically, BSIMSOI consists of physical and empirical parameters. At the

beginning of the parameter extraction procedure, some prerequisite device design process related parameters have to be provided as listed in table 4.1. To keep the physical meaning of the compact model, it is always advisable to use direct measurement of a physical parameter rather than indirect identification by fitting. The incorrect identification of one parameter adversely affects the identification of the other model parameters [109]. In this work, these parameters correspond to the physical parameters of the UTB-SOI MOSFETs considered in this work as depicted in table 3.3. Doping concentration in the polysilicon gate, *Ngate* is used to model the polysilicon depletion effects. However, UTB-SOI MOSFET devices simulated in chapter 3 are assumed to have a metal gate. In BSIMSOI, the polysilicon depletion effects model can be bypassed by setting the value of *Ngate* to zero. Unlike BSIM3 [71], the inclusion of flat-band voltage (V_{fb}) in a unified current formula of BSIMSOI prevents direct access to the parameter during the extraction process thus requiring adjustment of the BSIMSOI threshold voltage parameters.

A two-stage statistical parameter extraction strategy suitable for both the BSIMSOI compact model and the statistical circuit simulation task involved has been developed and are presented in the following section. This strategy ensures the generation of compact model libraries which closely match the physically simulated characteristic of the statistical ensembles of real device in the presence of intrinsic parameter fluctuation sources. This approach also allows the sources of intrinsic fluctuation to be investigated individually or in combination.

4.3 Statistical Parameter Extraction

As discussed in chapter 2, the BSIMSOI compact model has been developed for deterministic (not statistical) devices and does not explicitly include effects associated with intrinsic parameter fluctuations. For example, in a deterministic model two devices with the same dimensions, identical process and transport parameters give rise to an identical device characteristics. In reality they will have different characteristics due to different sources of IPF that affect their electrical behavior. Although, the BSIMSOI compact model does not explicitly consider intrinsic parameter fluctuation effects, it has a number of empirical parameters

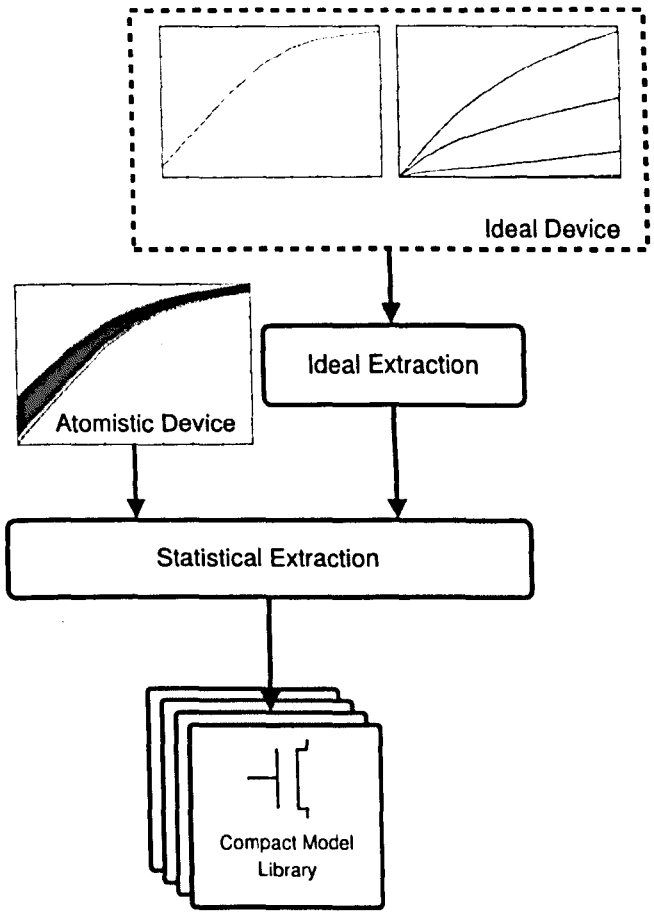


Figure 4.2: Flowchart of a two-stage statistical compact model parameter extraction methodology.

introduced to model process variation conditions. It has been observed that, although a large number of compact model parameters are needed to accurately model MOSFET behaviour at circuit level, process fluctuations influence only a handful of parameters [110]. Therefore, a carefully chosen subset of parameters can be used to model the fluctuation in UTB-SOI MOSFETs characteristics introduced by random discrete dopants, body thickness variations and gate line edge roughness. In principle, BSIMSOI is flexible enough to describe device mismatch induced by IPF using a number of empirical parameters originally introduced to model device performance variation caused by different foundry processes.

Figure 4.2 illustrates the basic idea of the two-stage statistical parameter extraction strategy developed in this work. In the first parameter extraction stage, a number of key BSIMSOI parameters are extracted from the I_D-V_G and I_D-V_D characteristics of an ideal UTB-SOI MOSFETs. The ideal devices has continuously doped source/drain regions, uniform body thickness and straight gate line edge. Therefore only one extraction procedure is required for a particular UTB-SOI MOSFETs generation of interest. The ideal device extraction strategy is presented in detail in section 4.3.1. The extracted parameters are then grouped into two parts. Parameters which are considered insensitive to intrinsic fluctuations are fixed after the first stage while several BSIMSOI parameters are selected to represent the impact of different sources of intrinsic parameter fluctuations in the second statistical extraction stage. This statistical extraction strategy is repeated for each of the ensemble of 200 microscopically different 10 nm, 7.5 nm and 5 nm channel length UTB-SOI MOSFET with different sources of intrinsic parameter fluctuations. The variations in the simulated devices can be captured accurately using only the I_D-V_G characteristic reducing the computational burden of the 3-D "atomistic" device simulation [107, 111].

4.3.1 Ideal Device Extraction

Regardless of device geometry, accurate and physical compact model extraction for each device requires current-voltage characteristics at three distinct bias conditions.

- I_D-V_G with low V_D bias
- I_D-V_G with high V_D bias
- I_D-V_D with different V_G bias

Device behaviour targeted for extraction includes carrier mobility, threshold voltage, subthreshold region and short channel effects. The extraction procedure follows closely [112] with some extraction steps either skipped or modified, depending on the specific goals, while keeping compatibility as close as possible. The key to the physical extraction of the basic parameters is to extract the value

of the parameters from the correct physical phenomenon in the measured or simulated device on which the parameter is based. The BSIMSOI compact model parameter extraction strategy for the ideal device include the following steps:

1. V_{th0}, body effect parameters (K_1 and K_2) and low field mobility (μ_0) are extracted from I_D-V_G characteristics at low V_D. V_{th0} is the threshold voltage at zero substrate bias, V_B. This is one of the most important parameters governing the threshold voltage in BSIMSOI and should be a positive number for NMOS and negative for PMOS. As only NMOS devices have been simulated in chapter 3, V_{th0} together with μ_0 is used to artificially create a PMOS device. K_1 and K_2 are the first and second order body effect coefficient. These two parameters directly control the threshold voltage and are usually associated with heavy channel doping and large V_{BS} bias. μ_0 is the zero field mobility in the universal mobility formulation [113], when the device operating temperature is equal to *Tnom* the temperature at which the model parameters are extracted. In this work, for PMOS devices μ_0 is assumed to be half of the value obtained for NMOS devices.

2. Subthreshold swing (*Nfactor*), threshold voltage short channel effects (D_{vt0}, D_{vt1}) and subthreshold region offset voltage (V_{off}) parameters are extracted from I_D-V_G characteristics at low V_D. *Nfactor* is treated as a fitting parameter aiming to improve the fit between simulation and simulated data, as well as to accommodate various devices geometries under various bias conditions. *Nfactor* is extracted again when the related bulk charge coefficient, A_{bulk} is extracted. D_{vt0} and D_{vt1} are the first and second order coefficients describing the impact of the charge sharing on the threshold voltage in short channel devices. V_{off} provides an extra degree of freedom to improve the fit of off-current without re-optimisation of V_{th0} and μ_0 extracted earlier. It can be used in the simultaneous optimization of the drain current in both the subthreshold and the strong inversion regions.

3. Drain/source resistance related (R_{dsw}, *Prwg*) parameters are extracted from I_D-V_G characteristics at low V_D. R_{dsw} characterize the drain/source resistance per μm of gate width which exist right in the current path. A

large R_{dsw} value lowers the drive current and degrades the device transient performance. *Prwg* is the gate bias effect coefficient of R_{dsw}. Generally, *Prwg* is viewed as a fitting parameter without any physical significant.

4. Drain induced barrier lowering (DIBL) related parameters (*Eta0*, *Etab*, D_{sub}, P_{clm}) and saturation velocity (v_{sat}) parameter are extracted from I_D-V_G characteristics at high V_D. *Eta0* is the DIBL coefficient for threshold voltage calculation which is extracted by fitting the required magnitude of the DIBL correction to the threshold voltage. *Etab* is used to model the substrate bias effect on threshold voltage due to DIBL in short channel devices. *Etab* can be merely treated as a fitting parameter to improve accuracy of the threshold voltage behaviour with respect to the applied V_B. D_{sub} is the channel length dependence of DIBL effects on the threshold voltage. It is used to control the amount of threshold voltage change as a function of channel length. P_{clm} is the channel length modulation parameter in the calculation of the drain current. v_{sat} is the carrier saturation velocity at the nominal temperature *Tnom* and is a critical parameter determining the device current in short channel devices.

5. *Nfactor* and DIBL related parameters (*Eta0*, *Etab*, D_{sub}, P_{clm}) are extracted from I_D-V_D characteristics.

6. Channel length dependency parameter of the substrate charge coefficient (*A0*), non-saturation factors for R_{dsw} (A_1, A_2) and body charge coefficient related parameter (A_{gs}) are extracted from I_D-V_D.

The proposed extraction strategy accurately fits simulation data with RMS error less than two percent for the ideal 10 nm, 7.5 nm and 5 nm channel lengths UTB-SOI MOSFET. The good overall agreements between the ideal device simulation results and the extracted BSIMSOI model parameters is illustrated in figure 4.3. The quality of I_D-V_G fit for the 10 nm, 7.5 nm and 5 nm devices is shown in figure 4.3(a), 4.3(b), 4.3(c) respectively while I_D-V_D fit quality is illustrated in figure 4.3(d), 4.3(e), 4.3(f) respectively. Parameters which are insensitive to intrinsic fluctuations are fixed after this parameter extraction phase while a few BSIMSOI parameters are selected for extraction in the second-stage,

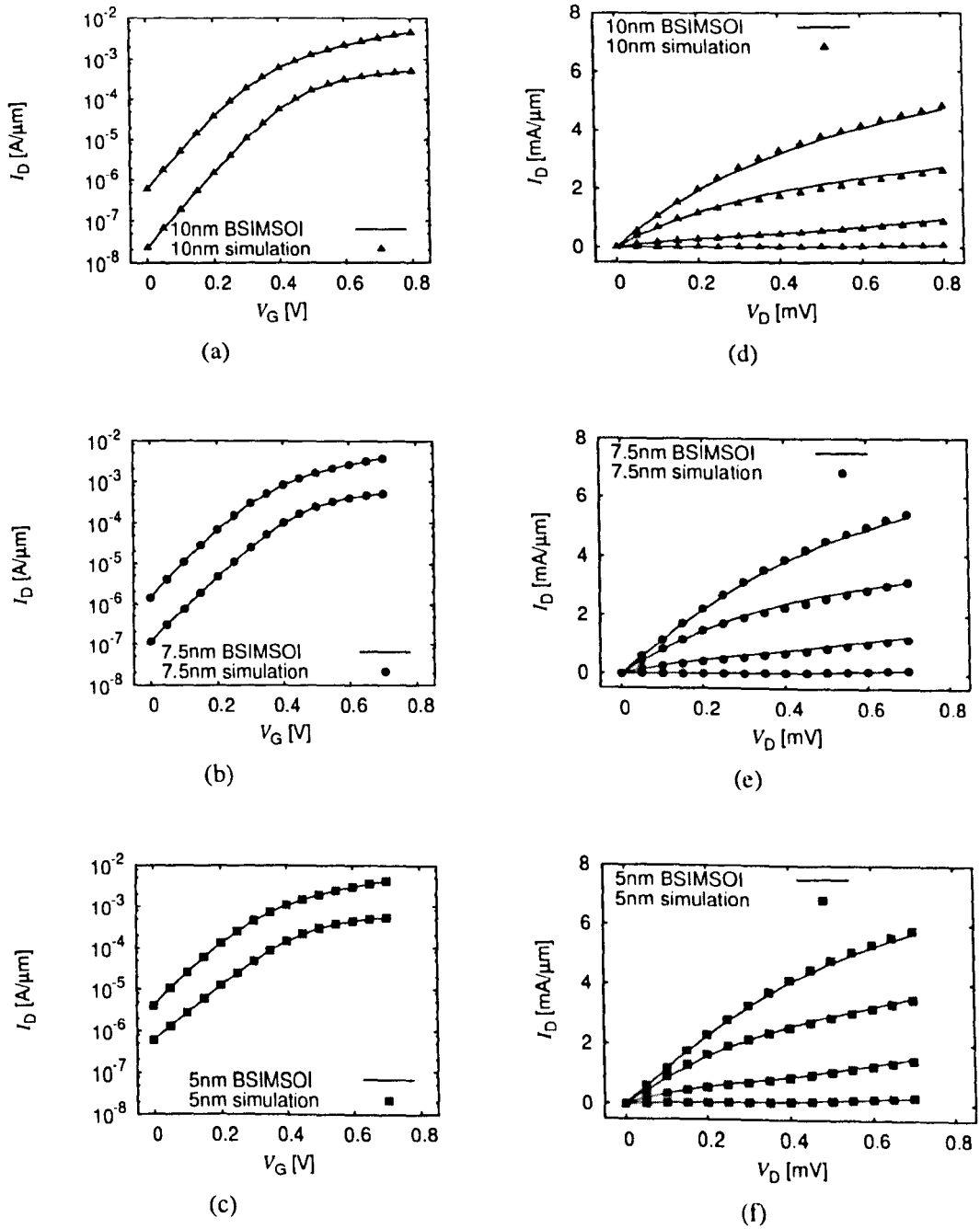


Figure 4.3: Quality of BSIMSOI extraction compared to ideal device simulation for equal body characteristics of uniformly doped 10 nm, 7.5 nm and 5 nm channel lengths UTB-SOI MOSFET.

to represent the variations in MOSFET characteristics due to intrinsic parameter fluctuations.

4.3.2 Atomistic Device Extraction

The stochastic nature of mismatch caused by IPF makes it necessary to use a large sample of electrical characteristics in order to have high confidence in the statistical circuit simulation. The data sets required for the statistical compact model extraction are from the simulations of 200 macroscopically identical, but microscopically different 10 nm, 7.5 nm and 5 nm channel length UTB-SOI MOSFET described in chapter 3. Using the extracted model parameters from the ideal device as base parameters, seven parameters are re-extracted using only I_D-V_G characteristics during the statistical extraction strategy. This data and parameters selection is based on previous findings that the impact of IPF characteristics can be accurately captured in compact models from I_D-V_G characteristics only [107, 111]. This approach reduce the computational burden of the 3D device simulation, making the simulation of I_D-V_D characteristics unnecessary. The focus of the statistical extraction strategy is on adjusting drain saturation current and threshold voltage because they play a dominant role in the simulation of digital circuits [111, 114].

The statistical parameter extraction strategy is carried out in two steps. The best accuracy fit at the end of each optimization step is ensured by setting aggressive error limits. The first step is based on the I_D-V_G characteristics at low drain bias, matching threshold voltage and sub-threshold slope using R_{dsw}, *Prwg*, *Nfactor* and V_{off} parameters. R_{dsw}, is only optimised for simulation of UTB-SOI MOSFET with random discrete dopants and the combined source of IPF. Then the saturation region of the device characteristics is matched at high drain bias using the parameters A_1, A_2 and D_{sub}.

In BSIMSOI, R_{dsw} and *Prwg* can reflect effective channel length variation and access resistance fluctuation in the strong inversion. In the case of BTV and LER, there is no strong influence of access resistance, therefore R_{dsw} is not required. The parameter *Nfactor* is re-optimised to improve the subthreshold fit, while the V_{off} parameter can be effectively used to reflect threshold voltage fluctuation caused

by each source of IPF individually or in combination. Parameters A_1 and A_2 mediate the saturation voltage, and therefore can be used to map IPF induced electric field fluctuations in the pinch-off region. Finally, D_{sub} is used to reflect atomistic fluctuation caused DIBL effects variation.

Table 4.2: Average and standard deviation of the relative RMS error from statistical BSIMSOI parameter extraction corresponding to choosen parameters for (a) low drain and (b) high drain bias.

	10 nm		7.5 nm		5 nm	
	μ	σ	μ	σ	μ	σ
BTV	1.40	0.61	0.35	0.11	0.46	0.18
LER	1.44	0.45	0.36	0.02	0.48	0.24
RDD	1.66	0.41	0.25	0.08	0.10	0.11
BTV+ LER+ RDD	1.83	0.71	1.81	0.21	0.29	0.10

(a)

	10 nm		7.5 nm		5 nm	
	μ	σ	μ	σ	μ	σ
BTV	0.51	0.70	0.83	0.13	1.42	0.22
LER	1.40	0.88	0.08	0.03	0.39	0.19
RDD	0.73	0.17	0.30	0.18	0.45	0.23
BTV+ LER+ RDD	2.03	1.53	0.58	0.08	0.19	0.14

(b)

To assess the accuracy of the device model and the statistical parameter extraction strategy, the I_D-V_G RMS relative percentage error is calculated between atomistic simulation data and the corresponding BSIMSOI results. Summary of the average and standard deviation of I_D-V_G RMS percentages error from the statistical extraction strategy for the 10 nm, 7.5 nm and 5 nm channel length UTB-SOI MOSFET including each source of IPF individually or in combination

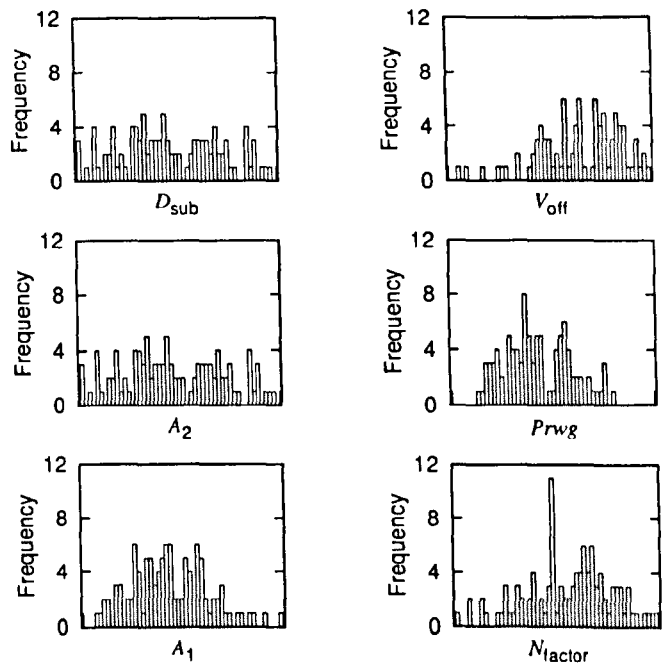


Figure 4.4: Distributions of selected BSIMSOI parameters from statistical extraction of 10 nm channel length UTB-SOI MOSFET with body thickness variations from an ensemble of 200 devices.

is shown in table 4.2. The mean RMS errors of the statistical compact model extraction from all channel lengths are less than two percent for each source of IPF for both extraction step. The I_D-V_G RMS errors have a very narrow normal distribution for the ensembles of 200 microscopically different transistors of each channel length and for each source of IPF. These results clearly demonstrate that the choice of seven key parameters adequately describes the effect of IPF over the whole range of device operation for all samples of devices with channel length of 10 nm, 7.5 nm and 5 nm. It is worth mentioning that the RMS error for the whole sample of transistors with a particular channel length depends on the accuracy of the ideal device parameter extraction and could be further improved by improving the extraction strategy.

Figure 4.4 shows the histograms of the selected BSIMSOI parameters from the statistical extraction of 10 nm channel length UTB-SOI MOSFET with body thickness variations. Each parameter has a different distribution with distinct

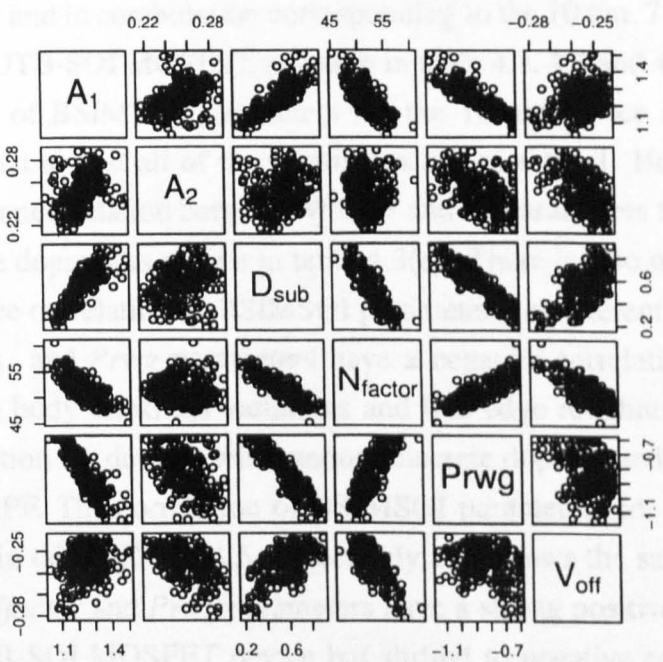


Figure 4.5: Scatter plots of selected BSIMSOI parameters from statistical extraction of 10 nm channel length UTB-SOI MOSFET with body thickness variations from an ensemble of 200 devices.

characteristics. Although BSIMSOI is developed with physical foundation, it still rely on smoothing functions, which are not physical. Therefore, acquiring a set of parameters which are uncorrelated are almost impossible. Figure 4.5 illustrates a scatter plots of the selected BSIMSOI parameters from the same device as above. The figure clearly illustrate that there are correlations between the selected BSIMSOI empirical process parameters choosen to reflect the body thickness fluctuation effects.

The detailed analysis of BSIMSOI parameter correlation for each source of IPF individually and in combination corresponding to the 10 nm, 7.5 nm and 5 nm channel length UTB-SOI MOSFET is shown in table 4.3, 4.4 and 4.5 respectively. The correlation of BSIMSOI parameters for the 10 nm device in table 4.3(a)-4.3(d), shows that almost all of the parameters are correlated. However, there is one instance of uncorrelation between *Nfactor* and A_I parameters for devices with random discrete dopants as shown in table 4.3(c). There is also no clear trend in the 10 nm device correlation of BSIMSOI parameter for different sources of IPF. For example, A_I and *Prwg* parameters have a negative correlation for the case of devices with body thickness variations and line edge roughness, but shows a positive correlation for devices with random discrete dopants and combination of all sources of IPF. The correlation of BSIMSOI parameters for the 7.5 nm and 5 nm depicted in table 4.4 and 4.5 respectively also shows the same observation. For example, *Nfactor* and *Prwg* parameters have a strong positive correlation for the 10 nm UTB-SOI MOSFET device but shifted to negative correlation as the device is scaled 5 nm channel length. Due to the statistical extraction strategy introduced in this work and the inherent limitation of the BSIMSOI model, correlation relationship between parameters is not important.

Table 4.3: Correlation of BSIMSOI parameters from statistical extraction of 10 nm UTB-SOI MOSFET for different sources of intrinsic parameter fluctuations. (a) BTV, (b) LER, (c) RDD and (d) BTV+LER+RDD.

	A_1	A_2	D_{sub}	*Nfactor*	*Prwg*	V_{off}
A_1	1.00	0.42	0.81	−0.73	−0.86	0.26
A_2	0.42	1.00	0.21	−0.02	−0.44	−0.50
D_{sub}	0.81	0.21	1.00	−0.85	−0.90	0.63
Nfactor	−0.73	−0.02	−0.85	1.00	0.79	−0.74
Prwg	−0.86	−0.44	−0.90	0.79	1.00	−0.34
V_{off}	0.26	−0.50	0.63	−0.74	−0.34	1.00

(a)

	A_1	A_2	D_{sub}	*Nfactor*	*Prwg*	V_{off}
A_1	1.00	−0.28	0.31	−0.05	−0.19	−0.18
A_2	−0.28	1.00	0.36	0.57	−0.77	−0.77
D_{sub}	0.31	0.36	1.00	−0.39	−0.12	−0.10
Nfactor	−0.05	0.57	−0.39	1.00	−0.85	−0.85
Prwg	−0.19	−0.77	−0.12	−0.85	1.00	1.00
V_{off}	−0.18	−0.77	−0.10	−0.85	1.00	1.00

(b)

	A_1	A_2	D_{sub}	*Nfactor*	*Prwg*	V_{off}	R_{dsw}
A_1	1.00	−0.29	−0.02	0.00	0.06	−0.11	−0.34
A_2	−0.29	1.00	0.08	0.46	0.46	−0.50	−0.41
D_{sub}	−0.02	0.08	1.00	−0.77	−0.70	0.62	0.66
Nfactor	0.00	0.46	−0.77	1.00	0.94	−0.89	−0.85
Prwg	0.06	0.46	−0.70	0.94	1.00	−0.88	−0.79
V_{off}	−0.11	−0.50	0.62	−0.89	−0.88	1.00	0.79
R_{dsw}	−0.34	−0.41	0.66	−0.85	−0.79	0.79	1.00

(c)

	A_1	A_2	D_{sub}	*Nfactor*	*Prwg*	V_{off}	R_{dsw}
A_1	1.00	−0.41	0.09	−0.19	0.21	0.41	−0.17
A_2	−0.41	1.00	0.46	−0.22	−0.33	−0.53	0.34
D_{sub}	0.09	0.46	1.00	−0.53	0.01	−0.20	0.01
Nfactor	−0.19	−0.22	−0.53	1.00	0.02	−0.36	−0.01
Prwg	0.21	−0.33	0.01	0.02	1.00	0.14	−0.88
V_{off}	0.41	−0.53	−0.20	−0.36	0.14	1.00	−0.19
R_{dsw}	−0.17	0.34	0.01	−0.01	−0.88	−0.19	1.00

(d)

Table 4.4: Correlation of BSIMSOI parameters from statistical extraction of 7.5 nm UTB-SOI MOSFET for different sources of intrinsic parameter fluctuations. (a) BTV, (b) LER, (c) RDD and (d) BTV+LER+RDD.

	A_1	A_2	D_{sub}	*Nfactor*	*Prwg*	V_{off}
A_1	1.00	−0.25	0.30	−0.69	−0.82	0.01
A_2	−0.25	1.00	0.28	0.22	0.17	−0.06
D_{sub}	0.30	0.28	1.00	−0.70	−0.68	0.81
Nfactor	−0.69	0.22	−0.70	1.00	0.85	−0.61
Prwg	−0.82	0.17	−0.68	0.85	1.00	−0.46
V_{off}	0.01	−0.06	0.81	−0.61	−0.46	1.00

(a)

	A_1	A_2	D_{sub}	*Nfactor*	*Prwg*	V_{off}
A_1	1.00	−0.58	−0.55	−0.18	−0.97	−0.97
A_2	−0.58	1.00	0.84	0.37	0.61	0.61
D_{sub}	−0.55	0.84	1.00	0.20	0.68	0.70
Nfactor	−0.18	0.37	0.20	1.00	0.07	0.10
Prwg	−0.97	0.61	0.68	0.07	1.00	1.00
V_{off}	−0.97	0.61	0.70	0.10	1.00	1.00

(b)

	A_1	A_2	D_{sub}	*Nfactor*	*Prwg*	V_{off}	R_{dsw}
A_1	1.00	−0.37	−0.24	0.36	0.41	−0.47	−0.50
A_2	−0.37	1.00	0.55	−0.13	−0.03	−0.05	0.18
D_{sub}	−0.24	0.55	1.00	−0.78	−0.47	0.37	0.53
Nfactor	0.36	−0.13	−0.78	1.00	0.79	−0.72	−0.76
Prwg	0.41	−0.03	−0.47	0.79	1.00	−0.64	−0.88
V_{off}	−0.47	−0.05	0.37	−0.72	−0.64	1.00	0.63
R_{dsw}	−0.50	0.18	0.53	−0.76	−0.88	0.63	1.00

(c)

	A_1	A_2	D_{sub}	*Nfactor*	*Prwg*	V_{off}	R_{dsw}
A_1	1.00	0.63	0.06	0.81	−0.43	−0.90	−0.92
A_2	0.63	1.00	0.22	0.64	−0.41	−0.63	−0.67
D_{sub}	0.06	0.22	1.00	−0.37	0.28	0.26	0.10
Nfactor	0.81	0.64	−0.37	1.00	−0.68	−0.98	−0.94
Prwg	−0.43	−0.41	0.28	−0.68	1.00	0.65	0.55
V_{off}	−0.90	−0.63	0.26	−0.98	0.65	1.00	0.96
R_{dsw}	−0.92	−0.67	0.10	−0.94	0.55	0.96	1.00

(d)

Table 4.5: Correlation of BSIMSOI parameters from statistical extraction of 5 nm UTB-SOI MOSFET for different sources of intrinsic parameter fluctuations. (a) BTV, (b) LER, (c) RDD and (d) BTV+LER+RDD.

	A_1	A_2	D_{sub}	*Nfactor*	*Prwg*	V_{off}
A_1	1.00	0.16	0.29	−0.66	−0.04	0.06
A_2	0.16	1.00	−0.23	0.17	−0.07	0.02
D_{sub}	0.29	−0.23	1.00	−0.35	−0.04	0.13
Nfactor	−0.66	0.17	−0.35	1.00	0.55	−0.25
Prwg	−0.04	−0.07	−0.04	0.55	1.00	−0.26
V_{off}	0.06	0.02	0.13	−0.25	−0.26	1.00

(a)

	A_1	A_2	D_{sub}	*Nfactor*	*Prwg*	V_{off}
A_1	1.00	−0.98	−0.35	−0.79	0.95	−0.51
A_2	−0.98	1.00	0.41	0.84	−0.97	0.53
D_{sub}	−0.35	0.41	1.00	0.84	−0.24	0.08
Nfactor	−0.79	0.84	0.84	1.00	−0.72	0.36
Prwg	0.95	−0.97	−0.24	−0.72	1.00	−0.55
V_{off}	−0.51	0.53	0.08	0.36	−0.55	1.00

(b)

	A_1	A_2	D_{sub}	*Nfactor*	*Prwg*	V_{off}	R_{dsw}
A_1	1.00	0.08	−0.03	−0.21	0.25	−0.15	−0.30
A_2	0.08	1.00	−0.18	0.58	−0.28	−0.13	−0.07
D_{sub}	−0.03	−0.18	1.00	−0.05	0.14	0.27	0.17
Nfactor	−0.21	0.58	−0.05	1.00	−0.28	0.08	0.36
Prwg	0.25	−0.28	0.14	−0.28	1.00	0.13	−0.22
V_{off}	−0.15	−0.13	0.27	0.08	0.13	1.00	0.30
R_{dsw}	−0.30	−0.07	0.17	0.36	−0.22	0.30	1.00

(c)

	A_1	A_2	D_{sub}	*Nfactor*	*Prwg*	V_{off}	R_{dsw}
A_1	1.00	−0.32	−0.04	0.45	0.0	−0.38	0.89
A_2	−0.32	1.00	−0.83	−0.09	0.0	0.72	−0.53
D_{sub}	−0.04	−0.83	1.00	0.08	0.0	−0.69	0.32
Nfactor	0.45	−0.09	0.08	1.00	0.0	−0.67	0.50
Prwg	0.0	0.0	0.0	0.0	0.0	0.0	0.0
V_{off}	−0.38	0.72	−0.69	−0.67	0.0	1.00	−0.56
R_{dsw}	0.89	−0.53	0.32	0.50	0.0	−0.56	1.00

(d)

4.4 Statistical Circuit Simulation

Worst and best case simulation is usually employed to predict the behaviour of the design. Typically this is achieved using a fixed parameters set describing nominal, worst and best processing conditions. Each individual parameter for a set of devices in a circuit is then put at their best or worst process corners. Thus there is a high risk of overly pessimistic or optimistic sets since it is unlikely that all individual parameter are at their extreme value at the same time. Conventional statistical circuit simulations such as Monte Carlo analysis rely on multivariate statistic such as Principle Component Analysis (PCA) [75, 76] to find a small number of uncorrelated parameters that together may explain most of the variation in the data. Such analysis is a powerful tool to understand parameter correlations but a practical and crucial problem exists because the resulting parameters only have mathematical meaning. Such an empirical approach could also create unrealistic devices and may not capture all physical fluctuation information.

The statistical extraction strategy introduced in this work captures accurately the IPF information from actual devices in a compact model library. This has implications for statistical circuit design. Rather than varying unphysical parameters or their corresponding ambiguous principal components, it is now possible to perform statistical circuit design using real devices. The compact model libraries built from ensembles of 200 microscopically different devices using the statistical extraction strategy described in this chapter are then used in circuit-level simulations. There are four different libraries for each of the 10 nm, 7.5 nm and 5 nm channel length UTB-SOI MOSFETs corresponding to each source of IPF investigated. Devices in a statistical circuit simulation can be randomly selected from the library of a corresponding channel length device and source of IPF, therefore would guarantee that the devices used in circuit simulations correctly represent realistic intrinsic parameter fluctuation effects.

4.5 Chapter Summary

In this chapter, a methodology for integrating "atomistic" device and circuit simulation of UTB-SOI MOSFET to analyse the impact of intrinsic parameter

fluctuations on corresponding circuits has been presented. The methodology consist of a two-stage statistical parameter extraction and a statistical circuit simulation. The two-stage statistical parameter extraction is able to accurately capture MOSFET characteristic fluctuations information obtained from the 3D 'atomistic' simulator into a representative set of BSIMSOI compact models. Using our statistical circuit simulation strategy, transistors used in circuit simulations have realistic intrinsic parameter fluctuation effects. The overall methodology allows to investigate different sources of intrinsic parameter fluctuations individually or in combination and could improve the general understanding of circuit stability and performance tolerance.

An increasingly important problem in manufacturing is how to deal with the effects of intrinsic parameter fluctuations on the behaviour of circuit. By assessing important circuits such as SRAM and CMOS logic, important intrinsic parameter fluctuations effects on circuits reliability, stability, timing issue, speed and power can be observed and dominant fluctuation effects in circuit operation can be identified. Using the statistical circuit simulation methodology described in this chapter, the impact of intrinsic parameter fluctuations on UTB-SOI based 6T SRAM cells will be investigated.

Chapter 5

6T SRAM Cells Simulation

5.1 Introduction

Intrinsic parameter fluctuations (IPF), introduced as a result of the underlying discreteness of charge and matter in ultra-small devices, will be one of the major challenges for the semiconductor industry in the next decade [1]. In most cases, the transistors used in SRAM cells are among the minimal size for each particular technology generation, and thus are critically sensitive to intrinsic parameter fluctuations [18, 115]. This intrinsic variation cannot be eliminated by tightening the manufacturing process control, and will have an increasing impact on SRAM performance and yield [13]. Failures due to the cumulative impact of various sources of IPF in an SRAM cells, are principally caused by mismatch between the neighboring active transistors in the cell. Mismatch in the characteristics of different transistors result in different types of failure event that includes destructive read or unsuccessful write, an increase in access time of the cell resulting in a violation of delay requirements, and destruction of the cell content in standby mode [17]. Increased failure rates in the cells of a memory array will reduce the yield of the associated chip.

So far, this thesis has addressed the effects of different sources of IPF on well scaled UTB-SOI MOSFETs, including the effects of random discrete dopants (RDD), body thickness variations (BTV) and line edge roughness (LER). The methodology to capture device fluctuation information obtained from the

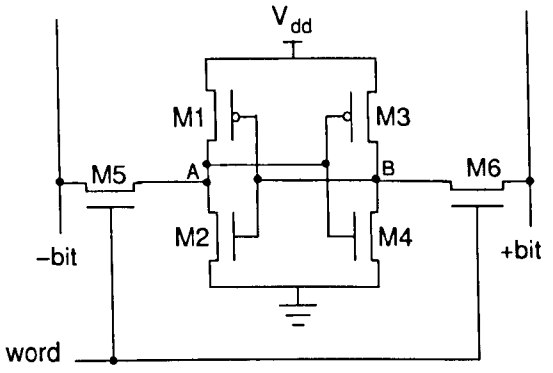


Figure 5.1: Circuit schematic of the 6-transistor SRAM.

3D 'atomistic' simulations into a representative set of BSIMSOI [22] compact models was presented in chapter 4. In this chapter, the impact of individual and combined sources of intrinsic parameter fluctuations on the static operation of next generation UTB-SOI SRAM cells is investigated using the BSIMSOI compact model library built earlier. The SRAM cells will be evaluated in terms of stability, performance and leakage with specific reference to the deviation of these properties from their nominal values, and the impact of this deviation on device yield.

In section 5.2 of this chapter, the SRAM architecture under consideration, circuit operating conditions and simulation strategy for statistical investigation of the impact of IPF on SRAM cells will be presented. In section 5.3, the stability of SRAM cells based on UTB-SOI MOSFETs with differing channel lengths and cell ratios is studied. Advantages of UTB-SOI MOSFETs, compared to conventional 35 nm bulk MOSFET [116] based SRAM cells, are also discussed. The impact of intrinsic parameter fluctuations on UTB-SOI SRAM cells, read and write characteristics are analysed and discussed in section 5.4. In section 5.5, SRAM cell leakage and static power dissipation is evaluated. Section 5.6, summarizes the results of this chapter.

5.2 Simulated SRAM Setup

In chapter 2 various memory configurations have been discussed. Each structure has been shown to be useful for specific applications. However, this thesis is primarily concerned with high-performance microprocessor cache, a market that has been totally dominated by the standard 6-transistor (6T) SRAM. With the projected growth in the percentage of chip area devoted to cache [117] in high-performance microprocessors, the impact of IPF on SRAM circuitry must be considered during the design cycle. A schematic of the 6T SRAM cells simulated in this work is shown in figure 5.1. The storage nodes (node A and node B) consists of two load PMOS transistors (M1 and M3) and two driver NMOS transistors (M2 and M4) with two access NMOS transistors (M5 and M6).

The specifications for supply voltage are obtained from the ITRS [1]. A supply voltage of 800 mV is used for the 10 nm transistor and 700 mV for both the 7.5 nm and 5 nm transistors. In order to study the statistical characteristics of SRAM cells subject to the intrinsic parameter fluctuations, a total of 200 unique SRAM cells are simulated in this work for each statistical simulation experiment. SRAM cells corresponding to 10 nm, 7.5 nm and 5 nm channel length UTB-SOI MOSFETs are constructed using randomly selected devices from the compact models library prepared earlier. Each compact models library comprise of 200 "atomistic" devices. So far in this work, only NMOS devices have been considered. In these simulations, PMOS devices are assumed to have an identical statistical distribution as a result of intrinsic parameter fluctuations, with a mobility half that of NMOS devices.

The impact of intrinsic parameter fluctuations on SRAM yield and performance is a strong function of the cell ratio, r defined as the ratio of the driver transistors (M2 and M4) width/length (W/L) to the access transistors (M5 and M6) W/L (5.1).

$$r = (W_d/L_d)/(W_a/L_a) \tag{5.1}$$

It will be shown that the probability of failure for any particular memory cell can be minimized by an optimal choice of r, achieved by appropriate sizing these transistors. However, any such optimization has an impact on the overall

silicon area, the static leakage and eventually the static power dissipation of the SRAM array. The impact of intrinsic parameter fluctuations on UTB-SOI devices is quantified by varying the SRAM cell ratio, r and measuring the stability and performance of the SRAM during read and write operations.

The cell ratio is altered by increasing the driver transistor width, while keeping the other transistor dimensions constant. High W/L ratio devices are often used in design, particularly when high drive currents are required. In this work, the load and access transistors have a W/L ratio of one while the driver transistor W/L ratio is determined by the choice of r. Larger W/L ratio devices are built by connecting in parallel randomly selected transistors from the compact models library, as the library contains only device with W/L=1. Neglecting edge effects, this technique correctly captures the statistics of wider devices.

To clearly illustrate the impact of intrinsic parameter fluctuations on SRAM cells, the peripheral read and write circuitry is omitted from the circuit simulation and ideal complementary signals are directly applied to the bit-lines. SRAMs are frequently placed near active logic circuits where the temperature of the die is high, and subthreshold leakage current will dominate cell leakage [118]. To distinguish IPF effects from temperature effects the 6T SRAM circuit was simulated at 300 K.

5.3 Cell Stability

In SRAM design, the stability of the cell is a critical factor in determining its sensitivity to process tolerances and operating conditions. Thus, is a critical factor in obtaining the desired yield of a chip. Each 6T SRAM cell contains two sets of matched inverters, as shown in figure 5.1 and for a given cell design, higher threshold voltage for each cell transistor improves cell stability. Any mismatch between the transistors caused by intrinsic parameter fluctuations between the pair degrades the stability of the whole cell. In this section, static noise margin and switch point voltage analysis are used to capture different aspects of SRAM cells read and write operation stability.

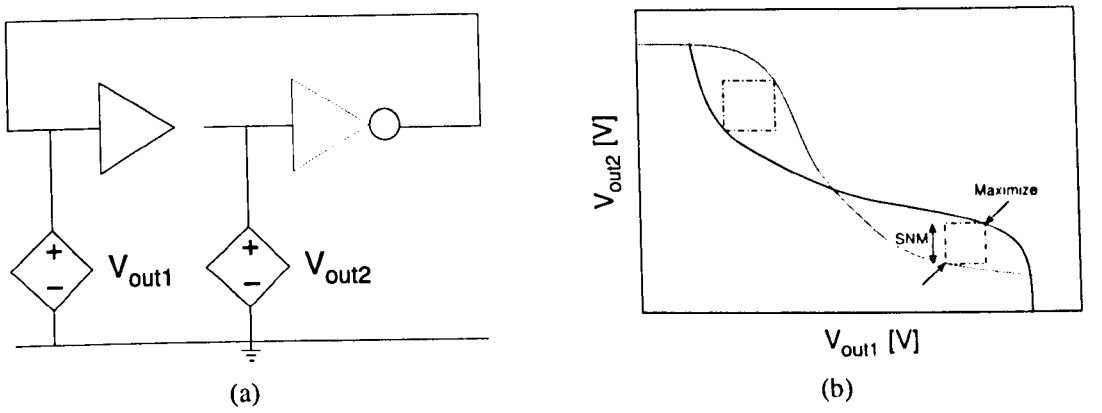


Figure 5.2: (a) SRAM cell represented by two inverters with static noise voltage sources included. (b) Graphical representation of SNM.

5.3.1 Static Noise Margin

Reading information from an SRAM cell should be non-destructive. After the read operation the logic state of the cell must remain unaltered. 6T SRAM cell is most unstable at the onset of the reading access. The read operation begins with the word-line being raised to the power supply voltage, V_{dd} and bit-lines initially precharged high. This causes the logic low node within the cell to rise due to the voltage division between driver transistors and access transistors. If the cell design allows the nominal value of this node voltage to come close to the nominal threshold voltage of the driver transistors, IPF caused by process variations may result in the node voltage passing the critical point where the state of the cell is flipped. The Static Noise Margin (SNM) [101], which is the minimum DC noise voltage needed to flip the cell state, is often used to measure the cell stability. SNM is a function of threshold voltage and depends on the relative strength of the two cross-coupled inverters in the cell. A large threshold voltage improves SNM and the cell state could only be flipped by large DC noise. However, as the electrical parameters of the transistors in these inverters are prone to intrinsic fluctuations, the SNM varies from memory cell to memory cell.

An SRAM cell can be represented by a flip-flop comprised of two inverters as shown in figure 5.2(a). SNM is simulated by using two voltage sources (V_{out1} and V_{out2}) which are placed inside the memory cell to obtain the static transfer

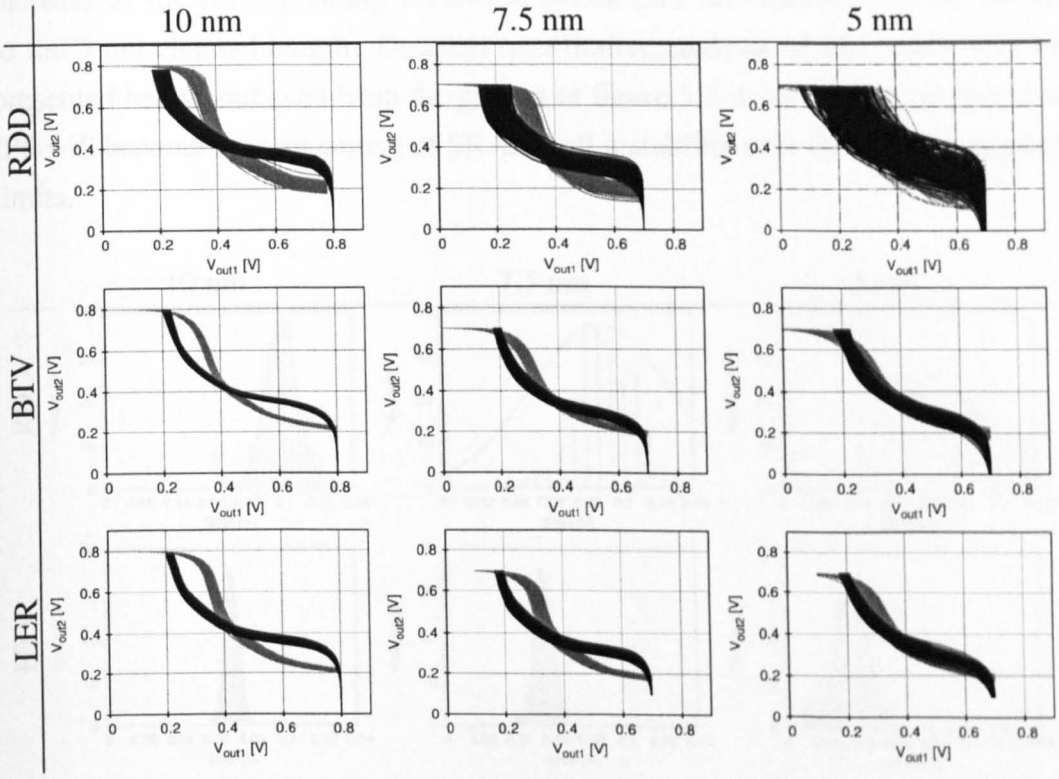


Figure 5.3: Static transfer curves of 200 distinct SRAM cells with a cell ratio of one. The columns represent UTB-SOI MOSFET channel lengths while the rows indicate the corresponding sources of intrinsic parameter fluctuations.

curve of each inverter. The static noise margin can be obtained graphically by drawing and mirroring the inverter characteristics and fitting the maximum possible square between the two curves as depicted in figure 5.2(b). For well matched transistors, the curves are symmetrical and the two SNM are the same. However, when intrinsic parameter fluctuations are included, the two maximum squares are different and the smallest of the two is defined as the SNM. Increasing cell ratio [119] and other circuit techniques such as dynamic-threshold SRAM [120] that push both of the static transfer curves away from each other will improve cell SNM, but will never eliminate the impact of IPF altogether.

Static transfer curves for an ensemble of 200 distinct SRAM cells with a cell ratio of one, considering transistor parameter variations resulting from RDD, BTV and LER, are shown in figure 5.3. The fluctuations of the static transfer curves

increase as the corresponding UTB-SOI MOSFETs are scaled from the 10 nm to the 5 nm channel length. Detailed quantitative analysis of the results will be presented below, but even from the groups of figure 5.3 it can clearly be seen that IPF will become a major source of SRAM cell instability near the ultimate scaling limits.

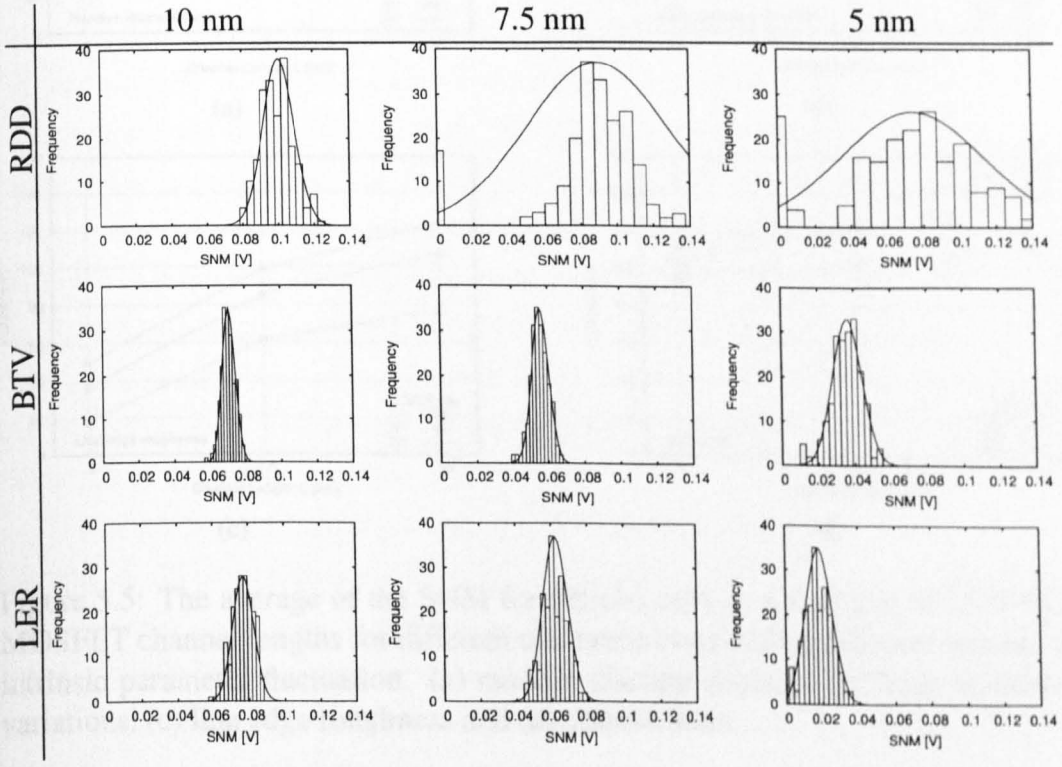


Figure 5.4: SNM distributions due to different sources of IPF in UTB-SOI based SRAM cells with a cell ratio of one. The columns represent UTB-SOI MOSFETs channel lengths while the rows are the corresponding sources of intrinsic parameter fluctuations.

To better visualize and compare the overall effects of different sources of IPF on the stability of 6T SRAM cells, SNM distributions for SRAM cells with 10 nm, 7.5 nm and 5 nm transistors are illustrated in figure 5.4. For all three sets of devices, the distribution of the SNM is close to a normal distribution, with an increasing standard deviation with channel length reduction. As noted above, the SNM fluctuations due to RDD shown in the first row are the worst for all UTB-SOI MOSFETs channel lengths. RDD also causes a considerable proportion of

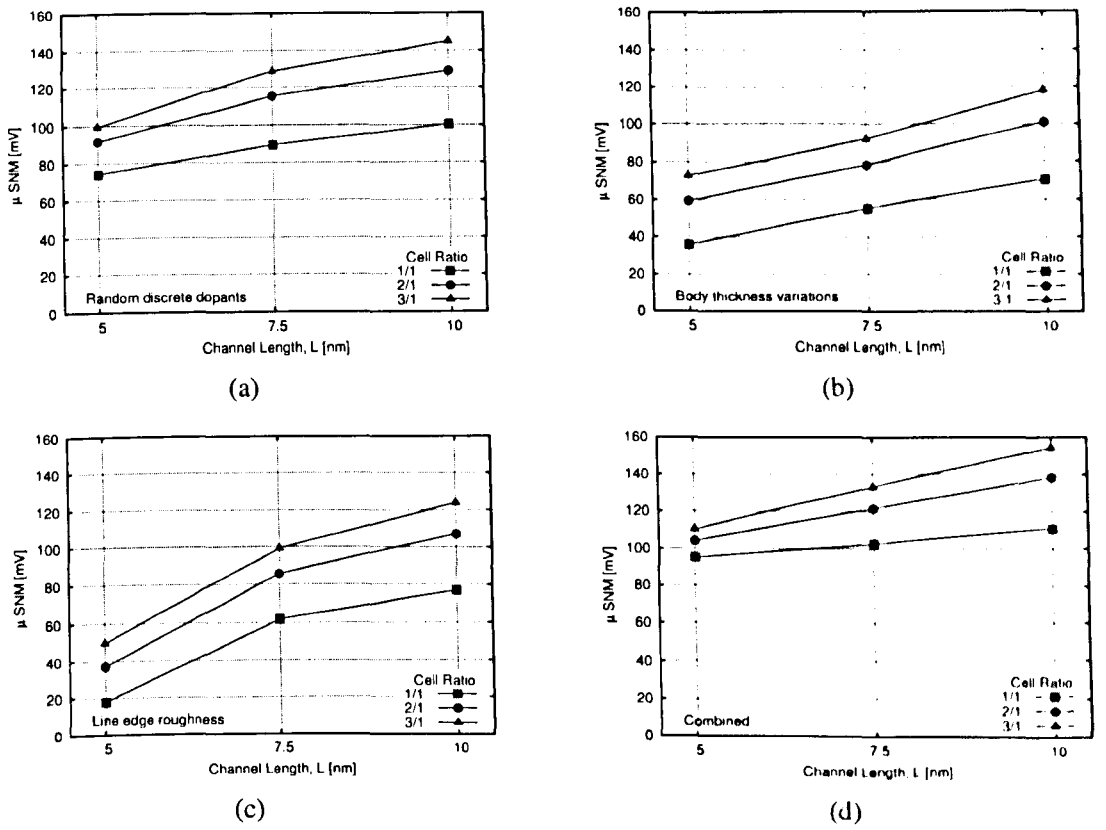


Figure 5.5: The average of the SNM for SRAM cells as a function of UTB-SOI MOSFET channel lengths for different cell ratios considering different sources of intrinsic parameter fluctuation. (a) random discrete dopants, (b) body thickness variations, (c) line edge roughness and (d) combination.

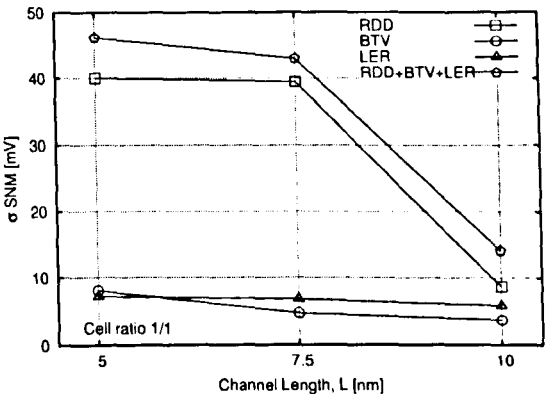
devices at the 7.5 nm and 5 nm channel length fail to operate even under otherwise ideal conditions. The impact of RDD on SNM has already been expected from UTB-SOI MOSFET simulation results in chapter 3. RDD caused a threshold voltage standard deviation, σV_T of 25 mV and 75 mV for the 7.5 nm and 5 nm UTB-SOI MOSFET. As SNM is a function of threshold voltage, noise margin will be eliminated if SRAM cell are built from transistors with extreme threshold voltage lowering. Approximately 10 percent failure rate at 7.5 nm channel length and a 13 percent failure rate at 5 nm channel length.

Figure 5.5 illustrates the average SNM for SRAM cells based on UTB devices with different cell ratios, considering each source of IPF individually and in combination. It clearly shows the expected trend that by increasing the cell ratio,

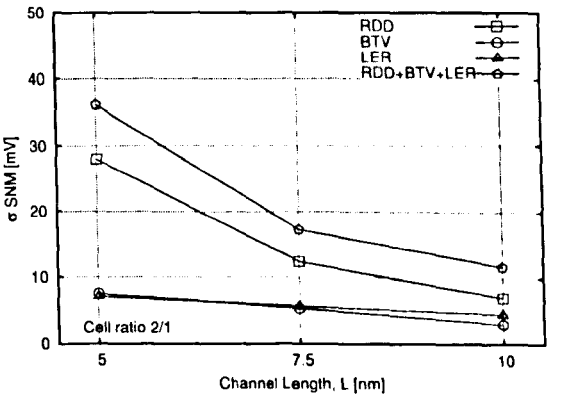
the cell stability for all UTB-SOI channel length is improved. The improvement of average SNM are much larger in longer channel length device. For SRAM cells built from transistors with the presence of all source of IPF shown in figure 5.5(d), the average SNM for the 10 nm devices is increased by 40 mV while the average SNM for 7.5 nm and 5 nm are only increased by 30 mV and 20 mV respectively. The impact of each individual source of IPF on the average SNM are depicted in figure 5.5(a) to figure 5.5(c). Comparing the average SNM between each source of IPF individually or in combination from figure 5.5(a) to figure 5.5(d) gives a false notion that SNM of SRAM cell with the presence of all source of IPF are much better. This is in fact not true as this is related to the statistical behaviour of the average threshold voltage, $\langle V_T \rangle$ from the ensemble of 200 UTB-SOI MOSFETs observed in chapter 3. As explained earlier, SNM is a function of threshold voltage and in the presence of all sources of IPF, the average threshold voltage, $\langle V_T \rangle$ is the highest, thus giving a skewed impression of a better SNM. To clearly compare the impact of each source of IPF individually or in combinations, the standard deviation of the mean must be used.

The channel length dependence of SNM standard deviation, due to different sources of IPF for different cell ratio configuration are illustrated in figure 5.6. For all case of cell ratio configuration, SRAM cells built from transistors with the presence of all IPF source have the largest standard deviation. In the presence of all IPF sources, SRAM cells with minimum cell ratio (r=1), have a standard deviation of 14 mV for the 10 nm channel length device, increasing to 34 mV for the 5 nm device. The impact of each individual source of IPF on the SNM standard deviation are depicted in figure 5.6(a) to figure 5.6(c). SRAM cells built from transistors with the presence of BTV and LER have a standard deviation of less than 10 mV. For all case of cell ratio configuration, LER dominates at longer channel length. However, there is a crossover below 7.5 nm channel length.

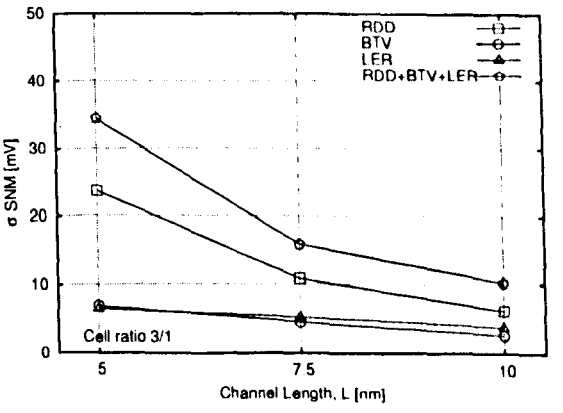
To facilitate the comparison of standard deviation between different channel length, the normalised standard deviation (σ/μ) of the SNM is calculated. Figures 5.7 illustrate the normalised standard deviation of the SNM due to different sources of IPF as a function of UTB-SOI MOSFETs channel length for SRAM cells with different cell ratios. The magnitude of the fluctuations increase as the UTB-SOI MOSFETs are scaled to shorter channel length. Although SNM



(a)

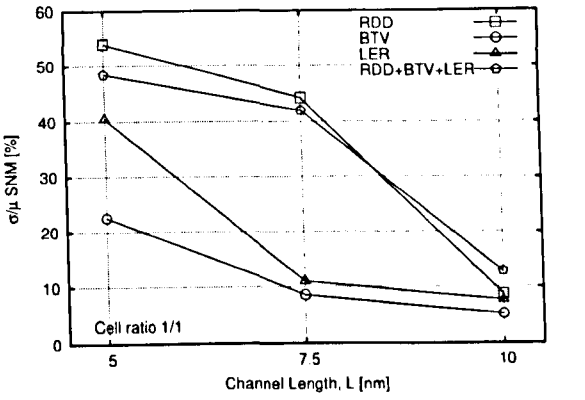


(b)

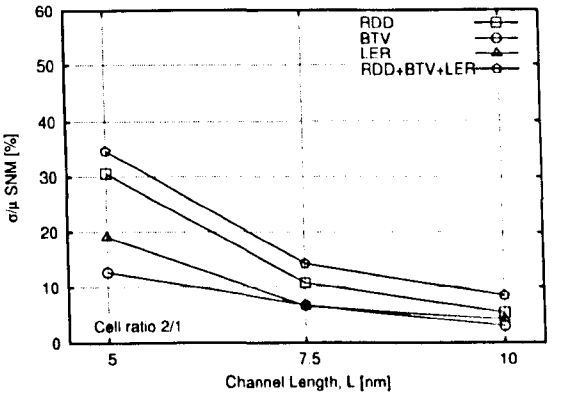


(c)

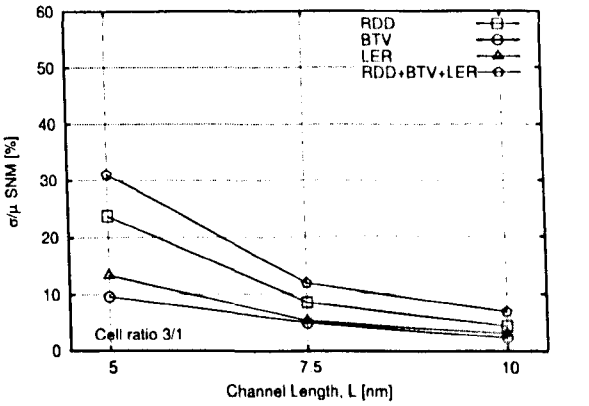
Figure 5.6: Standard deviation of SNM due to different sources of IPF in SRAM cells that utilises 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs, with SRAM cell ratios of (a) 1/1, (b) 2/1 and (c) 3/1.



(a)



(b)



(c)

Figure 5.7: Normalised standard deviation of SNM due to different sources of IPF in SRAM cells that utilises 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs, with SRAM cell ratios of (a) 1/1, (b) 2/1 and (c) 3/1.

fluctuations remain well under control for the 10 nm channel length device, at minimum cell ratio, primarily as a result of increasing variation due to RDD the normalised SNM standard deviation for 7.5 nm and 5 nm channel length devices are considerably degraded. Compared to combined source of IPF, the steep degradation of the average SNM of RDD causes a rapid growth and crossover of the SNM normalised standard deviation at minimum cell ratio. BTV and LER result in less than 15 percent normalised standard deviation for the 10 nm and the 7.5 nm devices but increases to more than 20 percent for the the 5 nm SRAM. The magnitude of fluctuation for transistors with combined sources of IPF (RDD+BTV+LER) increases from approximately 10 percent at 10 nm channel length to more than 31 percent at 5 nm channel length, for SRAM with a cell ratio of one despite the effect of BTV and LER continuing to be well controlled for the 7.5 nm device.

The negative impact of IPF increase with the transistor scaling can be compensated by increasing the SRAM cell ratio. Increasing the cell ratio not only improves the average SNM as discussed earlier, but also reduces the magnitude of its fluctuations which is partly reflected by the reduced normalized standard deviation. The increase of the cell ratio delivers between 10 and 30 percent reduction of the SNM fluctuation for 7.5 nm and 5 nm UTB-SOI MOSFETs for different sources of IPF. However increasing cell ratio delivers less improvement of the SNM with the reduction of the channel length. For the 5 nm transistors, the need to increase cell ratio will reduce the benefit of the device scaling compared to 10 nm and 7.5 nm channel length transistors.

As the number of transistors per chip continues to increase, SNM fluctuations must be small enough to satisfy future yield requirements. For example, a 4 MB (32 Mbit) cache, including error correction, usually contains almost 38 million memory cells and requires a tolerance of 5.44σ to have only one cell failure per cache [115]. A common technique when considering yield is to apply the six-sigma (6σ) approach, adopted by Motorola [102]. Devices operating outside 6σ from the mean value (μ-6σ) will occur on average only 3.4 times per million devices. Calculated values of μ-6σ from ensembles of 200 distinct SRAM cells built from 10 nm and 7.5 nm UTB-SOI MOSFETs are plotted in figure 5.8 as a function of cell ratio. It is clear that an increase in cell ratio

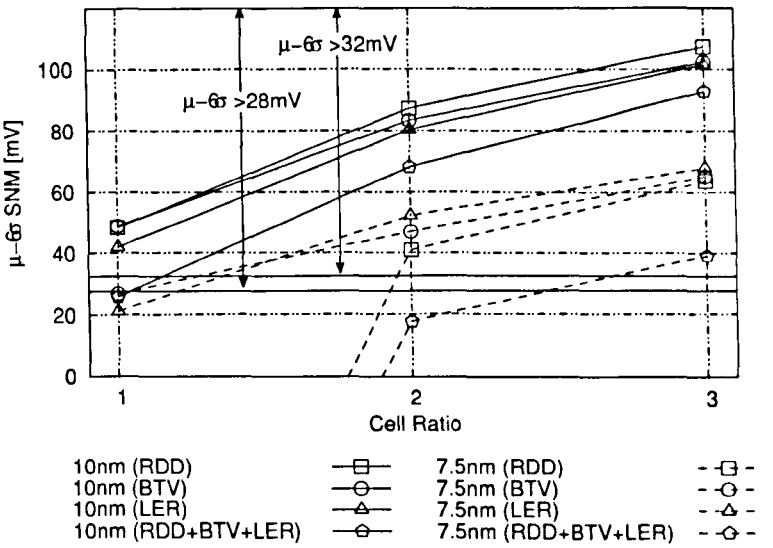


Figure 5.8: μ-6σ of Static Noise Margin (SNM) as a function of cell ratio for 10 nm, and 7.5 nm UTB-SOI MOSFET SRAMs. Lines: μ-6σ>32 mV for 10 nm and >28 mV for 7.5 nm.

leads to an improvement in μ-6σ which implies improved SRAM cell yield. As a guideline for SRAM, μ-6σ should exceed 4 percent of the supply voltage to achieve 90 percent yield on 1 Mbit SRAMs [121]. This criteria is satisfied for a cell ratio of one for 10 nm channel length devices for any individual source of IPF. However, if the combination of sources of IPF is taken into account, the 10 nm channel length device will require at least a cell ratio of two. The 7.5 nm channel length UTB-SOI MOSFET SRAM requires a cell ratio of two if only BTV or LER are considered in isolation and a cell ratio of three for either RDD, or a combination of all sources of IPF. SRAM cells based on 5 nm channel length devices could not fulfill the required guideline even at higher cell ratios. Resorting to higher cell ratios only increases cell area, negating the improved storage density that is one of the main reason for scaling devices to shorter channel length. This implies that 6T SRAMs will not gain the full benefits from further UTB MOSFET scaling to channel lengths smaller than 10 nm.

5.3.2 Switch Point Voltage

Writing data into 6T SRAM cell is performed by applying opposite signals on each bit-line. This forces the cell into the state defined by the bit-lines. While SRAM read operation stability requires a large and stable SNM, it is also important to have a reasonably low switch point voltage (SPV), defined as the bit-line voltage which will cause cell data to begin to change under a write operation [115]. The cell internal nodes (node A and node B) remain in their initial state until the SPV is reached. Then the node storing the logic low rises suddenly, the high node falls, and the cell switches state. The SPV must be far enough from both supply voltage (V_{dd}) and ground so that no combination of offsets and noise can cause a write failure or even an accidental write when a read is intended.

The average switch point voltage for different UTB-SOI MOSFET based SRAM cells as a function of cell ratio are shown in figure 5.9(a), 5.9(b) and 5.9(c). Usually, a symmetric 6T memory cell has a switch point voltage that is slightly less than the half of the power supply, V_{dd} [115]. Optimal switch point voltage results in better noise immunity. However, SRAM cells subject to IPF have an average SPV of more than 60 percent of the power supply voltage for 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFET devices. For all the devices under consideration, increasing the cell ratio from r=1 to r=3 results in approximately 20 percent higher switch point, making it more difficult to write into the cell. The SPV fluctuations caused by different sources of IPF, individually or in combination, are relatively insensitive to cell ratio. An increased cell ratio does not result in any significant reduction in the magnitude of the fluctuations as shown in figure 5.9(d), 5.9(e) and 5.9(f). The combination of all sources of IPF causes approximately a 12 percent normalised standard deviation in the value of SPV. Upon further inspection, it can be seen that the 6σ range, for all cell ratios is close to the ground ($\approx$100 mV) or greater than the supply voltage (700 mV). Additionally, almost 5 percent of the 5 nm channel length cells are unwritable due to either a combination of all IPF effects, or solely due to RDD, even at a cell ratio of one.

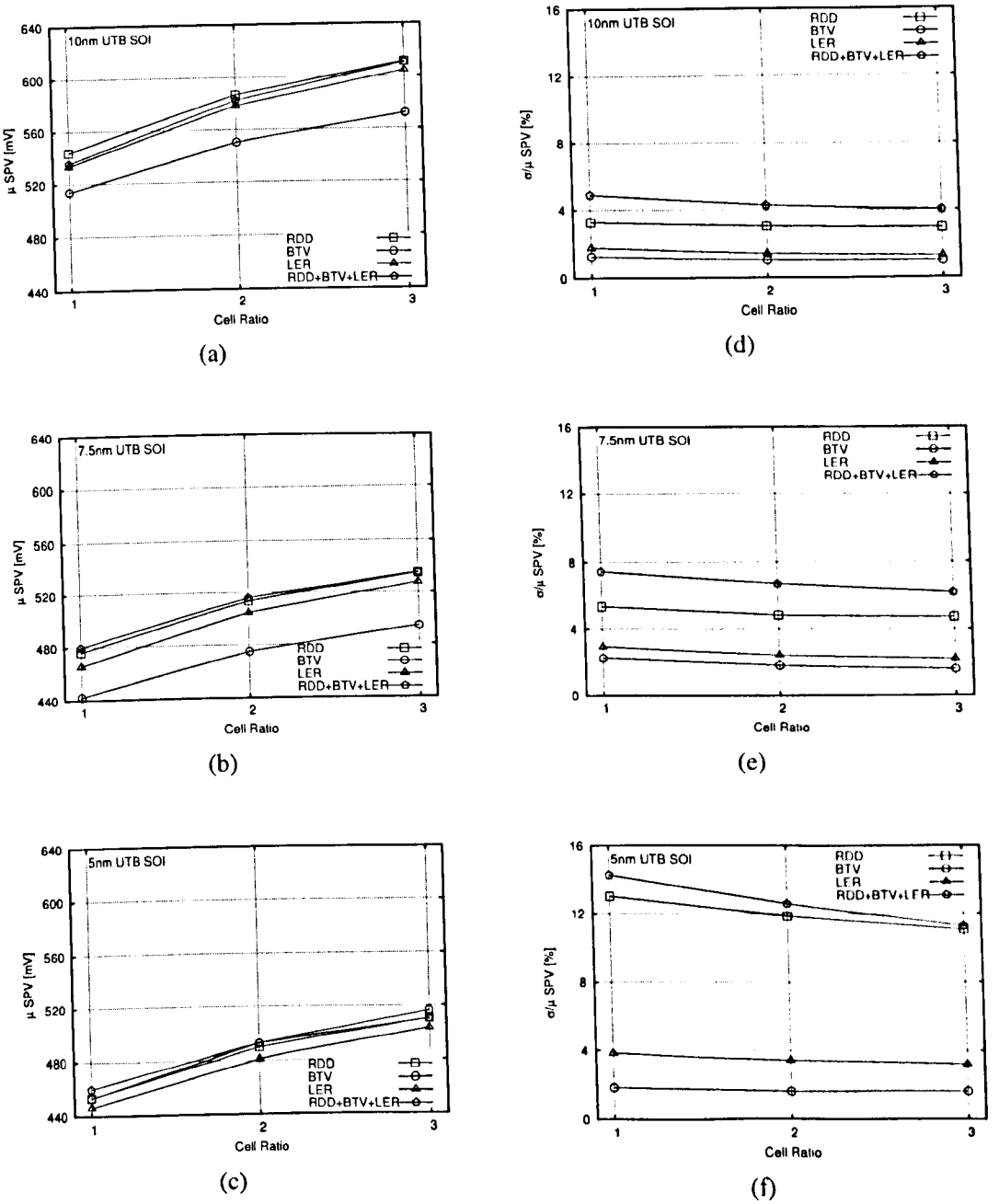
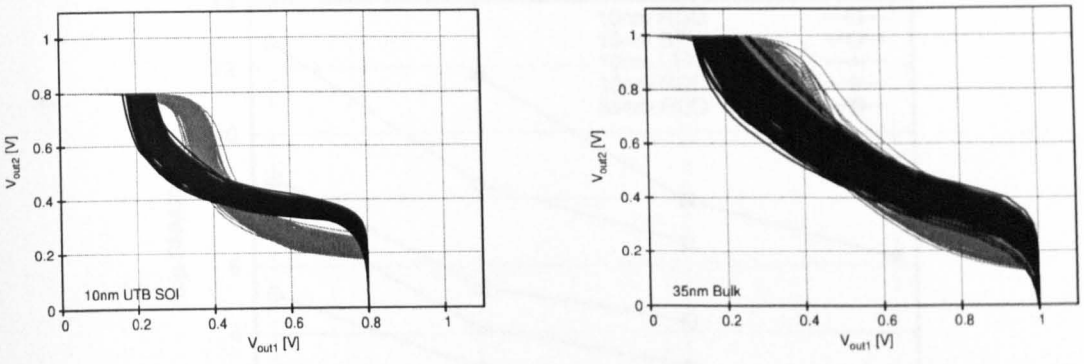


Figure 5.9: Average switch point voltage for (a) 10 nm, (b) 7.5 nm and (c) 5 nm UTB-SOI MOSFET SRAMs as a function of cell ratio with different sources of intrinsic parameter fluctuation. $V_{dd}/2$ is 400 mV for 10 nm SRAMs and 350 mV for both 7.5 nm and 5 nm SRAMS. Normalised standard deviation of switch point voltage as a function of cell ratios for (d) 10 nm, (e) 7.5 nm and (f) 5 nm UTB-SOI MOSFET SRAMs.



(a) (b)

Figure 5.10: Static transfer characteristics of 200 distinct SRAM cells utilising (a) 10 nm UTB-SOI MOSFETs and (b) 35 nm bulk MOSFETs.

5.3.3 UTB-SOI vs Bulk MOSFETs

To show the practical advantages of UTB-SOI MOSFET based SRAM cells with respect to stability in the presence of IPF, a comparison is made between 10 nm channel length UTB-SOI MOSFET memory cells and cell structured from well calibrated 35 nm bulk devices [19]. The static transfer curves for an ensemble of 200 SRAM cells built from 10 nm channel length UTB MOSFETs, considering the combination of IPF sources (RDD+BTV+LER) is shown in figure 5.10(a). The opening of the butterfly transfer curves for 10 nm UTB-SOI can be clearly compared to the results obtained for SRAM constructed from 35 nm conventional bulk MOSFETs shown in figure 5.10(b). The worse bulk MOSFET performance for an identical cell ratio configuration is due to larger fluctuations resulting from the random discrete dopants in the channels of the bulk devices. A recent experimental study [13] has confirmed the adverse effect of random doping fluctuations on the yield and stability of SRAM cells.

Normalised standard deviation of the SNM as a function of cell ratio for SRAM constructed from UTB-SOI MOSFETs and bulk devices is depicted in figure 5.11. The UTB-SOI MOSFET cells are simulated for cell ratios from r=1 to r=3. Bulk MOSFET cells cannot operate with a cell ratio of one and are simulated with cell ratios from r=2 to r=4. The trend of increased SNM stability is observed for 35 nm bulk MOSFET based memory cells as the cell ratio

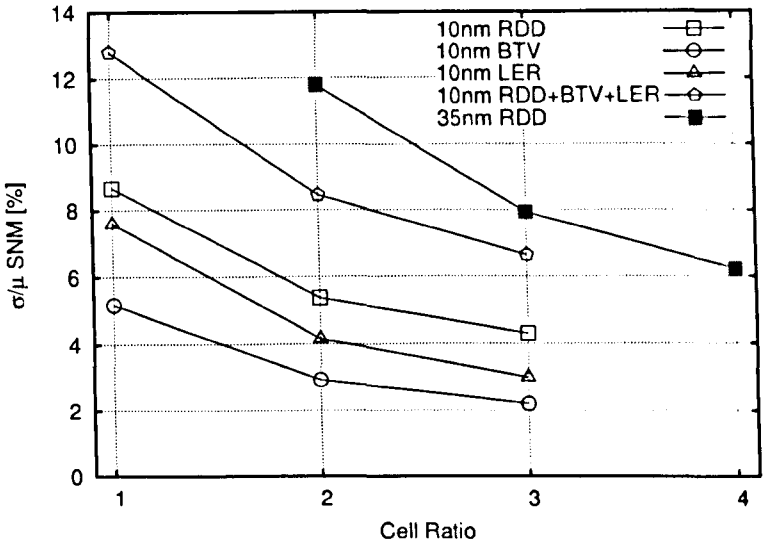


Figure 5.11: Normalised standard deviation of SNM as a function of cell ratio for 10 nm UTB-SOI MOSFET based SRAM due to different sources of IPF. Equivalent results for SRAM constructed from 35 nm bulk MOSFETs are also shown. The bulk devices are only subjected to random discrete dopants.

is increased. However, SRAM cells based on 35 nm bulk MOSFETs are more sensitive to the random doping effects compared to 10 nm UTB-SOI MOSFETs with the combination of all IPF sources.

The calculated μ-6σ dependence on cell ratio is compared in figure 5.12 from SRAM cells utilising 10 nm UTB-SOI and 35 nm bulk MOSFET. It is clear that for both devices the increase of the cell ratio leads to improvement in μ-6σ which implies that a larger fraction of SRAM cells for each geometry achieve stability threshold. A memory cell based on 35 nm bulk MOSFETs requires a cell ratio of at least three, considering only intrinsic fluctuations caused by discrete random dopants. According to figure 5.12, from the SNM point of view, 10 nm UTB-SOI MOSFET SRAM cells are more stable even though operated at 80 percent of the supply voltage of 35 nm bulk MOSFET based SRAM.

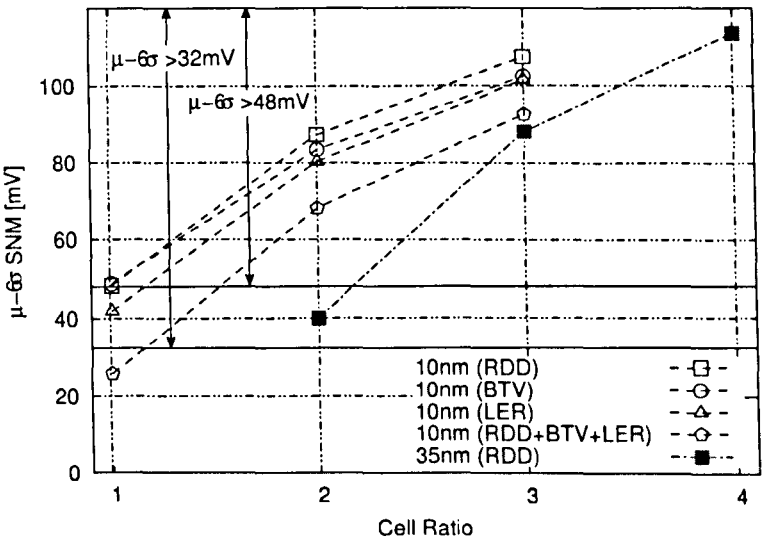


Figure 5.12: μ-6σ for SNM as a function of cell ratio for SRAM constructed from 10n m UTB-SOI MOSFETs and 35 nm bulk MOSFETs with different sources of intrinsic parameter fluctuations. Lines: μ-6σ >32 mV for 10 nm UTB-SOI MOSFETs and >48 mV for 35 nm bulk MOSFETs.

5.4 Cell Performance

The performance of an SRAM array is determined by the read and write operation of its slowest cell. A read operation is performed by holding both bit-lines high and selecting the desired word-line. Once the word-line is enabled, data in the cell will pull one of the bit-lines low through the access transistor (M5, M6) and driver transistor (M2, M4). The differential signal on the bit-lines is detected, amplified and read out through the output buffer [122]. One important performance parameter is the read access time which represents the propagation delay from the time when the address is presented at the memory chip until the time when data become available at the memory output.

In this work, in order to obtain the relative read operation speed, the discharge time for the bit-line is estimated from the simulation of an ensemble of 200 6T SRAM cells for each of the investigated UTB-SOI MOSFETs. The read discharge time (RDT) is a major component in determining array access time, and the overall chip speed is fundamentally limited by the cell discharge time.

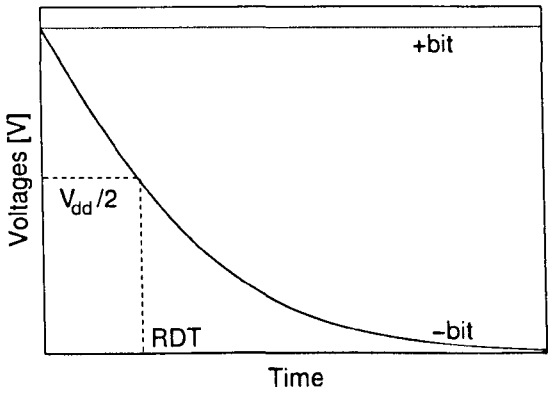


Figure 5.13: A typical read discharge-time simulation waveforms. Both bit-lines are initially precharged at supply voltage and RDT is measured when bit-line voltage drop to $V_{dd}/2$.

The RDT will be affected by the bit-line capacitance which depends on both the architectural configuration of the memory array and the UTB-SOI MOSFETs choosen. However, in the following statistical circuit simulations a constant 0.05 pF bit-line capacitance is assumed. In order to secure a sufficient noise margin, the threshold for the sense amplifier is assumed to be half of the supply voltage. The read discharge time is defined by the bit-line voltage drop to the sense amplifier threshold after the access transistors are switched on as shown in figure 5.13.

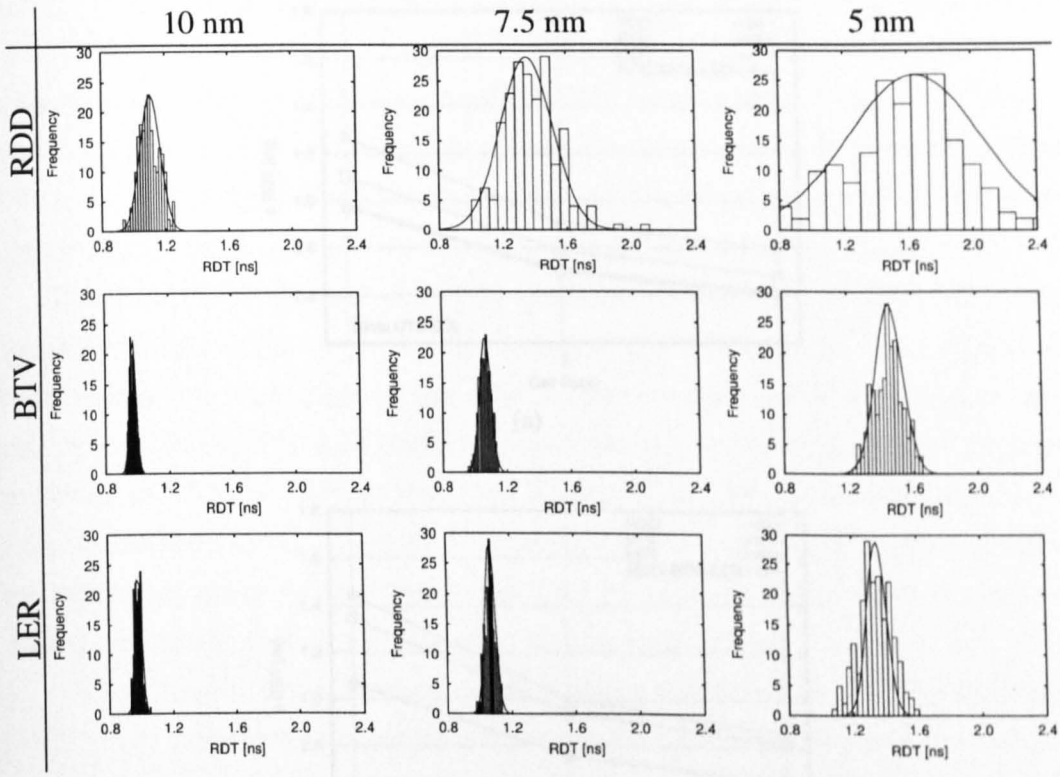
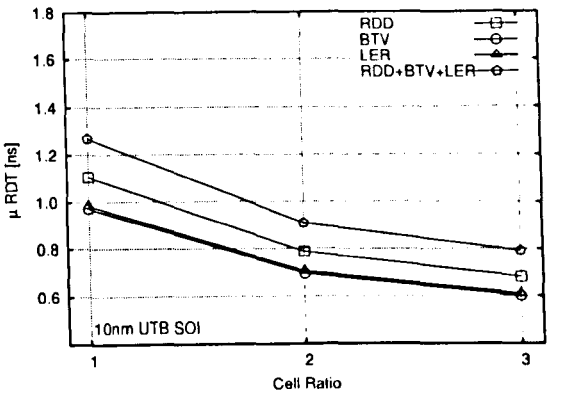


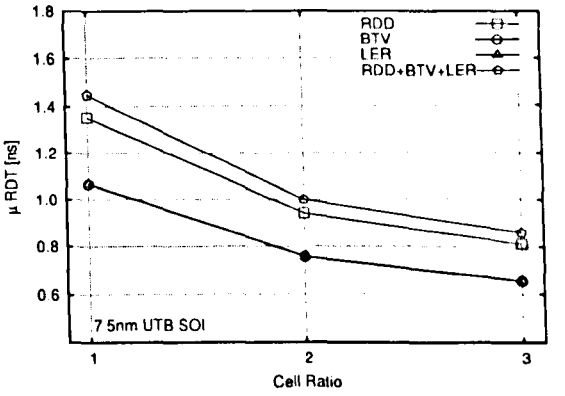
Figure 5.14: Read discharge time distributions for UTB-SOI MOSFET based SRAM cells with a cell ratio of one. The columns represent UTB-SOI MOSFET channel lengths while the rows are the corresponding sources of intrinsic parameter fluctuations.

The histogram of the read discharge time distributions for different channel lengths of UTB-SOI MOSFETs with different sources of IPF are presented in figures 5.14. Each source of IPF has a different impact on the average read performance of the SRAM cells, but more importantly, IPF causes significant performance differences between the fastest and slowest SRAM cell accesses and may cause a violation of the delay requirements for reliable memory cell operation at a specific clock frequency.

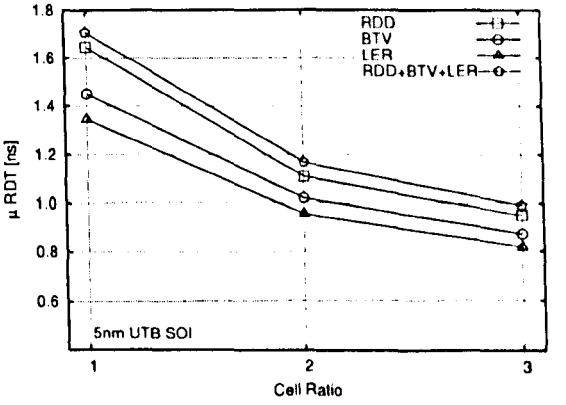
Under nominal conditions, the discharge time for each UTB-SOI MOSFET investigated improves between 17 and 25 percent with the increase of the cell ratio to two, and between 31 and 75 percent with the increase of the cell ratio to three considering all sources of IPF in combination. These results, together with the effects of each single sources of fluctuations are illustrated in figure 5.15.



(a)



(b)



(c)

Figure 5.15: Average of read discharge time as a function of cell ratio with different sources of intrinsic parameter fluctuation for (a) 10 nm, (b) 7.5 nm and (c) 5 nm UTB-SOI MOSFET based SRAM cells.

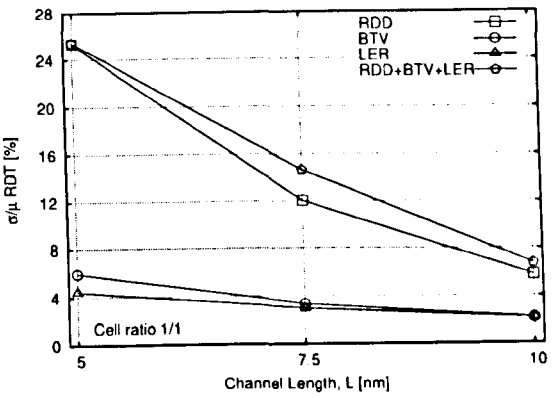
Larger cell ratios reduce the cell pull down time due to increasing current drive from larger driver transistor, which will help to improve general read access performance. However it is also clear that IPF have a negative impact on SRAM cell read access time. From the three individual sources of IPF investigated in this work, RDD has the worst impact on read discharge time with performance degradation greater than the effect of any other single source of fluctuations.

The normalised standard deviation illustrated in figures 5.16 shows that even though nominal speed improves due to larger cell ratios, there is no significant reduction in the variations of the read access between SRAM cells even at a cell ratio of three. The read performance difference for devices in the individual presence of BTV or LER is less than 5 percent for any UTB-SOI MOSFETs. RDD considered either solely or in combination with other IPF sources result in the worst variations in read discharge time of approximately 6 percent for the 10 nm transistors, raising to 24 percent for the 5 nm devices.

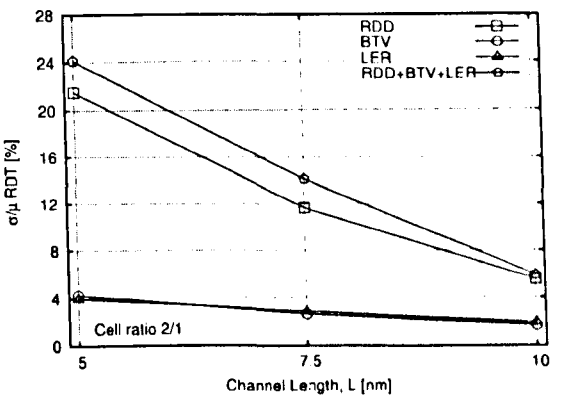
Although write time is not one of the critical requirements for SRAM design [122], large variations in write time may still disrupt functionality of the memory arrays. Unlike read discharge time, write operation is not affected by bit-line capacitance, assuming that a constant voltage is applied to flip the cell. In this work, the write time is measured from the time the access transistors are switched on after applying an appropriate value to the bit-lines, to the moment when the two internal storage nodes reach 90 percent of their final value. The worst case flip time is recorded as the write time for the cells as illustrated in figure 5.17.

The average write times for all investigated UTB-SOI MOSFETs are presented in figures 5.18. It is important to note that although a higher cell ratio improves stability, it degrades the write performance, as a higher voltage is required to flip the storage nodes. IPF further contributes to the degradation of write performance, extending the time needed to flip an SRAM cell contents. A compromise must be made between SRAM cell stability and write performance. However, in most cases cell stability is more important than write speed.

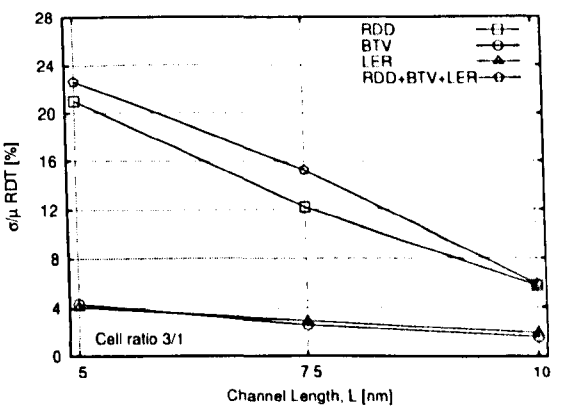
The normalised standard deviation of write times for different channel lengths of UTB-SOI MOSFET based memory cell is shown in figures 5.19. Similar to the case of read performance, the magnitude of fluctuations in SRAM cells write performance becomes worst as the UTB-SOI MOSFET based SRAM is scaled



(a)



(b)



(c)

Figure 5.16: Normalised standard deviation of read discharge time as a function of channel length with different sources of intrinsic parameter fluctuation for UTB-SOI MOSFET based SRAM cells with cell ratio of (a) 1/1, (b) 2/1 and (c) 3/1.

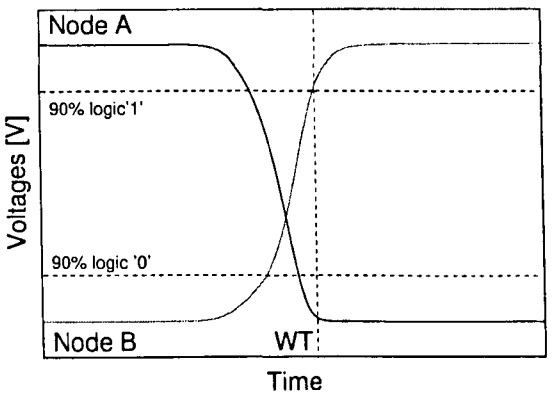
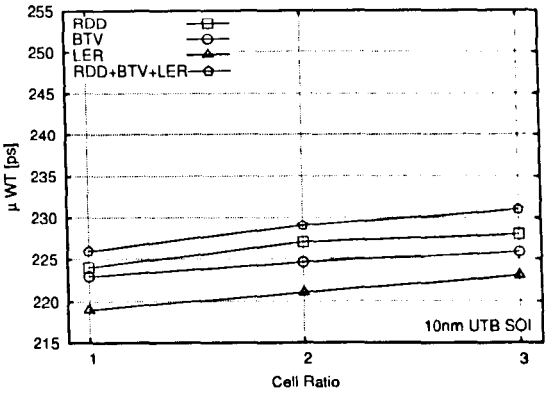
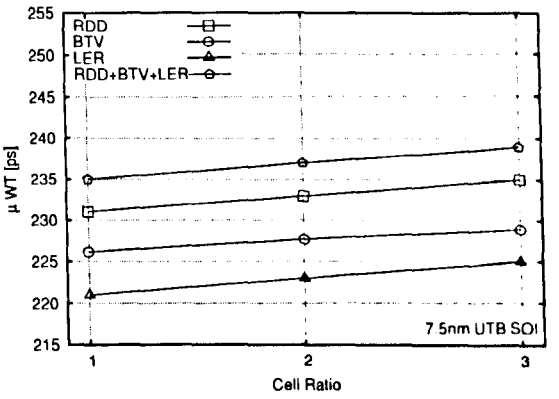


Figure 5.17: Write-time simulation with constant voltage applied to bit-lines.

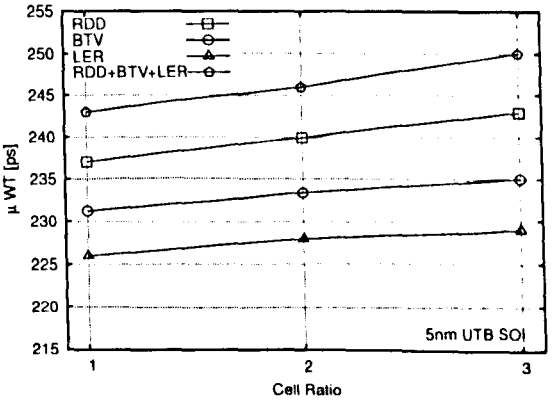
from 10 nm to 5 nm channel length especially in the presence of RDD. Another important conclusion that can be drawn from the results plotted in figures 5.19 is that write time fluctuation is also less sensitive to an increase in cell ratio. There is almost no reduction in the magnitude of write time variation for any of the simulated UTB-SOI MOSFET as the cell ratio is increased from r=1 to r=3.



(a)

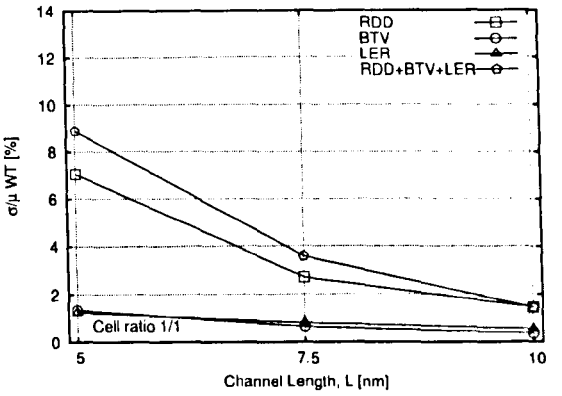


(b)

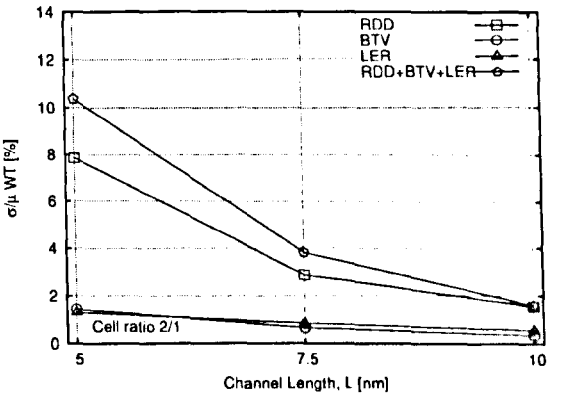


(c)

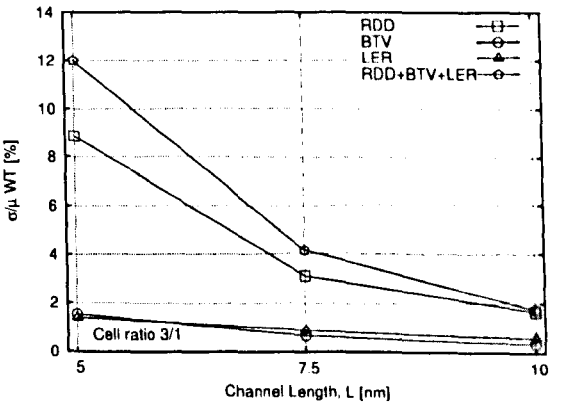
Figure 5.18: Average write time as a function of cell ratio with different sources of intrinsic parameter fluctuations for (a) 10 nm, (b) 7.5 nm and (c) 5 nm UTB-SOI MOSFET based SRAM cells.



(a)



(b)



(c)

Figure 5.19: Normalised standard deviation of write time as a function of channel length with different sources of intrinsic parameter fluctuation for UTB-SOI based SRAM cells with cell ratios of (a) 1/1, (b) 2/1 and (c) 3/1.

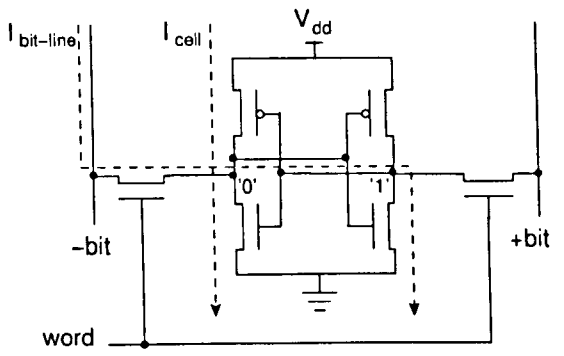


Figure 5.20: Dominant leakage paths for 6T SRAM cells. Bitline leakage, $I_{\text{bit-line}}$ is the leakage from bit-line to ground and cell leakage, I_{cell} is the leakage from V_{dd} to ground.

5.5 Leakage and Power Dissipation

While yield and performance are key issues for high performance SRAMs, leakage and power consumption cannot be neglected. The total leakage in a memory cell is primarily caused by the sub-threshold leakage, the gate leakage, and the junction leakage through different transistors in the cell. Another important component of leakage in SRAM circuits is associated with the current discharge of the bit-lines capacitance [105], which is dependent on the physical layout of the memory cell arrays. Basically, the bit-line capacitance is mainly due to the drain capacitance of the access transistors of the memory cell that share electrical connections with millions of other cells in its column and the total interconnect capacitance to these access transistors.

The simulations presented here will only consider the leakage and power dissipation associated with a single memory cell during static or standby operation. Presently, static power dissipation is comparable to dynamic power [51] and is predicted to become more important as MOSFET is scaled in the nanometre region. According to a projection from Intel, the static leakage component of the total power in a microprocessor may exceed dynamic power as the technology decreases below the 65 nm technology generation [29].

During standby, the word-line is held low so that the two access transistors are off, isolating the cell from the bit-lines. In this state, most of the leakage

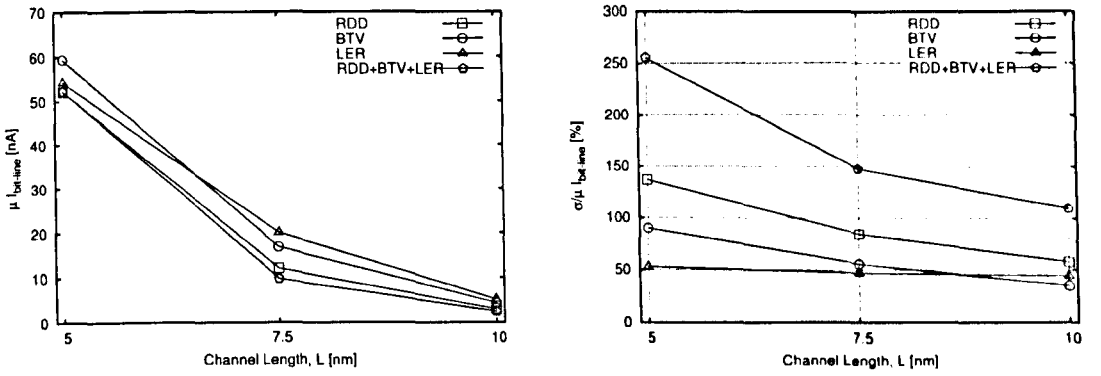


Figure 5.21: (a) Average and (b) normalised standard deviation of bit-line leakage, $I_{bit\text{-}line}$ for 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFET based SRAM cells with different sources of intrinsic parameter fluctuations.

is dissipated by the transistors that are in their off state. The two dominant leakage paths for a 6T SRAM cells are the bit-line to ground ($I_{\text{bit-line}}$) and V_{dd} to ground (I_{cell}) as shown in figure 5.20. Leakage through these two paths makes up 93 percent of the total leakage [123].

The bit-line leakage, $I_{bit\text{-}line}$ is interesting from two different perspectives. One is that it contributes to the total power dissipation and the other is a performance issue. During a read or write cycle, unselected cells in a column of the memory array act as a leakage source discharging the bit-lines. Therefore, the minimum delay to read and write data to a cell to some extent also depends on other memory cells on the bit-line. Figure 5.21 depicts the channel length dependence of the mean and normalised standard deviation of bit-line leakage from UTB-SOI MOSFET based SRAM cells storing a logic low. The mean of the bit-line leakage is approximately 5 nA for 10 nm devices increasing non-linearly to 53 nA for 5 nm devices considering the combination of all sources of IPF. No one particular sources of IPF produces a significantly different mean bit-line leakage. These results are plotted in detail in figure 5.21(a). Overall IPF also causes a much worse normalised standard deviation for bit-line leakage of more than 40 percent for all UTB-SOI MOSFETs as depicted in figure 5.21(b). Note that the impact of LER on bit-line leakage is almost constant as the UTB-SOI MOSFET based

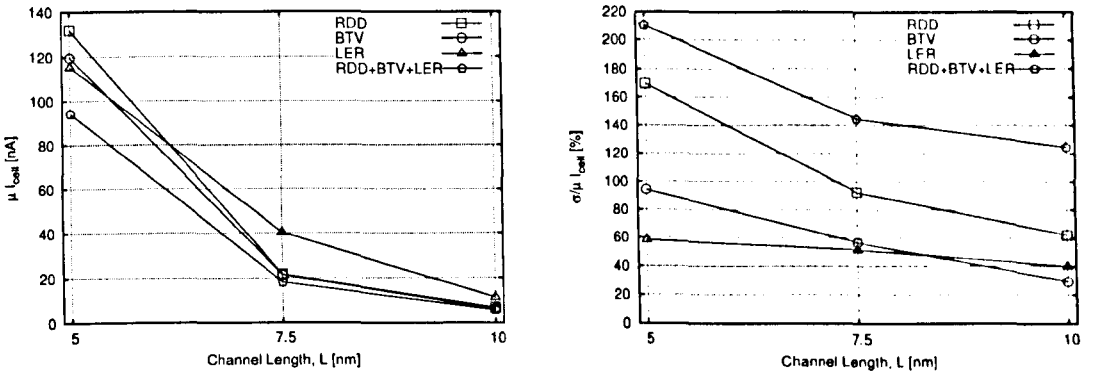


Figure 5.22: (a) Average and (b) normalised standard deviation of cell leakage, I_{cell} for 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFET based SRAM cells with different sources of intrinsic parameter fluctuations.

SRAMs are scaled to smaller channel lengths because the LER parameter are also scaled according to the requirement of the ITRS [1].

The cell leakage, I_{cell} is the total leakage through the latch and is very important for the overall static power dissipation of the system. The total static power dissipation of the memory array is the sum over the total ensemble of cells and should be capped to a defined level to prevent the chip from overheating, or reducing the battery life for low power applications. To clearly isolate the cell leakage of the SRAM cells in simulations, the access transistors are switched off and the bit-lines are held low to prevent the bit-lines leakage contribution to the total leakage. The mean cell leakage for 10 nm devices is approximately 5 nA, increasing non-linearly as the UTB-SOI MOSFETs are further scaled. For the 5 nm devices, the average leakage for the combined source of IPF is 90 nA. The effect of the individual and combined sources of IPF on average cell leakage is shown in detail in figure 5.22(a). As illustrated in figure 5.22(b), the cell leakage has a similar trend of the channel length dependence of the normalized standard deviation as the bit-line leakage.

The projected amount of static power dissipation for SRAM cache arrays with 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs is depicted in figure 5.23. The static power is calculated by multiplying the sum of bit-line and cell leakage

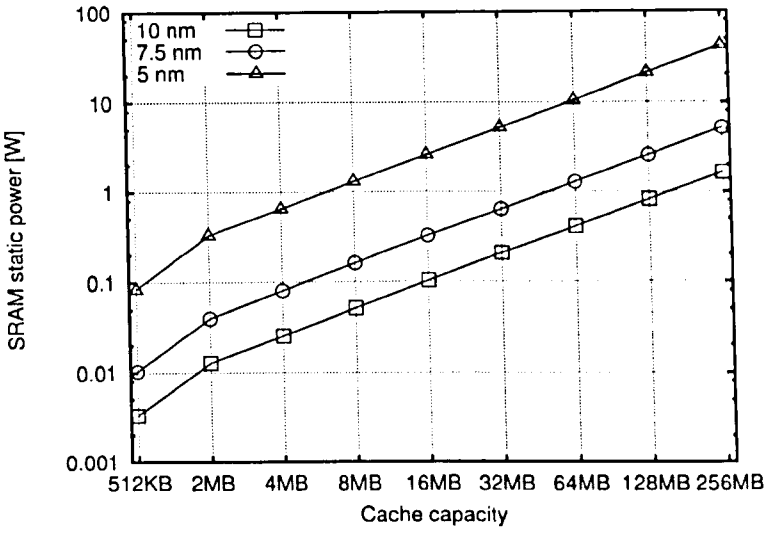


Figure 5.23: Static power in SRAM arrays as a function of projected cache capacities for 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFETs considering all sources of intrinsic parameter fluctuations in combination.

with projected stand-by supply voltage to obtain the static power dissipation per SRAM array. To maintain sufficient noise margin, a nominal power supply voltage of 560 mV for the 10 nm SRAM arrays and 490 mV for the 7.5 and 5 nm SRAM arrays are chosen. The nominal power supply has been chosen by multiplying the corresponding power supply voltage to the 'subtreshold slope adjustment factor' of single gate UTB-SOI MOSFETs (0.7) [1]. The subthreshold slope adjustment factor takes account of using advance UTB and double-gate MOSFETs. Specifically, this is a multiplying factor for the subthreshold slope, reducing it towards its minimum ideal value of 60 mV/decade. Conventional bulk MOSFET has a factor of one, while UTB-SOI MOSFET has a factor ranges of 0.7 to 0.8. As cache memory in microprocessors is projected to double with each successive technology generation, the projected static power shown in figure 5.23 is obviously unacceptable, bearing in mind that the cell leakage used in this projection is the raw statistical average, without consideration of the spread, peripheral circuitry and the temperature effects which would need to be accounted for in an industrial setting. The increase in leakage current outweighs the reduction in supply voltage at each channel length, with a net effect of increase

in static power dissipation.

5.6 Chapter Summary

The cumulative impact of the intrinsic parameter fluctuations introduced by random discrete dopants, body thickness variations and line edge roughness in UTB-SOI MOSFETs on the operation of 6T SRAM cells has been investigated using a statistical circuit simulation methodology. From the yield point of view, the operation of 6T SRAM may not gain the full benefits from further UTB-SOI MOSFET scaling to channel lengths smaller than 10 nm. At a cell ratio of one, there is approximately 10 percent failure rate for SRAMs with 7.5 nm transistors and 13 percent failure rate for SRAMs with 5 nm transistors. Increasing cell ratio delivers less improvement of the SNM with the reduction of the channel length and does not reduce the magnitude of SNM standard deviation. The major source of device mismatch in UTB-SOI MOSFETs is the random discrete dopants in the source and drain region. Applying the six-sigma tolerance criteria, in the presence of all sources of IPF, 10 nm UTB-SOI MOSFET based SRAM cells require at least a cell ratio of two, while 7.5 nm SRAM cells requires at least a cell ratio of three.

The stability advantages of SRAM cells utilising UTB-SOI MOSFET compared to bulk MOSFET SRAM cells has also been discussed. The operation of 10 nm UTB-SOI MOSFET based SRAM cells is more stable compared to 35 nm bulk MOSFET memory cells even though operated at 80 percent of the supply voltage. Therefore, the transition to UTB-SOI technology could extend the benefits of SRAM scaling beyond the 25 nm technology generation. However, simulation results show that the intrinsic parameter fluctuations is becoming one of the major factors limiting the integration of UTB-SOI into billion transistor count chips for transistors with channel length below 10 nm.

The significant impact of intrinsic parameter fluctuations especially random discrete dopants on the performance of UTB-SOI MOSFET based SRAM cells cannot be ignored. SRAM simulation considering combination of all sources of intrinsic parameter fluctuations show 6 to 24 percent access performance difference between fastest and slowest SRAM cells which may cause violation of delay requirement for reliable memory cell operation.

It is also anticipated that intrinsic parameter fluctuations will increase the overall leakage of cache memory, contributing to an increasing fraction of static energy consumption for the next generation high performance microprocessors. The combined effect of large cache structures (>16 MB) and large leakage current results in expected power dissipation nearing 100 mW for high performance 10 nm UTB-SOI MOSFET based SRAM cells and more than a watt for 5 nm based SRAM cells. Increased power translates to more heat which in turn degrades performance and reliability.

Chapter 6

Conclusions

The aim of this thesis was to investigate the impact of different sources of intrinsic parameter fluctuations in next generation UTB-SOI MOSFETs on the functionality and the performance of the corresponding 6T-SRAM cells. This covers three different aspects of UTB-SOI MOSFET device modelling and simulation. The first aspect is the device-level modelling, applied to study the impact of intrinsic parameter fluctuations in a family of well scaled UTB-SOI MOSFETs. The inclusion of different sources of intrinsic parameter fluctuation allows detailed analysis on important electrical characteristics of the scaled devices. The second aspect is the development of a statistical circuit modelling framework which takes into account the intrinsic parameter fluctuations in UTB-SOI MOSFETs. This methodology provides a link between device-level and circuit level modelling of intrinsic parameter fluctuation. The simulation results obtained from device-modelling simulation have been translated into a compact model framework for use in circuit-level simulation. The third aspect is statistical circuit-level modelling applied to study the influence of different sources of intrinsic parameter fluctuations on 6T SRAM based on UTB-SOI MOSFETs.

In Chapter 2, a literature review embracing various aspect of this thesis has been presented. The scaling limitation of conventional bulk MOSFET which shifts the interest of the research and industrial community towards advance UTB-SOI MOSFET architecture has been identified. The inherent advantage of UTB-SOI MOSFETs have been discussed in comparison to bulk counterparts.

Several design considerations using gate and source/drain engineering have been presented to alleviate these problem existing technology and process limitations. MOSFET scaling continues in to the nanometre regime, the discreteness of charge and matter introduces intrinsic parameter fluctuations that can not be removed by tightening of the process control or by the introduction of new materials. Intrinsic parameter fluctuations are becoming a reality that has to be properly reflected in device and circuit simulations. The Glasgow 3D atomistic simulator has been employed in order to accurately model the 3D nature of the intrinsic parameter fluctuation sources. The "atomistic" simulator includes quantum correction which plays an increasingly important role in nanometer scale devices. Compact models such as Berkeley BSIMSOI are required to to investigate UTB-SOI MOSFET circuit behaviour. However, modern compact models are largely empirical, preventing a direct link to technology, device design parameters and proper physical understanding. In order to assess the impact of different sources of intrinsic parameter fluctuations on circuit behaviour, statistical compact model simulation methodology is required. The SOI based SRAM cells are superior compared to their bulk counterparts in terms of performance, density and power dissipation. It also suffers from intrinsic parameter fluctuations which are most pronounced in minimum geometry MOSFETs commonly used in area-constrained circuits such as SRAM cells. To fully realise the performance benefit of UTB-SOI MOSFET, a detailed study of their susceptibility to IPF is required.

In Chapter 3, simulation results for the intrinsic parameter fluctuations in ensembles of 200 well scaled 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFET have been presented. The transistors correspond to the long term, high performance requirement of the ITRS roadmap. The individual and combined effects of random discrete dopants, body thickness variations and gate line edge roughness were investigated. For all investigated UTB-SOI MOSFET, the intrinsic parameter fluctuations increase with decreasing channel length and are dominated by random discrete dopants in the source/drain region. However, the effects of body thickness variation and line edge roughness could not be disregarded. The specific design parameters of the scaled UTB-SOI MOSFETs devices will determine which of these two sources of fluctuations will dominate in the future. The inclusion of all sources of fluctuations results in a threshold voltage standard deviation of

22 mV in the 10 nm devices and increases to 79 mV for 5 nm devices. The simulation results also demonstrate that fluctuations caused by failing to scale line edge roughness become more critical compared to the fluctuations induced by random discrete dopants. If lithographic technology are not improved, line edge roughness resulted in more than 25 percent increase of treshold voltage standard deviation compared to random discrete dopants. The sources of IPF also results in a substantial increase of fluctuations in off-current and on-current of the simulated devices. The standard deviation of the off-current, considering all sources of fluctuations in combination, is 0.28 orders of magnitude for the 10 nm UTB-SOI MOSFETs, rising to 0.9 orders of magnitude for the 5 nm devices. The combined sources of IPF cause between 11 to 28 percent standard deviation of on-current for the UTB-SOI MOSFETs investigated in this work. The simulation results indicate that the scaling of UTB-SOI MOSFET below 10 nm channel length will be extremely difficult from the intrinsic parameter fluctuations point of views.

In Chapter 4, UTB-SOI MOSFET data characteristics corresponding to the 10 nm, 7.5 nm and 5 nm channel length devices considering different sources of intrinsic parameter fluctuations both individually or in combination, have been converted into sets of compact model libraries. To facilitate the process, a new statistical circuit simulation methodology which takes into account each source of intrinsic fluctuations in UTB-SOI MOSFETs has been developed. The methodology allows seamless integration into the currently available EDA tools. The methodology combines a statistical compact model extraction strategy and a statistical circuit simulation procedure. The statistical compact-model extraction employs the Berkeley BSIMSOI model and a two stage extraction strategy. Although, BSIMSOI does not explicitly consider intrinsic parameter fluctuations, it has a number of empirical parameters introduced to model process variation conditions that can be used to model the fluctuations in atomistic UTB-SOI MOSFET devices. The achieved RMS differences between the atomistic simulation data and the corresponding BSIMSOI result less than two percent for each source of IPF at all channel lengths. This clearly demonstrates that the statistical parameter extraction strategy can adequately describe the effect of IPF over the whole range of simulated devices. In the statistical circuit simulation, devices are randomly selected from the compact model library built by

the statistical extraction strategy. This guarantees that the devices used in circuit simulations correctly represent realistic intrinsic parameter fluctuations effects.

In Chapter 5, the impact of different sources of intrinsic parameter fluctuations on 6T SRAM cells based on the 10 nm, 7.5 nm and 5 nm UTB-SOI MOSFET has been investigated individually or in combination. The SRAM cell have been evaluated in terms of stability, performance and leakage. As expected, random discrete dopants in the source/drain regions dominate the SRAM variability compared to other sources of intrinsic parameter fluctuations. Random discrete dopants results an approximately 10 percent SNM failure rate at 7.5 nm channel length and a 13 percent failure rate at 5 nm channel length. Increasing the cell ratio, r improves the SNM of the simulated SRAM cells by 20 to 40 percent. The increase of the cell ratio also reduces the fluctuations of the SNM. Increasing the cell ratio to three delivers 30 percent reduction of the SNM standard deviation for the 10 nm channel length SRAM cells. However, the improvement is less pronounced at shorter channel lengths. Simulation results demonstrate that 10 nm UTB-SOI MOSFET are more stable than 35 nm bulk MOSFET even though operated at 80 percent of the expected supply voltage. Intrinsic parameter fluctuations caused significant disparity in access performance which may cause violation of the delay requirement for reliable memory cell operation. SRAM simulation considering combination of all sources of intrinsic parameter fluctuations show 6 to 24 percent access difference between fastest and slowest SRAM cells. It is also anticipated that intrinsic parameter fluctuations will increase the overall leakage of cache memory contributing to an increasing static power consumption. The combined effect of large cache structures (>16 MB) and large leakage current results in expected power dissipation nearing 100 mW for high performance 10 nm UTB-SOI MOSFET based SRAM cells and more than a watt for 5 nm based SRAM cells.

6.1 Future Work

There are several future research directions stemming from this work. For the device modelling aspect, the introduction of roughness at the gate electrode/gate dielectric interfaces will be a natural extension of this work. Considering other

sources of fluctuation including structural non-uniformity of high-k gate dielectric and traps or defects in the gate insulator at the interface or in the Si body MOSFET that will cause microscopic variations in device characteristics is also important. Investigation of unintentional strain induced fluctuations is another possible direction of research.

Since intrinsic parameter fluctuations are one of the important factors that impact the design of the next generation circuits, a more physically based compact model is required. The compact model should have the ability to predict the magnitude of intrinsic parameter fluctuations and the quantum mechanical effects governing the operation of nanoscale MOSFETs. Since the variations of the transistor characteristics due to intrinsic parameter fluctuations will be increasing with scaling, it is imperative to understand the nature of their impact on various circuits and to develop design techniques to reduce their impact.

References

[1] Semiconductor Industry Association (SIA), "International Technology Roadmap for Semiconductors," 2005.

[2] H.-S. P. Wong, "Beyond the conventional transistor," in *IBM Journal of Research and Development*, vol. 46, pp. 133–168, 2002.

[3] T. Ghani, K. Mistry, P. Packan, S. Thompson, M. Stettler, S. Tyagi, and M. Bohr, "Scaling challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors," in *Symposium on VLSI Technology*, pp. 174–175, 2000.

[4] T. Mizuno, M. Iwase, H. Niiyama, T. Shibata, K. Fujisaki, T. Nakasugi, A. Toriumi, and Y. Ushiku, "Performance fluctuations of 0.10 μm MOSFETs-limitation of 0.1 μm ULSIs," in *Symposium on VLSI Technology*, pp. 13–14, 1994.

[5] T. Mizuno, J. Okumtura, and A. Toriumi, "Experimental study of threshold voltage fluctuation due to statistical variation of channel dopant number in MOSFET's," *IEEE Transactions on Electron Devices*, vol. 41, no. 11, pp. 2216–2221, 1994.

[6] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFET's: A 3D atomistic simulation study," *IEEE Transactions on Electron Devices*, vol. 45, no. 12, pp. 2205–2513, 1998.

[7] K. Nishinohara, N. Shigyo, and T. Wada, "Effects of microscopic

fluctuations in dopant distributions on MOSFET threshold voltage," *IEEE Transactions on Electron Devices*, vol. 39, no. 3, pp. 634–639, 1992.

[8] H.-S. Wong and Y. Taur, "Three-dimensional "atomistic" simulation of discrete distribution effects in sub-0.1μm MOSFET's," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 705–708, 1993.

[9] T. Yamaguchi, H. Namatsu, M. Nagase, K. Yamazaki, and K. Kurihara, "Nanometer-scale linewidth fluctuations caused by polymer aggregates in resist films," *Applied Physics Letters*, vol. 71, no. 16, pp. 2388–2390, 1997.

[10] S. Kaya, A. R. Brown, A. Asenov, D. Magot, and T. Linton, "Analysis of statistical fluctuations due to line edge roughness in sub 0.1μm MOSFET's," in *Simulation of Semiconductor Processes and Devices (SISPAD)*, 2001.

[11] J. Croon, G. Storms, S. Winkelmeier, I. Pollentier, M. Ercken, S. Decoutere, W. Sansen, and H. Maes, "Line edge roughness: characterization, modeling and impact on device behavior," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 307–310, 2002.

[12] A. Asenov, S. Kaya, and J. H. Davies, "Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations," *IEEE Transactions on Electron Devices*, vol. 49, no. 1, pp. 112–119, 2002.

[13] A. Bhavnagarwala, S. Kosonocky, C. Radens, K. Stawiasz, R. Mann, Q. Ye, and K. Chin, "Fluctuation limits and scaling opportunities for CMOS SRAM cells," in *International Electron Devices Meeting (IEDM) Technical Digest*, 2005.

[14] R. Venkatraman, R. Castagnetti, and S. Ramesh, "The statistics of device variations and its impact on SRAM bitcell performance, leakage and stability," in *International Symposium on Quality Electronic Design (ISQED)*, 2006.

[15] B. Doris, M. Ieong, T. Kanarsky, Y. Zhang, and R. A. Roy, "Extreme scaling with ultra-thin Si channel MOSFETs," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 267–270, IEEE, 2002.

[16] L. Chang, Y.-K. Choi, D. Ha, P. Ranade, S. Xiong, J. Bokor, *et al.*, "Extremely scaled silicon nano-CMOS devices," in *Proceedings of the IEEE*, vol. 91, pp. 1860–1873, 2003.

[17] S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Statistical design and optimization of SRAM cell for yield enhancement," in *International Conference on Computer Aided Design (ICCAD)*, 2004.

[18] F. J. Kurdahi, A. M. Eltawil, Y. H. Park, R. N. Kanj, and S. R. Nassif, "System-level SRAM yield enhancement," in *International Symposium on Quality Electronic Design (ISQED)*, 2006.

[19] B. Cheng, S. Roy, and A. Asenov, "The impact of random doping effects on CMOS SRAM cell," in *European Solid-State Circuits Conference (ESSCIRC)*, pp. 219–222, 2004.

[20] J. B. Kuang, S. Ratanphanyarat, *et al.*, "SRAM bitline circuits on PD SOI: Advantages and concerns," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 6, pp. 837–844, 1997.

[21] B. Johnson, T. Quarles, A. Newton, *et al.*, *SPICE3 Version 3f User's Manual.* University of California, Berkeley, 1992.

[22] *BSIMSOI 3.1 MOSFET Model User Manual.* University of California, Berkeley, 2003.

[23] F. Schellenberg, "Lithography: The integration of TCAD and EDA." `http://www.mentor.com/products/ic_nanometer_design/news/lithography_tcad_eda.cfm`, 2004.

[24] D. Frank, R. Dennard, E. Nowak, P. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," in *Proceedings of the IEEE*, vol. 89, pp. 259–288, 2001.

[25] Y. Taur, D. Buchanan, W. Chen, D. Frank, K. Ismail, *et al.*, "CMOS scaling into the nanometer regime," in *Proceedings of the IEEE*, vol. 85, pp. 486–504, 1997.

[26] H.-S. Wong, D. Frank, P. Solomon, C. Wann, and J. Welser, "Nanoscale CMOS," in *Proceedings of the IEEE*, vol. 87, pp. 537–570, 1999.

[27] A. Asenov, J. R. Watling, A. R. Brown, and D. K. Ferry, "The use of quantum potentials for confinement and tunnelling in semiconductor devices," *Journal of Computational Electronics*, vol. 1, pp. 503–513, 2003.

[28] B. Yu, H. Wang, A. Joshi, Q. Xiang, E. Ibok, and M.-R. Lin, "15 nm gate length planar CMOS transistor," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 11.7.1–11.7.3, 2001.

[29] B. Doyle, R. Arghavani, D. Barlage, S. Datta, M. Doczy, J. Kavalieros, *et al.*, "Transistor elements for 30nm physical gate length and beyond," *Intel Technology Journal*, vol. 3, no. 2, 2002.

[30] S. Thompson, N. Anand, M. Armstrong, C. Auth, B. Arcot, and M. Alavi, "A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1 μm 2 SRAM cell," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 61– 64, 2002.

[31] S.-H. Lo, D. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's," *IEEE Electron Device Letters*, vol. 18, no. 5, pp. 209–211, 1997.

[32] T. Ghani, S. Ahmed, P. Aminzadeh, J. Bielefeld, P. Charvat, C. Chu, *et al.*, "100 nm gate length high performance/low power CMOS transistor structure," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 415–418, 1999.

[33] C. F. D. Taur, Y. Wann, "25 nm CMOS design considerations," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 789–792, 1998.

[34] H. Kawaura, T. Sakamoto, and T. Baba, "Observation of source-to-drain direct tunneling current in 8 nm gate electrically variable shallow junction metal–oxide–semiconductor field-effect transistors," *Applied Physics Letters*, vol. 76, no. 25, pp. 3810–3812, 2000.

[35] D. J. Frank, "Power-constrained CMOS scaling limits," *IBM Journal of Research and Development*, vol. 46, no. 2/3, p. 235, 2002.

[36] M. Pelella, W. Maszara, S. Sundararajan, *et al.*, "Advantages and challenges of high performance CMOS on SOI," in *IEEE International SOI Conference*, pp. 1–4, 2001.

[37] D. Suh and J. Fossum, "Dynamic floating-body instabilities in partially depleted SOI CMOS circuits," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 661–664, 1994.

[38] J. Gautier and J.-C. Sun, "On the transient operation of partially depleted SOI NMOSFET's," *IEEE Electron Device Letters*, vol. 16, no. 11, pp. 497–499, 1995.

[39] F. Assaderaghi, G. Shahidi, M. Hargrove, K. Hathorn, H. Hovel, and S. Kulkarni, "History dependence of non-fully depleted (NFD) digital SOI circuits," in *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 122–123, 1996.

[40] F. Assaderaghi and G. Shahidi, "SOI at IBM: current status of technology, modeling, design, and the outlook for the 0.1 μm generation," in *IEEE International SOI Conference*, pp. 6–9, 2000.

[41] C. Chuang, P. Lu, and C. Anderson, "SOI for digital CMOS VLSI: Design considerations and advances," in *Proceedings of the IEEE*, vol. 86, pp. 689–720, 1998.

[42] R. Luyken, M. Stadele, W. Rosner, J. D. L. Schulz, T.; Hartwich, and L. Risch, "Perspectives of fully-depleted SOI transistors down to 20nm gate length," in *IEEE International SOI Conference*, pp. 137– 139, 2002.

[43] Y. Omura, S. Nakashima, and K. Izumi, "0.1μm-gate ultrathin-film CMOS devices using SIMOX substrate with 80-nm-thick buried oxide layer," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 675–678, 1991.

[44] J. T.-J. K. W. H.-S. B. F. Skotnicki, T. Hutchby, "The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance," *Circuits and Devices Magazine, IEEE*, vol. 21, no. 1, pp. 16– 26, 2005.

[45] T. Ernst, S. Cristoloveanu, G. Ghibaudo, T. Ouisse, S. Horiguchi, and Y. Ono, "Ultimately thin double-gate SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 830– 838, 2003.

[46] T. Ichimori and N. Hirashita, "Fully-depleted SOI CMOSFETs with the fully-silicided source/drain structure," *IEEE Transactions on Electron Devices*, vol. 49, no. 12, pp. 2296–2300, 2002.

[47] D. E. Ioannou, "Scaling limits and reliability of SOI CMOS technology," *Journal of Physics*, vol. 10, no. 1-6, 2005.

[48] N. Mohapatra, M. Desai, S. Narendra, and V. Rao, "The effect of high-K gate dielectrics on deep submicrometer CMOS device and circuit performance," *IEEE Transactions on Electron Devices*, vol. 49, no. 5, pp. 826–831, 2002.

[49] G. Bersuker, J. H. Sim, C. D. Young, R. Choi, B. H. Lee, P. Lysaght, *et al.*, "Effects of structural properties of Hf-based gate stack on transistor performance," in *Proceedings of Material Research Society*, vol. 811, pp. 31–35, 2004.

[50] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, *et al.*, "Fermi level pinning at the polySi/metal oxide interface," in *Symposium on VLSI Technology*, p. 9, 2003.

[51] R. Zhang and K. Roy, "Low-power high-performance double-gate fully depleted SOI circuit design," *IEEE Transactions on Electron Devices*, vol. 49, no. 5, pp. 852–862, 2002.

[52] S. Yamakawa, K. Sugihara, T. Furukawa, Y. Nishioka, T. Nakahata, and Y. Abe, "Drivability improvement on deep-submicron MOSFETs by elevation of source/drain regions," *IEEE Electron Device Letters*, vol. 20, no. 7, 1999.

[53] J. Kedzierski, P. Xuan, E. Anderson, J. Bokor, T.-J. King, and C. Hu, "Complementary silicide source/drain thin-body MOSFETs for the 20 nm gate length regime," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 57–60, 2000.

[54] Z. Krivokapic, W. Maszara, and M.-R. Lin, "Manufacturability of 20-nm ultrathin body fully depleted SOI devices with FUSI metal gates," *IEEE Transactions on Semiconductor Manufacturing*, vol. 18, no. 1, pp. 5–12, 2005.

[55] A. Asenov, A. R. Brown, J. H. Davies, S. Kaya, and G. Slavcheva, "Simulation of intrinsic parameter fluctuations in decananometer and nanometer-scale MOSFETs," *IEEE Transactions on Electron Devices*, vol. 50, no. 9, pp. 1837–1852, 2003.

[56] A. Asenov, G. Slavcheva, A. Brown, *et al.*, "Increase in the random dopant induced threshold fluctuations and lowering in sub-100 nm MOSFETs due to quantum effects: a 3-D density-gradient simulation study," *IEEE Electron Device Letters*, vol. 48, no. 4, pp. 722 – 729, 2001.

[57] D. Frank, Y. Taur, M. Ieong, and H.-S. Wong, "Monte Carlo modeling of threshold variation due to dopant fluctuations," in *VLSI Technology Digest of Technical Papers*, pp. 169–170, 1999.

[58] M. Sherony, L. Su, J. Chung, and D. Antoniadis, "Reduction of threshold voltage sensitivity in SOI MOSFET's," *IEEE Electron Device Letters*, vol. 16, no. 3, 1995.

[59] S. Xiong and J. Bokor, "Sensitivity of double-gate and FinFET devices to process variations," *IEEE Transactions on Electron Devices*, vol. 50, no. 11, pp. 2255– 2261, 2003.

[60] V. Trivedi and J. Fossum, "Scaling fully depleted SOI CMOS," *IEEE Transactions on Electron Devices*, vol. 50, no. 10, pp. 2095–2103, 2003.

[61] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. ichi Takagi, "Experimental study on carrier transport mechanism in ultrathin-body SOI n- and p-MOSFETs with SOI thickness less than 5nm," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 47–50, 2002.

[62] D. Esseni, A. Abramo, L. Selmi, and E. Sangiorgi, "Physically based modeling of low field electron mobility in ultrathin single- and double-gate SOI n-MOSFETs," *IEEE Transactions on Electron Devices*, vol. 50, no. 12, pp. 2445 – 2455, 2003.

[63] A. Asenov, A. R. Brown, J. H. Davies, and S. Saini, "Hierarchical approach to atomistic 3-D MOSFET simulation," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, vol. 18, no. 11, pp. 1558–1565, 1999.

[64] A. R. Brown, F. Adamu-Lema, and A. Asenov, "Intrinsic parameter fluctuations in nanometre scale thin-body SOI devices introduced by interface roughness," *Superlattices and Microstructures*, vol. 34, pp. 283–291, 2003.

[65] R. Williams and J. Watts, "Compact models for IBM's Silicon-on-Insulator technologies," *MicroNews*, vol. 7, no. 1, 2001.

[66] J. Fossum, P. Yeh, and J. Choi, "Floating-body problems and benefits in fully depleted SOI CMOS VLSI circuits," in *International Electron Devices Meeting (IEDM) Technical Digest*, 1991.

[67] L. Su, D. A. Antoniadis, N. D. Arora, B. S. Doyle, and D. B. Krakauer, "Spice model and parameters for fully-depleted SOI MOSFET's including self-heating," *IEEE Electron Device Letters*, vol. 15, no. 10, 1994.

[68] J. Kuo, "SPICE compact modeling of PD-SOI CMOS devices," in *IEEE HKEDM*, pp. 1–4, 2000.

[69] S. Fung, L. Wagner, M. Sherony, J. M.-M. Zamdmer, N.; Sleight, E. Leobandung, S. Lo, T. Chen, and F. Assaderaghi, "A partially-depleted SOI compact model - formulation and parameter extraction," in *Symposium on VLSI Technology*, pp. 206–207, 2000.

[70] K. Goto, P. Su, Y. Tagawa, T. Sugii, and C. Hu, "80nm SOI CMOS parameter extraction for BSIMPD," in *IEEE International SOI Conference*, pp. 55–56, 2001.

[71] *BSIM3v3.2.2 MOSFET Model User Manual.* University of California, Berkeley, 1999.

[72] K. A. Bowman, X. Tang, J. C. Eble, and J. D. Meindl, "Impact of extrinsic and intrinsic parameter fluctuations on CMOS circuit performance," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 8, pp. 1186–1193, 2000.

[73] J. Chen, C. Hu, Z. Liu, and P. Ko, "Realistic worst-case spice file extraction using BSIM3," in *Custom Integrated Circuits Conference*, pp. 375–378, 1995.

[74] S. Nassif, A. Strojwas, and S. Director, "A methodology for worst-case analysis of integrated circuits," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, vol. 5, no. 1, pp. 104– 113, 1986.

[75] K. Takeuchi and M. Hane, "A highly efficient statistical compact model parameter extraction scheme," in *Simulation of Semiconductor Processes and Devices (SISPAD)*, pp. 135–138, 2005.

[76] J. Power, A. Mathewson, and W. Lane, "Mosfet statistical parameter extraction using multivariate statistics," in *International Conference on Microelectronic Test Structures (ICMTS)*, pp. 209–214, 1990.

[77] J. Chen, C. Hu, C.-P. Wan, P. Bendix, and A. Kapoor, "E-T based statistical modeling and compact statistical circuit simulation methodologies," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 635–638, 1996.

[78] M. Miyama, S. Kamohara, M. Hiraki, K. Onozawa, and H. Kunitomo, "Pre-silicon parameter generation methodology using BSIM3 for circuit performance-oriented device optimization," *IEEE Transactions on Semiconductor Manufacturing*, vol. 14, no. 2, pp. 134–142, 2001.

[79] A. J. Bhavnagarwala, X. Tang, and J. D. Meindl, "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 4, pp. 658–665, 2001.

[80] V. Palankovski, N. Belova, T. Grasser, H. Puchner, S. Aronowitz, and S. Selberherr, "A methodology for deep sub-0.25 μm CMOS technology prediction," *IEEE Transactions on Electron Devices*, vol. 48, no. 10, pp. 2331–2336, 2001.

[81] S. Naffziger, G. Colon-Bonet, T. Fischer, R. Riedlinger, T. Sullivan, and T. Grutkowski, "The implementation of the Itanium 2 microprocessor," *IEEE Journal of Solid-State Circuit*, vol. 37, no. 11, pp. 1448–1460, 2002.

[82] K. Kumagai, T. Yamada, *et al.*, "A new SRAM cell design using 0.35μm CMOS/SIMOX technology," in *IEEE International SOI Conference*, pp. 174–175, 1997.

[83] S. B. Park, Y. W. Kim, Y. G. Ko, *et al.*, "A 0.25-μm, 600-MHz, 1.5-v, fully depleted SOI CMOS 64-bit microprocessor," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 11, pp. 1436–1445, 1999.

[84] A. Aipperspach, D. Allen, D. Cox, N. Phan, and S. Storino, "A 0.2-μm, 1.8-v, SOI, 550-MHZ, 64-b PowerPC microprocessor with copper interconnects," *IEEE Solid-State Circuits*, vol. 34, no. 11, pp. 1430–1435, 1999.

[85] L. Chang, D. Fried, J. Hergenrother, J. Sleight, R. Dennard, R. Montoye, *et al.*, "Stable sram cell design for the 32 nm node and beyond," in *Symposium on VLSI Technology*, pp. 128–129, 2005.

[86] K. Koh, B. J. Hwang, *et al.*, "Highly manufacturable 100 nm 6T lower power SRAM with single Poly-Si gate technology," in *International Symposium on VLSI Technology, Systems, and Applications*, pp. 64–67, 2003.

[87] Z. Guo, S. Balasubramanian, R. Zlatanovici, T.-J. King, and B. Nikoli, "FinFET-based SRAM design," in *International Symposium on Low Power Electronics and Design*, pp. 2–7, 2005.

[88] B. Doris, Y. Kim, B. Linder, M. Steen, *et al.*, "High performance FDSOI CMOS technology with metal gate and high-k," in *Symposium on VLSI Technology*, pp. 214– 215, 2005.

[89] F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, and C.-C. Huang, "5nm-gate nanowire FinFET," in *Symposium on VLSI Technology*, pp. 196– 197, 2004.

[90] D. Burnett, K. Erington, C. Subramanian, and K. Baker, "Implications of fundamental threshold voltage variations for high-density SRAM and logic circuits," in *Symposium on VLSI Technology*, pp. 15–16, 1994.

[91] T. Ezaki, T. Ikezawa, and M. Hane, "Investigation of realistic dopant fluctuation induced device characteristics variation for sub-100 nm CMOS

by using atomistic 3D process/device simulator," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 311– 314, 2002.

[92] A. Asenov, M. Jaraiz, S. Roy, G. Roy, F. Adamu-Lema, A. Brown, V. Moroz, and R. Gafiteanu, "Integrated atomistic process and device simulation of decananometre MOSFETs," in *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, pp. 87– 90, 2002.

[93] S. Jallepalli, J. Bude, W. K. Shih, M. R. Pinto, C. M. Maziar, and A. F. T. Jr., "Electron and hole quantization and their impact on deep submicron silicon p- and n-MOSFET characteristics," *IEEE Transactions on Electron Devices*, vol. 44, no. 2, pp. 297–303, 1997.

[94] C. S. Rafferty, B. Biegel, Z. Yu, M. G. Ancona, J. Bude, and R. W. Dutton, "Multi-dimensional quantum effects simulation using a density-gradient model and script-level programming technique," in *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, pp. 137–140, 1998.

[95] H.-W. Kim, J.-Y. Lee, *et al.*, "Experimental investigation of the impact of LWR on sub-100-nm device performance," *IEEE Transactions on Electron Devices*, vol. 51, no. 12, pp. 1984–1988, 2004.

[96] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuations in decananometre MOSFETs introduced by Gate Line Edge Roughness," *IEEE Transactions on Electron Devices*, vol. 50, pp. 1254–1260, 2003.

[97] A. R. Brown, A. Asenov, and J. R. Watling, "Intrinsic fluctuations in sub 10 nm double-gate MOSFETs introduced by discreteness of charge and matter," *IEEE Transactions on Nanotechnology*, vol. 1, pp. 195–200, 2002.

[98] F. Adamu-Lema, *Scaling and Intrinsic Parameter Fluctuation of Nano-CMOS Devices*. PhD thesis, Electronics and Electrical Eng. Dept., University of Glasgow, 2005.

[99] H. Iwai, T. Ohguro, and S. ichiro Ohmi, "NiSi salicide technology for scaled CMOS," *Microelectronic Engineering*, vol. 60, no. 1, pp. 157–169, 2002.

[100] G. Sery, S. Borkar, and V. De, "Life is CMOS: why chase the life after?," in *Design Automation Conference*, pp. 78– 83, 2002.

[101] E. Seevinck, F. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748–754, 1987.

[102] P. Fieler and J. Loverro, N., "Defects tail off with six-sigma manufacturing," *IEEE Circuits and Devices Magazine*, vol. 7, no. 5, pp. 18–20, 48, 1991.

[103] H. S. Momose, S. Nakamura, T. Ohguro, T. Yoshitomi, E. Morifuji, T. Morimoto, Y. Katsumata, and H. Iwai, "Study of the manufacturing feasibility of 1.5-nm direct-tunneling gate oxide MOSFET's: Uniformity, reliability, and dopant penetration of the gate oxide," *IEEE Transactions on Electron Devices*, vol. 45, no. 3, pp. 691–700, 1998.

[104] D. Frank, Y. Taur, and H.-S. Wong, "Generalized scale length for two-dimensional effects in MOSFETs," *IEEE Electron Device Letters*, vol. 19, no. 10, pp. 385–387, 1998.

[105] S. Natarajan and A. Marshall, "SOI SRAM design advances and considerations," in *International Conference on Electronics, Circuits and Systems*, vol. 2, pp. 835– 838, 2002.

[106] H. Nakayama, P. Su, C. Hu, M. Nakamura, H. Komatsu, K. Takeshita, and Y. Komatsu, "Methodology of self-heating free parameter extraction and circuit simulation for SOI CMOS," in *IEEE Custom Integrated Circuits Conference*, pp. 381–384, 2001.

[107] C. Galup-Montoro, M. Schneider, H. Klimach, and A. Arnaud, "A compact model of MOSFET mismatch for circuit design," *IEEE Journal of Solid-State Circuit*, vol. 40, no. 8, pp. 1649–1657, 2005.

[108] Synopsys, *Aurora: Parameter Extraction and Optimization Program User Manual*, 2003.

[109] P. Bendix, "Subtleties of spice mosfet parameter extraction," in *International Conference on Microelectronic Test Structures (ICMTS)*, pp. 65–68, 1989.

[110] F. Corsi, C. Marzocca, and G. Portacci, "New experimental technique for fast and accurate MOSFET threshold extraction," *Electronics Letters*, vol. 29, no. 15, pp. 1358–1360, 1993.

[111] M. Miyama, S. Kamohara, K. Nakura, M. Shinozaki, T. Akioka, K. Okuyama, and K. Kubota, "Statistical BSIM3 model parameter extraction and fast/slow model parameter determination for high speed sram parametric yield estimation," in *International Workshop on Statistical Metrology*, pp. 42–45, 2000.

[112] P. Su, *An International Standard Model for SOI Circuit Design*. PhD thesis, Electrical Engineering and Computer Science, University of California, Berkeley, 2002.

[113] M.-S. Liang, J. Y. Choi, P.-K. Ko, and C. Hu, "Inversion-layer capacitance and mobility of very thin gate-oxide MOSFET's," *IEEE Transactions on Electron Devices*, vol. 33, no. 3, pp. 409–413, 1986.

[114] D. B. M. Klaassen, "Compact modelling of submicron CMOS," in *Proceedings of the 22nd European Solid-State Circuits Conference (ESSCIRC)*, pp. 40–46, 1996.

[115] R. Heald and P. Wang, "Variability in sub-100nm SRAM designs," in *International Conference on Computer Aided Design (ICCAD)*, pp. 347–352, 2004.

[116] S. Inaba, K. Okano, S. Matsuda, M. Fujiwara, A. Hokazono, K. Adachi, *et al.*, "High performance 35nm gate length CMOS with NO oxynitride gate dielectric and Nisalicide," *IEEE Transactions on Electron Devices*, vol. 49, no. 12, pp. 2263–2270, 2002.

[117] D. Burger, "System-level implications of processor-memory integration," in *24th International Symposium on Computer Architecture*, 1997.

[118] R. W. Mann, W. W. Abadeer, M. J. Breitwisch, O. Bula, J. S. Brown, B. C. Colwill, *et al.*, "Ultralow-power SRAM technology," *IBM Journal of Research and Development*, vol. 47, no. 5/6, pp. 553–566, 2003.

[119] K. J. O'Connor, "A source sensing technique applied to SRAM cells," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 4, pp. 500–511, 1995.

[120] A. M.-J. Bhavnagarwala, A.J.; Kapoor, "Dynamic-threshold CMOS SRAM cells for fast, portable applications," in *13th Annual IEEE International ASIC/SOC Conference*, pp. 359–363, 2000.

[121] P. Stolk, H. Tuinhout, R. Duffy, E. Augendre, L. P. Bellefroid, M. J. B. Bolt, *et al.*, "CMOS device optimization for mixed-signal technologies," in *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 215–218, 2001.

[122] A. K. Sharma, *Semiconductor Memories: Technology, Testing and Reliability*. IEEE Press, 1997.

[123] C. H. Kim and K. Roy, "Dynamic Vt SRAM: a leakage tolerant cache memory for low voltage microprocessors," in *International Symposium on Low Power Electronics and Design*, 2002.