Monolithic Microwave/Millimetrewave Integrated Circuit Resonant Tunnelling Diode Sources with around a Milliwatt Output Power

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This thesis is dedicated to my loving parents JianYang Wang and ChangJiang Wang.

献给我的父亲（王建阳) & 母亲（王长江）

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Abstract

Resonant tunnelling diode (RTD) oscillators are considered to be one of the most promising solid-state terahertz sources which can operate at room temperature. The main limitation of RTD oscillators up to now is their low output power. For the published terahertz (THz) RTD oscillators, the output power is in the range of micro-Watts (μW). This thesis describes systematic work on RTD device modelling, and on the design, fabrication and measurement of high power monolithic microwave integrated circuit (MMIC) RTD oscillators.

The RTD device consists of a narrow bandgap layer (quantum well) sandwiched between two thin wide bandgap layers (barriers). When the device is biased, electrons with kinetic energy lower than the barriers may tunnel through the double barrier-quantum well (DBQW) structure, and the device exhibits a negative differential resistance (NDR) in this case. To investigate this phenomenon, a new numerical model based on quantum mechanics was developed. The model involves self-consistent solving of the Schrödinger equation until the quasi-eigen energy state converges. This model is expected to serve to optimize the RTD device structure for millimetre-wave and terahertz applications.

Besides RTD device modelling, the fabrication process for single devices and for MMIC RTD oscillator circuits was developed and optimized on this project. Optical lithography, wet/dry etching and metallization were the main fabrication techniques utilized. For device sizes of a few square microns, the fabrication process required the development of new steps, i.e, via opening through polyimide. The fabrication process was optimized and high yield was obtained.

On this project, one of the challenges was to realize RTD oscillators in the form of MMICs, aiming at about 100 GHz with milli-Watts output power, in accordance with a recently proposed power combining circuit topology. To accomplish such an oscillator, proper design of passive components was essential. On this project, these components included 50Ω coplanar waveguides (CPW), shorted CPW stubs, metal-insulator-metal (MIM) capacitors and thin film resistors. The design procedure for these components is described, and their performance characterized by DC or scattering parameter measurements as appropriate. Two types of MMIC RTD oscillator layouts were designed, fabricated and characterized. Details are described in this thesis. Measurement results showed that for the fabricated 75 GHz oscillator, the output power obtained was $-0.2\ dBm$ (0.96 mW), and for the 86 GHz oscillator, the measured output power was $-4.6\ dBm$ (0.35 mW), both of which, to the author's knowledge, were the highest power for published indium phosphide (InP)-based RTD oscillators operating in the W-band frequency range.

Publications

[1] **J. Wang** and E. Wasige, "Self-consistent Analysis of the IV characteristics of Resonant Tunnelling Diodes," *Terahertz Science and Technology*, Vol.5, No.4, pp. 153-162, Dec. 2012.

[2] **J. Wang**, L. Wang, C. Li, B. Romeira and E. Wasige, "28 GHz MMIC Resonant Tunneling Diode Oscillator of around 1mW Output Power," *Electronics letters*, vol. 49, No.13, pp. 816-818, Jun.2013.

[3] **J. Wang**, L. Wang, C. Li, D. Cumming and E. Wasige, "Novel Resonant Tunnelling Diode Oscillator with High Output Power," *UK Semiconductor conference 2013*, Sheffield Hallam University, Jul. 2013.

[4] **J. Wang** and E. Wasige, "IV characteristics of Resonant Tunnelling Diodes investigated by a numerical model based on semiconductor physics," *HETECH (Heterostructure Technology) 2013*, University of Glasgow, Sep.2013.

[5] **J. Wang**, L. Wang, C. Li, K. Alharbi, A. Khalid and E. Wasige, "W-band InP-based Resonant Tunnelling Diode Oscillator with Milliwatt Output Power," *The 26th International Conference on Indium Phosphide and Related Materials*, Montpellier, France, May, 2014.

[6] L. Chong, J. Grant, **J. Wang** and D. Cumming, "A Nipkow disk integrated with Fresnel lenses for terahertz single pixel imaging," *Optics Express*, vol 21, No. 21, pp. 24452-24459, Oct.2013.

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Chapter 1

THz Technology: Sources

1.1 Introduction

Terahertz (THz) is generally defined as the electromagnetic radiation with frequencies located in the region between 300 GHz–3 THz with corresponding wavelength $\lambda = 1\ mm \sim 100\ \mu m$ [1] [2]. In some references [3] [4], it is also referred to as the frequency between 100 GHz–10 THz. This frequency range lies between traditional microwave electronics and infrared photonics, as shown in Figure 1.1.

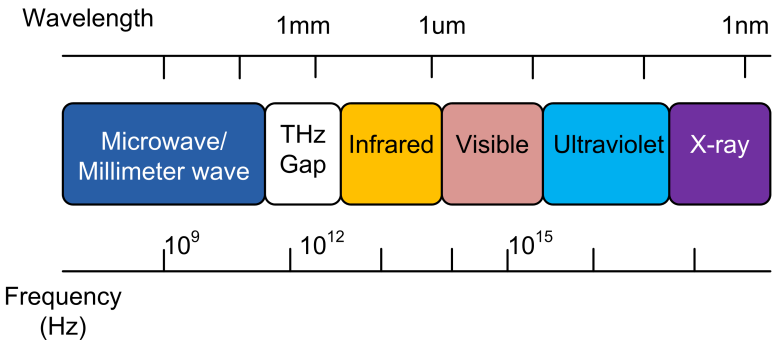

Figure 1.1: *Frequency and wavelength spectra of electromagnetic waves.*

Terahertz radiation can penetrate through many materials such as clothing, wood, plastics, etc. as well as organic materials of living organisms without any damage associated with ionizing radiation (such as with X-ray), so terahertz techniques can support promising applications in security systems to reveal undercover weapons, scan sealed packages non-destructively, and also in medical imaging systems. Terahertz techniques can also be utilized in high-resolution radar imaging systems and compact wide-bandwidth wireless-communication systems [2] [5]. However, producing reliable and powerful coherent terahertz signals is a technical challenge.

At the low frequency end, the high electron mobility transistors (HEMTs) and heterojuction bipolar transistors (HBTs) are the electronic devices with current gain cut off frequency (f_T) approaching 1 THz [6–9]. However the cut-off frequency of the transistors are mostly limited by the carriers drift velocity. The transistor cut-off frequency f_T can be approximately estimated by $f_T = 1/(2\pi\tau)$, where τ represents the carriers transit time. For high electron mobility transistor (HEMT), τ equals the gate length L_g divided by the drift velocity v. Under high electric field, v is close to the saturation velocity v_s, of which typical values for indium gallium arsenide (InGaAs) $v_s = 4.3 \times 10^7\ cm/s$ [8], gallium arsenide (GaAs) $v_s = 2 \times 10^7\ cm/s$, silicon (Si) $v_s = 10^7\ cm/s$ and graphene $v_s = 4 \times 10^7\ cm/s$ [9]. To achieve high frequency, for HEMTs, the gate length L_g must be scaled down. The highest $f_T = 610\ GHz$ (with $L_g = 15\ nm$) was reported [8] for HEMTs, while for HBTs, $f_T = 670\ GHz$ with thin base layer (20 nm) and collector layer (60 nm) was demonstrated [10]. Stringent lighography requirements are therefore required (thin gate length for HEMTs, and thin contacts - base collector parasitic capacitance - for HBTs), which limits the applicability of transistors in

THz electronics. In addition, since electronic circuits are typically realised at a quarter or less of the transistor cut-off frequency, the fastest transistors are only useful up to about 200 GHz.

At the high frequency end, the most commonly and commercially available terahertz sources are gas lasers. These sources are able to provide relatively high power in hundreds milli-Watts range, however these sources require large cavities, kilowatt power supply and cryogenic cooling, which impose prohibitive cost and size constraints [1] [4] [11].

The lack of reliable, compact, high power terahertz sources, which can operate at room temperature, has resulted in one of the least tapped regions of the electromagnetic spectrum between the traditional microwave and infrared region. This region is also sometimes termed the "THz gap". In recent years, this gap has been narrowed by high speed microwave electronics devices and the development of long wavelength photonic devices.

1.2 THz Sources

As mentioned above, the lack of compact, high power and room-temperature operating THz sources greatly limits the development of modern THz systems, there has been significant research contributing to THz source development. There are many candidates that show great potential for THz applications. In general these THz generation techniques fall into four categories [12].

(i) Lasers: A laser is a device based on the stimulated emission of electromagnetic radiation. The process involves an electron that transits from a high energy state to a low energy state with associated photon emission with the same

phase and frequency [13] . The simplest laser system as shown in Figure 1.2 includes a gain medium where stimulated emission occurs and a set of mirrors to reflect the beam passing though the gain medium and being amplified [14]. The frequencies of most lasers are located at the high end of the THz range with

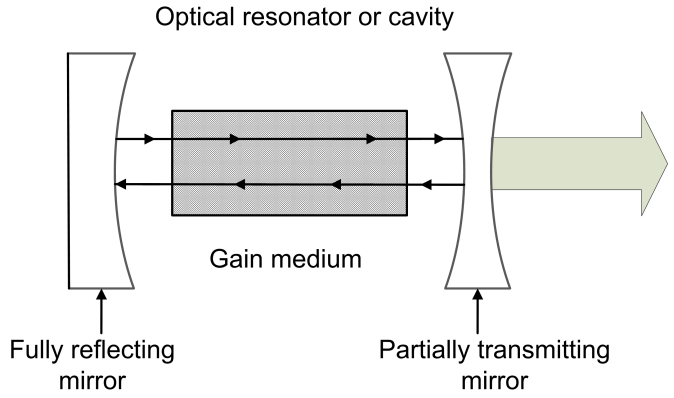

Figure 1.2: *Simplified schematic of typical laser [14].*

several hundreds of nanometers wavelength. At the low end of THz range, there are several laser devices developed to bridge the THz gap, such as far-infrared (FIR) gas laser [15], quantum cascade lasers (QCL) [16], etc. The schematic representation of FIR laser is shown in Figure 1.3. One of the most widely used FIR laser consists of an external carbon dioxide (CO_2) laser to stimulate methanol (CH_3OH) gas molecules which is filled in the FIR gas tube to emit FIR radiation [17] [18]. As FIR gas laser requires cryogenic cooling, the whole system is bulky and costly, however it is a powerful THz source which can provide 100 mW at 118 μm wavelength [11].

QCL is an alternative to an FIR laser, and was first demonstrated in 1994 [16]. Different from the FIR gas laser, QCL is a solid-state semiconductor laser, which consists of multiple quantum well heterostructures. The published lowest frequency of QCL is 2.1 THz with 1.2 mW power in continuous-wave (CW) mode

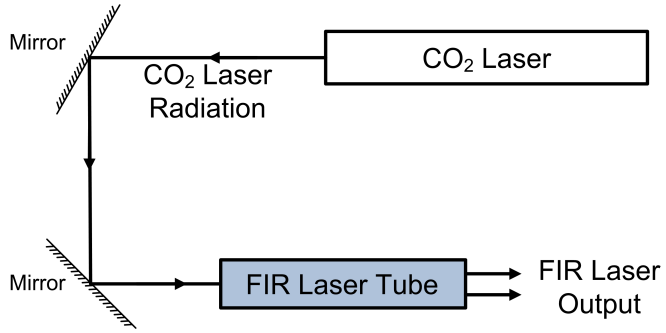

Figure 1.3: *Schematic diagram of a far-infrared (FIR) CO_2 laser.*

operating at 17K temperature [19]. The performance of QCL degrades sharply with rising temperature. No lasing was observed in CW mode of this QCL for temperature over 40K [19]. The requirement of bulk cryogenic cooling system limits its practical applications which require portability.

(ii) Free electron sources: Free electron sources such as gyrotron, backward-wave oscillators (BWOs), etc. generate THz radiation by spiralling electrical charges in strong magnetic fields [1]. The gyrotron is a cyclotron resonance maser (CRM) in which an intense flow of electrons (injected by a magnetron injection gun) gyrates at high speed in a strong magnetic field (introduced by symmetrical superconducting magnet) and emits electromagnetic wave as illustrated in Figure 1.4. The gyrotron is generally designed to obtain high power, killowatts (kW),

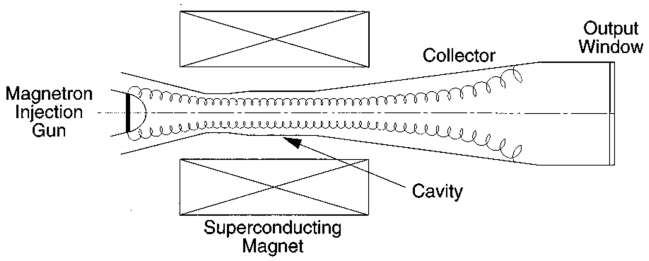

Figure 1.4: *Schematic diagram of a gyrotron [20].*

with frequency ranging around several hundred GHz [20] [21].

The backward-wave oscillator (BWO) is an another free electron vacuum tube device as shown in Figure 1.5. The electrons are emitted from a heated cathode and collimated by a strong magnetic field. The metallic grating structure induces periodic perturbation of electrons and excites surface wave on the periodic structure. If the electron beam velocity matches the phase velocity of the surface wave, the kinetic energy of the electrons is transferred to the electromagnetic wave [22]. The term "backward-wave" refers to the opposite propagation direction between the group velocity and phase velocity of the surface wave. The typical size of

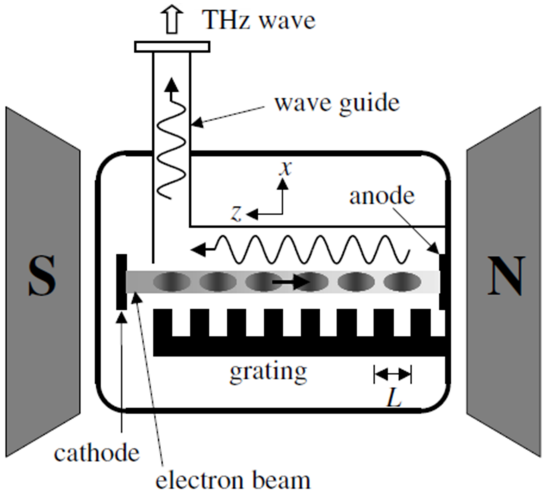

Figure 1.5: *Schematic diagram of a backward-wave oscillator (BWO) [22].*

BWO is about $30cm \times 30cm \times 30cm$. The bias voltage ranges from 1 kV to 10 kV while the magnetic field is about 1 T. BWOs cover the frequencies ranging from 0.03-1 THz. The output power decreases sharply with increasing frequency. At about 1 THz, the obtained power is about 1 mW [22]. The free electron systems suffer from bulk physical size, metallic wall losses and the requirement for high magnetic and electric fields [11].

(iii) Frequency multiplication: THz radiation is also produced by up-

converting microwave frequencies by using a chain of diode multipliers. As nonlinear element can generate harmonics of an input RF signal, a frequency multiplier makes use of such nonlinear circuits to multiply an input frequency. In THz range, the dominant technology is based on gallium arsenide (GaAs) Schottky diodes [23] [24] [25]. In order to produce sufficient output power at terahertz frequency, a high power local oscillator is required to pump the multipliers. Frequencies of up to 1.9 THz with 0.5 μW output power were realized by using planar Schottky diodes (GaAs) frequency tripler while a 600 GHz (3 mW) BWO source was utilized in the case of [25]. One disadvantage of frequency multipliers is that noise levels are increased by the multiplication factors because noise variations get multiplied the same way as the frequency is multiplied. Also low power efficiency and short device lifetime are the main limitations of the frequency multipliers [26] [27].

(iv) Negative differential resistance (NDR) devices: The schematic circuit of NDR oscillator is shown in Figure 1.6. The impedance of the NDR device is represented by $Z_S = R_S + jX_S$, where R_S is the negative resistance. The load impedance is represented by $Z_L = R_L + jX_L$. To start oscillation, the whole circuit must be unstable which means that the total circuit resistance is negative, i.e. $R_S + R_L < 0$. Depending on the nonlinear characteristic of the NDR device, at frequency w_0, the oscillator will operate in a stable state such that

$$R_S(V_0, w_0) + R_L = 0 \tag{1.1}$$

$$X_S(V_0, w_0) + X_L(V_0, w_0) = 0 \tag{1.2}$$

where V_0 is the bias voltage, and the oscillating frequency w_0 is determined by Equation 1.2. The NDR device in a resonant circuit will compensate the positive resistance loss, so the oscillation will be sustained [26] [28].

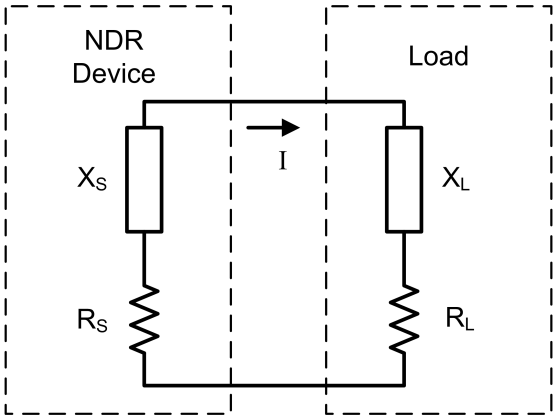

Figure 1.6: *The schematic circuit of negative differential resistance oscillator.*

Two terminal solid state devices such as Gunn diodes, impact ionization transit time (IMPATT) diodes, tunnel injection transit time (TUNNETT) diodes and RTD devices are common NDR devices. A Gunn diode is also known as a transferred electron device (TED) and is based on bulk properties of semiconductors. It only consists of N-doped semiconductor materials (e.g. GaAs, GaN, InP) [29–31]. As the electrons effective mass and mobility are different along different conduction band valley (Γ-valley and L-valley), Gunn diodes exhibit NDR with bias voltage. Gunn diode oscillators with fundamental frequency up to 162 GHz (25 mW) were achieved with devices on diamond heat sinks [32]. The IMPATT diode is basically a p-n junction diode, which is heavily reverse biased to the threshold voltage so that avalanche breakdown happens. Negative resistance characteristics of an IMPATT diode is produced by a combination of impact avalanche breakdown and charge-carrier transit time effects. The main

advantage of IMPATT diode is its high power capability, e.g. 25 mW at 217 GHz [33]. However, the maximum frequency of IMPATT diode is limited to low end frequencies of THz gap and IMPATT diodes suffer from high phase noise [12]. Another high frequency diode is the tunnel injection transit time (TUNNETT) diode. The concept of this diode was introduced by analysis of high frequency performance of the IMPATT diode. When the transit-time-negative resistance (TTNR) region is reduced to realize a high frequency oscillation of an IMPATT diode, electron tunnelling injection becomes dominant instead of the avalanche mechanism. Compared with the IMPATT diode, the advantages of TUNNETT diode are its low noise and high frequency [34]. At 706 GHz, the TUNNETT diode was demonstrated with output power of -67 dBm [35]. All the diode oscillators mentioned above were realized with rectangular waveguide (WR6-WR1.0) cavity technique, which is not compatible with MMICs, and their DC-RF conversion efficiency is normally low (<3 %) [32, 33, 35].

Resonant tunnelling diode (RTD), which make use of resonant tunnelling (through a quantum well) mechanism, is the fastest electronic device [1, 5, 12]. RTD oscillators were estimated to be able to operate up to 2.5 THz at room temperature [36]. Up to date, the highest reported frequency of a single RTD oscillator was 1.1 THz with 0.1 μW output power [37]. For RTD oscillators, the DC-RF conversion efficiency can also reach as high as 20% theoretically [38]. Therefore, the RTD device shows great potential for bridging the THz gap, especially for frequencies greater than 300 GHz, where other electronic devices are difficult to implement. At the moment, the main limitation of RTD sources is the low output power. This project aims to raise the power level of RTD oscillators in W-band frequency range (75-110 GHz).

1.3 State of the Art

For the first two decades of RTD device development from 1980s, RTD oscillators were realized using a quasi-optical resonator [39–43]as shown in Figure 1.7. A single RTD was mounted in a rectangular waveguide. The resonator was made

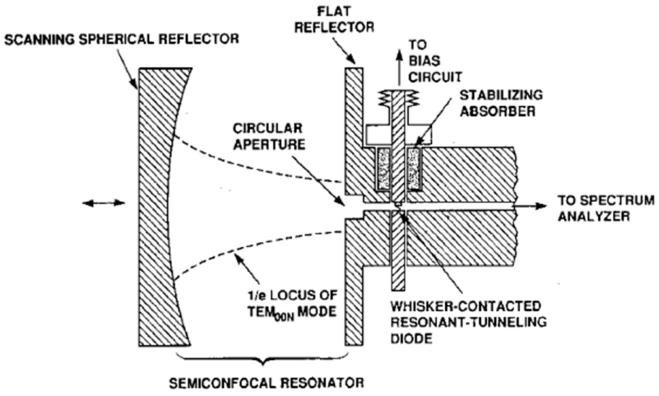

Figure 1.7: *Schematic cross-section of a quasi-optical RTD oscillator [39] [42].*

of a metallic plate acting as a semi-confocal resonator. Spurious bias oscillations were suppressed by a very lossy transmission line. Due to the large contact inductance (whisker contact) and series resistance, it was impractical to stabilize the DC bias circuit and a large portion of power was dissipated over the series resistance. The highest frequency of this quasi-optical RTD oscillator was 720 GHz with only 0.3 μW output power [41], and the highest power obtained was 50 μW for a single RTD oscillator operating at 210 GHz [43].

To overcome limitations of quasi-optical RTD oscillators, planar waveguide RTD oscillators were proposed with a single RTD device mounted within a slot metal film as described in [44–49]. This slot performs as a resonator sustaining a standing wave of electromagnetic field and also an antenna to radiate RF power at the same time [50]. The highest frequency of the single RTD slot antenna

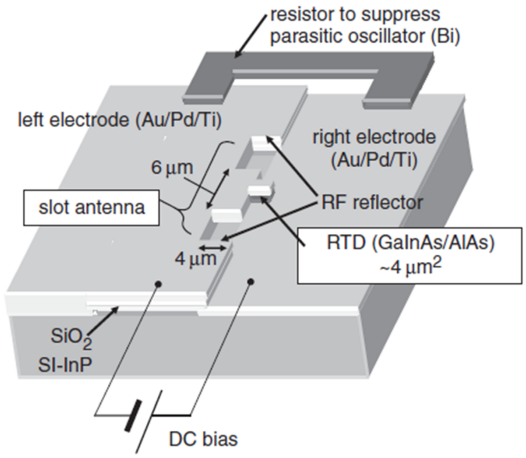

Figure 1.8: *Schematic diagram of a slot antenna- RTD oscillator [39] [42].*

oscillator published is 1.3 THz with 10 μW output power [51]. Due to the limited output power of such single oscillator, spatial power combining techniques by employing several oscillators as an antenna array were demonstrated [37] [45] [52]. The highest power obtained to date is 5 mW at 1.18 GHz, when 25 single RTD slot antenna oscillators were employed in parallel [53].

The schematic circuit of an RTD slot antenna (Figure 1.8) is shown in Figure 1.9, where $-G_n$ and C_n represent the negative conductance and self-capacitance of RTD device. $L_{an}$and C_{an} represent the inductance and capacitance of the slot antenna. R_L represent the radiation resistance. C_n, C_{an} and L_{an} determine the oscillation frequency. For a slot antenna, the impedance varies from infinity at the centre of the slot to zero at the edge of the slot. When an RTD is located at the center of the slot, the oscillator suffers from severe impedance mismatching, and the output power is low. To address this problem, the off-set slot antenna was developed to increase the output power. Published experimental results showed increased power by placing the RTD at different locations in a slot [46, 48, 49, 54].

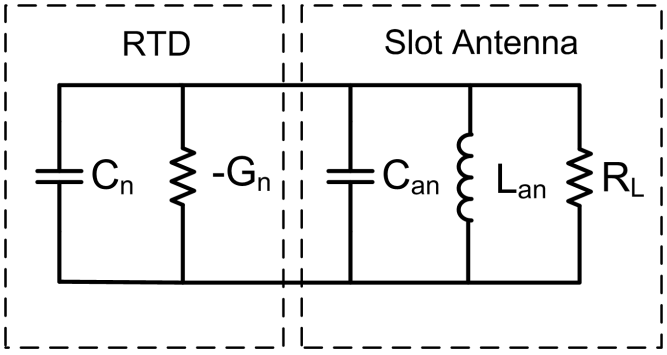

Figure 1.9: *Schematic circuit of a RTD slot antenna oscillator.*

However, the physical layout limits the impedance matching improvement of such offset slot antennas. For example, for the 650 GHz oscillator, the length of a slot antenna is only 30 μm [50]. For even higher frequency (1.02 THz), the slot length becames shorter (20 μm) [55]. The slot length is comparable to the geometry size of the RTD device ($2 - 4\ \mu m^2$) which makes the offset difficult to control.

Efforts have also been devoted to develop the RTD slot antenna oscillator array, where several oscillators were placed close to each other [47] [56]. But no procedure has been developed to realize power combining in a specific direction in space. The locations of individual oscillators was not uniquely defined, therefore the power can be combined or cancelled in unexpected directions.

The performance of RTD quasi-optical oscillators, slot antenna oscillators and the oscillators presented in this project are compared in Figure 1.10 in terms of frequencies versus power. It shows at the low frequency end (W-band), the output power of the oscillators in this project (red star) is much higher than other RTD oscillators operating in the similar frequency range. The details of the RTD oscillators designed and realised on this project will be described in the following chapters.

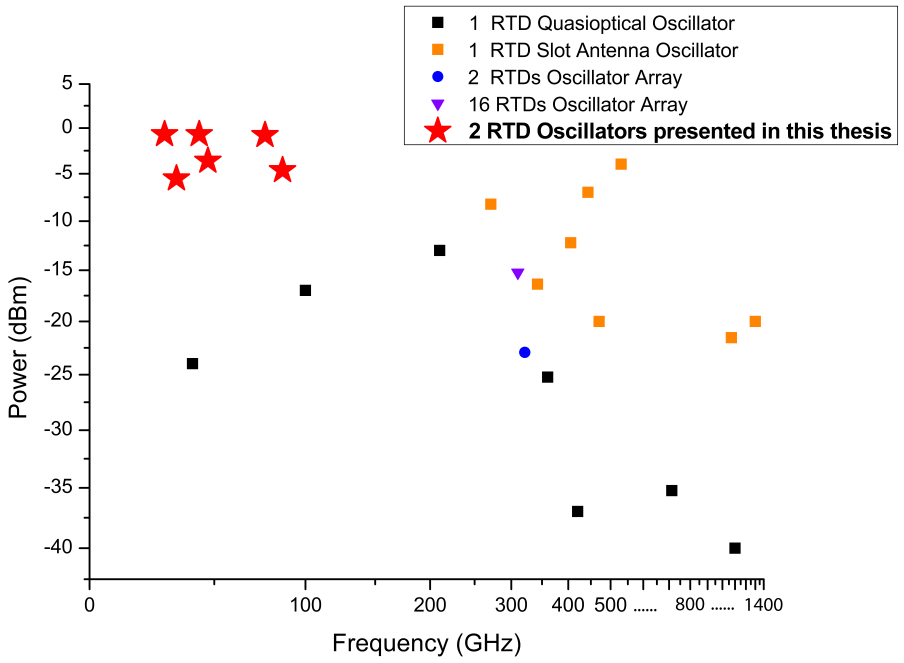

Figure 1.10: *State of the art RTD oscillator development [37, 39–43, 45, 47–50, 52, 54, 55, 57].*

1.4 Project Organization and Aim

This thesis is organized as follows: Chapter 1 is the introduction, and reviews THz sources in general and the development of RTD oscillator research. Chapter 2 describes a new self-consistent numerical model, which is based on quantum physics to simulate the current-voltage (I-V) characteristic of an RTD device, in particular the negative differential resistance (NDR) region. Chapter 3 explains the device and oscillator monolithic microwave integrated circuit (MMIC) fabrication techniques including photo lithography, dry/wet etching, metallization, lift-off and especially the new via opening process through polyimide developed in this project. Chapter 4 describes the passive components, including coplanar waveguide (CPW), metal-insulator-metal (MIM) capacitor, and thin film resistor

(NiCr). The description covers their design and experimental characterisation. These components were characterized using DC and scattering parameters (S-parameter) measurements. The ohmic contact resistance of the RTD, which plays an important role in oscillator performance, was also analysed using the transmission line model (TLM) method. The results of this analysis are presented in Chapter 4. Chapter 5 describes the design procedure of MMIC RTD oscillators employing two RTDs in parallel. There are two different double RTD oscillator layouts (type I and type II) designed in this project. Both layouts employed the same power combining topology. In Chapter 6, the frequency and output power measurement of these double RTD oscillators with two different layouts are described. These oscillators operated at 28.7 GHz, 33.7 GHz, 39.6 GHz, 75.2 GHz and 86.5 GHz, and most of them presented relatively high out power (around 1 mW). Finally, conclusions and future work are discussed in Chapter 7.

The aim of this PhD project was to realize monolithic microwave/millimetre wave integrated circuit (MMIC) RTD oscillator with operating frequencies up to 100 GHz with around a milli-Watt output power. The work is based on a power combining circuit topology, in which multiple RTD devices could be employed in a single oscillator circuit [38]. The key was to bias each device individually in the NDR region with shunt resistors to keep the device stable, and also to maximize the device size according to the stability criteria. Details about this circuit topology will be given in Chapter 5. The power combining circuit was proposed by Liquan Wang [38]. A hybrid oscillator prototype using 2 tunnel diodes was realized in his work. The measured output power was 0.22 mW at 437 MHz with DC to RF conversion efficiency over 50% [58]. In this project, the hybrid circuit has been scaled up to realise MMIC RTD oscillators with milli-

Watt output power. 75.2 GHz and 86.5 GHz MMIC RTD oscillators with output power -0.2 dBm (0.96 mW) and -4.6 dBm (0.35 mW), respectively, have been achieved so far, which to the author's knowledge are the highest output power published for RTD oscillators in W-band (75-110 GHz) frequencies.

Chapter 2

Self-Consistent RTD Numerical Model

2.1 Introduction

Resonant tunnelling theory was first proposed by Tsu and Esaki in 1973 [59] and the I-V characteristics with peak tunnelling current at resonant energy were observed experimentally on double barrier heterostructure ($GaAs/Al_{0.7}Ga_{0.3}As$) in 1974 [60]. The development of epitaxial crystal growth techniques such as molecular beam epitaxy (MBE) in the 1970s led to a great improvement in high quality RTD heterostructure materials growth. Extensive research has been devoted to resonant tunnelling devices since then.

In this chapter, the content is organized as follows: The first section has introduced the RTD heterostructure. The next two sections introduce the development of RTD heterostructures including those based on III-V materials and on Silicon. The fourth section describes the operating principle of the RTD device.

In section five, a new self-consistent model is developed to simulate the I-V characteristics of a single RTD device for a given layer structure. The final section discusses the simulation results.

The resonant tunnelling diode (RTD) is a two terminal electronic device that consists of a narrow band gap layer (quantum well) sandwiched between two thin wide band gap layers (barriers). The schematic layer structure of the RTD employed in this project is shown in Figure 2.1. It is noted that the undoped in-

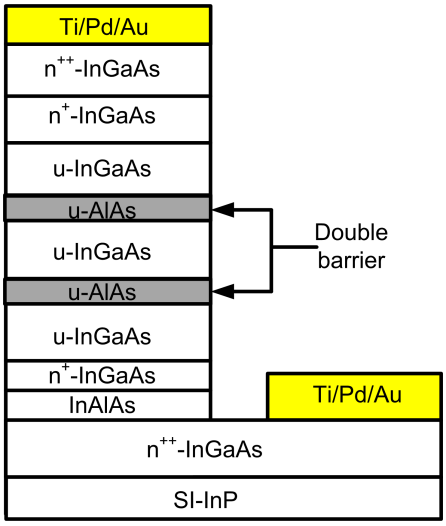

Figure 2.1: *The schematic layer structure of an InP-based RTD device employed in this project.*

dium gallium arsenide (InGaAs) is sandwiched between two thin un-doped indium aluminium (AlAs) layer. Because of the difference of these two semiconductor material bandgaps, a double barrier quantum well (DBQW) is formed. The band diagram of the DBQW is shown in Figure 2.2. There are several quantized energy states (E_{r1} and E_{r2}) existing in the well according to quantum mechanical theory. The term"resonant" in the name of resonant tunnelling diode refers to the behaviour of electrons with kinetic energy lower than the barrier potential

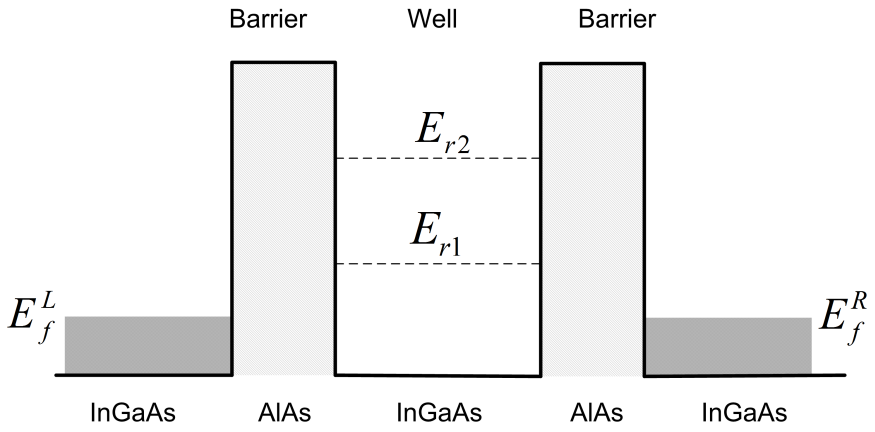

Figure 2.2: *The schematic conduction band diagram of a double barrier quantum well (DBBQW) RTD device. E_f^L and E_f^R denote the Fermi level of the left and right contact layer. E_{r1} and E_{r2} denote the quantized resonate state in the quantum well.*

but that still are able to travel though the double barriers. The possibility of electrons tunnelling through the barriers is defined by the transmission coefficient. At the resonant state, the transmission coefficient is close to unity. As the transmission coefficient of electrons tunnelling through the DBQW changes with the bias voltage, the I-V characteristic of resonant tunnelling devices exhibits negative differential resistance (NDR) [61–63].

RTD device is an attractive device, not only because it provides an insight into quantum mechanics theory, but also it shows broadband negative differential resistance from DC up to THz [36], which makes it a very promising electronic device for THz applications. Up to now, RTD oscillators with fundamental frequencies over 1 THz have been reported [37] [55]. However, the output power of the reported THz RTD oscillators is very low. The strategies to raise the power level of RTD oscillators has involved optimizing RTD layer structure to obtain a large peak-valley bias voltage difference (ΔV) and peak-valley bias current difference (ΔI), details of which will be explained in Chapter 3.

In order to engineer the RTD layer structure, a new numerical RTD model based on the resonant tunnelling mechanism was developed on this project. This computational model is different from other published works [62] [64]. Details will be explained in this chapter. It is expected that this model will support the design and optimization of RTD layer structures in high power THz RTD oscillator design.

2.2 Heterojunction

A heterojunction is a junction between two dissimilar semiconductor materials where the crystal structure is continuous across the interface [65]. A heterostructure normally consists of several thin heterojunction layers. Semiconductor film growth has benefited from modern epitaxial layer growth techniques such as molecular beam epitaxy (MBE) or metal organic chemical vapour deposition (MOCVD). Both techniques provide high quality semiconductor materials growth with precise composition and thickness control. As in this project the indium phosphide (InP) based RTD wafers were grown by MBE, MBE will be introduced briefly. Figure 2.3 shows the basic components of an MBE system. The sample is held in an ultra high vacuum chamber ($\sim 10^{-11}$ torr vacuum when fully pumped down). In each effusion cell high purity elements such as Si, Ga, Al, As, In and P are heated to generate atomic or molecular beams. Atoms of the elements travel in a straight line to impinge on a heated substrate. A shutter is placed in front of each effusion cell to control the composition of the material grown. Selecting a slow growth rate, allows for monolayer ($\sim$0.3 nm) growth. It is possible to grow high quality crystals while making abrupt changes in doping

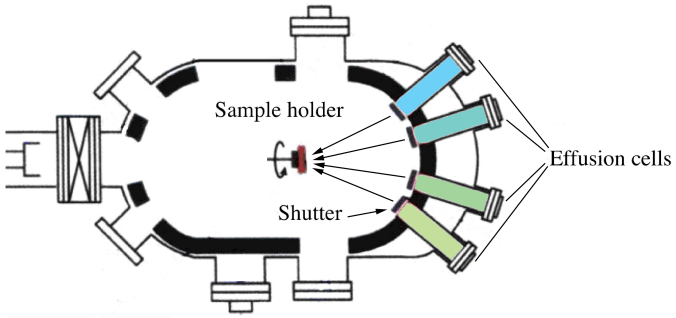

Figure 2.3: *The simplified MBE growth system.*

and crystal composition [61].

The epitaxial growth of two different semiconductor materials requires that they have a similar lattice constant to minimize the material stress. The stress will prevent thick epitaxial layer growth. The $In_xGa_{1-x}As/InP$ system lattice constant with different mole fraction x is shown in Figure 2.4 [61]. It is noted that when x=0.53, $In_xGa_{1-x}As$ has the same lattice parameter with InP which indicates that $In_{0.53}Ga_{0.47}As$ can be grown epitaxially on an InP substrate. Figure 2.4 shows the band gaps of different alloys. The band diagram can be engineered to improve the performance of resonant tunnelling devices by employing large band gap material with consistent lattice parameters.

2.3 RTD Material Systems

With the development of modern epitaxial growth techniques, high quality nano-scale heterostructure is attainable. RTD devices based on III-V semicon-

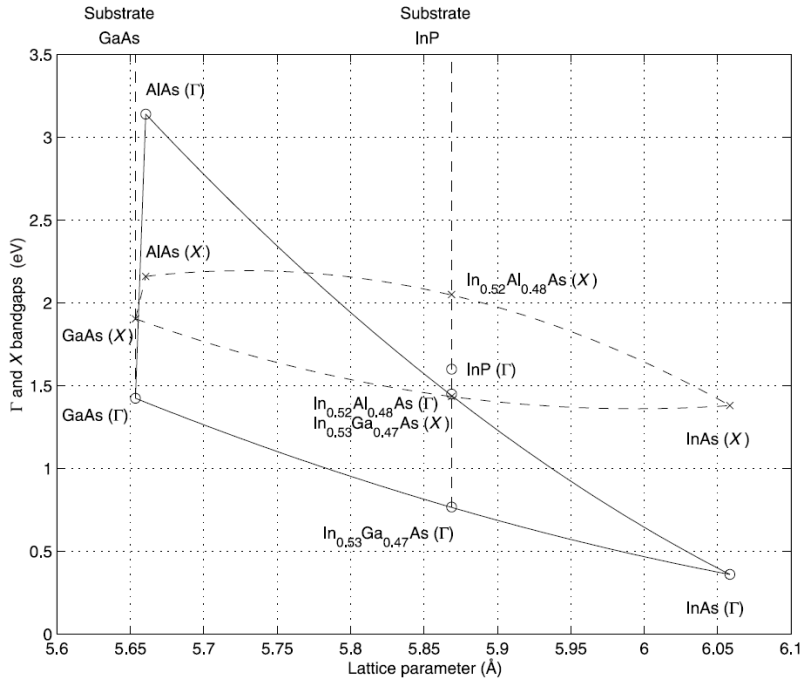

Figure 2.4: *Direct Γ (solid line) and indirect X (dashed line) band gaps of the alloys of the semiconductor binaries GaAs, AlAs and InAs, plotted versus their lattice parameters for all mole fractions x [61] .*

ductor materials have been published with record high peak current density $J_p = 2.4 \times 10^3\ kA/cm^2$, and oscillators with record oscillation frequencies over 1 THz [37] [55]. Meanwhile, due to the requirement for compatibility with silicon CMOS processing, Silicon-based RTDs are also being investigated by researchers [66–70].

2.3.1 III-V Based RTDs

RTD devices realized in III-V materials show attractive characteristics, such as THz intrinsic cut-off frequency, high peak current density and high peak valley current ratio (PVCR) performance [37, 41, 55, 71, 72]. The parameters of commonly used III-V semiconductor materials for RTDs are shown in Table 2.1,

in which the effective mass (m^*) , band gap (E_g), relative dielectric constant (ϵ_r) and conduction band offset (ΔE_c) of the different RTD material systems are compared. In general, small electron effective mass leads to high mobility and improved transport properties, and high conduction band offset will improve the PVCR by suppressing the thermal electron current [73].

Table 2.1: *III-V RTD material parameters (at room temperature (300K)) [62] [63] [74]*

Material	m^*	$E_g(eV)$	ϵ_r	$\Delta E_c(eV)$
GaAs	$0.067m_0$	1.42	12.9	0.28
AlAs	$0.1m_0$	2.16	10.1	
$In_{0.53}Ga_{0.47}As$	$0.042m_0$	0.71	12.9	0.65
AlAs	$0.1m_0$	2.16	10.1	
InAs	$0.027m_0$	0.36	14.6	1.35
AlSb	$0.12m_0$	1.61	12.04	
$Al_xGa_{1-x}As$	$(0.067 + 0.083x)m_0$	$1.424 + 1.247x$	$(12.90 - 2.84x)$	N/A
$Al_{0.48}In_{0.52}As$	$0.084m_0$	1.51	12.45	N/A

Note: $m_0 = 9.11 \times 10^{-31} kg$ is the electron rest mass.

Gallium Arsenide Based RTDs: GaAs/$Al_xGa_{1-x}As$ Material System

After the resonant tunnelling phenomenon was first demonstrated in 1973 [59], extensive research contributed to the first prototype RTD device based on the GaAs/$Al_xGa_{1-x}As$ material system [71] [72]. GaAs (low band gap) was sandwiched between $Al_xGa_{1-x}As$ barriers (high band gap). By changing the composition (mole fraction x) of Al and Ga, when $x = 0.42$, high PVCR=3.9 at room temperature with $J_p = 7.7\ kA/cm^2$ were reported by Huang et al in 1987 [71]. Oscillator frequency up to 420 GHz ($0.2\ \mu W$) was reported based on a GaAs/AlAs material system [39].

The conduction band offset between GaAs and $Al_xGa_{1-x}As$ is estimated by

Equation 2.1 [62].

$$\Delta E_c(x) = \begin{cases} 0.748x & (0 < x < 0.45) \\ 0.6[1.247x + 1.147(x - 0.45)^2] & (0.45 < x) \end{cases} \tag{2.1}$$

The electron effective mass $m^* = (0.067 + 0.083x)m_0$ for $Al_xGa_{1-x}As$ and $m^* = 0.067m_0$ for GaAs. The typical specific contact resistance (ρ_C) reported was about 10^{-6} Ωcm^2 and the saturation velocity of electrons in n^+-GaAs layer was less than 1×10^7 cm/s [62] [75]. Due to low barrier potential and high effective mass, as shown in Table 2.1, compared to InGaAs/AlAs, the PVCR and J_p of GaAs/$Al_xGa_{1-x}As$ material RTD is lower.

Indium Phosphide Based RTDs: InGaAs/$Al_xIn_{1-x}As$ Material System

Effort has been devoted to develop low effective mass and high conduction band offset semiconductor materials. The effective mass of $In_{0.53}Ga_{0.47}As$ is $0.044m_0$ which is much smaller than $0.067m_0$ for GaAs and the conduction band offset $\Delta E_C = 0.65$ eV higher than GaAs/AlGaAs system [62]. A specific contact resistance (ρ_C) less than 10^{-9} Ωcm^2 with a saturation velocity more than 1.5×10^7 cm/s is attainable in InGaAs/$Al_xIn_{1-x}As$ system [76]. Impressive results have been achieved in InGaAs/AlAs system. Better RTD performance with large $J_p = 2.4 \times 10^3$ kA/cm^2 and PVCR$\approx$ 2 was reported [55]. And the highest published RTD oscillator frequency is 1.3 THz (10 μW) [51] which was realised in the InGaAs/AlAs material system.

The RTD device utilized in this project is InGaAs/AlAs RTD. The details of each layer are shown in Table 2.2. Specifically, from the top layer to the bottom

Table 2.2: *The specific layer structure of the RTD device used in this project.*

Layer	Thickness (Å)	Composition	Doping Level(cm^{-3}):Dopant	Description
1	400	$In_{0.53}Ga_{0.47}As$	3×10^{19}:Si	Contact layer
2	800	$In_{0.53}Ga_{0.47}As$	2×10^{18}:Si	Emitter/Collector
3	500	$In_{0.53}Ga_{0.47}As$	2×10^{16}:Si	Spacer layer
4	14	AlAs	Un-doped	Barrier
5	55	$In_{0.53}Ga_{0.47}As$	Un-doped	Well
6	14	AlAs	Un-doped	Barrier
7	500	$In_{0.53}Ga_{0.47}As$	2×10^{16}:Si	Spacer layer
8	800	$In_{0.53}Ga_{0.47}As$	2×10^{18}:Si	Collector/Emitter
9	100	$In_{0.52}Al_{0.48}As$	1×10^{19}:Si	Etch stop layer
10	2000	$In_{0.53}Ga_{0.47}As$	3×10^{19}:Si	Contact layer
11	2000	$In_{0.53}Ga_{0.47}As$	2×10^{19}:Si	Buffer layer
12	SI: InP (635 μm)			Substrate

layer, the device consists of: a highly n-type doped contact layer ($In_{0.53}Ga_{0.47}As$); a collector/emitter layer ($In_{0.53}Ga_{0.47}As$), depending on the bias polarity; a spacer layer ($In_{0.53}Ga_{0.47}As$); a 1.4 nm un-doped barrier layer (AlAs); a 5.5 nm un-doped quantum well layer ($In_{0.53}Ga_{0.47}As$); another 1.4 nm un-doped barrier layer (AlAs); followed by a spacer layer ($In_{0.53}Ga_{0.47}As$); an emitter/collector layer ($In_{0.53}Ga_{0.47}As$); an etching stop layer ($In_{0.52}Al_{0.48}As$); a highly n-doped contact layer and the bottom layer is 200 nm $In_{0.53}Ga_{0.47}As$ buffer layer which is lattice matched and grown on the substrate (InP). The unintentional doping spacer layers ($In_{0.53}Ga_{0.47}As$) delivers two main advantages. One is to reduce the diffusion of impurities from the high doping layer to the barrier layer. The other is that they improve the device high frequency performance by reducing the junction capacitance [77] [61].

Gallium Arsenide Based RTDs: InAs/AlSb Material System

The InAs/AlSb system has several advantages over GaAs/AlGaAs and InGaAs/AlAs system such as low effective mass and high conduction band offset.

The effective mass of InAs is $0.023m_0$ and the conduction band offset is about 1.35 eV [78] [79]. The low specific contact resistance ($10^{-9}\ \Omega\ cm^2$), high saturation velocity of electrons ($5 \times 10^7\ cm/s$) benefit InAs/AlSb material system over other materials. The published highest single RTD oscillator frequency based on InAs/AlSb material system was 712 GHz with 0.3 μW power [41]. However InAs/AlSb system may suffer from impact ionization because of the low band gap of InAs (E_g=0.36 eV). At relatively high electric fields, an electron with energy slightly large than the band gap could collide with an electron in the valence band and knock it out into the conduction band. In the final state, two electrons exists in the conduction band and one hole in the valence band. The number of current carriers are therefore multiplied. This process places an important limitation on the power of devices because once the impact ionization starts, the current increases rapidly due to carrier multiplication. This phenomenon is also referred to as avalanche breakdown. Large band gap semiconductor devices are therefore preferred for high power applications [74].

2.3.2 Silicon-based RTDs

Attempts have been made to integrate an RTD into a complementary metal oxide semiconductor (CMOS) process with different silicon-based material systems such as Si/SiGe [66] [67], Si/CaF_2 [68], Si/SiO_2 [69], Si/γ-Al_2O_3 [70]. Successful integration will simplify logic circuit design by reducing the device size and number, improve the high frequency response and reduce the power consumption for present Si-based technologies [80]. Due to the difficulty in obtaining high quality interfaces on the Si-based approaches, most Si-based RTDs exhibit poor

performance with low peak current density (J_p) and peak to valley current ratio (PVCR) compared to III-V RTDs. It should be mentioned that improved n-type SiGe RTD shows comparable performances to III-V RTDs with $J_p = 282\ kA/cm^2$, PVCR=2.4 at room temperature, however the heating effects (due to the poor thermal conductivity of SiGe) lead to strongly area-dependent J_p [67]. Applications utilizing SiGe heterostructure have not been demonstrated at present.

Comparing III-V RTDs and silicon RTDs, for III-V RTDs, especially with InGaAs/AlAs material, the growth and fabrication technique is more mature. High J_p and PVCR are obtainable due to the small effective mass, high barrier conduction band discontinuity and low contact resistance. In this project, RTDs based on InGaAs/AlAs material system were utilized.

2.4 Operating Principle of RTD

The operating principle of RTD can be illustrated with the conduction band diagram shown in Figure 2.5 [61] [62]. When no bias voltage is applied (Figure 2.5 (a)), no current is observed due to thermal equilibrium. When bias voltage increases from zero, the conduction band profile of the double barrier quantum well (DBQW) shifts as shown in Figure 2.5 (b). Electrons obtain kinetic energy under an electric field. The probability of electrons tunnelling through the barriers (tunnelling current) increases in accordance with the bias voltage. This corresponds to the first positive differential resistance (PDR) region on the device's current-voltage (I-V) characteristic (Figure 2.6). When the energy of electrons corresponding to the increased bias voltage reaches the resonant energy state, the transmission coefficient is unity, which means a large amount of electrons

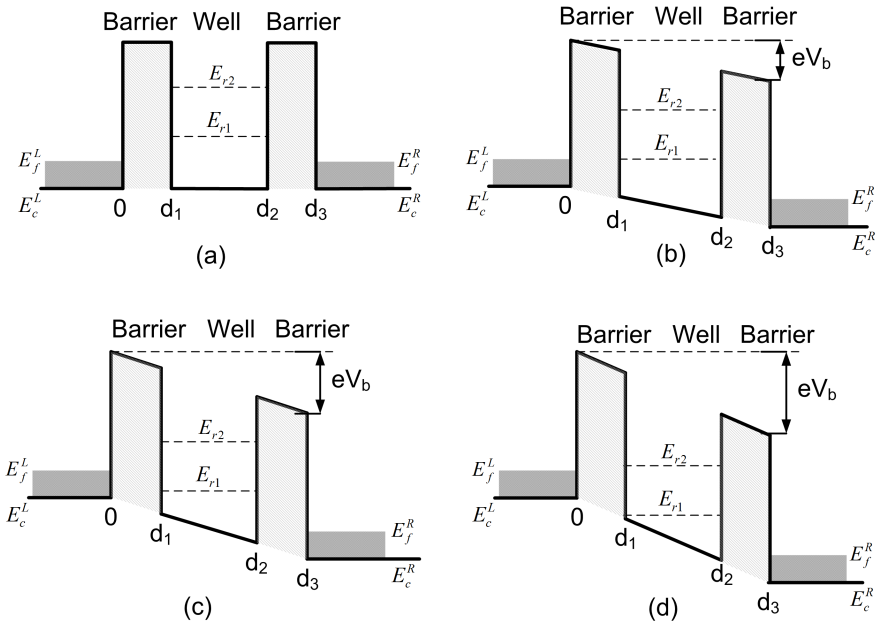

Figure 2.5: *Conduction band diagram of DBQW under different bias voltage(V_b):(a) no bias applied (b) threshold bias (c) resonant tunnelling (d) off resonance. E_f^L and E_f^R are the Fermi level of left emitter layer and right collector layer respectively. E_c^L and E_c^R are the conduction band edge of the emitter and collector. E_{r1} and E_{r2} represent the resonant energy state in the quantum well.*

will tunnel though the DBQW structure without being reflected. The peak DC current (I_p) is observed in the I-V plot (Figure 2.6). With further increase of the bias voltage, the transmission coefficient reduces drastically, so the current reduces with the increase of bias voltage. This region between V_p and V_v is also referred to as the negative differential resistance (NDR). The current is reduced due to the low transmission coefficient. When a larger bias voltage is applied, thermal emission of electrons contributes to most of the current [61] [62], so the current increases with the bias proportionally. The behaviour of electrons tunnelling is characterized by the wave function and the quantized state energy is defined by the Schrödinger equation. In quantum mechanics, the Schrödinger equation describes how the quantum state of particles changes in the form of

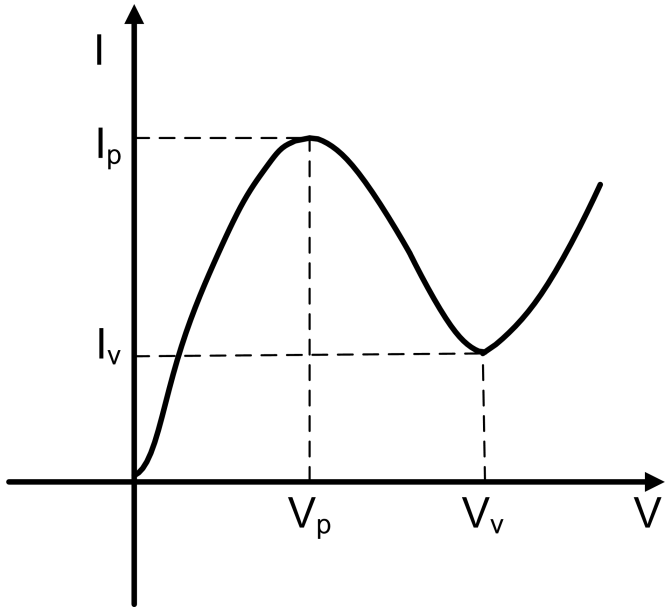

Figure 2.6: *The schematic current-voltage(I-V) characteristic of a RTD device. V_p is the bias voltage associated with the peak current I_p, while V_v denotes the bias voltage associated with the valley current I_v*

wave function $\Psi_1(z,t)$. Assuming sinusoidal time dependence of the form e^{-jwt} (note the negative sign in the exponent) and that $\Psi_1(z,t) = \Psi(z)\varphi(t)$ [81], the one dimensional time-independent Schrödinger equation takes the form

$$-\frac{\hbar^2}{2m^*}\frac{\partial^2}{\partial z^2}\Psi(z) + V(z)\Psi(z) = E_z\Psi(z) \tag{2.2}$$

where m^* is the electron effective mass, $\hbar$ is the reduced Plank constant, E_z is the longitudinal electron energy, $V(z)$ includes the barrier potential height (U_B) introduced by the heterojunction, the bias voltage (V_b) applied across the DBQW structure, and the contribution of the doping impurities and mobile electrons (V_{sc}). $V(z)$ provides the computable factor in combination with Poisson's equation for self-consistent current-voltage (I-V) calculation. The details of the self-consistent model will be described in the next section.

2.5 Self-Consistent RTD Numerical Model

The self-consistent I-V calculation flow chart is shown in Figure 2.7. The self-

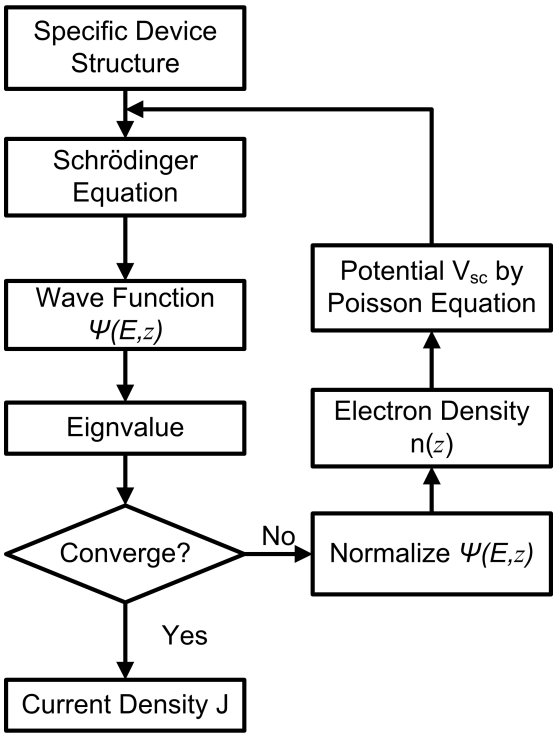

Figure 2.7: *Self-consistent IV calculation flow chart*

consistent calculation is achieved as follows: by solving the one-dimensional time-independent Schrödinger equation 2.2 in the perpendicular direction z, where the transverse x, y momentum is not considered, the electron wave function $\Psi(z)$ can be defined in the form of Airy functions [82–84]. According to the boundary condition that the wave function $\Psi(z)$ and its derivative $\frac{d\Psi(z)}{d(z)}$ must be continuous at the boundary of the quantum well and the barriers, the eigenvalue E_r in the quantum well is obtained. Meanwhile, because the space charge distribution in the quantum well gives rise to non-uniform potential profiles, the simple Fermi-Dirac distribution function can not describe the accumulated electrons accurately.

Electron density is therefore calculated by the non-equilibrium distribution function [62], and the resulting potential is derived from Poisson' s equation. The potential is substituted back into the Schrödinger equation leading to a new wave function solution. The wave function and eigenvalue are then calculated iteratively until the discrete eigenvalue E_r converge to a final solution. Once this is achieved, the current density is then obtained. This procedure was implemented by using MATLAB mathematical software. This computational model is similar to the model developed by Brennan in 1987 [64]. The difference is that instead of using transmission coefficient T_E to determine the convergence of computation, quasi-eigenvalue E_r convergence was used, because for a given DBQW structure, T_E are continuous values depending on both the electron energy (making the computation long) and the external bias, while E_r are discrete values depending on the external bias (improving convergence without loss of accuracy).

2.5.1 Finite Quantum Well Schrödinger Equation

The simple conduction band diagram of the InGaAs/AlAs DBQW structure, when no external bias voltage is applied, is shown in Figure 2.8, where the width of the quantum well is denoted as l_w. Assuming the electron effective mass m^* is constant across the barriers and quantum well, the rectangular barrier potential $V(z) = V$ when $|z| > \frac{l_w}{2}$. In this case, the Schrödinger equation 2.2 is solved

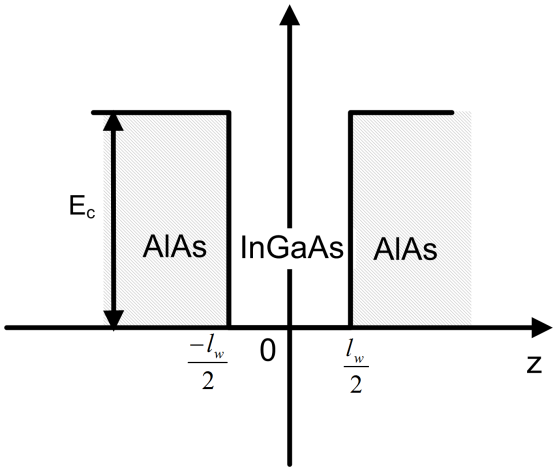

Figure 2.8: *The schematic conduction band diagram of InGaAs/AlAs with infinite barriers (AlAs) width. No external bias voltage is applied.*

separately in each region depending on l_w and so becomes

$$\begin{aligned} -\frac{\hbar^2}{2m^*}\frac{\partial^2}{\partial z^2}\Psi(z) &= (E-V)\Psi(z) \qquad z < -l_w/2 \\ -\frac{\hbar^2}{2m^*}\frac{\partial^2}{\partial z^2}\Psi(z) &= E\Psi(z) \qquad |z| \leq l_w/2 \\ -\frac{\hbar^2}{2m^*}\frac{\partial^2}{\partial z^2}\Psi(z) &= (E-V)\Psi(z) \qquad z > l_w/2 \end{aligned} \tag{2.3}$$

As the electron energy E is confined lower than the barrier potential V, $E - V \leq 0$, the general numerical solution is given by

$$\Psi(z) = \begin{cases} Ae^{\beta z} + A'e^{-\beta z} & z < -l_w/2 \\ Bcos(ikz) + B'sin(ikz) & |z| \leq l_w/2 \\ C'e^{\beta z} + Ce^{-\beta z} & z > l_w/2 \end{cases} \tag{2.4}$$

where $k = \sqrt{\frac{2mE}{\hbar^2}}$, $\beta = \sqrt{\frac{2m(V-E)}{\hbar^2}}$, A, A', B, B', C and C' are arbitrary constants.

The probability of an electron distribution over the DBQW region is unity,

which requires that

$$\int_{-\infty}^{\infty} |\Psi(z)|^2 dz = 1 \tag{2.5}$$

where $|\Psi(z)|^2$ represents the probability density of finding the electron. Equation 2.5 is the standard condition required to normalize the wave-function. As it is noted that

$$when \quad z \to -\infty, \qquad A'e^{-\beta z} \to \pm\infty \tag{2.6}$$

$$when \quad z \to +\infty, \qquad C'e^{\beta z} \to \pm\infty \tag{2.7}$$

which cannot satisfy the Equation 2.5, Equation 2.4 falls into two categories:

I. Even parity

$$\Psi(z) = \begin{cases} Ae^{\beta z} & z < -l_w/2 \\ Bcos(kz) & |z| \le l_w/2 \\ Ce^{-\beta z} & z > l_w/2 \end{cases} \tag{2.8}$$

II. Odd parity

$$\Psi(z) = \begin{cases} Fe^{\beta z} & z < -l_w/2 \\ Gsin(kz) & |z| \le l_w/2 \\ He^{-\beta z} & z > l_w/2 \end{cases} \tag{2.9}$$

where F, G and H are arbitrary constants. According to the boundary conditions that the wave function $\Psi(z)$ and its first derivative $\dfrac{\partial}{\partial z}\Psi(z)$ must be continuous, for even parity

$$Ae^{\beta(-\frac{l_w}{2})} = Bcos(k(-\frac{l_w}{2})) \qquad when \quad z = -\frac{l_w}{2} \tag{2.10}$$

$$Ce^{-\beta(\frac{l_w}{2})} = Bcos(k(\frac{l_w}{2})) \qquad when \quad z = \frac{l_w}{2} \tag{2.11}$$

Combining the above two equations gives $A = C$ and similarly for odd parity $F = -H$.

$$Fe^{\beta(-\frac{l_w}{2})} = Gsin(k(-\frac{l_w}{2})) \qquad when \quad z = -\frac{l_w}{2} \tag{2.12}$$

$$He^{-\beta(\frac{l_w}{2})} = Gsin(k(\frac{l_w}{2})) \qquad when \quad z = \frac{l_w}{2} \tag{2.13}$$

The wave function defined by Equation 2.8 and Equation 2.9 also must be continuous at the quantum well boundaries.

For even parity

$$when\ z = -\frac{l_w}{2}, \quad A\beta e^{\beta(-\frac{l_w}{2})} = -Bksin(k\frac{-l_w}{2}) \tag{2.14}$$

Dividing Equation 2.14 by Equation 2.10, gives

$$\beta = ktan(k\frac{l_w}{2}) \tag{2.15}$$

Now consider the function $f_{even}(E)$ such that

$$f_{even}(E) = ktan(k\frac{l_w}{2}) - \beta = \sqrt{\frac{2mE}{\hbar^2}}tan\left(\frac{l_w}{2}\sqrt{\frac{2mE}{\hbar^2}}\right) - \sqrt{\frac{2m(V-E)}{\hbar^2}} = 0 \tag{2.16}$$

The energy E can be derived from Equation 2.16 by Newton-Raphson iteration methodology. In quantum mechanical theory, the solution of E only exists for discrete values. These values are referred to as eigenvalue E_r. The calculation was considered for the InGaAs/AlAs DBQW physical structure used on this project, where the quantum well thickness $l_w = 5.5\ nm$ and the barrier thickness $l_b = 1.4\ nm$. After calculation, only one even parity eigenvalue ($E_{r1} = 140.68\ meV$) exists in the given RTD structure.

Similarly, for odd parity

$$when\ z = -\frac{l_w}{2}, \quad F\beta e^{\beta(-\frac{l_w}{2})} = Gkcos(k\frac{-l_w}{2}) \tag{2.17}$$

Dividing Equation 2.17 by Equation 2.12, gives

$$\beta = -kcot(k\frac{l_w}{2}) \tag{2.18}$$

and defining a function $f_{odd}(E)$ such that

$$f_{odd}(E) = -kcot(k\frac{l_w}{2}) - \beta = -\sqrt{\frac{2mE}{\hbar^2}}cot\left(\frac{l_w}{2}\sqrt{\frac{2mE}{\hbar^2}}\right) - \sqrt{\frac{2m(V-E)}{\hbar^2}} = 0 \tag{2.19}$$

After calculation, only one odd eigenvalue ($E_{r2} = 505.87\ meV$) exists for the same structure.

When a bias voltage is applied, the conduction band structure is shifted as shown in Figure 2.9. The potential energy V(z) is given by

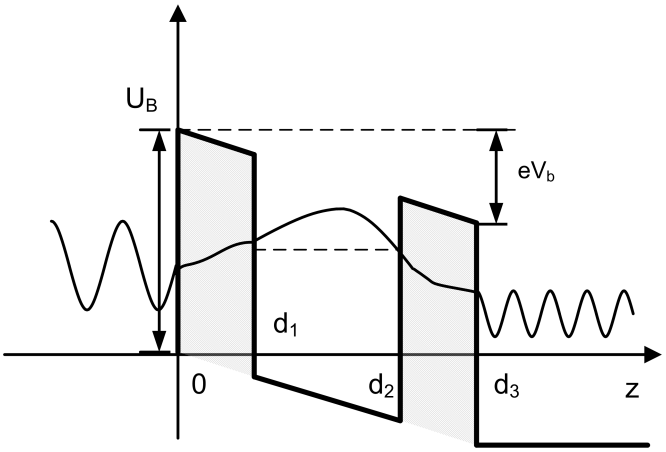

Figure 2.9: *RTD conduction band diagram under a bias voltage V_b. U_B is the barrier energy height.*

$$V(z) = \begin{cases} -\dfrac{eV_b}{d_3}z + U_B & 0 < z < d_1 \\ -\dfrac{eV_b}{d_3}z & d_1 < z < d_2 \\ -\dfrac{eV_b}{d_3}z + U_B & d_2 < z < d_3 \end{cases} \tag{2.20}$$

where U_B is the barrier potential energy, d_3 is the width of the DBQW including the double barriers and the quantum well.

When $0 < z < d_1$ and $d_2 < z < d_3$, substituting Equation 2.20 into the Schrödinger equation 2.2, gives

$$-\frac{\hbar^2}{2m^*}\frac{\partial^2}{\partial z^2}\Psi(z) - (\frac{eV_b}{d_3}z - U_B + E)\Psi(z) = 0 \tag{2.21}$$

If z is defined as

$$z = \alpha_0(\beta_z - \gamma_0) \tag{2.22}$$

where α_0 and γ_0 are arbitrary constants and β_z is dimensionless parameter, by using chain rule, Equation 2.21 becomes

$$\frac{\partial^2}{\partial\beta_z^2}\Psi(\beta_z) + \frac{2m^*}{\hbar^2}\alpha_0^2[\frac{eV_b}{d_3}\alpha_0(\beta_z - \gamma_0) - U_B + E]\Psi(\beta_z) = 0 \tag{2.23}$$

If the arbitrary constants α_0 and γ_0 are defined by

$$\begin{aligned} &\frac{2m^*}{\hbar^2}\frac{eV_b}{d_3}\alpha_0^3 = -1 \\ &\frac{eV_b}{d_3}\alpha_0\gamma_0 + E - U_B = 0 \end{aligned} \tag{2.24}$$

Equation 2.23 can be simplified to

$$\frac{\partial^2}{\partial\beta_z^2}\Psi(\beta_z) - \beta_z\Psi(\beta_z) = 0 \tag{2.25}$$

which is Airy's equation [84] [85]. When $d_1 < z < d_2$, Equation 2.23 remains unchanged only with $U_B = 0$. The Airy function approach provides an exact solution for structures consisting of piecewise linear potentials [86].

The full solution of Airy's equation is given by Equation 2.26 [83] [85].

$$\Psi(z) = \begin{cases} A_1^+ exp(jk_1z) + A_1^- exp(-jk_1z) & \text{if } z < 0 \\ A_2^+ Ai[\rho_2(z)] + A_2^- Bi[\rho_2(z)] & \text{if } 0 \le z < d_1 \\ A_3^+ Ai[\rho_3(z)] + A_3^- Bi[\rho_3(z)] & \text{if } d_1 \le z < d_2 \\ A_4^+ Ai[\rho_4(z)] + A_4^- Bi[\rho_4(z)] & \text{if } d_2 \le z < d_3 \\ A_5^+ exp(jk_5z) + A_5^- exp(-jk_5z) & \text{if } d_3 \le z \end{cases} \tag{2.26}$$

where Ai and Bi denote the Airy functions, and A_n^+, A_n^-, $(n = 1, 2...5)$ are arbi-

trary constants, with

$$\begin{aligned}
k_1 &= \frac{\sqrt{2m_L^* E_z}}{\hbar} \\
\rho_2(z) &= \left(\frac{2m_B^*}{\hbar^2}\right)^{\frac{1}{3}} (eF)^{-\frac{2}{3}}(U_B - E_z - eFz) \\
\rho_3(z) &= \left(\frac{2m_W^*}{\hbar^2}\right)^{\frac{1}{3}} (eF)^{-\frac{2}{3}}(-E_z - eFz) \\
\rho_4(z) &= \left(\frac{2m_B^*}{\hbar^2}\right)^{\frac{1}{3}} (eF)^{-\frac{2}{3}}(U_B - E_z - eFz) \\
k_5 &= \frac{\sqrt{2m_R^*(eV_b + E_z)}}{\hbar}
\end{aligned} \tag{2.27}$$

where $F = V_b/d_3$, V_b is the bias voltage.

The boundary continuity for the wave function $\Psi(z)$ requires

$$\begin{aligned}
&\Psi_{j-1}(z_j) = \Psi_j(z_j) \\
&\frac{1}{m_{j-1}^*}\frac{d}{dz}[\Psi_{j-1}(z_j)] = \frac{1}{m_j^*}\frac{d}{dz}[\Psi_j(z_j)]
\end{aligned} \tag{2.28}$$

Applying the boundary conditions to the wave function (2.26) gives

$$\begin{bmatrix} 1 & 1 \\ \frac{jk_1}{m_L^*} & \frac{-jk_1}{m_L^*} \end{bmatrix} \begin{bmatrix} A_1^+ \\ A_1^- \end{bmatrix} = \begin{bmatrix} Ai[\rho_2(z_0)] & Bi[\rho_2(z_0)] \\ \frac{\alpha}{m_{B1}^*}Ai'[\rho_2(z_0)] & \frac{\alpha}{m_{B1}^*}Bi'[\rho_2(z_0)] \end{bmatrix} \begin{bmatrix} A_2^+ \\ A_2^- \end{bmatrix} \tag{2.29}$$

$$\begin{bmatrix} Ai[\rho_2(z_1)] & Bi[\rho_2(z_1)] \\ \frac{\alpha}{m_{B1}^*}Ai'[\rho_2(z_1)] & \frac{\alpha}{m_{B1}^*}Bi'[\rho_2(z_1)] \end{bmatrix} \begin{bmatrix} A_2^+ \\ A_2^- \end{bmatrix} = \begin{bmatrix} Ai[\rho_3(z_1)] & Bi[\rho_3(z_1)] \\ \frac{\alpha}{m_W^*}Ai'[\rho_3(z_1)] & \frac{\alpha}{m_W^*}Bi'[\rho_3(z_1)] \end{bmatrix} \begin{bmatrix} A_3^+ \\ A_3^- \end{bmatrix} \tag{2.30}$$

$$\begin{bmatrix} Ai[\rho_3(z_2)] & Bi[\rho_3(z_2)] \\ \frac{\alpha}{m^*_W}Ai'[\rho_3(z_2)] & \frac{\alpha}{m^*_W}Bi'[\rho_3(z_2)] \end{bmatrix} \begin{bmatrix} A_3^+ \\ A_3^- \end{bmatrix} = \begin{bmatrix} Ai[\rho_4(z_2)] & Bi[\rho_4(z_2)] \\ \frac{\alpha}{m^*_{B2}}Ai'[\rho_4(z_2)] & \frac{\alpha}{m^*_{B2}}Bi'[\rho_4(z_2)] \end{bmatrix} \begin{bmatrix} A_4^+ \\ A_4^- \end{bmatrix} \tag{2.31}$$

$$\begin{bmatrix} Ai[\rho_4(z_3)] & Bi[\rho_4(z_3)] \\ \frac{\alpha}{m^*_{B2}}Ai'[\rho_4(z_3)] & \frac{\alpha}{m^*_{B2}}Bi'[\rho_4(z_3)] \end{bmatrix} \begin{bmatrix} A_4^+ \\ A_4^- \end{bmatrix} = \begin{bmatrix} e^{jk_5z_3} & e^{-jk_5z_3} \\ \frac{jk_5}{m^*_R}e^{jk_5z_3} & -\frac{jk_5}{m_R}e^{-jk_5z_3} \end{bmatrix} \begin{bmatrix} A_5^+ \\ A_5^- \end{bmatrix} \tag{2.32}$$

where $\alpha = -\left(\frac{2m^*_B eF}{\hbar^2}\right)^{\frac{1}{3}}$, m^*_{B1} is the first barrier effective mass, m^*_W is the quantum well effective mass, m^*_{B2} is the second barrier effective mass. Assuming $m^*_{B1} = m^*_{B2} = m_B$, let

$$\begin{aligned} \begin{bmatrix} M^t_{11} & M^t_{12} \\ M^t_{21} & M^t_{22} \end{bmatrix} = & \begin{bmatrix} 1 & 1 \\ \frac{ik_1}{m^*_R} & -\frac{ik_1}{m^*_R} \end{bmatrix}^{-1} \begin{bmatrix} Ai[\rho_2(z_0)] & Bi[\rho_2(z_0)] \\ \frac{\alpha}{m^*_{B1}}Ai'[\rho_2(z_0)] & \frac{\alpha}{m^*_{B1}}Bi'[\rho_2(z_0)] \end{bmatrix} \\ & \begin{bmatrix} Ai[\rho_2(z_1)] & Bi[\rho_2(z_1)] \\ \frac{\alpha}{m^*_{B1}}Ai'[\rho_2(z_1)] & \frac{\alpha}{m^*_{B1}}Bi'[\rho_2(z_1)] \end{bmatrix}^{-1} \begin{bmatrix} Ai[\rho_3(z_1)] & Bi[\rho_3(z_1)] \\ \frac{\alpha}{m^*_W}Ai'[\rho_3(z_1)] & \frac{\alpha}{m^*_W}Bi'[\rho_3(z_1)] \end{bmatrix} \\ & \begin{bmatrix} Ai[\rho_3(z_2)] & Bi[\rho_3(z_2)] \\ \frac{\alpha}{m^*_W}Ai'[\rho_3(z_2)] & \frac{\alpha}{m^*_W}Bi'[\rho_3(z_2)] \end{bmatrix}^{-1} \begin{bmatrix} Ai[\rho_4(z_2)] & Bi[\rho_4(z_2)] \\ \frac{\alpha}{m^*_{B2}}Ai'[\rho_4(z_2)] & \frac{\alpha}{m^*_{B2}}Bi'[\rho_4(z_2)] \end{bmatrix} \\ & \begin{bmatrix} Ai[\rho_4(z_3)] & Bi[\rho_4(z_3)] \\ \frac{\alpha}{m^*_{B2}}Ai'[\rho_4(z_3)] & \frac{\alpha}{m^*_{B2}}Bi'[\rho_4(z_3)] \end{bmatrix}^{-1} \begin{bmatrix} e^{jk_5z_3} & e^{-jk_5z_3} \\ \frac{jk_5}{m^*_R}e^{jk_5z_3} & -\frac{jk_5}{m^*_R}e^{-jk_5z_3} \end{bmatrix} \end{aligned} \tag{2.33}$$

$$\begin{bmatrix} A_1^+ \\ A_1^- \end{bmatrix} = \begin{bmatrix} M_{11}^t & M_{12}^t \\ M_{21}^t & M_{22}^t \end{bmatrix} \begin{bmatrix} A_5^+ \\ A_5^- \end{bmatrix} \tag{2.34}$$

This approach is often referred to as the Transfer Matrix Method (TMM) [82,83, 86,87]. To obtain the transmission coefficient T_E, it is assumed that all electrons approach the double barriers from the same side and there are no reflections happening on the right side of the heterostructure, which means that matrix (2.34) becomes

$$\begin{bmatrix} A_1^+ \\ A_1^- \end{bmatrix} = \begin{bmatrix} M_{11}^t & M_{12}^t \\ M_{21}^t & M_{22}^t \end{bmatrix} \begin{bmatrix} A_5^+ \\ 0 \end{bmatrix} \tag{2.35}$$

so

$$A_1^+ = M_{11}^t A_5^+ \tag{2.36}$$

$$A_1^- = M_{21}^t A_5^+ \tag{2.37}$$

The transmitted wave function is

$$\Psi_t = A_5^+ exp(jk_5 z) \tag{2.38}$$

and incident wave function is

$$\Psi_i = A_1^+ exp(jk_1 z) \tag{2.39}$$

The transmission coefficient T_E which refers to the probability ratio of the incident

and transmitted waves of a particular electron state is given by Equation 2.40.

$$T_E = \frac{v_5}{v_1}\frac{|\Psi_t|^2}{|\Psi_i|^2} = \frac{k_5}{k_1}\frac{1}{|M_{11}^t|^2} = \left(\frac{m_R^*(eV_b + E_z)}{m_L^*(E_z)}\right)^{1/2}\frac{1}{|M_{11}^t|^2} \tag{2.40}$$

where

$$\begin{aligned} v_5 &= \frac{\hbar k_5}{m^*} \\ v_1 &= \frac{\hbar k_1}{m^*} \end{aligned} \tag{2.41}$$

For the specific double barrier InGaAs(5.5 nm)/AlAs(1.4 nm) RTD structure, the calculated transmission coefficient as a function of the energy (E_z) under different applied bias voltage V_b is shown in Figure 2.10. When the energy of electrons equals the resonant energy, the transmission coefficient (T_E) is maximum. The quasi-eigenvalue can be derived numerically from Figure 2.10 by finding the maximum T_E. The calculated resonant energy in InGaAs/AlAs DBQW under different bias voltage (V_b) is shown in Table 2.3. As illustrated in the band diagram (Figure 2.5), with increase of the bias voltage, the resonant state energy is tilted down, so the calculated quasi-eigenvalue (E_{r1}, and E_{r2}) is reduced as expected.

Table 2.3: *Calculated resonant energy in InGaAs/AlAs DBQW Structure under different bias (V_b).*

Bias Voltage(V)	0.01	0.1	0.2	0.4
$E_{r1}(meV)$	103.2	57.4	6.1	-104.2
$E_{r2}(meV)$	468.4	423.8	374.9	278.9

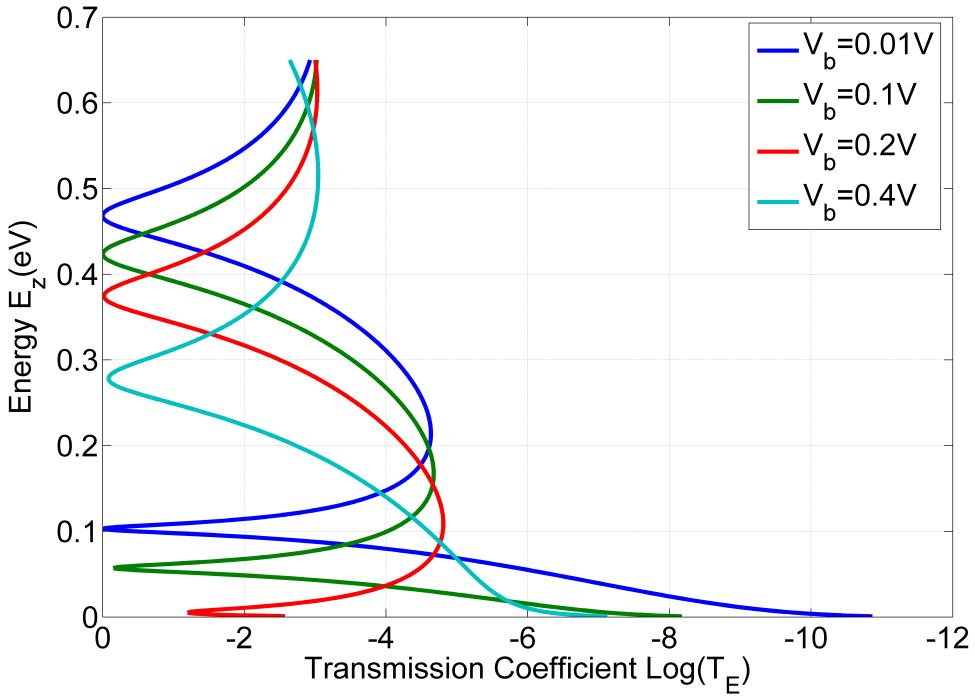

Figure 2.10: *Calculated transmission coefficient (T_E) as a function of the energy (E_z) with different bias voltage V_b for the DBQW structure shown in Figure 2.1*

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2.5.2 Normalized Wave Function

It is noted that there are unknown coefficients in the wave function either Equation 2.4 for the flat band diagram (A, A', B, B', C and C') or Equation 2.26 for the piecewise linear band diagram (A_n^+, A_n^-, $(n = 1, 2...5)$). The coefficients can be derived by wave function normalization. The standard condition for normalizing the wave function is shown in Equation 2.42, where $|\Psi(z)|^2$ is defined as the probability density of finding the electron at position z.

$$\int_{-\infty}^{+\infty} |\Psi(z)|^2 = 1 \tag{2.42}$$

Under bias voltage V_b, the full solution to the Schrödinger equation is the Airy's function, as shown in Equation 2.26. As solving the integration of Airy's function in Equation 2.42 is difficult, the following approximation has been made. Instead of a linearly reduced barrier potential, a constant barrier potential is approximated as shown in Figure 2.11, where l_w is the width of the quantum well. Thus the wave function can be represented by the sinusoidal wave function shown in Equation 2.4. The integration of the sinusoidal wave function becomes solvable analytically.

2.5.3 Electron Density and Poisson's Equation

In a doped semiconductor, there are two contributions to the charge density $n(z)$. One is the ionised doped impurities and the other is the free charge carriers [88]. The first one can be derived from the doping level, while the second can be calculated from the probability distributions of the carriers. The non-uniform potential arises from the distributions of carriers. The potential change

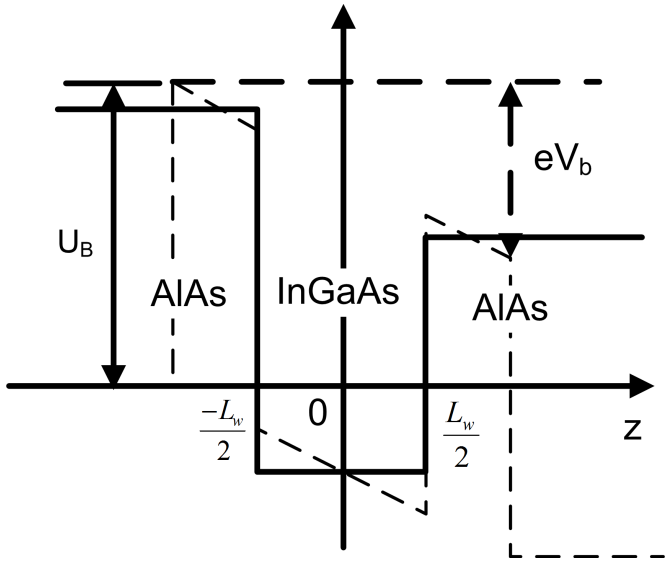


Figure 2.11: *The approximation of an RTD conduction band. The linearly varying energy potential (dotted line) was replaced with a flat constant potential (solid line). The approximation will benefit integrating wave function.*

cannot be neglected as they play an important part in the tunnelling mechanics [62] [89]. The electron density is given by Equation 2.43 including incident electrons from the left side of the DBQW ($n_l(z)$) and also from the right side of the DBQW ($n_r(z)$), where $E_{f,l}$ and $E_{f,r}$ is the Fermi energy on the left and right side respectively

$$\begin{aligned} n(z) &= n_l(z) + n_r(z) \\ &= \frac{mk_BT}{2\pi^2\hbar^2}\left[\int_0^\infty |\Psi(E_z)|^2 ln\left(1+e^{\left(E_{f,l}-\frac{E_z}{k_BT}\right)}\right)d(E_z)\right. \\ &\left. + \int_{-\infty}^0 |\Psi(E_z)|^2 ln\left(1+e^{\left(E_{f,r}-\frac{E_z}{k_BT}\right)}\right)d(E_z)\right] \end{aligned} \tag{2.43}$$

Substituting the normalized wave function $\Psi(E_z)$, which was obtained in the previous section, into Equation 2.43, the electron density can be calculated and is shown in Figure 2.12 for the simulated structure. It is noted that as the electrons tunnel through the DBQW in the form of wave function ($\Psi(E_z)$), at the centre of the quantum well ($z = 0$), the electron density is the maximum. As the barriers are undoped, the carrier density in the barriers ($2.75 < |z| < 4.15$) is the lowest. The electron distribution in the heterostructure gives rise to the

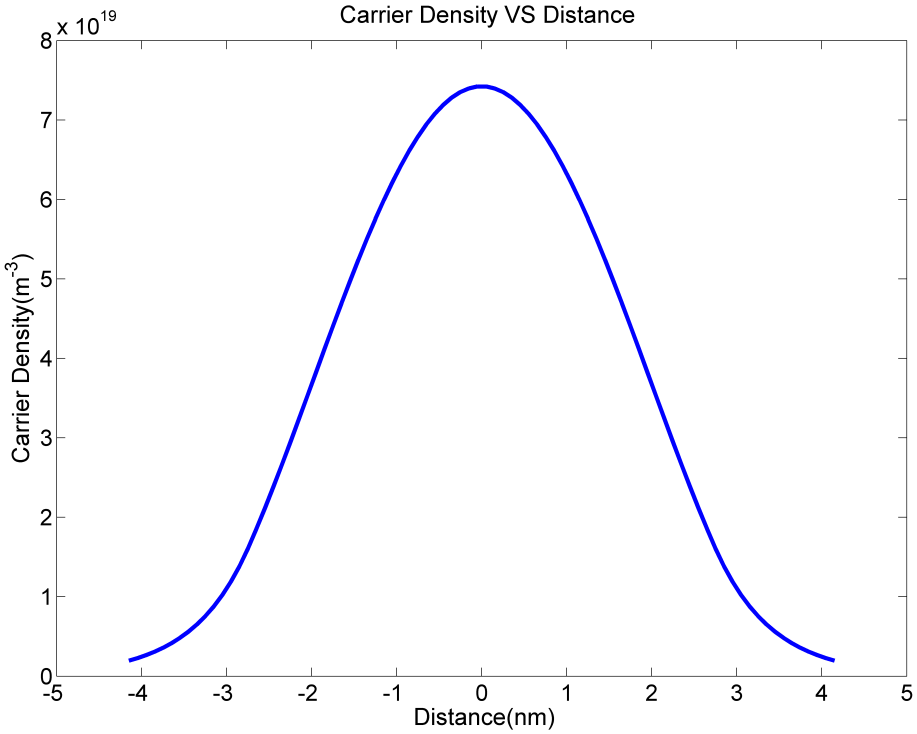


Figure 2.12: *Calculated distribution of electron density.*

additional potential energy V_{sc}. The potential V_{sc} can be calculated by Possion's equation

$$\frac{\partial}{\partial z}\left(\epsilon(z)\frac{\partial V_{sc}(z)}{\partial z}\right) = -e[N_D(z) - n(z)] \tag{2.44}$$

where $\epsilon(z)$ is the dielectric constant, and $N_D(z)$ is the density of doping impurities. In the un-doped barriers and quantum well, $N_D(z) = 0$. The potential V_{sc} due to electron distribution is plotted in Figure 2.13. In combination with Figure 2.12, as at the centre of the quantum well, the carrier density is large, which contributes to the high potential as shown in Figure 2.13. Similarly for low carrier density barriers, the potential is low accordingly. The potential V_{sc} derived from

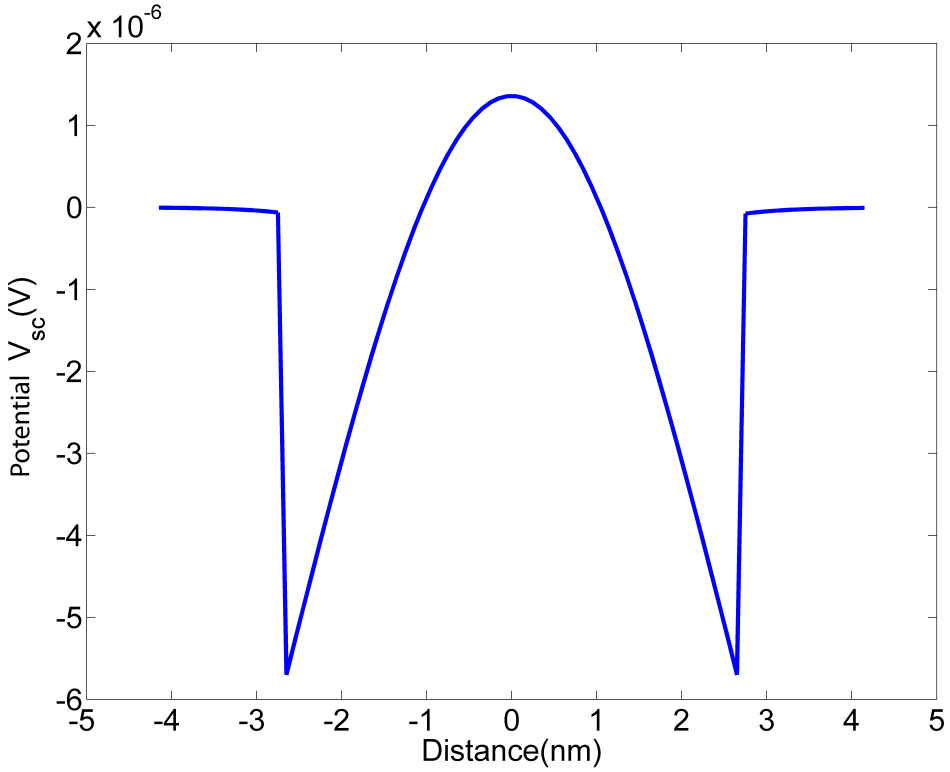


Figure 2.13: *The calculated potential (V_{sc}) due to the electron distribution.*

Equation 2.44 is then substituted back to the Schrödinger equation, where $V(z) = U_B + eV_{sc}$, and the calculation is repeated until the quasi-eignvalue converges. Once the self-consistent voltage V_{sc} is obtained and substituted to Schrödinger equation, the new wave function $\Psi(z)$ and the transmission coefficient ($T(E_z)$)

can be recalculated accordingly. The current density J_T can be evaluated by the well-known Tsu-Esaki Equation 2.45 [90] [59] [91].

$$J_T = \frac{emk_BT}{2\pi^2\hbar^3}\int_0^\infty T(E_z)ln\left(\frac{1+exp(E_{f,l}-E_z)/k_BT}{1+exp(E_{f,l}-eV-E_z)/k_BT}\right)dE_z \qquad (2.45)$$

2.5.4 Simulation Results and Discussion

The RTD layer structure was investigated with this numerical model, including the effect of the barrier width while keeping the quantum well width and barrier height constant; the effect of the quantum well width while keeping the other two parameters constant; and also the impact of the barrier height on the RTD I-V characteristic. The results of these investigations are described here.

Effect of Barrier Width

Figure 2.14 shows the simulated current density as a function of bias voltage for different barrier widths of 1.2 nm, 1.4 nm and 1.6 nm. The other structure parameters such as the quantum well width (5.5 nm) and the barrier height (0.65 eV) are kept unchanged. The simulation results indicate that with the increase of the barrier width, the peak current density reduced as expected because the thicker the barriers are, the more difficult for the electrons to enter into or escape from the quantum well.

Effect of Quantum Well Width

Figure 2.15 shows the simulated current density as a function of bias voltage for different quantum well widths of 5.3 nm, 5.5 nm and 5.7 nm. The other structure parameters such as the barriers width (1.4 nm) and the barrier height (0.65 eV) are kept unchanged. It is noted that with increase of quantum well

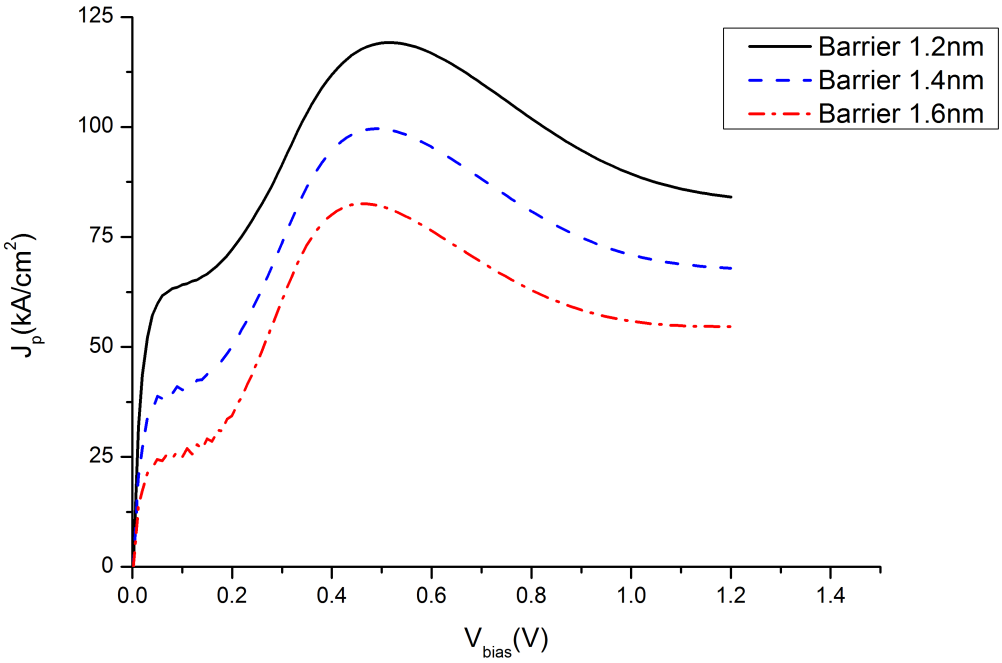


Figure 2.14: *Simulated current density as a function of bias voltage for different barriers width (*1.2 *nm,* 1.4 *nm,* 1.6 *nm). The quantum well thickness is* 5.5 *nm. The barrier height is* 0.65 *eV.*

width, the peak voltage V_p shifts to the left side. One of the reasons is probably because of the wide quantum well will push down the resonance energy level, thus the resonant tunnelling would happen at low bias voltage [92].

Effect of Barrier Height

Figure 2.16 shows the simulated current density as a function of bias voltage for different barrier height of 0.55 eV, 0.60 eV and 0.65 eV. The other structure parameters such as the barriers width (1.4 nm) and the quantum well width (5.5 nm) are kept unchanged. The high barrier height reduces the peak current density but provides high transmission coefficient benefiting large PVCR. In practice, the trade-off between large peak current density and large PVCR is achieved by

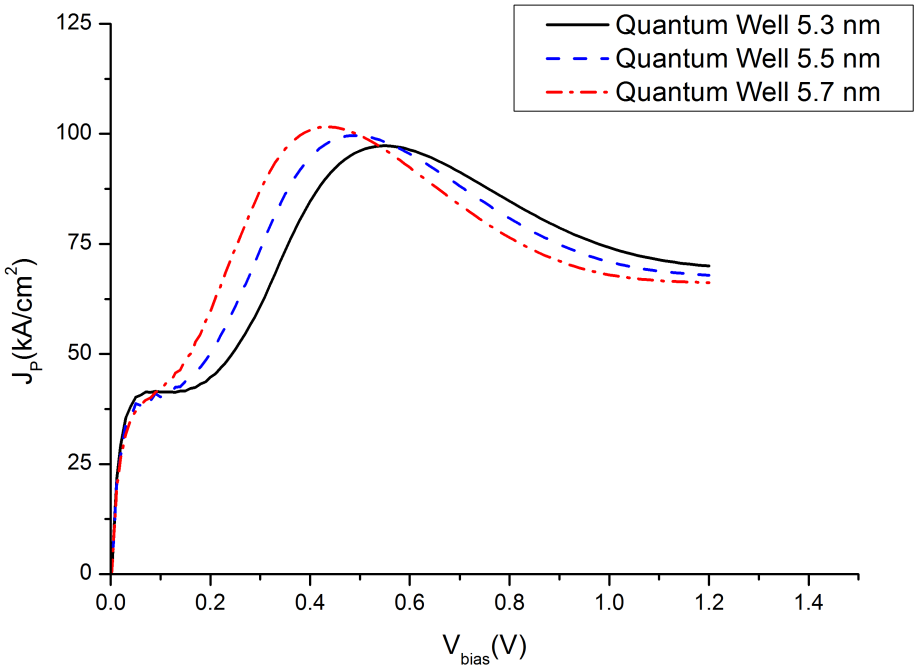


Figure 2.15: *Simulated current density as a function of bias voltage for different quantum well width (5.3 nm, 5.5 nm, 5.7 nm). The barrier thickness is 1.4 nm. The barrier height is 0.65 eV.*

adopting different band gap materials.

In summary, to achieve high peak current density, a thinner barrier width and a lower barrier height are required, but the PVCR is also reduced. With a wider quantum well, the required DC bias voltage is lower. The simulation results are consistent with the work published in [93] [94].

As the contact resistance plays an important role in the performance of an RTD, when considering the series contact resistance, the I-V equation can be expressed by

$$V_{bias} = JAR_s + V \tag{2.46}$$

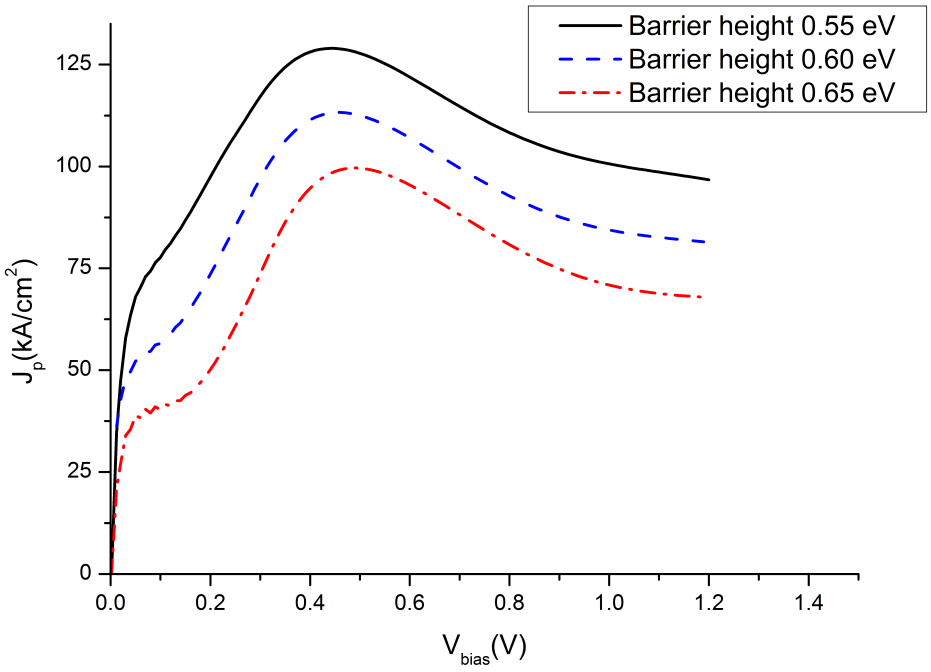


Figure 2.16: *Simulated current density as a function of bias voltage for different barrier heights (*0.55 *eV*, 0.60 *eV*, 0.65 *eV). The barrier thickness is* 1.4 *nm. The quantum well is* 5.5 *nm.*

where J is the current density, A is the RTD mesa size, and V is the voltage potential across the RTD device only. For a given InGaAs/AlAs RTD layer structure, with the barrier width $l_b = 1.4\ nm$, the quantum well thickness $l_w = 5\ nm$, the conduction band offset $U_B = 0.65\ eV$, the effective mass of InGaAs $m^* = 0.042\ m_0$. The calculated self-consistent I-V characteristics of the RTD device ($5 \times 5\ \mu m^2$) with and without a series resistance are shown in Figure 2.17. The simulation and measurement results of RTD devices fabricated on this project will be described in Chapter 6.

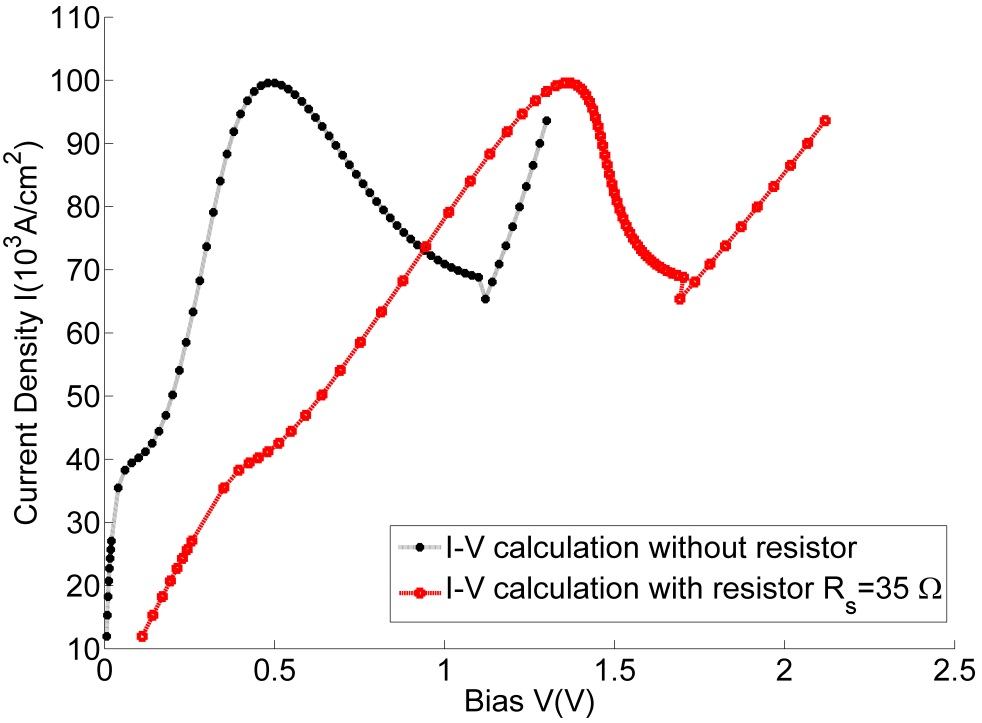


Figure 2.17: *Calculated I-V characteristics of an InGaAs/AlAs RTD (mesa size* $5 \times 5\ \mu m^2$ *) with/without considering the contact resistance.*

2.5.5 Summary

In this chapter, a self-consistent numerical model has been developed to simulate the current-voltage (I-V) characteristics of an RTD. The difference of this model to earlier work is that the convergence criteria is the quasi-eigen value (resonant energy level) instead of the transmission coefficient of electrons through the barriers [62] [64]. The model is expected to support the optimization of RTD layer structures to be employed in high power RTD oscillator design. As the resonant tunnelling- quantum mechanics are still not fully understood, a more complex model including the scattering effect [61] [95], the space-charge effect [77], etc. needs to be investigated further.

Chapter 3

Fabrication Processes and RTD MMIC Technology

3.1 Introduction

This chapter will focus on the fabrication processes required to realise RTD integrated circuits. All the fabrication was undertaken in the James Watt Nanofabrication Center (JWNC) at the University of Glasgow. The JWNC possesses clean rooms ranging from class 10,000 down to class 10, which reduces the possibility of circuit failure due to dust particles. A description of the basic fabrication process is provided in the first 4 sections, while new processes for the reliable realisation of RTD devices and integrated circuits is described thereafter. The main fabrication techniques involved are listed below

- Optical lithography
- Wet/Dry etching

- Metal Deposition
- Lift-off process

RTD devices of three different mesa sizes $3\times3\ \mu m^2$, $4\times4\ \mu m^2$, and $5\times5\ \mu m^2$ were fabricated by optical lithography because of its adequate resolution, low cost and high throughput compared to electron beam (e-beam) lithography. There are 9 optical mask layers required in total to accomplish an RTD oscillator fabrication. Mask alignment is a critical process to assure the accurate relative position of each layer superimposed. Both wet and dry etching processes were employed to pattern the devices. As an RTD is a two-terminal vertical device, wet etching is used to etch III-V semiconductor materials, while dry etching process is mainly used to open a contact via over a polymer. The polymer, polyimide PI-2545 [96], is used as a passivation layer and an insulation layer. As very few papers describe the polymer dry etching process, significant effort was devoted to develop a method for opening a via with a suitable side wall profile in the polymer to facilitate contact to the top electrode. Finally, a good lift-off process for patterning of the metallisation was also developed. The processes described in this chapter are detailed in Appendix A.

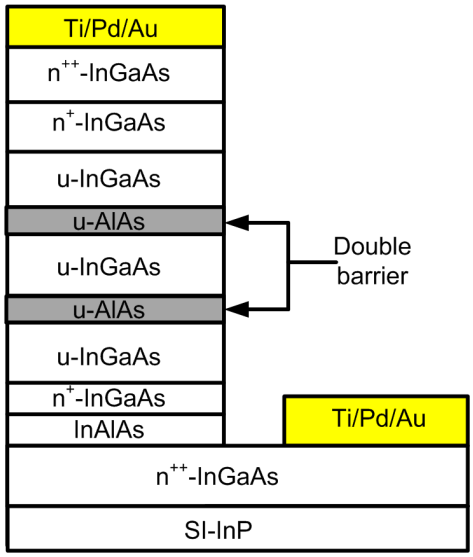
3.2 General Fabrication Steps

RTD is a two-terminal vertical transport device. The schematic structure of an RTD with information of each layer is shown in Figure 3.1. The indium gallium arsenide (InGaAs) quantum well is sandwiched between aluminium arsenide (AlAs) double barriers. On either side of the double barriers are undoped InGaAs

spacer layer, followed by lightly doped InGaAs emitter and collector layer, with highly doped InGaAs contact layers completing the device.

Layer Number	Thickness (Å)	Semiconductor Composition
1	400	$In_{0.53}Ga_{0.47}As$
2	800	$In_{0.53}Ga_{0.47}As$
3	500	$In_{0.53}Ga_{0.47}As$
4	14	AlAs
5	55	$In_{0.53}Ga_{0.47}As$
6	14	AlAs
7	500	$In_{0.53}Ga_{0.47}As$
8	800	$In_{0.53}Ga_{0.47}As$
9	100	$In_{0.52}Al_{0.48}As$
10	2000	$In_{0.53}Ga_{0.47}As$
11	2000	$In_{0.53}Ga_{0.47}As$
12	635 (um)	SI : InP

(a)



(b)

Figure 3.1: *The schematic layer structure of an RTD device (b) with layer information (a).*

The fabrication flow diagram for a device is illustrated in Figure 3.2. At the beginning, contact metal layers (Ti (20 nm)/Pd (30 nm)/Au (80 nm)) are deposited on top of the emitter contact layer (n^{++} InGaAs) as shown in Figure 3.2(a). The inset diagram shows the thin double barriers (AlAs)/quantum well (InGaAs) layer structure. Then an acid solvent (H_3PO_4:H_2O_2:H_2O=1:1:38) is used to etch down to the collector contact layer as shown in Figure 3.2(b). After wet etching, collector metal is deposited as shown in Figure 3.2(c). Wet etching again of the InGaAs contact and buffer layers is done to expose the substrate (InP) as shown in Figure 3.2(d). This step isolates the individual RTD devices and exposes the substrate for the deposition/realization of the required passive structures. The passivation layer, the polyimide PI-2545, is deposited by spinning

and a via is opened by dry etching over the polymer as shown in Figure 3.2(e). The final step (Figure 3.2(f)) is to deposit the metal contact pad (Ti/Pd/Au, 20 nm/30 nm/80 nm). Now the single RTD device fabrication is completed. There are 9 optical mask layers in total: emitter layer; etching protection layer; collector layer; etching protection layer; via opening layer; bond pad layer; resistor pattern layer; capacitor pattern layer; and finally the top contact pad layer. As the oscillator circuit also needs passive components such as capacitors and resistors, extra fabrication steps are taken to accomplish the circuit. These will be described later in section 4.8.

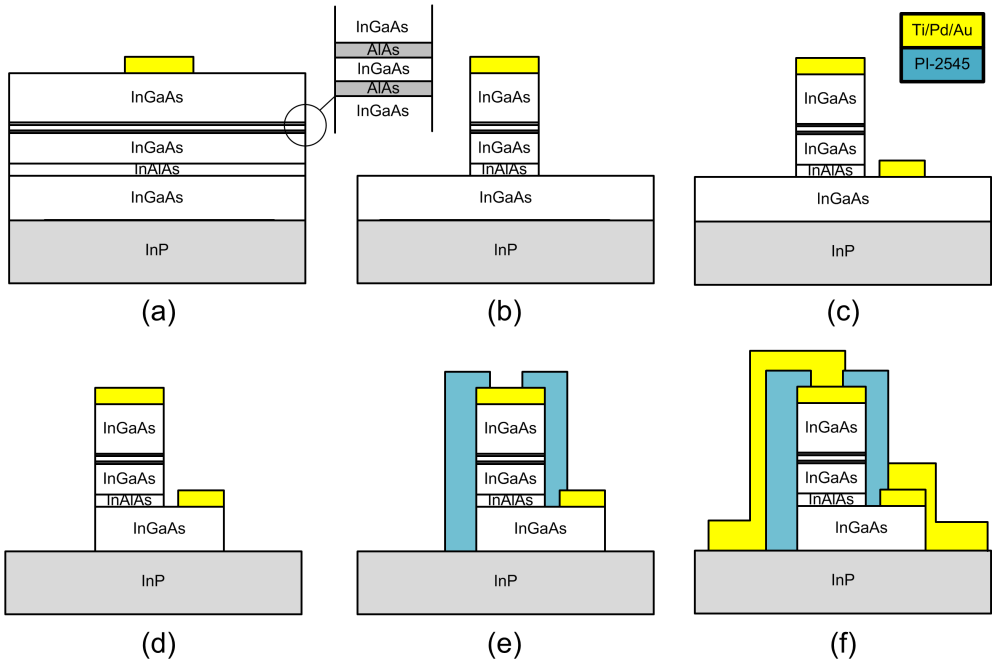


Figure 3.2: *A single RTD device fabrication flow diagram: (a) Pattern emitter metal contact. (b) Wet etch to collector layer. (c) Pattern collector metal contact. (d) Wet etch to substrate (InP). (e) Deposit polymer (PI-2545) and open a via by dry etching. (f) Pattern bond metal pads.*

3.2.1 Optical Lithography

Lithography is a complicated and critical process in microelectronic integrated circuit fabrication [97–99]. Among all the lithography techniques such as electron beam (E-beam) lithography, extreme ultraviolet (EUV) lithography, X-ray lithography (XRL), and ion beam lithography, etc, optical lithography is the most commonly used technique because of its high throughput, low cost and ease of operation [97]. Optical lithography involves projecting ultra-violet (UV) light (wavelength $\lambda \cong 0.2 - 0.4\ \mu m$) through an optical mask to expose the light-sensitive photoresist underneath the mask. After developing, various patterns on the mask are transferred to the photoresist which is spun on the wafer surface. These patterns define the different components of the integrated circuit (IC) such as the electrode contact, the bond pad, the via window, etc. The performance of the exposure tool is determined by three parameters: resolution, which is the minimum dimension that can be transferred from a mask to the photo resist; registration, which is a criterion of how accurately patterns on successive masks can be aligned; and throughput, which is the number of wafers that can be processed per hour for a given mask. Compared with E-beam lithography, which is preferable for sub-micron fabrication, optical lithography has high throughput, however the resolution and registration are limited due to light wave diffraction. The best resolution achievable with the Karl Suss MA6 mask aligner used in this project and with an UV source of wavelength $\lambda = 365\ nm$ is $0.5\ \mu m$. As the minimum device size is $3 \times 3\ \mu m^2$, optical lithography technique was capable to satisfy the resolution requirement. When designing a THz RTD oscillator with oscillation frequency over 300 GHz, the mesa size of an RTD that is required will

shrink down to sub-micrometer dimensions to minimize the device capacitance. In such a case, electron-beam (e-beam) lithography [100] or recently developed soft-reflow technique [101] would be required.

3.2.1.1 Sample Preparation

The RTD epi-material was grown on a 3 inch wafer by IQE Ltd using molecular beam epitaxy (MBE). At the start of fabrication process, the 3 inch wafer needs to be cleaved into approximately 1 $cm \times 1$ cm square samples. Before cleaving, both sides of the wafer are covered with thin photoresist to protect it from scratches and contamination. As dust particles adhering to the photo mask or the sample surface may lead to circuit failure, it is essential to keep both the mask plate and the sample clean all the time. The cleaning process includes an ultrasonic bath in acetone ($(CH_3)_2CO$), methanol (CH_3OH) and isopropyl alcohol (IPA) to remove the contaminants chemically and physically. It has to be pointed out that because both sides of the InP wafer are polished, it is necessary to identify on which side the epitaxy layers are grown by measuring the resistance of the surface before fabrication actually starts. The measured resistance of the semi-insulating substrate is usually very high, mega-Ohms, while that of the highly doped n-type InGaAs cap layer is usually tens of Ohms.

3.2.1.2 Optical Mask

The optical mask is made of a fused-silica substrate covered with a chromium (Cr) metal layer. A thin electron-sensitized polymer is spun on top before the designed patterns are written by electron beam exposure. After developing and etching, the photo mask patterns are transferred from an initial design to the

mask. In this project, these patterns which define each component of the oscillator were designed by L-Edit software (Tanner Research, Inc.) [102]. Figure 3.3 shows the finalised layout of a completed mask design showing the layouts of various devices, components and circuits. There are nine different layers in total and each layer was placed on the mask plate successively representing the fabrication flow, as shown in Figure 3.3(b).

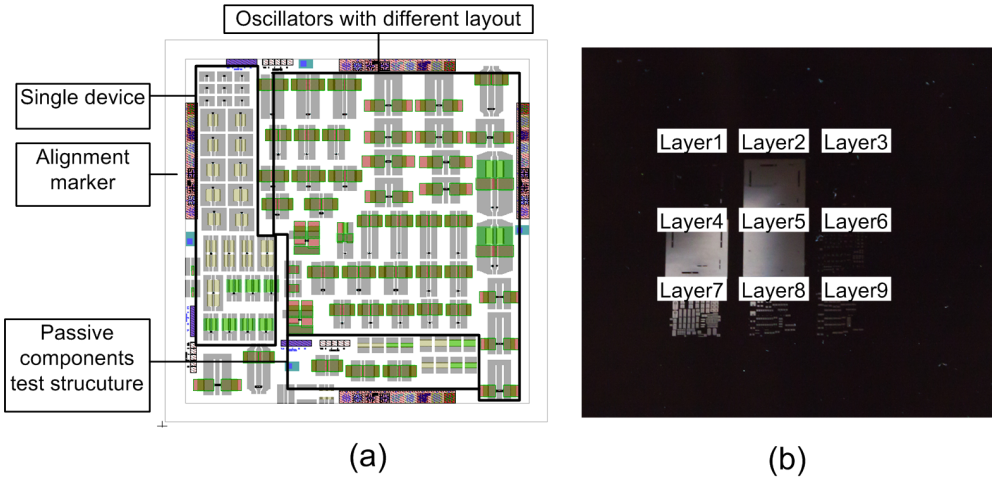


Figure 3.3: *Optical Mask for RTD oscillators. (a)Mask layout designed by L-Edit software. 9 different layers are superimposed on each other.(b)Finished mask plate with 9 layers placed sequentially.*

3.2.1.3 Photoresist

Photoresist is a photosensitive material used to transfer a pattern from the mask to wafer. These materials play a critical role in photo-lithography. Depending on the polarity, the photoresist can be divided into two categories: positive and negative. With positive photoresists, the exposed region dissolves more quickly during the developing process while the unexposed region remains almost unchanged on the surface. Negative photoresists behave in an opposite manner.

Generally the resolution of positive resist is better than negative resist. Therefore they are more widely used in IC fabrication. Negative photoresist adheres well to the wafer without pretreatment, however the primary disadvantage of negative photoresists is their swelling action, which will broaden the line-width during development [97]. As a result, negative resists are normally not suitable for features with dimensions less than 2.0 μm. The photoresists used in this project were the S1805 and the S1818, positive photoresist from Shipley Europe Ltd. The difference between these two photoresists are the spin-thickness. As shown in Figure 3.4, when the spin speed is 4000 rpm, the thickness of S1805 is about 0.5 μm while S1818 is about 2 μm. When a photoresist acts as a sacrificial layer in the lift-off process, its profile plays an important role. The thickness of photoresist is chosen according to the different metal thickness to be deposited.

3.2.2 Metallisation and Lift-off

The metal contact of the device was accomplished by metallisation and lift off processes. The technique used to deposit thin film metal is electron-beam physical vapor deposition (EBPVD), in which the target component (anode) is bombarded with an electron beam emitting from the heated source metal (cathode) under a high vacuum environment [104]. Atoms of the source metal evaporate into the target sample forming a thin solid film layer. As the atoms travel in a straight line, EBPVD provides poor side wall coverage which benefits the lift-off application but could compromise the contact continuity. One method to improve the step coverage is to rotate the wafer while evaporating. The EBPVD equipment used in this project was a Plassys MEB 550S (Plassys II) system. The available met-

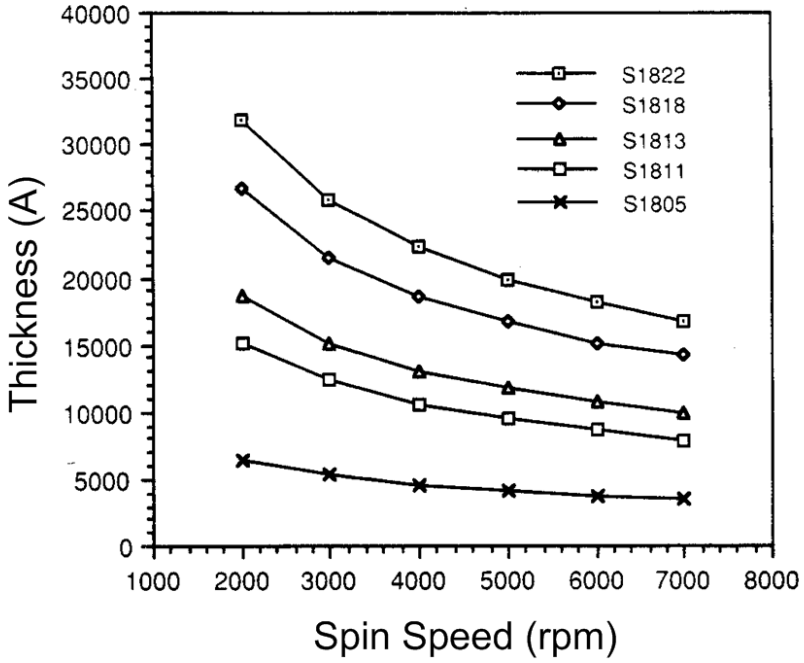


Figure 3.4: *S1800 series photoresist spin speed curves [103].*

als are gold (Au), germanium (Ge), platinum (Pt), aluminium (Al), nickel (Ni), Nickel-Chromium (NiCr) and Molybdenum (Mo). For n-doped InGaAs, the optimized contact metal scheme is Ti/Pd/Au (20 nm/30 nm/80 nm) [76] [105] [106]. Very low specific contact resistance ($0.73 \pm 0.44\ \Omega\mu m^2$) can be obtained by using this metal alloy [76]. The ohmic metal contact schemes to n-type InGaAs are summarized in Table 3.1

Table 3.1: *Summary of ohmic contact to n-type InGaAs*

Metallization	Anneal	Temp(°C)	InGaAs Cap Doping (cm^{-3})	ρ_C ($\Omega\mu m^2$)	Reference
Ti/Pt/Au	yes	150-300	$10^{18} - 10^{20}$	20-50	[107–110]
Ni/Ge/Au	yes	150-300	$10^{18} - 10^{20}$	40-100	[107]
Ti/Pd/Au	no	N/A	$10^{18} - 10^{20}$	0.73-3.2	[76, 106]
Ti/Pd/Au	yes	350-400	$10^{18} - 10^{20}$	4.6-25	[105, 106]
Ti/Ni/Au	yes	250	10^{18}	300	[110]

Increased doping level, optimized surface treatment (de-oxidization by using NH_4OH [76] [105] or HCL [106]) and favourable contact alloy selection will reduce the specific contact resistance of contacts to n-InGaAs. In this project the specific contact resistance was measured by transmission line model (TLM) technique, the details will be given in Chapter 4.

After the contact metal is deposited, the following step is to lift-off the unwanted thin film metal by dissolving the photoresist in an appropriate solvent, such as 50°C warm acetone. The thickness of the photoresist must be greater than the thickness of metal to form the discontinuity in order to allow acetone to dissolve the underlying photoresist for a good lift-off process. After developing, an undercut profile of the photoresist is preferred. To ensure a good lift-off process, there are two strategies that can be employed. One of the strategies is to use a single layer lift-off process when the thickness of metal is around 100 nm. In this process, the sample is soaked in Chlorobenzene(C_6H_5Cl) for a couple of minutes prior to exposure to alter the solubility of the photoresist. Because of the different dissolving rates between the soaked and unsoaked parts of the resist, an undercut is formed. Performing a good lift-off depends on the thickness of the top lip and the slope of the photoresist wall under the lip [111]. The process is illustrated in Figure 3.5.

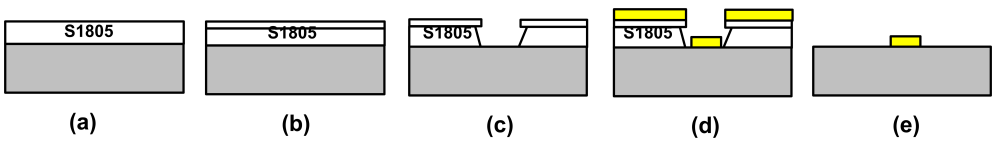


Figure 3.5: *Single layer lift off process: (a) Coat and prebake photoresist on the sample (b) Soak in Chlorobenzene(C_6H_5Cl) (c) Expose and develop the photoresist. Due to different dissolving rates, an overhang profile is ensured (d) Metallisation (e) Lift off.*

The other strategy is called dual layer lift-off process using Lift-Off Resist (LOR) in combination with photoresist. The process is illustrated in Figure 3.6. Before coating the photoresist, a thin layer LOR is spun on the sample surface as a sacrificial layer. After exposure and development, due to different dissolution rates, an overhang profile forms as illustrated in Figure 3.6(d) to assure a good lift-off.

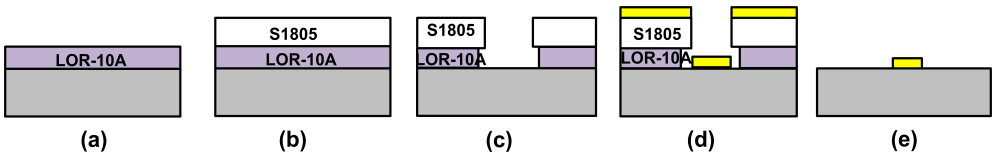


Figure 3.6: *Dual layer lift off process:(a) Coat and prebake LOR-10A (b) Coat and prebake photoresist over LOR-10A (c) Expose and develop both photoresist and LOR-10A (d) Metallisation. The re-entrant profile ensures film discontinuity (e) Lift off.*

The two lift-off recipes were assessed for their suitability in realising RTD integrated circuits. Figure 3.7 shows the metal edge profile for single and dual layer lift-off processes for thick metal deposition. It is noticeable in Figure 3.7(a) that when 200 nm thick Aluminium was deposited, it partially covered the side walls of the resist. After lift-off, the metal along the side walls stands upwards from the surface resulting in poor contact with other overlapped metal layers or the metal may peal off in subsequent processes, resulting in unexpected short circuits. In Figure 3.7(b), 500 nm thick Aluminium was deposited and lifted off by the dual layer (LOR/S1818) technique. This indicates a good metal contact without edge problems.

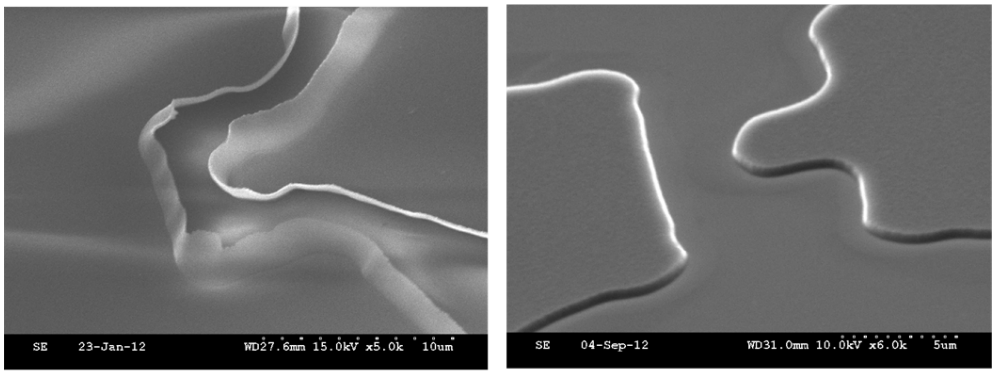


Figure 3.7: *Metal edge profile comparison between single and dual layer lift off. (a) Single-layer (S1818) lift-off. After coating S1818, the sample was soaked in chlorobenzene for 8 minutes. The thickness of Al deposited was 200 nm. (b) Dual-layer(LOR10A/S1818) lift-off. After coating and pre-baking LOR10A, photoresist S1818 was spun and pre-baked. After exposure and development, the thickness of Al deposited was 500 nm.*

3.2.3 Dielectric Deposition

Dielectric films are deposited for the purpose of insulating or passivating devices. Unlike physically based methods for depositing thin metallic films such as EBPVD, Chemical Vapor Deposition (CVD) is a chemical process to deposit various dielectric materials such as silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) by using a chemical reaction among gaseous compounds. Inductively Coupled CVD (ICP-CVD) is one of the CVD techniques commonly used to deposit high quality Si_3N_4 at room temperature. Low deposition temperature, low compressive stress and good electrical characteristics, including high breakdown voltage and low leakage current, make ICP-CVD the preferable technique for Metal-Insulator-Metal (MIM) capacitor fabrication [97]. The equipment utilized in the project was System 100 ICP-CVD from Oxford Instruments. This high density plasma tool is mainly used to deposit low stress Si_3N_4 with thickness from 5 nm up to hundreds

of nanometres with a breakdown voltage greater than 4×10^6 V/cm [112].

3.2.4 Wet Etching and Dry Etching

Patterns, which are transferred from the optical mask to the photoresist by optical lithography, must be transferred to the semiconductor to complete the device. This process is accomplished by wet or dry etching. Wet etching makes use of a chemical solvent, which is usually a diluted acid such as H_3PO_4/HCL/HF, to react with the etching material while dry etching, Reactive Ion Etching (RIE), involves two mechanisms. One is physical reaction, where accelerated gas ions bombard the material surface physically. The other mechanism is chemical reaction, where energetic ions react with the exposed material. Compared with dry etching, the advantages of wet etching are low cost, low surface damage and high selectivity. However, the biggest disadvantage is that the wet etching is isotropic (actually depends on crystal orientation). Therefore some of the semiconductor underneath the contact is etched, causing an undercut, at the same time as the exposed semiconductor material is etched down. The undercut due to wet etching is severe when the aspect ratio of the feature is high. The undercut profile will reduce the effective device size, degrade the device performance, or even worse lead to device failure. Therefore, the etching rate of the wet etch process has to be investigated carefully. In this project, both wet and dry etching were involved. Wet etching was mainly used to pattern the semiconductor material, which is InGaAs in this case. The chosen solvent was H_3PO_4:H_2O_2:H_2O=1:1:38 which will not attack the substrate InP. Thus the etching selectivity is high. The measured etching rate of InGaAs at room temperature was about 110 nm/min. Figure 3.8

shows a fabricated $4 \times 4\ \mu m^2$ device after wet etching.

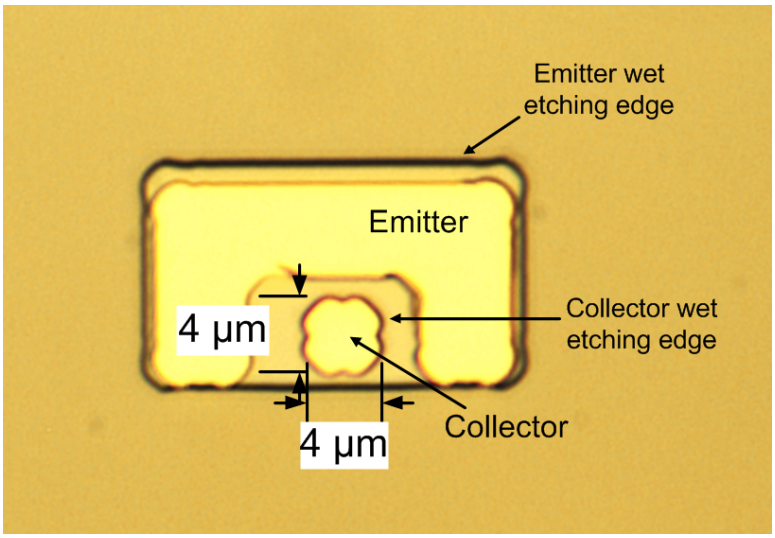


Figure 3.8: *The micrograph of an RTD device after wet etching. The central mesa size is about* $4 \times 4\ \mu m^2$.

If the main consideration is resolution and vertical sidewalls, a dry etching process is preferred. Dry etching technique is suitable for III-V semiconductor materials and various polymers. For instance, InGaAs can be etched by Methane/Hydrogen (CH_4/H_2) gas [38] [113]. As the dimensions of the RTD in this project are in micrometers large, the dry etching technique for InGaAs was not implemented.

3.3 Process Module Development

On this project, a new process to open up a via in polyimide and so enable a contact to the top electrode was required. The polyimide (PI-2545) from HD MicroSystem was employed to passivate the mesa side wall and also to provide isolation between the emitter and collector metal contacts. PI-2545 is widely

used as a dielectric interlayer and passivation layer because of its low dielectric constant ($\epsilon_r = 3.3$), thermal stability (up to 500 °C), low cost, tapered via profile and compatibility with the photo-lithography process [96].

3.3.1 Via Opening Process

A via hole is required through PI-2545 to enable the connection between the top device contact and the bond pads. Via opening is the critical process in the RTD fabrication process. Specifically the process requires a 2×2 μm^2 via hole over a 3×3 μm^2 mesa. Other via sizes were 2.5×2.5 μm^2 and 3×3 μm^2 for the 4×4 μm^2 and 5×5 μm^2 mesa size. Accurate mask alignment and precise control of dry etching parameters are crucial. Misalignment and over/under etching will lead to device failure.

To avoid high aspect ratio (the ratio of the depth of the hole to the diameter of the hole), the thickness of PI-2545 was considered. The spin speed curve of PI-2545 is given in Ref. [96] and is repeated here as shown in Figure 3.9 for reference. The mesa height from the top metal contact to the substrate was about 838 nm. The thickness of PI-2545 was chosen accordingly to avoid a too high aspect ratio for the via hole. In this case, when the spin speed was 8000 rpm, the measured thickness of PI-2545 was about 1.2 μm. A description of different processes to open a via in the polyimide now follows.

PI-2545 Wet Etch The polyimide PI-2545 were patterned by using positive photoresist (S1805) as a mask, and the etching was done using 2.38% TMAH (0.26N) developer [96]. Figure 3.10 shows micrographs of the via hole in polyimide for 3 mesa sizes and so 3 via sizes. After wet etching, the vias are significantly

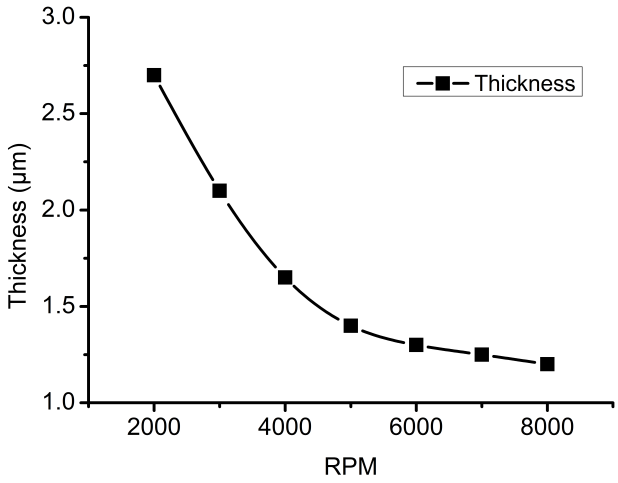


Figure 3.9: *Spin speed/thickness curve for PI-2545 [96].*

smaller than designed and are not fully opened. This approach was therefore unsuitable for RTD fabrication.

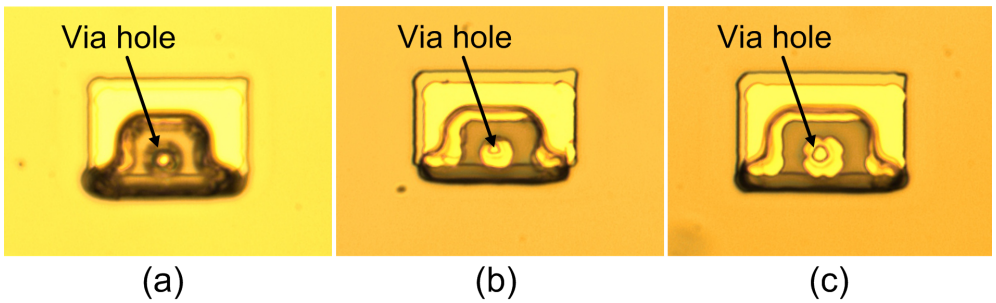


Figure 3.10: *The micrograph of PI-2545 via opening process developed by wet etching. (a) The central contact pads size is* 3×3 μm^2 *while the via size is* 2×2 μm^2*. (b) The central contact pads size is* 4×4 μm^2 *while the via size is* 2.5×2.5 μm^2*. (c) The central contact pads size is* 5×5 μm^2 *while the via size is* 3×3 μm^2*.*

PI-2545 Dry Etch with hard mask (Aluminium)

As the PI-2545 wet etching process was found not to be suitable, a dry etching process was therefore investigated. There are several essential factors to be considered when using the dry etching technique. The first is the polyimide

dry etching gases. The second is the etching mask chosen. Polyimide etching rates and edge profiles with various etching gas composition are described in Ref. [114]. It was found that the concentration of CF_4:O_2 = 1:20 showed a via profile tapered around 45°, which was ideal for a good step coverage. The same gas composition was adopted in this project, but etching using only O_2 plasma was also tested. The difference will be compared later in this section. Both hard mask (Aluminum) and soft mask (S1805 photoresist) process were employed and compared. Aluminium (Al) was first chosen as the etching mask because of the ease of deposition and removal, and also its compatible with photo lithography technique. The process is listed below:

- Preparation of PI-2545 (details in appendix A)
- Deposit Al (75 nm)
- Patten the S1805 photoresist by photo lithography
- Wet etch Al (H_3PO_4:HNO_3:CH_3COOH:H_2O=80:5:5:10)
- PI-2545 dry-etch using O_2 for 20 minutes
- Strip off Al by using the developer MF-319 for 3 minutes

After following the above fabricating steps, the micrographs of the fabricated device are shown in Figure 3.11. The sharp and straight side wall can be noticed in Figure 3.11(a), which led to a broken circuit after bond pads deposition. This can be seen in Figure 3.11(b).

PI-2545 Dry Etch with soft mask (S1805)

To obtain a smooth slope profile of the PI-2545, the CF_4:O_2 = 1:20 dry etching gas was utilized and the S1805 photoresist was employed as the etching mask. The

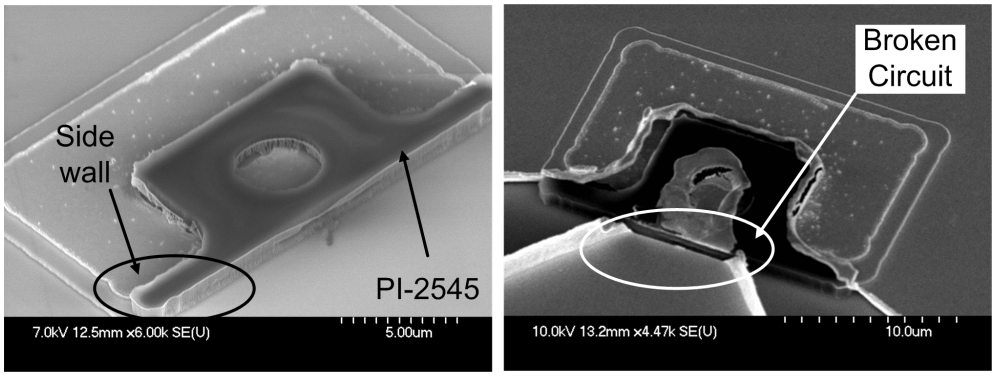


Figure 3.11: *The micrographs of PI-2545 via opening process developed by O_2 plasma dry etching. 75 nm Al was used as etching mask. (a) The after etching profile of PI-2545. The sharp and straight side wall is noticed. (b) After depositing metal bond pads Ti/Pt/Au (15 nm/15 nm/200 nm), the circuit is broken at the edge.*

measured dry etching rate was about 240 nm/min for PI-2545, and 170 nm/min for S1805 photoresist. To ensure etching down 1.2 μm thick PI-2545 (5 minutes etching time), the required thickness of S1805 was 850 nm. According to the spin curve of S1805 shown in Figure 3.4, the required spin speed was around 1500 rpm (0.9 μm). After S1805 was patterned through standard photo lithography process, hard bake was applied at 115°C for 10 minutes to smooth the edge of S1805 for the purpose of a well tapered via hole profile. The profile changes of S1805 with and without hard bake is illustrated in Figure 3.12. Figure 3.12 (a) and (b) show the resist profiles with and without hard baking of the photoresist, respectively. Figure 3.12 (c) and (d) are scanning electron microscope (SEM)images of parts of fabricated devices showing the polyimide profile for the two cases.

Figure 3.13 shows SEM images of fabricated RTD devices with different polyimide edge profiles for the cases of hard baking the photoresist mask and not doing so. After a via is opened by CF_4/O_2 plasma dry etching , metal contact pads were deposited over the via. It is clear that the step coverage is much bet-

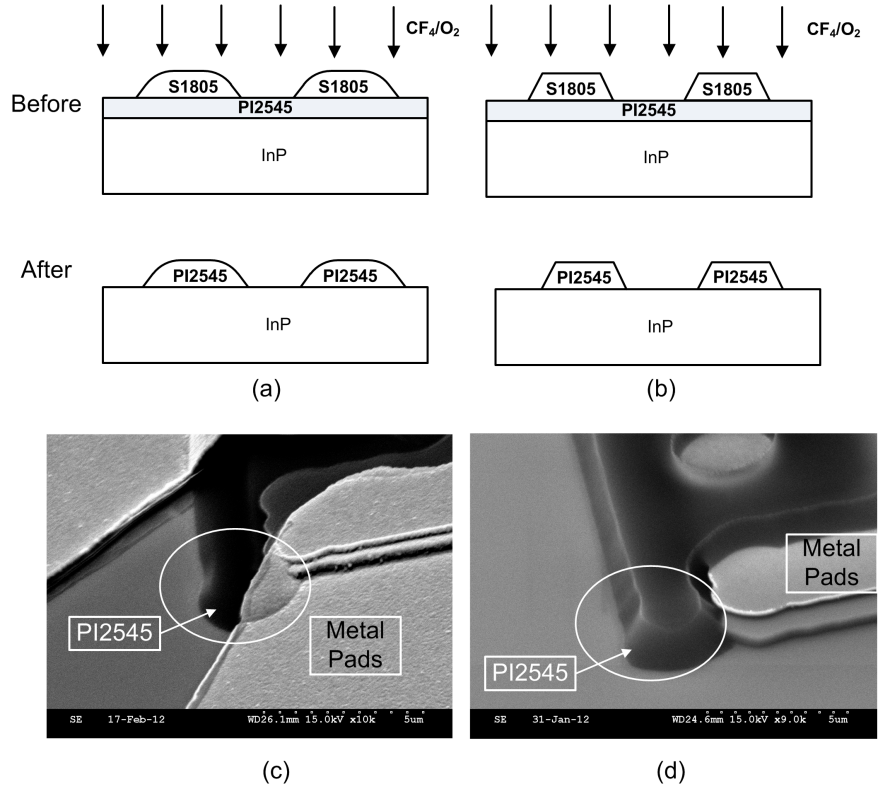


Figure 3.12: *S1805 profile comparison with and without hard bake (*115°C*). The profile of PI-2545 was also affected by the mask (S1805). (a) Smooth edge profile due to hard bake. (b) Sharp edge profile without hard bake. The SEM pictures of PI-2545 after dry etching (c) with hard bake. (d) without hard bake.*

ter in Figure 3.13(b) than that in Figure 3.13(a), i.e. after hard baking of the photoresist and not doing so, respectively. Therefore with a hard bake process the edge profile of PI-2545 is much smoother which benefits the step coverage.

Figure 3.14 shows SEM micrographs of the fabricated via hole after O_2 plasma dry etching. It shows well defined profile of the polyimide, including tapered side wall and clearly opened vias.

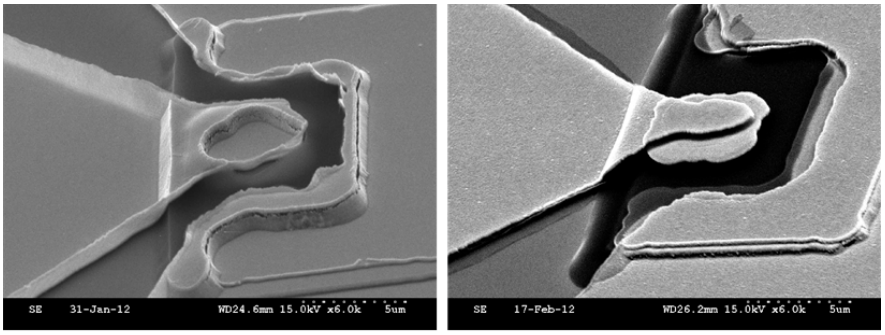


Figure 3.13: *SEM pictures of the fabricated devices with different polyimide edge profile (PI-2545). (a) Without hard bake, the edge of PI-2545 is sharp. The crack is noticed on the metal contact, which will lead to circuit failure. (b) With hard bake (*115°C*), the edge of PI-2545 is smooth. Good metal contact is obtained.*

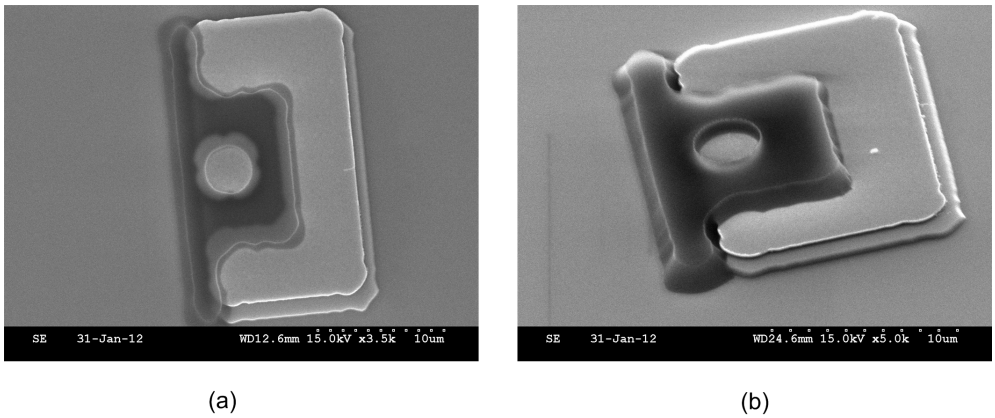


Figure 3.14: *SEM pictures of* $3 \times 3\ \mu m^2$ *via opening over* $5 \times 5\ \mu m^2$ *metal contact in the centre. (a) Top-view. (b) Side-view.*

3.3.2 Fabricated RTD Devices

The process modules described in the preceding sections were used to fabricate RTD devices. Following the steps as illustrated in Figure 3.2, SEM micrographs of the fabricated single RTD device are shown in Figure 3.15. There were 19 single RTD devices fabricated on the same wafer in total, and 17 of them exhibited consistent I-V characteristics. It was found that the yield of this fabrication process was as high as 90%. Measured device characteristics and an evaluation

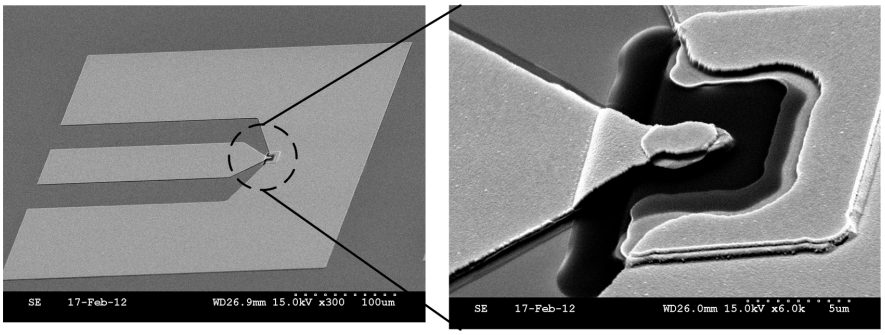


Figure 3.15: *SEM pictures of the fabricated RTD device. (a) The overview of the device. The central area is magnified and shown in (b). The mesa size is* $3 \times 3\ \mu m^2$*. Good contacts between bond pads and electrodes are observed.*

of these is described in Chapter 6.

3.4 RTD Oscillator MMIC Processes

To realize an oscillator, passive components are required in addition to the RTD device. These include thin film resistors, metal-insulator-metal (MIM) capacitors and coplanar waveguides. The RTD oscillator MMIC fabrication process is illustrated in Figure 3.16. After following the fabrication process illustrated in Figure 3.2(a)∼(e) for individual RTD devices and before patterning the contacts to device electrodes as shown in Figure 3.2(f), the nichrome (NiCr) film resistor is first deposited on the InP substrate (Figure 3.16(b)), and then the emitter metal is deposited as shown in Figure 3.16(c). This metal layer also acts as the bottom contact for the MIM capacitor. The next step is to deposit the insulator (Si_3N_4) by ICP-CVD (Figure 3.16(d)). The final step is to deposit the collector metal contact and also the top metal contact of MIM capacitor as shown in Figure 3.16(e). This step is also used to realise the required coplanar waveguides. The

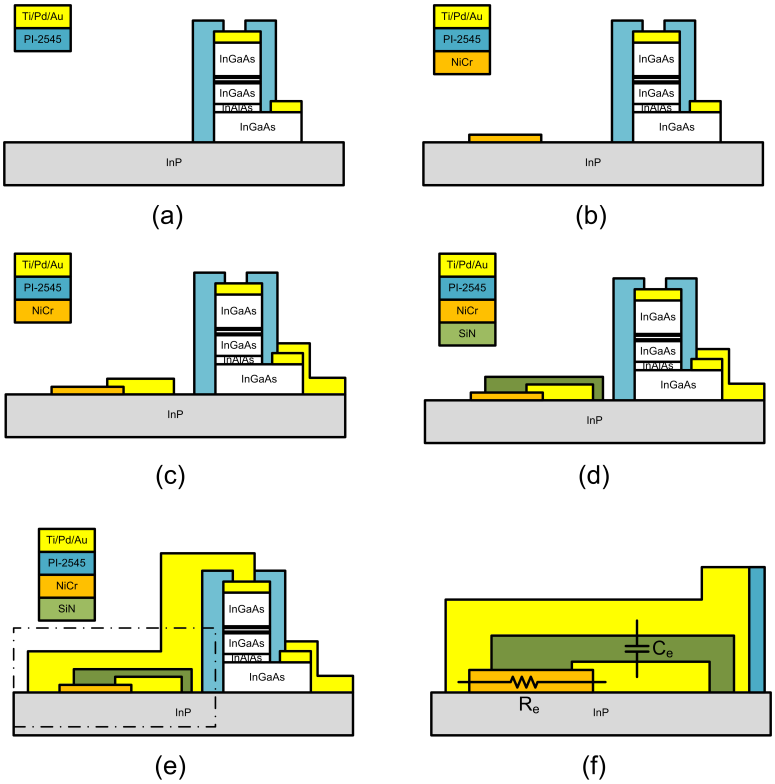


Figure 3.16: *MMIC RTD oscillator fabrication flow diagram: (a) Fabricated RTD device by flowing the process shown in Figure 3.2. (b) Deposit NiCr resistor. (c) Pattern emitter metal contact and also the MIM capacitor bottom contact. (d) Deposit SiN as MIM capacitor insulator. (e) Pattern collector metal contact and also the MIM capacitor top contact. (f) The overlapped shunt resistor (R_e) and MIM capacitor (C_e) are illustrated with its circuit symbol.*

metal scheme is Ti/Au (20 nm/380 nm). The overlapped NiCr resistor and MIM capacitor is illustrated by its circuit model as shown in Figure 3.16(f). Chapter 4 will describe the design and characterization of the passive components.

The fabricated oscillator circuits including by-pass capacitors (C_e) and shunt resistors (R_e) are shown in Figure 3.17. Two different oscillator layouts are displayed. Details about these circuits including their electrical performance will be described in Chapter 6.

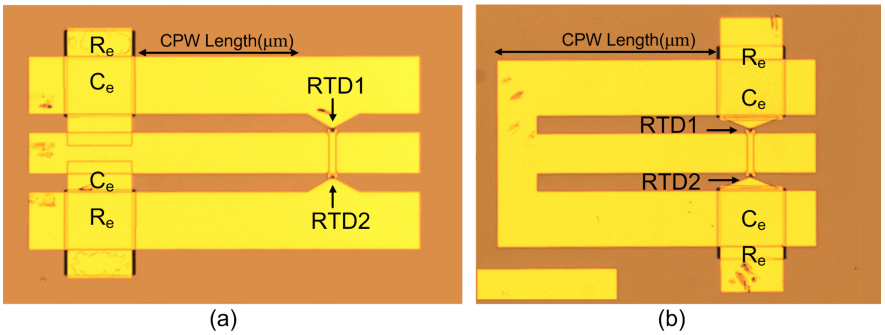


Figure 3.17: *MMIC RTD oscillator circuits with two different layouts. Both employ 2 RTD devices in parallel. Each RTD device is biased individually with its own stabilizing circuit. Locations of the integrated resistors (R_e) and capacitors (C_e) are also shown.*

3.5 Summary

In this chapter, the fabrication processes for RTD devices and integrated circuits have been described. The whole process involves 9 optical lithography steps, 2 wet etching steps and 1 dry etching step. The minimum mesa size processed was $3 \times 3\ \mu m^2$. For the lift-off process used in metallisation, two strategies were considered. The dual layer lift-off process proved to be an effective process for thick metal lift-off. The via opening process is the most vital and difficult process. Both wet and dry etching, hard and soft mask via opening process were tested. The PI-2545 wet etching process showed poor results. For PI-2545 dry-etch process, several factors including the etching mask, gas composition, the sample preparation, the thickness of PI-2545 and S1805, etc. were considered and tested. Over- or under-etching of the polyimide would lead to device failure. A reliable via etching process in the PI-2545 polyimide was developed. Using the developed process modules, the MMIC RTD oscillator fabrication processes were developed and optimized. The specific process details are provided in Appendix A. The processes were used to realize RTD devices and oscillators successfully.

Chapter 4

Passive Components and Ohmic Contacts

4.1 Introduction

In the earlier chapters, the characteristics of the active device, RTD, and its fabrication process were described. As noted in Chapter 3, to realise an oscillator, passive components are also required. In this project, these components included:

- Coplanar waveguide (CPW): 50Ω CPW transmission line on an InP substrate and shorted CPW structure as a part of an oscillator resonator,
- Metal-insulator-metal (MIM) capacitor in series and in parallel configuration as DC-blocking and RF-decoupling circuit, respectively, and
- Thin film nichrome (NiCr) resistor.

In this chapter, the design procedure and characterization of these components are described. As the series ohmic contact resistance of an RTD device plays an

important role in the performance of an RTD oscillator, the characterization of these ohmic contacts is also included in this chapter.

4.2 Design of Passive Components

4.2.1 Coplanar Waveguide (CPW)

Coplanar waveguide (CPW) was first demonstrated by C.P. Wen in 1969 [115]. Since then, tremendous research has been devoted to its development. A conventional CPW consists of a central strip conductor located between two finite width ground planes, as shown in Figure 4.1, where w, s, g, l and t are the CPW signal line width, the gap distance between the signal line and the ground plane, the ground plane width, the CPW length and the thickness of the CPW conductor, respectively. The dielectric constant and the thickness of the substrate are denoted as ε_r and h. The unique features of CPW are listed as follows [116] :

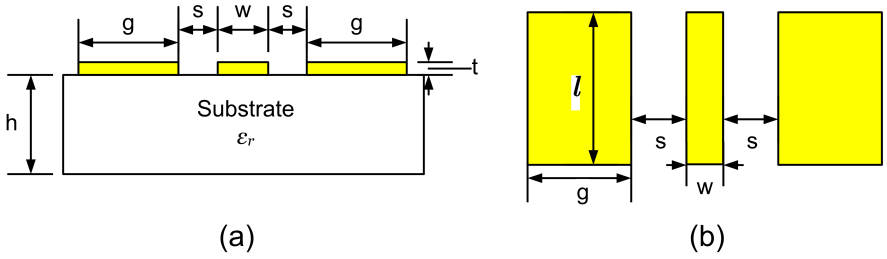


Figure 4.1: *A CPW structure on a substrate with dielectric constant ε_r and thickness h. The signal line width is w, the gap between the signal line and ground plane is s, the width of ground plane is g, the thickness of the conductor is t and the length of the CPW is denoted as l. (a) Cross section view. (b)Top view.*

- Compatible with MMIC techniques as all the conductors are on the same side of the substrate

- Facilitates shunt/series surface mounting of active/passive devices
- Easily engineered characteristic impedance by changing the geometry of conductors
- Simplifies the fabrication process, of which only one mask layer is required for photo-lithography

The closed-form equations for effective dielectric constant ε_{eff} and characteristic impedance Z_0 of a finite ground CPW (FG-CPW) on a finite substrate are given by [117]

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{eff}}} \frac{K(k_1')}{K(k_1)} \tag{4.1}$$

$$\varepsilon_{eff} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K(k_1')K(k_2)}{K(k_1)K(k_2')} \tag{4.2}$$

where $K(k_{1,2})$ represents a complete elliptic function, and

$$k_1 = \frac{w}{w+2s} \sqrt{\frac{g(w+2s+g)}{(s+g)(w+s+g)}} \tag{4.3}$$

$$k_2 = \frac{sinh(\pi w/4h)}{sinh[\pi(w+2s)/4h]} A \tag{4.4}$$

$$k_{1,2}' = \sqrt{1-k_{1,2}^2} \tag{4.5}$$

$$A = \sqrt{\frac{1 - sinh^2[\pi(w+2s)/4h]/sinh^2[(\pi(w+2s+2g)/4h])}{1 - sinh^2(\pi w/4h)/sinh^2[\pi(w+2s+2g)/4h]}} \tag{4.6}$$

Normally the thickness of the conductor t is three times the skin depth δ to reduce the attenuation [116]. For example, the gold resistivity $\rho_{Au} = 2.44 \times$

$10^{-8}\ \Omega m$, the vacuum permeability $\mu_0 = 4\pi \times 10^{-7}\ H/m$, the relative permeability $\mu_r = 1$, at frequency f =100 GHz, the skin depth (δ) is

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}} = 248.6\ nm \cong 0.25\ \mu m \tag{4.7}$$

Thus the conductor thickness should satisfy $t > 3\delta = 745.8\ nm$. The skin depth is inversely proportional to the square root of frequency. In practice, the width of the ground plane g should be at least two times the centre strip width w to reduce the radiation loss introduced by a narrow ground plane [118] [119].

In this project, a computer aided design (CAD) software used to calculate the dimensions of CPW was "LineCalc" tool embedded in Advanced Design System (ADS) software from Agilent Technologies. LineCalc is an analysis and synthesis program for calculating electrical and physical parameters of transmission lines [120], such as microstrip, coupled microstrip, strip line, or coplanar waveguide for given impedance and substrate parameters. LineCalc performs calculations using analysis techniques which are similar to Equation 4.1 and Equation 4.2. In this project, to design the characteristic impedance $Z_0 = 50\ \Omega$ CPW on InP substrate with the dielectric constant $\varepsilon_r = 12.5$ [121] and the thickness $h = 635\ \mu m$, the calculation results shows the required width of the signal line $w = 60\ \mu m$ and the gap width $s = 40\ \mu m$. This CPW line with $w = 60\ \mu m$ and $s = 40\ \mu m$ were fabricated and characterized on this project. Experimental results will be described in Section 4.3.1.

In this project, the CPW line was used in the realisation of inductors and so the detailed procedure for designing an inductor using shorted CPW stub is described here. Figure 4.2(a) shows the layout of a shorted stub, while Figure 4.2(b)

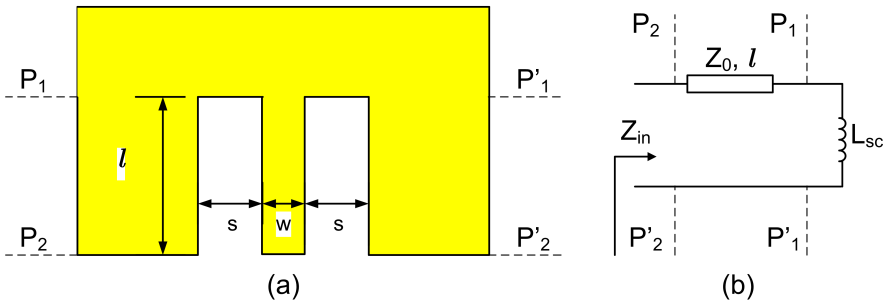


Figure 4.2: *(a) Physically shorted CPW structure. (b) Shorted CPW equivalent circuit.*

shows the equivalent circuit of this structure. In this structure, the current flows through the metallisation at the end of the slots. Magnetic energy is therefore stored behind the termination, which gives rise to an inductive reactance denoted as L_{sc}. This L_{sc} is located beyond the physical end of the slots (reference plane P_1-P_1' in Figure 4.2(a)). The distance corresponding to the reference plane P_1-P_1' is described in terms of effective length extension l_{ext} [116] [122]. l_{ext} can be determined by the geometrical size of the CPW structure. A simple design rule for l_{ext} is given by [122]

$$l_{ext} \approx \frac{w + 2s}{8} \tag{4.8}$$

This approximation holds good when the conductor thickness t is small ($t < \frac{s}{3}$) [116]. The shorted end inductance L_{sc} value is given by

$$L_{sc} = \frac{Z_0 tan(\beta l_{ext})}{\omega} \tag{4.9}$$

when l_{ext} is small compared to the wavelength, the term $tan(\beta l_{ext})$ approximately equals βl_{ext} and hence Equation 4.9 can be re-written as

$$L_{sc} = \frac{Z_0 \beta l_{ext}}{\omega} \tag{4.10}$$

where $\beta = \dfrac{2\pi f_o\sqrt{\varepsilon_{eff}}}{c_0}$ and $\omega = 2\pi f$. ε_{eff} is the CPW effective dielectric constant. For a finite-width ground CPW on a relatively thick substrate with a single dielectric layer, the effective dielectric constant is given by $\varepsilon_{eff} = \dfrac{1}{2}(\varepsilon_r + 1)$ [116], where ε_r is the relative permittivity of the substrate; c_0 is the velocity of light in free space; and Z_0 is the CPW characteristic impedance.

When the electrical length of the CPW is smaller than $\pi/2$, the reactance of the shorted CPW is inductive. This is an important feature of the shorted CPW as a part of the resonator design. For instance, to design an (RTD) oscillator operating at frequency f_o, for parallel resonance, the frequency can be determined by

$$f_o = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}} \tag{4.11}$$

where C_{eq} is the equivalent RTD device capacitance(s) and L_{eq} is the required inductance. The input impedance seen towards the short end from reference plane P_2-P_2' in Figure 4.2 is given by transmission line impedance Equation 4.12.

$$Z_{in} = Z_0\frac{Z_L + jZ_0tan(\beta l)}{Z_0 + jZ_Ltan(\beta l)} \tag{4.12}$$

where $Z_L = j\omega L_{sc}$. The equivalent inductance L_{eq} is then given by

$$j\omega L_{eq} = Z_{in} = jZ_0\frac{\omega L_{sc} + Z_0tan(\beta l)}{Z_0 - \omega L_{sc}tan(\beta l)} \tag{4.13}$$

Combining Equation 4.13 and Equation 4.11, for a given desired frequency f_o (angular frequency w_o), the length of CPW (l) can be determined by Equation 4.14 below, which provides a guideline for an RTD oscillator design employing

shorted CPW stub as a part of the resonator.

$$l = \frac{C_0}{w_o\sqrt{\varepsilon_{eff}}} arctan\left[\frac{Z_0 w_o(L_{eq} - L_{sc})}{(Z_0^2 + w_o^2 L_{eq} L_{sc})}\right] \tag{4.14}$$

4.2.2 Metal-Insulator-Metal (MIM) Capacitor

Capacitors are one of the most commonly used passive components in RF applications. They are used in filter circuits, coupling circuits, dc block circuits, RF bypass circuits, impedance matching networks, resonators, etc [123]. In MMIC circuit design, interdigital capacitors and metal-insulator-metal (MIM) capacitors are the common capacitor types. Comparing these two capacitors, with the same size, the attainable capacitance of the MIM capacitor is larger than the interdigital capacitor [116] [124], which is preferable for RF bypass circuits. Therefore only MIM capacitors were employed in this project. Normally a MIM capacitor consists of a dielectric layer sandwiched between two metal plates. The layout of a MIM capacitor is shown in Figure 4.3.

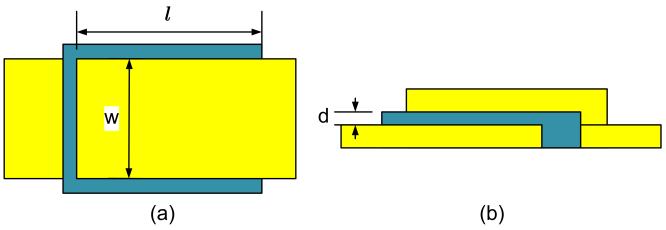


Figure 4.3: *The layout of MIM capacitor. w is the width of the conductor, l is the length of the overlapped conductors. d is the thickness of the insulator. (a) Top view. (b) Cross-section view.*

The high dielectric constant insulator Si_3N_4 is deposited by inductively coupled plasma chemical vapour deposition (ICP-CVD) at room temperature as an insulator. The dielectric constant ε_r of Si_3N_4 is about 6.8. The value of the

capacitor can be estimated by Equation 4.15

$$C = \epsilon_0 \epsilon_r \frac{wl}{d} \tag{4.15}$$

where $\epsilon_0 = 8.854 \times 10^{-12}\ F/m$ is the vacuum permittivity and ϵ_r is the dielectric constant. $w,\ l,\ d$ are the dimensions of the capacitor shown in Figure 4.3. The value of the capacitor (C_e) was chosen to act as a short circuit at the desired frequency f_0. In practice, the reactive capacitance was chosen to be less than 0.1 Ω, i.e. $(2\pi f_0 C_e)^{-1} < 0.1$. For 75 nm thick Si_3N_4, a typical capacitance value of 0.8 $fF/\mu m^2$ can be expected from Equation 4.15. Two types of capacitors, in series and in parallel configuration, with different sizes were investigated. The equivalent circuit and the fabricated series capacitor is shown in Figure 4.4 (a) and (b), respectively, and that for the shunt capacitor is shown in Figure 4.5 (a) and (b). The series capacitor was used as the DC block, while the shunt capacitor was used as an RF short circuit. Capacitors of different sizes, $120 \times 60\ \mu m^2$ and $100 \times 200\ \mu m^2$, were fabricated and characterized in this project. Experimental results will be described in Section 4.3.2.

4.2.3 Thin Film Resistor

In MMIC realisations, thin film resistors are widely used in feedback networks, impedance matching circuits, bias circuits and terminations etc. Normally the thin film resistors are fabricated by evaporating a thin resistive film on the substrate. When choosing a thin film resistor, several factors are need to be considered:

- Sheet resistivity

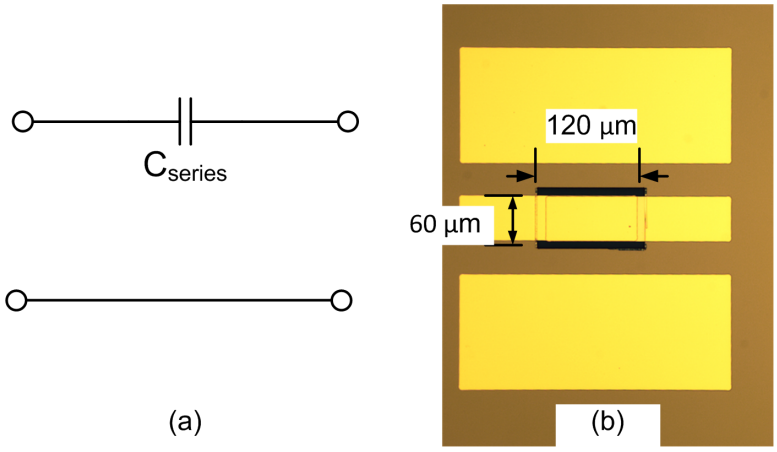


Figure 4.4: *(a) Coplanar waveguide series MIM capacitor schematic circuit.(b) The micrograph of the fabricated series MIM capacitor.*

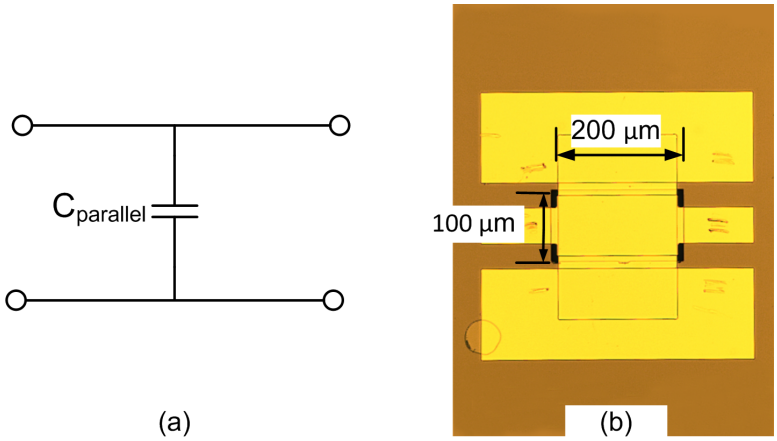


Figure 4.5: *(a) Coplanar waveguide parallel MIM capacitor schematic circuit.(b) The micrograph of the fabricated parallel MIM capacitor.*

- Current/power density handling capability
- Resistance accuracy or reproducibility
- Temperature coefficient of resistance (TCR)
- Frequency response

The material to be used for the film resistor should have high electrical resistivity, high current/power handling capacility and low temperature coefficient of resistance (TCR). Tantalum nitride (TaN) and Nichrome (NiCr) are the most widely used film materials. NiCr resistors are fairly easy to fabricate, sheet resistance is controllable by changing the geometrical size, and they show a low TCR (77 $ppm/°C$) [125] [126]. Due to accessibility, only NiCr thin film resistor were employed in this project. The geometry of the fabricated thin film NiCr resistor is shown in Figure 4.6(a). The length of the resistor is l while the width is denoted as w. The cross section of the resistor is also illustrated in Figure 4.6(b). The

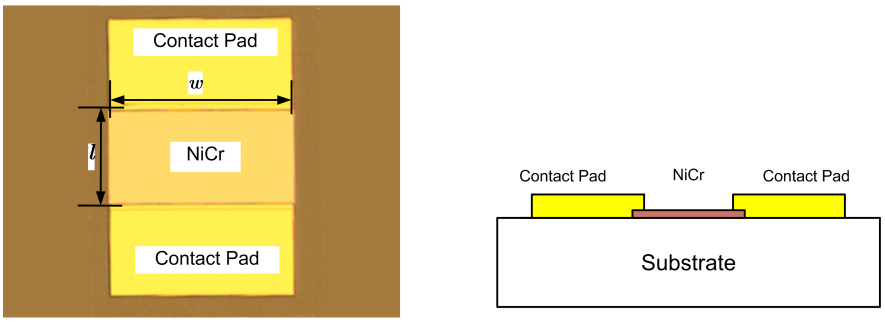


Figure 4.6: *(a) Micrograph of a NiCr film resistor. (b) Cross section sketch of the resistor.*

resistor value R can be calculated by

$$R = \rho\frac{l}{wd} = R_{sh}\frac{l}{w} \tag{4.16}$$

where ρ is the material bulk resistivity, l is the length of the resistor along the direction of current flow, and w and d are the width and the thickness of the film material, respectively. The resistance can also be expressed in terms of sheet resistance R_{sh} together with l and w, as show in Equation 4.16.

A 33 nm thick NiCr film provides approximately $R_{sh} = 50\Omega/\square$ [127] [128]. To design a $R = 15\ \Omega$ NiCr resistor with $w = 300\ \mu m$, the calculated length $l = 90\ \mu m$. Three different NiCr resistors ($R = 15, 20, 25\ \Omega$) were designed with geometries shown in Table 4.1. Experimental results will be described in Section 4.3.3.

Table 4.1: *NiCr film resistor geometries*

Designed Value (Ω)	$R_{sh}(\Omega/\square)$	$l(\mu m)$	$w(\mu m)$
15	50	90	300
20	50	120	300
25	50	150	300

4.3 Characterisation of Passive Components

This section describes the characterisation of the individual passive components required for the realization of RTD MMIC oscillators. The main characterizing technique utilized for the CPW line and MIM capacitors is scattering parameter (S-paramter) measurement, which is performed by using a calibrated vector network analyser (VNA). With the build-in RF source, a VNA measures the reflected and transmitted coefficient as a function of frequency. The accessible VNA in the project is N5250C VNA from Agilent Technoliges, which can sweep the frequency from 10 MHz to 110 GHz. Before any accurate measurements can be performed, the VNA must be calibrated using precise reference impedance standards to correct the systematic errors, which results from the reflection and transmission losses within the measurement system [129]. The calibration method used in this project is Short-Open-Load-Through (SOLT) method, which utilizes a short circuit, an open circuit, a precise defined load (50 Ω) and a through con-

nection. Since the behaviours of these standards are known, the systematic errors existing in the system can be defined by measuring these standards with the VNA. After calibration, the VNA can be utilized to make accurate measurements.

4.3.1 Coplanar Waveguide

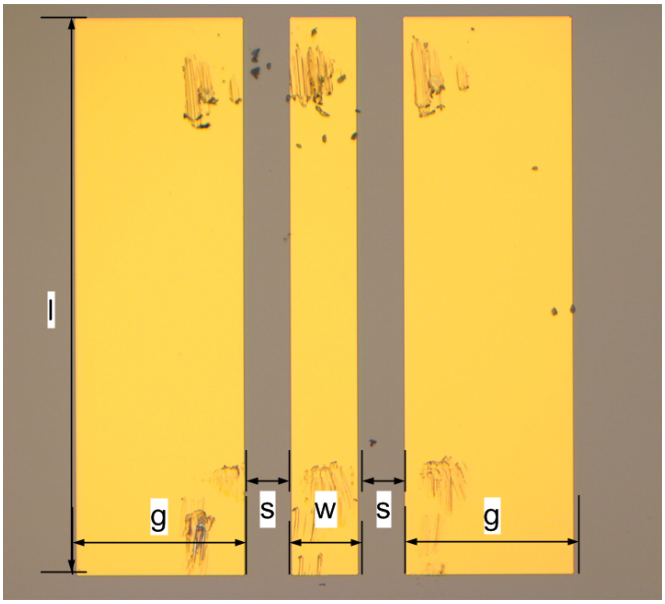


Figure 4.7: *The micrograph of the design CPW test structure. The centre strip width w is 60 μm, the gap width s is 40 μm, the ground plane width g is 150 μm and the length l is 490 μm.*

To design a coplanar waveguide (CPW) with a characteristic impedance $Z_0 = 50\ \Omega$ on a semi-insulating InP substrate of dielectric constant $\varepsilon_r = 12.5$ and thickness $h = 635\ \mu m$, the calculated centre strip width w is 60 μm and the gap width s is 40 μm. The ground plane width g is 150 μm, which is 2.5 times the centre strip width to reduce the radiation loss [118] [119]. The fabricated CPW test structure of 490 μm length is shown in Figure 4.7. It was characterized by 2-port S-parameter measurements from 10 MHz to 110 GHz. The input reflection

coefficients, S_{11} and S_{22}, are plotted on Smith chart as shown in Figure 4.8. The characteristic impedance Z_0 of the coplanar waveguide is very close to the

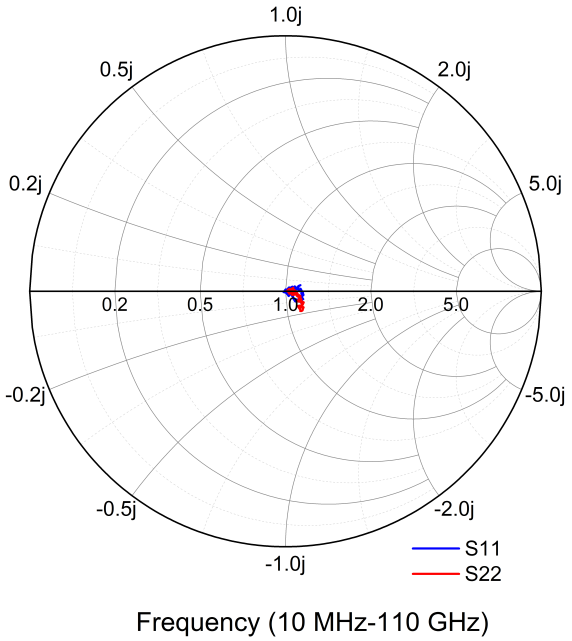


Figure 4.8: *The S-parameter (S_{11}, S_{22}) measurement result of the CPW (length 490 μm) with designed characteristic impedance $Z_0 = 50\ \Omega$.*

designed value 50 Ω. The insertion loss of the CPW is estimated about 0.2 dB/mm in the V-band and 0.51 dB/mm in the W-band.

4.3.2 MIM Capacitors

As described in Section 4.2.2, metal-insulator-metal (MIM) capacitors are widely used in RF circuits due to the low leakage current and low process variations [123]. In this project, MIM capacitors were mainly utilized as RF decoupling and DC blocking circuits. Two types of capacitors, in series and in parallel configuration were designed with two different sizes, $120 \times 60\ \mu m^2$ and $200 \times 100\ \mu m^2$. Figure 4.9 shows micrographs of the fabricated capacitors. The thickness of the

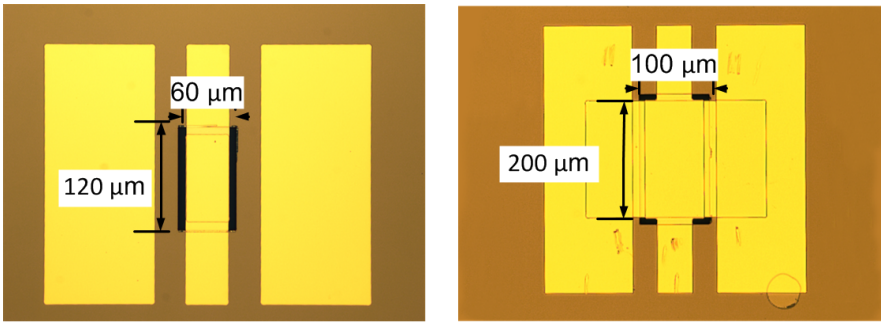


Figure 4.9: *(a)Fabricated series MIM capacitor with* $C_{series} = 5.7\ pF$*.(b)Fabricated parallel MIM capacitor with* $C_{parallel} = 16.1\ pF$*.*

insulator (Si_3N_4) is 75 nm. The calculated capacitor values are $C_{series} = 5.7\ pF$ and $C_{parallel} = 16.1\ pF$. These capacitors were expected to act as short circuits in the millimetre-wave range. The performance of the capacitors was investigated by two-port S-parameter measurements. The results are shown in Figure 4.10. Figure 4.10 shows the input reflection coefficient, S_{11}, for both capacitors over a frequency of 10 MHz-110 GHz on a Smith chart. For the $100 \times 200\ \mu m^2$ parallel capacitor, when the frequencies are above 10.0 GHz, the capacitor acts as a short circuit with input impedance under $0.3 + j0.2\ \Omega$ (Figure 4.10). For the $120 \times 60\ \mu m^2$ series capacitor, when the frequency ranges from 10 GHz to 100 GHz, the series capacitor acts as a shorted circuit. At 10 GHz, $Z_{in} = 50.3 - j3.2\ \Omega$. When the frequency is over 100 GHz, the parasitic elements, such as the parasitic resistance arising from skin effect and the parasitic inductance arising from the pads and plates, degrade the capacitor performance. For the DC blocking or RF decoupling circuit functions, the designed MIM capacitors in this project are suitable for frequencies between 10 GHz and 100 GHz.

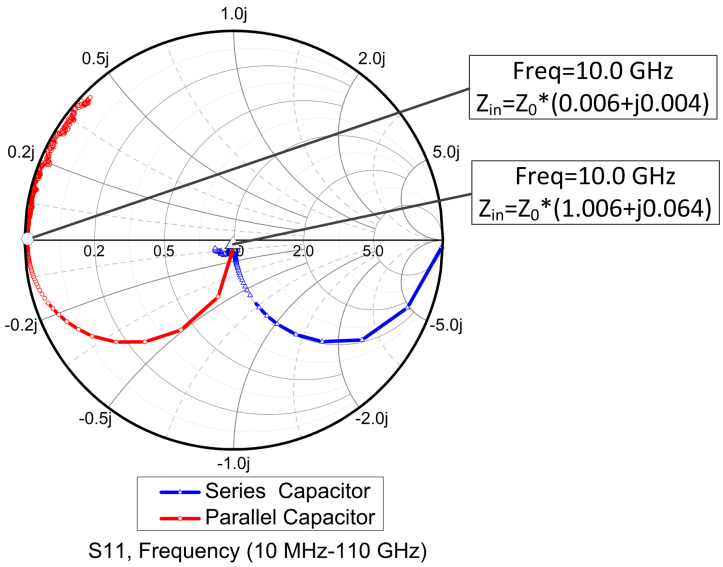


Figure 4.10: *The S-parameter measurement results, S_{11}, of the series/parallel MIM capacitor (blue/red line).*

4.3.3 Thin Film Resistor (NiCr)

As described in Section 4.2.3, NiCr resistors with three different values R= 15, 20, and 25 Ω were designed and fabricated. A micrograph of a fabricated NiCr resistor with dimensions (length l × width w) is shown in Figure 4.11(a). The cross section sketch is shown in Figure 4.11(b). The resistor value were characterized by DC measurement using B1500A semiconductor device parameter analyser from Agilent. The theoretical values and the practical measurement results are compared in Table 4.2. The discrepancy between the designed and measured/fabricated values of up to 15 % may due to the non-uniform deposition rate of the metal film, the contaminated interface between the film and contact pads, or the non-calibrated NiCr sheet resistance value, etc.

The typical allowed current density value for NiCr material is about 4 × 10^6 A/cm^2 [130], thus the current handling of a resistor in a bias circuit is de-

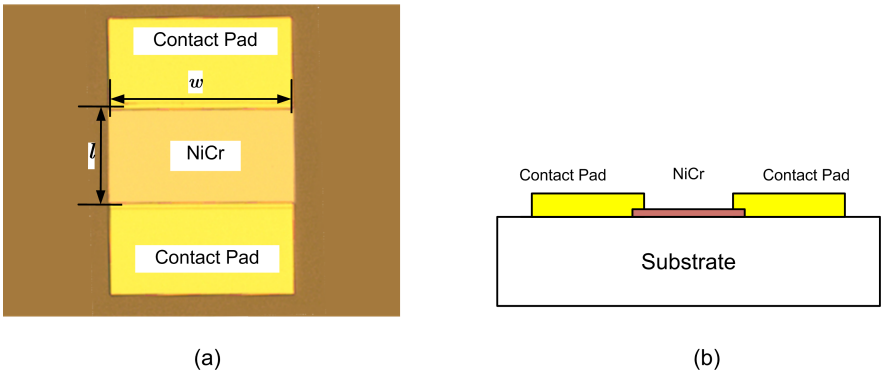


Figure 4.11: *(a) Micrograph of a NiCr film resistor. (b) Cross section sketch of the resistor.*

Table 4.2: *NiCr film resistor*

Designed Value (Ω)	$R_{sh}(\Omega/\square)$	$l(\mu m)$	$w(\mu m)$	Measured Value (Ω)	Divergence
15	50	90	300	13.80	8.0%
20	50	120	300	16.95	15.3%
25	50	150	300	21.3	14.8%

termined by the required bias voltage and the cross section size of the resistive film. For a 33 nm thick NiCr resistor of $R = 20\ \Omega$, and dimensions $w = 300\ \mu m$, $l = 120\ \mu m$ the approximate maximum allowed current is $0.40\ A$ with the maximum allowed bias voltage $V_{bias} = 8.0\ V$.

4.4 Metal-Semiconductor Ohmic Contact

The metal-semiconductor contact resistance theory was proposed by Schottky in the 1930s [131]. Resistance plays an important part in device performance. Large contact resistance will degrade the performance of specific devices in terms of consuming power and reducing the cut-off frequency [132]. In this project, the ohmic contact of the RTDs was investigated by transmission line model (TLM)

measurement [133]. The technique involves measuring voltage between a series of metal-semiconductor contacts by applying a constant current. The contacts are separated by various distances, as shown in Figure 4.12. The resistivity was measured by 4-point probe measurement (four terminal sensing) [134–136], of which two outer probes were used to source current and the other two inner probes were used to sense the voltage as shown in Figure 4.12. Due to the high resistivity of the voltmeter, almost no current goes through the sense cable. The measurement accuracy is raised by excluding the cable resistance and the contact resistance of the probe.

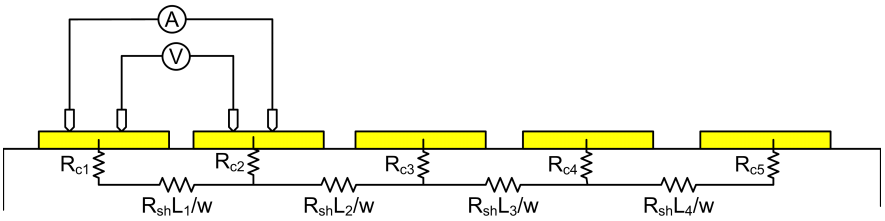


Figure 4.12: *Four-point probes TLM measurement diagram.*

The top view of the TLM measurement structure is shown in Figure 4.13. A series of identical contact pads with width w and length d are separated by various gap distance l_n (n=1, 2, 3, 4). Mesa etching is required to restrict the current flow along only one direction between contact pads [137].

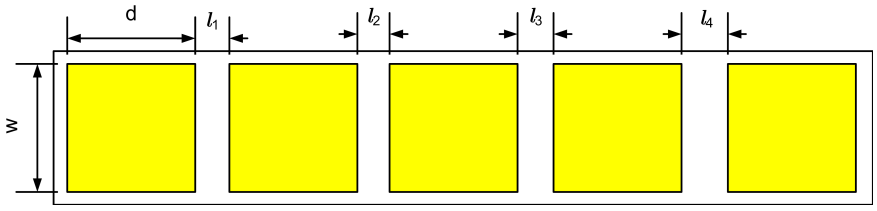


Figure 4.13: *The top view of the TLM measurement structure: metal contacts are separated by various distances l.*

By applying the TLM measurement as shown in Figure 4.12, the measured to-

tal resistance (R_t) includes the first contact resistance (R_{C1}), the sheet resistance in-between the contacts (R_{sh}) and the second contact resistance (R_{C2}). Assuming $R_C = R_{C1} = R_{C2}$

$$R_t = 2R_C + R_{sh}\frac{l}{w} \tag{4.17}$$

The measurement is repeated among several contacts which are separated by various distances. A linear plot of resistance (R_t) versus distance (l) can be obtained as shown in Figure 4.14. From Equation 4.17, it is found that the slope

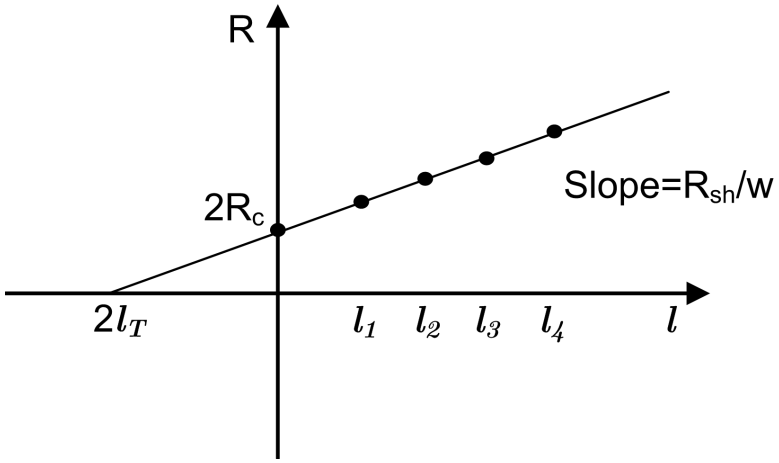
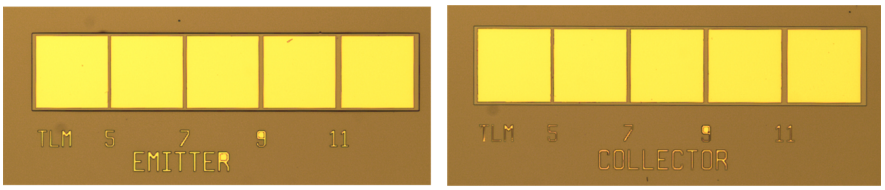


Figure 4.14: *The plot of measured resistance as a function of contacts separation distance l by TLM method.*

of the line is the semiconductor sheet resistance over the width of the contact (R_{sh}/w). When $l = 0$, the intersection of the line with the R-axis equals double contact resistance ($2 \times R_c$). When $R_t = 0$, the interception of the line with the l-axis equals double the transfer length ($2 \times l_T$) . The transfer length defines the distance through which most of the current can transfer from the metal into the semiconductor or the opposite [132]. The specific contact resistance ρ_C is given by Equation 4.18 [138]

$$\rho_C = R_C l_T w \frac{sinh(d/l_T)}{cosh(d/l_T)} \tag{4.18}$$

The fabricated on-wafer TLM test structures are shown in Figure 4.15. The contact pads was the same as the emitter/collector metal scheme which was Ti/Pd/Au (20/30/80 nm). The pads gap distance l_n were 5 μm, 7 μm, 9 μm, 11 μm respectively. The measured resistance values are shown in Table 4.3 and



(a) (b)

Figure 4.15: *The micrograph of the TLM test structures for emitter(a) and collector(b)*

plotted in Figure 4.16. The graphs are linear as expected. The contact resistance

Table 4.3: *TLM measurement results*

Gap (μm)	Resistance (Ω)		
5	1.14	1.22	1.21
7	1.35	1.43	1.45
9	1.57	1.63	1.64
11	1.76	1.81	1.83

(a) *Collector metal contact resistance measurement for 3 TLM patterns*

Gap (μm)	Resistance (Ω)		
5	0.56	0.56	0.56
7	0.63	0.60	0.65
9	0.72	0.70	0.77
11	0.81	0.77	0.79

(b) *Emitter metal contact resistance measurement for 3 TLM patterns*

(R_C), transfer length (l_T), sheet resistance (R_{SH}) and specific contact resistance (ρ_C) are extracted for both the emitter and collector contacts and shown in Table 4.4. The achieved specific contact resistance ρ_C = 122.07/175.61 $\Omega\mu m^2$ was

Table 4.4: *Extracted data from TLM measurement*

	$R_C(\Omega)$	$l_T(\mu m)$	$R_{SH}(\Omega/\square)$	$\rho_C(\Omega\mu m^2)$
Emitter	0.35	3.39	15.25	175.61
Collector	0.18	4.53	5.95	122.07

worse by two orders of magnitude compared with 0.73 ± 0.44 $\Omega\mu m^2$ with the

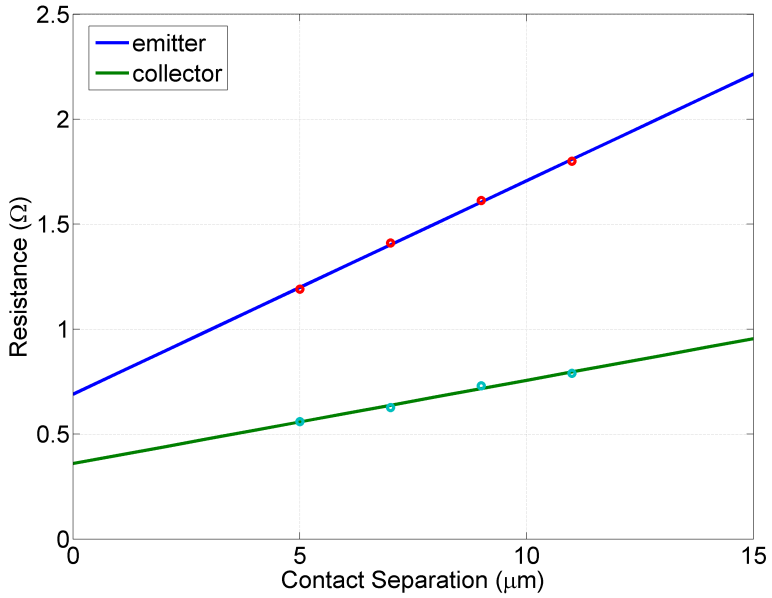


Figure 4.16: *The plot of total resistance R_t as a function of contacts separation distance l.*

same metallisation scheme [76]. However, this contact resistance was deemed satisfactory and no optimisation was done as the focus of the project was to deliver a MMIC technology. The reason for the poor contact resistance was probably that the oxidation layer over InGaAs led to high contact resistance. A de-oxidation process by using a diluted acid will be necessary to reduce the contact resistance in the future.

4.5 Summary

In this chapter, the electrical performance of passive components, the MIM capacitor, the coplanar waveguide, and the thin film resistor, required for realisation of integrated circuit RTD oscillators were investigated. From S-parameter measurements, it was found that the designed series and parallel MIM capacitors

act as RF decoupling circuits for frequencies over 10 GHz. CPW transmission line with characteristic impedance $Z_0 = 50\ \Omega$ on InP substrate was successfully designed and tested. The measured NiCr thin film resistor value shows divergence from the calculation, but this was not critical to the realisation of the MMIC oscillators. Besides the passive components, the Ti/Pd/Au-InGaAs contact resistance was characterized by TLM test structures. In this project, the contact resistance value was much higher than published results. It is expected that this resistance will be reduced by improved surface preparation process before metallization and thereby improve the oscillator performance.

Chapter 5

MMIC RTD Oscillator Design

5.1 Introduction

As described in Chapter 2, RTD devices exhibit negative differential resistance (NDR) which extends from DC up to terahertz. This feature makes the RTD a very promising device to realize compact, room temperature operating terahertz sources. This chapter will describe negative resistance oscillator design utilizing RTDs. Up to date, the biggest limitation of RTD oscillators is low output power. To address this problem, a power combining circuit employing multiple RTD devices was proposed [38]. Figure 5.1 shows the proposed circuit. Each device (RTD1 and RTD2) is biased individually with a decoupling capacitor (C_e) to prevent RF power being dissipated by the shunt resistor (R_e) which is utilized to suppress the low frequency bias oscillations. Also, large sized RTD devices can be employed in the oscillator realisation. More details about the stabilizing resistor will be given later in this chapter.

A hybrid tunnelling diode oscillator circuit utilizing this power combing topol-

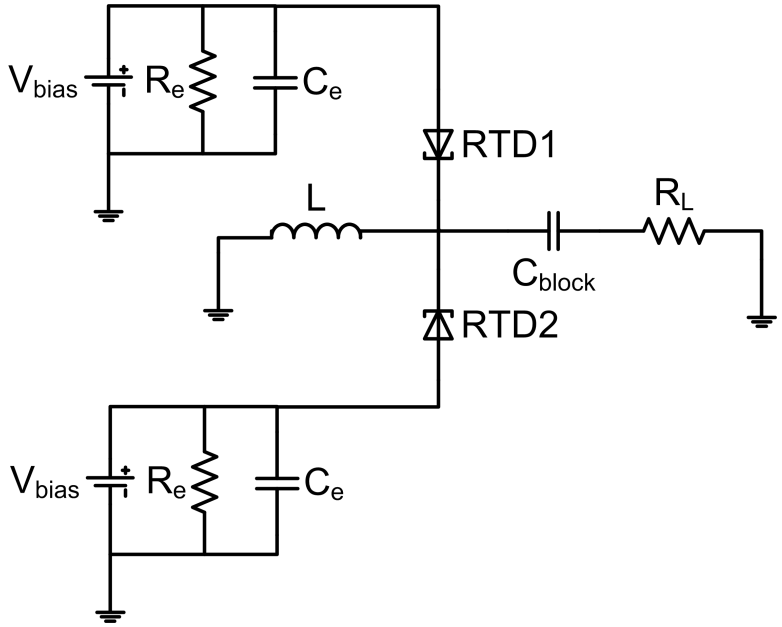


Figure 5.1: *A two RTD oscillator topology. Each device(RTD1 and RTD2) is biased individually with shunt resistor (R_e) and decoupling capacitor (C_e). L, C_{block} and R_L represents the resonator inductance, the DC block capacitor and the load resistance, respectively.*

ogy was first realized at 437 MHz with -6.5 dBm power [38]. This output power was 2 dB higher than for a single tunnel diode oscillator. The result validated the feasibility of the power combining circuit topology. The biggest challenge of this project was to scale up the oscillator design from the low frequency hybrid realisation to a high frequency microwave/millimeterwave integrated circuit RTD oscillator operating at around 100 GHz with around a milli-Watt power. Before the RTD oscillator topology is discussed, it is necessary to review the current-voltage characteristics of the fabricated RTD devices.

5.2 Characteristics of RTD

The typical measured current-voltage (I-V) characteristic of a single RTD device (4×4 μm^2 mesa size) is shown in Figure 5.2. When the bias voltage is located between around 1.1 V and 1.8 V, the device exhibits a negative differential resistance (NDR) region. Due to low frequency bias oscillations [139] [140], the I-V curve shows a plateau-like feature in the NDR region.

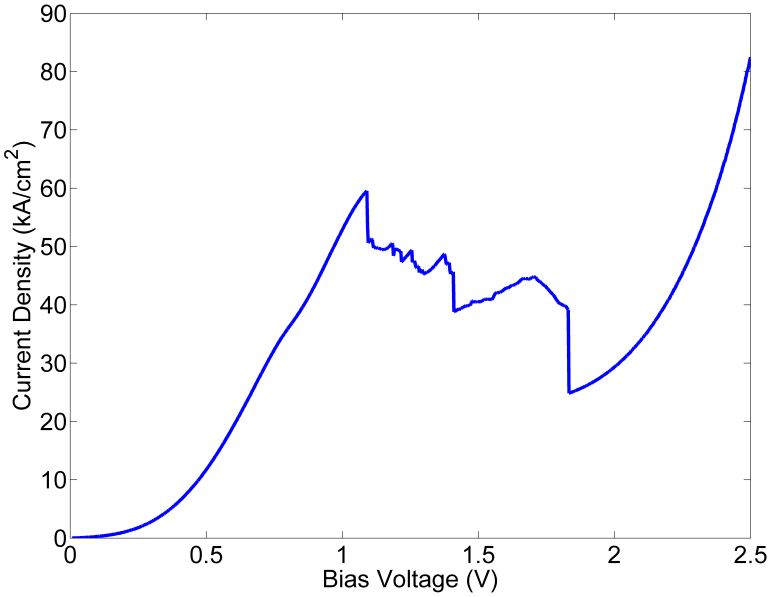


Figure 5.2: *Measured I-V characteristics of a single* $4 \times 4 \mu m^2$ *RTD device. When the bias voltage is located between 1.1 V and 1.8 V, the device exhibits a negative differential resistance (NDR) region. The peak current density* $J_p = 59.5$ kA/cm^2

The large signal model of an RTD device, exhibiting the non-linear I-V characteristics, is shown in Figure 5.3(a). The RTD is represented by a voltage controlled current source $I(V)$ in parallel with the self capacitance C_n. The self-capacitance C_n can be estimated from the mesa geometrical size of the device by

Equation 5.1 .

$$C_n = \frac{\varepsilon A}{d} \tag{5.1}$$

where ε is the dielectric constant, A is the RTD mesa size, d is the length of the double barrier quantum well structure including the spacer layers [39] [62] [141]. The voltage controlled current source $I = f(V)$ in the NDR region can be represented by the cubic polynomial Equation 5.2 for analytical purposes [142]. The origin of the I-V characteristics is shifted to the middle of the NDR region for this model.

$$I(V) = -aV + bV^3 \tag{5.2}$$

where a and b are constant coefficients. The corresponding small signal equivalent circuit for the RTD is shown in Figure 5.3(b), where R_s is the series resistance arising from ohmic contacts and the resistivity of the emitter and collector regions. The parallel capacitance C_n results from the charging and discharging of electrons between the emitter and collector regions. The negative differential conductance is denoted as $-G_n$. A more complex model would also include the quantum well inductance L_{qw} in series with the negative conductance. The parasitic inductance L_{qw} arises from the time delay to build up the charge in the quantum well [40] [62] [141].

As at the peak/valley point of the I-Vcurve $I(V)$,

$$\frac{dI(V)}{dV} = -a + 3bV^2 = 0 \tag{5.3}$$

the peak bias voltage V_p and the valley bias voltage V_v can be derived by solving Equation 5.3 to give

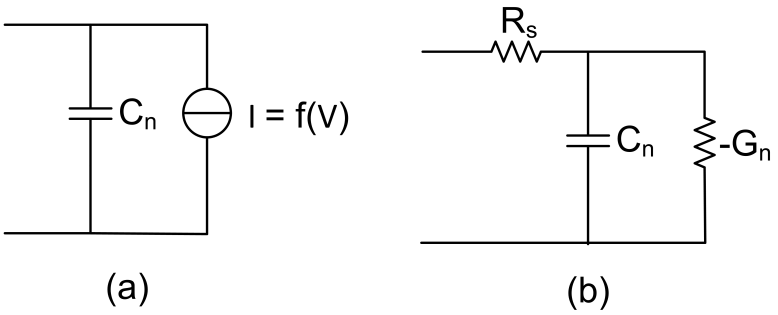


Figure 5.3: *(a) RTD device large signal model, the device is represented by self-capacitance C_n in parallel with voltage controlled current source $I(V)$. (b) RTD small signal model. The negative differential conductance is denoted as $-G_n$. R_s is the series resistance.*

$$V_p = -\sqrt{\frac{a}{3b}}$$
$$I_p = -aV_p + bV_p^3$$
$$V_v = \sqrt{\frac{a}{3b}}$$
$$I_v = -aV_v + bV_v^3$$

and also the peak-valley voltage/current difference $\Delta V/\Delta I$ can be derived

$$\Delta V = V_v - V_p = 2\sqrt{\frac{a}{3b}} \tag{5.4}$$

$$\Delta I = I_p - I_v = \frac{4a}{3}\sqrt{\frac{a}{3b}} \tag{5.5}$$

Combining Equation 5.4 and Equation 5.5, the constants a and b can be expressed

as

$$a = \frac{3}{2}\frac{\Delta I}{\Delta V} \tag{5.6}$$

$$b = \frac{2\Delta I}{\Delta V^3} \tag{5.7}$$

while the RTD negative conductance $-G_n$ by

$$-G_n = \frac{\Delta I}{\Delta V} = -a + 3bV^2 \tag{5.8}$$

The maximum conductance value G_{n_max} is located at the middle of the NDR region with its value $G_{n\_max} = a = \frac{3}{2}\frac{\Delta I}{\Delta V}$, when $V = 0$.

While the large signal model of RTD is utilized for DC analysis to find the operating point or bias condition, the small signal model can be used to help with the oscillator design such as obtaining the input impedance of an RTD, determining the oscillating frequency, etc. From Figure 5.3(b), the RTD input impedance Z_{rtd} can be written as

$$Z_{rtd} = R_s - \frac{G_n}{G_n^2 + w^2 C_n^2} - j\frac{wC_n}{G_n^2 + w^2 C_n^2} \tag{5.9}$$

It is found from Equation 5.9 that at certain angular frequency w_r, the real part of Z_{rtd} becomes zero. Thus w_r is given by

$$w_r = 2\pi f_r = \frac{1}{C_n}\sqrt{\frac{G_n}{R_s} - G_n^2} \tag{5.10}$$

f_r is an important quantity that defines the upper limit of the frequency, i.e. cut-off frequency, response of a RTD device. When the frequency is larger than f_r, the

real part of Z_{RTD} becomes positive, and so the RTD will not function as an active device. It can also be noted from Equation 5.10 that a large series resistance R_s will degrade the RTD performance by reducing f_r. Using the alternative expressions for C_n, G_n and R_s, Equation 5.10 can be re-written as follows

$$\begin{aligned} f_r &= \frac{1}{2\pi C_n}\sqrt{\frac{G_n}{R_s} - G_n^2} \\ &= \frac{d}{2\pi\varepsilon_0\varepsilon_r A}\sqrt{\frac{2\Delta J A^2}{3\Delta V \rho_C} - \frac{4\Delta J^2 A^2}{9\Delta V^2}} \\ &= \frac{d}{2\pi\varepsilon_0\varepsilon_r}\sqrt{\frac{2\Delta J}{3\Delta V \rho_C} - \frac{4\Delta J^2}{9\Delta V^2}} \end{aligned} \tag{5.11}$$

where $C_n = \dfrac{\varepsilon_0\varepsilon_r A}{d}$, $G_n = \dfrac{2\Delta I}{3\Delta V} = \dfrac{2\Delta J A}{3\Delta V}$, and $R_s = \dfrac{\rho_C}{A}$, with ΔJ being the difference between the peak and valley current densities, and ρ_C the specific contact resistance. It can be deduced from Equation 5.11 that for a given RTD layer structure, the cut-off frequency f_r is related to the peak to valley current density (ΔJ) and ρ_C, which is mostly affected by the layer design and the fabrication process, respectively, and is not related to the device size A. A large ΔJ to ΔV ratio and small ρ_C will raise the cut-off frequency of the device, which benefits high frequency applications. This is a new interpretation of high frequency RTD device design, i.e, high frequency operation is not merely determined by scaling/shrinking the device size but by layer design and contact resistance.

For an RTD device with $\Delta J = 2.2 \times 10^5\ Acm^{-2}$, $\Delta V = 0.6\ V$, $\rho_C = 2 \times 10^{-7}\ \Omega cm^2$ [139], the calculated cut-off frequency $f_r = 1.14\ THz$, which is close to 932 GHz, the value estimated by a complex model described in [139]. Since RTD devices exhibit the NDR characteristic from DC up to THz, therefore as long as the sum of the circuit admittance has a negative real part (instability

status), the circuit will oscillate, theoretically with frequencies up to f_r. However, the instability may exist at frequencies other than the designed frequency. The resonance, which exists in the DC bias circuit, is referred to as the bias circuit oscillation. In the presence of the parasitic bias oscillation, the output RF power is distributed between the bias oscillation and the designed frequency, which places a significant constrain on the output power. So before the single RTD oscillator is introduced, it is necessary to investigate the strategy to suppress bias oscillations in the next section.

5.3 DC Stability and Device Sizing

From the I-V measurement data shown in Figure 5.2, a plateau-like current distortion is observed in the NDR region (between V_p and V_v). This is because of the presence of the bias oscillation, which reduces the RF power at the design frequency. To suppress the bias oscillation, the strategy adopted in this project is to employ a shunt resistor (R_e), as shown in Figure 5.4 [38], in which the RTD is represented by its small signal equivalent circuit. The device contact resistance is neglected here.

The admittance looking into the circuit is

$$Y_{in} = (Z_{in})^{-1} = \frac{1}{R_e} + \left[jwL_s + (-G_n + jwC_n)^{-1}\right]^{-1} \tag{5.12}$$

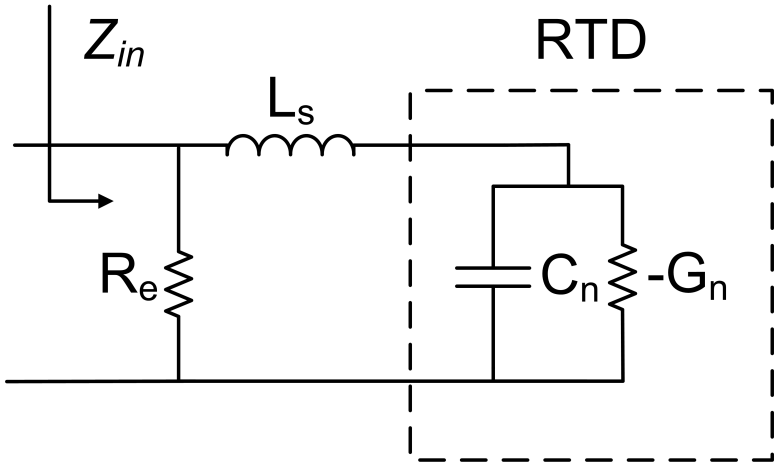


Figure 5.4: *DC stabilized RTD circuit with shunt resistor (R_e) to suppress the bias oscillation. L_s denotes the parasitic inductance. C_n is the self-capacitance and $-G_n$ is the negative differential conductance.*

and the real part of this admittance is

$$\begin{aligned} Real(Y_{in}) &= \frac{1}{R_e} + \frac{-\frac{G_n}{G_n^2 + w^2 C_n^2}}{(\frac{G_n}{G_n^2 + w^2 C_n^2})^2 + (wL_s - \frac{wC_n}{G_n^2 + w^2 C_n^2})^2} \\ &= \frac{1}{R_e} - G_n \frac{1}{(1 - w^2 L_s C_n)^2 + (wL_s C_n)^2} \end{aligned} \tag{5.13}$$

For the circuit to be DC stable (low frequency oscillations are suppressed), it requires that the real part of the admittance, Equation 5.13, is positive [38] [140], which gives

$$\begin{aligned} Real(Y_{in}) &= \frac{1}{R_e} - G_n > 0 \\ R_e &< \frac{1}{G_n} \end{aligned} \tag{5.14}$$

As $Real(Y_{in})$ as the function of w decreases monotonically when $w > \frac{1}{\sqrt{L_s C_n}}$,

at high frequencies, Equation 5.15 below will be satisfied.

$$\frac{1}{R_e} - G_n \frac{1}{(1 - w^2 L_s C_n)^2 + (w L_s C_n)^2} < 0 \tag{5.15}$$

In this case, the real part of the circuit admittance will be less than zero, i.e. $Real(Y_{in}) < 0$, high frequency oscillations would exist in the circuit to making it possible to design RTD oscillators that have no bias oscillations.

Since

$$G_n = \frac{3}{2}\frac{\Delta I}{\Delta V} = \frac{3}{2}\frac{\Delta J A}{\Delta V} \tag{5.16}$$

where $\Delta J = J_p - J_v$ is the difference between the peak and valley current densities J_p and J_v, and A is the RTD mesa size. To satisfy Equation 5.14, it requires that

$$R_e < \frac{2}{3}\frac{\Delta V}{\Delta J A} \tag{5.17}$$

Thus for a given shunt resistor R_e, the criteria to stabilize RTD device with the maximum size A should satisfy

$$A_{max} < \frac{2}{3}\frac{\Delta V}{\Delta J R_e} \tag{5.18}$$

For a specific RTD device with the I-V characteristics as shown in Figure 5.2, where $\Delta V = 0.75\ V$, $\Delta J = 0.35\ mA/\mu m^2$, with a shunt resistor $R_e = 20\ \Omega$ (the resistor value is chosen low enough to achieve bias stability but high enough to minimise the DC power dissipation within this resistor), the stability criteria of

the maximum device size A_{max}

$$A_{max} < \frac{2}{3}\frac{\Delta V}{\Delta J}\frac{1}{(R_e)} = 71.4\ \mu m^2 \tag{5.19}$$

thus three different mesa sizes, $3 \times 3\ \mu m^2$, $4 \times 4\ \mu m^2$, and $5 \times 5\ \mu m^2$ were designed in this project to satisfy both stability criteria and low self capacitance requirement (for high frequency oscillator design). For instance, assuming the device size $A = 70\ \mu m^2$, the corresponding self-capacitance estimated by Equation 5.1 is 149.9 fF. To resonate this capacitance with an inductor $L = 5\ pH$, for example, the calculated oscillating frequency is 183.8 GHz. More details about the frequency calculation of an RTD oscillator will be given in Section 5.4. For comparison, when the device size shrinks down to 9 μm^2, the estimated frequency can reach 512.3 GHz in theory.

5.4 Single RTD Oscillators

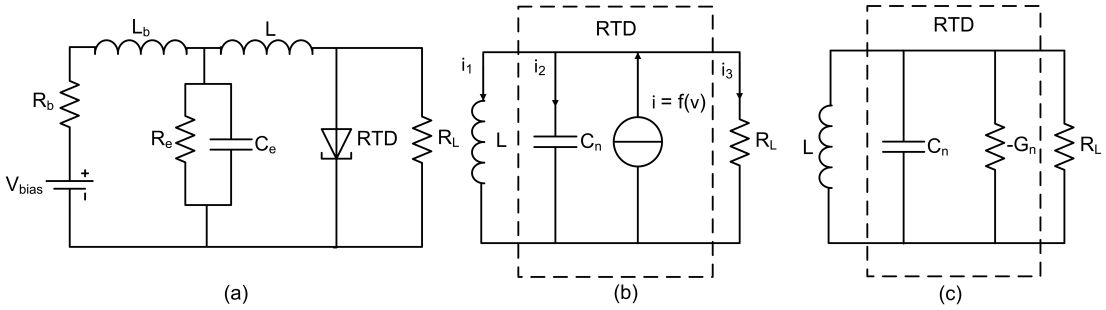


Figure 5.5: *(a) Single RTD oscillator topology with shunt resistor R_e and decoupling capacitor C_e. R_b and L_b denote the bias cable resistance and inductance. R_L is the load resistance and resonator inductance L. (b) Large signal model. RTD is represented by its self-capacitance C_n in parallel with voltage controlled current source $i(v)$. (c) Small signal equivalent circuit. RTD is represented by its self-capacitance C_n in parallel with the negative conductance $-G_n$.*

The single RTD oscillator circuit is shown in Figure 5.5(a), where V_{bias} is the bias voltage to set the device in the NDR region. R_b and L_b are the resistance and inductance introduced by the connecting cable. The shunt resistor R_e is employed to suppress the low-frequency bias oscillation, and C_e is the decoupling capacitor acting as the RF short to the ground to avoid the RF power being dissipated by the resistor R_e. Here the decoupling capacitor was designed following Equation 5.20, i.e. it should act as a short circuit at the desired frequency f_o

$$(2\pi f_o C_e)^{-1} < 0.1 \tag{5.20}$$

The value of R_e should satisfy Equation 5.17, which is

$$R_e < R_n = \frac{2\Delta V}{3\Delta J A} \tag{5.21}$$

to suppress bias oscillations [38] [143]. Equation 5.21 indicates important information for RTD oscillator design: For a large size RTD device, the absolute value of negative resistance (R_n) is small, which requires much smaller shunt resistor R_e to suppress the bias oscillations. For example, for an RTD device with $\Delta V = 0.4\ V$, $\Delta J = 9\ mA/\mu m^2$ [100], if the device size $A = 10\ \mu m^2$, the calculated $R_e = 2.9\ \Omega$, which is an impractically small resistor. Also a large portion of DC power will be dissipated by such a small value shunt resistor. Instead, from Equation 5.21, it can be noted that for a given shunt resistor value R_e, the RTD device size can be maximized with high output power capability while the low frequency bias oscillations can also be suppressed [38].

The RF equivalent circuit of the circuit shown in Figure 5.5(a) is represented in

Figure 5.5(b), where the RTD is replaced by its large single model, which consists of a self-capacitance (C_n) in parallel with voltage controlled current source ($i = f(v) = -av + bv^3$). According to the Kirchhoff's current law

$$i_1 + i_2 + i_3 - i = 0 \tag{5.22}$$

where i_1, i_2, i_3 are branch currents as shown in Figure 5.5(b) and so

$$\frac{1}{L}\int vdt + C_n\frac{dv}{dt} + vG_L + (-av + bv^3) = 0 \tag{5.23}$$

which on differentiating and re-arranging gives

$$LC_n\frac{d^2v}{dt} + L(G_L - a + 3bv^2)\frac{dv}{dt} + v = 0 \tag{5.24}$$

Assuming the voltage v is a sinusoidal signal

$$v = Vcos(\omega t) \tag{5.25}$$

where V is the signal amplitude, and the angular frequency is given by $\omega = \frac{1}{\sqrt{LC_n}}$. The instantaneous power over the load is given by

$$P_L = v^2G_L = (Vcos(\omega t))^2G_L \tag{5.26}$$

The average power by integrating Equation 5.26 over one period is given by

$$P_{Lavg} = G_L\frac{V^2}{2} \tag{5.27}$$

and the instantaneous power over the RTD is given by

$$P_{RTD} = -i \times v = av^2 - bv^4 \tag{5.28}$$

and similarly by integrating Equation 5.28 over one period, the average power is

$$P_{RTDavg} = \frac{aV^2}{2} - \frac{3bV^4}{8} \tag{5.29}$$

As the power generated by RTD equals the power dissipated over the load, thus

$$\frac{aV^2}{2} - \frac{3bV^4}{8} = G_L \frac{V^2}{2} \tag{5.30}$$

The solution of V in Equation 5.30 is given by

$$V = 2\sqrt{\frac{G_n - G_L}{3b}} \tag{5.31}$$

Substituting Equation 5.31 for Equation 5.27, the average power dissipated over the load is given by

$$P_L = 2(G_n - G_L)\frac{G_L}{3b} \tag{5.32}$$

and when

$$G_L = \frac{G_n}{2} \tag{5.33}$$

, the maximum power delivered to the load is [38] [50] [139]

$$P_{max} = \frac{G_n^2}{6b} = \frac{3}{16}\Delta I \Delta V \tag{5.34}$$

Equation 5.34 provides an estimation of the expected maximum RF output power

that can be generated by a single RTD oscillator, where ΔI is the peak-valley current difference and ΔV is the peak-valley voltage difference.

Finally, the small signal equivalent circuit of the single RTD oscillator is shown in Figure 5.5(c) where the RTD is represented by its small signal model (see Figure 5.3(b)). The series resistance R_s in the small signal model has been ignored in the following analysis due to its small value. The frequency of the oscillation (f_o) can be derived from the susceptance of the circuit being set to zero

$$2\pi f_o C_n - \frac{1}{2\pi f_o L} = 0 \tag{5.35}$$

and therefore

$$f_o = \frac{1}{2\pi\sqrt{LC_n}} \tag{5.36}$$

5.5 Double RTD Oscillator Circuits and Layouts

As for the single RTD oscillator, the output power is limited due to the difficulty to employ large size RTD device without bias oscillation (small R_e is required), the oscillator circuit topology utilizing 2 RTDs was proposed as shown in Figure 5.6(a) [58]. Each device, i.e. RTD1 and RTD2, is biased individually with a separate stabilizing circuit. The value of R_e is independent of the number of NDR devices in the circuit. Each individual device size can be maximized according to Equation 5.17. To analyse this circuit accurately, the series contact resistance R_s in RTD small signal model is now considered. The small signal equivalent circuit for the 2 RTD oscillator is shown in Figure 5.6(b). As 2

RTDs are combined in parallel, the equivalent circuit (Figure 5.6(b)) can also be presented by equivalent conductance G' and susceptance B'.

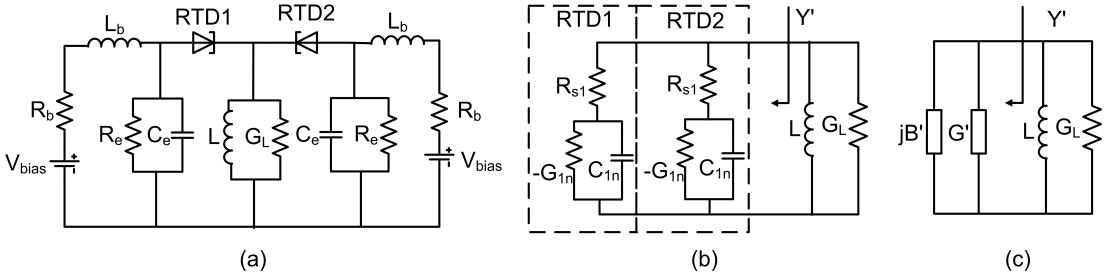


Figure 5.6: *(a) 2 RTDs oscillator circuit topology. 2 RTD devices are employed in parallel with each device is biased separately. (b) Small signal equivalent circuit. (c) Equivalent circuit where 2 RTDs (parallel) are represented by equivalent conductance G' and susceptance B'.*

In Figure 5.6(b), the equivalent admittance Y' can be expressed as

$$Y' = G' + jB' \tag{5.37}$$

where

$$G' = \frac{2\left(R_s - \dfrac{G_n}{G_n^2 + \omega^2 C_n^2}\right)}{\left(R_s - \dfrac{G_n}{G_n^2 + \omega^2 C_n^2}\right)^2 + \left(\dfrac{\omega C_n}{G_n^2 + \omega^2 C_n^2}\right)^2} \tag{5.38}$$

$$B' = \frac{2\left(\dfrac{\omega C_n}{G_n^2 + \omega^2 C_n^2}\right)}{\left(R_s - \dfrac{G_n}{G_n^2 + \omega^2 C_n^2}\right)^2 + \left(\dfrac{\omega C_n}{G_n^2 + \omega^2 C_n^2}\right)^2} \tag{5.39}$$

assuming two identical RTD devices are employed, $G_n = G_{1n} = G_{2n}$, $R_s = R_{s1} = R_{s2}$, $C_n = C_{1n} = C_{2n}$, and $G_L = \dfrac{1}{R_L}$.

The frequency of oscillation can be derived by equating the imaginary part of

circuit susceptance to zero, i.e,

$$jB' + \frac{1}{j\omega L} = 0 \tag{5.40}$$

The output power dissipated by the load is derived in the same manner as for a single RTD oscillator

$$P_L = 2(G' - G_L)\frac{G_L}{3b} \tag{5.41}$$

For an RTD device with the same layer structure as that shown in Chapter 2, the estimated $C_n = 34.2\ fF$ with mesa size $A = 4 \times 4\ \mu m^2$. The measured series resistance was $R_s \approx 11.2\ \Omega$ as shown in Chapter 4. For each fixed value of L, the frequency w can be calculated using Equation 5.40, and then the power from Equation 5.41. For the resonator inductance L value ranging from 4 pH to 150 pH, the calculated power versus frequency is shown in Figure 5.7. The calculation indicates that the circuit shown in Figure 5.6(a) employing two $4 \times 4\ \mu m^2$ RTDs could give about 1 mW power at frequency of around 250 GHz.

Two RTD oscillator circuits (type I and type II), each employing 2 RTD devices were designed, fabricated and characterized on this project. The circuits were realized as MMICs in CPW technology. One of the most important advantages of MMIC over hybrid realization is the reduced parasitics (because no bond wire connections are required as in hybrid circuits) [144]. As described in section 3.4.1, the features of CPW include not only easy series or shunt integration of active devices, but also easy realization of inductive/capacitive elements using short/open stubs.

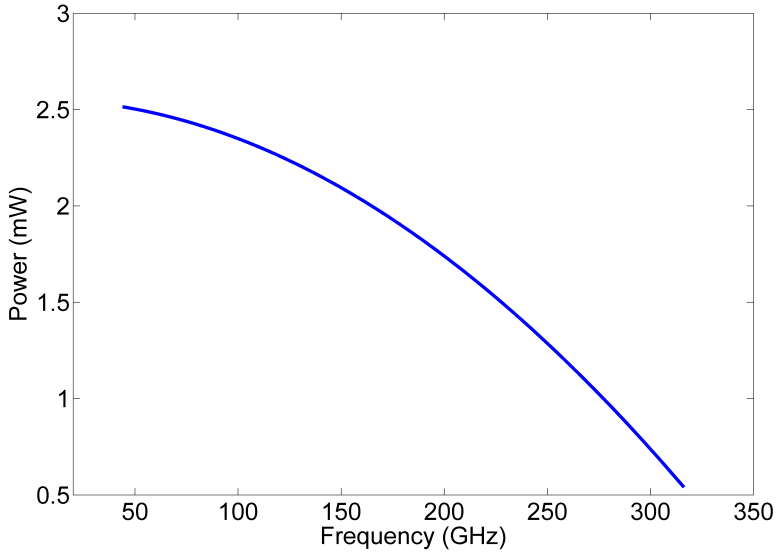


Figure 5.7: *Calculated two RTD oscillator output power versus frequency. The device mesa size is* $A = 16\ \mu m^2$, $R_s = 11.2\ \Omega$, $C_n = 34.2\ fF$, $-Gn = -10.89\ mS$, $G_L = 20\ mS$, $4\ pH < L < 150\ pH$.

5.5.1 Double RTD Oscillator Layout (Type I)

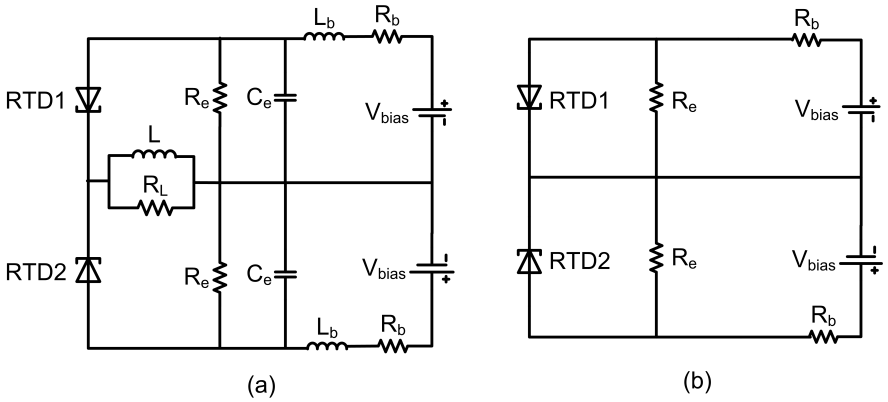


Figure 5.8: *(a) The schematic circuit of double RTD oscillator layout (type I). (b)The DC equivalent circuit.*

The schematic oscillator circuit employing 2 RTD devices is shown in Figure 5.8(a) with its corresponding DC equivalent shown in Figure 5.8(b), where R_b and

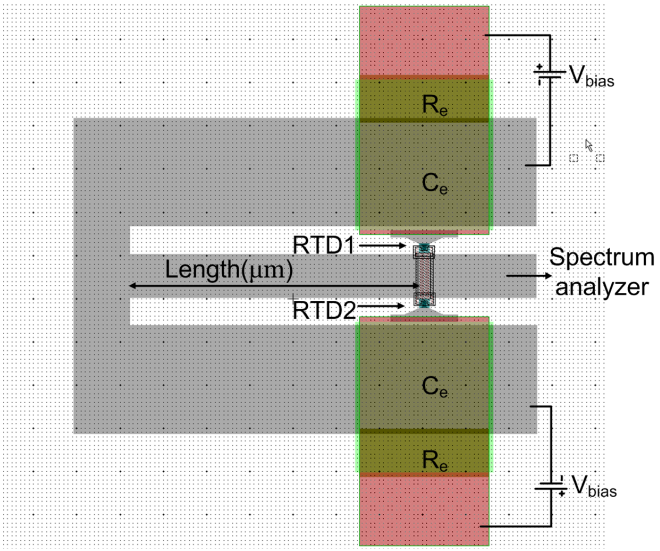


Figure 5.9: *Double RTD oscillator layout (Type I) drawn by L-Edit software.*

L_b denote the resistance and inductance of the bias cable. R_e is the stabilizing resistor, C_e is the bypassing capacitor. As shown in Figure 5.8(b), each RTD device, RTD1 and RTD2, are biased individually with separate resistors (R_e) to suppress the bias oscillations. The RF equivalent circuit is the same as Figure 5.6(b).

The layout of this oscillator, referred to here as *type I*, is shown in Figure 5.9. The stabilising resistor (NiCr) R_e were designed with three different values, 15 Ω, 20 Ω and 25 Ω as shown in Table 4.1. $C_e = 28.5\ pF$ is the bypass MIM capacitor with dimensions ($180\ \mu m \times 200\ \mu m$) for an expected oscillation frequency of at least 22 GHz. The inductance L was realised as a shorted CPW of characteristic impedance $Z_0 = 50\ \Omega$. For the oscillator employing two $5 \times 5\ \mu m^2$ RTDs, three different frequencies, 22 GHz, 38 GHz and 54 GHz, were designed with respect to three different shorted CPW stub lengths, which were 710 μm, 300 μm and 150 μm, respectively. The load (R_L) is the input impedance of the spectrum

analyser (usually 50 Ω).

5.5.2 Double RTD Oscillator Layout (Type II)

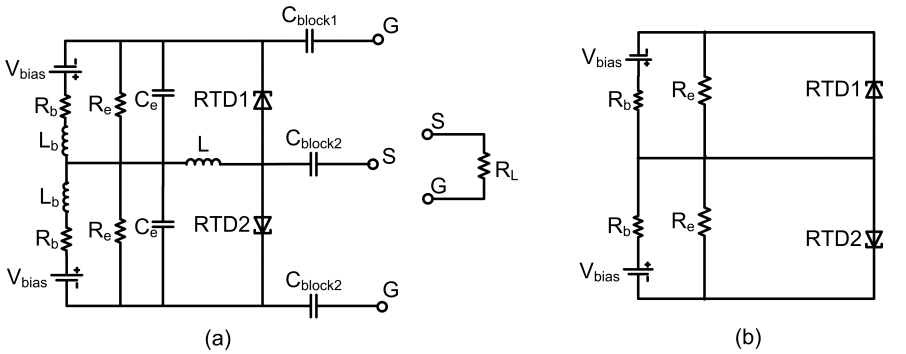


Figure 5.10: *(a) The schematic circuit of double RTD oscillator layout (type II). (b)The DC equivalent circuit. Capacitor $C_{block1,2,3}$ blocks the DC bias reaching the load (spectrum analyser).*

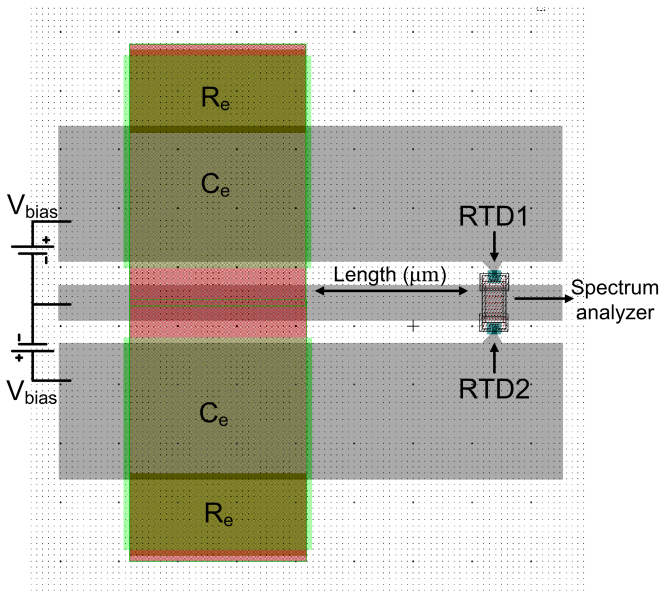


Figure 5.11: *Double RTD oscillator layout (Type II) drawn by L-Edit software.*

The other double RTD oscillator schematic circuit is shown in Figure 5.10(a) with the corresponding DC equivalent circuit shown in Figure 5.10(b), where

RTD1 and RTD2 are biased individually, and the load (R_L) is the input impedance of the spectrum analyzer (usually 50Ω). The RF equivalent circuit is also the same as that in Figure 5.6(b).

The layout of the designed oscillator is shown in Figure 5.11 and is referred to here as *type II*. Instead of using a directly shorted CPW structure as done in the type I realization (Figure 5.9), here the two capacitors (C_e) in Figure 5.11 act as an RF short circuit. For the oscillators employing two 4×4 μm^2 RTDs, three different frequencies, 28 GHz, 43 GHz and 74 GHz, were designed with respect to three different CPW lengths, which were 600 μm, 300 μm and 100 μm, respectively. The values of the passive components (R_e, C_e) are the same for both types of oscillators.

5.6 Summary

In this chapter, the principle of operation of negative resistance oscillators was reviewed. Since RTD devices exhibit negative differential resistance (NDR) characteristics from DC up to terahertz, they can be employed to realize THz sources. The advantages of RTD THz sources are their compact size and room temperature operation. However, the use of present RTD oscillators in real applications is limited by their low output power. Thus oscillator circuits employing multiple RTD devices, with each device biased individually with maximised size, were proposed to address this problem. The design of the proposed RTD oscillators was described in this chapter, including the proper sizing of RTD devices. The next chapter will describe in detail the fabrication process used to realise the oscillators.

Chapter 6

Device/Oscillator Measurement and Characterisation

6.1 Introduction

The characterisation of single RTD devices and double RTD oscillators is described in this chapter. Single RTD devices with three different mesa sizes, $3 \times 3\ \mu m^2$, $4 \times 4\ \mu m^2$ and $5 \times 5\ \mu m^2$ were measured. The I-V characteristics clearly showed the NDR feature of these single devices, which indicated their suitability for applications in oscillator circuits. As described in previous chapters, there were two different double RTD oscillator layouts, type I and type II. The electrical performance of these oscillators in terms of oscillation frequency and output power will be detailed in this chapter. Millimetre-wave RTD oscillators with record output powers of around a milli-Watt were demonstrated in this project and are described in this chapter.

6.2 DC Measurement

The schematic circuit of the DC measurement is shown in Figure 6.1, where the RTD is represented by its circuit symbol, and the current through the RTD is represented by a non-linear function of the bias voltage, $I = f(V)$. The actual

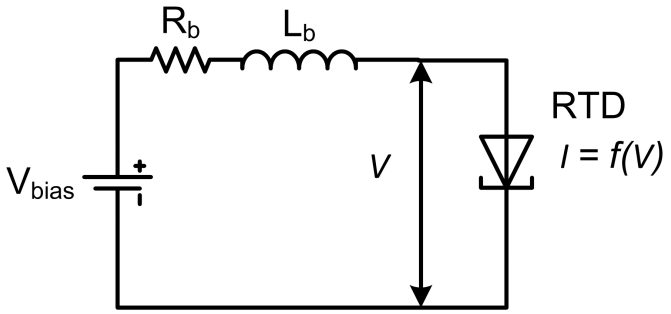


Figure 6.1: *Direct RTD device I-V measurement circuit. R_b and L_b represents the resistance and inductance of the bias cable. The current $I = f(V)$ exhibits the NDR characteristics of the RTD.*

DC measurement set up is shown in Figure 6.2. A B1500A semiconductor device parameter analyzer from Agilent Technologies was used in the measurement. Two DC probes were landed on the metal contact pads as shown in Figure 6.2(b). The top view of the single RTD device central area is shown in Figure 6.2(c). The

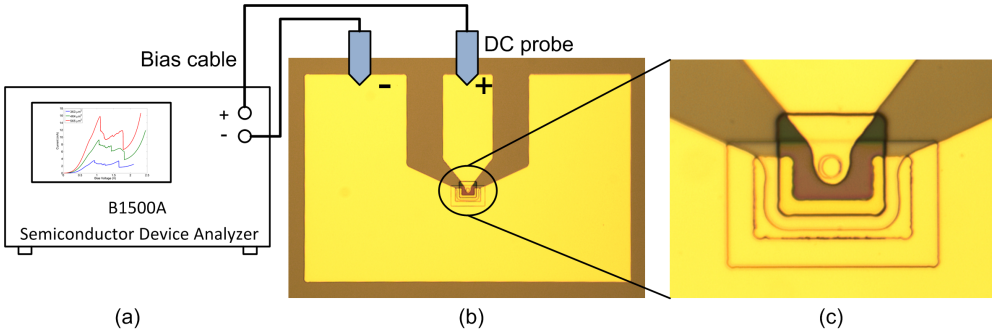


Figure 6.2: *RTD device DC measurement set up. DC bias was supplied by B1500A semiconductor device parameter analyzer (a). Two DC probes were placed on the contact pads as shown in (b). The top view of the device central area is shown in (c).*

measured I-V characteristics for various mesa sizes, the $3 \times 3\ \mu m^2$, $4 \times 4\ \mu m^2$, and $5 \times 5\ \mu m^2$ devices are shown in Figure 6.3. It is noted that when the RTD

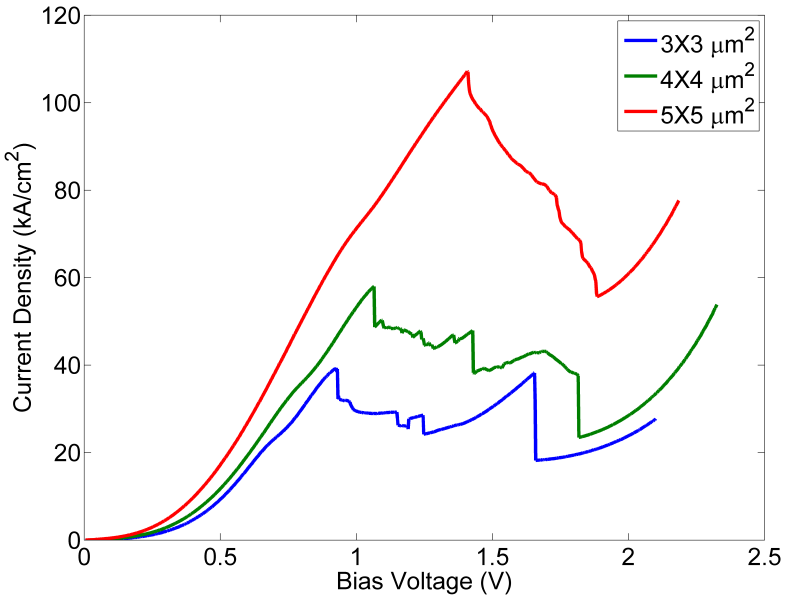


Figure 6.3: *Measured I-V characteristics of various RTD devices.*

devices are biased in the NDR region, the I-V curves show plateau-like distortion due to the bias oscillations [139] [140] [143]. Details of this well known feature will be described in Appendix B for completeness.

There were 9 single RTD devices on a 1 $cm \times 1\ cm$ sample. Besides the devices, the sample also contained other test structures and oscillator circuits as described earlier in Chapter 3. For each mesa size, the $3 \times 3\ \mu m^2$, the $4 \times 4\ \mu m^2$, and the $5 \times 5\ \mu m^2$, there were 3 devices on each sample. The I-V characteristics of each device with the same mesa size showed consistency on the same sample. However different samples showed slightly different characteristics. The peak current density (J_p) varied from 107.2 kA/cm^2 to 39.3 kA/cm^2 between samples. The reasons for this variability may include non-reproducibility of the fabrication

process e.g. different ohmic contact resistance. The peak voltage value V_p (V), the valley voltage value V_v (V), the peak current value I_p (mA), the peak current density $J_p = \frac{I_p}{A}$ (kA/cm^2), the valley current value I_v (mA) , the peak-valley bias voltage difference $\Delta V = V_v - V_p$ (V), the peak-valley current difference $\Delta I = I_p - I_v$ (mA), and the absolute value of negative conductance $G_n = \frac{3\Delta I}{2\Delta V}$ (mS) can be obtained from the measured characteristics and are given in Table 6.1. The estimated maximum RF power P_{max} (mW) by Equation 5.34 for each single device is 0.26 mW for the 3×3 μm^2 device, 0.79 mW for the 4×4 μm^2 device and 1.18 mW for the 5×5 μm^2 device, respectively.

Table 6.1: *RTD DC Measurement*

Size (μm^2)	V_p/I_p (V/mA)	J_p (kA/cm^2)	V_v/I_v (V/mA)	$\Delta V/\Delta I$ (V/mA)	G_n (mS)	Estimated P_{max} (mW)
3×3	0.93/3.54	39.3	1.66/1.64	0.73/1.90	3.90	0.26
4×4	1.06/9.28	58.0	1.82/3.76	0.76/5.52	10.89	0.79
5×5	1.40/26.80	107.2	1.89/13.92	0.49/12.88	39.42	1.18

6.2.1 Measured and Simulated RTD I-V Characteristic

As described in Chapter 2, a self-consistent model was developed to simulate the I-V characteristic of RTD device. In this section, the comparison between the calculation and the measurement results for 5×5 μm^2 device is described and plotted in Figure 6.4. A fair agreement was achieved. At low bias voltage range (0 V$\sim$ 0.5 V), a large difference between the model and the measurement exists. The reason for this needs to be further investigated. A more complex model including the scattering effect [61] [95], the space-charge effect [77], etc. may need to be considered to improve the simulation accuracy.

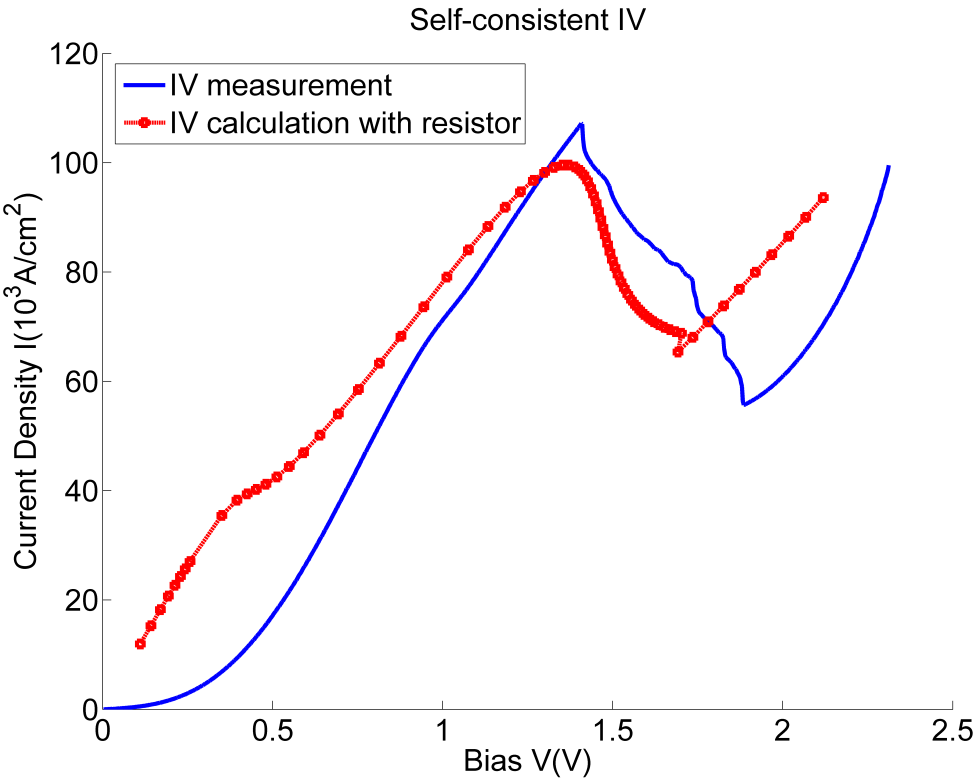


Figure 6.4: *Comparison between the measurement result of the InGaAs/AlAs RTD (5×5 μm^2) and calculated I-V characteristic by using self-consistent model, of which the parasitic resistance $R_s = 35$ Ω was considered.*

6.2.2 RTD Large Signal Model

In order to analyse the non-linear I-V characteristic of an RTD, a polynomial numerical model was set up to fit the measured I-V data by using MATLAB software. The curve fitting toolbox in MATLAB provides such an analytical data processing technique for both linear and non-linear analysis. After the order and unknown coefficients of the polynomial are defined, the curve fitting tool finds the optimized value of each coefficient. The accuracy of fit can be evaluated both graphically and numerically by checking the value of root mean squared error (RMSE). RMSE is frequently used to evaluate the difference between values

predicted by a model and the values actually observed. RMSE is defined by Equation 6.1

$$RMSE = \sqrt{\frac{\sum_{i=1}^{n} (X_{obs} - X_{mod})^2}{n}} \tag{6.1}$$

where X_{obs} is the observed values, X_{mod} is the modelled values and n is the number of sampling [145]. The value of RMSE closer to 0 indicates that the model has a smaller error and that the fit will be useful for prediction.

For a $4 \times 4\mu m^2$ RTD biased in the NDR region, by shifting the origin of the I-V coordinates to the middle of the NDR region, a cubic polynomial model, Equation 6.2, can be used to fit the data [142]. The cubic polynomial model is expressed by

$$I(V) = -aV + bV^3 \tag{6.2}$$

where the constant coefficient $a = -8.2$ and $b = 16.7$ was obtained by the curve fitting tool (MATLAB). The value of RMSE was 0.41. Figure 6.5 shows the measured and fitted cubic model for an RTD. The models are fitted to the measured data in the two positive differential resistance (PDR) regions, with the data in the NDR region ignored because it is modified by bias oscillations. A more accurate numerical model utilizes a 9th order polynomial equation, given by Equation 6.3, for which an RMSE of 0.17 was obtained.

$$I(V) = a_0 + a_1V + a_2V^2 + a_3V^3 + ... + a_9V^9 \tag{6.3}$$

where $a_0 = -1.0$, $a_1 = -10.5$, $a_2 = 6.1$, $a_3 = 34.7$, $a_4 = -13.6$, $a_5 = -32.8$, $a_6 = 10.6$, $a_7 = 17.2$, $a_8 = -0.05$, $a_9 = -1.9$. Both models approximate the NDR region in the same way and the fitting results are compared graphically in Figure

6.5.

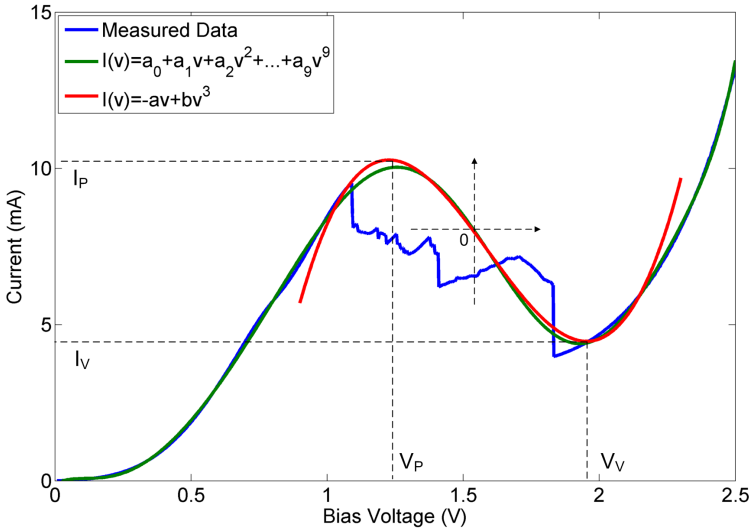


Figure 6.5: *Measured I-V characteristics compared with polynomial numerical fitting (green), including a cubic model for the NDR region (red).*

The large signal model was used in simulations to assess oscillator performance, but these are not shown due to the immaturity of the process and therefore device variability, i.e. the device models were not quite representative of the fabricated devices.

6.3 Frequency and Power Measurement

Depending on the oscillation frequency of the oscillator, diverse equipment are required to set up the measurement platform. The proper choice of equipment will ensure the accuracy, reliability and reproducibility of the measurement. For frequencies below 50 GHz, the signal spectrum and output power can be measured directly by using a spectrum analyser. The spectrum analyser can graphically represent the amplitude of the measured signal as a function of frequency. The

accessible spectrum analyzer in this project was the E4448A spectrum analyser from Agilent Technologies. The upper frequency limit of the E4448A is 50 GHz. For frequencies between 50 GHz and 325 GHz, the measurement involves an external mixer to down-convert the frequencies.

For RF power measurement, there are two approaches implemented in this project. One is to use a spectrum analyser. The other is to use a power meter. A spectrum analyser provides all the information of the signal such as output power, bandwidth, stability, carrier-to-noise ratio, etc. However, when an external mixer is involved to down-convert the high frequency signal, the insertion loss of the mixer needs to be calibrated. The measurement accuracy and reliability can be affected depending on the quality of the mixer. Alternatively, a combination of a power sensor to pick up the related RF signal, and a power meter to process and display the data, provides a well-characterized traceability path back to reference standards [146]. The limitation of a power meter is that it is a broadband equipment. It cannot identify the spectrum at which most of the RF power is distributed.

For high frequency measurements, each equipment or component involved, such as RF probes, cables, connectors, mixers, etc., needs to be carefully considered and calibrated where possible to assure measurement reliability and accuracy. The details of the measurement procedure for the oscillator frequency and output power are provided in Appendix C, since the procedure is standard practice. As described in Chapter 5, double RTD oscillators with 2 different layouts (type I and type II) were designed and fabricated. The performance of these oscillators is described next.

6.3.1 Type I Oscillator Measurement

This oscillator, employed two $5 \times 5\ \mu m^2$ RTD devices in parallel with corresponding layout (type I), is shown in Figure 6.6(a). Each RTD device had a separate DC decoupling circuit to suppress low frequency bias oscillations. The optical picture of this RTD oscillator (type I) measurement setup with probes landed on the chip is shown in Figure 6.6(b). The length of the CPW transmis-

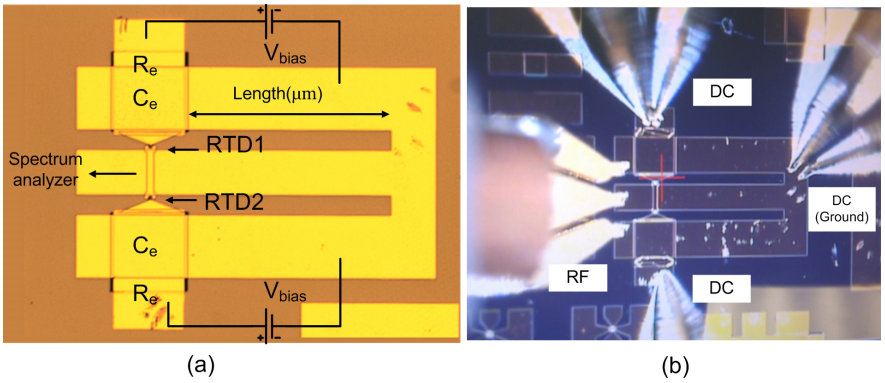


Figure 6.6: *Type I double RTD oscillator measurement. Three DC probe (one common ground) were landed to bias two RTDs individually. RF signal was extracted from RF probe on the left side. (a)The schematic measurement set up. (b) Actual measurement with probes landing on the contact pads.*

sion line was 710 μm, and the estimated frequency, derived from Equation 4.11 in combination with Equation 4.13, was $f_o = 21.8\ GHz$. As described in Chapter 5, oscillators with different desired frequencies and CPW lenghth (300 μm and 150 μm) were also designed and fabricated. However, due to NiCr resistor failure, these oscillators did not work. Therefore, only the 710 μm CPW RTD oscillator result is presented here. When the bias voltage was 1.42 V, the total bias current was 203.6 mA. The measured oscillation frequency was 28.7 GHz with -5.8 dBm output power as shown in Figure 6.7. After compensating the probe and the cable loss, the actual output power was about -0.7 dBm (0.85 mW), which is the

highest power reported for Ka-band RTD oscillator [147].

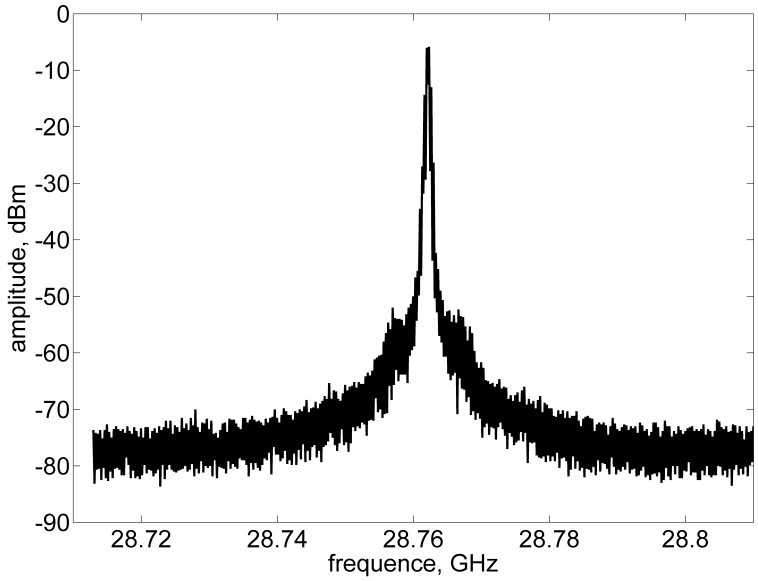


Figure 6.7: *Measured spectrum of the double RTD oscillator (Type I) when* $V_{bias} = 1.42\ V$, $I_{bias} = 203.6\ mA$, $Span = 100\ MHz$, $RBW = 300\ kHz$, $VBW = 30\ kHz$.

As the self-capacitance (C_n) of a specific RTD device changes with the bias voltage [141] [148], the voltage controlled oscillation (VCO) was observed as shown in Figure 6.8. The frequency tuning range is $\Delta f = 1\ GHz$ with tuning sensitivity $\Delta f/\Delta V_{bias} = 6.26\ GHz/V$. The output power fluctuates between -10.3 dBm to -5.8 dBm over the tuning range, a 4.5 dB difference. The single side band phase noise of the oscillator was also measured. Figure 6.9 shows the phase noise performance at 28.7 GHz carrier frequency. It was -95 dBc/Hz at 100 kHz and -114 dBc/Hz at 1MHz offset. This is 3 dB better at 100 kHz and 8 dB worse at 1MHz compared to a Ka-band low phase noise HEMT oscillator [149].

As the shunt resistors ($R_e \approx 15.6\ \Omega$) were employed in the oscillator circuit, when DC bias was 1.42 V, the DC current flowing via the resistors was $i_{Re} =$

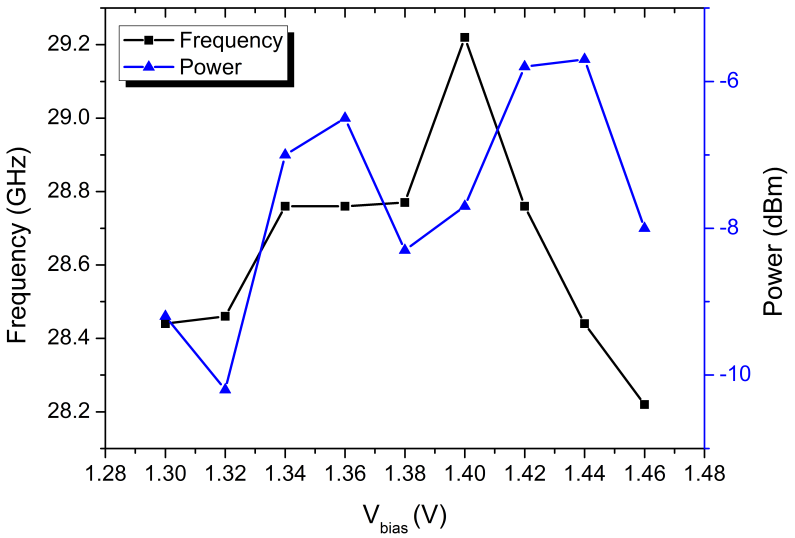


Figure 6.8: *Measured frequency and RF power of the double RTD oscillator (Type I) (VCO) as a function of bias voltage V_{bias}*

$\frac{V_{bias}}{R_e/2} = 180.6\ mA$, and the current through the diode $i_{bias} - i_{Re} = 23.0\ mA$. The DC power dissipated by the two RTDs was therefore 32.66 mW. Thus, device DC-RF conversion efficiency was $\frac{0.85}{32.66} \times 100\% = 2.6\%$ without considering the DC power dissipated by the shunt resistor. The DC-RF conversion efficiency of the oscillator was quite low. This could be attributed to the high contact resistance, as may be seen from Table 4.4, and the use of a 50 Ω load that was not matched to the oscillator impedance. Efforts need to be taken to improve the conversion efficiency in the future.

As the characteristics of a VCO include centre frequency, output power, phase noise, power consumption, tuning range, etc., it is difficult to compare the performance of VCOs realised in different technologies. Nonetheless, a widely accepted

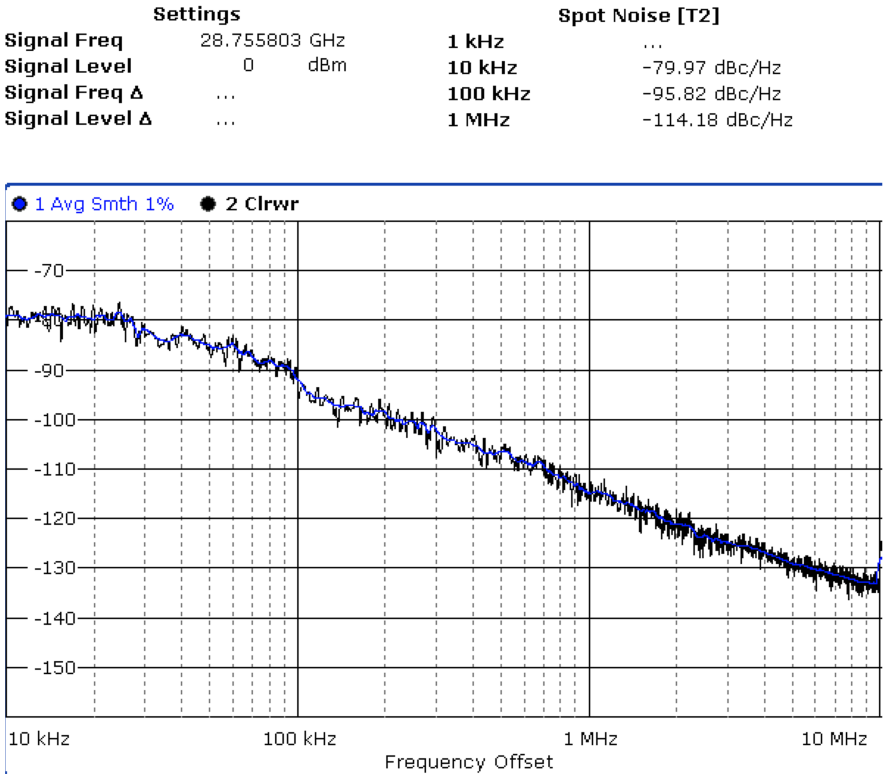


Figure 6.9: *Measured SSB phase-noise performance at 28.7 GHz carrier frequency.*

concept to identify the performance is the *figure of merit* (FOM) [150–153]:

$$FOM = L\{f_{offset}\} - 20log(\frac{f_0}{f_{offset}}) + 10log(\frac{P_{DC}}{1\ mW}) \tag{6.4}$$

where $L\{f_{offset}\}$ is the phase noise in dBc/Hz at offset frequency f_{offset} from the carrier frequency f_0. P_{DC} is the DC power dissipation in mW. The performance of a VCO is considered to be better with a higher absolute value of the FOM. The calculated FOM of the fabricated 28.7 GHz RTD MMIC VCO is -178.3 dBc/Hz when considering the total DC power dissipation including that dissipated by the shunt resistor. This FOM is relatively low compared to other oscillator technologies. The Ka-band (26.5 GHz-40 GHz) VCO performance of various oscillators

from the literature and this work are compared in Table 6.2. The relative low FOM for the first prototype RTD oscillator in this project, is expected to be greatly improved by increasing the DC-RF conversion efficiency.

Table 6.2: *Comparison of the Ka-band VCO performances*

Technology	f_0 (GHz)	Tuning Range (GHz)	Phase noise @1MHz offset (dBc/Hz)	P_{DC} (mW)	FOM (dBc/Hz)	Die Size (mm^2)	Ref.
0.15 μm pHEMT	28.3	3.8	-102	11.8	-180.3	0.5	[150]
InGaP/GaAs HBT	38	1.1	-112	125	-182.6	3.2	[151]
SiGe HBT	28	4.1	-84.2	129	-152.3	0.25	[152]
0.18 μm CMOS	29.9	0.18	-110	27	-185.1	0.24	[153]
InGaAs/AlAs RTD	28.7	1.0	-114	289.1	-178.3	0.89	This Work

6.3.2 Type II Oscillator Measurement

Four oscillators with different design frequencies using type II configuration were fabricated and characterized. The oscillator layout that shows how the measurement is set up, i.e. the DC bias and spectrum analyser connections, is shown in Figure 6.10(a). Figure 6.10(b) shows an optical picture of an actual measurement with probes landed on the chip. The DC bias was applied through ground-signal-ground (GSG) probe on the right side, while the RF signal was extracted from the left side. All the spectrum measurement results for different oscillators are shown in Figure 6.11. Figure 6.11(a) demonstrates the oscillator employing two 4×4 μm^2 sized RTDs working at 33.7 GHz with -9.6 dBm power. The length of the shorted CPW was $l = 620$ μm. The frequency span of the spectrum analyser was 500 MHz, and the resolution bandwidth (RBW) was 300 KHz, while the video bandwidth (VBW) was 100 KHz. Figure 6.11(b) demonstrates

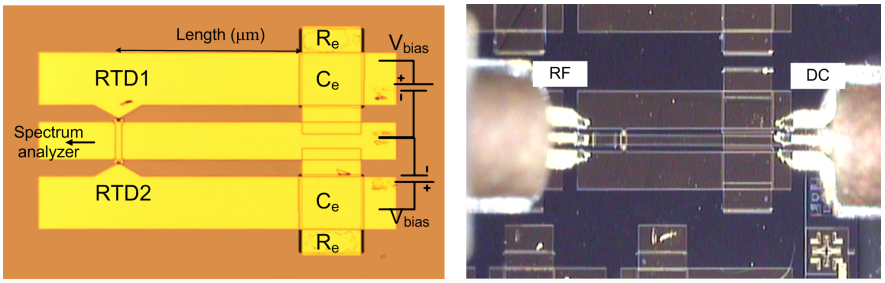


Figure 6.10: *Type II double RTD oscillator measurement. The DC bias was applied through GSG probe on the right side. RF signal was extracted from the left side. (a) The schematic measurement set up. (b) Actual measurement with probes landing on the contact pads.*

double RTD oscillator employing the same size as shown in Figure 6.11(a) but with shorter CPW length of 320 μm. The oscillator operated at 39.6 GHz with -3.7 dBm power. The configurations of the spectrum analyser was as follows: Span=500 MHz, RBW=100 KHz, and VBW=100 KHz. Similarly, a double RTD oscillator employing the same size devices as before but even shorter CPW length ($l = 120\ \mu m$) worked at 75.2 GHz with -41.9 dBm output power. The spectrum is shown in Figure 6.11(c). The span was 100 MHz. The RBW was 2 MHz and the VBW was 150 KHz. Finally, Figure 6.11(d) shows the measured spectrum of a double RTD oscillator employing larger size devices ($5 \times 5\ \mu m^2$) and the shortest CPW length ($l = 75\ \mu m$) that operated at 86.5 GHz with -49.7 dBm power. The span was 300 MHz. The RBW was 3 MHz while the VBW was 3 MHz.

Table 6.3: *Measurement Results*

Mesa Size (μm^2)	Designed Frequency (GHz)	CPW Length (μm)	Frequency (GHz)	Measured Power (dBm)	Calibrated Power (dBm)/(mW)	DC-RF Conversion Efficiency
4×4	28	620	33.7	-9.6	-5.5/0.28	0.96%
4×4	43	320	39.6	-3.7	-0.1/0.98	2.2%
4×4	74	120	75.2	-1.2*	-0.2/0.96	1.5%
5×5	75	75	86.5	-5.6*	-4.6/0.35	0.49%

Note: * The power was measured by a power meter.

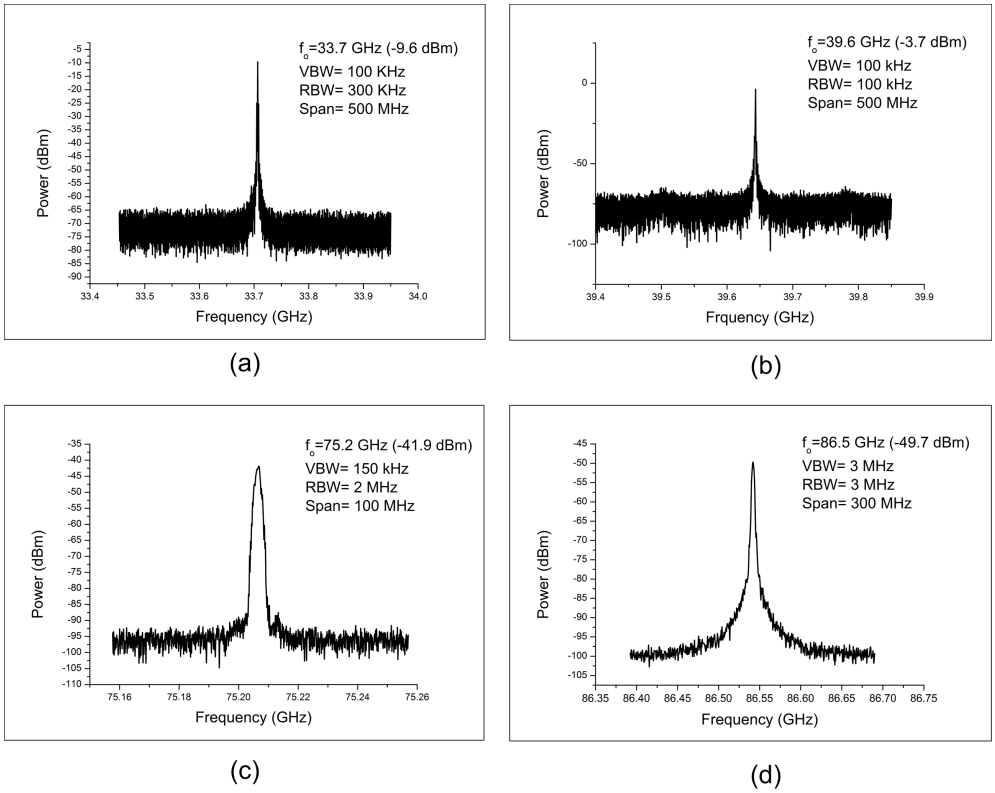


Figure 6.11: *Measured spectrum of the double oscillator (type II). (a) 33.7 GHz (-9.6 dBm) double RTD* ($4 \times 4\ \mu m^2$) , $V_{bias} = 1.65\ V$, $I_{bias} = 172.6\ mA$, *VBW=100 kHz, RBW=300 kHz. Span=500 MHz. (b) 39.6 GHz (-3.7 dBm) double RTD* ($4 \times 4\ \mu m^2$) , $V_{bias} = 1.70\ V$, $I_{bias} = 216.9\ mA$, *VBW=100 kHz, RBW=100 kHz. Span=500 MHz. (c) 75.2 GHz (-41.9 dBm*) double RTD* ($4 \times 4\ \mu m^2$) , $V_{bias} = 1.74\ V$, $I_{bias} = 230.9\ mA$, *VBW=150 kHz, RBW=2 MHz. Span=100 MHz. (d) 86.5 GHz (-49.7 dBm*) double RTD* ($5 \times 5\ \mu m^2$) , $V_{bias} = 1.58\ V$, $I_{bias} = 200.2\ mA$, *VBW=3 MHz, RBW=3 MHz. Span=300 MHz. *Note: For frequencies over 50 GHz, mixers were utilized to extend the frequency range of the spectrum analyser. As the loss of the mixer was not calibrated, the actual power were measured by power meter with its value shown in Table 6.3*

.

A summary of these measurement results is tabulated in Table 6.3. For frequencies below 50 GHz, the measured output power was compensated by the probe and cable loss. For frequencies above 50 GHz, as the external mixer was involved in the measurement, of which the insertion loss was not calibrated, the actual power was therefore, measured by a power meter (Agilent 437B) in com-

bination with W-band power sensor (Agilent W8486A). The probe/cable loss at 34 GHz and 40 GHz was 1 dB/3.1 dB and 1 dB/2.6 dB, respectively. The total loss at 75 GHz and 86 GHz including the mixer loss was 40.7 dB and 44.1 dB, respectively. The calibrated power shown in Table 6.3 took these losses into account. The measurement and calibration details were given in Appendix C.

It can be noted that all the oscillators operating from 33.7 GHz to 86.5 GHz presented relatively high output power, especially the 75.2 GHz double RTD oscillator employing two RTDs, each with a mesa size of $4 \times 4\mu m^2$, delivering -0.2 dBm (0.96 mW) output power, which is the highest power reported for an RTD oscillator operating in W-band to date. It can also be noted in Table 6.3 that the DC-RF conversion efficiency was under 2.2%. The reasons for this low efficiency include high contact resistance (the specific contact resistance which was 175.6 $\Omega\mu m^2$ for the emitter and 122.1 $\Omega\mu m^2$ for the collector) and the impedance mismatch between the oscillator and the 50Ω load.

6.3.3 Discussion

To design an RTD oscillator with frequency f_o, the length of CPW l is determined by the resonance condition (Equation 4.11) and the shorted CPW stub (Equation 4.14). The equations are repeated here:

$$f_o = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}}$$

$$l = \frac{C_0}{w_o\sqrt{\varepsilon_{eff}}} arctan\left[\frac{Z_0 w_o(L_{eq} - L_{sc})}{(Z_0^2 + w_o^2 L_{eq}L_{sc})}\right]$$

The CPW length l versus frequency f_o is plotted in Figure 6.12. The blue solid line represents the double RTD oscillator employing two 4×4 μm^2 RTDs while the black solid line represents the oscillator employing two large size 5×5 μm^2 RTDs. Measurement results shown in Table 6.3 are also plotted in Figure 6.12 for comparison. The oscillators employing two 4×4 μm^2 RTDs are plotted in a

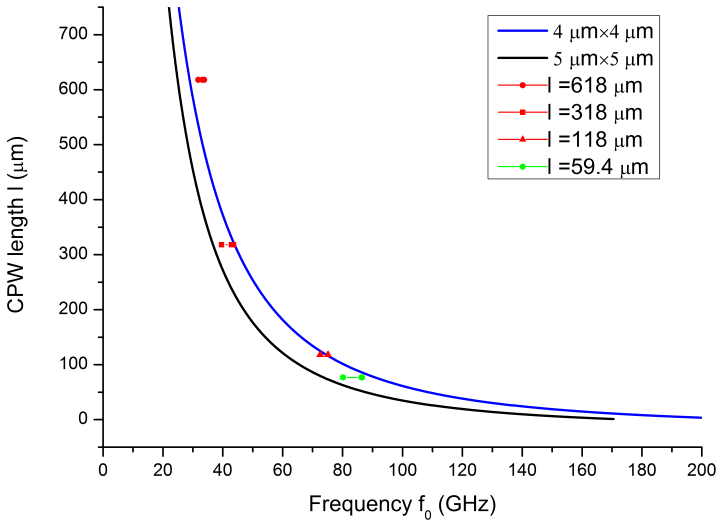


Figure 6.12: *The calculated CPW length l versus frequency f_o, compared with the measurement results.*

red line while those employing 5×5 μm^2 RTDs are plotted in a green line. Since the capacitance of a specific RTD changes with the bias voltage [141] [148], voltage controlled oscillation (VCO) was also observed. Thus in the plot, oscillators with the same CPW length possess multiple frequency values. The difference between theoretically calculated oscillator frequencies and measurement results can be observed in the plot. The reasons for the differences include the assumption that the self-capacitance C_n was constant, which we know not to be true, and not taking into account the quantum well inductance(L_{qw}), which is attributed

to the charging and discharging of the quantum well [139] [141]. The decoupling MIM capacitor C_e is also not ideal and influences the oscillation frequency. The reactance of C_e may not be ignored at the oscillation frequencies. For the type II oscillator layout, the CPW was terminated with 300 $\mu m \times 200$ μm MIM capacitor. In this case, the length of the shorted CPW becomes difficult to determine accurately because its length is comparable to the size of the MIM capacitors. These probable reasons lead to the difference between simulations and experiments.

As discussed in Chapter 5, to obtain the maximum output power, theoretically the RTD negative conductance G_n and the load (the input impedance of a spectrum analyser) conductance $G_L = 0.02$ should satisfy $G_L = \frac{G_n}{2}$. From Table 6.1, it is noted that for a single 4×4 μm^2 RTD device, $G'_n = 0.01$ S. As two single devices were connected in parallel in the circuit topology, the equivalent conductance $G_n = 2G'_n = 0.02 < 2G_L$. Higher output power are expected with the circuit improvement by matching the impedance.

6.4 Summary

In this chapter, the measured I-V characteristic of single RTD devices were investigated. The average peak current density was $J_p \approx 60\ kA/cm^2$ and the peak to valley current ratio (PVCR) was about 2.41. Double RTD MMIC oscillators with two different layouts, type I and type II, were characterized. The best result obtained was 75.2 GHz double RTD oscillator with -0.2 dBm (0.96 mW) output power, which to the author's knowledge, is the highest power reported for an RTD oscillator operating in W-band to date. However the DC-RF conversion efficiency of the oscillators presented in this thesis is very low. It is expected that

the efficiency can be increased by reducing the contact resistance and matching the oscillator to the load impedance. Higher output power at millimeter-wave and possibly at THz frequencies can be expected with improved circuit design and implementation.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

The resonant tunnelling diode (RTD) oscillator is considered to be one of the most promising solid-state terahertz sources which can operate at room temperature. Theoretically the RTD oscillator can operate up to 2.5 THz [36]. Up to now, the terahertz RTD oscillator has been realized at 1.1 THz (0.1 μW) [37]. However the biggest limitation of a RTD oscillator is its low power. The purpose of this PhD project was to realize an MMIC RTD oscillator with frequency up to 100 GHz with around a milli-Watt output power.

The results achieved in this project are as follows:

I. A 75.2 GHz oscillator with -0.2 dBm (0.95 mW) output power (oscillator type II) and an 86.5 GHz oscillator with -4.6 dBm (0.34 mW) (oscillator type II), where both oscillators employed two RTDs in parallel with each device biased individually, were demonstrated. This is the highest power obtained for RTD oscillator operating in W-band frequency range. Type I oscillator operating at 28 GHz with -0.7 dBm output power has been

published [147]. Theoretical analysis in Chapter 3 indicates that with fixed device sized ($4 \times 4\ \mu m^2$), the oscillator frequency can be raised up to 200 GHz with further reducing the CPW length down to 20 μm (Figure 6.12), and the calculated power would be around 1.7 mW at 200 GHz (Figure 5.7). Higher frequency in THz range can also be obtained by reducing the CPW length in combination with smaller device sizes.

II. A reliable RTD fabrication process with very high yield (90 %) was developed. As the device size shrinks down to a few microns, the fabrication process (especially the via opening over the passivation layer) utilizing photo-lithography becomes difficult. PI-2545 polyimide was chosen as a passivation layer due to its low dielectric constant, which is desirable for high frequency applications. The choice and the profile of the drying etching mask, the thickness of PI-2545 and of the mask depending on the spin speed, the separate dry etching speed, and the composition of dry etching gas have all been carefully investigated and optimum conditions were established. A dry etching process for the PI-2545 polyimide with smooth edge profiles was developed on this project.

III. A self-consistent numerical model based on the physics of resonant tunnelling was developed and implemented in MATLAB software [154]. The model involves using the Airy function to obtain an accurate transmission coefficient for electrons tunnelling through the barrier and the consideration of potential shift due to free charge distribution.The model is expected to serve to optimize the RTD structure for terahertz applications.

7.2 Future Work

7.2.1 Higher Frequency with High Power

As described in Chapter 3, for a given RTD with fixed device size, the oscillation frequency can be further increased by reducing the CPW length, the frequency of two RTD oscillators with mesa size 16 μm^2 is expected to be over 200 GHz. Instead of reducing the length of CPW, the self-capacitance of the RTD device can also be reduced by employing a smaller mesa size device. Combining these two methods, the frequency of two RTD oscillators is expected to be greatly increased while keeping the output power high. For present oscillator layouts (type I and type II), the main consideration employing multiple RTD devices is the space limitation. New MMIC oscillator layout employing more than two RTDs need to be developed in the future. It is also noted in the project that the contact resistance is relatively high which degrades the oscillator performance in terms of both the frequency and output power. Further research should optimize the fabrication process to obtain low series contact resistance.

7.2.2 Device Fabrication

The minimum size of the fabricated RTD in this project was 3×3 μm^2. To design very high frequency (THz) RTD oscillator, smaller sized devices with low self-capacitances will be required. E-beam lithography will have to be employed because the small features are beyond the resolution of traditional optical lithography. Also, the wet etching process may not be suitable for small devices because the etching undercut profile may destroy the device which would severely reduce

the effective device size. Dry etching will be the preferable etching technique for sub-micron devices.

7.2.3 Device Characterisation

The proper oscillator circuit design requires a scalable RTD equivalent circuit model incorporated with computer-aided design (CAD) software. As an RTD can be stabilized in the NDR region by employing a shunt resistor, it is possible to extract the small signal model by S-parameter measurement without the interference of the bias oscillation. The current RTD small signal model underestimates the device self-capacitance (C_n). A more accurate model is required to help with RTD oscillator design in the future.

Appendix A. Fabrication Process

Sample cleaning

1. Ultrasonic bath in acetone for 3 minutes
2. Ultrasonic bath in methanol for 3 minutes
3. Ultrasonic bath in IPA for 3 minutes
4. Rinse in de-ionised (DI) water for 3 minutes
5. Blow Dry with N_2

Collector

1. Spin primer at 4000 rpm for 5 seconds
2. Spin S1805 at 4000 rpm for 30 seconds
3. Bake on hotplate at 115 °C for 1 minutes
4. Post-develop in 1:1 MDC:H_2O for 60 seconds
5. Rinse in DI water for 1 minute
6. Bake on hotplate at 90 °C for 2 minutes

7. Expose by MA6 for 1.5 seconds
8. Develop in 1:1 MDC:H_2O for 50 seconds
9. Rinse in DI water for 3 minutes
10. Blow dry with N_2
11. Ash at 140W for 2 minutes
12. Deposit ohmic contact Ti/Pd/Au 20/30/100 nm
13. Lift off in acetone at 50 °C for 30 minutes
14. Rinse in DI water for 5 minutes
15. Blow dry with N_2

Etch to emitter layer

1. Spin primer at 4000 rpm for 5 seconds
2. Spin S1805 at 4000 rpm for 30 seconds
3. Bake on hotplate at 115 °C for 1 minute
4. Expose by MA6 for 1.5 seconds
5. Develop in 1:1 MDC:H_2O for 50 seconds
6. Blow dry with N_2
7. Ash at 140W for 2 minutes
8. Dip in H_3PO_4:H_2O_2:H_2O=1:1:38 etchant for 5 minutes

9. Rinse in DI water for 3 minutes
10. Blow dry with N_2

Emitter

1. Spin primer at 4000 rpm for 5 seconds
2. Spin S1805 at 4000 rpm for 30 seconds
3. Bake on hotplate at 115 °C for 1 minute
4. Post-develop in 1:1 MDC:H_2O for 60 seconds
5. Rinse in DI water for 1 minute
6. Bake on hotplate at 90 °C for 2 minutes
7. Expose by MA6 for 1.5 seconds
8. Develop in 1:1 MDC:H_2O for 50 seconds
9. Rinse in DI water for 3 minutes
10. Blow dry with N_2
11. Ash at 140W for 2 minutes
12. Deposit ohmic contact Ti/Pd/Au 20/30/100 nm
13. Lift off in acetone at 50 °C for 30 minutes
14. Rinse in DI water for 5 minutes
15. Blow dry with N_2

Etch to substrate

1. Spin primer at 4000 rpm for 5 seconds
2. Spin S1805 at 4000 rpm for 30 seconds
3. Bake on hotplate at 115 °C for 1 minute
4. Expose by MA6 for 1.5 seconds
5. Develop in 1:1 MDC:H_2O for 50 seconds
6. Blow dry with N_2
7. Ash at 140W for 2 minutes
8. Dip in H_3PO_4:H_2O_2:H_2O=1:1:38 etchant for 5 minutes
9. Rinse in DI water for 3 minutes
10. Blow dry with N_2

Passivation

1. Dispense VM651:H_2O=1:999 on sample and hold for 20 seconds
2. Spin at 3000 rpm for 30 seconds
3. Spin polyimide PI2545 at 8000 rpm for 30 seconds
4. Bake in 180 °C oven for 6 hours

Via opening

1. Spin primer at 4000 rpm for 5 seconds

2. Spin S1805 at 1500 rpm for 30 seconds
3. Bake on hotplate at 115 °C for 2 minutes
4. Expose by MA6 for 2.2 seconds
5. Develop in 1:1 MDC:H_2O for 50 seconds
6. Blow dry with N_2
7. Bake on hotplate at 115 °C for 10 minutes
8. Etch by CF_4/O_2 in 80 plus RIE for 5 minutes
9. Strip S1805 in 1165 photoresist stripper at 50 °C for 20 minutes
10. Rinse in DI water
11. Blow dry with N_2

Film resistor

1. Spin S1818 at 4000 rpm for 30 seconds
2. Bake on hotplate at 90 °C for 3 minutes
3. Dip in Chlorobenzene for 8 minutes
4. Blow dry with N_2
5. Expose by MA6 for 5.5 seconds
6. Develop in 1:1 MDC:H_2O for 50 seconds
7. Rinse in DI water for 3 minutes

8. Blow dry with N_2
9. Ash at 180W for 5 minutes
10. Dip in HCL:H_2O=1:10 for 20 seconds
11. Deposit thin film resistor NiCr 33 nm
12. Lift off in acetone at 50 °C for 20 minutes
13. Rinse in DI water for 5 minutes
14. Blow dry with N_2

Bond pad and CPW

1. Spin LOR 10A at 6000 rpm for 30 seconds
2. Bake on hotplate at 150 °C for 3 minutes
3. Spin S1818 at 4000 rpm for 30 seconds
4. Bake on hotplate at 115 °C for 3 minutes
5. Expose by MA6 for 6 seconds
6. Develop in MF319 for 2.5 minutes
7. Rinse in DI water for 3 minutes
8. Blow dry with N_2
9. Ash at 180W for 1 minutes
10. Deposit contact metal Ti/Al/Ti/Au 25/195/30/250 nm

11. Lift off in acetone at 50 °C for 20 minutes
12. Rinse in DI water for 3 minutes
13. Dip in 1165 photoresist stripper at 50 °C for 30 minutes
14. Rinse in DI water for 5 minutes
15. Blow dry with N_2

SiN insulator

1. Spin S1818 at 4000 rpm for 30 seconds
2. Bake on hotplate at 90 °C for 3 minutes
3. Dip in Chlorobenzene for 8 minutes
4. Blow dry with N_2
5. Expose by MA6 for 5.5 seconds
6. Develop in 1:1 MDC:H_2O for 50 seconds
7. Rinse in DI water for 3 minutes
8. Blow dry with N_2
9. Ash at 140W for 3 minutes
10. Deposit SiN 75 nm by ICP-CVD
11. Lift off in acetone at 50 °C for 30 minutes
12. Rinse in DI water for 5 minutes

13. Blow dry with N_2

Bond pad

1. Spin LOR 10A at 6000 rpm for 30 seconds
2. Bake on hotplate at 150 °C for 3 minutes
3. Spin S1818 at 4000 rpm for 30 seconds
4. Bake on hotplate at 115 °C for 3 minutes
5. Expose by MA6 for 6 seconds
6. Develop in MF319 for 2.5 minutes
7. Rinse in DI water for 3 minutes
8. Blow dry with N_2
9. Ash at 180W for 1 minute
10. Deposit contact metal Ti/Al/Ti/Au 25/195/30/250 nm
11. Lift off in acetone at 50 °C for 20 minutes
12. Rinse in DI water for 3 minutes
13. Dip in 1165 photoresist stripper at 50 °C for 30 minutes
14. Rinse in DI water for 5 minutes
15. Blow dry with N_2

Appendix B. Relaxation Oscillations

One of the reasons for the limited output power of RTD oscillators is the undesired low frequency relaxation-oscillations. These low frequency oscillations have been known for a long time and are described in various places [38,140,155–157]. It is important to review these oscillations here briefly for completeness. Figure 1 shows the RTD device with the biasing connected, where R_b,L_b denote the resistance and inductance arising from the bias cable, $-R_n$ and C_n represent the negative differential resistance and self-capacitance of the RTD. According to

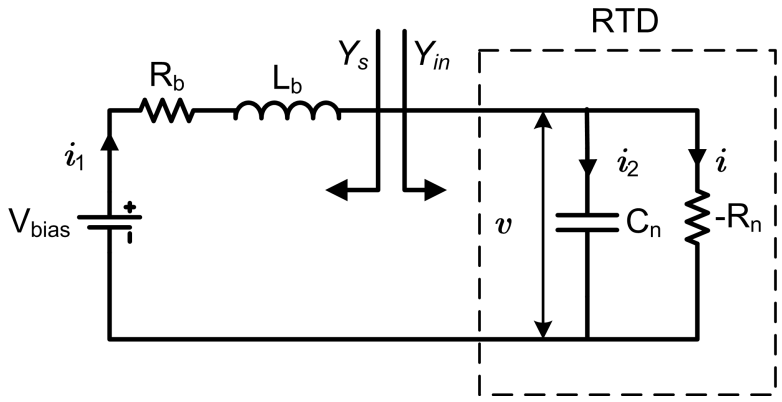


Figure 1: *The RTD device biasing schematic circuit, where RTD is represented by its small signal model.*

Kirchhoff's circuit laws, the schematic circuit in Figure 1 can be described by

$$V_{bias} - i_1 \times R_b - L_b \frac{di_1}{dv} - v = 0 \tag{1a}$$

$$i_1 = i_2 + i \tag{1b}$$

as

$$i_2 = C_n \frac{dv}{dt} \tag{2}$$

$$i = -\frac{v}{R_n} \tag{3}$$

Equation (1b) becomes

$$i_1 = C_n \frac{dv}{dt} + -\frac{v}{R_n} \tag{4}$$

Substitute Equation (4) back to Equation (1a) gives

$$L_b C_n \frac{d^2v}{dt^2} + \frac{dv}{dt}(C_n R_b - \frac{L_b}{R_n}) + v(1 - \frac{R_b}{R_n}) - V_{bias} = 0 \tag{5}$$

The general solution of Equation (5) is

$$v = A_1 e^{\lambda_1 t} + A_2 e^{\lambda_2 t} + \frac{V_{bias} R_n}{R_n - R_b} \tag{6}$$

where A_1, A_2 are two constants depending on the initial condition. The two characteristic roots λ_1, λ_2 are

$$\lambda_{1,2} = \frac{1}{2}(\frac{1}{C_n R_n} - \frac{R_b}{L_b}) \pm \sqrt{\frac{1}{4}(\frac{1}{R_n C_n} - \frac{R_b}{L_b})^2 - \frac{1}{L_b C_n}(1 - \frac{R_b}{R_n})} \tag{7}$$

When the inductance L_b is relatively large, the real part of the roots is positive, and a square wave-like oscillation (relaxation oscillation) is presented along in the circuit, i.e. along the bias line.

The relaxation oscillation was measured by a Tektronix DPO 4054 Phosphor Oscilloscope. The schematic measurement circuit is shown in Figure 2, where R_b, L_b denote the resistance and inductance of the bias cable, respectively. R_L is the input impedance of the oscilloscope (usually 50 Ω). L denotes the inductor arising from the coaxial cable (60 cm length) connecting the RF probe and the bias-tee. When $V_{bias} = 1.6\ V$, $i = 10.2\ mA$, the measurement result is shown in

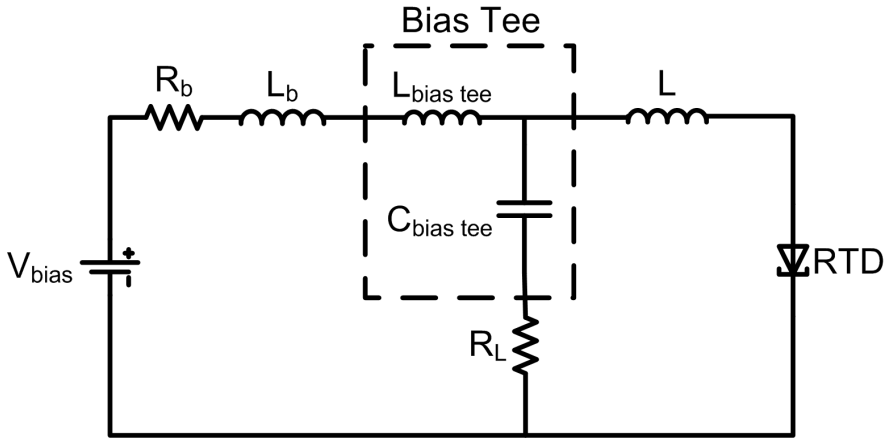


Figure 2: *Relaxation-Oscillation measurement circuit. The bias voltage was applied though a bias-tee. The inductance L arises from the cable connecting between the RF probe and a bias-tee.*

Figure 3. The square wave oscillation is presented. The time interval $T_1 \approx 3\ nS$, $T_2 \approx 1.5\ nS$, $T_3 \approx 7\ nS$, $T_4 \approx 1.4\ nS$.

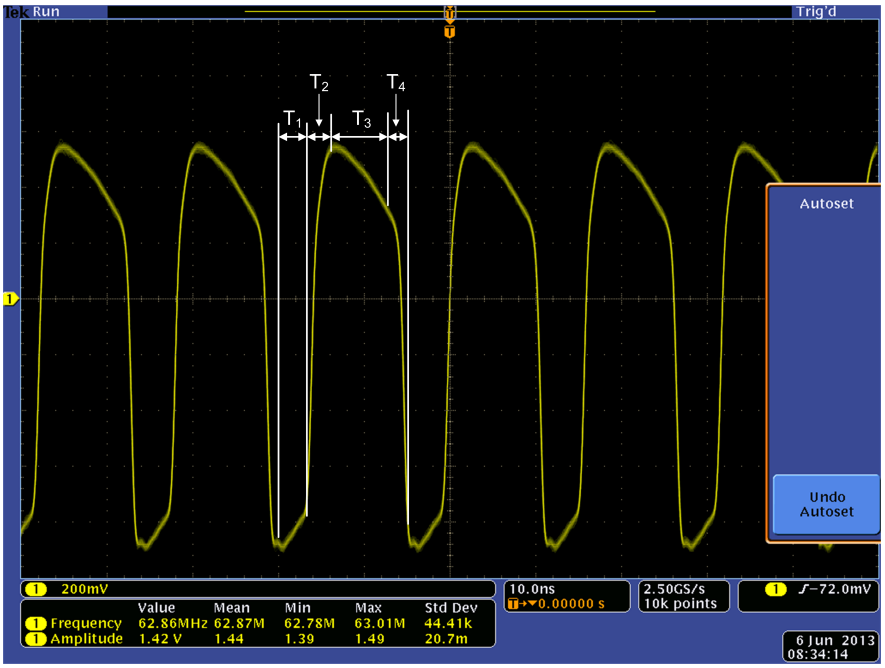


Figure 3: *Relaxation oscillation was measured by Tektronix DPO 4054 Phosphor Oscilloscope. When* $V_{bias} = 1.6\ V$, $i = 10.2\ mA$, *the RTD device* ($5 \times 5\ \mu m^2$) *was biased in NDR region. The measured frequency was about 62.8 MHz.*

Appendix C. Oscillator Frequency and Power Measurement

Oscillator Frequency Measurement

The frequency range of the commercial spectrum analyser, the E4448A from Agilent Technologies, is from 3 Hz up to 50 GHz with $\pm 0.19\ dB$ amplitude accuracy, and $-154\ dBm$ displayed average noise level [158]. For frequencies over 50 GHz an external mixer is utilized to expand the frequency coverage by down-converting the measured frequencies. A block diagram of this measurement set-up is shown in Figure 4(a), where the mixer is placed between the device under test (DUT) and the spectrum analyser. The most common mixer-spectrum analyser measurement is made by using fundamental mixing, where only the fundamental frequency of the local oscillator (LO) from a spectrum analyser is utilized. This approach offers many benefits such as high sensitivity and less extraneous signals. However, this approach is less desirable for high frequency measurement because the LO frequency must be of the same order or even much higher than the signal frequency, so the harmonic mixing method is utilized. Compared with fundamen-

tal mixing, the main benefits of harmonic mixing is that the high frequency can be down-converted by using the low frequency range of the LO. However there are some drawbacks such as the amplitude accuracy is reduced because of the variable conversion loss of the external mixer, the phase noise is increased so the frequency measurement accuracy is affected, and the cost and complexity of the measurement are also increased. The harmonic mixer utilized in this project is 11970W mixer from Agilent Technologies [159]. It covers the frequency range between 75 GHz and 110 GHz, i.e. W-band. Figure 4(b) shows a picture of the mixer within the measurement set up. The cascade ACP 110 GSG probe and the DUT can also be seen in this picture.

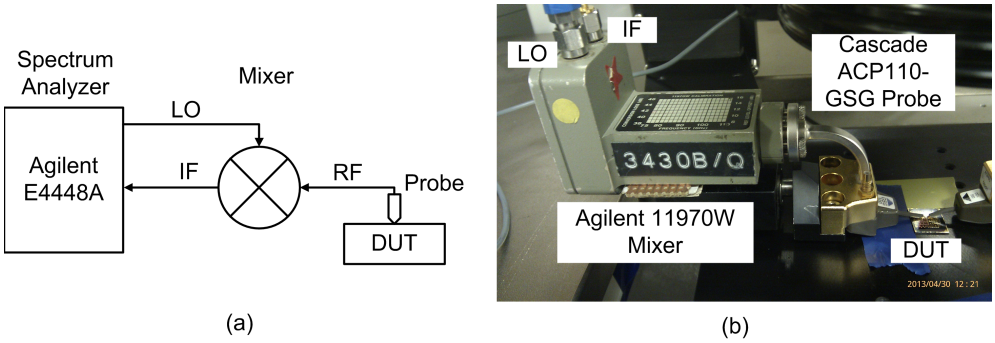


Figure 4: *Frequency spectrum measuring set-up. (a) Measurement block diagram. An external mixer is utilized to extend the frequency coverage. Depending on the mixer model and the architecture of the spectrum analyser, a diplexer is not always required. (b)W-band (75-110 GHz) frequency measurement utilizing 11970W harmonic mixer from Agilent. The probe employed is the 75-110 GHz waveguide Air Coplanar Probe (ACP) from Cascade Microtech.*

The mixer produces both sum and difference frequencies of LO and RF as shown in Equation 8, where n is the order of the harmonic of the local oscillator being used.

$$f_{IF} = nf_{LO} \pm f_{RF} \tag{8}$$

The desired intermediate frequency (IF) output is the difference frequency, which can be selected by low-pass filtering. In the E4448A, the fundamental frequency of the LO covers 2.85 to 6.9214 GHz at a power output level $16.5 \pm 2\ dBm$. The RF input signal is down-converted to 321.4 MHz IF signal by using harmonics of the LO [158]. With the harmonic number n ranging from 14 to 18, the mixer can cover the frequencies range from V-band (50-75 GHz) to W-band (75-110 GHz) [159].

From Equation 8, for a given RF input signal, the down-converted output IF is given by

$$f_{IF} = nf_{LO} - f_{RF} \tag{9}$$

Therefore the input RF signal can be represented by

$$f_{RF} = nf_{LO} - f_{IF} \tag{10}$$

Now considering the input RF signal

$$f'_{RF} = nf_{LO} + f_{IF} \tag{11}$$

the mixer output IF yields

$$f'_{IF} = -f_{IF} \tag{12}$$

Mathematically this frequency is identical to f_{IF} because the Fourier spectrum of any real signal is symmetric about zero frequency. The f'_{RF} signal is the image signal. In external mixing, all true signals come with an image to form a pair. To distinguish the true signal from the image signal, the E4448A spectrum analyser

shifts the LO by the image shift function [160].

Each mixer covers a specified frequency band. For example, WHMP-15 harmonic mixer from Farran Technology provides suitable measurement for V-band (50 GHz - 75 GHz). The typical conversion loss of the WHMP-15 is 25 dB [161]. For frequencies located in W-band (75-110 GHz), the 11970W harmonic mixer from Agilent Technologies is designed to cover this frequency range. The typical conversion loss is 46 dB [159]. By choosing the external mixers, the conversion loss must be properly calibrated in order to assure measurement accuracy.

Oscillator Power Measurement

The RF signal power can be measured by either a spectrum analyser or a power meter. In this project, both approaches were utilized. For frequencies below 50 GHz, the oscillator output power was measured directly by the spectrum analyser, the E4448A. To ensure the measurement accuracy, the system loss, including the insertion loss of the probe (P_{probe_loss}), the transmission loss of the cable (P_{cable_loss}), need to be compensated by using Equation 13, where real output power (P_{real}) is the compensated power, and $P_{measure}$ is the measured power from a spectrum analyser.

$$P_{real} = P_{measure} + P_{probe\_loss} + P_{cable\_loss} \tag{13}$$

In this project, the cable loss was calibrated by a standard signal source, the Wiltron 68187B with a frequency range from 10 MHz to 60 GHz. The cable to be calibrated is connected between the standard source and spectrum analyser. At one end, the source delivers a signal with known power at fixed frequency through the cable. At the other end, the signal is measured by a spectrum

analyser. The difference between the output power from the source and the measured power from the spectrum analyser is the cable loss. There were four different coaxial cables with a core diameter of 1.85 mm calibrated, the Aspen cable 1 and 2 with the same length (24-inch) from Advanced Technical Materials Inc., the V086MMHF-36D (36-inch long) and V086MMHF-24D (24-inch long) from RF Coax Inc. The transmission loss is shown in Figure 5 for frequencies between 26 GHz and 50 GHz.

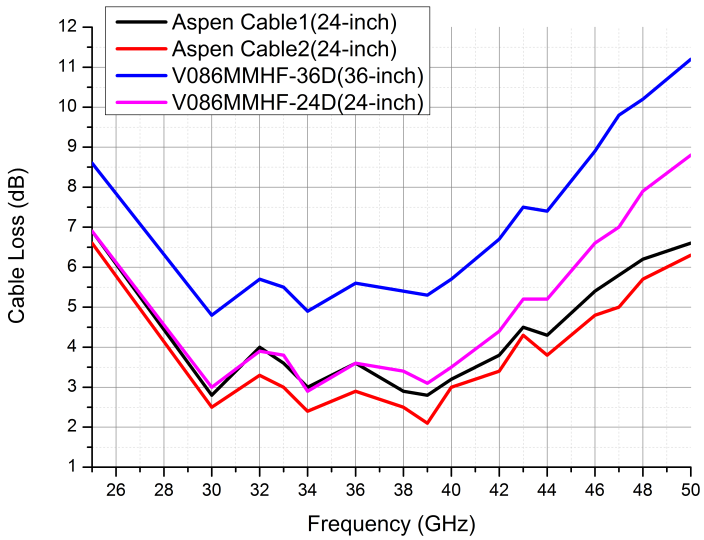


Figure 5: *The loss of various mm-wave cables*

The ACP65-GSG probe from Cascade Microtech was utilised to probe the DUT and to measure signals from DC up to 65 GHz. The minimum pad size for good contact is 80 $\mu m \times 80\ \mu m$, the maximum allowed DC current is 5 A, and the typical insertion loss is 1∼2 dB [162]. For the ACP110-GSG probe also from Cascade Microtech, which was utilized for W-band measurement, the minimum pad size for good contact is 80 $\mu m \times 80\ \mu m$, the maximum allowed DC current

is 0.50 A, and the typical insertion loss is 1∼2 dB [128] [163].

For high frequencies above 50 GHz in our case, an external mixer has to be employed as described before. Therefore the conversion loss of the mixer must be compensated when measuring the power. As the conversion loss of a mixer is frequency and (RF/LO) power dependant [128] [164], the mixer calibration is not easy to implement in the laboratory and so the loss specified by the manufacturer was used in our measurements. The typical conversion loss of W-band (75 GHz to 110 GHz) mixer, the 11970W provided by Agilent Technologies, is shown in Figure 6 for the 18-110 GHz range. The maximum conversion loss for 11970W is 46 dB in the W-band [159].

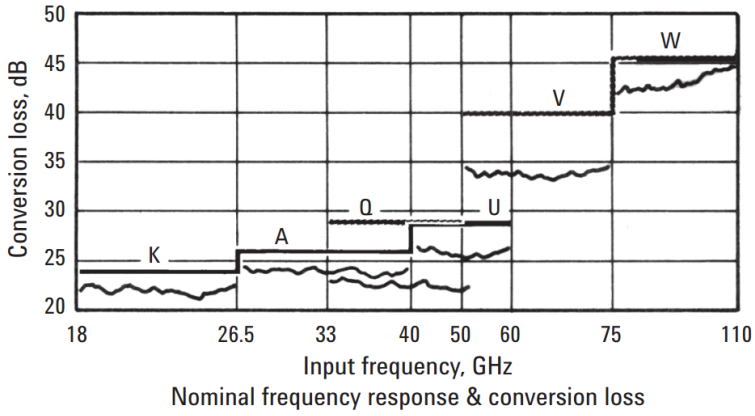


Figure 6: *Agilent 11970 series mixer conversion loss [159] .*

Alternatively, a power meter provides a simple way to measure the RF power. The actual output power of the fabricated oscillators was measured by a power meter in combination with a spectrum analyser, where possible, to inspect the signal spectrum simultaneously. The Agilent 437B power meter combining with W8486A Waveguide power sensor covers the frequency ranging from 75 GHz

to 110 GHz with an average power between -30 dBm to +20 dBm [165]. The measurement block diagram is shown in Figure 7 and the actual equipment set up is shown in Figure 8.

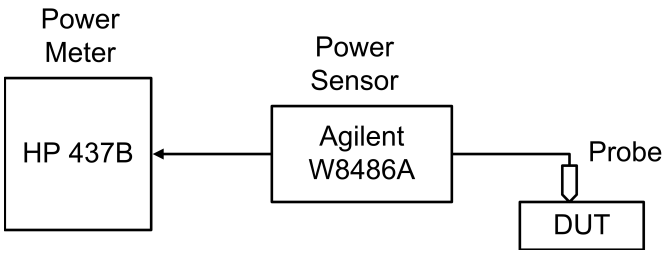


Figure 7: *High frequency (75 GHz-110 GHz) power measurement block diagram by using HP 437B power meter in combination with Agilent W8486A waveguide power sensor.*

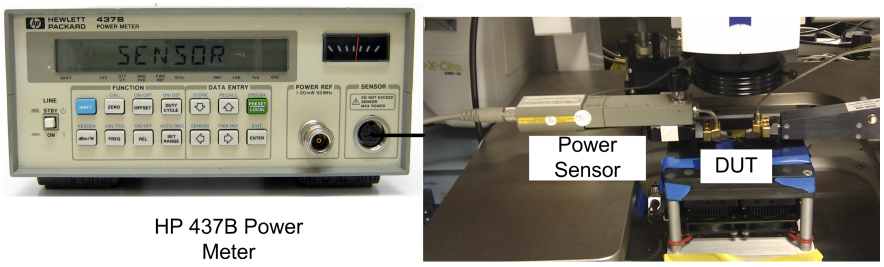


Figure 8: *Power measurement by using HP 437B power meter.*

Appendix D. List of Symbols

ADS2009 Advanced Design System 2009

CAD Computer Aid Design

CMOS Complementary Metal Oxide Semiconductor

CPW Coplanar Waveguide

CRM Cyclotron Resonance Maser

DBQW Double Barriers Quantum Well

DI De-Ionised

EBPVD Electron Beam Physical Vapor Deposition

FET Field Effect Transistor

FIR Far-InfraRed

FOM Figure of Merit

GSG Ground Signal Ground

HEMT High Electron Mobility Transistor

ICP-CVD Inductively Coupled Plasma Chemical Vapour Deposition

IF Intermediate Frequency

IMPATT Impact Ionization Transit time

JWNC James Watt Nanofabrication Center

LO Local Oscillator

LOR Lift Off Resist

MBE Molecular Beam Epitaxy

MMIC Monolithic Microwave Integrated Circuit

MOCVD Metal Organic Chemical Vapour Deposition

MOSFET Metal Oxide Semiconductor Field Effect Transistor

NDR Negative Differential Resistance

PECVD Plasma Enhanced Chemical Vapor Deposition

PVCR Peak to Valley Current Ratio

QCL Quantum Cascade Lasers

RBW Resolution Bandwidth

RIE Reactive Ion Etching

RMSE Root Mean Squared Error

RTD Resonant Tunnelling Diode

SEM Scanning Electron Microscope

TCR Temperature Coefficient of Resistance

THz Terahertz

TLM Transmission Line Model

TMM Transfer Matrix Method

TUNNETT Tunnel Injection Transit Time

VBW Video Bandwidth

VNA Vector Network Analyser

Physical Constants

$\epsilon_0 = 8.85 \times 10^{-12} F/m$ Vacuum permittivity

$\hbar = 1.05 \times 10^{-34} Js$ Reduced Plank constant

$\mu_0 = 4\pi \times 10^{-7}\ H/m$ Vacuum permeability

$\rho_{Au} = 2.44 \times 10^{-8}\ \Omega m$ Gold resistivity

$c_0 = 3 \times 10^{8}\ m/s$ Velocity of light in free space

$e = 1.60 \times 10^{-19} C$ Elementary charge

$m_0 = 9.11 \times 10^{-31} kg$ Electron rest mass

Chemicals

Al Aluminium

AlAs Aluminium Arsenide

AlSb Aluminium Antimonide

As Arsenic

C_6H_5Cl Chlorobenzene

CH_4 Methane

CO_2 Carbon Dioxide

Cr Chromium

Ga Gallium

GaAs Gallium Arsenide

H_2 Hydrogen

HCL Hydrogen Chloride

In Indium

InAlAs Indium Aluminium Arsenide

InGaAs Indium Gallium Arsenide

InP Indium Phosphide

NH_4OH Ammonium Hydroxide

P Phosphorus

Si Silicon

Si_3N_4 Silicon Nitride

SiO_2 Silicon Dioxide

Symbols

ΔE_c Conduction band offset

ϵ_r Relative dielectric constant

ρ_C Specific contact resistance($\Omega \mu m^2$)

$\Psi(x,t)$ Time dependant wave function

J_p Peak current density

m^* Electron effective mass

R_{sh} Sheet resistance($\Omega/\square$)

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