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Switched-Current Filtering Systems: Design, Synthesis and Software Development

A Thesis submitted to the
Faculty of Engineering
of the University of Glasgow
for the degree of
Doctor of Philosophy

by

ANDREW NG ENG JWEE
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SUMMARY

The scope of this thesis covers aspects of the design and synthesis of different switched-current filtering systems and their implementation into the filter and equaliser compiler XFILT. Previous work on matrix-based design of SI filters was focused mainly on general Left and Right decomposition structures of modest order. This has been extended to include other decompositions, namely the LU-UL and UL-LU decompositions, which have shown potential for wideband applications. The design of very high order filters constraints the choice of filter structure to that of a doubly-terminated ladder because of its inherent low passband sensitivity. Other factors that determine the feasibility of a design include the component value spread and total circuit size or area. A prototype manipulation scheme that is applicable to matrix-derived bilinear-LDI type filters has been exploited to design very high order SI filters with effective reductions in spreads and area. For the designed example of a 21st order lowpass filter, a remarkable reduction in spread and area of 99.94% and 99.83% respectively was achieved. Modifications to the general Left and Right decomposition structures also yielded simple input circuitry and avoided a dynamic-range scaling problem inherent to Right decomposition structures.

Allpass filters are commonly employed in many applications to perform group delay equalisation in the passband. They are non-minimum phase by definition and are characterised by poles and zeros in mirror-image symmetry. SI allpass filters of both cascade biquad and bilinear-LDI ladder types have been in existence. These were implemented using Euler based integrators. Cascade biquads are known to have highly sensitive amplitude responses and Euler integrators suffer from excess phase. The equalisers that are proposed here are based on bilinear integrators instead of Euler ones. Derivation of these equalisers can proceed from either the s-domain, or directly from the z-domain, where a prototype is synthesised using the respective continued-fractions expansions, and simulated using standard matrix methods. The amplitude response of the bilinear allpass filter is shown to be completely insensitive to deviations in the reactive ladder section. Simulations of sensitivities and non-ideal responses reveal the advantages and disadvantages of the various structures.

Existing SI multirate filters have to date been implemented as direct-form FIR and IIR polyphase structures, or as simple cascade biquad or ladder structures with non-optimum settling times. FIR structures require a large number of impulse coefficients to realise highly selective responses. Even in the case of linear phase response with symmetric impulse coefficients, when the number of coefficients can be halved, significant overheads can be incurred by additional multiplexing circuitry. Direct-form IIR structures are simple but are known to be sensitive to coefficient deviations and structures with non-optimum settling times operate entirely at the higher clock frequency. The novel SI decimators and interpolators proposed are based on low sensitivity ladder structures coupled with FIR polyphase networks. They operate entirely at the lower clock frequency which maximises the time available for the memory cells to settle. Two different coupling architectures with different advantages and disadvantages are studied.

Finally, novel SI N-path and pseudo-N-path circuits are introduced. These are based on fully-balanced structures that perform the $z \rightarrow -z$ lowpass-to-highpass, and $z \rightarrow -z^2$ lowpass-to-bandpass transformation respectively. The pseudo-N-path cells operate on the circulating-delay principle, which avoids clock-feedthrough noise in the passband and generation of mirror-frequency components. In addition, the centre of the passband is fixed at a quarter of the clock frequency, providing frequency stability for narrow bandpass responses. Various non-ideal effects on the frequency responses are analysed and simulated. Comparisons of sensitivity and mirror-frequencies rejection are also made between the proposed structures and a direct narrowband bandpass filter.

ACKNOWLEDGMENTS

First and foremost, I would wish to express my gratitude and thanks to my supervisor Prof. John I. Sewell for giving me the opportunity to undertake this research. In these three years, he has given me much support and encouragement during the many high and low moments experienced. He has always been approachable and available when guidance was needed, and above all, freedom was given to explore the different avenues of interest.

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The smooth running of the workstations and resolving of the many UNIX and software problems would not be possible without the tireless assistance of the computer support group headed by Dr. David Muir. In particular, the help rendered by Stephen Gallacher is greatly appreciated and acknowledged.

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I am greatly indebted to my parents for providing me with love, upbringing, and an education which has culminated in this present work. Special thanks is also due to my wife Joanne for her patient understanding and encouragement throughout the course of this work. It is to them that I dedicate this thesis.

TABLE OF CONTENTS

List of Abbreviations

AAF	Anti-Aliasing Filter
AC	Alternating Current
A/D	Analog/Digital
AIF	Anti-Imaging Filter
AMI	American Microsystems, Inc.
ASIMOV	A SI MOdule gereration enVironment
CAD	Computer Aided Design
CDS	Correlated Double Sampling
CFE	Continued Fractions Expansion
CFT	Clock Feed-Through
CMFB	Common Mode Feed Back
CMFF	Common Mode Feed Forward
CMOS	Complimentary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
D/A	Digital/Analog
DC	Direct Current
DFII	Direct Form II
DS	Double Sampling
FET	Field Effect Transistor
FFT	Fast Fourier Transform
FIC	FIR-IIR Cascade
FIR	Finite Impulse Response
HSPICE	H Simulation Program with Integrated Circuit Emphasis (Meta-Software)
IF	Intermediate Frequency
IFC	IIR-FIR Cascade
IIR	Infinite Impulse Response
LDI	Lossless Discrete Integrator
LHS	Left Hand Side
LTI	Linear Time Invariant
LTV	Linear Time Varying

MATLAB	MATrix LABoratory (The MathWorks, Inc.)
MFI	Multiple Feed In
MFO	Multiple Feed Out
MOS	Metal Oxide Semiconductor
NMOS	Negative-Metal Oxide Semiconductor
PLL	Phase Lock Loop
PMOS	Positive-Metal Oxide Semiconductor
QAM	Quadrature Amplitude Modulation
RBW	Relative Band-Width
RHS	Right Hand Side
SC	Switched Capacitor
SCADS	Switched Current Analog Design System
SCNAP4	Switched Circuit Numerical Analysis Program 4
SFG	Signal Flow Graph
SI	Switched Current
SPFT	Single Path Frequency Translated
SPICE	Simulation Program with Integrated Circuit Emphasis
SS	Single Sampling
SWITCAP	SWITched Capacitor Analysis Program
VHDL	VLSI Hardware Description Language
VLSI	Very Large Scale Integration
WDF	Wave Digital Filter
XFILT	X-windows FILTer and equaliser compiler

CHAPTER 1:
INTRODUCTION

1.1 MOTIVATION AND GENERAL AIM

1.2 OUTLINE OF THE THESIS

1.3 STATEMENT OF ORIGINALITY

REFERENCES

The trend towards mixed-signal or more generally system-on-chip designs has been driven mainly by two factors. Firstly, shrinking geometries of advanced digital processes allows ever increasing number of transistors to be packed onto a single chip. Secondly, the arrival of the multimedia revolution has seen a merging of product functionality, and the economic advantage to be gained from single chip solutions. However, it is the digital part which typically dominates and forms the core of the chip while analogue circuits have been relegated to the periphery[1]. Therefore, most analogue circuits perform interface and signal conditioning functions such as analog-to-digital, digital-to-analog conversion and filtering. As a result, many state-of-the-art processes are now optimised for digital circuits and as such, have only a single-poly layer and ever decreasing supply voltages. This makes integrating traditional voltage-mode analogue functions in digital processes increasingly difficult for several reasons. Firstly, the lowering of supply voltages directly affects the voltage swing and dynamic-range, and the need to drive load capacitances places a limitation on speed[1,2]. Secondly, as many analogue techniques rely on a matching of ratios to implement signal processing functions, the vastly reduced dimensions will aggravate the mismatch problem, diminishing the level of achievable accuracy. Thirdly, the availability of only one single-poly layer makes it extremely difficult realise highly linear, floating capacitances[1].

Switched-current[1] is a relatively new, current mode sampled-data technique that was originally conceived to make integration of analogue circuits fully compatible with advanced digital processes. No linear floating capacitors are required, only the parasitic gate-source capacitance of MOSFETs are needed to store voltages that define drain currents. Other advantages are the potential for high speed and low voltage operations. These are based on the premises that simple current mirror type circuits with low impedance and voltage nodes are used. Current-mode techniques are more favourable when capacitive loads are required to be driven at low voltage levels[2]. In addition, dynamic-range of current swings is only indirectly affected by the lowering of supply voltages[1]. To date, the switched-current technique has found diverse applications and much effort has also been directed towards minimising many non-ideal effects and problems.

1.1 MOTIVATION AND GENERAL AIM

The analog part of a typical mixed-mode chip design cycle has always been a bottleneck due to a lack of effective tools for analogue design. XFILT[5,6] is a design automation tool that synthesises filter and delay equalisers in various realisations such as passive RLC, active-RC, transconductance-C, switched-capacitor and switched-current. The aim of this thesis is to investigate and develop novel switched-current circuits and building blocks and to study their suitability as filtering systems for implementation into the filter and equaliser compiler XFILT[5,6]. These range from conventional filters targeted at high order and wideband applications, to delay equalisers, decimators, interpolators, N-path and pseudo-N-path filters.

1.2 OUTLINE OF THE THESIS

Chapter 2 begins with a brief introduction to the operating principles of switched-current circuits and describes both the first and second generation memory cells[1]. Various non-ideal factors that affect the performance of practical circuits are briefly outlined. A review of advances in memory cell design is then given, where the memory cells are organised by techniques employed to eliminate clock-feedthrough/charge injection. Next, SI systems are reviewed where particular emphasis is placed on filtering systems given their relevance to the context of this thesis. The chapter ends with a brief introduction and review of the few existing switched-current design automation tools and XFILT.

Chapter 3 deals with switched-current filter design techniques for high order and wide band filtering applications. In the first part, a brief review is first given of general SI filter design by matrix methods[7]. Modifications to existing Left and Right decomposition methods are then introduced which simplify the input circuitry, improve sensitivity and avoid a dynamic-range scaling problem inherent to Right decomposition type designs. A prototype manipulation technique applicable to matrix-derived bilinear-LDI structures is then employed to design very high order SI filters with remarkably reduced spreads and areas. In the second part, design issues

related to wideband SI filter design are addressed and SI filter structures derived by the UL-LU and LU-UL matrix decomposition method[8] are introduced. Various design examples are given for illustration and sensitivity simulations are used for comparing the different designs.

Chapter 4 concerns the design of switched-current ladder delay equalisers or allpass filters that are based on bilinear integrators. Previous work on SI delay equalisers is based on Euler or LDI integrators[9]. After a brief background introduction, two design approaches are introduced. The first is based on simulating an s-domain prototype using the bilinear $s \rightarrow z$ transformation while the second approach proceeds directly with a z-domain allpass transfer function. Either way, both methods eventually employ matrix methods to derive the resultant active SI allpass structure. It will be shown that the amplitude response is completely insensitive to deviations in any of the component values in the reactive part of the filter. The effects of several non-ideal factors and sensitivity are simulated for both the amplitude and group delay responses. Comparisons of different realisations highlight the advantages of the bilinear integrator based circuits over the Euler ones.

Chapter 5 departs from the conventional and ventures into the area of multirate circuits. The introduction briefly describes the applications of decimators and interpolators and gives a review of existing SI multirate circuits. In the first part to follow, two SI IIR decimators based on FIR polyphase networks coupled to low sensitivity ladder structures are proposed. These are derived via a multirate transformation procedure which enables the entire structure to operate at the lower clock frequency, maximising the time available for the memory cells to settle. In the second part, two corresponding interpolator structures are derived via a direct transposition procedure, which avoids the need of redesign. Design examples and sensitivity comparisons of different structures are given.

Chapter 6 is involved with the design of N-path and pseudo-N-path SI filters. In the introduction, the background and operating principles are explained. Next, a family of fully-balanced N-path and pseudo-N-path cells based on the Forward Euler, Backward Euler, and bilinear integrators are proposed. The N-path cells perform the

$z \rightarrow -z$ or lowpass-to-highpass transformation while the pseudo-N-path cells perform the $z \rightarrow -z^2$ or lowpass-to-bandpass transformation using the circulating-delay principle. The effects of various non-ideal factors on the frequency response of the cells are analysed and confirmed by simulation. Design examples are given and different designs are compared in terms of sensitivity and robustness to non-ideal factors.

Chapter 7 summarises the work done in the previous chapters, discusses the results and draws relevant conclusions. Finally, recommendations for future work and new research directions are proposed.

1.3 STATEMENT OF ORIGINALITY

The most significant results of the research work presented in this thesis are compiled in the following list and to the best of the author's knowledge, are original and as indicated, have either been published, submitted for publication, or will be published.

In Chapter 3, modifications made to the general Right and Left decomposition SI structures[7] result in simplified input circuitry, improved sensitivity performance and avoids a dynamic-range scaling problem inherent to Right decomposition type designs. A 21st order SI lowpass filter was designed using a technique which allowed remarkable reduction of spreads and area. For the design of wideband filters, SI filter structures based on the LU-UL and UL-LU matrix decompositions which exhibit low sensitivity at large relative bandwidths were introduced.

- [A.E.J. Ng and J.I. Sewell: 'Feasible Designs for High Order Switched-Current Filters', Proceedings - IEEE International Symposium on Circuits and Systems, Monterey, California, May, 1998, pp. MAA15-6].

- [A.E.J. Ng and J.I. Sewell: 'Ladder Decompositions for Wideband Switched-Current Filter Applications', Proceedings - IEEE International Symposium on Circuits and Systems, Monterey, California, May, 1998, pp. MAA15-24].

- [A.E.J. Ng and J.I. Sewell: 'Feasible Designs for High Order Switched-Current Filters', Proc. IEE Circuits, Devices and Systems, vol.145, (5), pp.297-305, 1998].

- [A.E.J. Ng and J.I. Sewell: 'Ladder Decompositions for Wideband Switched-Current Filter Applications', Proc. IEE Circuits, Devices and Systems, vol.145, (5), pp.306-313, 1998].

- [A.E.J. Ng and J.I. Sewell: 'Switched-Current Techniques Under Pressure: High Order and Wideband Filter Design', Proc. 4th IEE Analog Signal Processing Colloquium, Oxford, UK, October, 1998, pp.4/1-4/11].

In Chapter 4, novel SI ladder allpass filters based on bilinear integrators are proposed for group-delay equalisation. Synthesis of these structures can proceed either via the s-domain or directly from the z-domain. The singly-terminated reactive ladder section of the prototype is then simulated using standard matrix methods. The allpass amplitude response of the structures is completely insensitive to any deviation in the component values within the ladder section. Other characteristics also compare favourably to Euler integrator based ladder and cascade biquad based designs. This work has been submitted for publication.

- [A.E.J. Ng and J.I. Sewell: 'Switched-Current Bilinear Ladder Group-Delay Equalisers', submitted to - IEEE International Symposium on Circuits and Systems, Geneva, Switzerland, May, 2000].

In Chapter 5, novel SI IIR decimator and interpolator structures based on FIR polyphase networks and low-sensitivity ladder structures are proposed. These were derived by a multirate transformation procedure which enabled operation at the lower clock frequency, maximising the available settling time. The interpolators were derived by direct transposition.

- [A.E.J. Ng and J.I. Sewell: 'Switched-Current Elliptic Decimators Based on Bilinear-Transformed Ladder Structures', Proc. 5th IEEE ICECS, Lisboa, Portugal, September, 1998, (3), pp.355-358].

- [A.E.J. Ng and J.I. Sewell: 'Ladder Derived Switched-Current Decimators', Proc. 4th IEE Analog Signal Processing Colloquium, Oxford, UK, October, 1998, pp.5/1-5/9].

- [A.E.J. Ng and J.I. Sewell: 'Bilinear-Transformed Switched-Current Ladder Interpolators', Proceedings - IEEE International Symposium on Circuits and Systems, Orlando, Florida, May, 1999, vol. II-468, 4p].

- [A.E.J. Ng and J.I. Sewell: 'Ladder Derived Switched-Current Decimators and Interpolators', IEEE Trans. CAS II: Analog and Digital Signal Processing, vol.46, (9), pp. 1161-1170, 1999].

In Chapter 6, a family of novel N-path and pseudo-N-path SI cells with fully-balanced structures are proposed. For the N-path cells, integrators are transformed into differentiators via the $z \rightarrow -z$ or lowpass-to-highpass transform. For the pseudo-N-path SI cells, integrators are transformed into resonators via the $z \rightarrow -z^2$ or lowpass-to-bandpass transform. These allow the design of narrowband bandpass SI filters from a z-domain lowpass prototype.

- [A.E.J. Ng and J.I. Sewell: 'Pseudo-N-Path Cells for Switched-Current Signal Processing', Proceedings - IEEE International Symposium on Circuits and Systems, Orlando, Florida, May, 1999, vol. II-484, 4p].

- [A.E.J. Ng and J.I. Sewell: 'N-Path and Pseudo-N-Path Cells for Switched-Current Signal Processing', IEEE Trans. CAS II: Analog and Digital Signal Processing, vol.46, (9), pp. 1148-1160, 1999].

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[8] P. Li: 'Theory and methodology of integrated ladder filter design', PhD Thesis, Department of Electronics and Electrical Engineering, University of Glasgow, 1990.

[9] Y. Lu: 'Modern VLSI analogue filter design: methodology and software development', PhD Thesis, Department of Electronics and Electrical Engineering, University of Glasgow, 1995.

CHAPTER 2:
INTRODUCTION AND REVIEW OF THE SWITCHED-CURRENT TECHNIQUE

2.1 INTRODUCTION

2.2 BASIC OPERATING PRINCIPLE OF SI CIRCUITS

2.3 NON-IDEAL FACTORS

- 2.3.1 Transistor Mismatch
- 2.3.2 Finite Output/Input Conductance Ratios
- 2.3.3 Clock-Feedthrough and Charge Injection
- 2.3.4 Settling
- 2.3.5 Noise

2.4 REVIEW OF ADVANCES IN MEMORY CELL DESIGN

- 2.4.1 Charge Cancellation Techniques
- 2.4.2 Algorithmic Techniques
- 2.4.3 Combined Algorithmic and Charge Cancellation Techniques
- 2.4.4 Attenuation Techniques
- 2.4.5 Zero-Voltage Switching Techniques
- 2.4.6 Voltage Tracking or Adaptive Techniques

2.5 SI SYSTEMS

- 2.5.1 Filters
  - A. FIR Filters
  - B. IIR Filters
  - B1. Direct Form Implementations
  - B2. Cascade Biquad Based
  - B3. Ladder Based
  - C. Delay Equalisers and Allpass Filters
  - D. Multirate Filters
  - E. N-Path and Pseudo-N-Path Filters
- 2.5.2 AD Converters and Miscellaneous SI Systems

2.1 INTRODUCTION

The purpose of this chapter is to provide a general review of the most significant aspects of the switched-current(SI) technique[1,8]. Developments to date are traced, evaluated and organised into different functional categories. The basic operating principle and circuits of the SI technique are first explained. This is followed by a brief description of several non-ideal factors that affect the performance of SI circuits. A great deal of research effort has been focused on minimising the effects of the many non-ideal factors, in particular that of clock-feedthrough/charge-injection which is a chief cause of distortion errors. The many types of SI memory cells are categorised by the error correcting techniques employed. Next, a review of SI systems is given. The main focus is on the various filtering systems as they are directly related to the work in this thesis. A brief reference to SI data converters and other miscellaneous systems is also given. Finally, an introduction is given to SI integrated filter design automation and aspects of this work as implemented into the filter and equaliser compiler XFILT[99,101].

2.2 BASIC OPERATING PRINCIPLE OF SI CIRCUITS

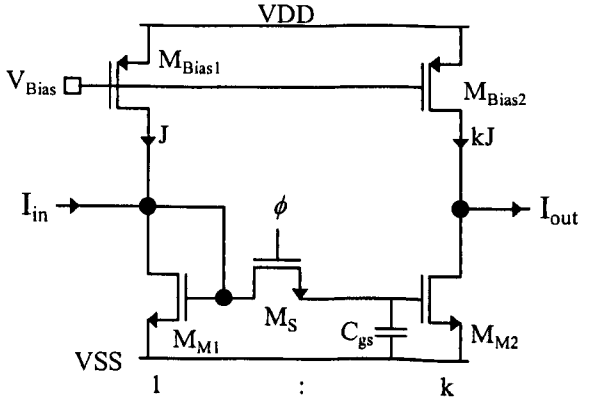


Figure 2.1 Basic 1st generation SI memory cell

The advantages of SI circuits over traditional SC circuits are simplicity, compatibility with advanced digital processes and potential for high speed and low voltage operation. This is because no operational amplifiers or linear floating capacitors are required, but only simple current-mode circuits with low impedance nodes, where the inherent parasitic gate-source

overlap capacitance of the MOS transistor is used as a memory element to store voltage. The supply voltage can be low as it mainly sets the bias levels, while dynamic range of the currents is not directly affected.

SI memory cells are broadly classified as either of 1st generation or 2nd generation type[1,8,9,10]. From these basic cells, circuits can be built that implement many signal processing functions. The 1st generation SI memory cell is essentially a current mirror with a switch M_S connecting the gates of the two main transistors as shown in Fig. 2.1. Transistors M_{M1} and M_{M2} are biased in saturation by M_{Bias1} and M_{Bias2} respectively. Diode connected M_{M1} provides a low input resistance node for the summing of currents. Switch M_S closes when ϕ goes high and charges the gate-source capacitor C_{gs} to a voltage of V_{gs} that sustains the current flowing in M_{M1}. By normal current mirror action, I_{out} will ideally be $-kI_{in}$ and is concurrently available with I_{in}. When ϕ goes low and switch M_S turns off, a voltage close to V_{gs} is held on the gate of M_{M2}, which maintains the output current at approximately $-kI_{in}$ until the next time ϕ goes high. Note that the role of the parasitic capacitor C_{gs} is only to hold charge corresponding to a V_{gs} that is dictated by the current level. Thus, the switched-current memory cell is a current-voltage processor as opposed to a charge-voltage processor such as a switched capacitor circuit. Consequently, the capacitors need not be linear, which allows SI circuits to be integrated in standard, single-poly digital processes.

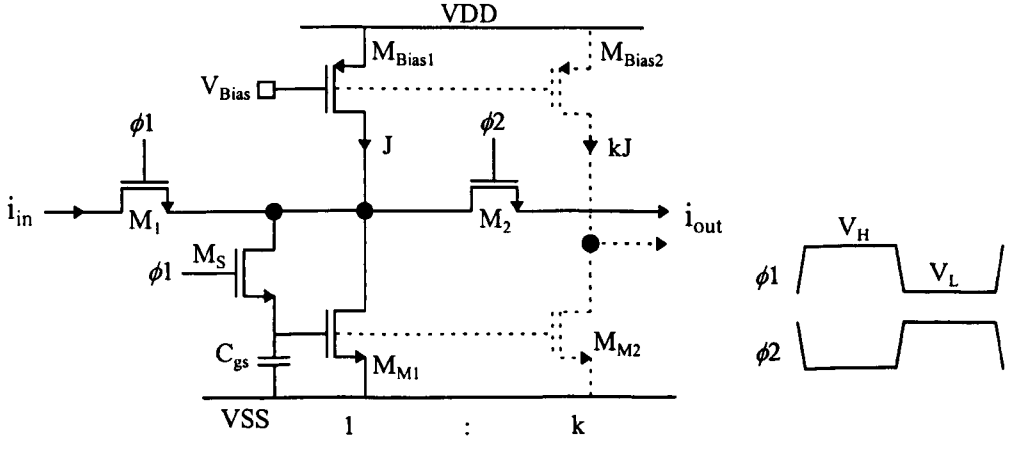


Figure 2.2 Basic 2nd generation SI memory cell and clock waveforms

The 2nd generation SI cell emerged shortly after the 1st generation cell and is shown in Fig. 2.2. The operation of the cell is described as follows: During the sampling phase $\phi 1$, both switches M_1 and M_S are closed while M_2 is open. Transistor M_{M1} is therefore diode-connected and conducts a drain-source current of $J+i_{in}$, causing C_{gs} to charge to V_{gs}. In the hold phase $\phi 2$, switches M_1 and M_S are opened whilst M_2 is closed. This isolates the charge held in C_{gs} and so a voltage close to V_{gs} is maintained. The drain-source current of $J+i_{in}$ is sustained in transistor M_{M1} and results in an output current of $-i_{in}$. Thus, the cell has memorised the input current from the previous phase. The part of the circuit shown in dotted lines provides a full period, scaled output current sample as will commonly be required to implement scaled filter coefficients

In general, the current steering switches M_1 and M_2 can be driven by overlapping two-phase clocks while voltage sampling switches such as M_S should be clocked by non-overlapping clock phases. This is to ensure that no open circuit or disruption to the current path will occur, and that sampling will be completed before the input sample is removed.

2.3 NON-IDEAL FACTORS

The switched-current technique was primarily introduced as an alternative to the voltage-mode switched-capacitor technique to overcome the many limitations brought on by the ever shrinking feature sizes of advanced digital processes[1]. However, for any technique to make a significant impact and gain wide acceptance, various non-ideal factors will have to be effectively dealt with to achieve a level of performance that is comparable with other state-of-the-art techniques.

SI circuits are predominantly implemented by MOS transistors and so far, only ideal circuits have been described. The impact of non-idealities will vary depending on the required performance specifications of the target application. Most of the non-ideal factors have been treated in considerable detail[1]. The following sub-sections serve only as a brief, general introduction to the nature of some common non-ideal effects.

2.3.1 Transistor Mismatch

In typical CMOS processes, the absolute matching accuracy of components such as transistors and capacitors can vary by as much as ±20%. In contrast, the relative matching or ratio of components can match to within ±0.1%, which makes analogue techniques such as SC and SI feasible. However, inevitable mismatches in geometric dimensions resulting from process variations, and even the relative alignment of different transistors will result in mismatches in physical parameters such as transconductance(gm), threshold voltage(V_T) and channel length modulation parameter(λ). It was shown[1] that mismatches in V_T and β produce no errors in the gain of the basic current memory. However, the variance of gain error will be inversely proportional to the transistor area when mirroring is performed.

2.3.2 Finite Output/Input Conductance Ratios

During sampling, the gate and drain of memory transistor are shorted and thus have the same voltage. When the memory cell is in its holding phase, the drain voltage may change and induce an error in the memorised drain current. This is due to the channel shortening effect and also coupling of voltage variations at the drain to the gate via the drain-gate capacitance C_{dg}. Consequently, an equivalent output conductance exists for the memory cell which if not negligibly small compared to the small-signal input conductance($\approx g_m$), will give rise to a small-signal gain error but no phase error. In an integrator however, both gain and phase errors will occur[1].

2.3.3 Clock-feedthrough and Charge Injection

Sampling switches are implemented by MOS transistors with their gates driven by high frequency digital clocks. These clock signals will couple through to the drain and source terminals via the gate diffusion overlap capacitance. Furthermore, when the switch is turned off, channel charge is ejected from the drain, source and substrate. A fraction of this combined charge will enter the gate-source storage capacitor C_{gs}, resulting in an error in the drain current. Due to the complex dynamics involved, no closed form solution has been found. However, from simplified analyses, the effect of charge injection on the frequency response of the memory cell and integrator is found to be similar to that caused by finite

output conductance[1]. Furthermore, significant distortion is introduced due to the non-linear signal dependence of the injected charge[1,11,49].

2.3.4 Settling

A residual error voltage will be present on C_{gs} if, within the duration of the sampling phase, C_{gs} is not completely charged. This will induce an error in the drain current. It has been shown that during sampling, the dynamics of a memory cell can be described by a second order system. An underdamped step response might cause instability and should be avoided. For the memory cell, settling errors result in both magnitude and phase errors[1].

2.3.5 Noise

The dominant noise source affecting SI circuits is thermal noise. Low frequency flicker noise is usually eliminated by the highpass effect of the correlated-double-sampling(CDS) action inherent to second generation memory cells[1]. On the other hand, broadband thermal noise is undersampled and gets folded back into the baseband. Detailed noise analyses of the memory cell and integrator can be found in [1].

2.4 REVIEW OF ADVANCES IN MEMORY CELL DESIGN

From the previous discussion of non-ideal factors in Section 2.3, it is clear that the basic circuits of Figs. 2.1 and 2.2 will not be capable of implementing practical systems to any reasonable level of accuracy. In practice, additional circuitry is needed to enhance the performance of the basic cells and is currently an active area of research. Much research effort has been focused on the reduction of clock-feedthrough and charge injection errors(CFT). The techniques employed can be broadly classified [103,105] into the categories that follow.

2.4.1 Charge Cancellation Techniques

Charge Cancellation techniques combine two or more CFT error components in a controlled way to achieve partial or total cancellation[103]. In its simplest form, a dummy switch[32] consisting of a MOS transistor with the drain and source shorted, of approximately half the sampling switch size is placed at the storage node and clocked in anti-phase to absorb the injected charge. The effectiveness of this method is limited by the accuracy of the clock edges, which is difficult to control precisely in practice. Alternatively, CMOS switches can be used, the idea being that injected charges of opposite polarities cancel. Cancellation will however be incomplete due to differences in the NMOS and PMOS transistors, strong signal dependency of the injected charge and the fact that cancellation only occurs at the crossover of the clock voltages. In [25], the CMOS switched was optimised while in [23], the outputs from complementary memory circuits were combined to achieve cancellation. In a new cell that uses a similar technique[52], the CMOS switch was connected to an optimised, fixed gate potential that theoretically will result in the cancellation of charges from the PMOS and NMOS transistors. However, due to the problems mentioned earlier, complete cancellation is difficult to achieve and some residual signal dependent errors will remain.

Other forms of the cancellation technique have been proposed for both the 1st generation and 2nd generation memory cells[11,103,24,53]. The memory cell proposed in [53] is shown in Fig. 2.3. In phase $\phi 2$, M_2 samples the bias current J while the output current is delivered. At the end of phase $\phi 2$, switch M_{S2} opens and injects a constant charge, and the current flowing in M_2 becomes J-δi. In phase $\phi 1$, the main transistor M_1 samples the input together with δi, giving rise to a drain current of J+i_{in}+δi. When switch M_{S1} opens, a signal dependent charge is injected, which produces an error current of -δi-δi_S, where δi_S is the signal dependent component of the error current. The resulting output current is given by J-J-i_{in}-δi+δi+δi_S = -i_{in}+δi_S. Therefore, this memory cell cancels only the signal-independent charge injection errors.

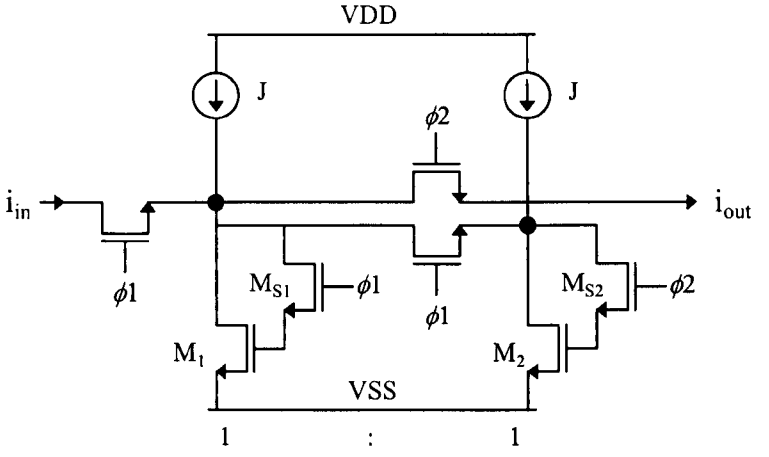


Figure 2.3 A constant CFT cancellation 2nd generation SI memory cell[53]

A 2nd generation type memory cell that cancels both the signal dependent and independent charge injection components[24] is shown in Fig. 2.4. The memory cell is split into three equal parts, each injecting different proportions of charge, controlled by different numbers of unit switches. By adding the scaled differences of the individual error currents, it is then possible to compensate for the error current at the output of the cell[24].

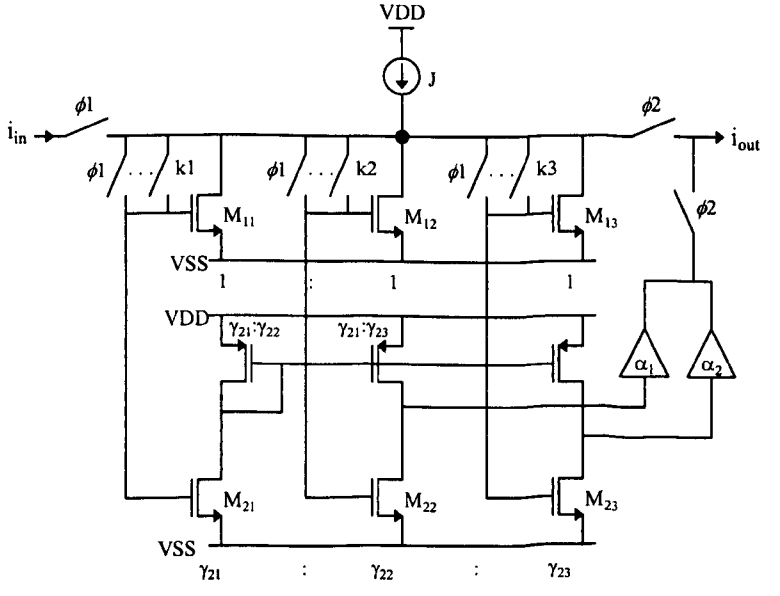


Figure 2.4 Complete CFT cancellation 2nd generation SI memory cell[24]

2.4.2 Algorithmic Techniques

Algorithmic techniques all use some form of iterative sampling method where CFT errors are gradually cancelled[103]. An early version of an algorithmic cell[17] is shown in Fig. 2.5.

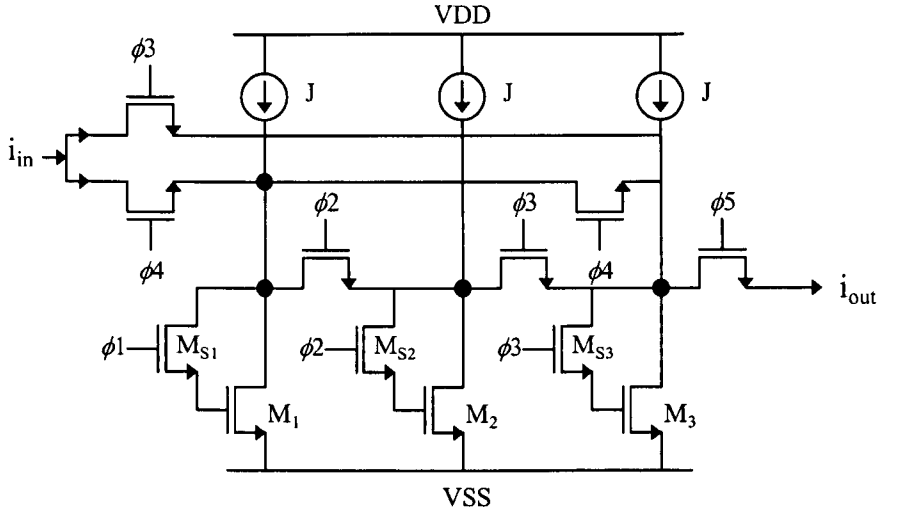


Figure 2.5 Algorithmic memory cell [17]

This cell works by basically inverting the charge injection error and passing it through the same cell again so that cancellation is achieved without the need for matching. However, five clock phases and three basic memory cells are required, which puts a severe limitation on the operating speed of the cell.

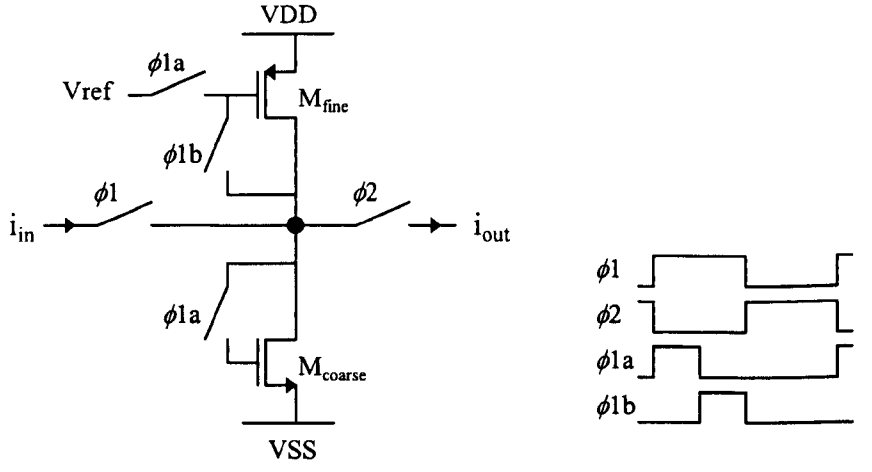


Figure 2.6 The S^2I two step algorithmic memory cell[12]

A well known algorithmic cell is the two step S^2I[12] memory, shown in Fig. 2.6. In phase ϕ1a, the input is sampled by the 'coarse' memory transistor while the 'fine' transistor is configured as a bias current source. When the sampling switch opens at the end of phase ϕ1a, charge is injected into the storage node. In phase ϕ1b, with the input still connected, the difference between the input and stored current, which is the error current, is sampled by the 'fine' memory transistor. The output current delivered in phase ϕ2 is formed by subtracting the 'fine' current from the 'coarse' sample. The main error from the 'coarse' memory transistor is eliminated but there still remains a residual, signal dependent error from the charge injected into the 'fine' memory transistor. For further refinement of the residual error current, the n-step S^nI[16] cell was proposed. Improved versions of the S^2I cell can be found in [13,14], where additional non-ideal factors were compensated for, and where a virtual earth is produced in both the 'coarse' and the now implicit 'fine' sampling phases. Other variants of the two-step memory cell exist which seek to reduce the switching transient and increase available settling time[104], employ current conveyors with reduced power dissipation[46], and operate with low voltage supplies[47].

2.4.3 Combined Algorithmic and Charge Cancellation Techniques

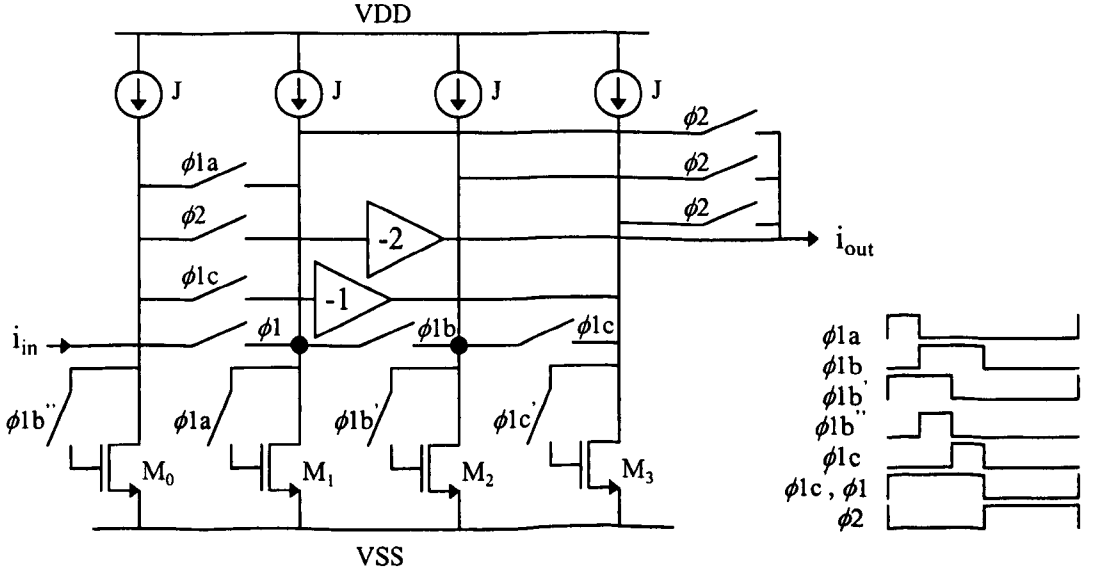


Figure 2.7 Combined algorithmic and charge cancellation memory cell[29]

As implied, these techniques employ a combination of both the Algorithmic and Charge Cancellation techniques to eliminate the CFT errors. In [29], a second generation type cell was proposed for total cancellation of charge injection errors as shown in Fig. 2.7. The idea was to cancel the signal dependent errors with the n-step algorithmic technique while the accumulated signal independent errors were then cancelled by weighted replicas.

In a similar cell[26], a single PMOS-NMOS S^2I cell was used in conjunction with a dummy circuit that cancels the signal independent CFT error of the 'fine' stage at the output. A rather different scheme[22] that remotely resembles the S^2I technique is based around a regulated cascode second generation cell, has just an additional grounded capacitor switched to the main storage node. The idea is to first inject half the signal dependent charge equally into both capacitors, then open the main sampling switch to inject charge into the main capacitor, and finally to short both capacitors to subtract the error from both capacitors. However, imperfect cancellation will result from unequal splitting of charge due to differences in node impedances and voltages. And because of the different loading of the capacitors, settling performance might be affected.

2.4.4 Attenuation Techniques

Attenuation techniques aim directly to reduce the error voltage or the amount of charge that is actually injected onto the gate of the memory transistor[103]. The most apparent way is to increase the size of the storage capacitor. However, this will severely restrict the operating speed of the memory cell. In one of the earliest schemes[7], a high loop gain was created around the Miller-capacitance to minimise charge injection to the main storage node at the opening of the switch. A second sampling switch is then opened such that the charge injected is attenuated by capacitive division. In [20,21], a Miller capacitance enhancement technique was used as shown in Fig. 2.8, where a small capacitor placed in the feedback loop of an amplifier creates the effect of a large capacitance for effective attenuation of injected charge. The loop gain is kept low during sampling and switched to high just before the switch charge injection occurs.

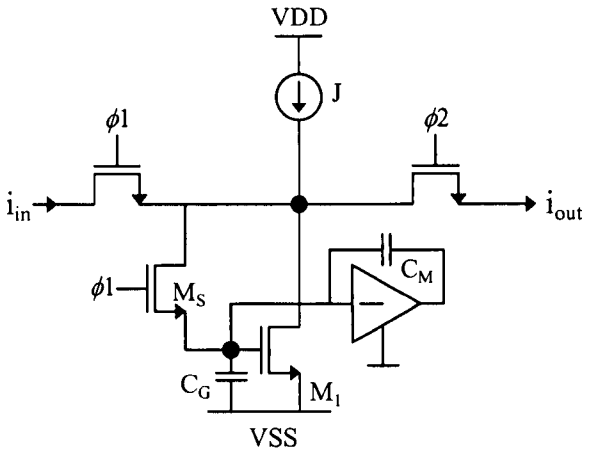


Figure 2.8 Miller-enhanced SI memory cell[21]

2.4.5 Zero-Voltage Switching Techniques

Signal dependent CFT errors can be eliminated by maintaining the sampling switch at a fixed potential or 'virtual ground'. This way, the switch always opens at the same potential and charge injection will be constant, which can then be easily eliminated. The memory cell shown in Fig. 2.9 is based on locating the storage node at a virtual ground provided by an operational amplifier[28]. Thus, the signal dependent charge injected is avoided. However, high linearity is achieved at the cost of a double-poly capacitor. A MOS capacitor can be used but will limit the signal range due to biasing requirements and will also introduce non-linearities. A similar, fully differential cell[51] uses additional circuitry to set the common-mode voltage levels at the cell input and gates of the main memory transistors to eliminate any signal-independent charge injection.

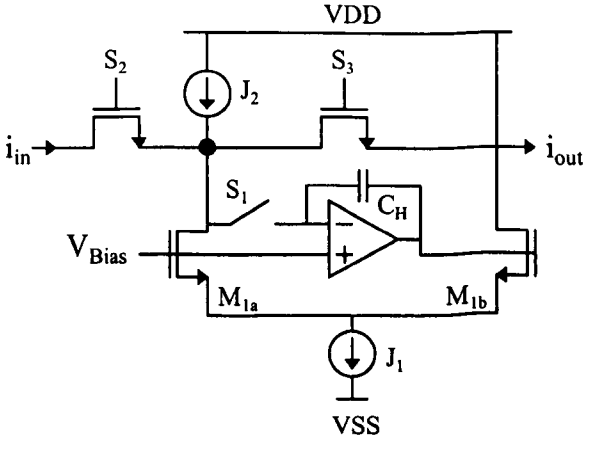


Figure 2.9 Zero-voltage switching SI sampler[28]

A rather unconventional memory cell configuration[34] has its summing node at the source of the main memory transistor, which is held constant by the regulating action of a high gain negative feedback circuit. As the switches are connected to this node, charge injection is signal independent.

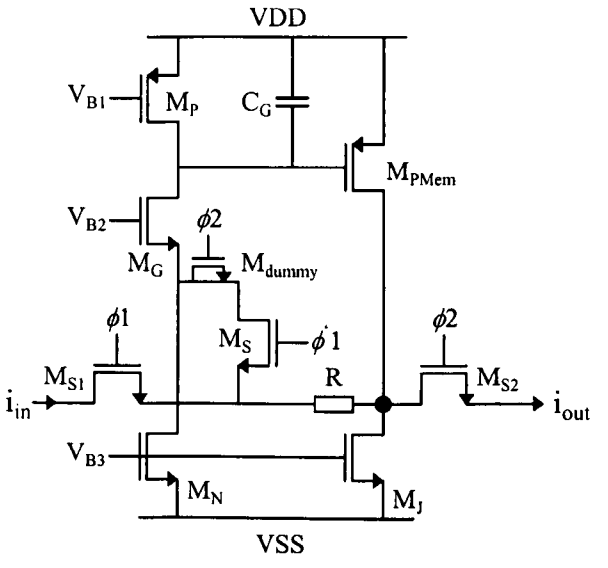


Figure 2.10 Modified grounded-gate memory cell with dummy switch cancellation[27]

In another example[27] shown in Fig. 2.10, a modified common-gate PMOS memory cell was proposed where the sampling switch was removed from the gate of the main memory transistor to the source side of the NMOS common gate transistor. This way, the sampling switch is held at a near constant voltage, and any signal independent charge injection was cancelled by a dummy switch.

2.4.6 Voltage Tracking or Adaptive Techniques

It is well known that the amount of charge injected is a function of the clock slope and voltage levels. By adaptive control of the clock slope or voltage levels, an almost constant CFT can be achieved. In one scheme[15,33], the clock signal level was made to track the input signal such that a constant voltage is maintained across the sampling switch. In another scheme[45], adaptive control of the clock edges combined with a dummy switch significantly improved the cancellation of clock-feedthrough.

2.5 SI SYSTEMS

As with the SC technique, diverse applications have also been found for the SI methodology which include sampled-data filters[55-57,59-81], Nyquist[89,103] and over-sampling[47,93,94] data converters, mixers[87], comparators[88], multipliers[91], phase lock loops(PLLs)[90], pulse-width modulators and oscillators[92]. This section will give an overview of the many existing SI systems. However, heavier emphasis will be placed on filtering applications as it is more relevant to the context of this thesis.

2.5.1 SI Filters

Sampled-data filters are ubiquitous and in the realm of analogue and mixed-signal processing, they are widely employed as reconstruction filters for A/D and D/A converters, IF filters for radio, TV, video and other front-end signal processing tasks. In recent years, there has been a proliferation of reports on SI filter applications[55-57,59-81]. These can broadly be classified into the following types of filters:

A. SI FIR filters

These filters are characterised by a finite impulse response and are particularly important for applications requiring linear phase responses. An early SI FIR filter[78] employed first generation memory cells in a tapped serial delay line configuration as shown in Fig. 2.11. The taps were realised by scaled current mirrors at the end of each delay stage(shown shaded), and summed together to form the output. The transfer function of the FIR filter is given by

$$H(z) = \sum_{k=0}^{M} a_k z^{-k}$$

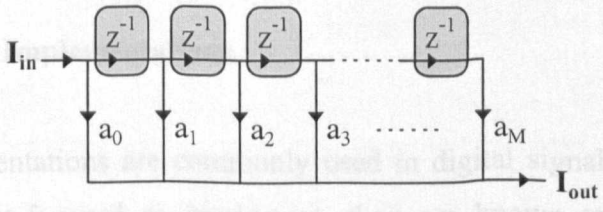


Figure 2.11 Tapped delay line direct FIR structure[78]

SI FIR filters based on differentiator elements instead of unit delays were proposed in [76]. The general transfer function of this type of FIR filter is given by

$$H(z) = \sum_{k=0}^{M} a_k (z^{-1} - 1)^k$$

and the structure is shown in Fig. 2.12. The main advantage of the differentiator based FIR structure over that using unit delays is that sensitivities with respect to variations in multiplier coefficient deviations is lower when the signal-to-clock frequency ratio is less than 1/6[76].

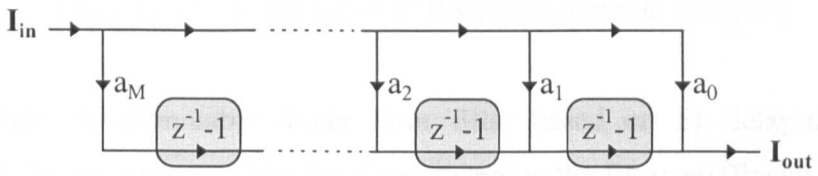


Figure 2.12 Differentiator based FIR structure[76]

In [48], elemental lowpass and highpass FIR sections were proposed for video applications which consisted of second generation memory cell based parallel delay lines. Compared to a serial delay line, a parallel delay line requires the same number of clock phases as the memory cells and is more sensitive to transistor mismatch. A hybrid analog-digital SI FIR filter[58] was proposed for channel equalisation of coaxial or twisted pair cables used in 64-QAM digital modem applications.

B. SI IIR Filters

IIR filters are by far the most common of all the SI filtering systems and can be realised in many different forms. They are characterised by an infinite impulse response and realise highly selective responses using recursive structures.

B1. Direct Form Implementations

Direct form implementations are commonly used in digital signal processing. Although compact and straight-forward to implement, they are known to have poor sensitivity characteristics. Therefore, few examples of SI direct form filters can be found.

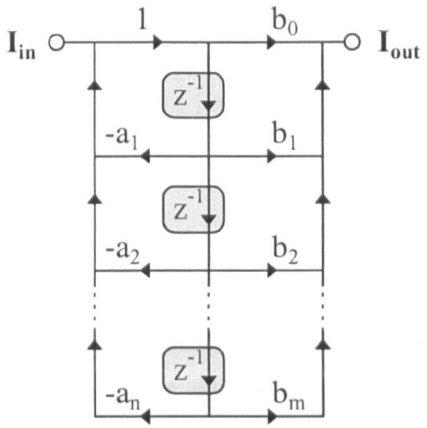


Figure 2.13 Structure of SI IIR programmable filter[81]

In [81], a fully programmable direct form filter based on SI delay-multipliers was demonstrated. Programming, which involved changing the filter coefficients, was achieved by connecting transistors of different sizes from an array. The IIR filter structure is shown in Fig. 2.13 and the transfer function is given by

$$H(z) = \frac{\sum_{k=0}^{m} b_k z^{-k}}{1 + \sum_{k=1}^{n} a_k z^{-k}}$$

A direct form SI IIR filter based on differentiators can be found in [76] which realises a transfer function of

$$H(z) = \frac{-b_0 + \sum_{k=1}^{N} b_k (z^{-1} - 1)^k}{a_0 - \sum_{k=1}^{N} a_k (z^{-1} - 1)^k}$$

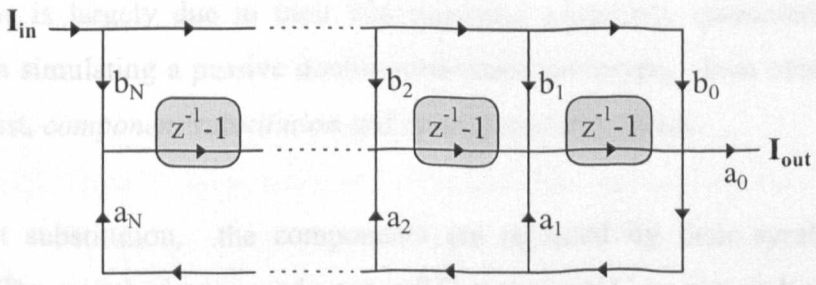


Figure 2.14 Differentiator based direct form SI IIR filter[76]

The filter structure is shown in Fig. 2.14. The advantage of using differentiators is the ease with which highpass responses can be realised. This contrasts with integrator based filters, which cannot be directly applied to highpass filters without modifications[76].

B2. Cascade Biquad Based

A high order transfer function can be factorised and expressed as a product of biquadratic polynomials for pure even order functions, and in the case of an odd order function, with an accompanying first order rational polynomial. This reduces the task of realising a high order function into a simple cascade of 2nd order biquadratic blocks. One of the main advantage of this type of realisation is the ease with which each biquad section, realising a pole/zero pair, can be individually tuned. Although attractive, this decoupled nature of cascade biquad filters results in relatively high sensitivity compared to their ladder based counterparts. This makes them unsuitable in the realisation of high-order or high-Q filters.

An early 6th order biquad[8] based on first generation bilinear integrators was used to demonstrate the SI technique. This was followed by a systematic procedure to design SI cascade biquad filters from an SC reference circuit. The example was based on mapping the coefficients of a bilinear-transformed continuous time biquadratic polynomial to that of an SI biquad structure. First generation Euler integrators were used. Similar biquads have been fabricated with measured lowpass, highpass and bandpass responses[62].

B3. Ladder Based

Of the different ways of realising an active IIR filter, ladder based designs are the most popular. This is largely due to their low passband sensitivity characteristic, which is inherited from simulating a passive doubly-terminated prototype. Two common forms of simulation exist, *component substitution* and *operational simulation*.

In component substitution, the components are replaced by their synthesised, active counterpart. The switched-transconductance(ST) technique[1] is one such example where elements such as resistors, inductors, capacitors and composite elements can be synthesised using a tunable transconductor and a switched-current processor. In [80], SI filters based

on the simulation of capacitors and transconductors of continuous-time gm-C filters were proposed.

The majority of SI ladder filters are based on the operational simulation of a reference prototype filter. In this method, the internal equations characterising a doubly-terminated passive prototype are realised. The mapping between the continuous time and discrete time domains is usually the bilinear s→z transform, which maps the entire left half of the s-plane into the unit circle of the z-plane. For integrator based filters, the bilinear integrator can be used[8,63,64,66-68], which allows a direct simulation of the transformed s-domain prototype. With some rearrangement and modifications, Euler integrators can be used in the so called bilinear-LDI method[69-74]. A typical doubly terminated ladder structure is shown in Fig. 2.15, which consists of coupled two-integrator loops.

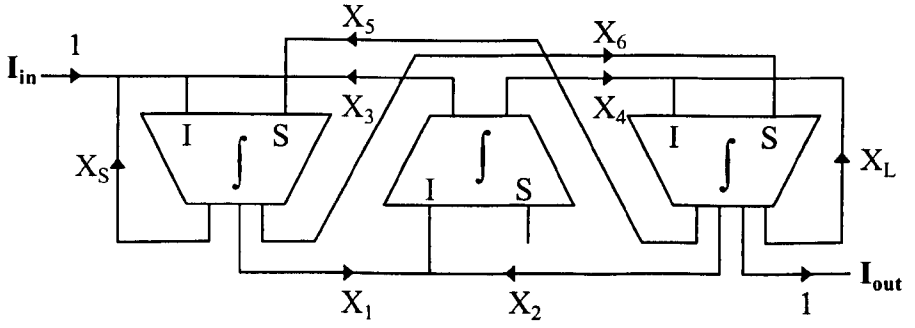


Figure 2.15 Typical topology of an operationally simulated ladder filter

The I and S inputs represent integrating and summing(or feedthrough) nodes respectively. The topology of the ladder structure is dependent on the derivation procedure employed, and many alternatives can be obtained by matrix decomposition methods[71-73]. Individual topologies will have different salient points such as canonicity, sensitivity, spread and total area estimate.

An alternative way of realising ladder SI filters is the based on the Wave Digital Filter(WDF) technique[77,103]. Here, the variables simulated are the delay, transmission and reflection occurring in waves propagating in a microwave filter. The associated elements of WDFs are delays and adaptors.

The author's contributions are in the area of SI ladder filter design for high order and wideband filtering applications[72,73]. Successfully proven for SC filters[107], it is shown that similar benefits can be derived when the techniques are applied to SI filters. Details of this work are documented in Chapter 3 of this thesis.

C. Delay Equalisers and Allpass SI Filters

Allpass filters have flat amplitude responses and are used primarily for group-delay equalisation. The z-domain transfer function of an n-th order allpass filter takes the general form

$$H(z) = k\frac{z^n P(z^{-1})}{P(z)}$$

where k=-1 for n even and k=+1 for n odd. Although lattice and ladder based SC allpass filters are relatively common, very few references to SI implementation can be found. In [106], SI ladder based allpass filters were designed using second generation Euler integrators. The structure consists of a feedforward summing network and a singly-terminated reactive ladder shown in Fig. 2.16, and has a transfer function of

$$H(z) = 1 - \frac{2}{1 + Y(z)}$$

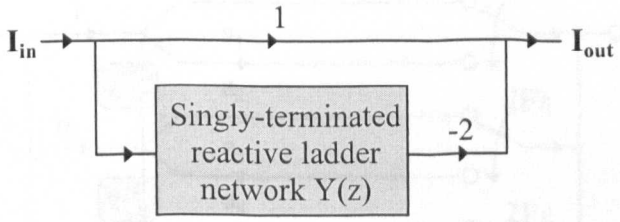
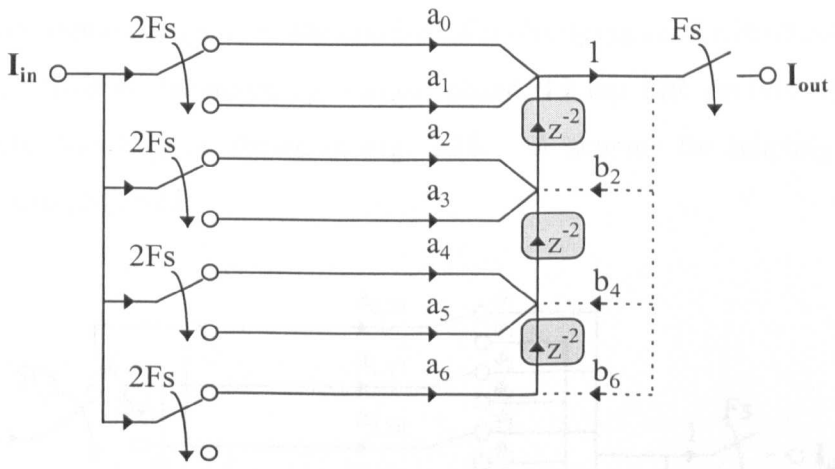


Figure 2.16 Top level structure of a ladder based SI allpass filter[106]

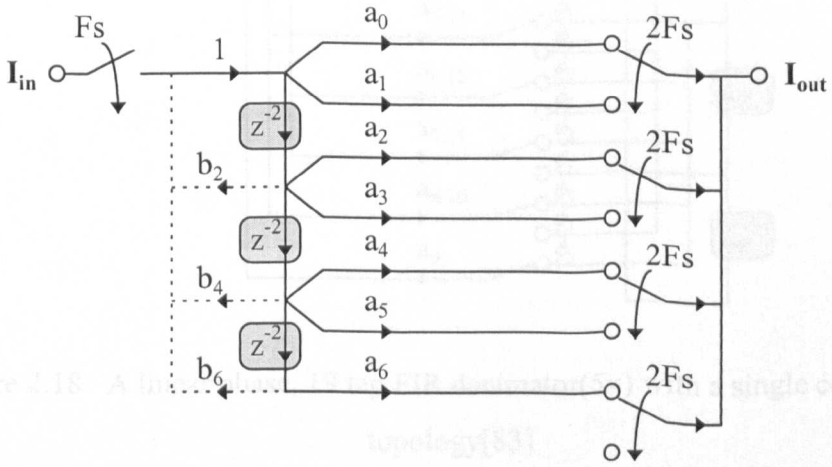
The author's contribution to this area are SI ladder allpass filters based on bilinear integrators which can be designed either from an s-domain prototype or directly in the z-domain. Details are documented in Chapter 4 of this thesis.

D. Multirate SI Filters

The basic building blocks of multirate filters are decimators and interpolators. Decimators decrease the sampling rate, while simultaneously performing filtering to prevent aliasing at the lower output sampling frequency. Interpolators on the other hand increase the sampling rate while simultaneously filtering out the unwanted images that are generated at the higher output sampling frequency.



(a) SI FIR/IIR decimator SFG



(b) SI FIR/IIR interpolator SFG

Figure 2.17 SFG of SI FIR/IIR decimator(2×) and interpolator(2×) proposed in [82]

In [82], both SI FIR and IIR decimators and interpolators were proposed as shown in Figs. 2.17a and b. These were based on direct form polyphase block-delayed(shown shaded) structures using multiple input and output commutators respectively. The feedback branches shown in dotted lines are used only in the recursive IIR structures.

High speed polyphase FIR decimators for wide bandwidth video filtering applications were proposed in [83]. A single input commutator topology was used to reduce asymmetric clock-feedthrough errors that might otherwise produce significant distortion. For linear phase, symmetric impulse responses, the number of multiplying coefficients can be halved by multiplexing. This is illustrated by a linear phase, 19 tap FIR decimator(5×) with a single commutator topology as shown in Fig. 2.18. A scheme for relaxing the timing constraints was also proposed.

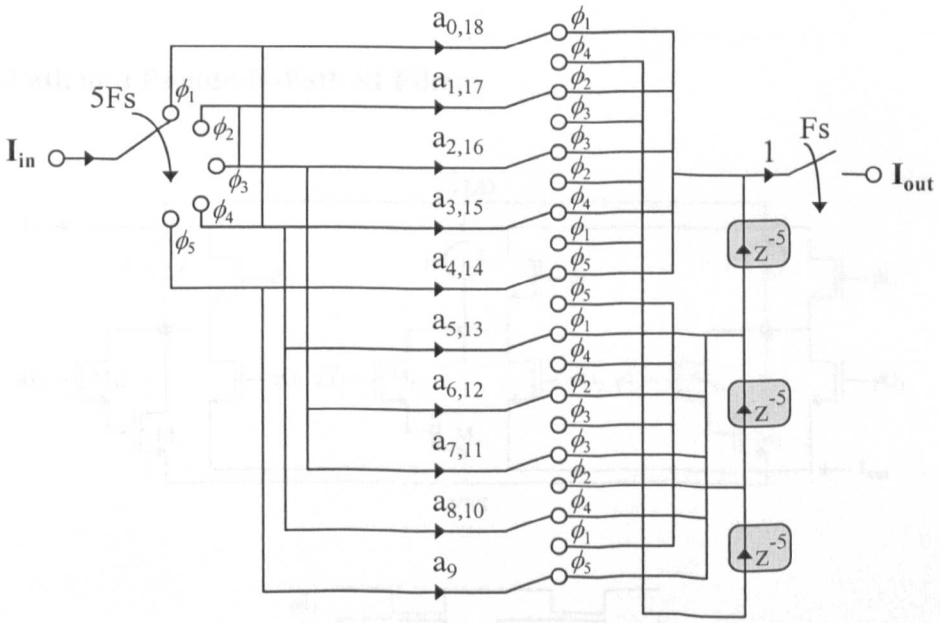


Figure 2.18 A linear phase, 19 tap FIR decimator(5×) with a single commutator topology[83]

In [102], an SI bandpass filter realised as a cascade of a lowpass filter clocked at a higher rate of 72MHz and a highpass filter clocked at a lower rate of 36MHz demonstrated a significant reduction in component spread of 86.4% and total area of 40.4% over a single rate example. A SI single-path-frequency-translated(SPFT) narrowband (relative bandwidth = 0.4%) bandpass filter was demonstrated using cascade biquad decimators and

interpolators. Compared to an equivalent single rate version, the multirate SPFT design achieved a reduction in spread of 92.5% and total area of 91.1%, and also a significant improvement in passband sensitivity. However, biquad structures are known to be more sensitive than doubly terminated ladders and in the example, both the decimator and interpolator operated at the higher sampling frequency. This makes them non-optimum in terms of available settling time for the memory cells.

The author's contribution to this area[84-86,110] are ladder based SI decimators and interpolators which realise highly selective responses with transmission zeros in the stopband, maintain low sensitivity in the passband, and operate at the lower sampling frequency. The increased time available for the memory cells to settle enhances the prospective high frequency operation of the circuits. Details of the proposed decimators and interpolators are documented in Chapter 5 of this thesis.

E. N-Path and Pseudo-N-Path SI Filters

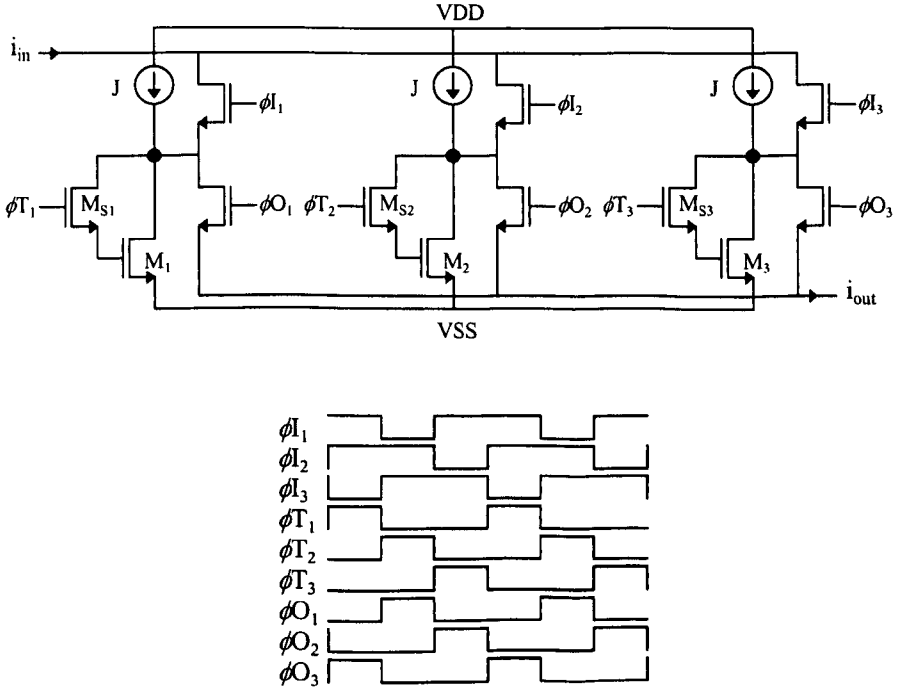


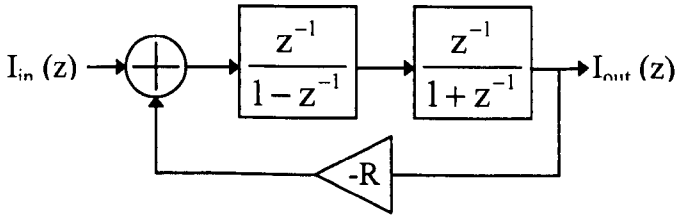
Figure 2.19 Pseudo-2-path $z \rightarrow -z^2$ transform resonator cell[93]

To date, very few, if any references can be found on the systematic design of N-path or pseudo-N-path SI filters although they are very well established in the SC technique. The only references to SI pseudo-N-path or similar circuits are found in SI bandpass sigma-delta($\Sigma\Delta$) modulator systems[93,94]. In [93], a pseudo-N-path resonator using the $z\rightarrow -z^2$ lowpass to bandpass transform was proposed. The cell, which is shown in Fig. 2.19, essentially consists of three second generation memory cells connected in parallel. By a clever, but nevertheless complicated clocking scheme, the $z\rightarrow -z^2$ transform was achieved to yield a transfer function of

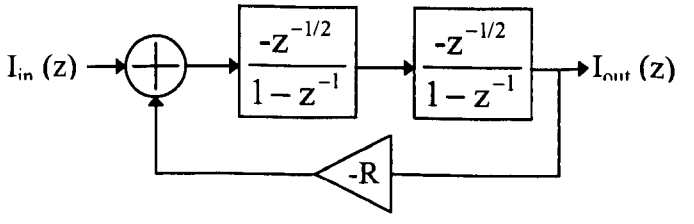
$$H(z) = \frac{-z^{-1}}{1+z^{-2}}$$

A different approach was taken[94] to realise $z\rightarrow -z^2$ transformed resonators. Unlike the N-path or pseudo-N-path techniques, the resonators were formed by a cascade of integrators/differentiators placed in the forward path of a closed loop system as shown in Figs. 2.20a,b to realise a Forward Euler transfer function of

$$H(z) = \frac{-z^{-2}}{1+z^{-2}}$$



(a)



(b)

Figure 2.20 Two feedback structures for realising a $z\rightarrow -z^2$ transformed resonator[94]

The structure (a) uses a cascade of a Forward Euler integrator and differentiator whereas structure (b) uses two Backward Euler integrators. A nominal feedback coefficient of R=2

is used. It can be shown[94] that deviation of this value, when R>2, will result in instability of structure (a), and shifting of the resonant frequency away from a quarter of the sampling frequency for structure (b).

The author's contribution to this area are $z \rightarrow -z$ transformed N-path and $z \rightarrow -z^2$ transformed pseudo-N-path fully balanced SI cells[95,111]. These cells can be used in stand-alone configurations or in the design of N-path and pseudo-N-path SI filters via a simple on-to-one replacement procedure. Details of these circuits are documented in Chapter 6 of this thesis.

2.5.2 AD Converters and Miscellaneous SI Systems

Apart from filters, a diverse range of other SI applications can be found. These include Nyquist[89,103] and oversampling[47,93,94] AD converters, mixers[87], comparators[88], multipliers[91], phase lock loops[90], pulse width modulators and oscillators[92].

2.6 INTEGRATED FILTER DESIGN AUTOMATION AND XFILT

In the race to shorten design cycles and increase integration, it is clear that pace and progress are digital driven. Advanced and efficient tools such as VHDL or Verilog are available to the digital designer for simulation, analysis and synthesis, to the point where digital design is now more akin to a task in programming. In stark contrast, analogue interface designs, while occupying a relatively small part of a mixed-signal chip, require a disproportionate amount of time to design, test and debug. This is due to the complex relationships that exist between circuit performance and circuit variables in analogue designs. As a consequence, efficient analogue design tools are lagging far behind their digital counterparts.

On the SI scene, some attempts have been made to address this problem. A CAD system named SCADS has been introduced for the automated design of SI filters[96,97]. It uses a knowledge based approach and a top-down methodology as shown in Fig. 2.21. The part enclosed by a dotted-line box is the XFILT[99,101] filter and equaliser compiler which will

be discussed in greater detail later. Design specifications are first entered and approximation routines then generate a passive RLC prototype which is used to synthesise the block-level SI filter. At this point, a switched-netlist simulator can be used to verify for correct ideal responses and to perform sensitivity and noise simulations. The noise information is passed on to the transistor synthesis algorithm, where it constitutes part of a set of design rules used for determining transistor dimensions and bias current levels. Significant effects of interconnect capacitance and parasitics are accounted for by post layout extraction and iteratively optimising the design using a SPICE like simulator until all design specifications are satisfied.

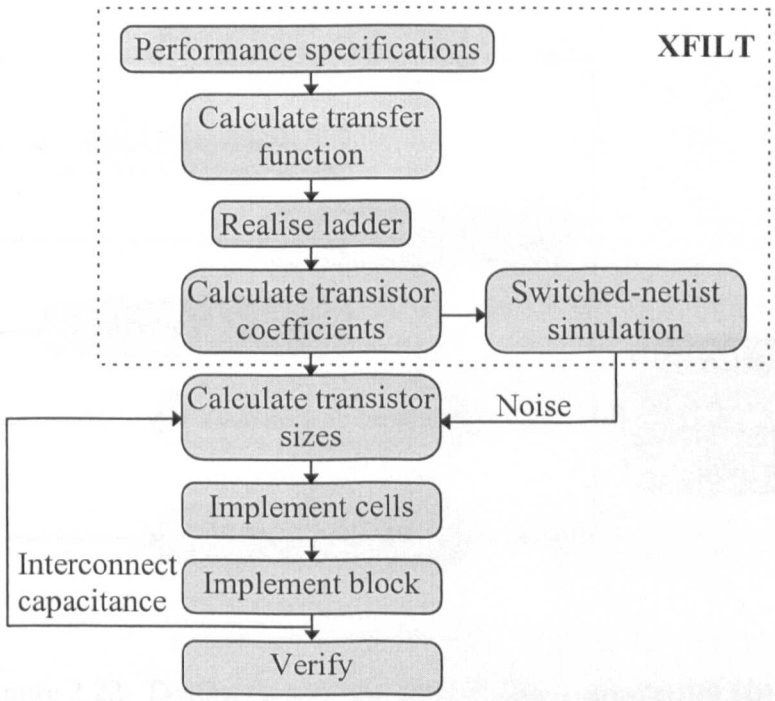


Figure 2.21 Design flow of the SCADS SI filter design system[96]

The XFILT[99,101] filter and equaliser compiler was designed as a general filter synthesis program capable of generating passive-RLC, active-RC, SC, gm-C and SI filters with classical or arbitrary approximations. The design suite includes a built in general optimiser and external sockets for interfacing to switched-network[100,108] and SPICE type simulators. The general system structure of XFILT is shown in Fig. 2.22. The graphical interface is based on the X11-windows[109] system while the rest of the program is written in C. The design flow starts with the entering of desired filter specifications. In the

approximation step, routines are employed to fit a function to the prescribed response. Realisation of both ladder and cascade biquad filters are possible. If the ladder option is chosen, a passive prototype is synthesised by conventional partial/complete pole removal methods. For active filters, the passive prototype can be realised as one of the many possible active filter decompositions[107] in any of the techniques previously described. If the cascade biquad option is chosen instead, the high order transfer function will be realised as a cascade of second order sections with various optional pole-zero pairing strategies.

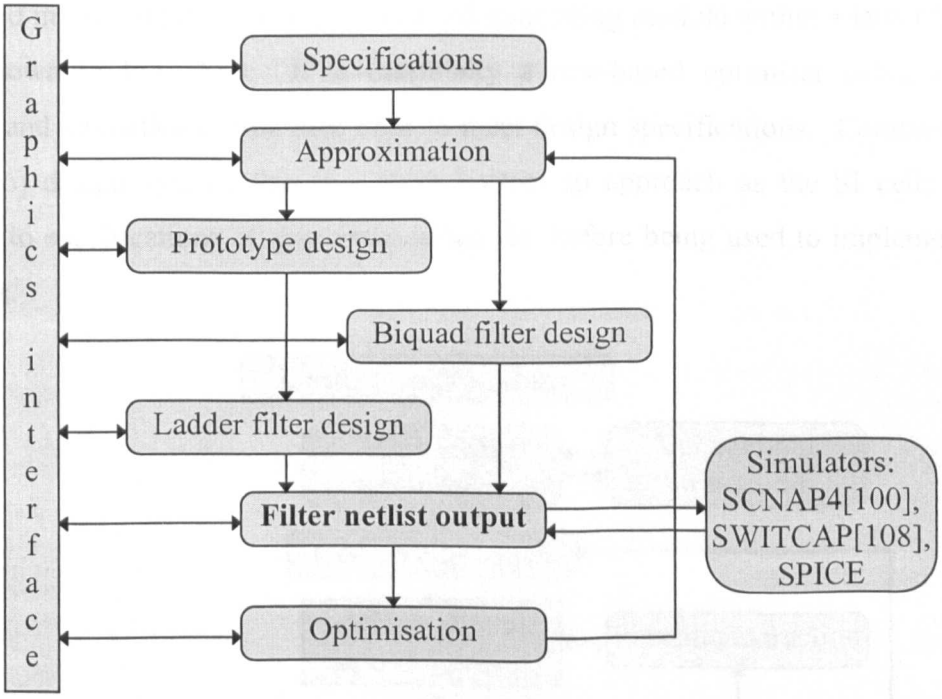


Figure 2.22 Design flow of the XFILT filter compiler[99,101]

A netlist of the selected filter type is produced and this can then be simulated using SCNAP4[100] or SWITCAP[108] for switched-networks, or SPICE for continuous-time circuits. If the design is satisfactory, the process is ended. Otherwise, the response of the filter can be optimised and the corrected response fed back to the Approximator to generate a new design. Throughout the entire design flow, there is constant interaction with the user entering commands and choices via menu buttons, while design information is output via the graphics window, and a UNIX running window in the background.

The contribution of the author is to the SI filter design process. Specifically, the main tasks involved creating novel SI circuits and structures to add on to the existing SI design library, which currently supports both single-ended or fully-differential cascade biquad and ladder designs. Further down the structural hierarchy, the building blocks consist of integrators and differentiators, while the memory cells can be of either first or second generation type. Detailed information on XFILT can be obtained by consulting the reference manual[101].

An SI cell design automation tool named ASIMOV(A SI MOdule generation enVironment) is described in [98], where it functions as a cell generating module within a larger SI design system shown in Fig. 2.23. It is essentially a rule-based optimiser using analytical equations and heuristics to fine tune cells to meet design specifications. Compared to the SCADS[96] design system, this is a more bottom-up approach as the SI cells are first optimised to specifications of gain error, offset etc. before being used to implement larger SI systems.

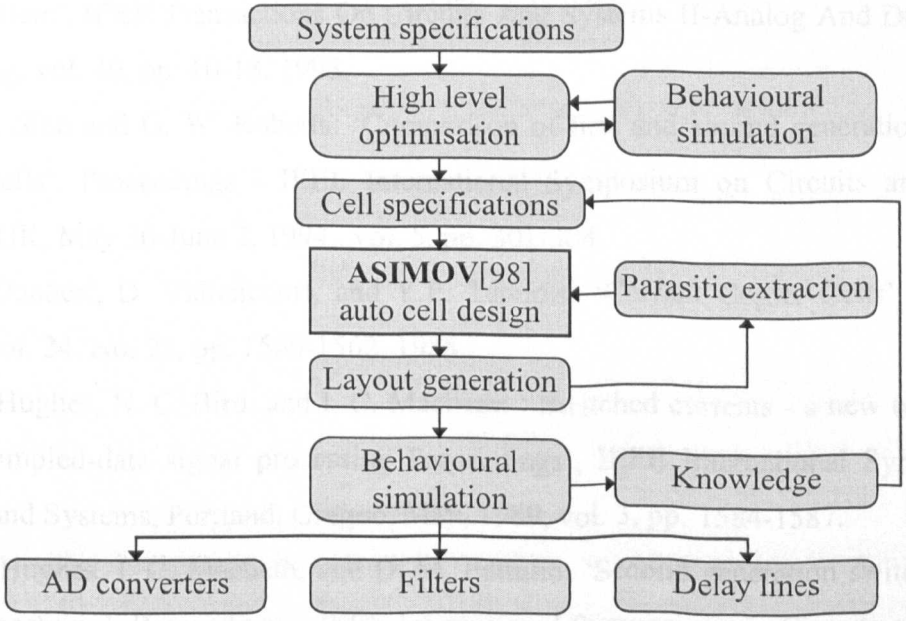


Figure 2.23 SI design flow and ASIMOV[98]

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CHAPTER 3:
SWITCHED-CURRENT LADDER FILTER DESIGN TECHNIQUES

3.1 INTRODUCTION

This chapter addresses some of the design issues related to high order and wideband SI filter design. The design of switched-current(SI) filters is a complex, multiple criteria optimisation procedure. Some common objectives are to minimise sensitivity of amplitude response to component variations, component value spread, total area requirement, power, noise, and non-ideal effects. In particular, emphasis is placed on low sensitivity and low component value spread structures.

3.2 GENERAL SI LADDER DECOMPOSITIONS

Active filters simulating the internal workings of doubly-terminated passive ladders are well known to possess superior sensitivity to component tolerances over cascade biquad implementations[2]. The general SI ladder derived design method is based on matrix decompositions[9]. A passive ladder is described by the nodal equation

$$(s\mathbf{C} + s^{-1}\Gamma + \mathbf{G})\mathbf{V} = \mathbf{J} \tag{3.1}$$

(where **C**, Γ and **G** are admittance matrices formed by the contributions of capacitors, inductors and resistors respectively. **V** and **J** are vectors representing the nodal voltages and input current sources). The voltage vector **V** is transformed into a current vector **I** using a scaling resistance of 1Ω.

$$(s\mathbf{C} + s^{-1}\Gamma + \mathbf{G})\mathbf{I} = \mathbf{J} \tag{3.2}$$

Applying the bilinear-transformation, $s \rightarrow \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}$, and some manipulation gives

$$(\psi^{-1}\mathbf{A} + \phi\mathbf{B} + \mathbf{D})\mathbf{I} = (1+z)\,\mathbf{J} \tag{3.3}$$

where **I** is the current variable, $\mathbf{A} = (2/T)\mathbf{C} + (T/2)\Gamma - \mathbf{G}$, $\mathbf{B} = 2T\Gamma$ and $\mathbf{D} = 2\mathbf{G}$. $\psi = z^{-1}/1-z^{-1}$ and $\phi = -1/1-z^{-1}$ represent Forward and Backward Euler integrators respectively.

The 'Left' type decompositions are obtained by factorising the **A**-matrix as $\mathbf{A} = \mathbf{A}_l\mathbf{A}_r$ to yield

$$\mathbf{A}_l\mathbf{W} = (\psi\mathbf{B} + \mathbf{D})\mathbf{I} - (1+z^{-1})\,\mathbf{J} \tag{3.4a}$$

$$\mathbf{A}_r\mathbf{I} = -\phi\mathbf{W} \tag{3.4b}$$

W is an intermediate variable, introduced so that the system can be expressed as two subsystems in terms of the operators ϕ and ψ.

'Right' type decompositions are obtained by factorising the inverse inductance matrix as $\mathbf{B} = \mathbf{B_l B_r}$ to yield

$$\mathbf{AI} = -\phi(\mathbf{B_l W}+\mathbf{D})\mathbf{I}+\lambda\mathbf{J} \tag{3.5a}$$

$$\mathbf{W} = \psi\mathbf{B_r} \tag{3.5b}$$

where $\lambda = (1+z^{-1})/(1-z^{-1})$ represents a bilinear integrator. Various subsets such as **A** = **LU**, **A** = **UL**, **A** = **IA**, **A** = **AI** for 'Right' type decompositions and **B** = **LU**, **B** = **UL**, **B** = **IA**, **B** = **AI** for 'Left' type decompositions will be used for performance comparison.

3.3 HIGH ORDER SI FILTER DESIGN

High order filters pose many design challenges. Typical obstacles facing the designer, among many, are high sensitivity, high spreads and large chip area. In high order active filter design, low sensitivity is crucial to preserve response accuracy, and this usually requires the use of ladder derived realisations. Doubly-terminated passive ladders are well known for their low sensitivity behaviour[3]. By simulating the internal workings of the ladder filter, active circuits seek to inherit this low sensitivity property. A large spread(>100) in component values also increases sensitivity as it renders the design prone to loss of response accuracy due to the finite precision of fabrication processes. At the circuit or transistor level, enhanced memory cells[4,5,6] are required in practical realisations to minimise non-ideal factors like charge injection and low conductance ratios.

In the sub-sections that follow, some of these problems are discussed and a ladder prototype manipulation scheme[10] is used to advantage in very high order SI filter designs, yielding a dramatic reduction in component spread and area. Modifications to the Left- and Right-decomposition methods[8] are presented to minimise input circuitry and also to overcome some inherent dynamic-range scaling problems.

3.3.1 The Bilinear-LDI Method

The approximate-LDI method[14], when applied to ladder based designs, suffers from the termination error problem. This gives rise to distortion in the passband which gets more pronounced for low clock-to-signal frequency ratios. The exact-LDI method[23] on the other hand, allows exact simulation of passive prototype filters via indirect use of LDI variables. In comparison, the bilinear transformation is exact, as it maps the entire left half s-plane into the unit circle of the z-plane, resulting in distortion free amplitude response and guaranteed stability. Direct realisation of SI filters using bilinear integrators has been demonstrated [11,12,13]. Matrix methods[8] for designing SI ladder filters using bilinear integrators[13] have been presented. However, as this method factorises the component matrices directly, it does not permit any manipulation of the decomposed matrices to facilitate the removal of ill-conditioned entries that give rise to large spreads.

Alternatively, there is the bilinear-LDI method, where the bilinear transformation is used together with Euler integrators[9,10,15], to give distortion free amplitude responses even for low clock to signal frequency ratios. The form that some of the matrices take in this method[9,10] is amenable to manipulation which allows component value spread to be significantly reduced.

3.3.2 Modified Matrix Decompositions for SI Ladder Filter Design

Beginning with (3.2), performing the bilinear transformation, $s \rightarrow \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}$, results in

$$\left[\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}\mathbf{C}+\frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\Gamma+\mathbf{G}\right]\mathbf{I}=\mathbf{J} \tag{3.6}$$

Equation (3.6) can be directly implemented by bilinear integrators after decomposition[8] into two first order sub-systems. To allow the use of LDI or Euler integrators, multiply through the system by $(1+z^{-1})/(1-z^{-1})$ to give

$$\left[\frac{2}{T}\mathbf{C}+\frac{T}{2}\left(\frac{1+z^{-1}}{1-z^{-1}}\right)^{2}\Gamma+\frac{1+z^{-1}}{1-z^{-1}}\mathbf{G}\right]\mathbf{I}=\frac{1+z^{-1}}{1-z^{-1}}\mathbf{J} \tag{3.7}$$

Note that

$$\left(\frac{1+z^{-1}}{1-z^{-1}}\right)^2 = 1-4\left(\frac{z^{-1}}{1-z^{-1}}\right)\left(\frac{-1}{1-z^{-1}}\right) \qquad \text{and} \qquad \frac{1+z^{-1}}{1-z^{-1}} = 1+2\frac{z^{-1}}{1-z^{-1}} \ ,$$

substitute into (3.7) to yield

$$\left[\frac{2}{T}\mathbf{C}+\left(\frac{T}{2}+2T\frac{z^{-1}}{\left(1-z^{-1}\right)^2}\right)\Gamma+\left(1+2\frac{z^{-1}}{1-z^{-1}}\right)\mathbf{G}\right]\mathbf{I} = \frac{1+z^{-1}}{1-z^{-1}}\mathbf{J} \tag{3.8}$$

The system described by equation (3.8) can be decomposed for SI implementation by using the 'Left' and 'Right' methods shown previously. 'Left' decomposition systems are preceded by a $(1+z^{-1})$ term which needs physical implementation, while a bilinear integrator is required at the input to 'Right' decomposition systems[9] to realise the bilinear zero at half the clock frequency. Similar input stages are also noted in other bilinear-LDI methods[15,16]. These can all be avoided and will result in a reduced component count, saving on chip area and current consumption. For Left-decomposition systems, a modified method[10] is presented, which does not involve the $(1+z^{-1})$ term but only simple feed-in branches.

A. Modified Left-Decomposition Method

Starting with equation (3.8) as

$$\left[\frac{2}{T}\mathbf{C}+\frac{T}{2}\left(1+4\frac{z^{-1}}{\left(1-z^{-1}\right)^2}\right)\Gamma+\left(1+2\frac{z^{-1}}{1-z^{-1}}\right)\mathbf{G}\right]\mathbf{I} = \frac{1+z^{-1}}{1-z^{-1}}\mathbf{J} \tag{3.9}$$

Divide both sides by z^{-1} and rewrite as

$$(\psi^{-1}\mathbf{A}+\phi\mathbf{B}+\mathbf{D})\mathbf{I} = (1+z)\mathbf{J} \tag{3.10}$$

where the **A** matrix is now $\mathbf{A} = (2/T)\mathbf{C}+(T/2)\Gamma+\mathbf{G}$.

Factorising $\mathbf{A}=\mathbf{A}_l\mathbf{A}_r$ and introducing the intermediate variable **W**, equation (3.10) can be expressed as

$$\mathbf{A}_l\mathbf{W} = -(\phi\mathbf{B}+\mathbf{D})\mathbf{I}+2\mathbf{J} \tag{3.11a}$$

$$\mathbf{A}_r\mathbf{I} = \psi\mathbf{W}+\mathbf{A}_l^{-1}\mathbf{J} \tag{3.11b}$$

As can be seen from (3.11a) and (3.11b), the inputs to the modified system are now $2\mathbf{J}$ and $\mathbf{A}_l^{-1}\mathbf{J}$. The input $2\mathbf{J}$ is just a single feed-in branch. For (3.11b), as **J** is a column vector with only one entry in the first row, i.e. $\mathbf{J}=[\ \text{Jin}\ \ 0\ \ \ldots\ 0\ ]^T$, a minimum of one input branch results only if $\mathbf{A}_l^{-1}$ is diagonal or upper triangular. This requires **A** to be factorised

as $\mathbf{A}=\mathbf{I_D A}$ or $\mathbf{A}=\mathbf{UL}$, where $\mathbf{I_D}$=identity matrix. For $\mathbf{A}=\mathbf{LU}$ and $\mathbf{A}=\mathbf{AI_D}$, $\mathbf{A_I}^{-1}$ will be a lower triangular or tri-diagonal matrix and this will give rise to two input branches. Details of the modified Left decomposition derivation procedure can be found in Appendix A.

An example of a 6th order elliptic bandpass filter is given to illustrate the method. Table 3.1 lists the design data and specifications for the passive prototype shown in Fig. 3.1.

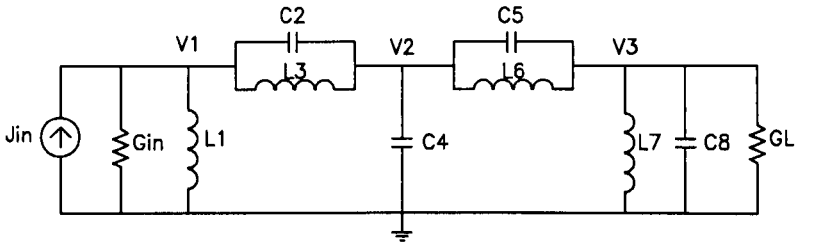


Figure 3.1 6th-order bandpass ladder prototype

To compensate for the frequency warping effect of the bilinear transform, a pre-warped scaling factor $\omega_s = \pi(f_p/F_s)$ was used to obtain the component values shown in Table 3.1; $f_p = F_s/\pi \tan(\pi f_o/F_s)$, f_o is the filter cutoff frequency and F_s is the clock frequency. The nodal matrices describing the prototype are written as

$$\mathbf{C}=\begin{bmatrix} C2 & C2 & \\ C2 & C2+C4+C5 & C5 \\ & C5 & C5+C8 \end{bmatrix}=\begin{bmatrix} C_{11} & C_{12} & \\ C_{21} & C_{22} & C_{23} \\ & C_{32} & C_{33} \end{bmatrix} \tag{3.12a}$$

$$\Gamma=\begin{bmatrix} L1^{-1}+L3^{-1} & L3^{-1} & \\ L3^{-1} & L3^{-1}+L6^{-1} & L6^{-1} \\ & L6^{-1} & L6^{-1}+L7^{-1} \end{bmatrix}=\begin{bmatrix} \Gamma_{11} & \Gamma_{12} & \\ \Gamma_{21} & \Gamma_{22} & \Gamma_{23} \\ & \Gamma_{32} & \Gamma_{33} \end{bmatrix} \tag{3.12b}$$

$$\mathbf{G}=\begin{bmatrix} Gin & & \\ & 0 & \\ & & GL \end{bmatrix} \tag{3.12c}$$

$$\mathbf{J}=\begin{bmatrix} J \\ 0 \\ 0 \end{bmatrix} \tag{3.12d}$$

$$\mathbf{I}=\begin{bmatrix} I_1 \\ -I_2 \\ I_3 \end{bmatrix} \tag{3.12e}$$

Using (3.10a), equations (3.11a) and (3.11b) can be expanded in terms of **W** and **I** respectively to give

$$\begin{bmatrix} W_1 \\ W_2 \\ W_3 \end{bmatrix} = \begin{bmatrix} U_{11}^{-1}[-(\phi B_{11} + D_{11})I_1 + \phi B_{12}I_2 - U_{12}W_2 + 2J] \\ U_{22}^{-1}[-\phi B_{21}I_1 + \phi B_{22}I_2 - \phi B_{23}I_3 - U_{23}W_3] \\ U_{33}^{-1}[\phi B_{32}I_2 - (\phi B_{33} + D_{33})I_3] \end{bmatrix} \tag{3.13a}$$

$$\begin{bmatrix} I_1 \\ -I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} L_{11}^{-1}[\psi W_1 + U_{11}^{-1}J] \\ L_{22}^{-1}[\psi W_2 - L_{21}I_1] \\ L_{33}^{-1}[\psi W_3 + L_{32}I_2] \end{bmatrix} \tag{3.13b}$$

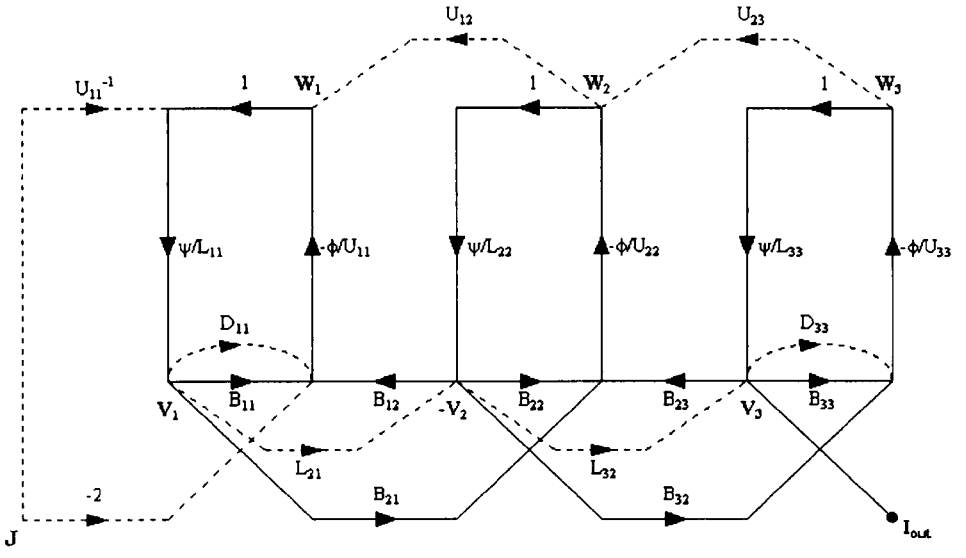
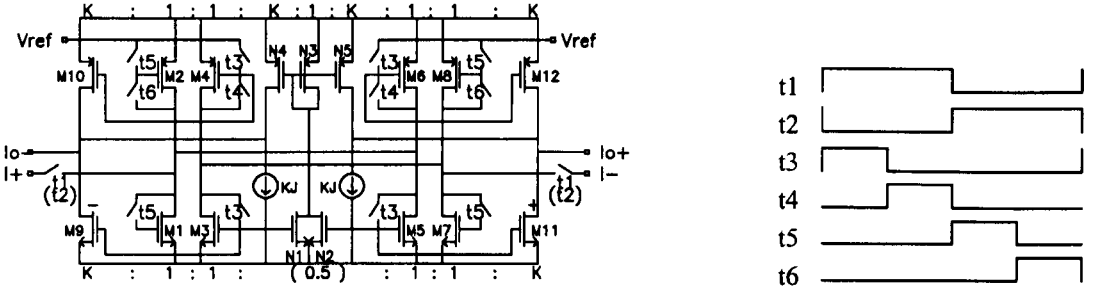


Figure 3.2 Modified Left-UL SFG for the 6th order bandpass filter

The modified Left-UL signal-flowgraph representing (3.13a) and (3.13b) is shown in Fig. 3.2, where the solid branches represent integrated inputs, while the dotted branches are feed-through signals connected directly to the integrator summing nodes. The ψ and $-\phi$ branches are realised by Forward and Backward Euler integrators, shown in simplified, fully-balanced form with S^2I memory cells[5] and common-mode feedforward[7] in Fig. 3.3. Transistors M1, M3, M5 and M7 form the balanced integrator pair with their connected drains acting as the current summing node, while transistors M2, M4, M6 and M8 serve the dual role of current source in phases t3, t5 and fine error memory in phases t4, t6. The outputs of the integrator are mirrored by transistors M9-M12 with a scaling factor k, representing the transconductance(gm) which is proportional to the transistor aspect ratio(W/L). A common-mode feedforward(CMFF)[7] circuit, formed by transistors

N1 to N5 is used to reject common-mode signals. Since the drains of N1 and N2 are connected together, twice the common-mode current is generated and is halved by setting their transistor ratios to 0.5. This is mirrored and scaled by the PMOS transistors N3-N5 to the output to eliminate the common-mode signals. Thus, common-mode currents which might seriously affect biasing and dynamic range are not propagated but confined to each block. The inputs indicated by I+, I-, produce Forward Euler integration when switched in t2 and Backward Euler integration when switched in t1. Feed-through inputs connect directly to the common summing nodes. A sample-and-hold circuit is required at the input for proper operation with the S^2I memory cells.



$$\text{Forward(t2 input): } \psi = k\frac{z^{-1}}{1-z^{-1}}, \quad \text{Backward(t1 input): } \phi = -k\frac{1}{1-z^{-1}}$$

Figure 3.3 Fully balanced S^2I Euler integrator and clock waveforms

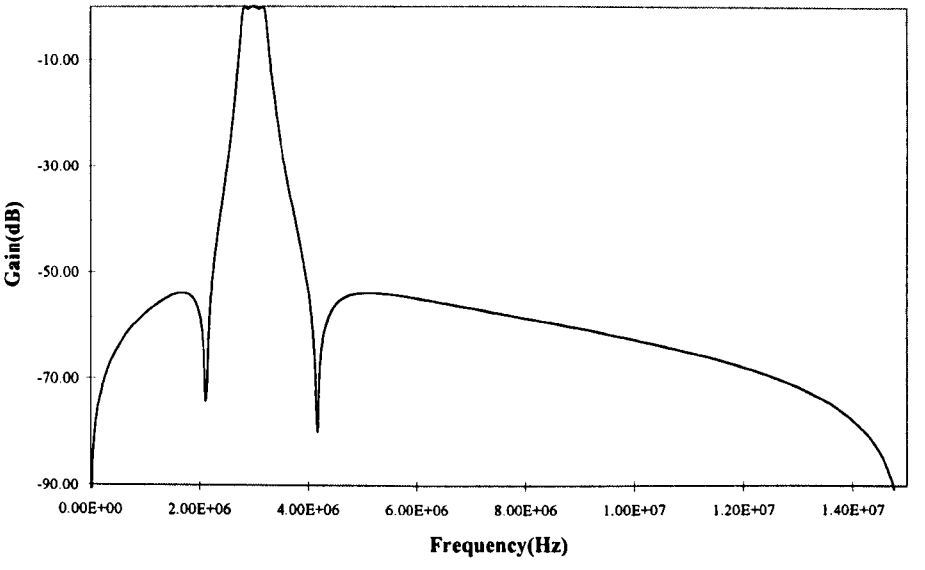


Figure 3.4 Simulated response of 6th order modified Left-UL bandpass switched-current filter

The branch coefficients of the filter structure are listed in Table 3.1. Table 3.2 lists the design statistics for the existing and modified Left-decomposition designs, showing comparable figures for spread and total gm units. The simulated amplitude response of the SI filter is shown in Fig. 3.4.

Table 3.1 Design data for the 6th order modified Left-UL band-pass filter

Filter specification:			
Lower passband edge	2.8MHz	Upper passband edge	3.2MHz
Lower stopband edge	2.0MHz	Upper stopband edge	4.0MHz
Stopband attenuation	> 50dB	Passband ripple	0.5dB
Normalised prototype component values:			
Gin = 1.0S		C5 = 4.00037e+2	
L1 = 5.44037e-1		L6 = 1.15015e-2	
C2 = 3.61624e+1		L7 = 5.25959e-4	
L3 = 5.43699e-1		C8 = 1.78902e+4	
C4 = 4.08246e+2		GL = 1.93389e-3	
Transistor ratios for the modified Left-UL SI bandpass filter			
x7	2.4016e-01	x17	6.7799e-02
x8	8.6519e-02	x18	6.3152e-01
x9	5.9308e-01	x19	6.2370e-01
x10	7.4548e-02	x20	7.3350e-01
x11	5.0915e-02	x21	1.6403e-01
x12	6.1768e-01	x22	1.6815e-01
x13	8.4236e-02	x24	4.0529e-02
x14	1.6372e-01	x25	1.2835e-01
x15	5.2138e-01	x26	1.000
x16	8.0639e-02	R27, R28	1.000
gm spread 24.67		Total gm 2365.92 units	
Clock frequency 30MHz			

Table 3.2 Statistics for Left-Decomposition designs

Decomposition	Spread	Total units
Left-LU	18.60	2186.24
Left-UL	22.67	2670.98
Left-IA	21.77	2539.46
Left-AI	20.63	2416.50
Mod Left-UL	24.67	2365.92
Mod Left-IA	25.66	2447.45

B. Modified Right-Decomposition Method

Right-decomposition SI systems are described[9] by

$$\mathbf{AI} = -\phi[\mathbf{B}_1\mathbf{W} + \mathbf{DI}] + \frac{1+z^{-1}}{1-z^{-1}}\mathbf{J}$$
$$\mathbf{I}_D\mathbf{W} = \psi\mathbf{B}_r\mathbf{I} \qquad (3.14)$$

where matrix **B** is factorised instead of **A** and $\mathbf{I}_D$ is the identity matrix. The bilinear input stage connects to the summing node of the first Backward Euler integrator[8,9] as shown in Fig. 3.5a. This is not a good solution for several reasons. Firstly, using a bilinear integrator requires the input to be sample-and-held, incurring circuitry overheads. Secondly, because the bilinear integrator is in cascade with the rest of the ladder structure, the pole at DC created by the denominator will make it impossible to achieve optimum dynamic-range scaling. The bilinear integrator will saturate well before any of the Euler integrators in the ladder structure. A better solution is to replace the bilinear integrator by a simpler $(1+z^{-1})$ FIR stage similar to Left-decomposition designs, which connects to the integrating input as shown in Fig. 3.5b. This way, the zero at Fclk/2 will be realised while avoiding the pole at DC. Alternatively, omit the input stages altogether and feed J_{in} directly to the integrating input as shown in Fig. 3.5c. However, this will give rise to the familiar LDI distortion which has to be corrected by applying an inverse weighting of $1/\cos(\omega T/2)$[17].

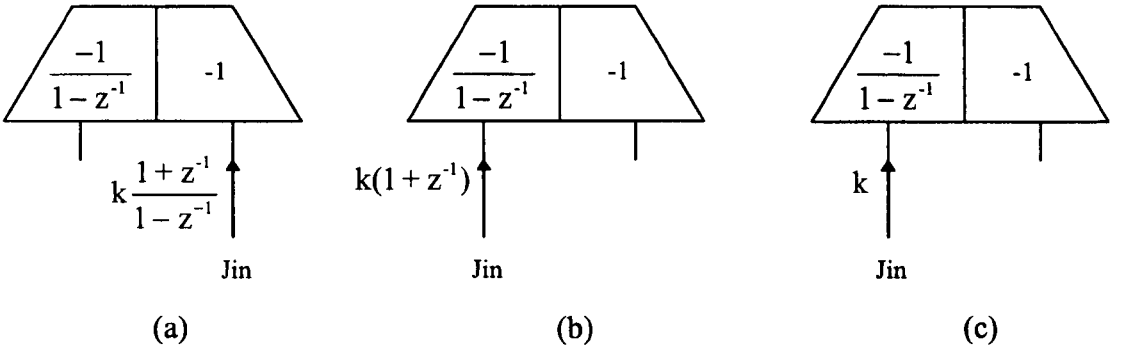


Figure 3.5 Input arrangements for Right-Decomposition designs
(a) Original bilinear input
(b) Simplified bilinear input using only $(1+z^{-1})$ stage
(c) Direct input with LDI distortion resulting

3.3.3 Spread Reduction For High Order Ladder Filter Design

The design of practical high order filters can sometimes be hindered by large component spreads. Take the example of an elliptic lowpass filter, with a passband ripple of ≤ 0.2dB, cutoff frequency of 1MHz and clocked at 10MHz. Table 3.3 gives a comparison of spreads and total gm between SI filters designed by matrix methods[8] using double-sampled bilinear integrators[13] and cascade biquads[4].

Table 3.3 Design statistics for different high order SI filters

Filter	Bilinear-Ladder		Cascade Biquad	
order	gm Spread	Total gm	gm Spread	Total gm
15	>1e+06	>1e+06	3706.13	1463850.66
17	>1e+06	>1e+06	12370.55	>5e+06
19	>1e+06	>1e+06	41286.70	>5e+06
21	>1e+06	>1e+06	140666.69	>5e+06

The figures obtained are clearly too large for practical implementation. Unfortunately, neither design formulation involves the **A**-matrix which is key to spread reduction[10].

In SI circuits, transmission zeros are realised by cross-coupled branches represented by the off-diagonal entries in the **A**-matrix. From the definition of **A** following (3.10), it can be seen that these entries can be cancelled by letting $(2/T)C_i = (T/2)L_i^{-1}$. The required capacitance values are changed to $C_i = -(T^2/4)L_i^{-1}$. The zeros now occur at $s^2 = -1/(L_iC_i) = 4/T^2 = (\pm 2F_s)^2$ on the real axis. A distortion to the filter response is thus incurred, which can be corrected during approximation with the transmission zeros shifted to $\pm 2F_s$ on the real axis. Both spread and total component count can be substantially reduced this way.

Consider the example of a 21st order elliptic lowpass video filter designed for a passband ripple of ≤ 0.6dB, cutoff frequency of 10MHz and clocked at 100MHz. The active passband order is maintained at 21. In case (a) of Table 3.4, transistor spreads and total gm units are tabulated for different designs with a full 21st order stopband. It can be seen that the values are prohibitively large for practical realisation. In case (b), a pair of high frequency transmission zero are shifted to ±2Fs on the real axis of the s-plane, leaving an active stopband order of 19. A pair of off-diagonal elements in the **A**-matrix is cancelled as a result of the negative capacitance, to yield remarkably reduced spreads and total gm units.

In case (c), 4 pairs of transmission zeros are shifted to ±2Fs on the real axis of the s-plane, a 13th order active stopband results and 4 negative capacitances are introduced into the prototype ladder and lead to even lower spread figures. For the Right-LU and Right-UL designs, this represents a reduction in spread of 99.94% and total area of 99.83%. Beyond this, spreads for certain designs could increase and significant deterioration of transition band steepness results. The specifications and component values of the passive prototype filter for case (c) are listed in Table 3.5, and Fig. 3.6 shows the prototype schematic.

Table 3.4 Circuit statistics for different designs of the 21st order lowpass filter

S: gm Spread		T: Total gm units				
	Left-LU	Left-UL	Left-IA	Right-LU	Right-UL	Right-IB
(a)S	22629.69	164855.01	164852.75	24977.71	24977.65	24977.59
T	328206.65	11951881.6	9162499.7	1891486.2	1891485.3	1877528.8
(b)S	132.97	49.33	50.05	58.39	58.39	58.39
T	12278.80	9411.400	9076.92	13274.10	13274.10	13780.00
(c)S	47.94	23.26	23.41	14.83	14.83	27.31
T	4459.35	4293.17	4114.32	3302.34	3302.34	6321.02

Table 3.5 Filter specifications and normalised component values for 21st order lowpass prototype of case(c)

Passband ripple	0.6dB					Passband edge	10MHz		
Stopband attenuation	>50dB					Stopband edge	10.005MHz		
R1	1.000	C8	9.302	C15	1.630	L22	1.924	C29	3.040
C2	5.994	C9	-0.227	L16	2.945	C23	3.758	C30	9.849
C3	-0.246	L10	4.403	C17	5.627	C24	5.010	L31	0.864
L4	4.066	C11	9.362	C18	2.743	L25	1.607	C32	1.981
C5	9.071	C12	-0.226	L19	2.359	C26	3.231	R33	1.000
C6	-0.230	L13	4.420	C20	4.545	C27	6.164		
L7	4.351	C14	7.812	C21	3.882	L28	1.358		

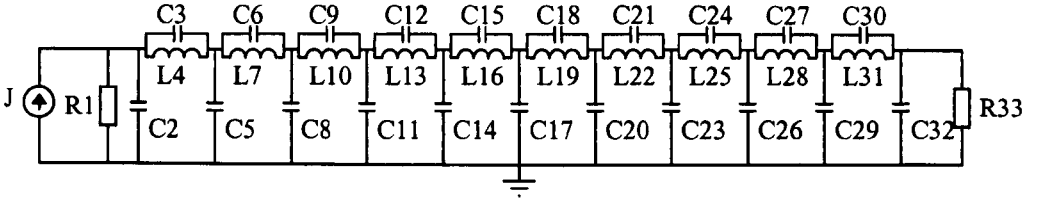


Figure 3.6 21st order passive prototype lowpass ladder filter

The signal flowgraph for the Right-LU decomposition design of case (c) is shown in Fig. 3.7. It can be seen that the cross-coupling feed-through branches on the left half side have been eliminated. The 'B' and 'F' branches represent Backward Euler and Forward Euler integrators respectively, while X78 at the input is the bilinear integrator required for Right-decomposition designs. This was eliminated in the design, as previously discussed for the case of Fig. 3.5c. The resulting LDI distortion was corrected by applying an inverse weighting of $1/\cos(\omega T/2)$.

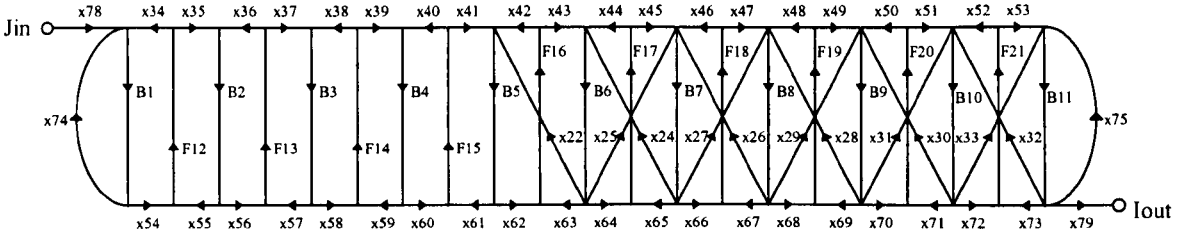


Figure 3.7 Right-LU decomposition SFG for 21st order lowpass filter

The branch coefficient values of the filter structure are listed in Table 3.6. The simulated response of this filter implemented using the integrators of Fig. 3.3 is shown in Fig. 3.8. Good response accuracy is observed.

Table 3.6 Transistor ratios or branch coefficients of the 21st order SI lowpass filter

X22	2.047e-01	X37	2.938e-01	X52	3.964e-01	X67	3.024e-01
X23	1.792e-01	X38	3.250e-01	X53	1.603e+00	X68	3.314e-01
X24	2.899e-01	X39	3.019e-01	X54	2.200e-01	X69	2.928e-01
X25	2.651e-01	X40	3.168e-01	X55	4.021e-01	X70	3.641e-01
X26	3.429e-01	X41	2.939e-01	X56	2.835e-01	X71	2.718e-01
X27	3.385e-01	X42	4.509e-01	X57	3.356e-01	X72	5.957e-01
X28	3.591e-01	X43	4.041e-01	X58	2.971e-01	X73	2.643e-01
X29	4.055e-01	X44	5.032e-01	X59	3.217e-01	X74	2.972e-01
X30	3.278e-01	X45	4.560e-01	X60	3.027e-01	X75	1.666e-01
X31	4.093e-01	X46	5.356e-01	X61	3.159e-01	X77	4.090e-01
X32	2.492e-01	X47	5.018e-01	X62	3.059e-01	X79	1.00e+00
X33	2.272e+00	X48	5.418e-01	X63	3.132e-01	R80	1.00e+00
X34	6.890e-01	X49	5.406e-01	X64	3.113e-01	R81	1.00e+00
X35	2.704e-01	X50	5.146e-01	X65	3.085e-01		
X36	3.493e-01	X51	4.797e-01	X66	3.187e-01		
gm Spread	13.63		Total gm	3266.70 units		Fclk	100MHz

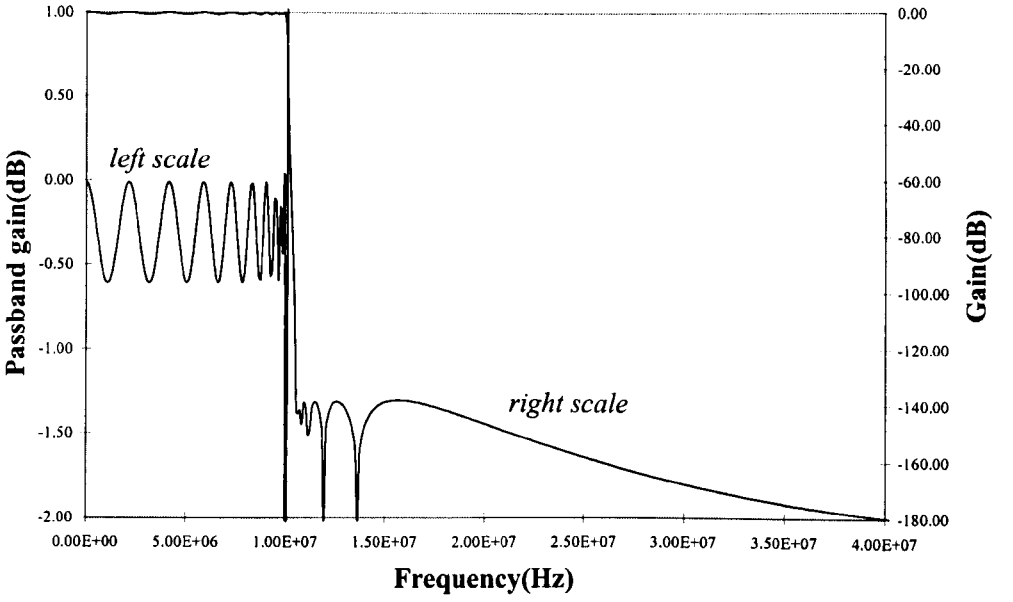


Figure 3.8 Simulated amplitude response of the 21st order lowpass filter

3.3.4 Sensitivity of the SI Filters

To estimate the sensitivity performance of the filters, the multiparameter sum sensitivity measure defined by

$$s(\omega) = \left[\sum_{i}^{m} \left(\frac{x_i \partial |H(\omega)|}{|H(\omega)| \partial x_i} \right)^2 \right]^{1/2} \tag{3.15}$$

was used to measure the sensitivity of the filter magnitude response $|H(\omega)|$ to deviations in transistor ratio coefficients x_i. The simulated passband sensitivity for the modified Left-UL bandpass SI filter is plotted in Fig. 3.9 together with the sensitivities of a modified Left-IA and existing realisations for comparison. The cascade biquad design has a relatively high overall sensitivity while sensitivity peaks at the passband edges characterise existing Left-decomposition[9] designs. In comparison, both the modified Left-UL and modified Left-IA designs clearly maintain low sensitivities throughout the passband.

The computed passband sum sensitivity of the 21st order lowpass filter is plotted in Fig. 3.10. Despite the cancellation of terms and the unconventional structure, the low sensitivity property is still preserved, which demonstrates the feasibility of realising very high order SI filters using the spread reduction technique. These building blocks have been incorporated

in the filter compiler XFILT[17] to enable ease of design and automatic generation of ladder and cascade structures. This makes it possible to evaluate and compare many different solutions to designs.

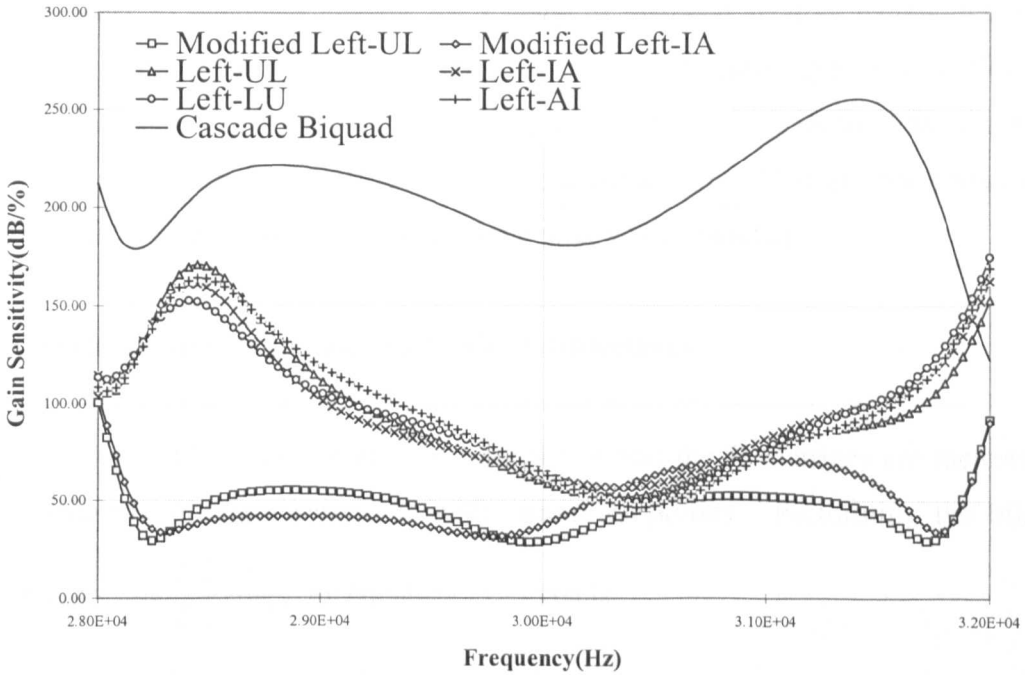


Figure 3.9 Amplitude response sensitivities of 6th order bandpass switched-current filters

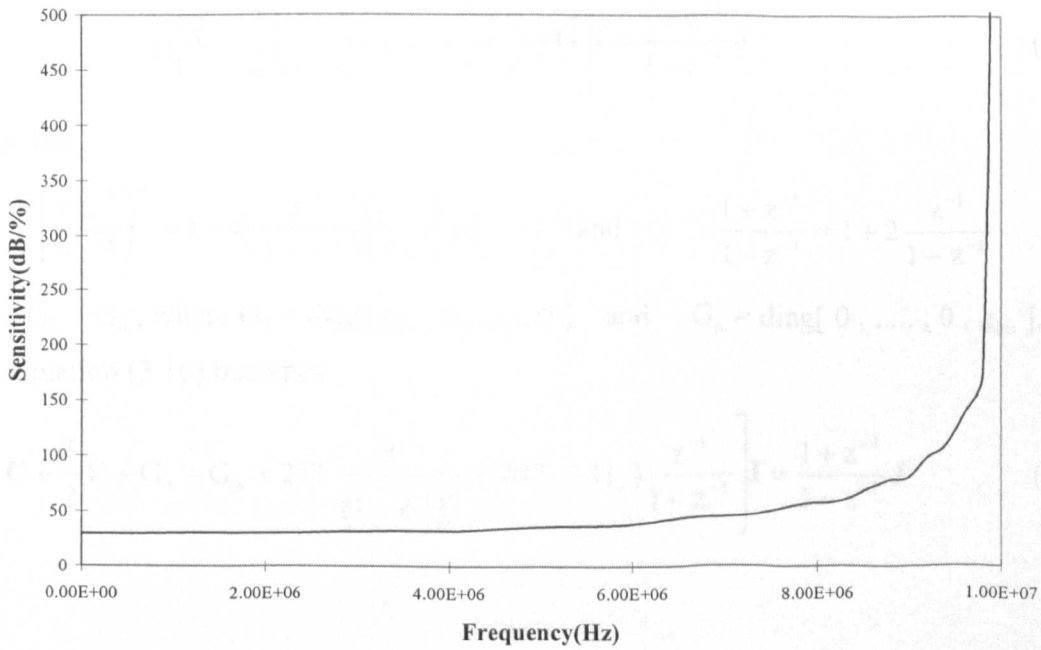


Figure 3.10 Passband amplitude response sensitivity of the 21st order lowpass switched-current filter

3.4 WIDE BAND SI FILTER DESIGN

Many filtering problems require wideband solutions, most notable of which are in voice band applications. As will be shown later, a comparison of average passband sensitivity for typical 6th order SI bandpass designs for a range of different relative bandwidths(RBW) reveals that leapfrog[2] and coupled-biquad based structures typically suffer from sensitivity problems at large RBWs. In this section, methods for wideband SI ladder filter design based on the UL-LU and LU-UL matrix decompositions[10] are presented, which preserve low passband sensitivity even for large relative bandwidths.

3.4.1 Switched-Current UL-LU And LU-UL Structures

In the UL-LU and LU-UL methods[10], both the **A** and the **B** matrices are factorised to yield significantly different structures with unique properties. Performing the bilinear-transformation, $s \rightarrow \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}$, on equation (3.2) yields

$$\left[\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}\mathbf{C}+\frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\Gamma+\mathbf{G}\right]\mathbf{I}=\mathbf{J}$$

Multiplying through by $(1+z^{-1})/(1-z^{-1})$ gives

$$\left[\frac{2}{T}\mathbf{C}+\frac{T}{2}\left(\frac{1+z^{-1}}{1-z^{-1}}\right)^{2}\Gamma+\frac{1+z^{-1}}{1-z^{-1}}\mathbf{G}\right]\mathbf{I}=\frac{1+z^{-1}}{1-z^{-1}}\mathbf{J} \qquad (3.16)$$

Noting that

$$\left(\frac{1+z^{-1}}{1-z^{-1}}\right)^{2}=1-4\left(\frac{z^{-1}}{1-z^{-1}}\right)\left(\frac{-1}{1-z^{-1}}\right) \qquad \text{and} \qquad \frac{1+z^{-1}}{1-z^{-1}}=1+2\frac{z^{-1}}{1-z^{-1}}$$

let $\mathbf{G} = G_l + G_n$, where $G_l = \text{diag}[\, g_{11}, 0, \ldots, 0\,]$ and $G_n = \text{diag}[\, 0, \ldots, 0, g_{nn}\,]$.
Then, equation (3.16) becomes

$$\left[\frac{2}{T}\mathbf{C}+\frac{T}{2}\Gamma+G_l+G_n+2T\Gamma\frac{z^{-1}}{\left(1-z^{-1}\right)^{2}}+2(G_l+G_n)\frac{z^{-1}}{1-z^{-1}}\right]\mathbf{I}=\frac{1+z^{-1}}{1-z^{-1}}\mathbf{J} \qquad (3.17)$$

A. The UL-LU Decomposition Method

Multiplying both sides of equation (3.17) by $(1-z^{-1})/z^{-1}$ and some rearranging yields

$$\left[\frac{1}{\psi}\mathbf{A} + \phi\mathbf{B} + zD_l + D_n\right]\mathbf{I} = (1+z)\mathbf{J} \tag{3.18}$$

where

$$\psi = \frac{z^{-1}}{1-z^{-1}}, \qquad \phi = \frac{1}{1-z^{-1}}, \qquad \mathbf{A} = \frac{2}{T}\mathbf{C} + \frac{T}{2}\Gamma - G_l + G_n, \qquad \mathbf{B} = 2T\Gamma,$$
$$D_l = 2G_l, \qquad D_n = 2G_n$$

Here, only Euler type integrator pairs(ϕ, ψ) are used and exactness of the amplitude response is preserved by the bilinear transform. Equation (3.18) can be realised by introducing intermediate variables and decomposing the system into two inter-related first order sub-systems. Derivations for these structures are aimed at preserving matrix sparsity which translates directly to the reduced complexity of the resulting circuits.

Factorise the **A** and **B** matrices in equation (3.18) as

$$\mathbf{A} = \mathbf{U}_A \mathbf{L}_A \tag{3.19a}$$

$$\mathbf{B} = \mathbf{L}_B \mathbf{U}_B \tag{3.19b}$$

to give

$$\psi^{-1}\mathbf{U}_A\mathbf{L}_A\mathbf{I} + \phi\mathbf{L}_B\mathbf{U}_B\mathbf{I} + zD_l\mathbf{I} + D_n\mathbf{I} = (1+z)\mathbf{J} \tag{3.20}$$

Define

$$\mathbf{W}_B = \mathbf{U}_B\mathbf{I} \tag{3.21a}$$

$$\mathbf{D}_{ns} = D_n\mathbf{U}_B^{-1} \tag{3.21b}$$

Equation (3.20) becomes

$$\psi^{-1}\mathbf{U}_A\mathbf{L}_A\mathbf{I} + zD_l\mathbf{I} + (\phi\mathbf{L}_B + \mathbf{D}_{ns})\mathbf{W}_B = (1+z)\mathbf{J} \tag{3.22}$$

Let

$$\mathbf{W}_A = \psi^{-1}(\mathbf{L}_A\mathbf{I} + \mathbf{U}_A^{-1}\mathbf{J}) \tag{3.23a}$$

$$\mathbf{D}_{ls} = D_l\mathbf{L}_A^{-1} \tag{3.23b}$$

then, equation (3.22) can be arranged as

$$\mathbf{U}_A\mathbf{W}_A - \psi^{-1}\mathbf{J} + \phi\psi^{-1}\mathbf{D}_{ls}\mathbf{L}_A\mathbf{I} + (\phi\mathbf{L}_B + \mathbf{D}_{ns})\mathbf{W}_B = (1+z)\mathbf{J}$$

$$\mathbf{U}_A\mathbf{W}_A - \psi^{-1}\mathbf{J} + \phi\mathbf{D}_{ls}\mathbf{W}_A - \phi\psi^{-1}\mathbf{D}_{ls}\mathbf{U}_A^{-1}\mathbf{J} + (\phi\mathbf{L}_B + \mathbf{D}_{ns})\mathbf{W}_B = (1+z)\mathbf{J}$$

$$\mathbf{U}_A\mathbf{W}_A - \psi^{-1}\mathbf{J}(1 + \phi\mathbf{D}_{ls}\mathbf{U}_A^{-1}) + \phi\mathbf{D}_{ls}\mathbf{W}_A + (\phi\mathbf{L}_B + \mathbf{D}_{ns})\mathbf{W}_B = (1+z)\mathbf{J} \tag{3.24a}$$

and writing this in recursive form with respect to $\mathbf{W}_A$,

$$\mathbf{U}_A\mathbf{W}_A = -(\phi\mathbf{L}_B + \mathbf{D}_{ns})\mathbf{W}_B - \phi\mathbf{D}_{ls}\mathbf{W}_A + \psi^{-1}\mathbf{J}(1 + \phi\mathbf{D}_{ls}\mathbf{U}_A^{-1}) + (1+z)\mathbf{J} \tag{3.24b}$$

finally combine the input terms

$$\mathbf{U}_A\mathbf{W}_A = -(\phi\mathbf{L}_B + \mathbf{D}_{ns})\mathbf{W}_B - \phi\,\mathbf{D}_{1s}\mathbf{W}_A + (2 + \mathbf{D}_{1s}\mathbf{U}_A^{-1})\mathbf{J} \tag{3.25}$$

From (3.21a) and (3.23a),

$$\mathbf{L}_A^{-1}(\psi\mathbf{W}_A - \mathbf{U}_A^{-1}\mathbf{J}) = \mathbf{U}_B^{-1}\mathbf{W}_B \tag{3.26}$$

The upper triangular matrix $\mathbf{U}_{BS}$ and lower triangular matrix $\mathbf{L}_{AS}$ are defined [10] to satisfy the identity

$$\mathbf{U}_{AS}\mathbf{L}_A = \mathbf{L}_{BS}\mathbf{U}_B \tag{3.27a}$$

such that

$$\mathbf{U}_{AS}(\psi\mathbf{W}_A - \mathbf{U}_A^{-1}\mathbf{J}) = \mathbf{L}_{BS}\mathbf{W}_B \tag{3.27b}$$

rearranging,

$$\mathbf{L}_{BS}\mathbf{W}_B = \psi\mathbf{U}_{AS}\mathbf{W}_A - \mathbf{U}_{AS}\mathbf{U}_A^{-1}\mathbf{J} \tag{3.28}$$

Equations (3.25) and (3.28) describe the final system. From (3.21a), the output is now W_{Bn}, which differs from I_n by only a constant as $\mathbf{U}_B$ is an upper triangular matrix.

B. The LU-UL Decomposition Method

Multiplying both sides of equation (3.17) by $(1-z^{-1})$ and rearranging yields

$$\left[\frac{1}{\phi}\mathbf{A} + \psi\mathbf{B} + z^{-1}D_1 + D_n\right]\mathbf{I} = (1+z^{-1})\mathbf{J} \tag{3.29}$$

where

$$\psi = \frac{z^{-1}}{1-z^{-1}}, \qquad \phi = \frac{1}{1-z^{-1}}, \qquad \mathbf{A} = \frac{2}{T}\mathbf{C} + \frac{T}{2}\Gamma + G_1 - G_n, \qquad \mathbf{B} = 2T\Gamma,$$

$$D_1 = 2G_1, \qquad D_n = 2G_n$$

Factorise the **A** and **B** matrices in equation (3.29) as

$$\mathbf{A} = \mathbf{L}_A\mathbf{U}_A \tag{3.30a}$$

$$\mathbf{B} = \mathbf{U}_B\mathbf{L}_B \tag{3.30b}$$

to give

$$\phi^{-1}\mathbf{L}_A\mathbf{U}_A\mathbf{I} + \psi\mathbf{U}_B\mathbf{L}_B\mathbf{I} + z^{-1}D_1\mathbf{I} + D_n\mathbf{I} = (1+z^{-1})\mathbf{J} \tag{3.31}$$

Define

$$\mathbf{W}_A = \mathbf{U}_A\mathbf{I} \tag{3.32a}$$

$$\mathbf{D}_{ns} = \mathbf{D}_n\mathbf{U}_A^{-1} \tag{3.32b}$$

Equation (3.31) becomes

$$\mathbf{L_A W_A} = \phi[\, -\psi \mathbf{U_B L_B I} - z^{-1} D_1 \mathbf{I} - \mathbf{D_{ns} W_A} + (1+z^{-1})\mathbf{J}\,] \tag{3.33}$$

Define

$$\mathbf{W_B} = \psi \mathbf{L_B I} - 2\mathbf{U_B}^{-1}\mathbf{J} \tag{3.34a}$$

$$\mathbf{D_{1s}} = D_1 \mathbf{L_B}^{-1} \tag{3.34b}$$

and writing (3.33) in terms of $\mathbf{W_B}$ and some rearranging yields

$$\begin{aligned}\mathbf{L_A W_A} &= -\phi \mathbf{U_B W_B} - \phi\, z^{-1} \mathbf{D_{1s} L_B I} - \phi \mathbf{D_{ns} W_A} - \mathbf{J} \\ &= -\phi \mathbf{U_B W_B} - \psi \mathbf{D_{1s} L_B I} - \phi \mathbf{D_{ns} W_A} + 2D_1 \mathbf{L_B}^{-1} \mathbf{U_B}^{-1}\mathbf{J} - 2D_1 \mathbf{L_B}^{-1}\mathbf{U_B}^{-1}\mathbf{J} - \mathbf{J} \\ &= -\phi \mathbf{U_B W_B} - \mathbf{D_{1s} W_B} - \phi \mathbf{D_{ns} W_A} - 2\mathbf{D_{1s}} \mathbf{U_B}^{-1}\mathbf{J} - \mathbf{J}\end{aligned} \tag{3.35}$$

to give the required

$$\mathbf{L_A W_A} = -[(\, \phi \mathbf{U_B} + \mathbf{D_{1s}}\,)\, \mathbf{W_B} + \phi \mathbf{D_{ns} W_A}\,] - (1 + 2\mathbf{D_{1s}} \mathbf{U_B}^{-1})\,\mathbf{J} \tag{3.36}$$

From (3.32a) and (3.34a),

$$\mathbf{U_A}^{-1}\mathbf{W_A} = \psi^{-1}\, \mathbf{L_B}^{-1}\, (\mathbf{W_B} + 2\mathbf{U_B}^{-1}\,\mathbf{J}) \tag{3.37}$$

The upper triangular matrix $\mathbf{U_{BS}}$ and lower triangular matrix $\mathbf{L_{AS}}$ are defined[10] to satisfy the identity

$$\mathbf{L_{AS} U_A} = \mathbf{U_{BS} L_B} \tag{3.38}$$

such that

$$\mathbf{L_{AS} W_A} = \psi^{-1}\, \mathbf{U_{BS}}\, (\mathbf{W_B} + 2\mathbf{U_B}^{-1}\,\mathbf{J}) \tag{3.39}$$

rearranging (3.33),

$$\mathbf{U_{BS} W_B} = \psi \mathbf{L_{AS} W_A} - 2\mathbf{U_{BS}} \mathbf{U_B}^{-1}\,\mathbf{J} \tag{3.40}$$

Equations (3.36) and (3.40) describe the final system. From (3.32a), the output is now W_{An}, which differs from I_n by only a constant. For lowpass filters, Γ is always singular[10], after decomposing **B** according to (3.30b), L_{B11} becomes zero and this causes D_{1s11} in (3.34b) to become infinity. Thus, lowpass filters cannot be simulated by the LU-UL method. Note that in both the UL-LU and LU-UL methods, no $(1+z^{-1})$ or the bilinear $(1+z^{-1})/(1-z^{-1})$ terms are required at either the input or output to realise the bilinear zero at $z = -1$. This contrasts with the general Left and Right decomposition methods of Section 3.2. This simplified input arrangement can minimise circuit overheads, especially in low order filters.

3.4.2 Sensitivity Performance Comparison of SI UL-LU and LU-UL Filters

It is known that the performance of bandpass filters is greatly influenced by the relative

bandwidth(RBW), defined as

$$RBW = (\omega^+ - \omega^-)/\omega_m \tag{3.41}$$

where $\omega_m = (\omega^+\omega^-)^{1/2}$. ω^+ and ω^- are the upper and the lower band-edge frequencies respectively. Sensitivity analysis was performed for various 6th order, standard elliptic bandpass designs for a range of RBWs. The clock-to-upper passband edge ratio is 9.375, passband ripple 0.5dB, and stopband attenuation > 50dB. The average measure of the multiparameter statistical sensitivity over the passband is given by

$$S = \frac{1}{\text{bandwidth}} \int_{\text{passband}} s(\omega)d\omega \tag{3.42}$$

where $s(\omega)$ is defined in (3.15). The results are plotted in Fig. 3.11.

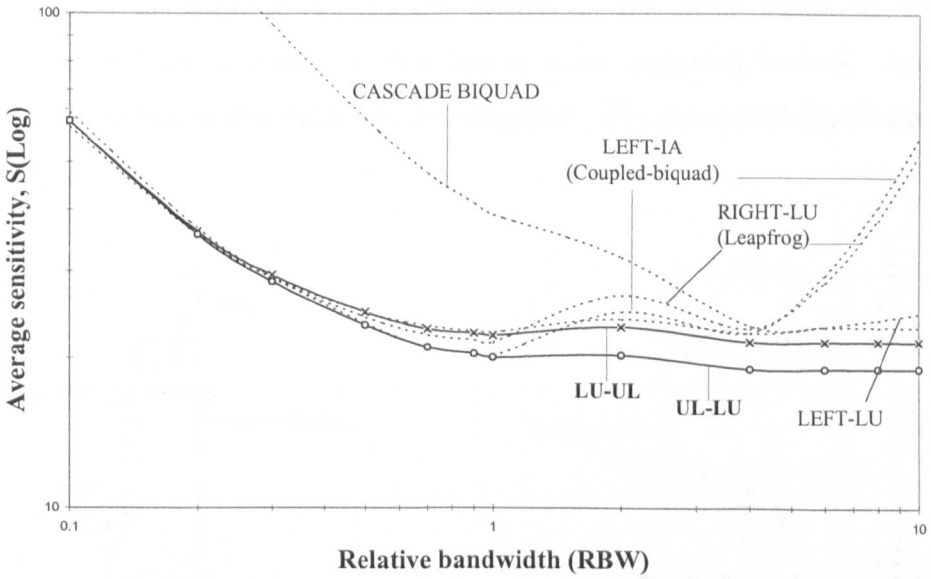


Figure 3.11 Average sensitivity vs RBW for 6th order SI bandpass

For RBW<<1, sensitivity and spreads increase for decreasing RBW, typifying the problems facing narrow and very narrow bandpass designs. In the mid and wide band range of RBW>1, both the UL-LU and LU-UL designs exhibit superior sensitivity performance over the other designs, most significantly for very large RBWs; whilst rapid increases are observed for the Right-LU(Leapfrog) and Left-IA(Coupled-biquad) designs. The cascade biquad design performs poorly for RBW<4 but maintains a reasonably low average sensitivity for large RBWs>4.

3.4.3 SI Design Examples and Implementation Using S^3I Memory Cells

The S^3I memory cell[21] operates on the same two-step principle as the S^2I[5] cell but with improved performance. The addition of a non-inverting amplifier and absence of a 'fine' sampling switch in the new configuration produces a virtual earth input voltage on both 'fine' and 'coarse' sampling phases and gives glitch-free operation. Precision was shown to be enhanced[21] by an order of magnitude and fewer clock waveforms are required. The simplified S^3I cell is shown in Fig. 3.12a. As the amplifier is disconnected on the output phase, it can be multiplexed with a second cell to form an integrator as shown in Fig. 3.12b. Forward Euler integration is obtained by switching the input in phase t1, while Backward Euler integration is achieved by simply changing the input phase to t2(shown in parenthesis). Feedthrough signals are fed directly to the summing node S. Transistors P3 and N3 form the scaled mirror output of the integrator. The associated clock waveforms are shown in Fig. 3.12c.

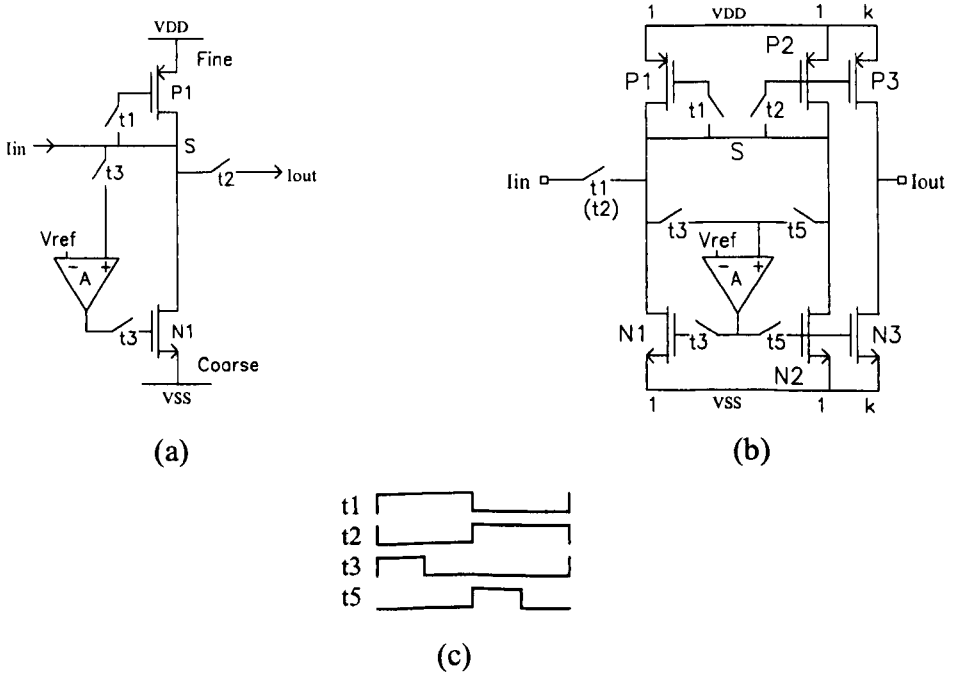


Figure 3.12 S^3I building blocks

(a) S^3I memory cell

(b) Basic S^3I Euler integrator

(c) Integrator clock waveforms

A. Design of a 5th order elliptic lowpass SI filter by UL-LU method

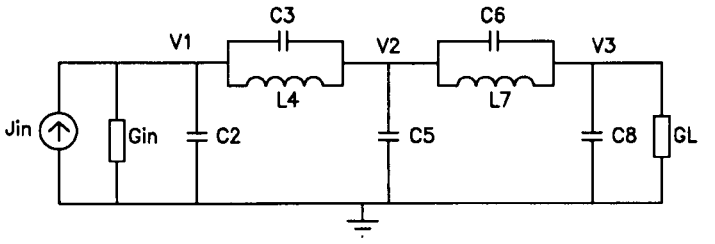


Figure 3.13 5th order elliptic lowpass passive prototype

The passive prototype used is shown in Fig. 3.13. The component matrices and variable vectors representing the nodal equations are written as

$$\mathbf{C} = \begin{bmatrix} C2+C3 & -C3 & \\ -C3 & C3+C5+C6 & -C6 \\ & -C6 & C6+C8 \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & \\ C_{21} & C_{22} & C_{23} \\ & C_{32} & C_{33} \end{bmatrix}$$

$$\Gamma = \begin{bmatrix} L4^{-1} & -L4^{-1} & \\ -L4^{-1} & L4^{-1}+L7^{-1} & -L7^{-1} \\ & -L7^{-1} & L7^{-1} \end{bmatrix} = \begin{bmatrix} \Gamma_{11} & \Gamma_{12} & \\ \Gamma_{21} & \Gamma_{22} & \Gamma_{23} \\ & \Gamma_{32} & \Gamma_{33} \end{bmatrix}$$

$$\mathbf{G} = \begin{bmatrix} G_{in} & & \\ & 0 & \\ & & G_L \end{bmatrix} = G_1 + G_n \qquad \mathbf{J} = \begin{bmatrix} J_{in} \\ 0 \\ 0 \end{bmatrix} \qquad \mathbf{V} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$

Using equations (3.19), (3.21), (3.23) and expanding (3.25) in terms of $\mathbf{W}_A$ gives

$$\begin{bmatrix} W_{A1} \\ W_{A2} \\ W_{A3} \end{bmatrix} = \begin{bmatrix} -U_{A11}^{-1}\{\phi\, L_{B11}W_{B1} + \phi D_{1S11}W_{A1} + U_{A12}W_{A2} + (2 + D_{1S11}U_{A11}^{-1})J_{in}\} \\ -U_{A22}^{-1}\{\phi\, L_{B21}W_{B1} + \phi\, L_{B22}W_{B2} + U_{A23}W_{A3}\} \\ -U_{A33}^{-1}\{\phi\, L_{B32}W_{B2} + \phi L_{B33}W_{B3} + D_{ns33}W_{B3}\} \end{bmatrix} \tag{3.43}$$

Similarly, expanding (3.28) in terms of $\mathbf{W}_B$ gives

$$\begin{bmatrix} W_{B1} \\ W_{B2} \\ W_{B3} \end{bmatrix} = \begin{bmatrix} L_{BS11}^{-1}\{\psi\,(U_{AS11}W_{A1} + U_{AS12}W_{A2}) - U_{AS11}U_{A11}^{-1}J_{in}\} \\ L_{BS22}^{-1}\{\psi\,(U_{AS22}W_{A2} + U_{AS23}W_{A3}) - L_{BS21}W_{B1}\} \\ L_{BS33}^{-1}\{\psi(\,U_{AS33}W_{A3}) - L_{BS32}W_{B2}\} \end{bmatrix} \tag{3.44}$$

The signal flow graph representing equations (3.43) and (3.44) is shown in Fig. 3.14. The ψ and ϕ branches are realised by Forward and Backward Euler integrators respectively.

Solid line branches connect to the integrator inputs Iin. The branches shown in dashed lines, representing feed-through signals, connect directly to the common summing node, S, of the integrators. Table 3.7 lists the design data for the lowpass filter and the circuit is given in Fig. 3.15.

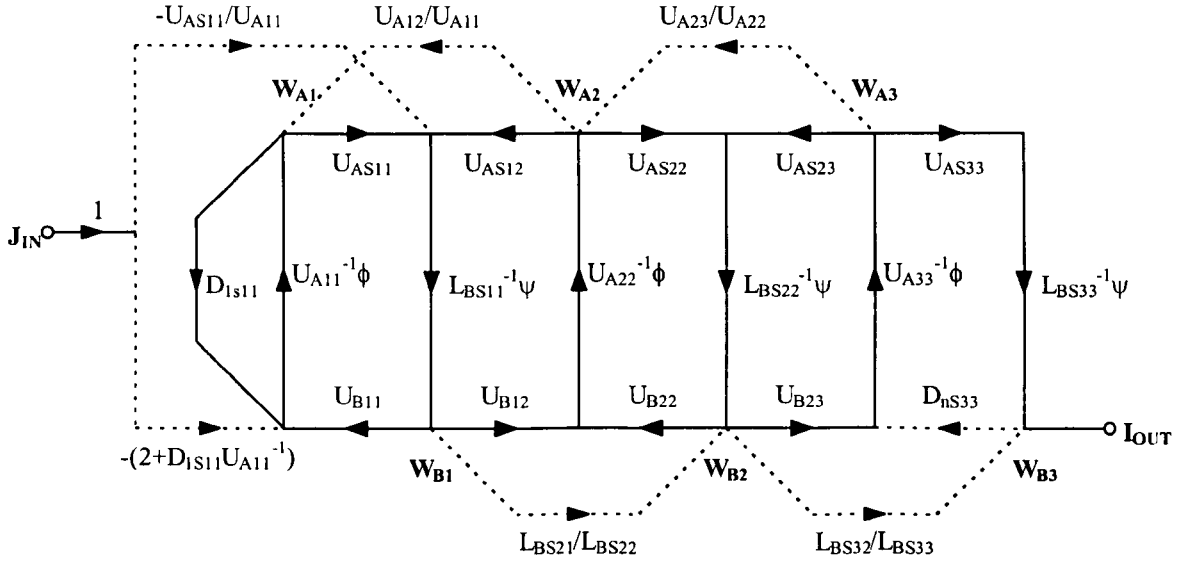


Figure 3.14 UL-LU signal flow graph for the 5th order SI lowpass filter

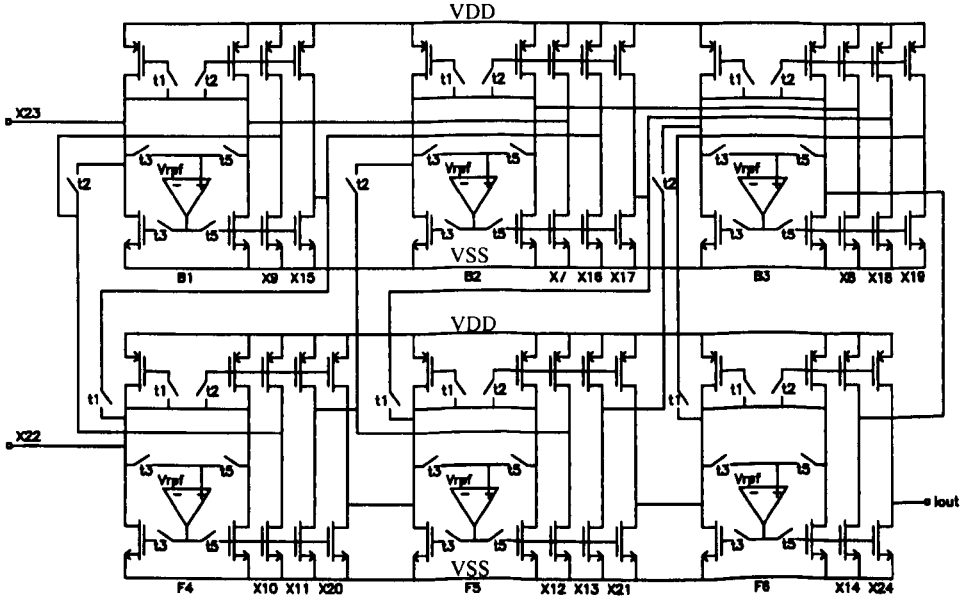


Figure 3.15 5th order UL-LU SI lowpass filter

Table 3.7 Design data for the 5th order lowpass filter

		Filter specification:			
Upper passband edge	1MHz	Stopband edge	1.667MHz	Stopband attenuation	
Passband ripple	0.603dB	Clock frequency	10MHz	>45.8dB	
		Normalised values for the passive prototype:			
Rin	1.000000e+00	L4	3.427935e+00	L7	2.985822e+00
C2	5.266390e+00	C5	7.200512e+00	C8	4.770045e+00
C3	3.407391e-01	C6	9.242849e-01	RL	1.000000e+00
		Transistor ratios for the SI UL-LU filter:			
x7	2.129816e-01	x15	2.097971e-01	x23	1.072429e+00
x8	9.524698e-02	x16	3.692527e-01	x24	1.000000e+00
x9	4.120537e-01	x17	3.993545e-01	R26	1.00000e+00
x10	1.064174e+00	x18	3.030140e-01	R27	1.00000e+00
x11	3.564073e-01	x19	8.764949e-01		
x12	3.344179e-01	x20	7.714552e-02		
x13	6.289623e-01	x21	5.181709e-01	gm spread	13.90
x14	3.954589e-01	x22	9.327838e-02	Total gm	1434.8 units

Simulations were performed using SCNAP4[22] with the various circuit parameters set as: gain of the operational amplifier(A)=100, bias voltage(Vref)=half rail-to-rail voltage, output conductance of transconductors(g_o)=$1e^{-5}$S, switch on-resistance(Ron)=100Ω, switch off-resistance(Roff)=$1e^{+12}$ Ω. The gain response with the filter clocked at 10MHz is shown in Fig. 3.16.

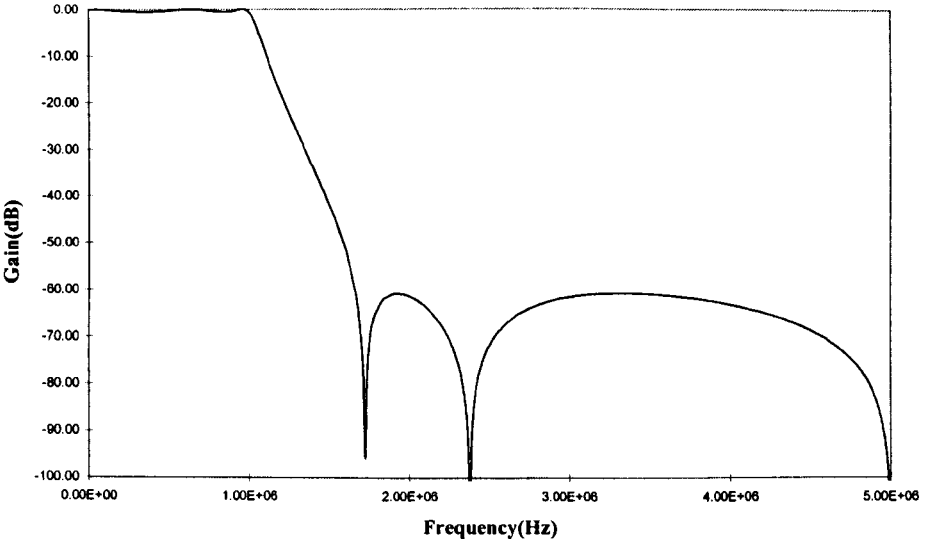


Figure 3.16 Simulated gain response of SI UL-LU lowpass filter

A simulation of passband sensitivities for various other lowpass filters is compared to the UL-LU design in Fig. 3.17. Both the Left-LU and Left-IA(Coupled-biquad) designs suffer from peaks in sensitivity towards low frequencies and at DC. The Right-LU(Leapfrog) design maintains low sensitivity throughout the passband but at a level higher than the UL-LU design. The cascade biquad design shows good low frequency sensitivity but increases significantly towards the passband edge. The UL-LU design clearly exhibits superior sensitivity performance.

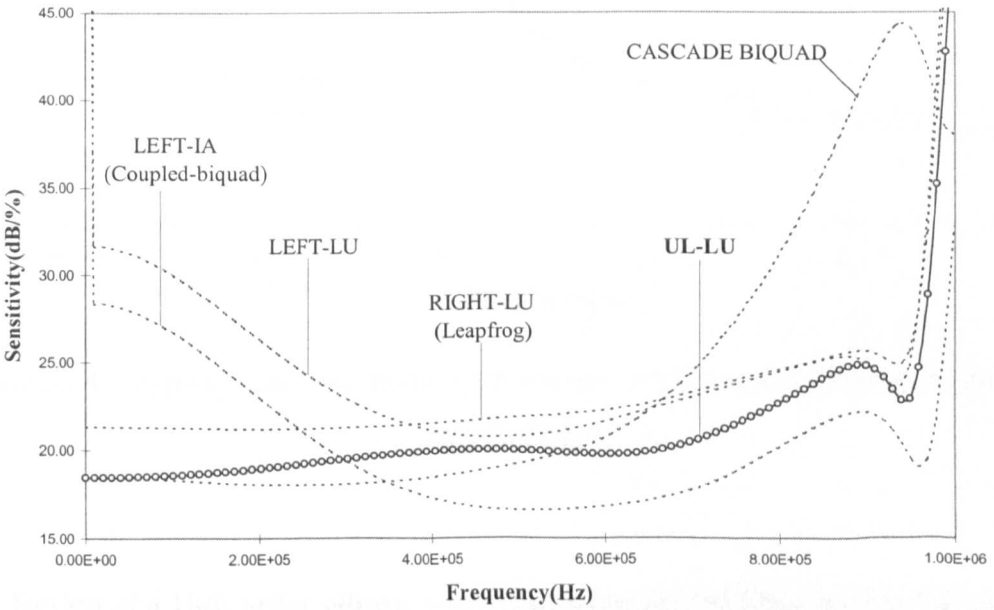


Figure 3.17 Passband sensitivity comparison for the SI UL-LU lowpass filter

The simulated noise performances given in Fig. 3.18 show the UL-LU, and Left-Decomposition designs suffering from higher noise in the passband and at low frequencies. Table 3.8 gives a comparison of the implementation costs and supports the conclusion that the UL-LU design offers the best solution to this lowpass problem.

Table 3.8 Circuit statistics for different designs of 5th order lowpass filter

Decomposition	Transistor spread	Total gm (units)
LEFT-LU	17.141593	1814.180879
LEFT-IA(Coupled-biquad)	17.577682	1828.339844
RIGHT-LU(Leapfrog)	18.245942	2702.541095
UL-LU	13.901371	1434.772683
CASCADE BIQUAD	9.573100	1190.366058

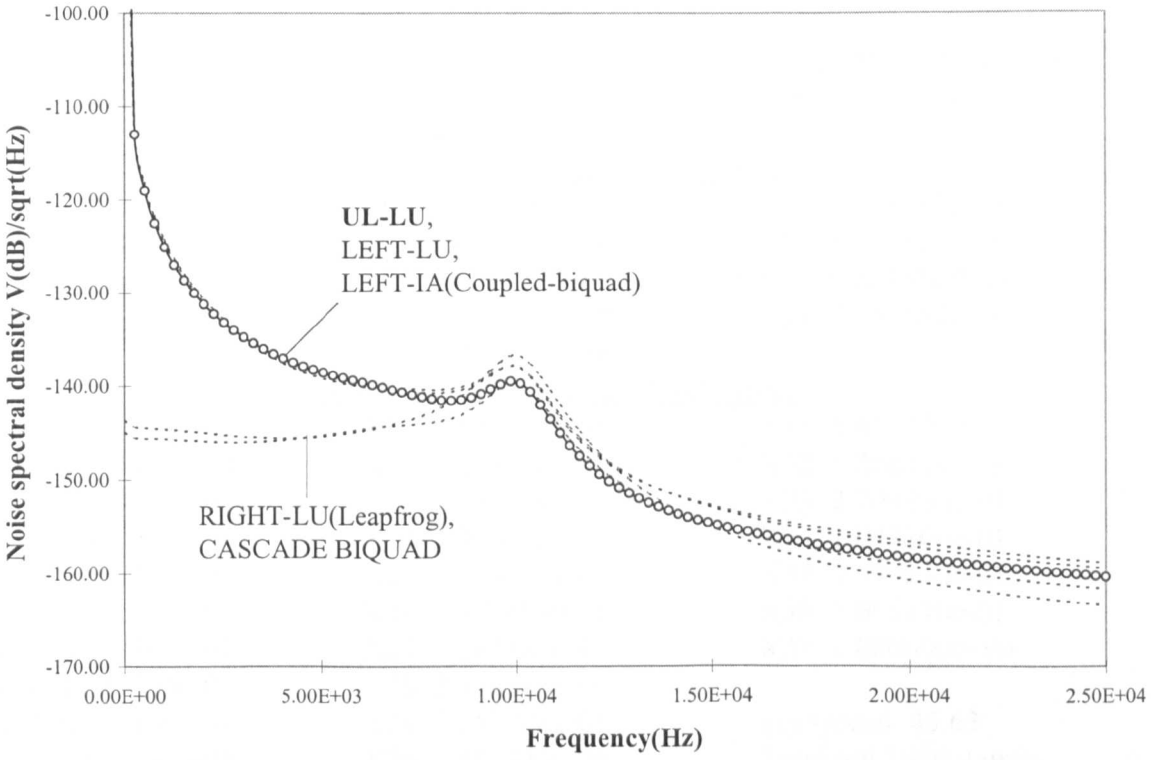


Figure 3.18 Typical simulated noise performance of SI lowpass filters with 10-band foldback effects

B. Design of a 10th order elliptic wideband bandpass SI filter by LU-UL method

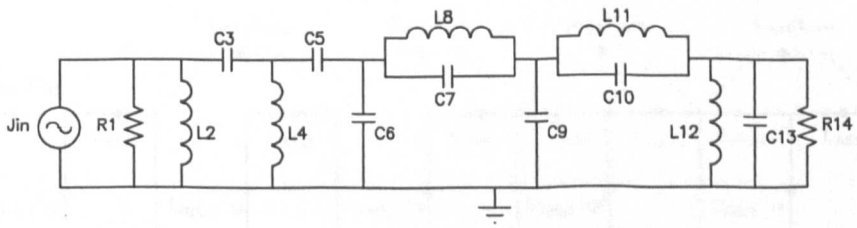


Figure 3.19 10th order elliptic bandpass passive prototype

The synthesised passive prototype shown in Fig. 3.19 is a quasi-elliptic filter, with all the lower stopband zeros shifted to the origin to reduce the spread. The relative bandwidth of the filter is 3.62. The design specifications are listed in Table 3.9.

Table 3.9 Design data for 10th order bandpass filter

		Filter specification:			
Lower PB edge	80kHz	Upper PB edge	1.2MHz	Lower SB edge	46.8kHz
Lower attenuation	40.5dB	Upper SB edge	1.34MHz	Upper attenuation	37dB
Passband ripple	1.7dB	Fclock	10MHz		
		Normalised values for the passive prototype:			
R1	1.000000E+00	C6	5.591399E+00	L11	1.178033E+00
L2	1.535371E+01	C7	5.966341E+00	L12	9.325125E+00
C3	4.374470E+01	L8	8.009731E-01	C13	9.031556E+00
L4	1.005315E+01	C9	7.961073E+00	R14	7.351160E-01
C5	4.944113E+01	C10	2.303288E+00		
		Transistor ratios for the SI LU-UL filter:			
X11	6.127729e-01	X21	3.856926e-01	X31	5.417323e-01
X12	2.284462e+00	X22	1.204070e+00	X32	1.256114e+00
X13	6.190005e-01	X23	8.914749e-01	X33	2.709830e-01
X14	5.988833e-01	X24	5.006653e-02	X34	1.043100e-01
X15	2.654423e-01	X25	1.273381e-01	X35	8.099850e-01
X16	1.161250e-01	X26	2.971864e-01	X36	7.691110e-01
X17	6.177562e-02	X27	5.281544e-01	X37	1.000000e+00
X18	1.649996e-01	X28	2.913257e-01		
X19	6.311456e-01	X29	5.357777e-01	gm spread	45.63
X20	8.112347e-01	X30	2.504443e-01	Total gm	1080.9 units

After deriving the component matrices and applying equations (3.30), (3.32), (3.39), the resulting signal flow graph corresponding to (3.36) and (3.40) is shown in Fig. 3.20. The SI realisation of the LU-UL bandpass filter is shown in Fig. 3.21 and its simulated gain response in Fig. 3.22.

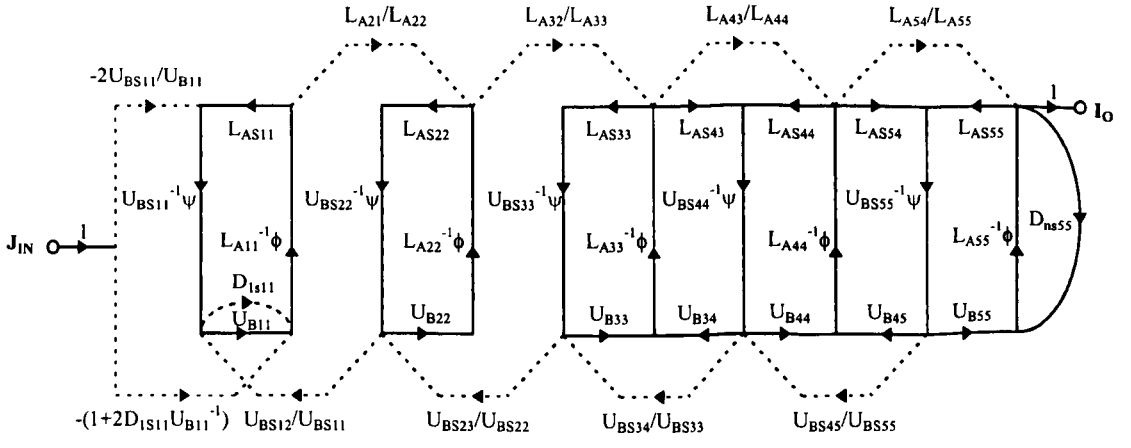


Fig. 3.20 SI LU-UL signal flow graph for the 10th order bandpass filter

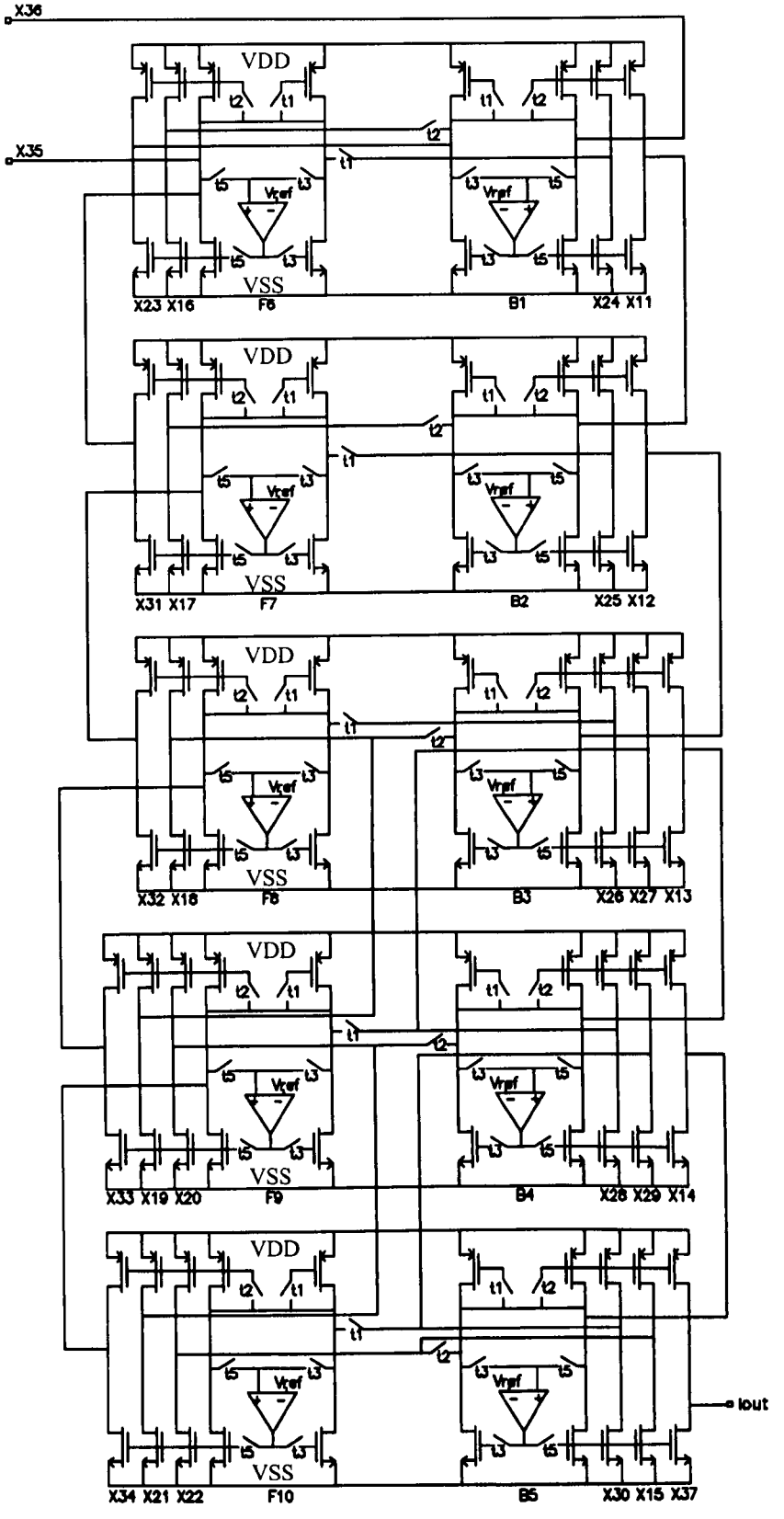


Figure 3.21 10th order LU-UL SI bandpass filter

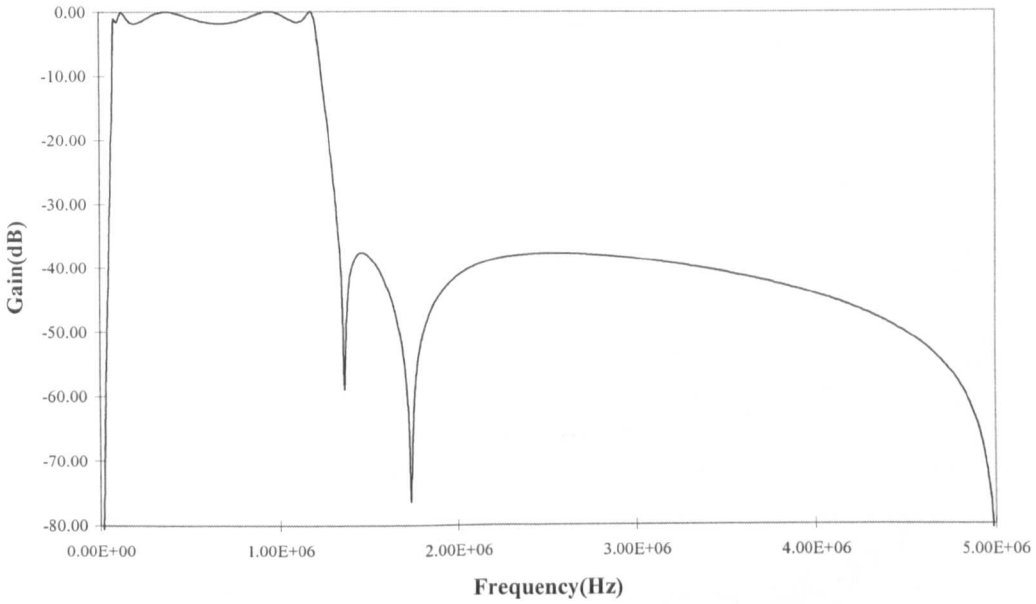


Figure 3.22 Simulated gain response of SI LU-UL bandpass filter

The passband sensitivity comparison of the LU-UL versus other designs is plotted in Fig. 3.23. The cascade biquad design has a large overall sensitivity which increases dramatically towards the upper passband edge. Similar peaks are observed in the vicinity of the upper passband edge for the Right-LU(Leapfrog) and Left-IA(Coupled biquad) designs. Near the lower passband edge, both the Left-IA(Coupled biquad) and Left-LU designs exhibit sensitivity peaks. It is apparent that both the UL-LU and LU-UL designs maintain low sensitivity throughout the passband.

The comparison of simulated noise behaviour in Fig. 3.24 demonstrates superior noise performance of the LU-UL and UL-LU designs, which translates to improved signal-to-noise ratios. Table 3.10 gives a comparison of the implementation costs for different designs. Both the UL-LU and LU-UL designs show reasonable and comparable transistor spreads and total gm values. Note that in all the designs, the prototype component values have been scaled by a factor of $\omega_s = \pi(f_p/F_s)$ to compensate for the frequency warping effect of the bilinear transform, where $f_p = F_s/\pi \tan(\pi f_o/F_s)$, f_o is the filter cutoff frequency and F_s is the clock frequency. Scaling for maximum dynamic range and minimum spread[9] has been performed to obtain the transistor ratios of the SI filters. The design routines for these SI UL-LU and LU-UL structures have been incorporated into the filter

and equaliser compiler XFILT[17], where the synthesis process, including pre-warping and scaling are automatically carried out.

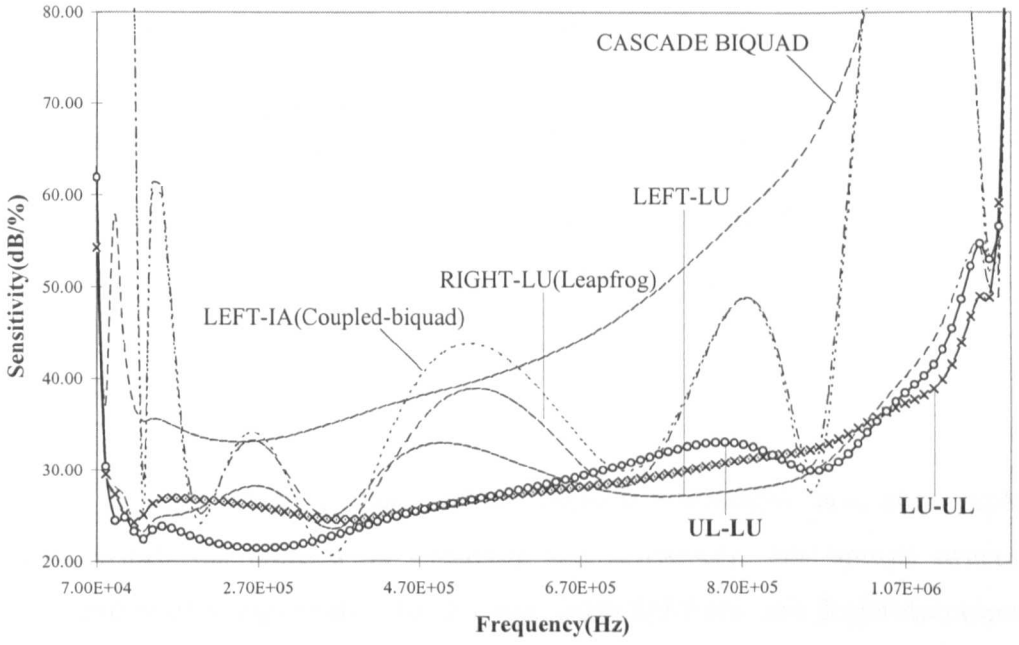


Figure 3.23 Passband sensitivity comparison for the SI bandpass filters

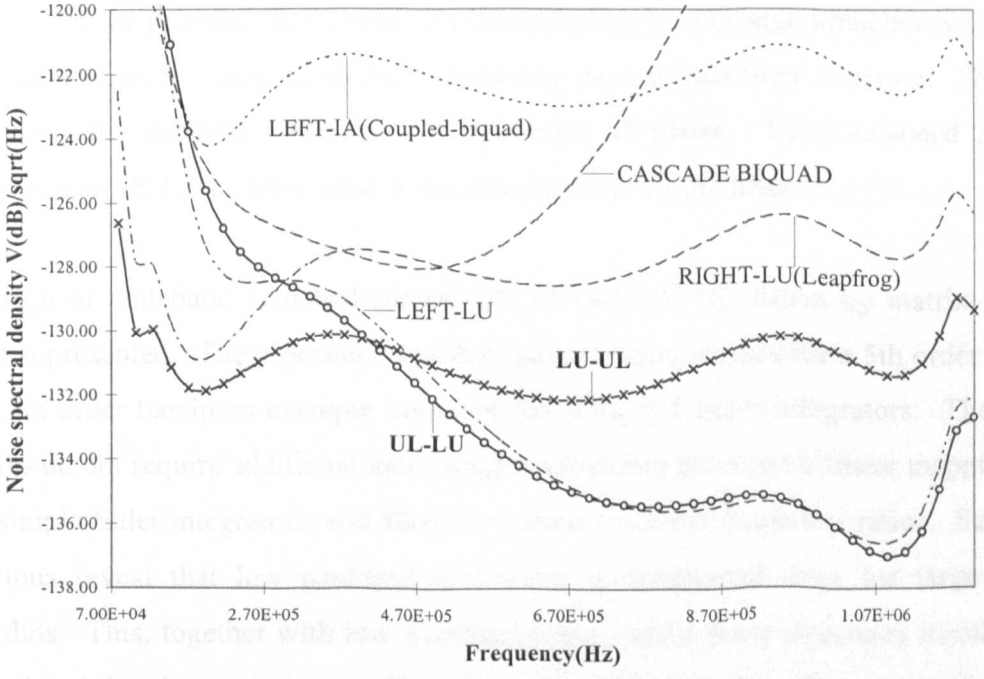


Figure 3.24 Typical simulated noise performance of SI bandpass filters with 10-band foldback effects

Table 3.10 Circuit statistics for different designs of 10th order SI bandpass filter

Decompositions	Transistor spread	Total gm (units)
LEFT-LU	28.27	1007.00
LEFT-IA(Coupled-biquad)	68.10	2230.10
RIGHT-LU(Leapfrog)	33.83	1501.82
CASCADE BIQUAD	1125.32	5306.93
UL-LU	57.04	1776.50
LU-UL	45.63	1080.91

3.5 CONCLUSIONS

The design of high order SI filters and its associated problems have been explored. In particular, effort was focused on obtaining low sensitivity, low spread structures with reduced number of components. To this end, modified Left- and Right-decomposition SI structures have been introduced with improved sensitivity and simple input stages. Using prototype ladder and matrix manipulation, quite remarkable reductions in spreads and total gm were achieved for a 21st order elliptic lowpass filter, while preserving low passband sensitivity. In the process, the number of cross-coupling feedthrough branches for realising transmission zeros are reduced, further simplifying the resultant filter structure. This paves the way for the feasible realisation of high-order SI filters. Fully-balanced SI Euler integrators using S^2I cells were used in the simulation of all the filters.

The design of wideband switched-current UL-LU and LU-UL filters by matrix methods have been presented. The procedure was derived and demonstrated for a 5th order lowpass and a 10th order bandpass example implemented using S^3I Euler integrators. These filter structures do not require additional input stages to preserve the exact bilinear mapping; they utilise simple Euler integrators, and allow low clock-to-cutoff frequency ratios. Sensitivity simulations reveal that low passband sensitivity is maintained even for large relative bandwidths. This, together with low passband noise, make these structures ideally suited for wideband bandpass designs. The UL-LU design has also demonstrated superior sensitivity and implementation efficiency in the lowpass design.

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CHAPTER 4:
DESIGN OF SWITCHED-CURRENT BILINEAR GROUP-DELAY EQUALISERS

4.1 INTRODUCTION

Allpass filters are primarily used for group-delay equalisation for applications which require linear or near-linear phase characteristics. However, as the allpass transfer function is non-minimum phase by definition, low sensitivity ladder simulation remains a problem. As such, most allpass functions have hitherto been implemented either as lattice structures[1] or as cascades of biquadratic sections[2]. A novel method for digital allpass filter design was previously proposed[3-5] which allowed the allpass function to be realised as the sum of a constant term and a ladder-realisable, reactive driving point impedance. The main advantage of this method is low sensitivity to component variation, achieved with low sensitivity ladder structures and the inherent structurally lossless property. This method was subsequently extended to include switched-capacitor[4,6] and switched-current[7] forms. These were however implemented either by Lossless-Discrete-Integrator(LDI) transformed structures, or Bilinear transformed structures with Euler integrators in the so-called Bilinear-LDI method. With the Bilinear-LDI method, use of the bilinear transform ensures 'exact' responses and low Fs/fo ratios. However, Euler integrators suffer from excess phase which should ideally be cancelled when employed in a two-integrator loop configuration. Therefore, it is highly desirable to derive structures that allow the use of bilinear integrators which do not suffer from excess phase and directly implements the bilinear-transform.

In this chapter, two approaches are presented for deriving SI allpass structures in terms of the bilinear integrator. The first proceeds via the s-domain while the second is a direct z-domain approach. The respective continued-fractions expansions are used to synthesise a prototype which can then be simulated using standard matrix methods[7]. The structurally lossless property of the singly-terminated reactive ladder section implies zero sensitivity contribution to the amplitude response of the equaliser. This is important as it minimises distortion to the amplitude response of the filter being equalised. Significant improvements in overall amplitude and group-delay sensitivities are made over existing Euler integrator based ladder realisations. Simulations of various non-ideal effects also reveal the merits of different designs.

4.2 DESIGN METHODS FOR BILINEAR INTEGRATOR BASED ALLPASS SWITCHED-CURRENT LADDER FILTERS

4.2.1 s-Domain Approach

An allpass transfer-function in the s-domain has poles and zeros in mirror image symmetry and is written as

$$H(s) = \pm\frac{P(-s)}{P(s)} \tag{4.1}$$

It can be shown[3] that (4.1) can be written with

$$Y(s) = \begin{cases} \dfrac{Ev P(s)}{Od P(s)} & \text{for } n \text{ even} \\ \dfrac{Od P(s)}{Ev P(s)} & \text{for } n \text{ odd} \end{cases} \tag{4.2}$$

for the Hurwitz polynomial

$$P(s) = Ev P(s) + Od P(s) \tag{4.3}$$

as

$$H(s) = \frac{1 - Y(s)}{1 + Y(s)} = 1 - \frac{2}{1 + Y(s)} \tag{4.4}$$

Y(s) represents the reactive driving point admittance, from which the passive prototype can be synthesised using continued-fractions expansion(CFE)[12]

$$Y(s) = C_1 s + \cfrac{1}{L_1 s + \cfrac{1}{C_2 s + \cfrac{1}{\ddots \; C_m s + \cfrac{1}{L_m s}}}} \tag{4.5}$$

Thus, in general, Y(s) can be expressed in matrix form using nodal formulations[6] as

$$\mathbf{Y}(s) = s\mathbf{C} + s^{-1}\Gamma + \mathbf{G} \tag{4.6}$$

where **C**, Γ and **G** are matrices formed by the contribution of capacitors, inductors and resistors respectively. Performing the bilinear transformation

$$s \rightarrow \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} \tag{4.7}$$

$$\text{with } \lambda^{-1} = \frac{z-1}{z+1} \tag{4.7a}$$

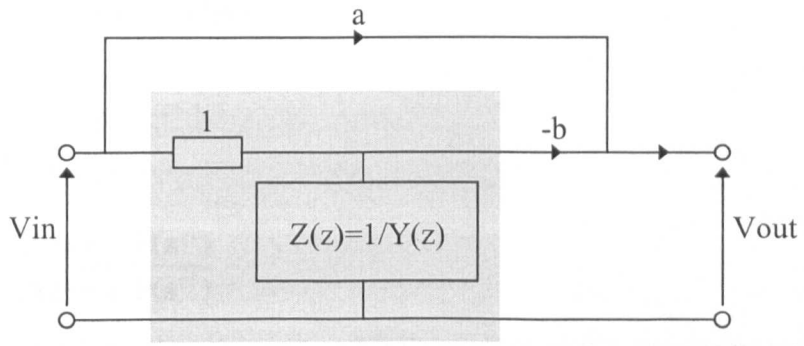
results in

$$\mathbf{Y}(z) = \mathbf{J}_1/\mathbf{V}_1 = \lambda^{-1}\mathbf{C} + \lambda\Gamma + \mathbf{G} \tag{4.8}$$

Hence, (4.4) can be written as

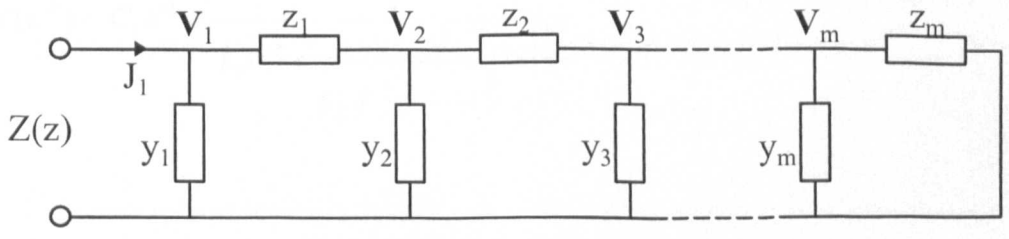
$$H(z) = 1 - \frac{2}{1+Y(z)} \tag{4.9}$$

which can be realised as shown in Fig. 4.1. The general structure of the synthesised Z(z) = 1/Y(z) driving point function is shown in Fig. 4.2.



a = 1.0, b = 2.0

Figure 4.1 Top level realisation of the allpass function



For s-domain: $y_i = sC_i$, $z_i = sL_i$

For z-domain: $y_i = \lambda^{-1}C_i$, $z_i = \lambda^{-1}L_i$

Figure 4.2 Typical structure of a synthesised driving point immittance function

4.2.2 z-Domain Approach

The transfer function for an n-th order allpass structure in the z-domain takes the general form of

$$H(z) = k\frac{z^n P(z^{-1})}{P(z)} \tag{4.10}$$

with k = -1 for n even, k = +1 for n odd.

This can be rearranged and expressed as

$$H(z) = 1 - \frac{P(z) - z^n P(z^{-1})}{P(z)} \tag{4.11}$$

$$= 1 - \frac{2}{1 + \dfrac{P(z) + z^n P(z^{-1})}{P(z) - z^n P(z^{-1})}} \tag{4.12}$$

Thus,

$$H(z) = 1 - \frac{2}{1 + Y(z)} \tag{4.13}$$

$$\text{where } Y(z) = \frac{P(z) + z^n P(z^{-1})}{P(z) - z^n P(z^{-1})} \tag{4.14}$$

Utilising a continued fractions expansion(CFE) method in [9], the reciprocal of (4.14), i.e. $Y(z^{-1})$ can be expanded in terms of the bilinear operator

$$\lambda^{-1} = \frac{z-1}{z+1} \tag{4.15}$$

as

$$Y(z^{-1}) = C_1\lambda^{-1} + \cfrac{1}{L_1\lambda^{-1} + \cfrac{1}{C_2\lambda^{-1} + \cfrac{1}{\ddots + \cfrac{1}{L_{n-1}\lambda^{-1}}}}} \tag{4.16}$$

Thus, Y(z) can be represented by the ladder part of Fig. 4.2 and expressed in matrix form using nodal formulations as

$$\mathbf{Y}(z) = \mathbf{J}_1/\mathbf{V}_1 = \lambda^{-1}\mathbf{C} + \lambda\Gamma + \mathbf{G} \tag{4.17}$$

which is identical to the expression in (4.8) for the s-domain approach.

4.3 SI SIMULATION USING BILINEAR INTEGRATORS

After determining the allpass structure and obtaining the z-domain description of the singly-terminated reactive section in terms of the bilinear integrator, simulation of the structure can proceed using conventional matrix methods[7] as follows:

From (4.8) or (4.17),

$$(\lambda^{-1}\mathbf{C}+\lambda\Gamma+\mathbf{G})\mathbf{V}=\mathbf{J} \tag{4.18}$$

Using a 1Ω scaling resistance, the voltage variable is changed to a current variable as

$$(\lambda^{-1}\mathbf{C}+\lambda\Gamma+\mathbf{G})\mathbf{I}=\mathbf{J} \tag{4.19}$$

$$\text{Let } \Gamma = \Gamma_L\Gamma_R \tag{4.20}$$

$$\text{Defining } \mathbf{W} = \lambda\Gamma_R\mathbf{I}\,, \tag{4.21}$$

and substituting (4.20) and (4.21) into (4.19) yields

$$\mathbf{CI}= -\lambda(\Gamma_L\mathbf{W}+\mathbf{GI}) + \lambda\mathbf{J} \tag{4.22}$$

The system of equations (4.21) and (4.22) together describe the operational simulation of the reactive section of the allpass structure. $\Gamma_L\Gamma_R$ can be obtained by either the LU-factorisation ($\Gamma = \Gamma_L\Gamma_U$, $\Gamma = \Gamma_U\Gamma_L$) or direct methods($\Gamma = \mathbf{I}_D\Gamma$, $\Gamma = \Gamma\mathbf{I}_D$)[7], where $\mathbf{I}_D$ is the identity matrix. The remaining functions of summation and scaling by a factor of 2.0 in Fig. 4.1 can be easily implemented in the SI realisation as will be shown in the example of a 6th order group-delay equaliser for a 3rd order lowpass filter.

4.3.1 Design Example of a Switched-Current Filtering System: Cascade of a 3rd Order Lowpass and a 6th Order Allpass Delay Equaliser

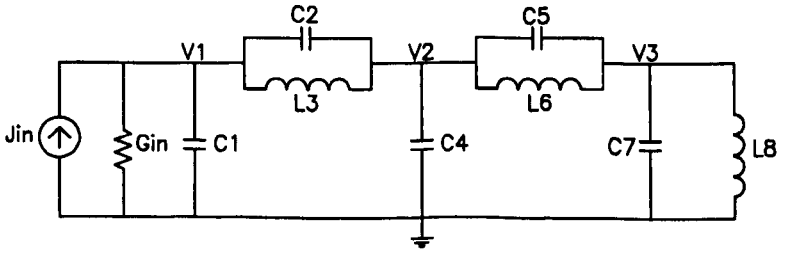


Figure 4.3 6th order singly-terminated allpass ladder prototype

Table 4.1 Design data for the 6th order allpass filter

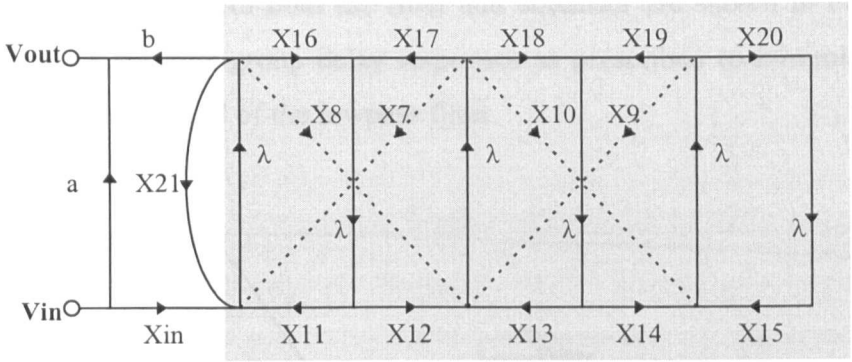
Specification of the delay equaliser			
Equalisation edge frequency	1MHz	In-band ripple	<0.06uSec.
Approximation type	Equiripple	Filter order	6
Sampling frequency	5MHz		

Poles and zeros of the allpass transfer function in the z-domain	
z-domain zeros	z-domain poles
1.372567±j0.1804098	0.7161887±j0.0941356
1.266440±j0.5030130	0.6820213±j0.2708898
1.117817±j0.7937362	0.5947315±j0.4223052

Normalised prototype component values					
Gin	1.00000	C2	-0.251444	C4	5.109904
C1	1.826231	L3	3.977036	C5	-0.167138
L6	5.983064	C7	7.439028	L8	10.54152

Transistor ratios for the SI allpass filter					
Xin	0.6350079	X12	0.2116817	X18	0.1683081
X7	0.1607860	X13	0.2116782	X19	0.1799743
X8	0.0532250	X14	0.1277082	X20	0.1021482
X9	0.0380966	X15	0.1277082	X21	0.6350065
X10	0.0214943	X16	0.2514389	Spread:	93.1
X11	0.6501820	X17	0.2531990		

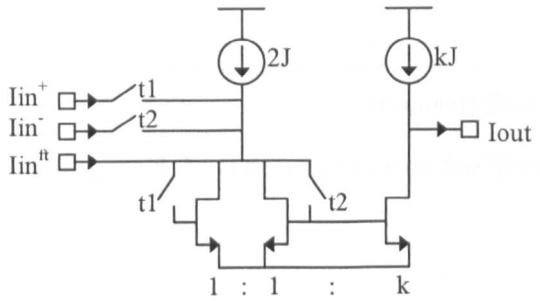
Consider the singly-terminated allpass ladder prototype shown in Fig. 4.3. By forming the respective component matrices according to (4.8) and applying (4.21), (4.22) with (4.20) as ($\Gamma = \Gamma_L\Gamma_U$) results in the SFG for the allpass filter as shown in Fig. 4.4, where the dashed-lines represent feedthrough(ft) branches. The design specifications for the allpass filter and corresponding coefficient values after scaling for maximum dynamic range and minimum spread are listed in Table 4.1. The conventional single sampling(SS) bilinear integrator[13] is shown in Fig. 4.5 while Fig. 4.6 shows the double sampling(DS) version proposed by Hughes and Moulding[8]. Double sampling allows the clock frequency to be halved compared to single sampling.



Reactive ladder section

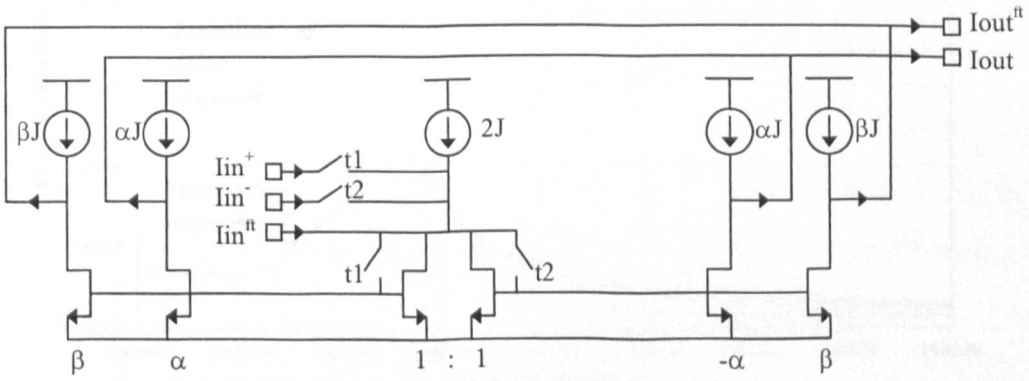
$$a = 1.0,\ b = 2.0,\ \lambda = \frac{1 + z^{-1}}{1 - z^{-1}}$$

Figure 4.4 SFG for the 6th order allpass ladder filter



$$H(z) = k\frac{1 + z^{-1}}{1 - z^{-1}}$$

Figure 4.5 Single-sampling(SS) bilinear integrator



$$H(z) = -\alpha\frac{1 + z^{-1}}{1 - z^{-1}} \qquad H_{ft}(z) = -\beta$$

Figure 4.6 Double-sampling(DS) bilinear integrator[8]

The simulated gain responses of both the filter and equaliser are shown in Fig. 4.7 while Fig. 4.8 shows the respective group delay responses as prescribed to minimise the group delay variation in the passband of the lowpass filter.

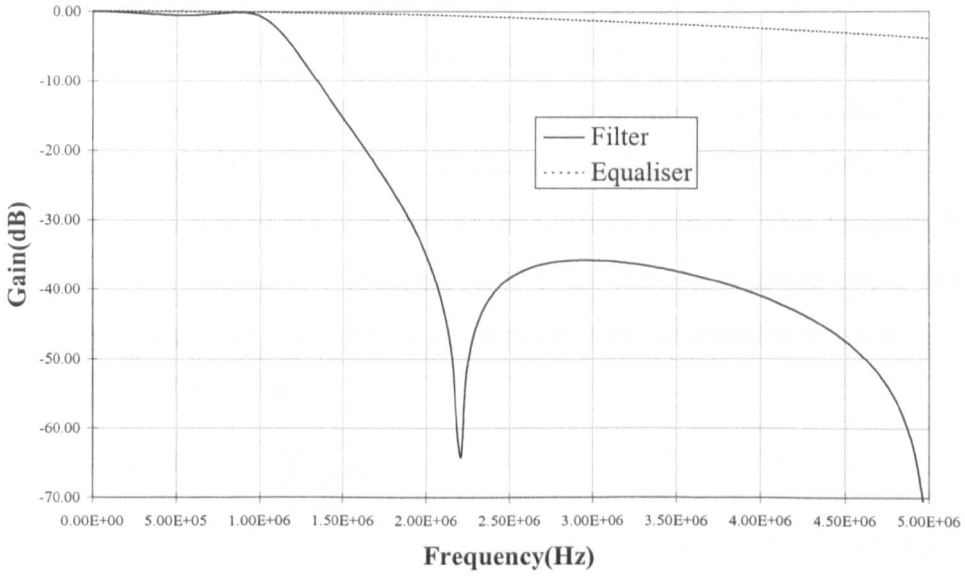


Figure 4.7 Gain response of the filter and allpass filter

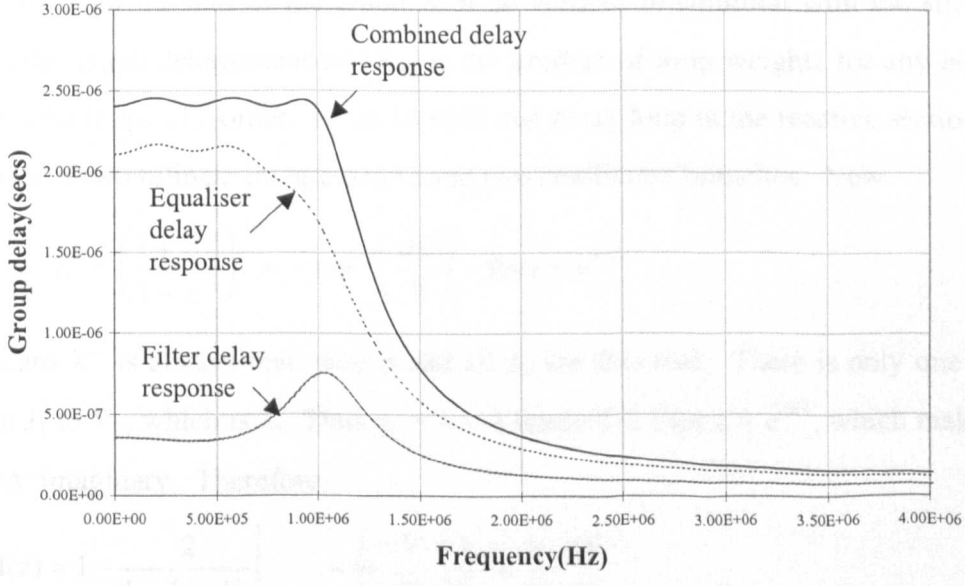


Figure 4.8 Group delay response of the switched-current filter system

4.3.2 Sensitivity and Non-ideal Factors

A. Sensitivity

As the coefficients in SI filters are implemented by W/L ratios of different transistors, the sensitivity of the filter response to their deviation has to be investigated. Developing an existing line of argument[6], it will be shown that due to the structurally-lossless property, the amplitude response of the bilinear integrator based allpass filter is also completely insensitive to any deviation in the elements of the reactive section. This property holds true as long as $Y=V_1/J_1$ is imaginary. Assuming X21=1, the transfer function of the SFG of Fig. 4.4 will have the same form as (4.13). The admittance of the reactive section can be found using Mason's gain rule[11] as

$$Y = \frac{V_1}{J_1} = \frac{1}{\Delta} \sum_{\substack{\text{all forward} \\ \text{paths}}} g_k \Delta_k \tag{4.23}$$

with

$$\Delta = 1 - \sum_m P_{m1} + \sum_m P_{m2} - \sum_m P_{m3} + \cdots \tag{4.24}$$

where g_k is the product of edge weights for the *k*th forward path, Δ_k is the cofactor of g_k, or the value of Δ for the part of the graph with no vertices in common with the *k*th forward path. Δ is the graph determinant and P_{mr} is the product of loop weights for any *m*th set of vertex-disjoint loops of *r*-order. It can be seen that every loop in the reactive section of Fig. 4.4 consists of two bilinear integrators(λ) and two coefficient branches. Now

$$\lambda^2 = \left(\frac{1+z^{-1}}{1-z^{-1}}\right)^2 = -\tan^{-2}\left(\frac{\omega T}{2}\right) \quad \text{for } z = e^{j\omega T} \tag{4.25}$$

which means λ^2 is always real, then Δ and all Δ_k are also real. There is only one forward path from J_1 to V_1, which is λ. Thus $g_1 = \lambda = 1/\text{jtan}(\omega T/2)$ for $z = e^{j\omega T}$, which makes $V_1/J_1 = (g_1\Delta_1)/\Delta$ imaginary. Therefore,

$$H(z) = 1 - \left.\frac{2}{1+J_1/V_1}\right|_{X21=1} = \frac{1-V_1/J_1}{1+V_1/J_1} = \frac{1-jX}{1+jX} \tag{4.26}$$

and the magnitude of H(z) will always be

$$|H(z)| = \left|\frac{1-jX}{1+jX}\right| = 1 \tag{4.27}$$

regardless of any deviation in element values within the reactive ladder section. The dominant contributors to the amplitude response sensitivities are therefore the branch 'a' from input to the output, ladder output branch 'b', and the termination X21. Their respective, normalised magnitude sensitivities are given by

$$\left.\frac{a}{|H|}\frac{\partial|H|}{\partial a}=\frac{1-|Y|^2}{1+|Y|^2}\right|_{\substack{b=2.0\\X21=1.0}} \le 1 \tag{4.28}$$

$$\left.\frac{b}{|H|}\frac{\partial|H|}{\partial b}=\frac{2}{1+|Y|^2}\right|_{a=X21=1.0} \le 2 \tag{4.29}$$

$$\left.\frac{X21}{|H|}\frac{\partial|H|}{\partial X21}=\frac{2}{1+|Y|^2}\right|_{\substack{a=1.0\\b=2.0}} \le 2 \tag{4.30}$$

To facilitate performance assessment, comparisons are made with ladder and cascade biquad realisations that are based on fully-balanced Euler integrators[10]. The sum-sensitivity of the gain responses to variations in component values are plotted in Fig. 4.9. It can be seen that both the SS and DS bilinear designs have the lowest sensitivity in the passband. Fig. 4.10 shows a plot of the group delay sensitivities to component variations. The cascade biquad design shows the lowest group delay sensitivity while increasing sensitivities are exhibited by the DS-bilinear integrator ladder, followed by the SS-bilinear integrator ladder and the Euler integrator ladder.

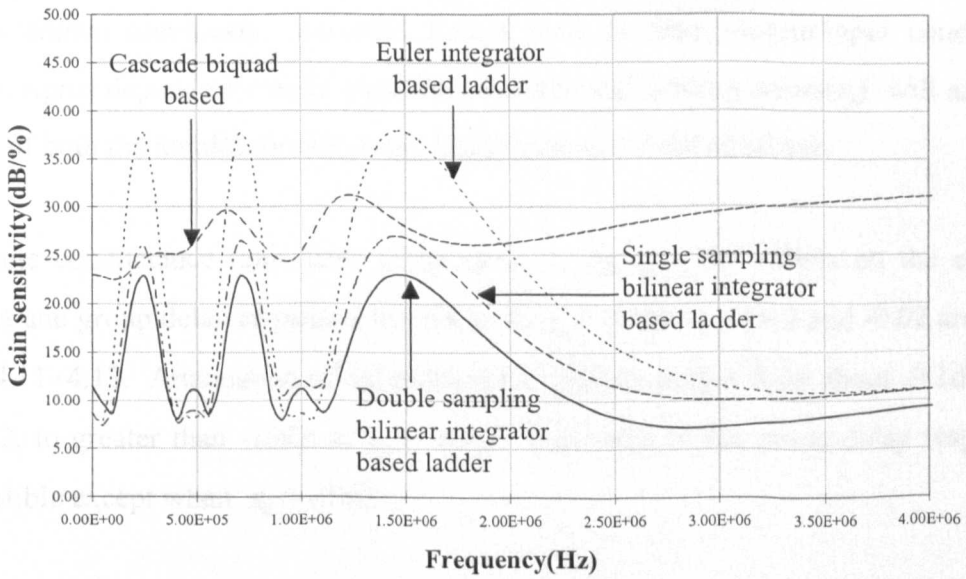


Figure 4.9 Gain response sensitivities

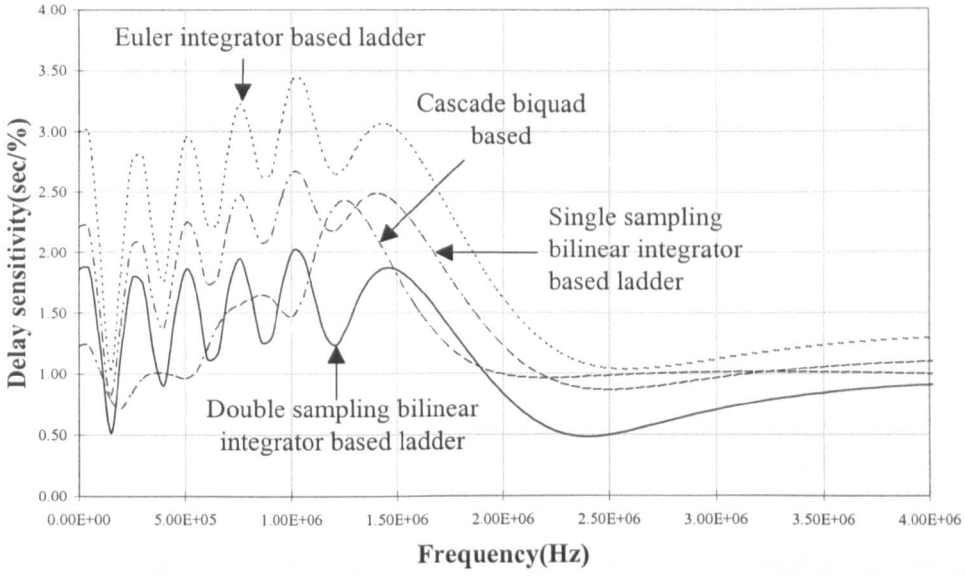


Figure 4.10 Group delay sensitivities

B. Non-ideal Factors

In a delay equaliser, the accuracy of both the group delay and amplitude responses are important to achieve the required delay compensation, while introducing minimum distortion to the amplitude response of the system being equalised. Although the amplitude response is completely insensitive to deviations in the components within the reactive ladder as shown previously, non-ideal factors such as finite output/input conductance ratios(ε_g), signal dependent charge injection errors(ε_c) and settling errors(ε_s) will affect the accuracy of both the amplitude and group delay response of the equaliser.

For a finite conductance ratio error factor of $\varepsilon_g = -2g_o/gm$, the effects on the equaliser amplitude and group delay responses for values of ε_g = -0.0002, -0.002 and -0.02 are shown in Figs. 4.11~4.13. Attenuation of the passband amplitude ranges from about -0.1dB for ε_g = -0.0002, to greater than -10dB at ε_g = -0.02. Deviation in the group delay response is imperceptible except when ε_g = -0.02.

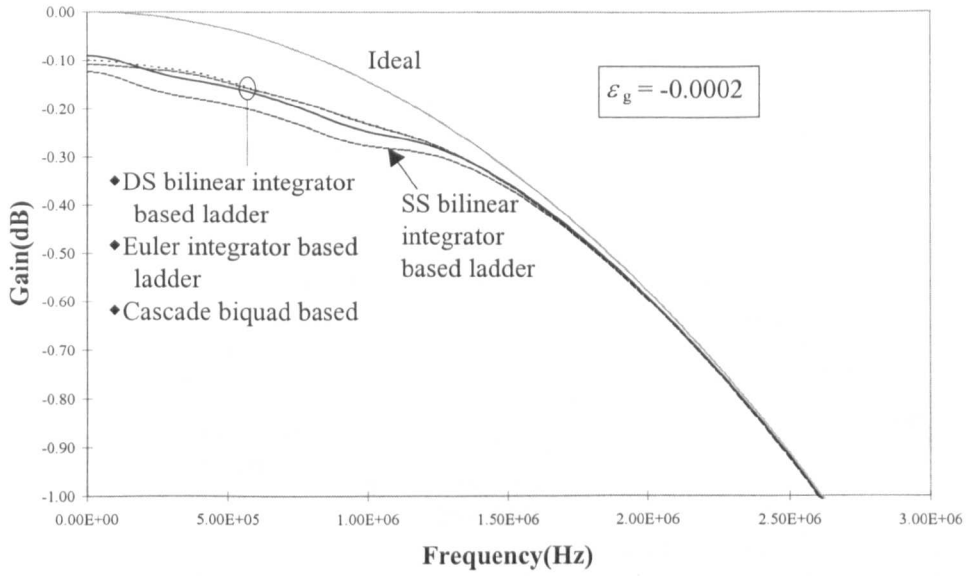


Figure 4.11a Amplitude response of the equalisers for a finite conductance ratio error factor of ε_g = -0.0002

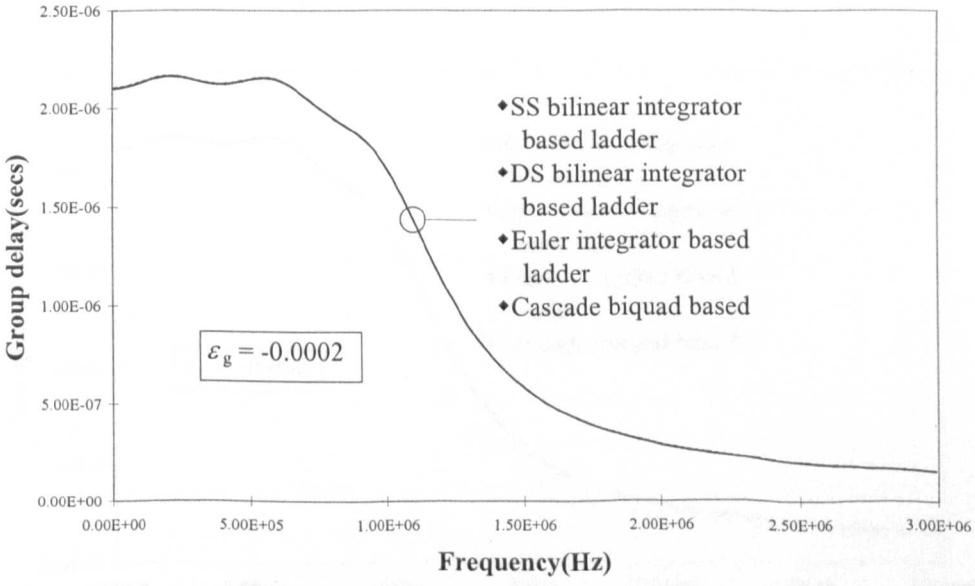


Figure 4.11b Group delay response of the equalisers for a finite conductance ratio error factor of ε_g = -0.0002

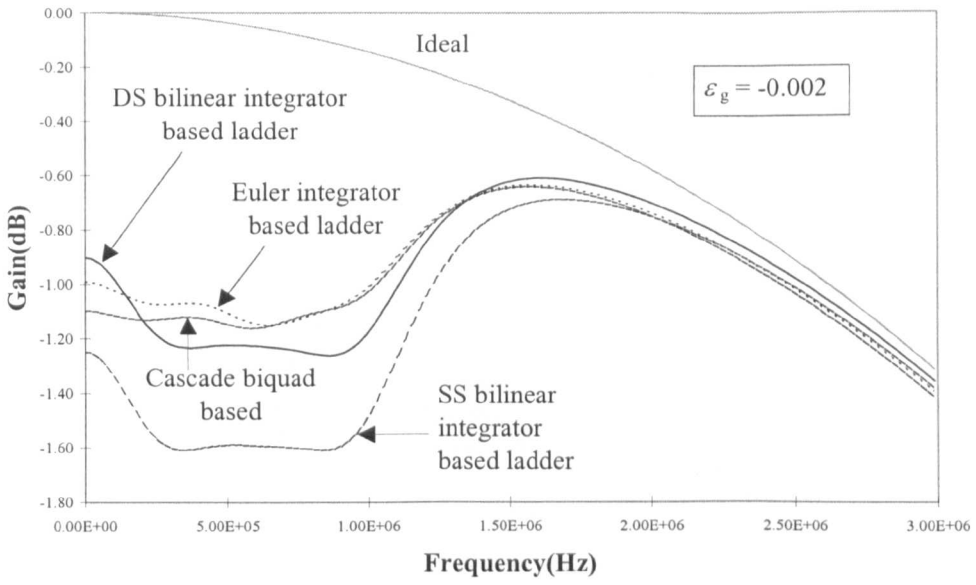


Figure 4.12a Amplitude response of the equalisers for a finite conductance ratio error factor of ε_g = -0.002

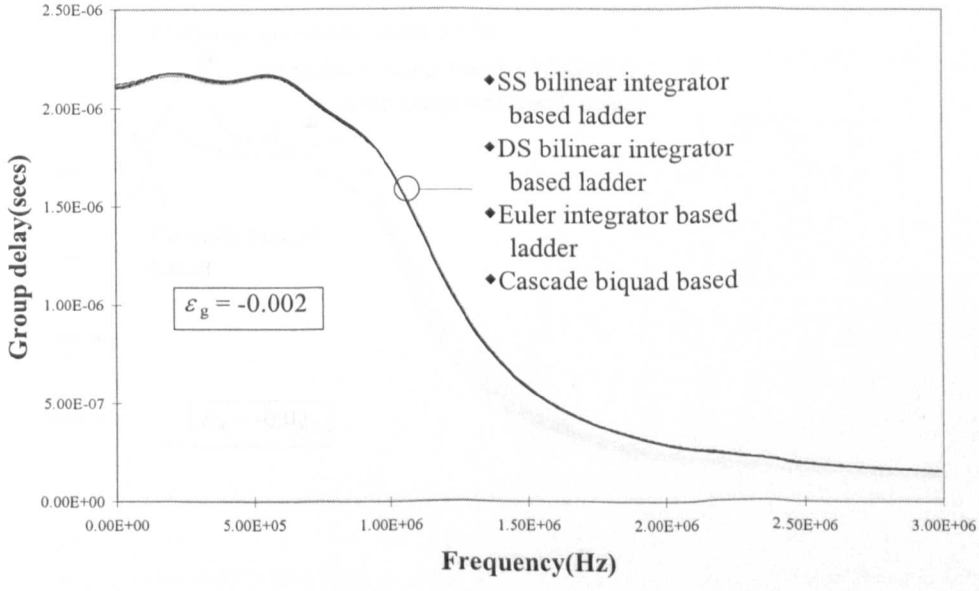


Figure 4.12b Group delay response of the equalisers for a finite conductance ratio error factor of ε_g = -0.002

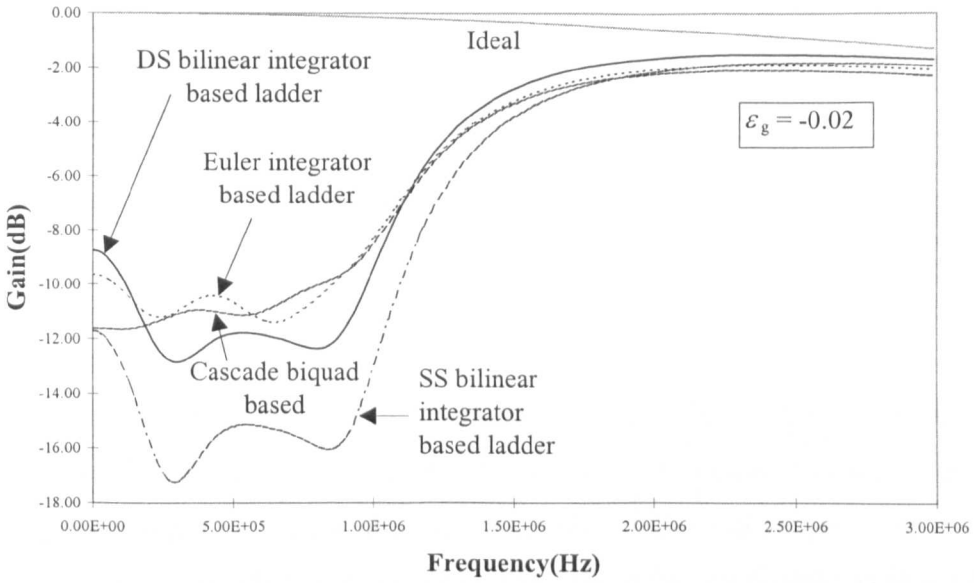


Figure 4.13a Amplitude response of the equalisers for a finite conductance ratio error factor of ε_g = -0.02

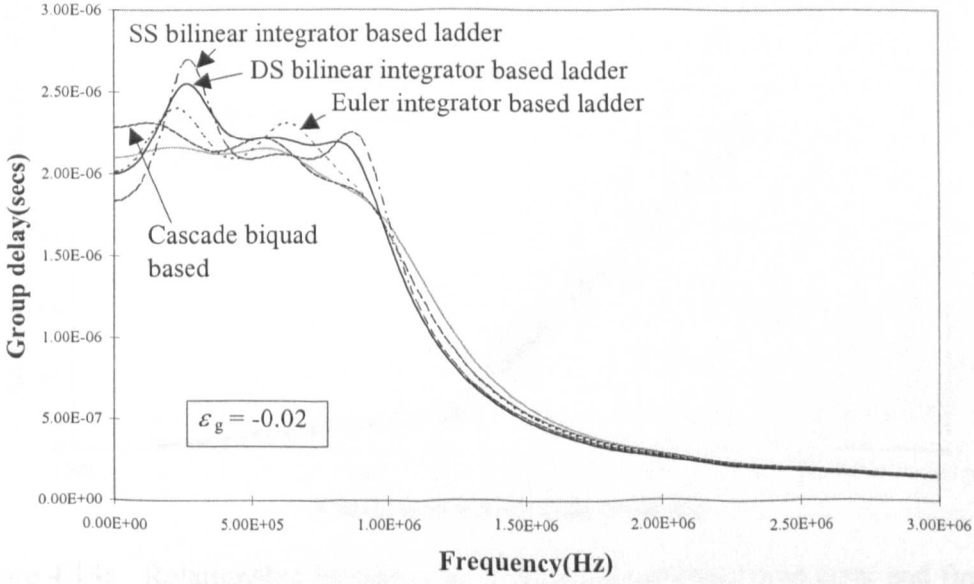


Figure 4.13b Group delay response of the equalisers for a finite conductance ratio error factor of ε_g = -0.02

The deviations from ideal over the passband of both the amplitude and group delay responses can be plotted against the non-ideal factor by defining the error measures of *absolute gain error* and *absolute group delay error* as

$$\int_0^{\text{Passband}} \left| |H_i(\omega)| - |H(\omega)| \right| d\omega \tag{4.31}$$

$$\int_0^{\text{Passband}} |GD_i(\omega) - GD(\omega)| d\omega \tag{4.32}$$

The respective plots against the finite conductance ratio error factor of ε_g are shown in Figs. 4.14a and 4.14b. From these, it is clear that the SS-bilinear integrator based ladder suffers the highest passband gain error and the Euler integrator based ladder the least. For group delay error, the worst affected is again the SS-bilinear integrator based ladder while the cascade biquad design is the least affected.

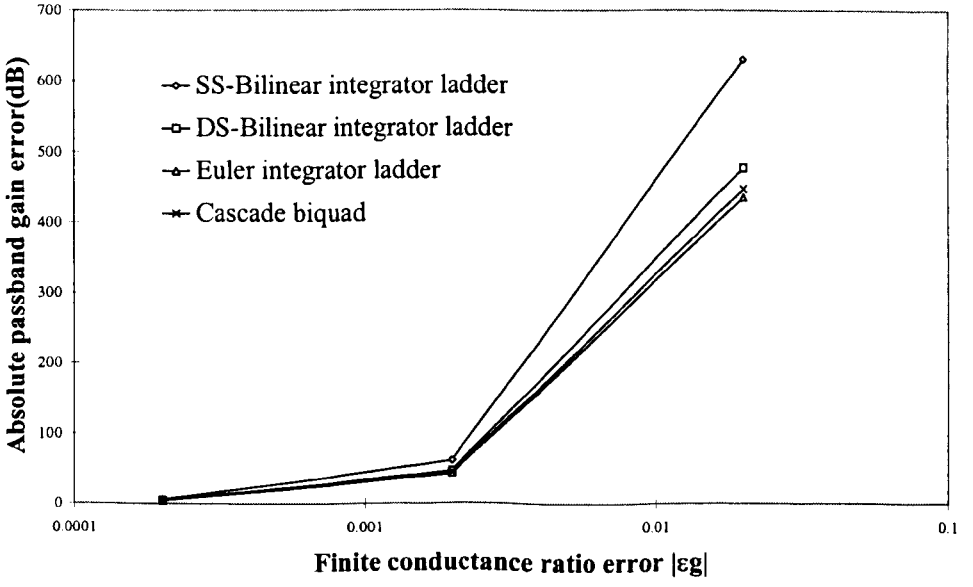


Figure 4.14a Relationship between the cumulative passband gain error and finite conductance ratio error(ε_g)

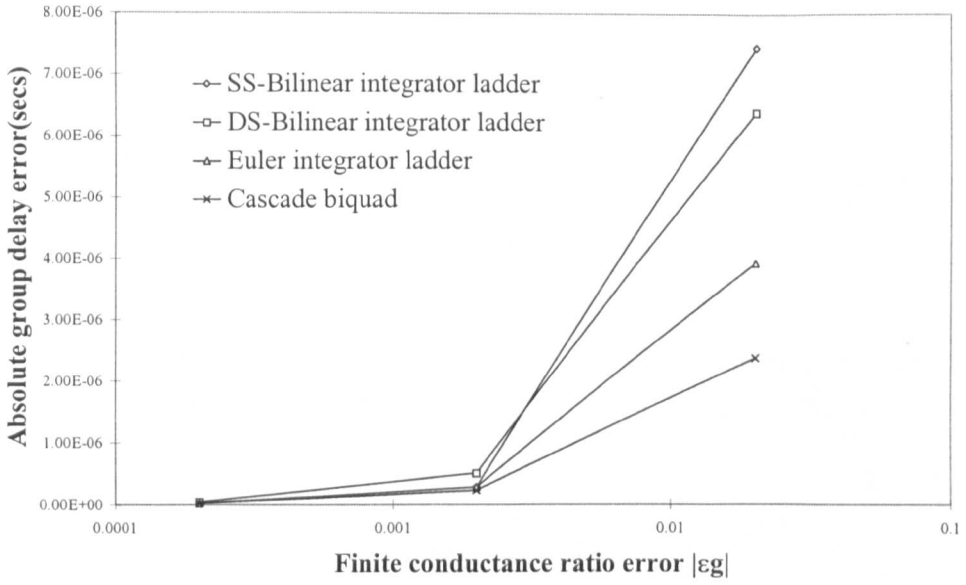


Figure 4.14b Relationship between the cumulative passband group delay error and finite conductance ratio error(ε_g)

Consider a small signal, signal dependent charge injection error factor of ε_c which generates an error current in a memory cell of $i_{err} = i_{in}\varepsilon_c$, and results in an output current of $i_o = -i_{in}+i_{err} = -i_{in}(1-\varepsilon_c)$. The effects on the equaliser amplitude and group delay responses for values of ε_c = 0.001, 0.01 and 0.05 are shown in Figs. 4.15~4.17. Attenuation of the passband amplitude ranges from about -0.2dB~ -0.4dB for ε_c = 0.001, to about -9dB~ -20dB at ε_c = 0.05. Deviation in the group delay response is insignificant except when ε_c = 0.05.

The plots of cumulative passband gain error and group delay error are shown in Figs. 4.18a and 4.18b respectively. It is clear that best overall design is the DS-bilinear integrator based ladder. As for the remaining designs, the gain responses are affected to a similar extent while the SS-bilinear integrator based ladder has a marginally better group delay response.

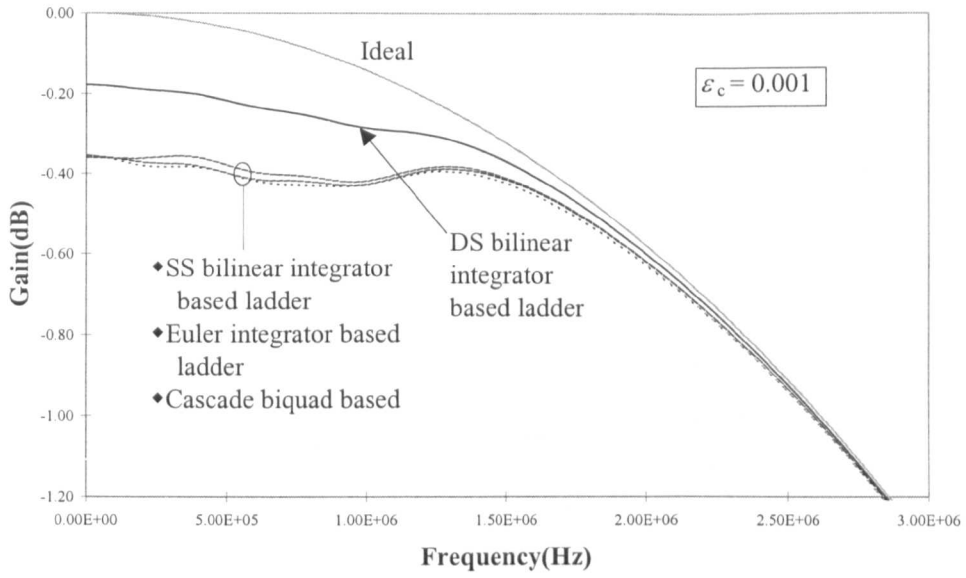


Figure 4.15a Amplitude response of the equalisers for a charge injection factor of $\varepsilon_c = 0.001$

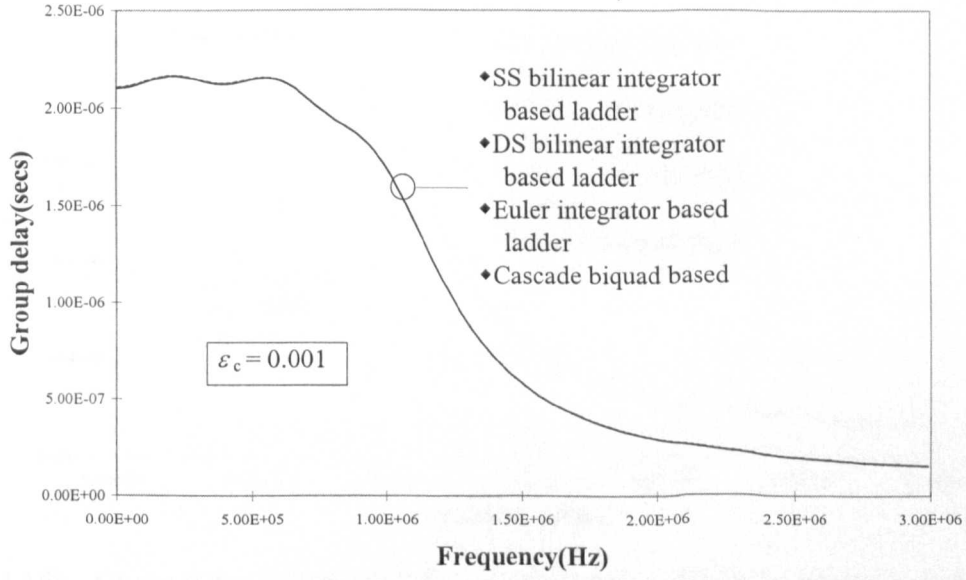


Figure 4.15b Group delay response of the equalisers for a charge injection error factor of $\varepsilon_c = 0.001$

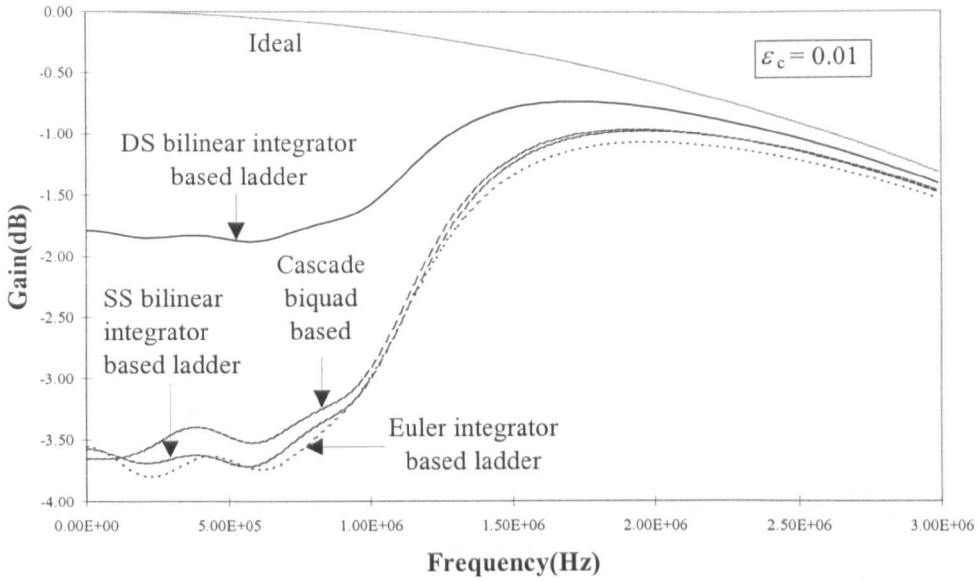


Figure 4.16a Amplitude response of the equalisers for a charge injection factor of $\varepsilon_c = 0.01$

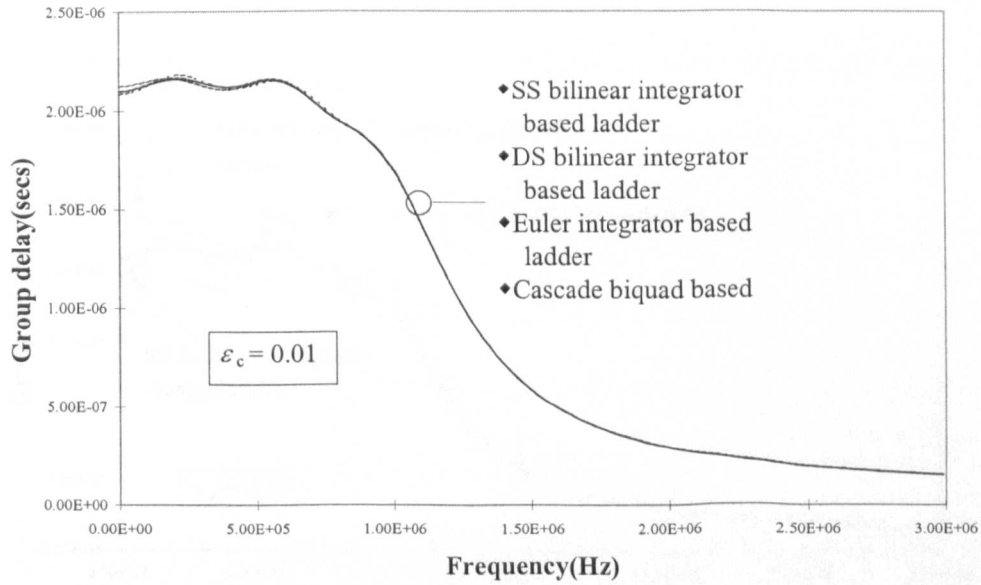


Figure 4.16b Group delay response of the equalisers for a charge injection error factor of $\varepsilon_c = 0.01$

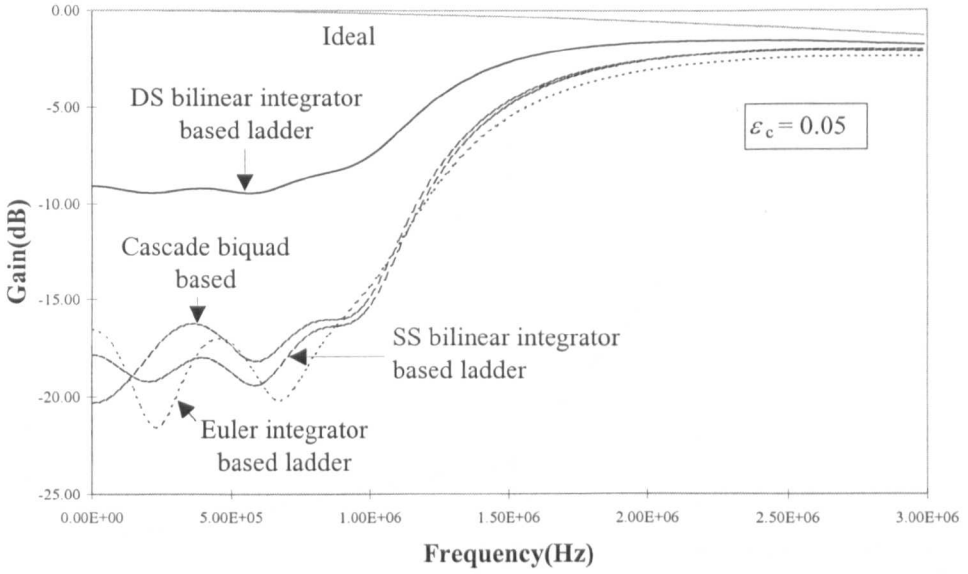


Figure 4.17a Amplitude response of the equalisers for a charge injection factor of $\varepsilon_c = 0.05$

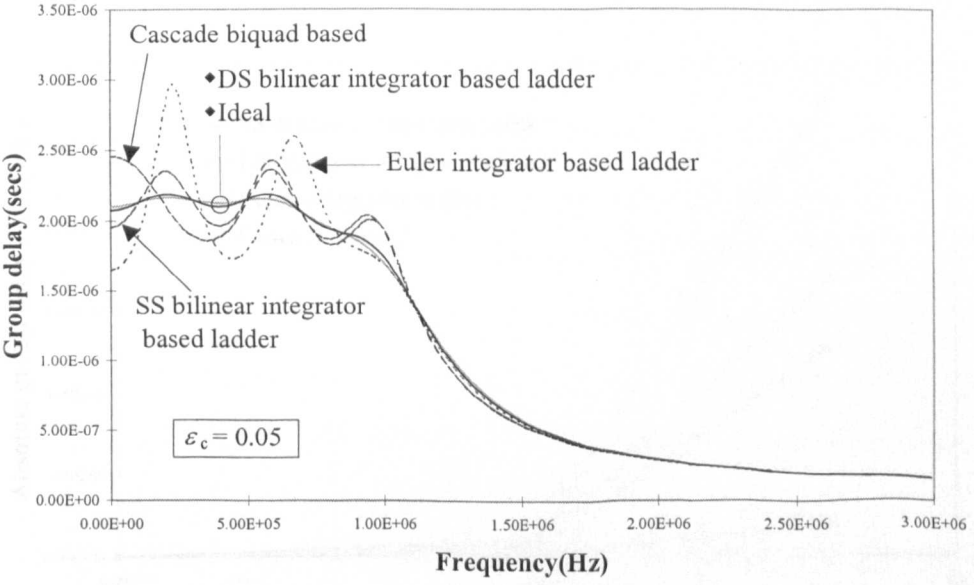


Figure 4.17b Group delay response of the equalisers for a charge injection error factor of $\varepsilon_c = 0.05$

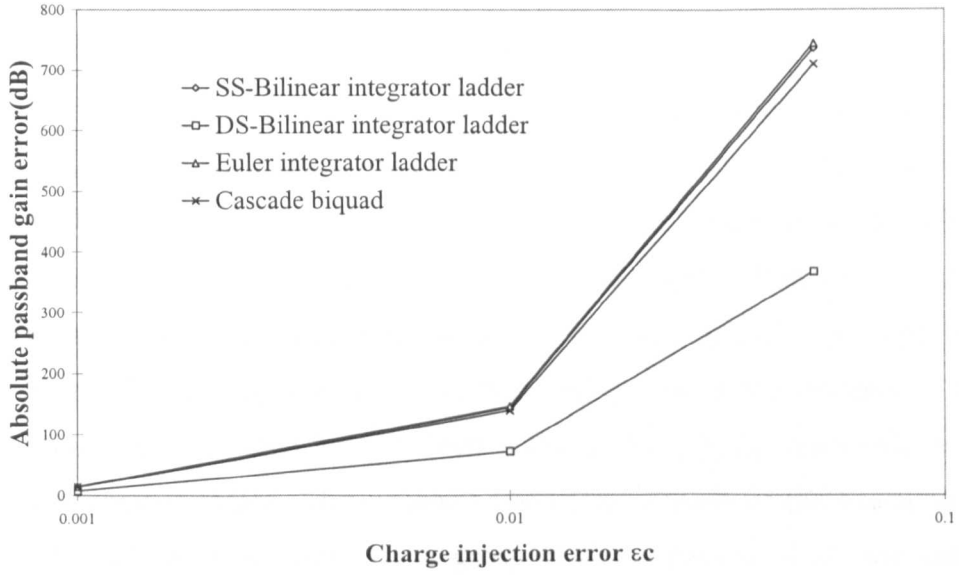


Figure 4.18a Relationship between the cumulative passband gain error and charge injection error(ε_c)

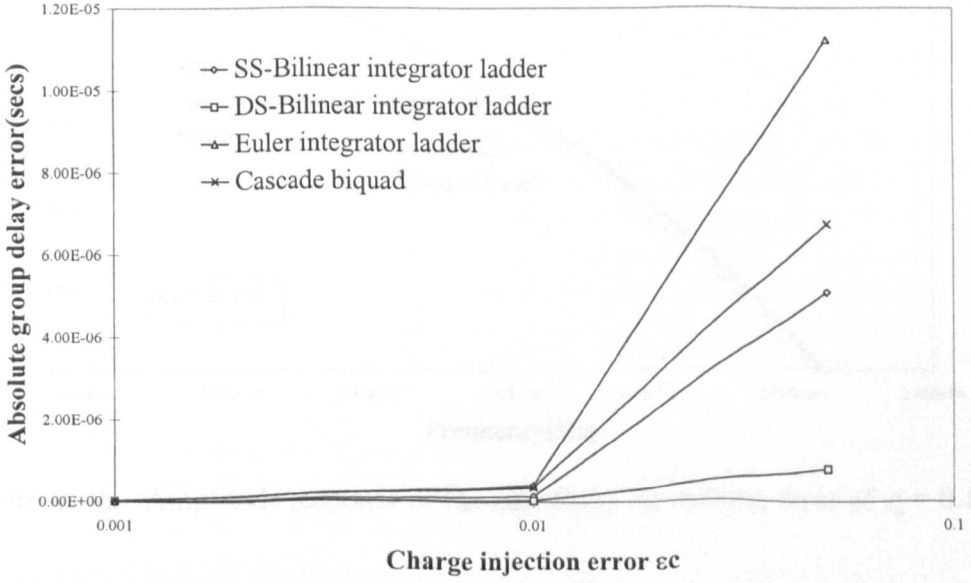


Figure 4.18b Relationship between the cumulative passband group delay error and charge injection error(ε_c)

Settling errors originate from incomplete charging of the memory gate-source capacitor in the duration of the sampling phase. This results in a non-linear output error current which introduces distortion to the circuit. For simplicity, we can ignore the non-linearities. The effect of a linear, small signal settling error ε_s on the amplitude and group delay responses of the equalisers are shown in Figs. 4.19~ 4.21. For the same settling time constant, the responses of the DS-bilinear integrator based ladder are minimally affected due to a doubling of available settling time resulting from halving the clock frequency. Both the Euler and SS-bilinear integrator based ladders suffer peaking of the amplitude response at the cutoff frequency of 1MHz. The passband gain of the cascade biquad based equaliser is minimally affected in comparison. The group delay responses of all the designs are generally robust to settling errors.

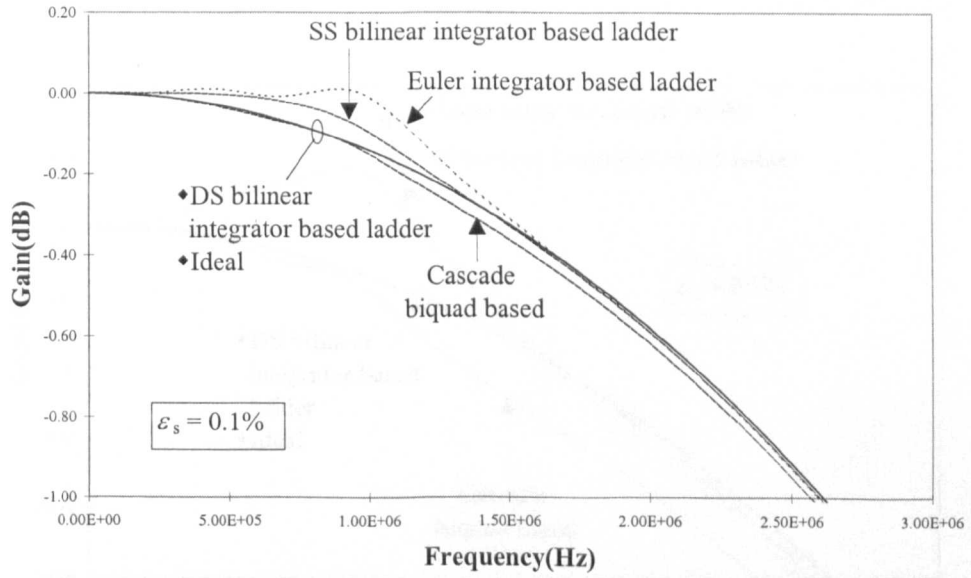


Figure 4.19a Amplitude response of the equalisers for settling error of $\varepsilon_s = 0.1\%$

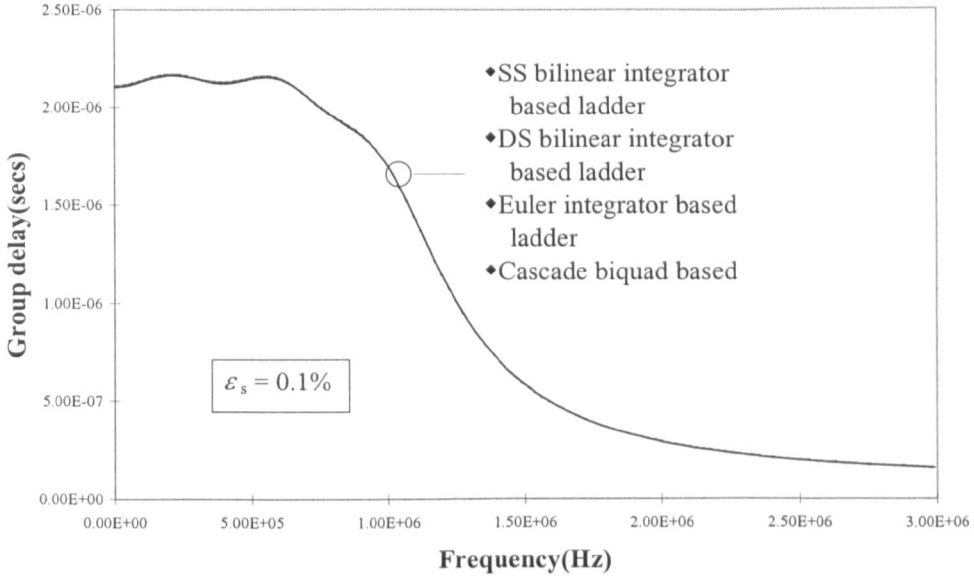


Figure 4.19b Group delay response of the equalisers for settling error of $\varepsilon_s = 0.1\%$

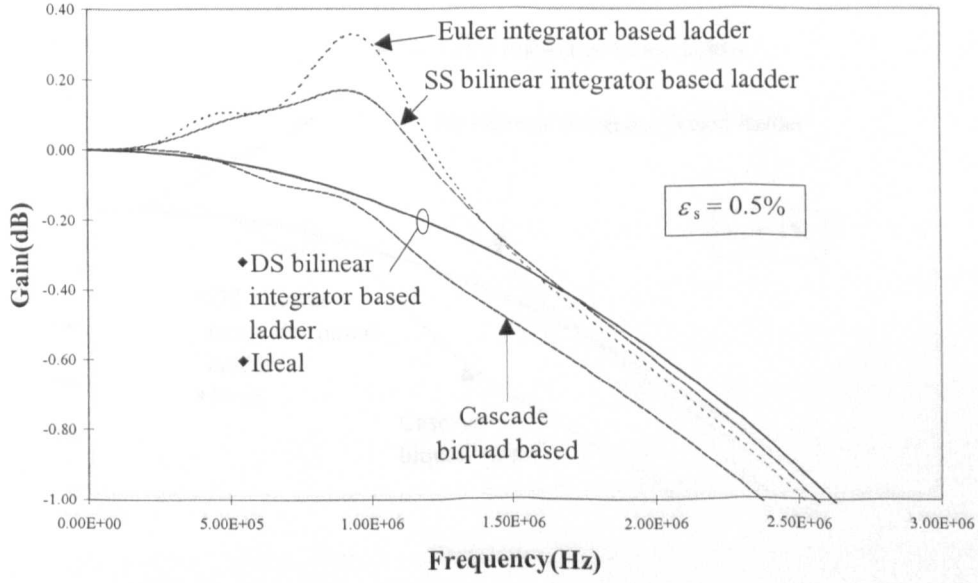


Figure 4.20a Amplitude response of the equalisers for settling error of $\varepsilon_s = 0.5\%$

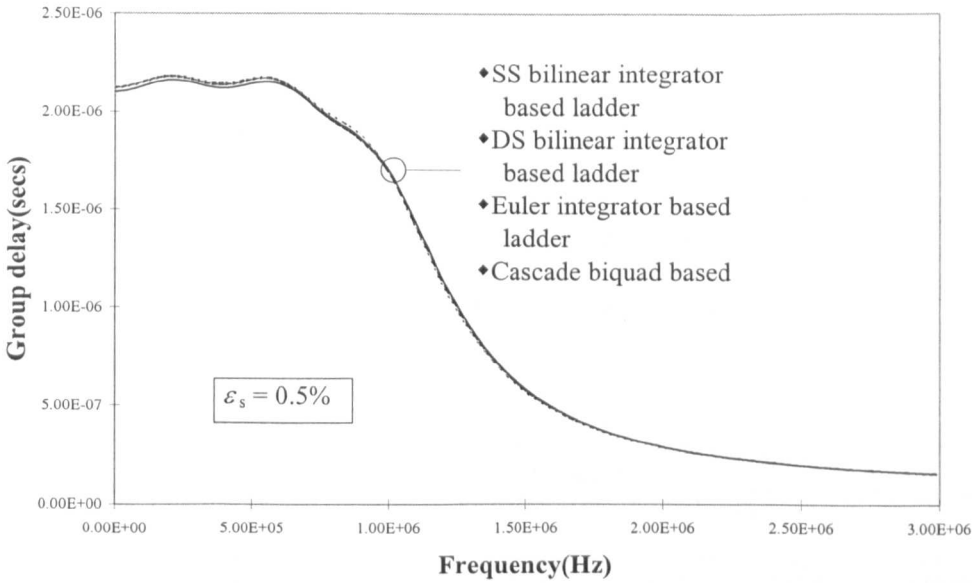


Figure 4.20b Group delay response of the equalisers for settling error of $\varepsilon_s = 0.5\%$

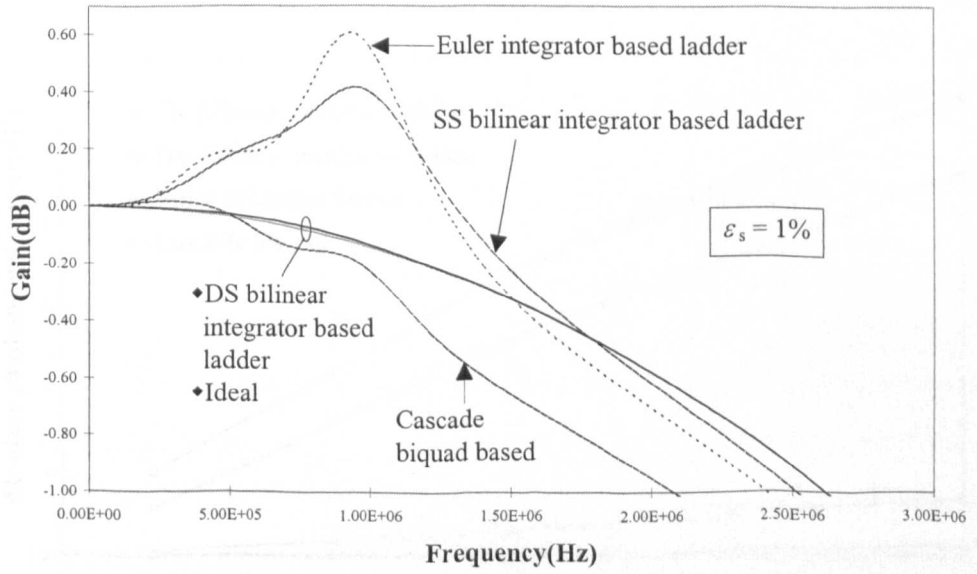


Figure 4.21a Amplitude response of the equalisers for settling error of $\varepsilon_s = 1\%$

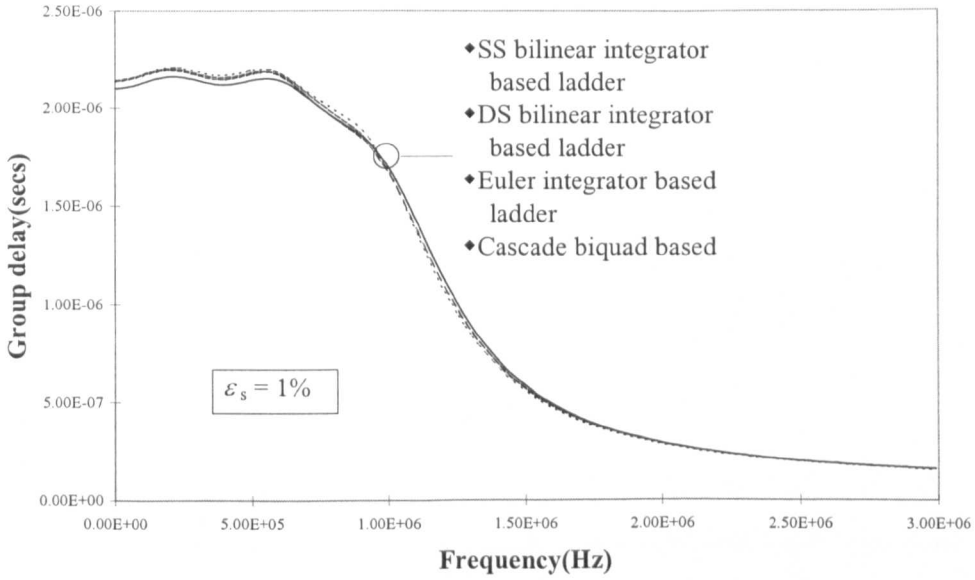


Figure 4.21b Group delay response of the equalisers for settling error of $\varepsilon_s = 1\%$

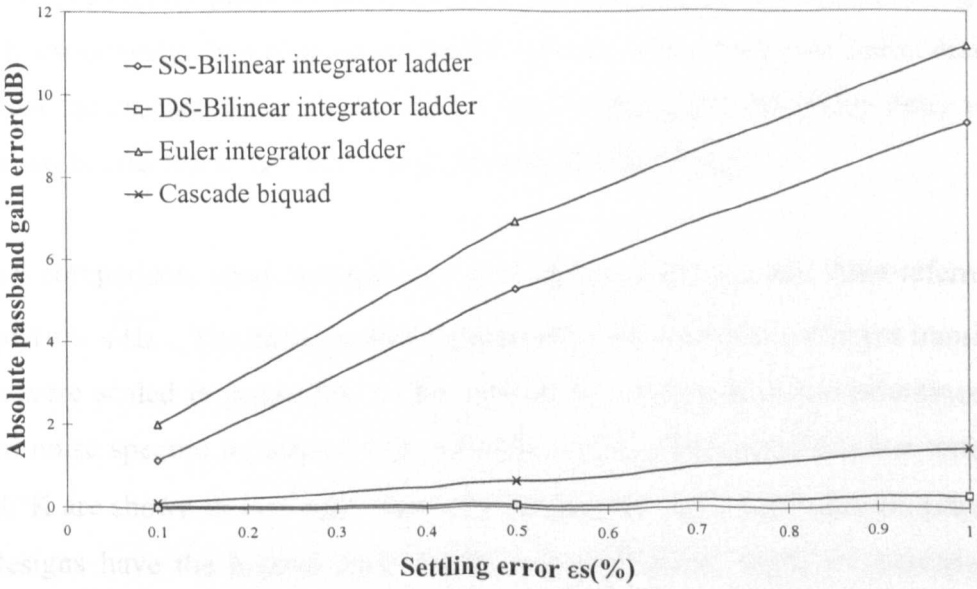


Figure 4.22a Relationship between the cumulative passband gain error and settling error(ε_s)

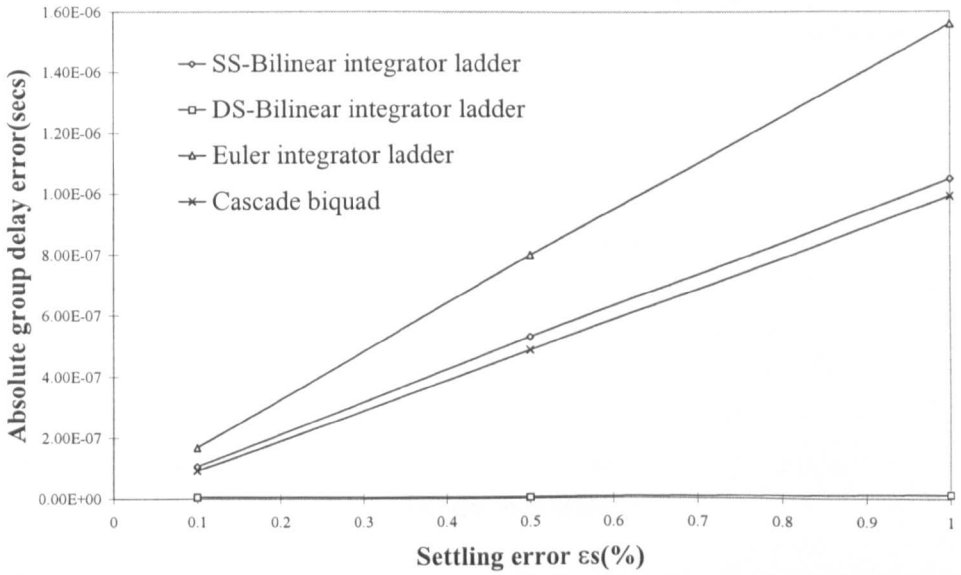


Figure 4.22b Relationship between the cumulative passband group delay error and settling error(ε_s)

The plots of cumulative passband gain error and group delay error are shown in Figs. 4.22a and 4.22b respectively. Not considering the DS-bilinear integrator based ladder design, it is evident that the cascade biquad based design has the best gain and group delay response while the worst affected is the Euler integrator based ladder design.

For a final comparison, noise simulations were performed using a unit drain-referred noise current of $1\text{nA}/\sqrt{\text{Hz}}$. The noise currents generated by the internal coefficient transistors of the filter were scaled in proportion to the root of the respective transconductances. The simulated noise spectral densities for an arbitrary, fixed noise-bandwidth at a temperature of T=300°K are shown in Fig. 4.23. Both the SS-bilinear and DS-bilinear integrator based ladder designs have the highest noise levels in the passband, while the cascade biquad based design has the lowest noise level.

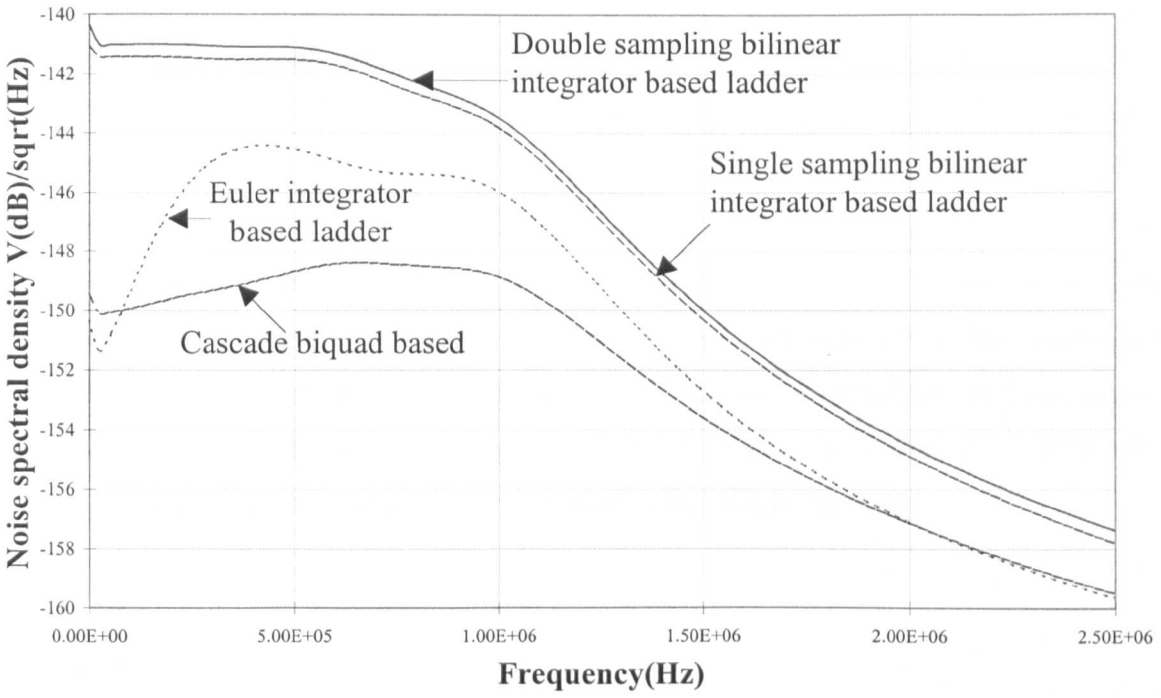


Figure 4.23 Simulated noise spectral densities for an arbitrary, fixed noise-bandwidth and a unit reference noise current of $1\text{nA}/\sqrt{\text{Hz}}$

4.4 CONCLUSIONS

Procedures for deriving bilinear integrator based SI allpass equalisers, based on describing the allpass function as the sum of a constant and a ladder realisable term, have been presented. The design can proceed either in the s-domain or directly in the z-domain when a passive prototype is first synthesised using the respective continued-fraction expansions. Thereafter, standard matrix methods are used to simulate the allpass structure. The reasons for implementing the allpass filter using bilinear type integrators are twofold. Firstly, bilinear integrators do not suffer from excess phase and directly implement the bilinear-transform. Secondly, bilinear integrator based equalisers are structurally different from Euler integrator based equalisers, and their sensitivity and non-ideal characteristics merit investigation. It was also shown that the magnitude of the bilinear equaliser is always equal to 1 regardless of the deviation in the elements of the reactive ladder section. Generally, it can be summarised that the best amplitude and group delay sensitivities are shown by the bilinear integrator based designs and the cascade biquad design respectively, while the Euler integrator based design fared poorly. For finite conductance ratio errors, the design

with the worst affected gain and group delay response is the SS bilinear integrator based equaliser, while the group delay of the cascade biquad design is least affected. For small signal signal dependent charge injection error, the best design appears to be the DS-bilinear integrator based ladder, with both gain and group delay responses of the Euler integrator based ladder design being the worst affected. For settling errors, the gain response of both the Euler integrator based ladder and the SS-bilinear integrator based designs perform worse than the cascade biquad design. The group delay response of all the designs are robust to the range of settling errors, but the Euler integrator based ladder fared marginally worse. For noise performance, the bilinear integrator based ladder designs are significantly worse than the cascade biquad and Euler integrator based ladder designs.

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CHAPTER 5:

LADDER DERIVED SWITCHED-CURRENT DECIMATORS AND INTERPOLATORS

5.1 INTRODUCTION

Decimators and interpolators are the basic building blocks used in multirate signal processing[1]. They effect changes in sampling rates and play important roles in many functions ranging from relaxing the specification of continuous time anti-aliasing(AAF), anti-imaging filters(AIF)[2] to realising of narrowband bandpass filters[3]. Switched-current systems[4] are sampled-data in nature and thus also require the bandlimiting of signals to prevent destructive aliasing. A high sampling rate relaxes the specifications of the continuous-time input AAF and output AIF but may pose problems of high component value spreads, high sensitivities to component variations and restricts time available for settling of system cells. A low sampling rate, while alleviating some of these problems, demands high order AAF and AIFs. These conflicting requirements are most conveniently reconciled by the use of decimators and interpolators[5].

SI decimators and interpolators of both FIR and IIR types have been previously proposed[6,7]. These were implemented with polyphase branches and delay blocks that permit operation at the lower sampling rate Fs, thus maximising the time available for settling. FIR structures are important for their linear phase, constant group delay characteristics. However, FIR decimators are generally less selective, unless long impulse response lengths are used[7]. SI IIR structures have been obtained by applying the multirate-transform[1] to a prototype z transfer function and implemented as direct-form structures[6]. Although able to realise highly selective functions more efficiently, direct form structures are known to be more sensitive than doubly terminated ladders. In [8], SI biquad decimators and interpolators were used in the design of narrowband bandpass filters. This is not an optimum solution as settling times of the prototype filters are determined by the higher sampling frequencies and biquads are also known to be quite sensitive to component variations.

A switched-capacitor decimator was recently proposed[9] which combined low-sensitivity ladder structures with polyphase input branches. The method was based on the state-space multirate-transformation of an all-pole LDI ladder filter operating at the higher frequency MFs to one that operates at the lower frequency Fs. The approximate-LDI transformation[2] introduces distortion to the passband characteristic which deteriorates

with decreasing Fs/fo ratio, whereas the exact-LDI transformation does not. Further, all-pole responses lack the selectivity of elliptic responses.

In this chapter, switched-current IIR decimators and interpolators are proposed, which are based on the above procedure, but extended to bilinear-transformed, elliptic ladder structures. The use of bilinear-transformation ensures exactness of response and increases selectivity by compression of the frequency axis. Highly selective elliptic type responses with finite-transmission zeros can also be realised. In addition, the low passband sensitivity of doubly-terminated ladders is preserved and settling time is maximised by operation at the lower sampling frequency Fs. Two types of decimator architectures which will realise the multirate transfer function, FIR-IIR Cascade(FIC) and Multiple Feed-In(MFI), are proposed and the steps for deriving them detailed. Applying direct transposition, it is shown how the interpolator structures can be obtained without the need for redesign. These are illustrated using an example of a 3rd order elliptic lowpass prototype for a downsampling and upsampling ratio of M=L=2 respectively. The remainder of this chapter deals with sensitivity of these circuits and it is shown that the absence of tight coupling in the IFC structure results in lower sensitivity in the stopband.

5.2 DESIGN PROCEDURE USING MULTIRATE TRANSFORMATIONS

The basic purpose of a decimator is to reduce the incoming sampling rate at MFs to Fs at the output as shown in Fig. 5.1. Conceptually, the output signal is formed by discarding every M'th sample. The frequency responses and signal spectra involved in a decimating operation of M=2 are shown in Fig. 5.2. The continuous-time anti-aliasing filter preceding the decimator can be of low order because the higher input sampling rate(MFs) of the decimator means the images of the input signal spectrum will be spaced further apart. To prevent aliasing at the decimator output, the input baseband spectrum has to be band-limited to less than half the output sampling rate, Fs/2. Therefore, even though the prototype filter within the decimator can have any arbitrary amplitude response, it has to reject spectral content beyond Fs/2. However, there are exceptions in multistage designs when some aliasing is tolerated, provided it falls within the filter transition band[1]. The

output spectrum of the decimator is shown by a solid trace in the lower half of Fig. 5.2. An un-bandlimited input signal will result in aliasing as indicated by the dotted lines.

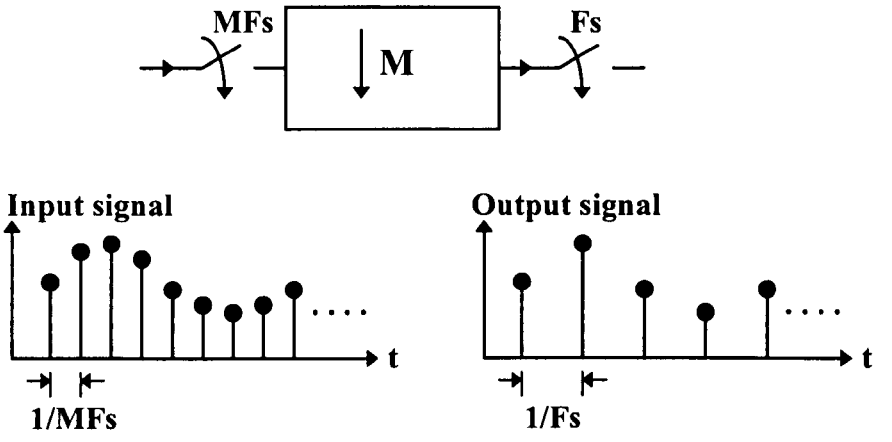


Figure 5.1 Symbolic representation of a decimator and its time domain input output signals

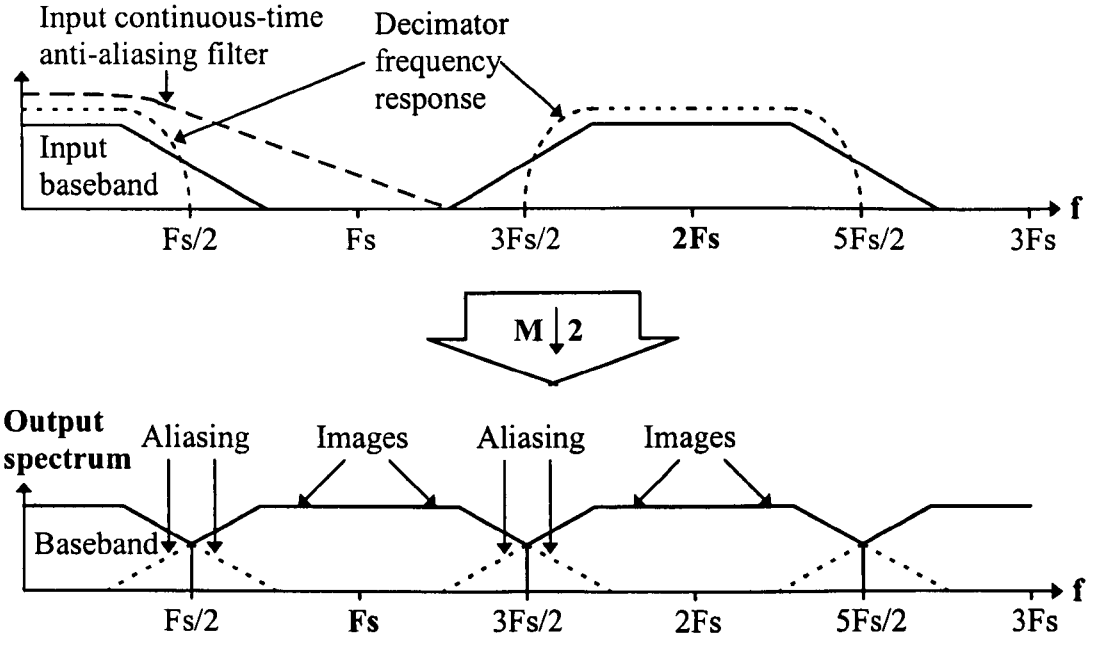


Figure 5.2 Frequency domain representation of decimation by M=2

A first-order discrete time transfer function can be transformed into a multirate transfer function by using the equality[1]

$$\frac{1}{1-az^{-1}} = \frac{\sum_{k=0}^{M-1}(a\,z^{-1})^k}{1-a^M z^{-M}} \tag{5.1}$$

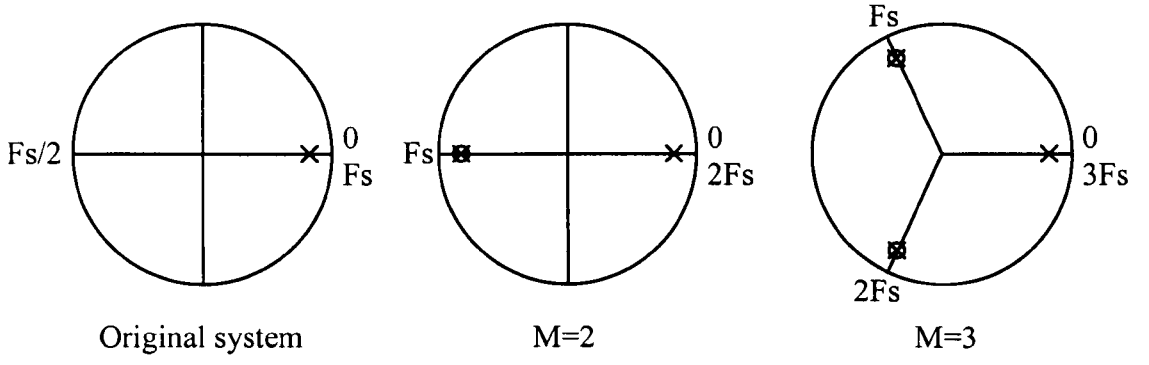


Figure 5.3 Poles and zeros in the z-plane for a 1st order multirate transformed system for M=2 and M=3 respectively

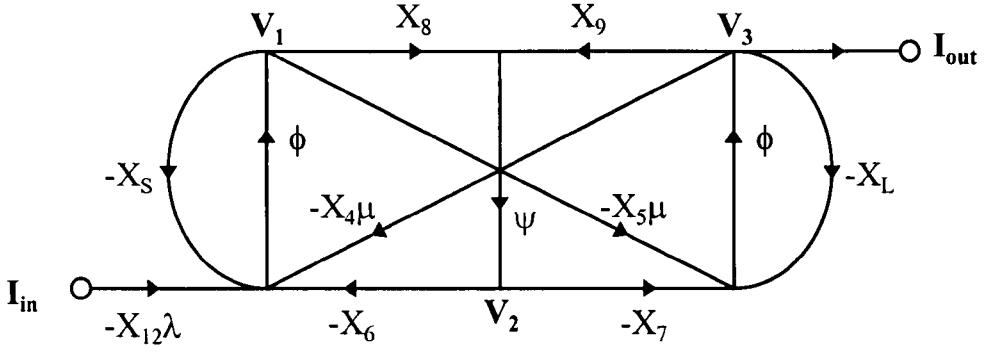
The relationship in (5.1) states that the original system(LHS) operates at a single high sampling rate of MFs while the equivalent transformed system(RHS) has a denominator that operates at the low sampling rate of Fs. In addition, there are now M number of poles and a numerator term that introduces M-1 number of zeros. However, the different transfer functions are nominally equal due to the pole-zero cancellations shown in Fig. 5.3.

This equivalence can be extended to transform matrix polynomials described in state-space formulation[9] by re-writing (5.1) as

$$\mathbf{I} - \mathbf{A}^M z^{-M} = \sum_{k=0}^{M-1} (\mathbf{A}z^{-1})^k . (\mathbf{I} - \mathbf{A}z^{-1}) \tag{5.2}$$

The state-space transfer function of a z-domain ladder structure operating at the higher sampling frequency MFs can be expressed[8] in terms of $\mathbf{I}\text{-}\mathbf{A}z^{-1}$. Using eqn.(5.2), the transfer function of an approximate-LDI SC filter was transformed from single-rate to multirate, with the denominator represented by the same recursive ladder structure and the numerator by an FIR polyphase network[9]. The entire structure operates at the lower sampling frequency Fs. This method can also be used to transform bilinear-LDI type filters.

The response of bilinear-transformed structures are exact and typically have a zero at half the clock frequency. This zero is usually realised by a $\lambda=1+z^{-1}$ factor or a bilinear integrator stage at either the input or output of a bilinear-LDI[10] filter. Also, elliptic responses contain finite transmission zeros which are realised by cross-coupling feed-through branches, i.e. $-X_4\mu$ and $-X_5\mu$ as shown in Fig. 5.4 for the signal flowgraph(SFG) of a 3rd order Right-LU[10] lowpass filter.



$$\phi = k\frac{1}{1-z^{-1}},\quad \psi = k\frac{z^{-1}}{1-z^{-1}},\quad \mu=(1-z^{-1}),\ \lambda=(1+z^{-1})$$

Figure 5.4 Signal-flowgraph of prototype filter

The differences between this bilinear-transformed SFG and that of a typical approximate-LDI transformed, all-pole one, are the presence of feed-through branches and the $\lambda=(1+z^{-1})$ term. A first order bilinear transfer-function has a numerator term of $(1+z^{-1})$. This can be multirate-transformed using the equivalence

$$1+z^{-1} = 2-\frac{1-z^{-M}}{\sum_{k=0}^{M-1} z^{-k}} \tag{5.3}$$

The system of equations describing the SFG in Fig. 1 are written as:

$$\begin{bmatrix} 1+X_S & X_6 & X_4 \\ 0 & 1 & 0 \\ X_5 & X_7 & 1+X_L \end{bmatrix}\begin{bmatrix} V_1(z) \\ V_2(z) \\ V_3(z) \end{bmatrix} - z^{-1}\begin{bmatrix} 1 & 0 & X_4 \\ X_8 & 1 & X_9 \\ X_5 & 0 & 1 \end{bmatrix}\begin{bmatrix} V_1(z) \\ V_2(z) \\ V_3(z) \end{bmatrix} = \begin{bmatrix} -X_{12} \\ 0 \\ 0 \end{bmatrix}(1+z^{-1})V_{in}(z) \tag{5.4}$$

or in compact form,

$$(\mathbf{A}-z^{-1}\mathbf{B})\mathbf{V}(z)=\mathbf{C}(1+z^{-1})V_{in}(z) \tag{5.5}$$

The output equation is given simply by

$$V_{out}(z) = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_1(z) \\ V_2(z) \\ V_3(z) \end{bmatrix} = \mathbf{D}\mathbf{V}(z) \tag{5.6}$$

To perform the multirate transformations, multiply both sides of (5.5) by $\mathbf{A}^{-1}$ to give

$$(\mathbf{I}-z^{-1}\mathbf{A}^{-1}\mathbf{B})\mathbf{V}(z)=\mathbf{A}^{-1}\mathbf{C}(1+z^{-1})V_{in}(z) \tag{5.7}$$

Applying (5.2) to the left hand side and (5.3) to the right hand side of (5.7) yields

$$\left[\mathbf{I}-(\mathbf{A}^{-1}\mathbf{B})^{M} z^{-M}\right]\mathbf{V}(z) = \mathbf{X}(z)V_{in}(z) \tag{5.8}$$

where

$$\mathbf{X}(z) = \sum_{k=0}^{M-1} (\mathbf{A}^{-1}\mathbf{B})^{k} z^{-k} \mathbf{A}^{-1}\mathbf{C}\left(2 - \frac{1-z^{-M}}{\sum_{k=0}^{M-1} z^{-k}}\right) = [\mathbf{X}_1(z) \quad \mathbf{X}_2(z) \quad \mathbf{X}_3(z)]^{T} \tag{5.8a}$$

Substituting (5.6) into (5.8) yields the multirate transfer function.

$$\frac{V_{out}(z)}{V_{in}(z)} = \mathbf{D}\left[\mathbf{I}-(\mathbf{A}^{-1}\mathbf{B})^{M} z^{-M}\right]^{-1}\mathbf{X}(z) \tag{5.9}$$

The denominator terms have the form z^{-nM}, where M=decimation factor; n={0, 1, 2, . . N}; N=system order. Thus, the recursive ladder structure operates at the lower sampling frequency Fs, which translates through to increased time for the memory cells to settle.

5.3 DECIMATOR STRUCTURES FOR REALISING THE MULTIRATE TRANSFER FUNCTION

Table 5.1 Transistor ratios of the reference elliptic lowpass filter

X_4 1.486165e-01	X_9 3.196775e-01
X_5 2.386774e-01	X_S 4.576771e-01
X_6 7.560506e-01	X_L 4.576771e-01
X_7 9.581267e-01	X_{12} 3.611495e-01
X_8 4.051205e-01	

Transistor spread: 6.73

Consider the example of a 3rd order Right-LU[10] elliptic lowpass filter operating at the higher sampling frequency MFs with M=2. The filter transistor ratios corresponding to the SFG of Fig. 5.4 are listed in Table 5.1. Substituting these values into (5.4)-(5.6) to form the respective matrices and applying (5.9) results in the numerical multirate transfer function

$$H(z) = -\frac{\sum_{k=0}^{6} a_k z^{-k}}{\sum_{k=0}^{3} b_{2k} z^{-2k}} \tag{5.10}$$

where the coefficients are listed in Table 5.2.

Table 5.2 Coefficients of the numerical transfer function

$a_0 = 0.191961$	$a_6 = 0.088602$
$a_1 = 0.504075$	$b_0 = 4.681974$
$a_2 = 0.669239$	$b_2 = -3.688141$
$a_3 = 0.716499$	$b_4 = 3.167880$
$a_4 = 0.631172$	$b_6 = -1.0$
$a_5 = 0.360399$	

Next, a decimator architecture has to be determined which will realise (5.10) while preserving low passband sensitivity and allowing operation at the lower sampling frequency. Two SI decimator architectures, the FIR-IIR Cascade(FIC) and the Multiple Feed-In(MFI) are proposed. These will be compared to the Direct Form-II(DFII)[6] decimator structure.

5.3.1 Direct Form-II(DFII) Decimator Architecture

This is the most straightforward method, where a prototype z-transfer function given by

$$H(z) = \frac{N(z)}{D(z)} = \frac{\sum_{i=0}^{N-1} c_i z^{-i}}{1 + \sum_{i=1}^{D} d_i z^{-i}} \tag{5.11}$$

with a unit delay of 1/MFs and D = N-1, can be transformed[1,6] into a multirate transfer function expressed as

$$H(z) = \frac{\sum_{n=0}^{N-1}\left(\sum_{m=0}^{M-1} a_{n,m}\right)(z^M)^{-n}}{1+\sum_{n=1}^{N-1} b_n (z^M)^{-n}} \tag{5.12}$$

The inner sum of the numerator can be formed by connecting related sets of coefficient branches to an input commutator operating at MFs. The outer sum is then formed by feeding each set via the appropriate block delays to form a polyphase FIR network as shown in Fig. 5.5. The denominator is realised as a recursive Direct Form-II(DFII) network with feedback branches.

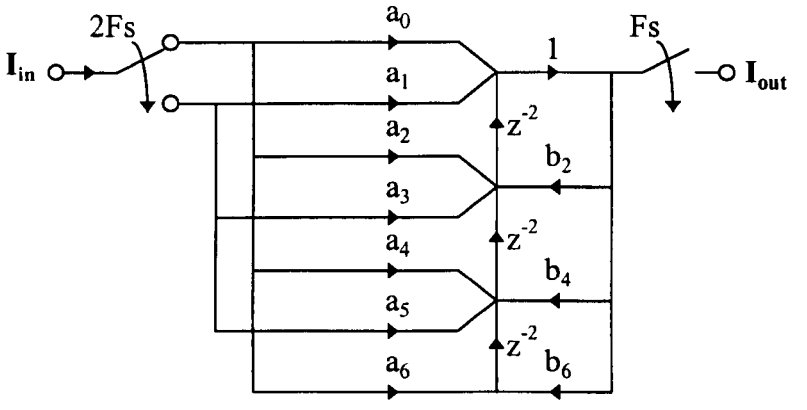


Figure 5.5 Signal-flowgraph of the Direct Form-II(DFII) decimator

The switched-current implementation of the DFII decimator is shown in simplified form in Fig. 5.6. The coefficients in Table 5.2 are directly implemented by the transistor ratios in the circuit.

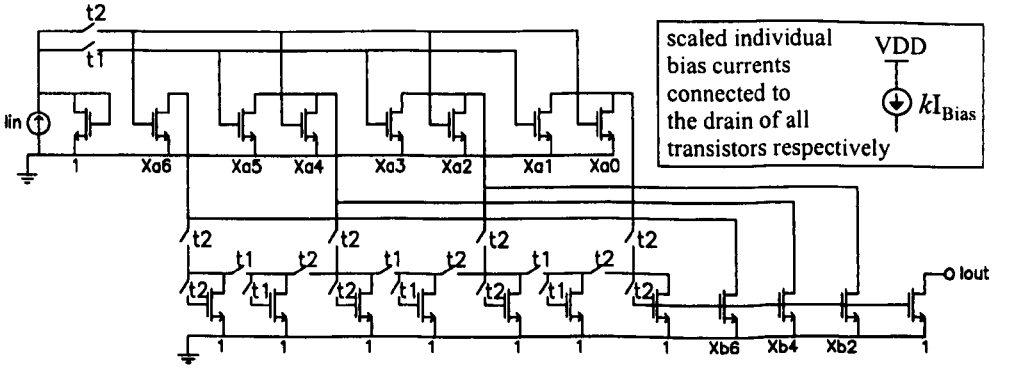
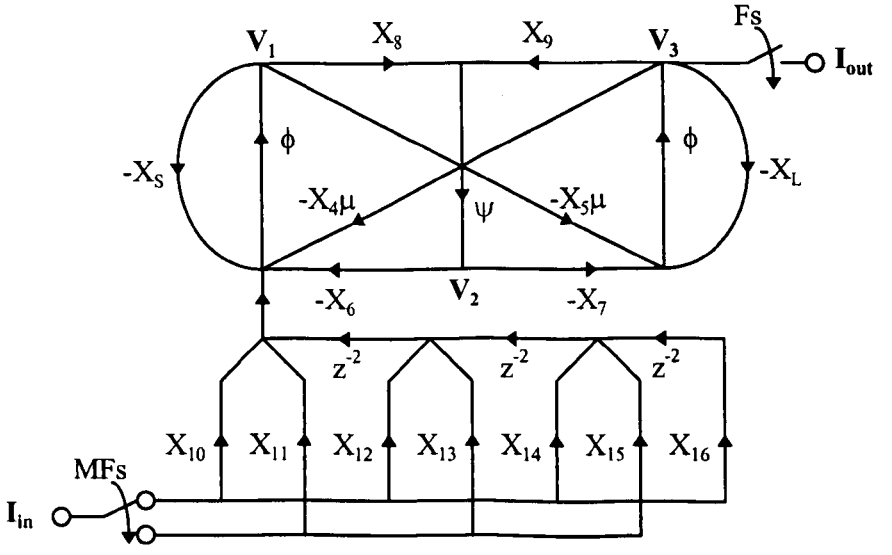


Figure 5.6 Simplified switched-current Direct Form-II(DFII) decimator schematic

5.3.2 FIR-IIR Cascade(FIC) Decimator Architecture

This is the first of the two proposed structures, where the numerator term of (5.10) is realised using an FIR section, which is cascaded with a recursive ladder structure that realises the denominator term. For a decimating factor of M=2, the input has to be sampled twice and the output sampled once. To this end, the FIR part can be polyphase decomposed[6,7] to obtain a structure that contains z^{-2} delay blocks and a two-input commutator as shown in the lower part of Fig. 5.7. The use of a single commutator allows many input transistor gates to be tied together. This minimises distortion due to asymmetric contribution of clock-feedthrough and charge injection by summing of the gate-source capacitances. Furthermore, as the FIR section is a separate network, scaling can easily be performed to make the sum of input capacitances of all polyphase networks equal in value. This causes the charge injection errors to behave approximately as a non-critical offset[7]. The structure of the doubly-terminated ladder is retained to realise the denominator while preserving low passband sensitivity. Thus, the individual branches within the polyphase network and the ladder structure both operate at the lower sampling frequency Fs, which allows more time for the memory cells to settle.



$$\phi = k\frac{1}{1-z^{-2}},\quad \psi = k\frac{z^{-2}}{1-z^{-2}},\quad \mu=(1-z^{-2})$$

Figure 5.7 Signal-flowgraph of FIR-IIR Cascade(FIC) decimator

There is no loss in generality by making the simplifying assumptions $X_6=X_7=X_8=X_9=X_C$, $X_S=X_L$ and $X_5=0$, then, inspection of the SFG in Fig. 5.7 gives

$$V_1 = -\frac{1}{1-z^{-2}}\left[X_S V_1 + X_C V_2 + X(z)V_{in}\right] - X_4 V_3$$
$$V_2 = \frac{1}{1-z^{-2}}\left[z^{-2}X_C V_1 + z^{-2}X_C V_3\right] \qquad (5.13)$$
$$V_3 = -\frac{1}{1-z^{-2}}\left[X_C V_2 + X_L V_3\right]$$

where $X(z)=X_{10}+X_{11}z^{-1}+X_{12}z^{-2}+X_{13}z^{-3}+X_{14}z^{-4}+X_{15}z^{-5}+X_{16}z^{-6}$.

Solving (5.13) for the symbolic transfer function and comparing terms with the numerical transfer function (5.10) results in the set of equations

$$(X_C^2 X_{10}) = a_0 \qquad (5.14a)$$
$$(X_C^2 X_{11}) = a_1 \qquad (5.14b)$$
$$(X_C^2 X_{12}) = a_2 \qquad (5.14c)$$
$$(X_C^2 X_{13}) = a_3 \qquad (5.14d)$$
$$(X_C^2 X_{14}) = a_4 \qquad (5.14e)$$
$$(X_C^2 X_{15}) = a_5 \qquad (5.14f)$$
$$(X_C^2 X_{16}) = a_6 \qquad (5.14g)$$
$$(1+X_S)^2 = b_0 \qquad (5.14h)$$
$$X_S^2+(4-2X_C^2)X_S+3+X_C^2(X_4-2)= -b_2 \qquad (5.14i)$$
$$X_C^2(X_4-2)+2X_S+3=b_4 \qquad (5.14j)$$

Table 5.3 Transistor ratios for the FIC decimator

X_{10}	0.141317	X_4	0.410087
X_{11}	0.371088	X_5	0.0
X_{12}	0.492677	X_6	1.165493
X_{13}	0.527469	X_7	1.165493
X_{14}	0.464653	X_8	1.165493
X_{15}	0.265317	X_9	1.165493
X_{16}	0.065227	X_S	1.163787
		X_L	1.163787

Transistor spread: 17.9

This yields the transistor ratios for the FIC structure in Table 5.3. The simplified schematic of the FIC switched-current decimator implemented using second-generation cells[4] is shown in Fig. 5.8. The bias current sources for each transistor have been omitted to highlight the circuit connections.

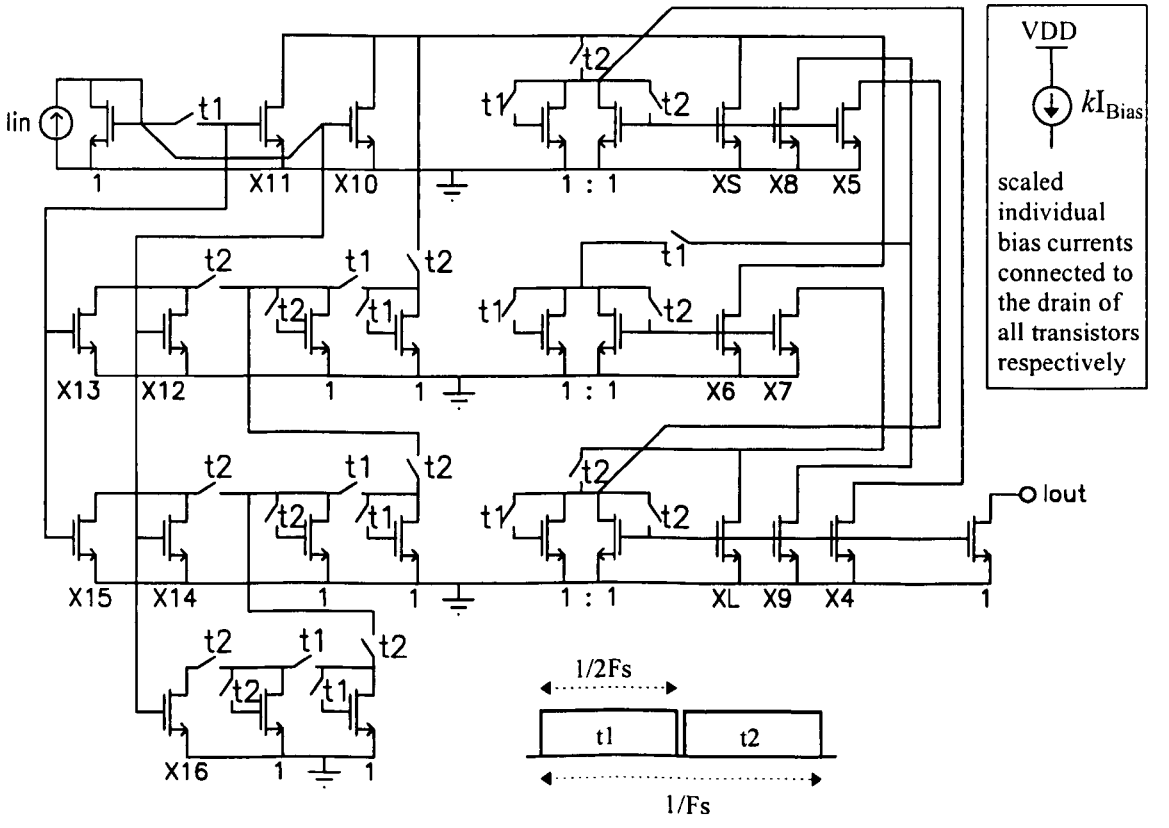
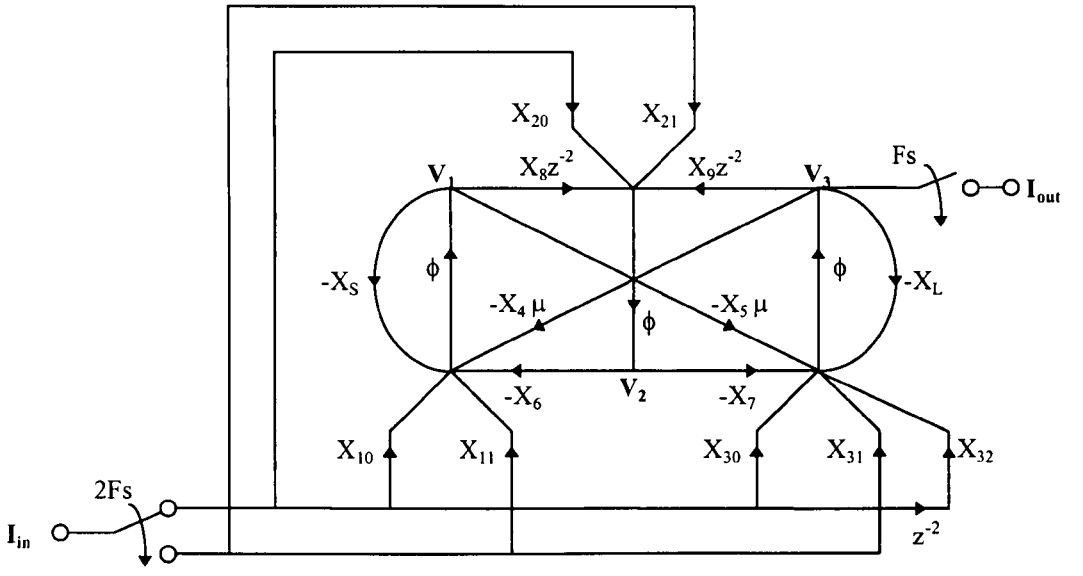


Figure 5.8 Simplified switched-current FIR-IIR Cascade(FIC) decimator schematic and clock waveforms

5.3.3 Multiple Feed-In(MFI) Decimator Architecture

This type of structure, first proposed[9] for an LDI, all-pole switched capacitor decimator, feeds the polyphase-decomposed numerator groups directly to each integrator within the recursive ladder structure as shown by the SFG in Fig. 5.9.



$$\phi = k\frac{1}{1-z^{-2}},\ \mu=(1-z^{-2})$$

Figure 5.9 Signal-flowgraph of the Multiple Feed-In(MFI) decimator

By utilising the delays implicit to the recursive structure, the complexity of each polyphase feed-in group is minimised. This allows the FIR section of the multiple feed-in(MFI) structure to use only one, instead of three delay blocks required in the FIC structure. However, the advantage gained is compromised by higher sensitivity, as will be seen in Section 5.5. The ladder section is identical to that used in the FIC decimator.

With $X_6=X_7=X_8=X_9=X_C$ and $X_S=X_L$, the equations for the SFG in Fig. 5.9 are given as

$$\begin{aligned} V_1 &= -\frac{1}{1-z^{-2}}\left[X_S V_1 + X_C V_2 + X_1(z)V_{in}\right] - X_4 V_3 \\ V_2 &= \frac{1}{1-z^{-2}}\left[z^{-2}X_C V_1 + z^{-2}X_C V_3 + X_2(z)V_{in}\right] \\ V_3 &= -\frac{1}{1-z^{-2}}\left[X_C V_2 + X_L V_3 + X_3(z)V_{in}\right] - X_5 V_1 \end{aligned} \tag{5.15}$$

where $X_1(z)=X_{10}+X_{11}z^{-1}$, $X_2(z)=X_{20}+X_{21}z^{-1}$ and $X_3(z)=X_{30}+X_{31}z^{-1}+X_{32}z^{-2}$.

The branch coefficients of the MFI decimator are determined by mapping the symbolic transfer function to the numerical transfer function in (5.10), as given by

$$(1+X_S)(X_C X_{20}-X_{30})=a_0 \tag{5.16a}$$

$$(1+X_S)(X_C X_{21}-X_{31})=a_1 \tag{5.16b}$$

$$X_C^2(X_{10}-X_{30})-X_C X_{20}+X_S(X_{30}-X_{32})+2X_{30}-X_{32}=a_2 \tag{5.16c}$$

$$X_C^2(X_{11}-X_{31})-X_CX_{21}+X_SX_{31}+2X_{31}=a_3 \quad (5.16d)$$

$$X_C^2X_{32}-X_SX_{32}+X_{30}-2X_{32}=-a_4 \quad (5.16e)$$

$$X_{31}=-a_5 \quad (5.16f)$$

$$X_{32}=-a_6 \quad (5.16g)$$

$$(1+X_S)^2=b_0 \quad (5.16h)$$

$$X_S^2+(4-2X_C^2)X_S+3+X_C^2(X_4-2)=-b_2 \quad (5.16i)$$

$$X_C^2(X_4-2)+2X_S+3=b_4 \quad (5.16j)$$

to yield the set of transistor ratios in Table 5.4. The simplified switched-current realisation of the MFI decimator is shown in Fig. 5.10.

Table 5.4 Transistor ratios for the MFI decimator

X_{10} 0.885935	X_4 0.410087
X_{11} 0.912658	X_5 0.0
X_{20} -0.602681	X_6 1.165493
X_{21} -0.109344	X_7 1.165493
X_{30} -0.791135	X_8 1.165493
X_{31} -0.360399	X_9 1.165493
X_{32} -0.088602	X_S 1.163787
	X_L 1.163787

Transistor spread: 13.2

In the design procedure, the symbolic transfer functions and decimator transistor ratios were solved using the MAPLE symbolic engine in MathCad. The need to derive the symbolic transfer function of the structures imposes an upper limit to the filter order or decimation factor that can be practically designed. This is because the number of symbolic terms increases rapidly with system order and decimation factor. For systems of order or decimation factor greater than six, MathCad failed to converge or yield any solutions. This presents a serious limitation to the design method.

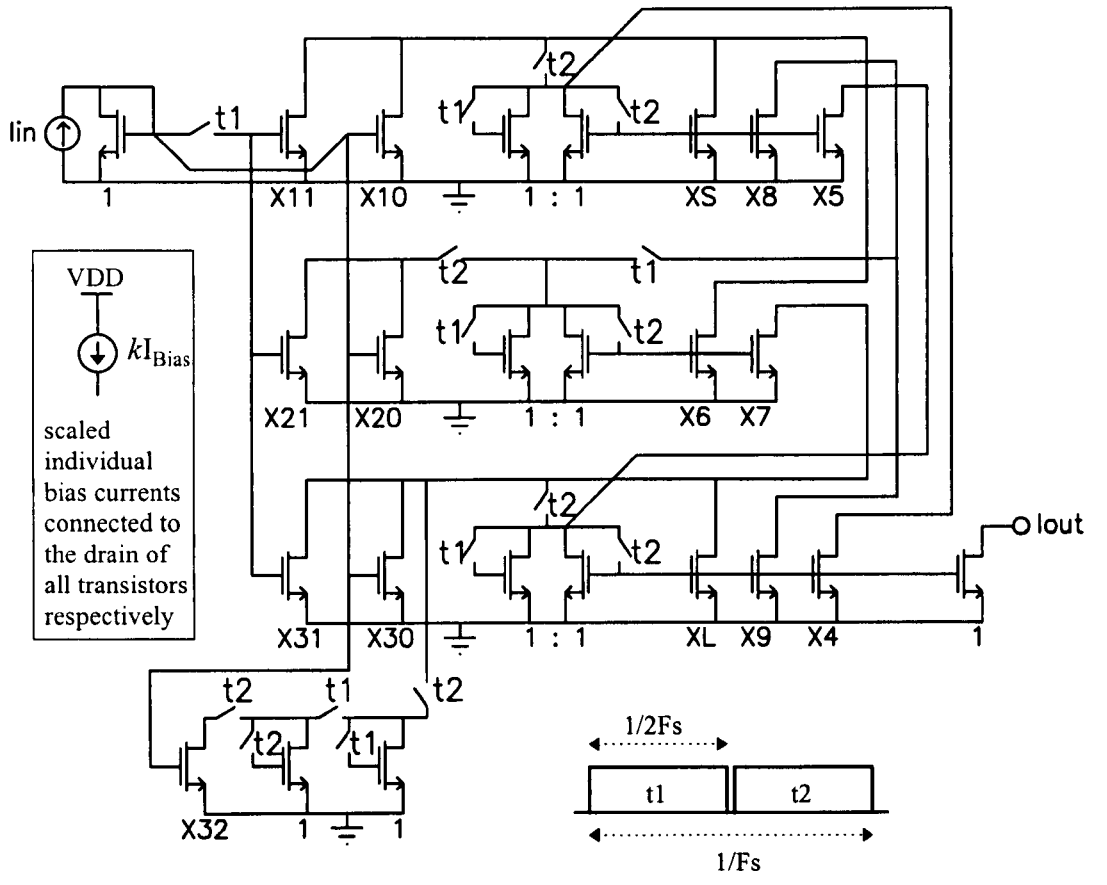


Figure 5.10 Simplified switched-current Multiple Feed-In(MFI) decimator schematic and clock waveforms

5.4 INTERPOLATOR STRUCTURES BY DIRECT TRANSPOSITION

The basic function of an interpolator is to increase the incoming sampling rate from Fs to LFs at the output as illustrated in Fig. 5.11 for sampled and held signals. The frequency domain spectra and responses are shown in Fig. 5.12 for a simple example of L=2. As before, the incoming signal has to be bandlimited to Fs/2. Images will be produced which will repeat at the lower sampling rate of Fs. At the higher output sampling rate of LFs, the images that are spaced further apart will coincide with one of the images at the lower sampling frequency. The task of the prototype filter within the interpolator is to remove the L-1 imaged bands at the output. The images at the output thus repeat at the higher rate of LFs and will be attenuated by the sinc(x) sample-hold effect.

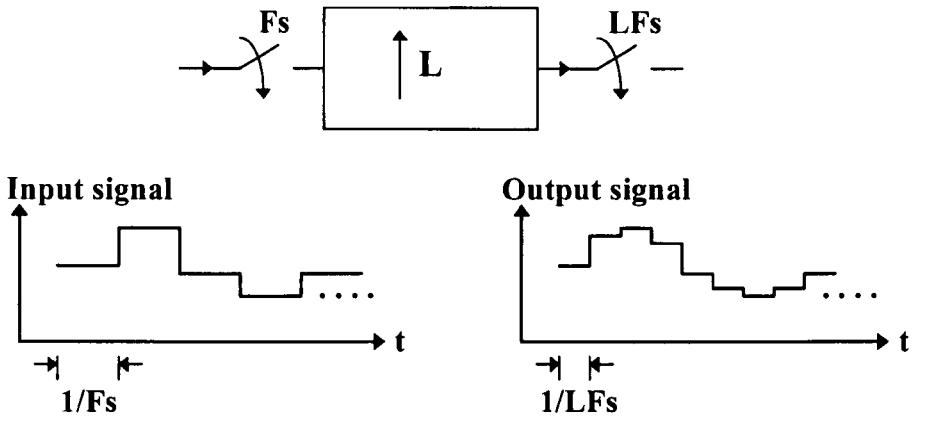


Figure 5.11 Symbolic representation of an interpolator and its time domain input output sampled and held signals

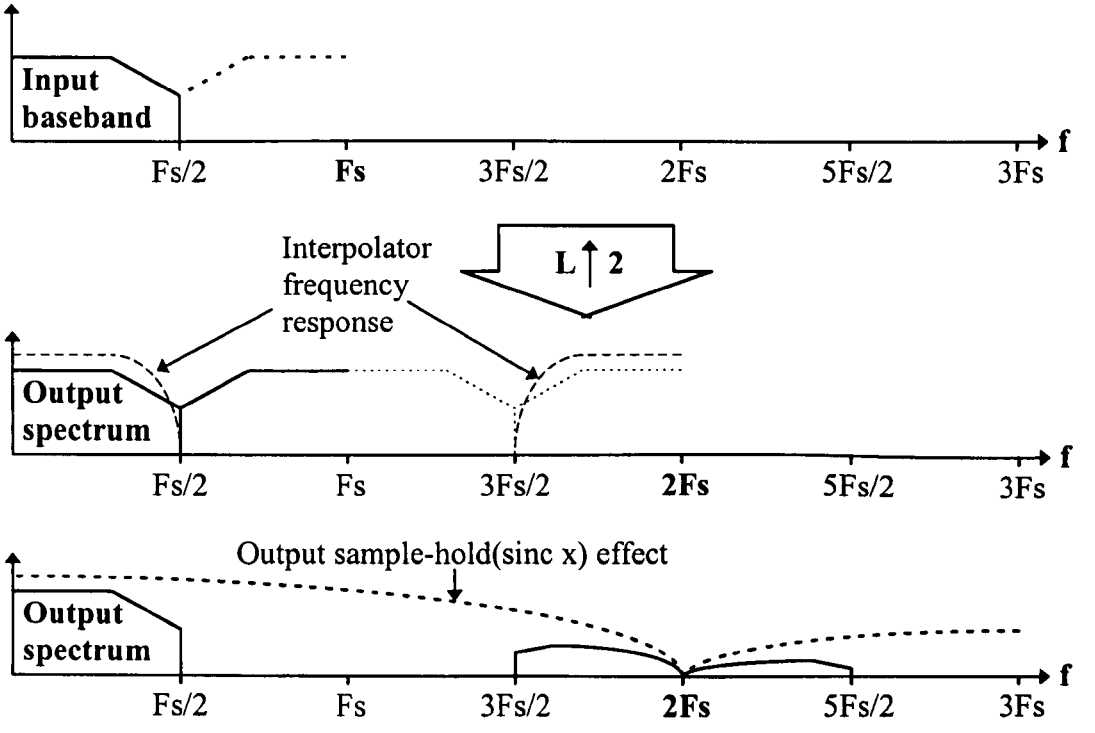


Figure 5.12 Frequency domain representation of interpolation by L=2

In general, any linear time-invariant(LTI) or time-varying(LTV) network has a dual or a complementary network that can be obtained by transposition[1]. In the transposition operation, all LTI branches remain the same except their directions are reversed. Thus, input summing points become output branching points and vice-versa. In addition, the input and output roles of the network are interchanged. A decimator is then transposed to become an interpolator with the same compression and expansion ratio, that is L=M. It follows then that equation (5.8) can be written with transposed components as

$$\left[\mathbf{I}^T - \left\{(\mathbf{A}^{-1}\mathbf{B})^M\right\}^T z^{-M}\right]\mathbf{V}(z) = \mathbf{D}^T V_{in}(z) \tag{5.17}$$

and equation (5.6) can be written as

$$V_{out}(z) = \mathbf{X}(z)^T \mathbf{V}(z) \tag{5.18}$$

Notice that the positions of the input matrix $\mathbf{X}(z)$ and output matrix $\mathbf{D}$ have been interchanged as required and now, $\mathbf{V}(z)=[V_3(z)\ V_2(z)\ V_1(z)]^T$. Substituting equation (5.17) into (5.18) yields the interpolator transfer function

$$\frac{V_{out}(z)}{V_{in}(z)} = \mathbf{X}(z)^T\left[\mathbf{I} - \left\{(\mathbf{A}^{-1}\mathbf{B})^M\right\}^T z^{-M}\right]^{-1}\mathbf{D}^T \tag{5.19}$$

Comparing this with the decimator transfer function in (5.9), it can be seen that apart from having transposed matrices, the order of multiplication has been reversed.

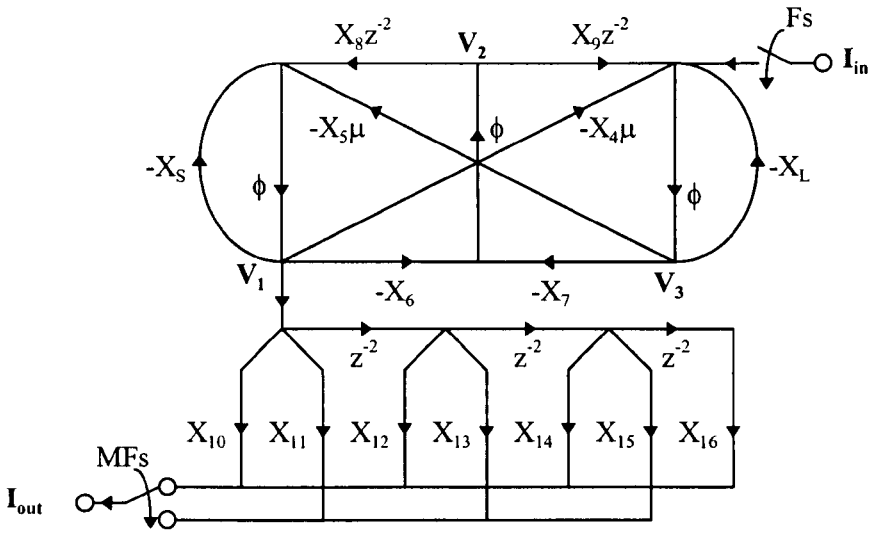
For the case of the IIR-FIR Cascade(IFC) interpolator, the output equation is given by

$$\begin{aligned} V_{out}(z) &= \mathbf{X}(z)^T\mathbf{V}(z) \\ &= [0\ \ 0\ \ X(z)]\mathbf{V}(z) \\ &= (X_{10}+X_{11}z^{-1}+X_{12}z^{-2}+X_{13}z^{-3}+X_{14}z^{-4}+X_{15}z^{-5}+X_{16}z^{-6})V_1(z) \end{aligned} \tag{5.20a}$$

For the case of the Multiple Feed-Out(MFO) interpolator, the output equation is given by

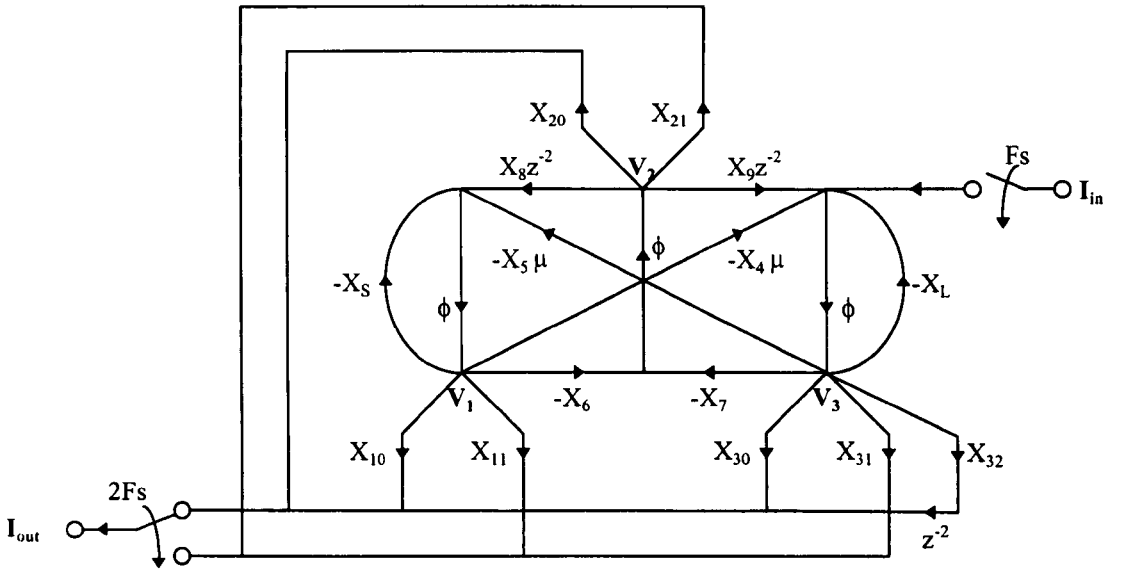
$$\begin{aligned} V_{out}(z) &= \mathbf{X}(z)^T\mathbf{V}(z) \\ &= [\mathbf{X}_3(z)\ \ \mathbf{X}_2(z)\ \ \mathbf{X}_1(z)]\mathbf{V}(z) \\ &= (X_{10}+X_{11}z^{-1})V_1(z) + (X_{20}+X_{21}z^{-1})V_2(z) + (X_{30}+X_{31}z^{-1}+X_{32}z^{-2})V_3(z) \end{aligned} \tag{5.20b}$$

The SFGs for the IFC and MFO interpolators are shown in Figs. 5.13 and 5.14 respectively. The first and last integrator will now have to perform Forward Euler, Backward Euler integration as well as accommodate feedthrough signals.



$$\phi = k\frac{1}{1-z^{-2}},\ \mu=(1-z^{-2})$$

Figure 5.13 Signal flowgraph of IIR-FIR Cascade(IFC) interpolator



$$\phi = k\frac{1}{1-z^{-2}},\ \mu=(1-z^{-2})$$

Figure 5.14 Signal flowgraph of Multiple Feed-Out(MFO) interpolator

Since only the direction of the branches has to be reversed, the same coefficients in Table 5.3 and 5.4 relating to the decimators can be used for the interpolators. This greatly simplifies the task of deriving the complementary interpolators and avoids the need for

tedious redesign from scratch. Similarly, the transposed SFG of the DFII[6] interpolator is shown in Fig. 5.15.

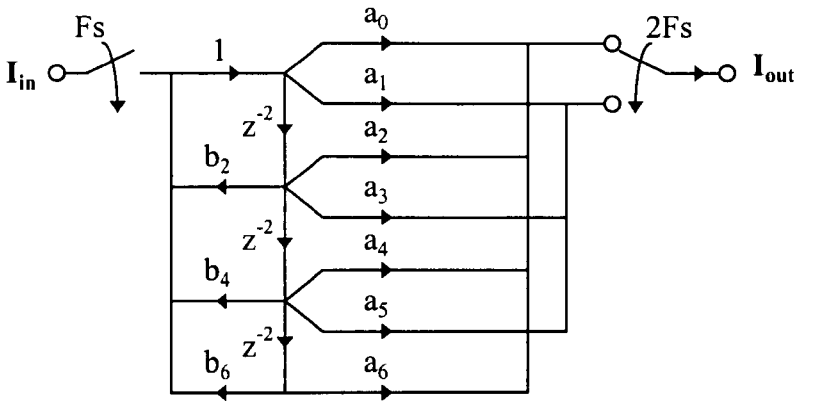


Figure 5.15 Signal-flowgraph of the Direct Form-II(DFII) interpolator

The simplified schematic for the switched-current interpolators are shown in Figs. 5.16, 5.17 and 5.18. The input to the interpolators has to be sampled and held. The simulated ideal frequency responses of both the decimators and interpolators are plotted in Fig. 5.19, and are identical to that of the reference filter.

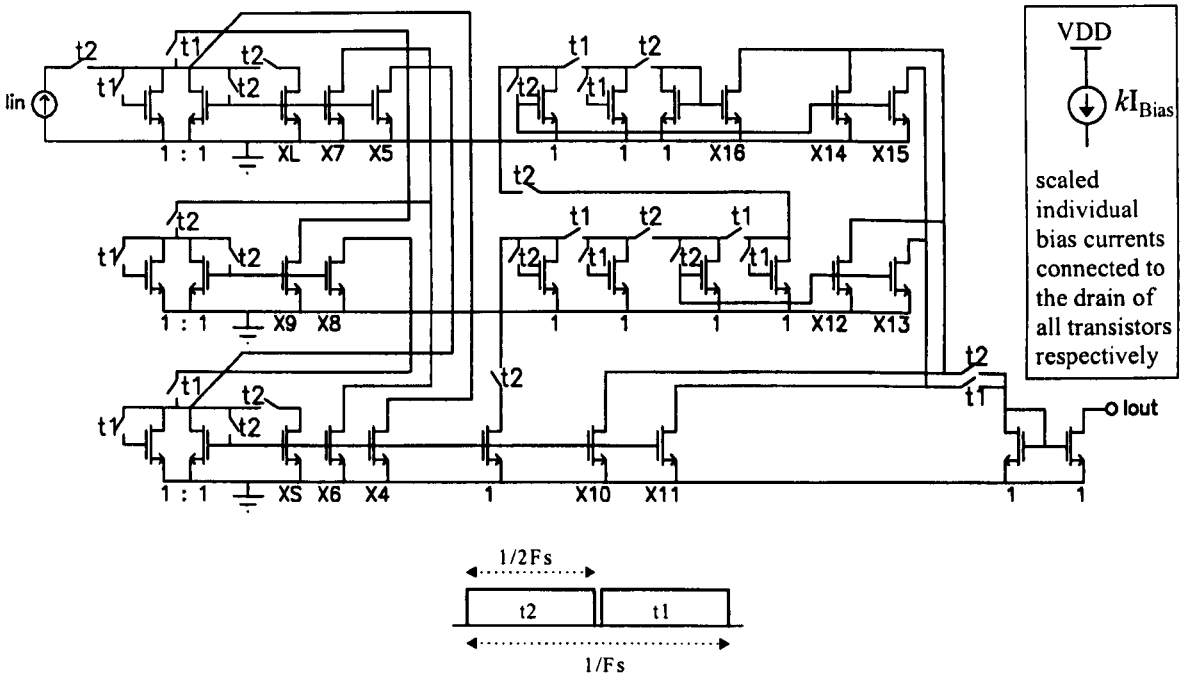


Figure 5.16 Simplified switched-current IIR-FIR Cascade(IFC) interpolator schematic and clock waveforms

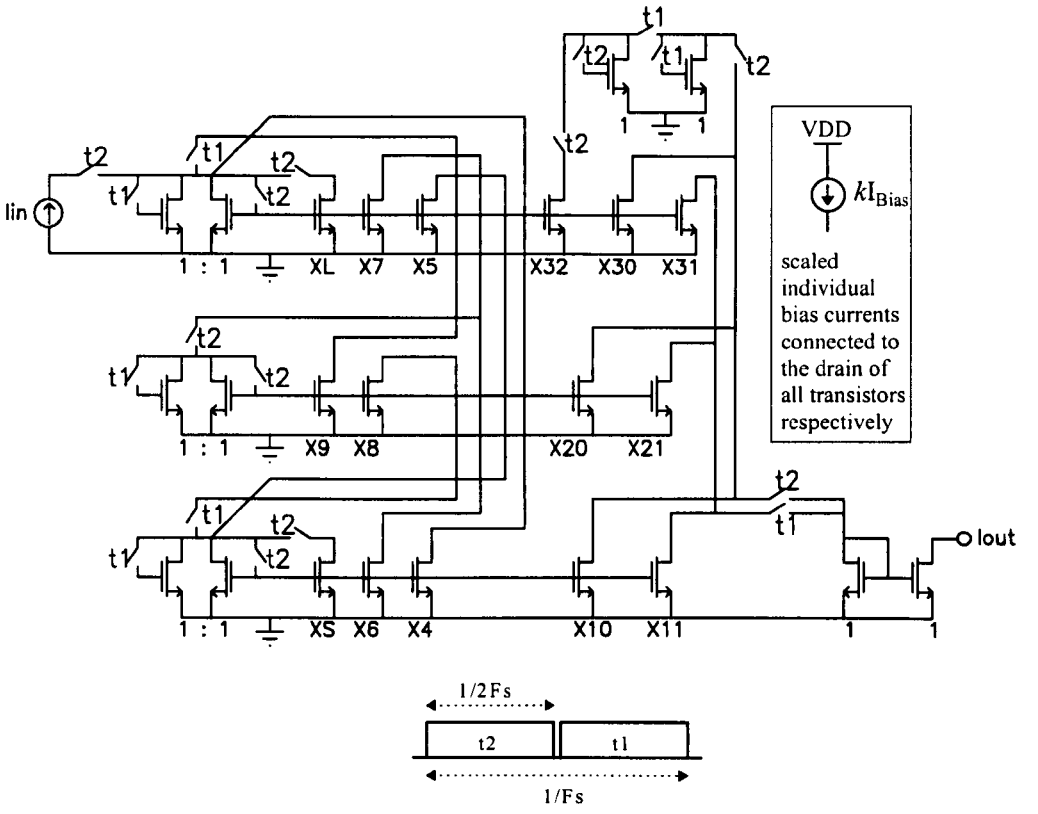


Figure 5.17 Simplified switched-current Multiple Feed-Out(MFO) interpolator schematic and clock waveforms

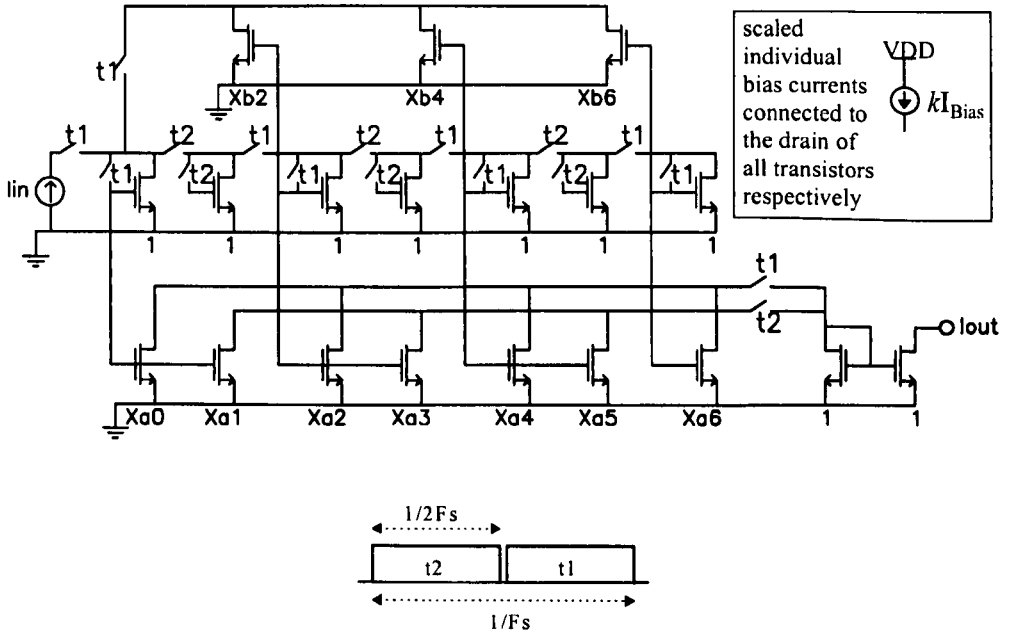


Figure 5.18 Simplified switched-current Direct Form-II(DFII) interpolator schematic and clock waveforms

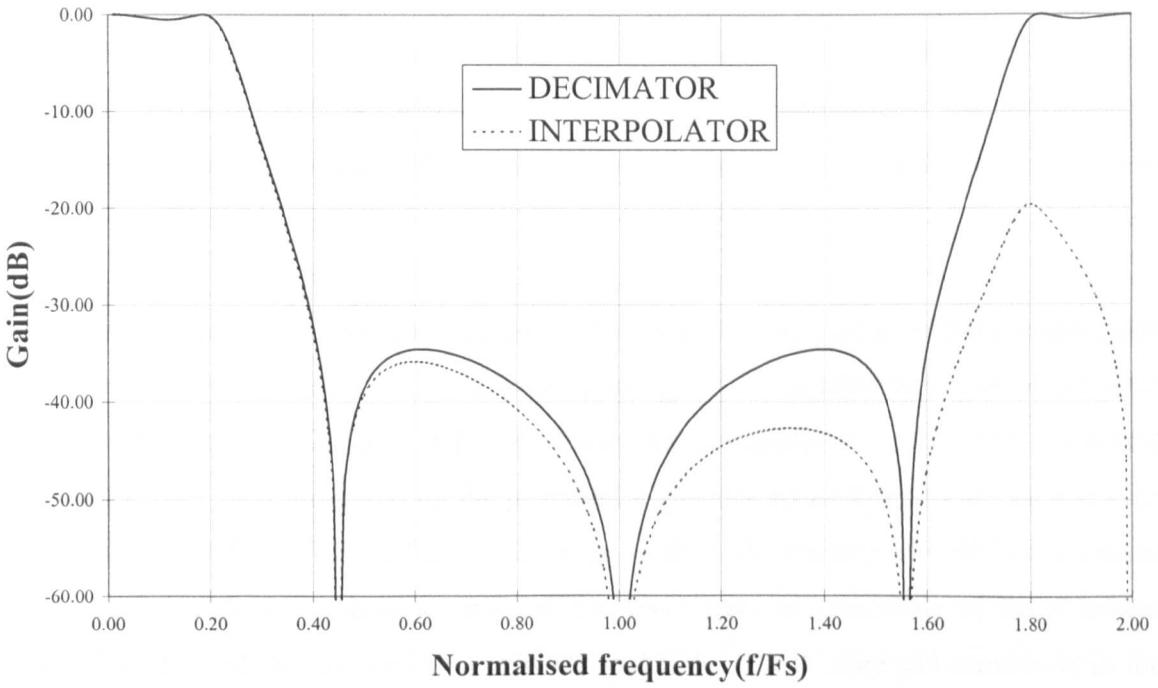


Figure 5.19 Simulated amplitude responses of the decimators and interpolators

Though the examples given here are simple, it is straight-forward to extend to higher decimation or interpolation rates. However, the significant sin(x)/x attenuation in the passband will require some form of compensation. Further, the responses are not just limited to elliptic ones. Unconventional responses such as quasi-elliptic, obtained by passive prototype manipulation[8], can also be accommodated.

5.5 CIRCUIT SENSITIVITIES AND IMPLEMENTATION ISSUES

5.5.1 Sensitivities

The decimator circuits just described, are based on simulating the multirate-transformed transfer function of a doubly-terminated ladder network. Therefore, if properly designed, the characteristic low sensitivity in the passband response should be inherited.

In the transformation process, the replicated poles centered around Fs are cancelled by the additional zeros introduced into the numerator of the transfer function as can be seen from (5.8a). The multirate transfer function is thus nominally equal to that of the prototype filter. Therefore, high sensitivity is expected from elements that contribute to the formation of these zeros, as any deviation from their nominal values will result in only partial cancellation of the poles.

The magnitude response sensitivities of the SI decimators to deviations in transconductance coefficients, computed using (3.15), are plotted in Figs. 5.20 together with that of the filter and a Direct Form-II(DFII)[6] IIR decimator for comparison. The low passband sensitivities have been preserved by the proposed decimator structures and are indeed even lower than that of the reference filter. The huge peak in the vicinity of 0.45f/Fs is caused by the elliptic notch, while those around 0.8f/Fs result from the sensitivity of the pole-zero cancellation in the stopband. Unlike a conventional filter, a high stopband sensitivity in the decimator can result in poor stopband attenuation and aliasing leaking through due to partial cancellation of the poles.

For the FIC decimator, contributions to the passband sensitivity by the FIR elements are small, as this section is responsible principally for the formation of zeros. Their main contribution is to the stopband sensitivity, where the zeros cancel the poles. Conversely, poles are formed by the recursive ladder structure and are mainly clustered in the passband region. This distinct contribution of sensitivity by the FIR and IIR sections to the stopband and passband respectively happens as both sections are separate and cascaded in the FIC decimator. This can be seen from (5.14a)~(5.14g), where only branches X8 and X7, which lie in the forward path of the recursive ladder, appear in the numerator of the transfer function as X_C^2. This minimises contribution to sensitivity due to interaction between elements of both sections.

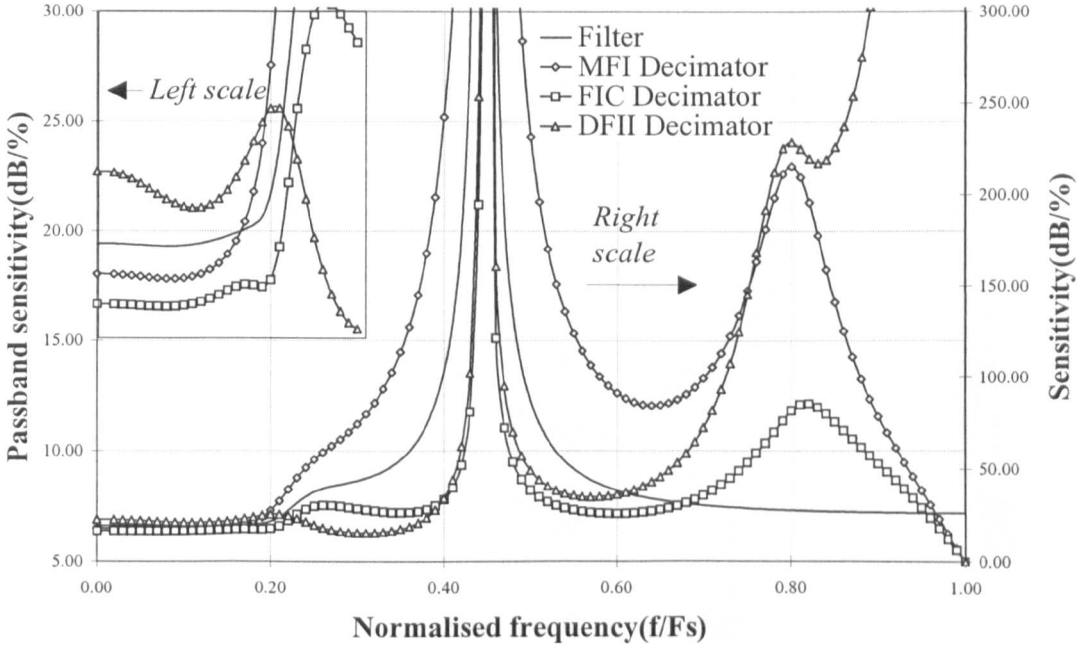


Figure 5.20 Sum-sensitivities of decimators with respect to all transconductance elements

With the MFI structure, different groups of polyphase branches feed directly to each integrator within the ladder network. This closer degree of coupling between the FIR and IIR sections results in more terms within the recursive ladder appearing in the numerator as seen from (5.16a)~(5.16g). Therefore, a significant increase in stopband sensitivities is observed in Fig. 5.20 for the MFI decimator as expected. Both passband and stopband sensitivities are relatively higher for the DFII decimator[6]. The frequency responses resulting from a ±1% deviation in all coefficients are plotted in Figs. 5.21a and 5.21b. The DFII and MFI decimators exhibit the greatest amount of response deviation in the passband and stopband respectively while the FIC decimator is minimally affected for both regions.

The sensitivity performance of the interpolators are shown in Fig. 5.22. Low passband sensitivities are preserved but are marginally higher. The stopband sensitivities are significantly worse than those for the decimators. Sensitivity is topology dependent, and the increased sensitivities of the interpolators are therefore caused by the altered topologies resulting from the direct transposition process.

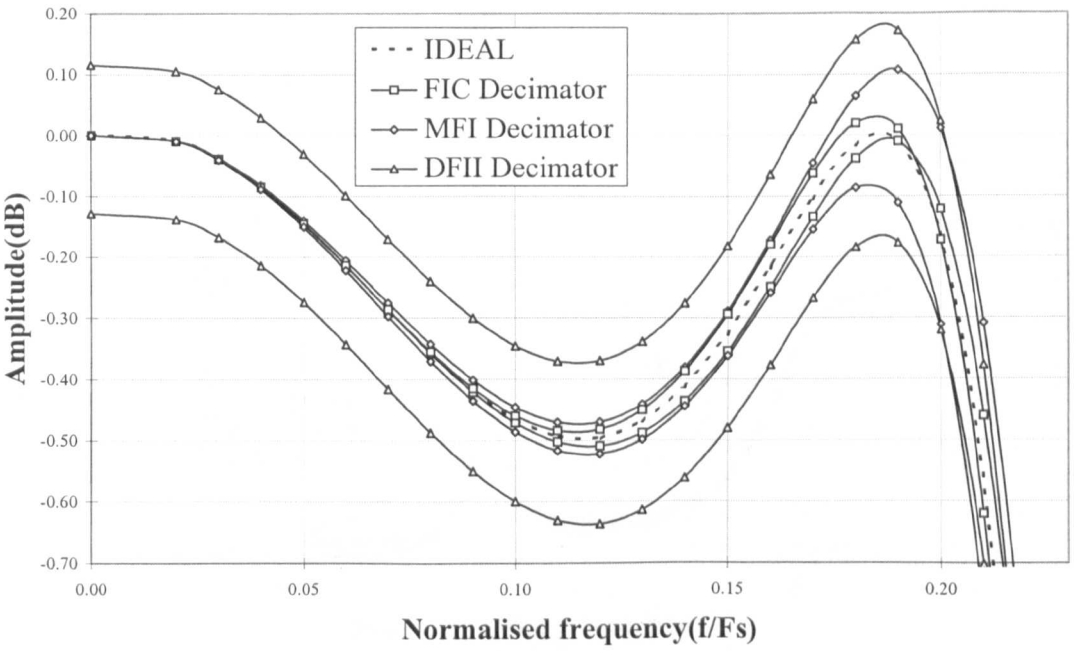


Figure 5.21a Effect of ±1% deviation in all transconductance on the passband of the decimators

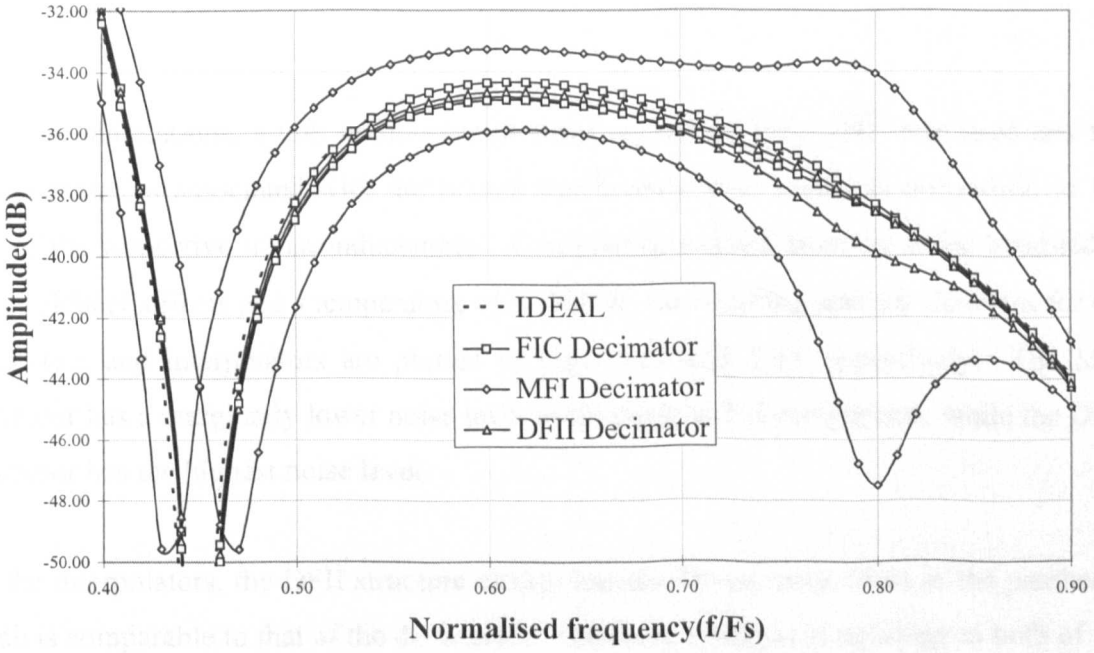


Figure 5.21b Effect of ±1% deviation in all transconductance on the stopband of the decimators

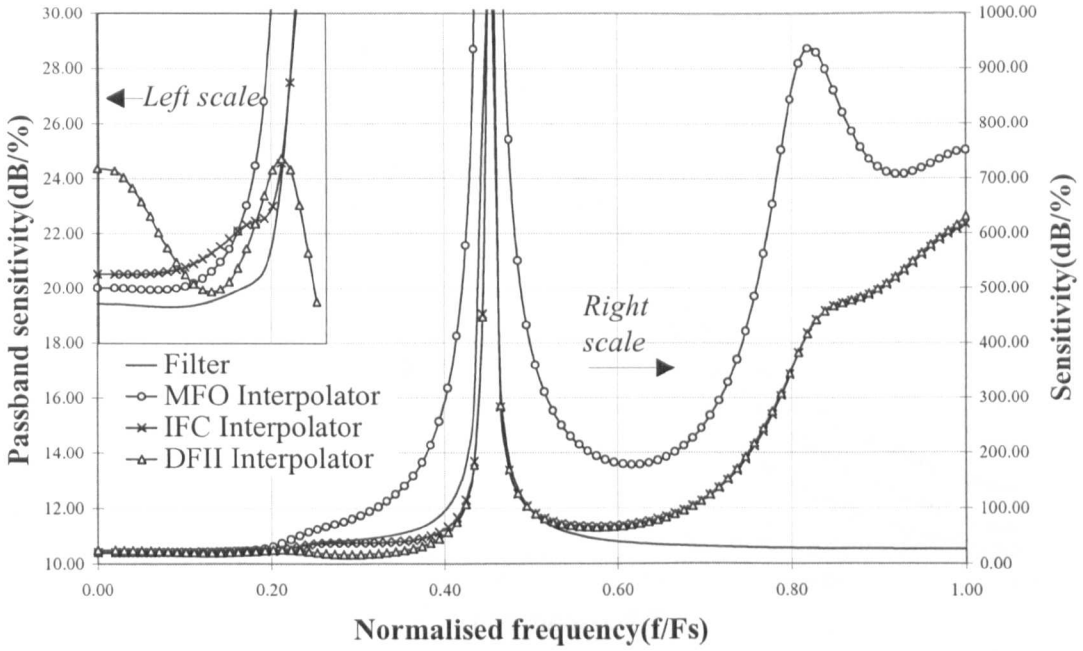


Figure 5.22 Sum-sensitivities of interpolators with respect to all transconductance elements

5.5.2 Noise

For noise simulations, a unit drain-referred noise current of $1\text{nA}/\sqrt{\text{Hz}}$ was used and the noise generators associated with the branch coefficients were scaled in proportion to the root of the respective transconductances. Considering a fixed arbitrary noise bandwidth, noise foldback effects and a temperature of T=300°K, the resulting spectral densities for the decimators and interpolators are plotted in Figs. 5.23 and 5.24 respectively. The MFI decimator has a marginally lower noise level in the passband in comparison, while the DFII decimator has the highest noise level.

For the interpolators, the DFII structure clearly has the lowest noise level in the passband, which is comparable to that of the decimators. However, changes in topology to both of the IFC and MFO interpolators resulting from the direct transposition process also changes the internal noise transfer functions to the respective outputs. This results in higher noise levels for the IFC and MFO interpolators since noise is folded back at the same higher output frequency of 2Fs for all the interpolators.

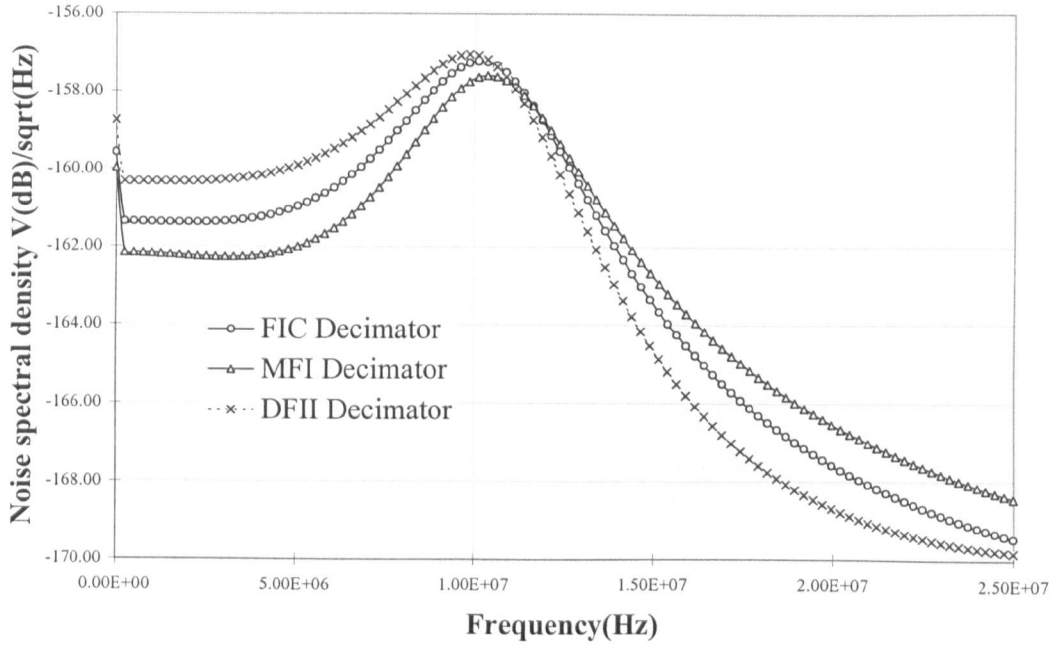


Figure 5.23 Simulated decimator noise spectral densities with 10-band foldback effects, T=300°K and a unit drain-referred noise current of 1nA/$\sqrt{\text{Hz}}$

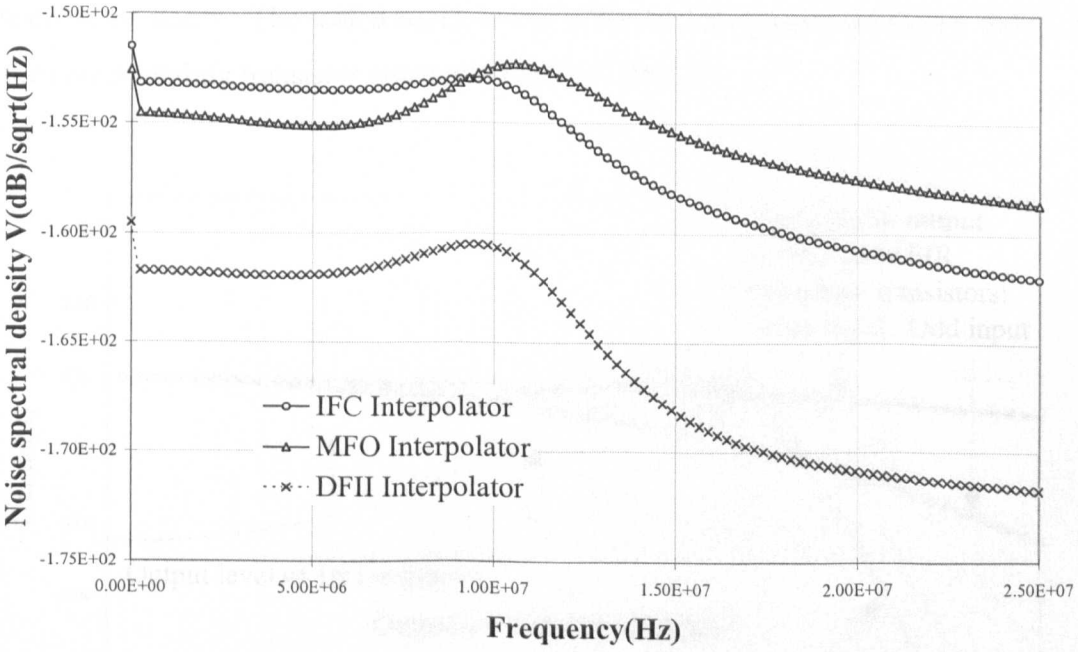


Figure 5.24 Simulated interpolator noise spectral densities with 10-band foldback effects, T=300°K and a unit drain-referred noise current of 1nA/$\sqrt{\text{Hz}}$

Table 5.5 Dynamic range scaled transistor ratios of the FIC decimator

X_{10}	0.141317	X_4	0.410087
X_{11}	0.371088	X_5	0.0
X_{12}	0.492677	X_6	1.958000
X_{13}	0.527469	X_7	1.958000
X_{14}	0.464653	X_8	0.693750
X_{15}	0.265317	X_9	0.693750
X_{16}	0.065227	X_S	1.163787
		X_L	1.163787

Transistor spread: 30

5.5.3 Implementation Issues

To give a more realistic assessment of circuit implementation, an M=2 FIC decimator and an L=2 IFC interpolator were simulated in HSPICE using real process models. Dynamic range scaling[16] was performed to equalise the peak signal modulation of the bias currents in the different stages. The scaled signal levels of the FIC decimator are shown in Fig. 5.25 and the corresponding transistor ratios are listed in Table 5.5.

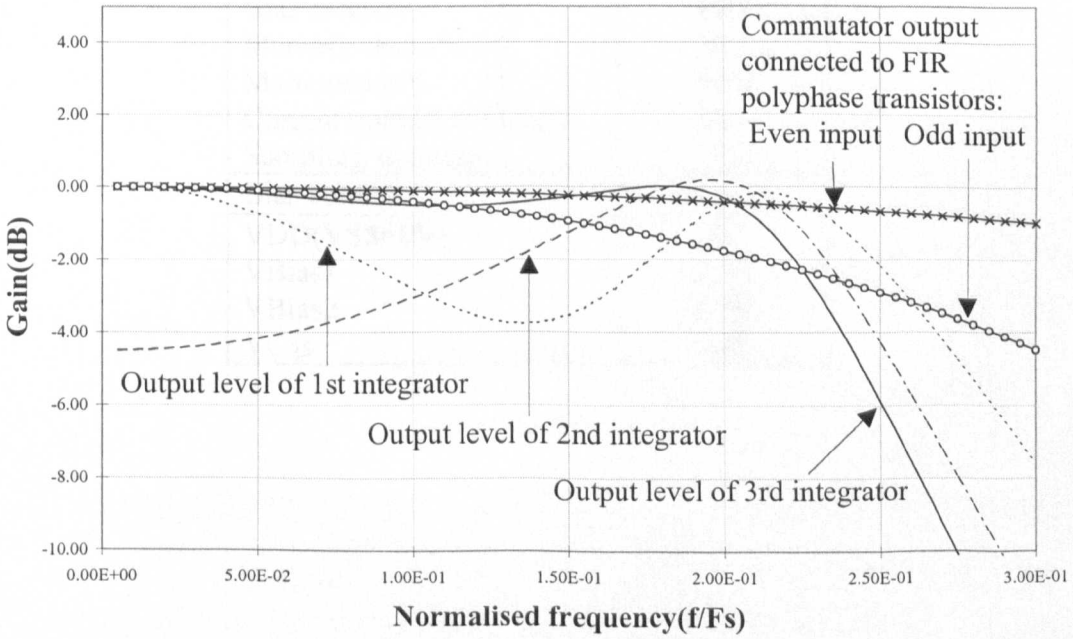


Figure 5.25 Dynamic range scaled signal levels of the FIC(M=2) decimator

The delay circuit that is fed by FIR transistors X12~X16(Fig. 5.8) has to be doubled in size to sink the summed currents. The memory cells were designed using models from an AMI double-metal 1.0μm digital CMOS process, and employ the S^2I[12] technique with cascodes and dummy switches added to reduce the output conductance and charge-injection respectively. The unit memory cell and associated clock waveforms are shown in Fig. 5.26 while its specifications are listed in Table 5.6. As the S^2I cell delivers the corrected current only in its output phase, care has to be taken to ensure direct feedthrough connections are minimised by rearranging the connections or by introducing a half-delay with a memory cell. Finally, settle scaling[15] of the transistors was performed to ensure the gate area of the loaded integrator outputs remained unchanged. Fig. 5.27 shows the HSPICE and SCNAP4[11] simulated frequency responses of the FIC decimator and IFC interpolator. The respective output responses to a sampled-and-held 100kHz sinusoidal input signal at 50% modulation of the bias current are shown in Figs. 5.28 and 5.29. The decimating and interpolating actions are clearly evident.

Table 5.6 Specifications of the SI memory cell

Transistors	(W/L) in μm
Bias current, M_J	42/2
Bias cascode, M_{JC}	80/1
Memory cascode, M_C	30/1
Main memory, M_1	50/4
Current transfer switches	20/1
Sampling switches	3/1
Bias current	100μA
VDD(VSS=0V)	3V
VBias1	1.5V
VBias2	1.2V
VCas	1.8V

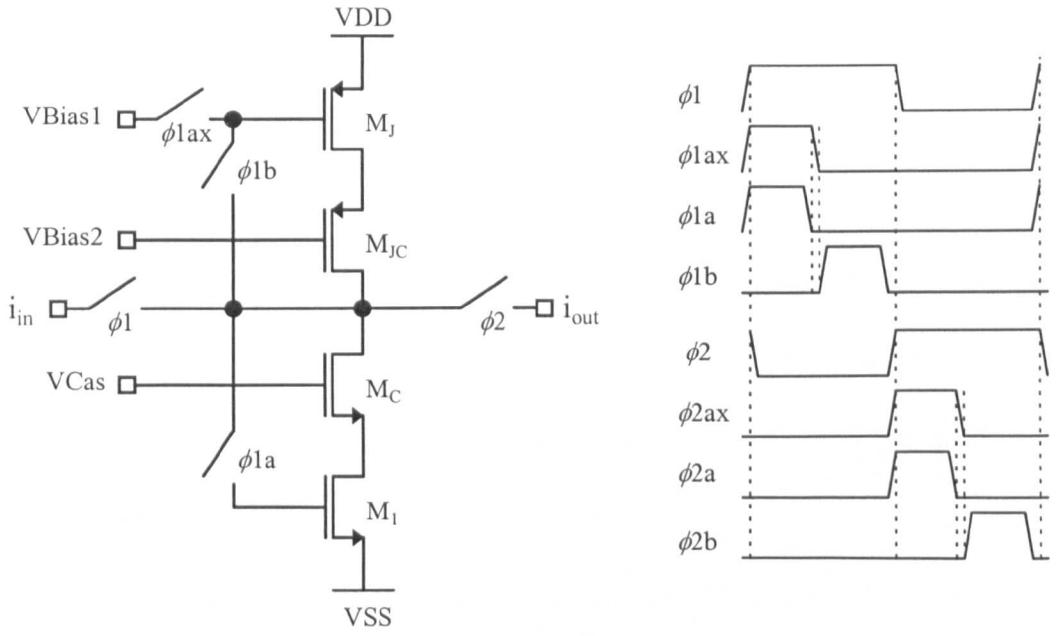


Figure 5.26 Cascoded S^2I memory cell and clock waveforms

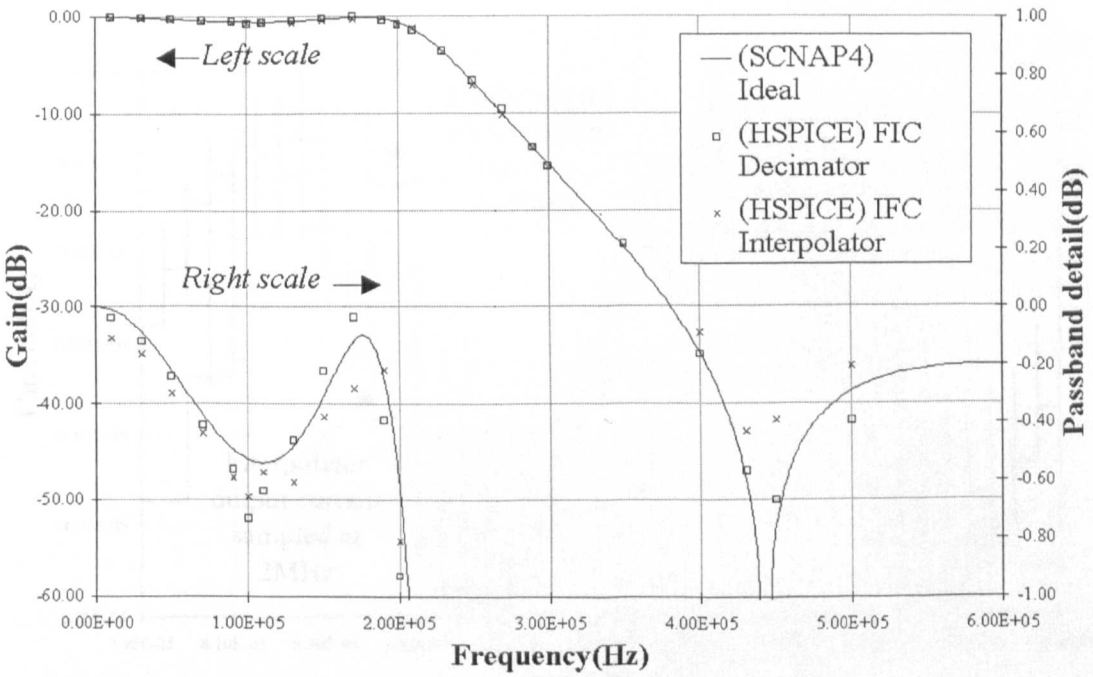


Figure 5.27 SCNAP4 and HSPICE simulated frequency response of the M=L=2 FIC decimator and IFC interpolator

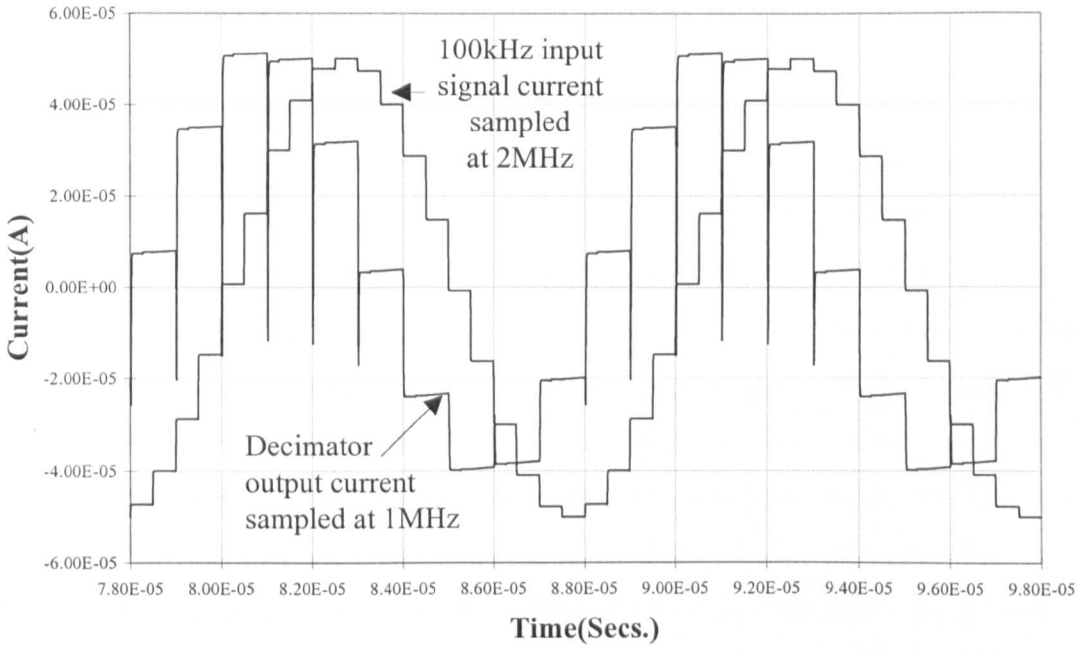


Figure 5.28 HSPICE simulated decimator output responses(M=2) for a 100kHz sampled-and-held input sinusoidal signal

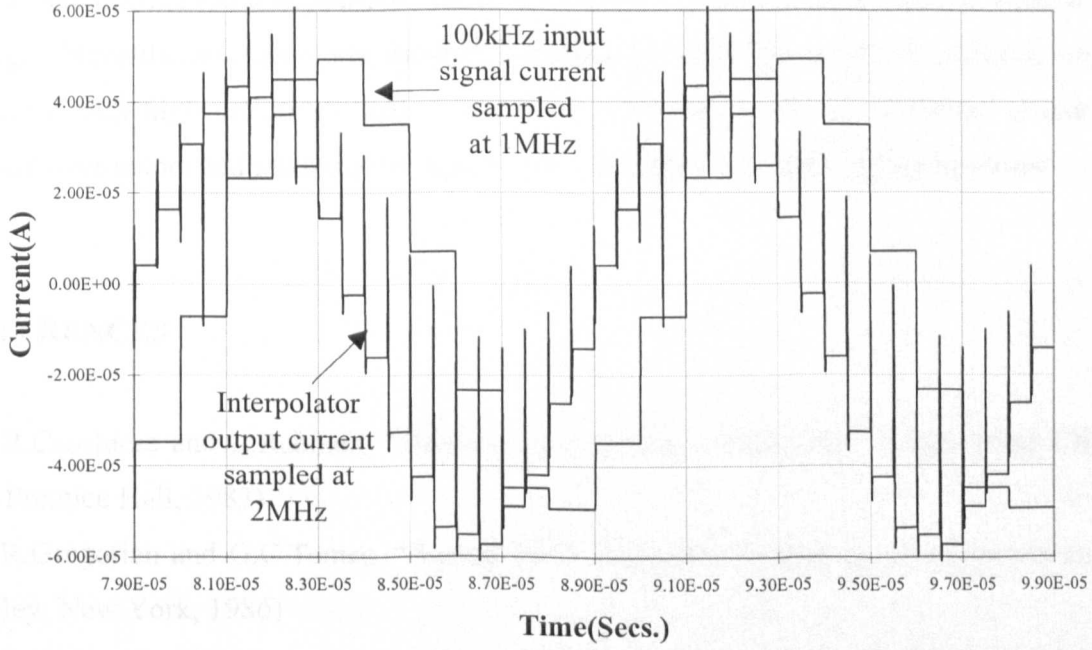


Figure 5.29 HSPICE simulated interpolator output responses(L=2) for a 100kHz sampled-and-held input sinusoidal signal

5.6 CONCLUSIONS

Bilinear-transformed, elliptic switched-current decimators and interpolators based on a combination of polyphase networks and low sensitivity ladder structures have been demonstrated with an M=L=2 fold reduction/increase in sampling rate. Settling time for the memory cells is maximised by the use of polyphase FIR networks, which together with the prototype filter, operate at the lower sampling rate. Of the two types of proposed structures, the FIR-IIR Cascade(FIC) type requires more delay terms, but is simpler and possesses superior sensitivity characteristics. The Multiple-Feed-In(MFI) type requires less delay terms, but suffers from poorer sensitivity characteristics. However, both exhibit passband sensitivities that are lower than that of the basic filter. The direct transposition method avoids redesign to obtain the interpolator structures, which share similar sensitivity characteristics, apart from the stopband region. Noise performance of the decimators are comparable. In comparison, the IFC and MFO interpolator structures obtained by direct transposition resulted in marginally higher noise levels. One serious drawback of this state-space multirate transform design method is the need to derive the symbolic transfer function of the structures. The rapid increase in the number of symbolic terms with filter order and decimation/interpolation factor effectively imposes a limit on the achievable design. Nevertheless, this is mitigated by the other favourable attributes mentioned, which together with high selectivity and exactness of response, make the proposed switched-current decimators and interpolators suitable for high frequency filtering applications.

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CHAPTER 6:
N-PATH AND PSEUDO-N-PATH CELLS FOR SWITCHED-CURRENT SIGNAL PROCESSING

6.1 INTRODUCTION

The concept of N-path[1] filtering was originally proposed for continuous time bandpass applications, and was subsequently extended to digital and switched-capacitor(SC) filters[2]. It is most commonly employed to derive narrowband bandpass filters[3], which might otherwise not be practical due to high component spreads and sensitivity. More importantly, the centre frequency of a discrete time N-path filter is centered at a multiple of the clock frequency, which provides the necessary frequency stability crucial to narrowband bandpass filtering. However, various problems plaguing the traditional N-path filter, such as path mismatches, mirror frequency noise and clock- feedthrough noise[3] have prompted the development of alternative methods.

The pseudo-N-path concept was proposed by Fettweis and Wupper[4] to overcome the problem of path mismatch. Instead of having N distinct paths, only one common path exists through which all signals traverse. Each memory-possessing element has to be supplemented by a circulating delay line which shifts the different states such that an N-path filter is realised. Circulating-delay and other variants[3, 5, 6, 7] of pseudo-N-path SC filters have already been in existence for some time.

N-path filters can be designed using either a lowpass or a highpass reference filter. Fig. 6.1 shows the amplitude response of N-path filters which use a lowpass prototype to achieve a $z \rightarrow z^N$ transformation. Generally, the Nyquist range is extended from Fs/2 to NFs/2. Each path filter has to be clocked at Fs in a time-interleaved manner to achieve an effective sampling rate of NFs. For pseudo-N-path filters, the clock rate has to be NFs, as there is only a common signal path through which all paths are processed. It is clear from Fig. 6.1 that to utilise the passband centered at Fs, a minimum of N=3 paths are required. Further disadvantages include the need for bandpass anti-aliasing(AAF) and anti-imaging filters(AIF) due to the undesired passband at DC, and the presence of clock-feedthrough noise in the passband for N-path type realisations.

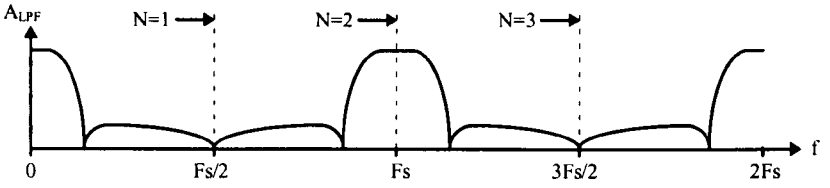


Figure 6.1 Nyquist range of N-path filter with lowpass prototype response

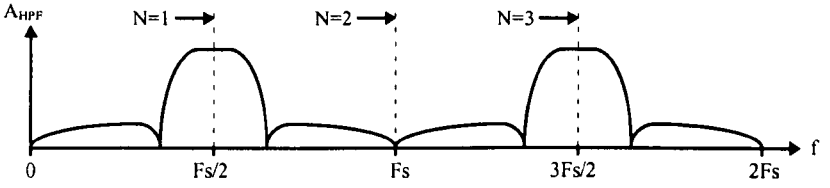


Figure 6.2 Nyquist range of N-path filter with highpass prototype response

In comparison, the use of highpass prototype filters with the $z \rightarrow z^N$ transformation has the response shown in Fig. 6.2. Only N=2 paths are required to utilise the passband centered at Fs/2. Simple lowpass AAFs and AIFs can now be used instead of bandpass ones. More importantly, the desired passbands are centered at odd multiples of Fs/2, which avoid clock-feedthrough noise. To obtain the type of response in Fig. 6.2 using only lowpass filters, the $z \rightarrow -z^N$ transformation can be used[7], which features in the cells proposed here.

Very few papers, if any, have to date been published in the area of N-path or pseudo-N-path SI circuits. In this chapter, novel SI N-path and pseudo-N-path cells based on the Forward Euler, Backward Euler and bilinear integrators are proposed. A z-domain lowpass reference filter can be transformed into a bandpass one by simply replacing the original integrators with the corresponding proposed cells. The fully-balanced integrators perform the $z \rightarrow -z$(lowpass to highpass) transformation and the $z \rightarrow -z^2$ (lowpass to bandpass) transformation, which is based on the circulating-delay principle. The effects of non-idealities such as finite conductance ratio, settling, clock feedthrough/charge-injection and noise on the pseudo-N-path integrators are analysed in detail. Using these cells, the procedures for designing ladder filters from a z-domain lowpass reference filter are illustrated with an N-path and a pseudo-N-path 6th order narrowband bandpass ladder filter.

Simulated results of amplitude response sensitivity and other non-ideal factors affecting the pseudo-N-path and N-path-filters are presented in the remaining part of this chapter. These include finite output conductance, charge-injection, mirror-frequencies rejection and noise.

6.2 SWITCHED-CURRENT N-PATH AND PSEUDO-N-PATH CELLS

The z-domain transfer functions and corresponding pole-zero diagrams for the Forward Euler, Backward Euler and Bilinear integrators are shown in Table 6.1 together with the results of $z \rightarrow -z$ and $z \rightarrow -z^2$ transformation. The cells are realised in fully-differential form to exploit the availability of inverted signals, in addition to the usual advantages[8]. The SI realisation of these cells is considered next by deriving their transfer-functions using a small-signal approach.

6.2.1 Switched-Current $z \rightarrow -z$ Transform Integrators

A. Forward Euler Integrator

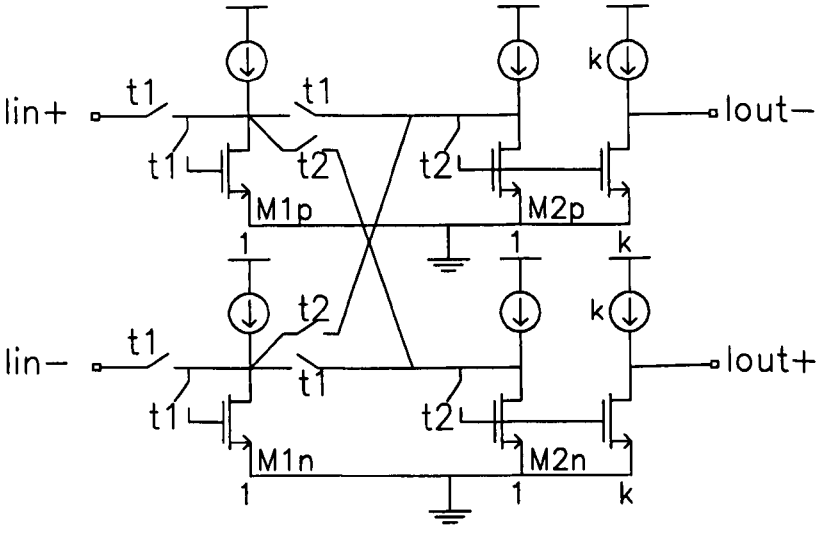


Figure 6.3 Switched-current $z \rightarrow -z$ transformation Forward Euler integrator

The small-signal operation can be described using the positive half of the circuit beginning in phase t1 of period (n-1) as follows:

t1(n-1)

$$i_{M1p}(n-1) = i_{in}^{+}(n-1) - i_{M2p}(n-1) \quad (6.1a)$$

$$i_{out}^{-}(n-1) = -i_{M2p}(n-1) \quad (6.1b)$$

t2(n)

$$i_{M2p}(n) = i_{M1p}(n) \quad (6.1c)$$

$$i_{out}^{-}(n) = -i_{M2p}(n) \quad (6.1d)$$

Substituting memorised current $i_{M1p}(n) = i_{M1p}(n-1)$ and (6.1d), (6.1b) into (6.1c) gives

$$-i_{out}^{-}(n) = i_{in}^{+}(n-1) + i_{out}^{-}(n-1) \quad (6.1e)$$

Taking z-transforms and rearranging yields the transfer function

$$H_{FE}(z) = k\frac{-z^{-1}}{1+z^{-1}} \quad (6.1f)$$

where k=1 will be assumed throughout.

B. Backward Euler Integrator

The z→ -z transform Backward Euler integrator can be obtained with the same cross-coupled, differential feedback structure as it shares a common denominator term. However, the inputs are sampled by memory cells M2p and M2n in phase t2 instead as shown in Fig. 6.4.

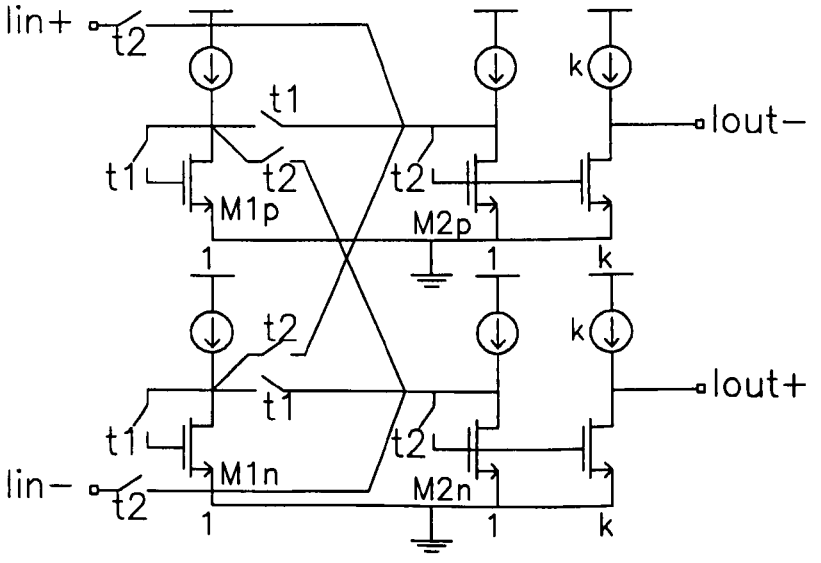


Figure 6.4 Switched-current z→ -z transformation Backward Euler integrator

The circuit operation is described as follows:

t1(n-1)

$$i_{M1p}(n-1) = -i_{M2p}(n-1) \quad (6.2a)$$

$$i_{out}^{-}(n-1) = -i_{M2p}(n-1) \quad (6.2b)$$

t2(n)

$$i_{M2p}(n) = i_{in}^{+}(n)+i_{M1p}(n) \quad (6.2c)$$

$$i_{out}^{-}(n) = -i_{M2p}(n) \quad (6.2d)$$

Substituting memorised current $i_{M1p}(n) = i_{M1p}(n-1)$ and (6.2d), (6.2b) into (6.2c) gives

$$-i_{out}^{-}(n) = i_{in}^{+}(n)+ i_{out}^{-}(n-1) \quad (6.2e)$$

Taking z-transforms and rearranging yields the transfer function

$$H_{BE}(z)= -k\frac{1}{1+z^{-1}} \quad (6.2f)$$

C. Bilinear Integrator

The bilinear integrator can be formed from the same basic structure and is shown in Fig. 6.5. Due to a numerator term of $(1-z^{-1})$, the input will have to be sampled on both phases. A full period sample-and-hold is therefore required at the input.

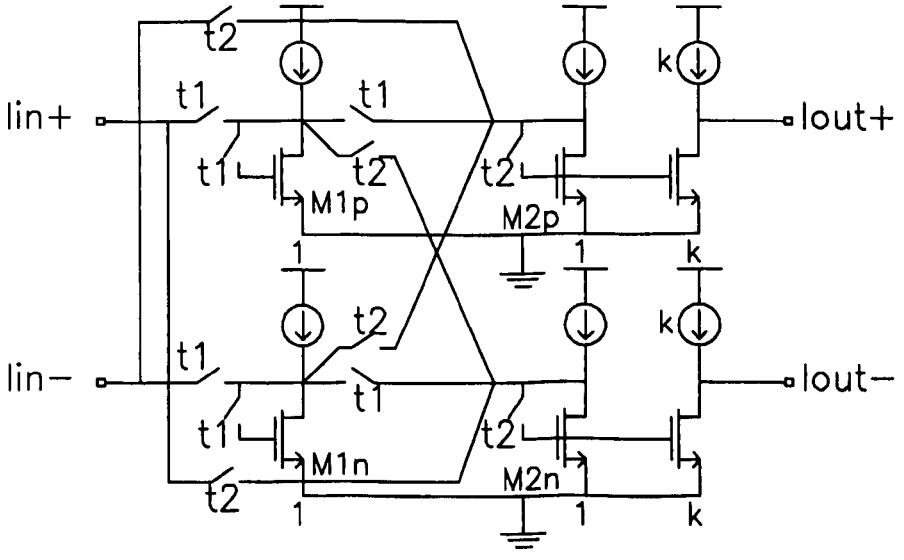


Figure 6.5 Switched-current z→ -z transformation Bilinear integrator

The circuit operation is described as follows:

t1(n-1)

$$i_{M1p}(n-1) = i_{in}^{+}(n-1) - i_{M2p}(n-1) \tag{6.3a}$$

$$i_{out}^{+}(n-1) = -i_{M2p}(n-1) \tag{6.3b}$$

t2(n)

$$i_{M2p}(n) = i_{in}^{-}(n) + i_{M1p}(n) \tag{6.3c}$$

$$i_{out}^{+}(n) = -i_{M2p}(n) \tag{6.3d}$$

Substituting memorised current $i_{M1p}(n) = i_{M1p}(n-1)$, $i_{in}^{-}(n) = -i_{in}^{+}(n)$ and (6.3d), (6.3b) into (6.3c) gives

$$-i_{out}^{+}(n) = -i_{in}^{+}(n) + i_{in}^{+}(n-1) + i_{out}^{+}(n-1) \tag{6.3e}$$

Taking z-transforms and rearranging yields the transfer function

$$H_{BI}(z) = k\frac{1 - z^{-1}}{1 + z^{-1}} \tag{6.3f}$$

To verify the correct operation of these circuits, computer simulation was performed using the switched network simulator SCNAP4[9]. The resulting amplitude responses are shown in Fig. 6.6 and correspond exactly with responses expected from the respective pole-zero diagrams in row two of Table 6.1.

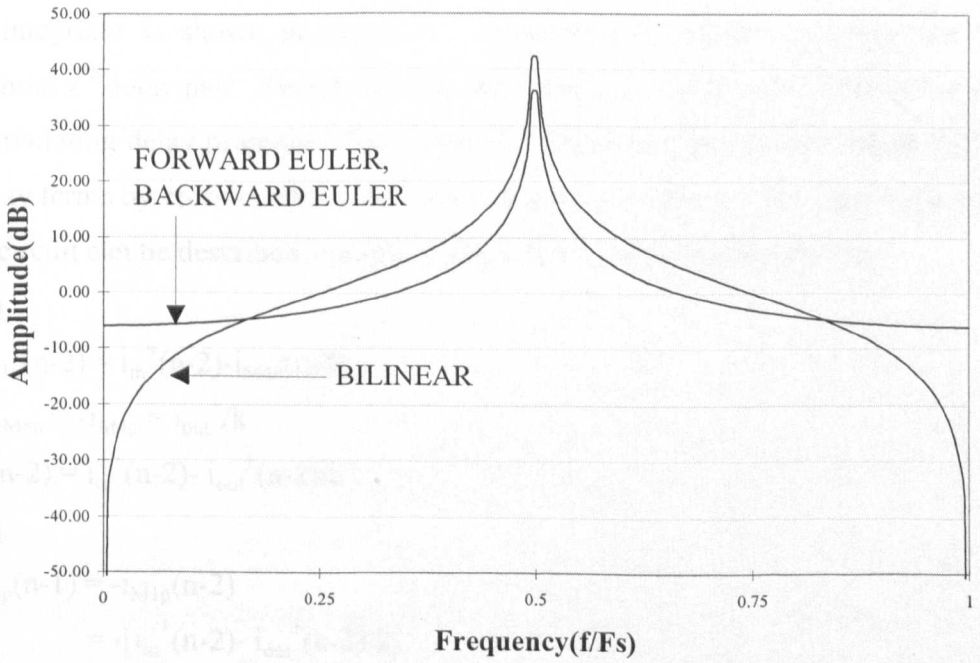


Figure 6.6 Simulated amplitude responses of the z→ -z transformation integrators

6.2.2 Switched-Current Pseudo-2-Path $z \rightarrow -z^2$ Transform Integrators

A. Forward Euler Integrator

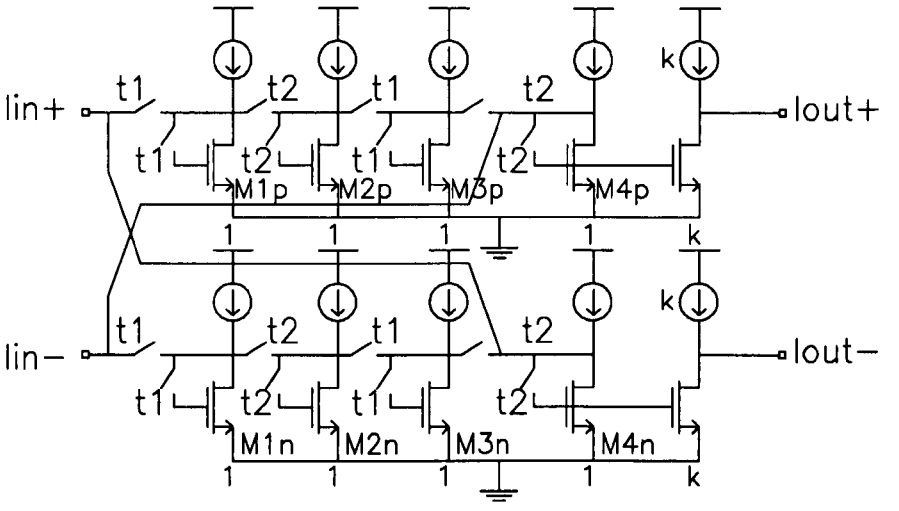


Figure 6.7 Pseudo-2-path switched-current $z \rightarrow -z^2$ transformation Forward Euler integrator

The simplified schematic of the fully-differential $z \rightarrow -z^2$ transform, pseudo-2-path Forward Euler integrator is shown in Fig. 6.7. Transistors M1p-M4p and M1n-M4n form a differential z^{-2} delay pair. Two delay cells are required in each path to satisfy the pseudo-2-path circulating delay principle. The integrating loops can be formed with sign reversal of the delay terms by cross-coupling the feedback loops as shown. The small signal operation of the circuit can be described starting at phase t1 of period (n-2) as follows:

t1(n-2)

$$i_{M1p}(n-2) = i_{in}^{+}(n-2) - i_{M4n}(n-2) \tag{6.4a}$$

Since $i_{M4n} = -i_{M4p} = i_{out}^{+}/k$

$$i_{M1p}(n-2) = i_{in}^{+}(n-2) - i_{out}^{+}(n-2)/k \tag{6.4b}$$

t2(n-1)

$$i_{M2p}(n-1) = -i_{M1p}(n-2)$$

$$= -[i_{in}^{+}(n-2) - i_{out}^{+}(n-2)/k] \tag{6.4c}$$

t1(n-1)

$$i_{M3p}(n-1) = -i_{M2p}(n-1)$$

$$= i_{in}^{+}(n-2) - i_{out}^{+}(n-2)/k \tag{6.4d}$$

t2(n)

$$i_{M4p}(n) = -i_{M3p}(n-1)$$
$$= -i_{in}^{+}(n-2)+i_{out}^{+}(n-2)/k \quad (6.4e)$$

Substituting $i_{M4p} = -i_{out}^{+}/k$ and some rearranging gives

$$i_{out}^{+}(n)+ i_{out}^{+}(n-2) = ki_{in}^{+}(n-2) \quad (6.4f)$$

Taking z-transforms yields

$$i_{out}^{+}(z)(1+z^{-2}) = ki_{in}^{+}(z)z^{-2} \quad (6.4g)$$

From (6.4g), the transfer function is given as

$$H_{FE}(z)=k\frac{z^{-2}}{1+z^{-2}} \quad (6.4h)$$

B. Backward Euler Integrator

The Backward Euler integrator is shown in Fig. 6.8. The inputs are sampled at memory cells M1p and M1n in phase t2 to established a direct path between the input and output as required for Backward Euler integration. The cross-coupling reverses the sign of the loop delay. The circuit operation is described as follows:

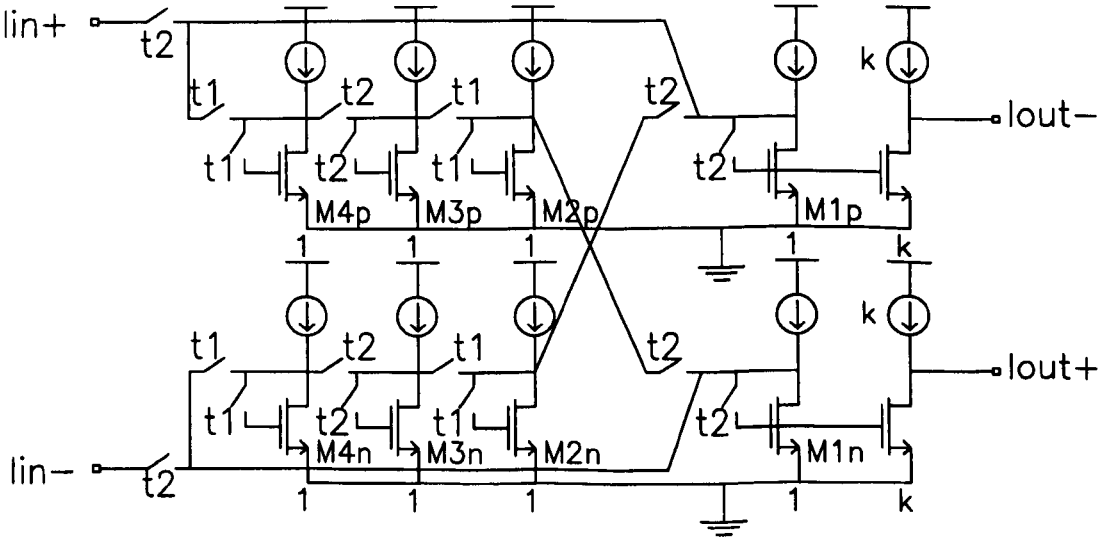


Figure 6.8 Pseudo-2-path switched-current $z\rightarrow -z^2$ transformation Backward Euler integrator

t1(n-2)

$$i_{M4p}(n-2) = -i_{M1p}(n-2) \tag{6.5a}$$

Since $i_{M1p} = -i_{out}^{-}/k$

$$i_{M4p}(n-2) = i_{out}^{-}(n-2)/k \tag{6.5b}$$

t2(n-1)

$$i_{M3p}(n-1) = -i_{M4p}(n-2)$$
$$= -i_{out}^{-}(n-2)/k \tag{6.5c}$$

t1(n-1)

$$i_{M2p}(n-1) = -i_{M3p}(n-1)$$
$$= i_{out}^{-}(n-2)/k \tag{6.5d}$$

t2(n)

$$i_{M1n}(n) = -i_{M2p}(n-1)+i_{in}^{-}(n)$$
$$= -i_{out}^{-}(n-2)/k+i_{in}^{-}(n) \tag{6.5e}$$

Substituting $i_{M1n} = -i_{out}^{+}/k = i_{out}^{-}/k$ and rearranging gives

$$i_{out}^{+}(n)+ i_{out}^{+}(n-2) = -ki_{in}^{-}(n) \tag{6.5f}$$

Taking z-transforms yields

$$i_{out}^{+}(z)(1+z^{-2}) = -ki_{in}^{-}(z) \tag{6.5g}$$

From (6.5g), the transfer function is given as

$$H_{BE}(z)= -k\frac{1}{1+z^{-2}} \tag{6.5h}$$

C. Bilinear Integrator

Fig. 6.9 show the schematic of the bilinear integrator. A full period sample-and-hold is required at the input as it samples on both phases. Note that the cross-coupled connection reverses the sign of the loop-delay while feedback is now to the middle of the delay line. This section can be used to realise bilinear-integrator based ladder filters. Similarly, the operation of the circuit can be described starting from the positive input as follows:

t1 (n-2)

$$i_{M1p}(n-2) = i_{in}^{+}(n-2) \tag{6.6a}$$

t2(n-2)

$$i_{M6p}(n-2) = -i_{out}^{+}(n-2)/k \tag{6.6b}$$

$$i_{M2p}(n-2) = -i_{M1p}(n-2) \quad (6.6c)$$

t1(n-1)

$$i_{M3p}(n-1) = -i_{M2p}(n-2) - i_{M6p}(n-2) \quad (6.6d)$$

t2(n-1)

$$i_{M4p}(n-1) = -i_{M3p}(n-1) \quad (6.6e)$$

t1(n)

$$i_{M5n}(n) = -i_{M4p}(n-1) \quad (6.6f)$$

t2(n)

$$i_{M6n}(n) = i_{in}^{+}(n) - i_{M5n}(n) \quad (6.6g)$$

Substituting in the previously memorised currents and noting that $i_{M6n}(n) = -i_{out}^{-}(n)/k = i_{out}^{+}(n)/k$ gives

$$i_{out}^{+}(n) + i_{out}^{+}(n-2) = k[i_{in}^{+}(n) - i_{in}^{+}(n-2)] \quad (6.6h)$$

Taking z-transforms and rearranging yields the bilinear transfer function

$$H_{BI}(z) = k\frac{1-z^{-2}}{1+z^{-2}} \quad (6.6i)$$

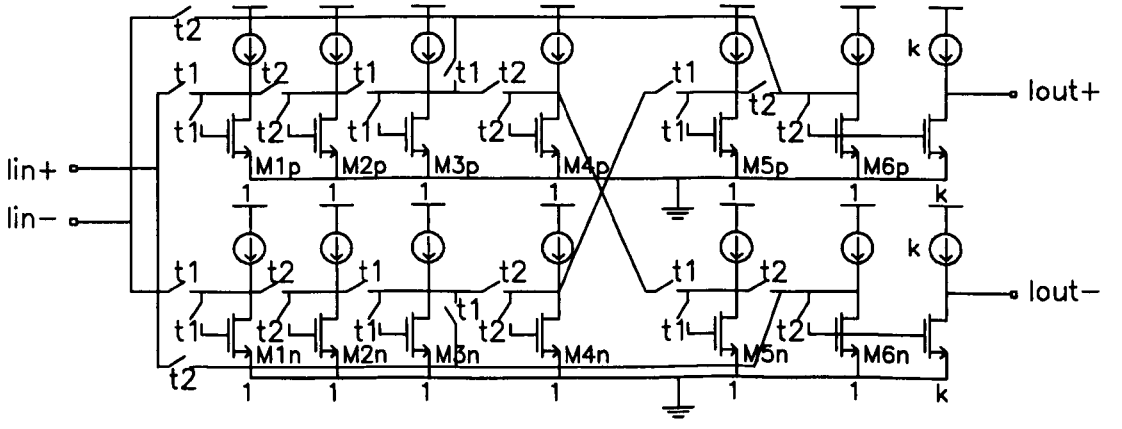


Figure 6.9 Pseudo-2-path switched-current $z \rightarrow -z^2$ transformation Bilinear integrator

D. FIR Section $(1-z^{-2})$

This circuit in Fig. 6.10 is designed to replace the bilinear integrator required at the input of certain $z \rightarrow -z^2$ transformed, bilinear-LDI filters. Cascading the FIR section at the output instead of having a bilinear integrator at the input avoids overloading the filter with the peak in response at Fs/4 while simultaneously realising the bilinear zero at Fs/2. Without

going through details, the circuit operation can be described as follows: The outputs from transistor pair M2p and M2n are fed to delay lines realising two unit delays of $-z^{-2}$. The outputs from M1p and M1n are then cross-connected directly to the output which sums to give the transfer function $H_{FIR}(z) = 1-z^{-2}$.

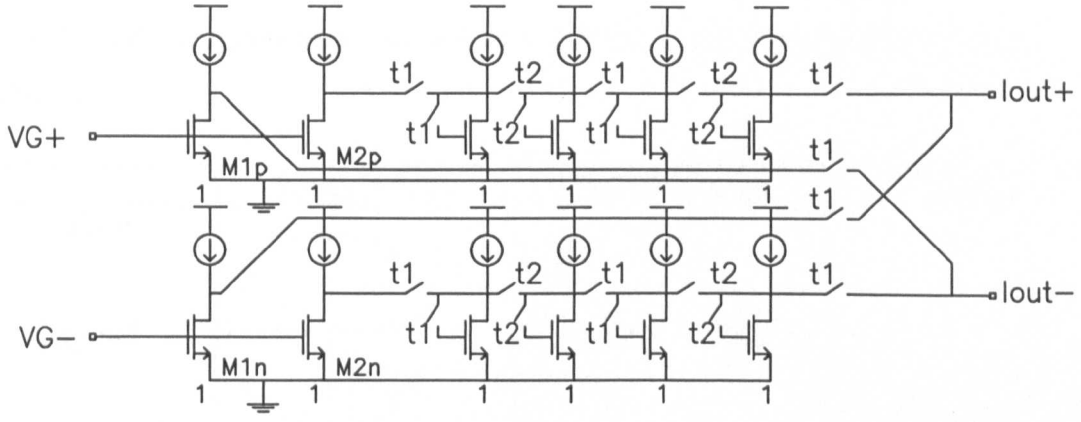


Figure 6.10 FIR output section ($1-z^{-2}$) for realising the bilinear zero

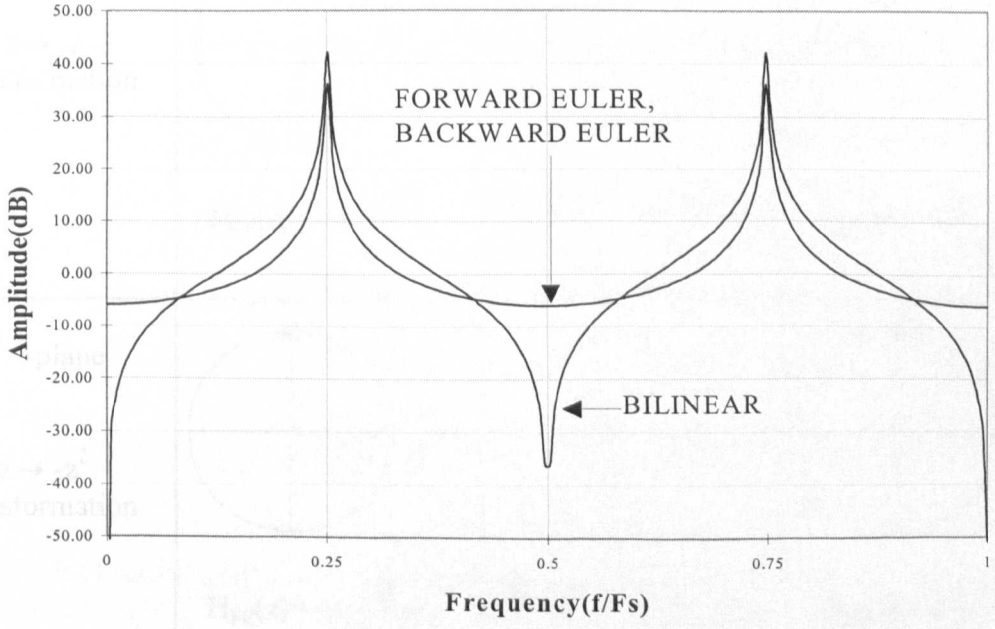
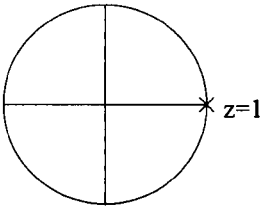
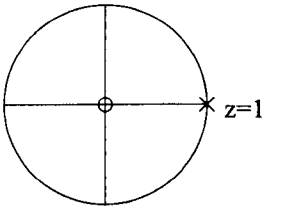
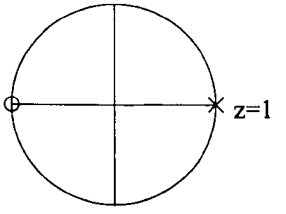
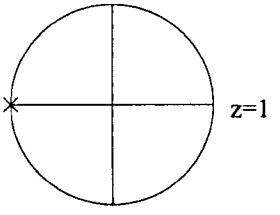
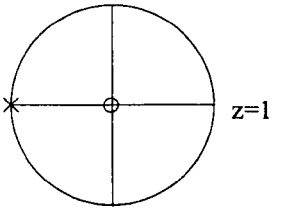
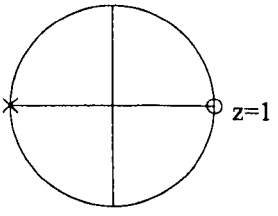
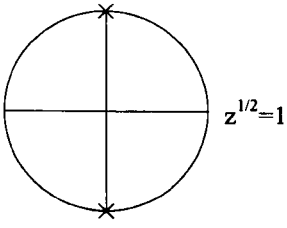
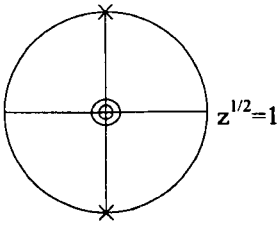
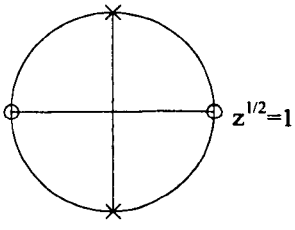


Figure 6.11 Simulated amplitude responses of the $z \rightarrow -z^2$ transformation pseudo-2-path integrators

To verify the correct operation of these circuits, they were simulated and the resulting amplitude responses are shown in Fig. 6.11. These responses correspond as expected to those from the respective pole-zero diagrams in row three of Table 6.1.

Table 6.1 z-domain pole-zero diagrams and transfer functions for the transformed integrators

	Forward Euler	Backward Euler	Bilinear
z-plane Original	 $H_{FE}(z)=k\frac{z^{-1}}{1-z^{-1}}$	 $H_{BE}(z)=-k\frac{1}{1-z^{-1}}$	 $H_{BI}(z)=k\frac{1+z^{-1}}{1-z^{-1}}$
z-plane $z\rightarrow -z$ transformation	 $H_{FE}(z)=-k\frac{z^{-1}}{1+z^{-1}}$	 $H_{BE}(z)=-k\frac{1}{1+z^{-1}}$	 $H_{BI}(z)=k\frac{1-z^{-1}}{1+z^{-1}}$
$z^{1/2}$-plane $z\rightarrow -z^2$ transformation	 $H_{FE}(z)=-k\frac{z^{-2}}{1+z^{-2}}$	 $H_{BE}(z)=-k\frac{1}{1+z^{-2}}$	 $H_{BI}(z)=k\frac{1-z^{-2}}{1+z^{-2}}$

6.3 EFFECTS OF NON-IDEAL FACTORS ON PSEUDO-N-PATH INTEGRATORS

In this section, the effects of non-idealities such as finite output/input conductance ratio, clock-feedthrough, charge-injection and incomplete settling of memory cells on the response of the pseudo-2-path integrators are addressed. To varying extents, most non-ideal factors will cause distortion, with significant contributors being charge-injection and incomplete settling of memory cells. However, the effort here is focused mainly on linear, small-signal errors and their effect on the frequency response. Full transistor level SPICE simulations take excessively long amounts of time to run. Further, it is only possible to perform time-domain transient simulations of the switched-networks. Therefore, it is highly desirable to develop simplified models that are relatively fast, maintain reasonable accuracy, and can be used in direct AC simulations using the switched-network simulator SCNAP4[9]. Theoretical basics of the non-ideal phenomena are given and where possible, comparisons are made between theoretical and simulated results.

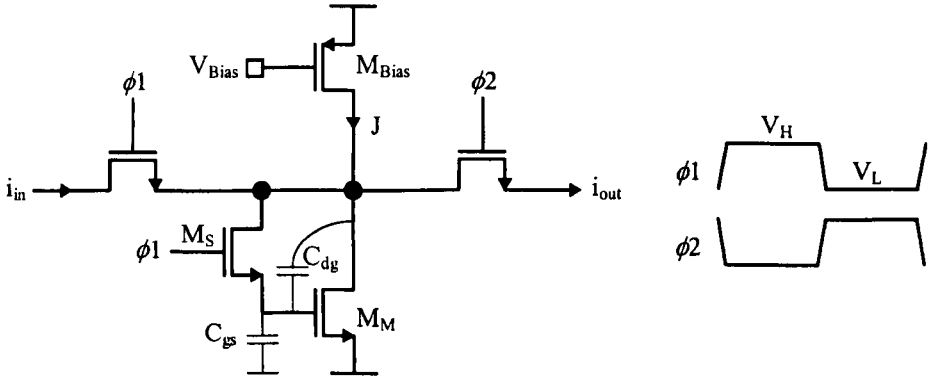


Figure 6.12 Basic second-generation switched-current memory cell and clock phases

6.3.1 Finite Output/Input Conductance Ratio Errors

To understand the error mechanisms associated with finite output/input conductance ratios, consider the operation of the basic second generation SI memory cell of Fig. 6.12. On the sampling phase($\phi 1$), transistor M_M is diode connected, forcing its drain

voltage to be the same as V_{gs}. When the holding mode is entered($\phi 2$), the memorised current is delivered to the load at the output. Any change in the drain voltage during this phase will produce an error current as a result of two main effects. The first of these is channel shortening, which gives a drain current of

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_T)^2(1 + \lambda V_{ds})$$

where λ is the channel shortening parameter, and a drain conductance of

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = \lambda I_{ds} \tag{6.7}$$

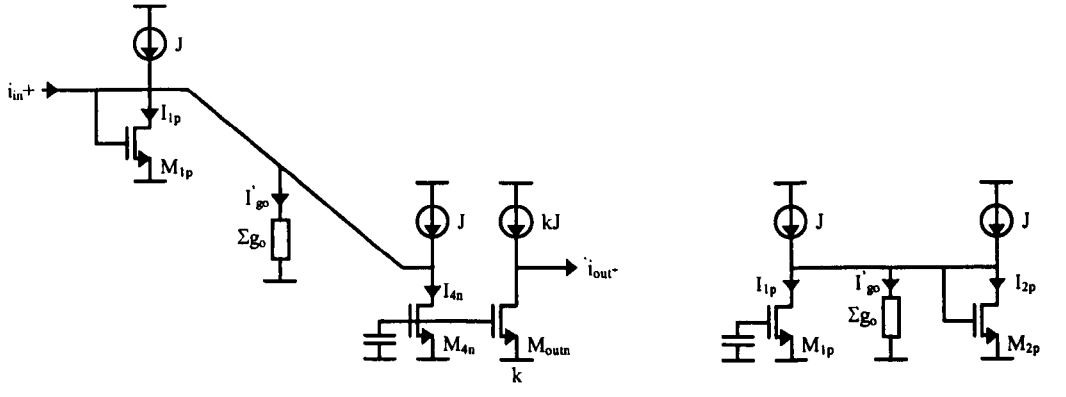
The second effect is due to the drain-gate(Miller) overlap capacitance C_{dg}, which couples voltage variations at the drain into the memory capacitor C_{gs}. This induces an error voltage at the gate of $\delta V_{ds}C_{dg}/(C_{dg}+C_{gs})$. The combined error current resulting from these two effects is given by

$$\delta I_{ds} = \delta V_{ds}\left(g_{ds} + \frac{C_{dg}}{C_{dg} + C_{gs}} g_m\right)$$

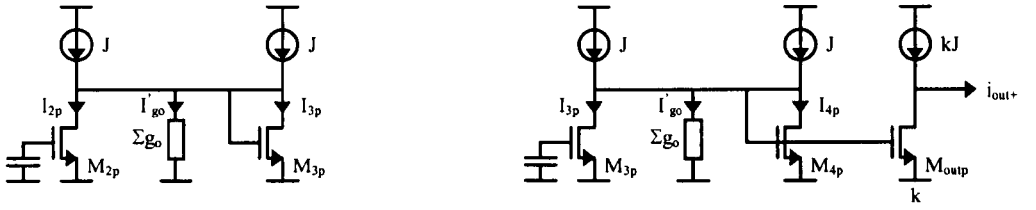
Memory cells can thus be modelled as an ideal memory transistor with a conductance g_o connected between the drain and source, where

$$g_o = g_{ds} + g_{ds(J)} + \frac{C_{dg}}{C_{gs} + C_{dg}} g_m \tag{6.8}$$

and $g_{ds(J)}$ is the drain conductance of the bias current source transistor M_{Bias}. In the following analyses, the effect of the small signal transmission error, ε_g, resulting from a finite g_o/g_m ratio, on the frequency response of the pseudo-2-path Forward Euler integrator in Fig. 6.7 will be studied.



(a) ϕ_1(n-2) (b) ϕ_2(n-1)



(c) $\phi_1(n-1)$ (d) $\phi_2(n)$

Figure 6.13 Circuit configuration of the pseudo-2-path Forward Euler integrator during different phases of a full cycle of operation

Starting from phase ϕ_1 of period (n-2),

$\underline{\phi_1(n-2)}$

$$I_{1p} = 2J+i_{in+}(n-2)-I'_{go}-I_{4n} \tag{6.9a}$$

Since $I_{1p} = J+i_{1p}$,

$$i_{1p} = J+i_{in+}(n-2)-I'_{go}-I_{4n} \tag{6.9b}$$

but $I'_{go} = v_{gs1}\Sigma g_o = (V_{gs}+i_{1p}/g_m)2g_o$, and $I_{4n} = J-i_{out-}(n-2)/k$, where V_{gs} and g_m are defined at $I_{ds} = J$. Therefore,

$$\begin{aligned} i_{1p} &= i_{in+}(n-2)-(V_{gs}+i_{1p}/g_m)2g_o+i_{out-}(n-2)/k \\ &= \frac{i_{in+}(n-2)+i_{out-}(n-2)/k-V_{gs}2g_o}{1+2g_o/g_m} \end{aligned} \tag{6.9c}$$

$\underline{\phi_2(n-1)}$

$$I_{2p} = 2J-I_{1p}-I'_{go} \tag{6.9d}$$

Since $I_{2p} = J+i_{2p}$ and $I_{1p} = J+i_{1p}$

$$i_{2p} = -i_{1p}-I'_{go} \tag{6.9e}$$

but $I'_{go} = v_{gs2}\Sigma g_o = (V_{gs}+i_{2p}/g_m)2g_o$, therefore,

$$\begin{aligned} i_{2p} &= -i_{1p}-(V_{gs}+i_{2p}/g_m)2g_o \\ &= \frac{-i_{1p}-V_{gs}2g_o}{1+2g_o/g_m} \end{aligned} \tag{6.9f}$$

$\underline{\phi_1(n-1)}$

$$I_{3p} = 2J-I_{2p}-I'_{go} \tag{6.9g}$$

Since $I_{3p} = J+i_{3p}$ and $I_{2p} = J+i_{2p}$

$$i_{3p} = -i_{2p} - I'_{go} \tag{6.9h}$$

but $I'_{go} = v_{gs3}\Sigma g_o = (V_{gs}+i_{3p}/g_m)2g_o$, therefore,

$$i_{3p} = -i_{2p} - (V_{gs}+i_{3p}/g_m)2g_o$$

$$= \frac{-i_{2p} - V_{gs}2g_o}{1+2g_o/g_m} \tag{6.9i}$$

$\underline{\phi_2(n)}$

$$I_{4p} = 2J - I_{3p} - I'_{go} \tag{6.9j}$$

Since $I_{4p} = J+i_{4p}$ and $I_{3p} = J+i_{3p}$

$$i_{4p} = -i_{3p} - I'_{go} \tag{6.9k}$$

but $I'_{go} = v_{gs4}\Sigma g_o = (V_{gs}+i_{4p}/g_m)2g_o$, therefore,

$$i_{4p} = -i_{3p} - (V_{gs}+i_{4p}/g_m)2g_o$$

$$= \frac{-i_{3p} - V_{gs}2g_o}{1+2g_o/g_m} \tag{6.9l}$$

Since $i_{out+} = -ki_{4p}$,

$$i_{out+}(n) = k\frac{i_{3p} + V_{gs}2g_o}{1+2g_o/g_m} \tag{6.9m}$$

By substituting the previously held currents and after some simplification, we obtain

$$i_{out+}(n) = \frac{-i_{out+}(n-2) + ki_{in+}(n-2)}{1+8g_o/g_m} \tag{6.9n}$$

Taking z-transforms and rearranging yields the non-ideal transfer-function of the pseudo-2-path Forward Euler integrator as

$$H_{FE}(z) = \frac{kz^{-2}}{1+8\frac{g_o}{g_m}+z^{-2}} \tag{6.9o}$$

By defining $\varepsilon_g = -2g_o/g_m$, (6.9o) can be expressed as

$$H_{FE}(z) = \frac{kz^{-2}}{1-4\varepsilon_g+z^{-2}} \tag{6.9p}$$

It can be shown using the approximation for small errors[8]

$$H\left(e^{j\omega T}\right) = \frac{H_i\left(e^{j\omega T}\right)}{[1-m(\omega)]e^{-j\theta(\omega)}} \approx \frac{H_i\left(e^{j\omega T}\right)}{1-m(\omega)-j\theta(\omega)}$$

where $m(\omega)$ is the magnitude error and $\theta(\omega)$ is the phase error, that for the pseudo-2-path Forward Euler integrator, $m(\omega) = 2\varepsilon_g$ and $\theta(\omega) = 2\varepsilon_g\tan(\omega T)$. Analysis of the

z→-z Forward Euler integrator of Fig. 6.3 will yield $m(\omega) = \varepsilon_g$ and $\theta(\omega) = \varepsilon_g \tan(\omega T)$. The result is expected, as the delay line in the pseudo-2-path integrator has twice the number of transistors. This underscores the susceptibility of circulating-delay type pseudo-N-path structures to finite-conductance ratio errors. Use of gain enhancement techniques such as cascoding and error correction memory cells[8] will be required to minimise the errors.

The system poles and magnitude at the resonant frequency are given by

$$z_p = \pm j \sqrt{\frac{1}{1+8\frac{g_o}{g_m}}} \quad \text{and} \quad \left|H_{FE}(z_p)\right| = k\frac{g_m}{8g_o} \tag{6.9q}$$

Clearly, the poles remain located along the imaginary axis while the gain is inversely proportional to g_o/g_m. Fortunately, the circuit remains stable as both g_m and g_o are positive quantities, confining both poles within the unit circle of the z-plane.

Following a similar analysis, the non-ideal transfer-functions of the pseudo-2-path Backward Euler and bilinear integrators can be derived as:

Backward Euler integrator:

$$H_{BE}(z) = \frac{-k(1-3\varepsilon_g)}{1-4\varepsilon_g + z^{-2}} \tag{6.10a}$$

with corresponding system poles and magnitude at the resonant frequency given by

$$z_p = \pm j \sqrt{\frac{1}{1+8\frac{g_o}{g_m}}} \quad \text{and} \quad \left|H_{BE}(z_p)\right| = k\frac{1+6\frac{g_o}{g_m}}{8\frac{g_o}{g_m}} \tag{6.10b}$$

and

Bilinear integrator:

$$H_{BI}(z) = \frac{k}{1-\frac{3}{2}\varepsilon_g}\,\frac{1-\frac{11}{2}\varepsilon_g - z^{-2}}{1-5\varepsilon_g\left(\frac{1}{1-\frac{3}{2}\varepsilon_g}\right)+z^{-2}} \tag{6.11a}$$

with corresponding system poles and magnitude at the resonant frequency given by

$$z_p = \pm j\sqrt{\frac{1+3\frac{g_o}{g_m}}{1+13\frac{g_o}{g_m}}} \quad \text{and} \quad \left|H_{BI}(z_p)\right| = k\frac{2+11\frac{g_o}{g_m}}{10\frac{g_o}{g_m}} \tag{6.11b}$$

To verify the non-ideal transfer-functions, simulations were carried out in SCNAP4 for various values of ε_g. The results are plotted together with the theoretical equations of (6.9p), (6.10a) and (6.11a) in Figs. 6.14~6.16 for comparison. It can be seen that the results agree closely, and that the effect of finite conductance ratio errors is to attenuate the resonant gain without affecting the resonant frequency. The difference between simulated and theoretical results worsens as ε_g increases. This is a consequence of discarding the higher order ε_g terms which become significant as the assumption $\varepsilon_c << 1$ becomes invalid.

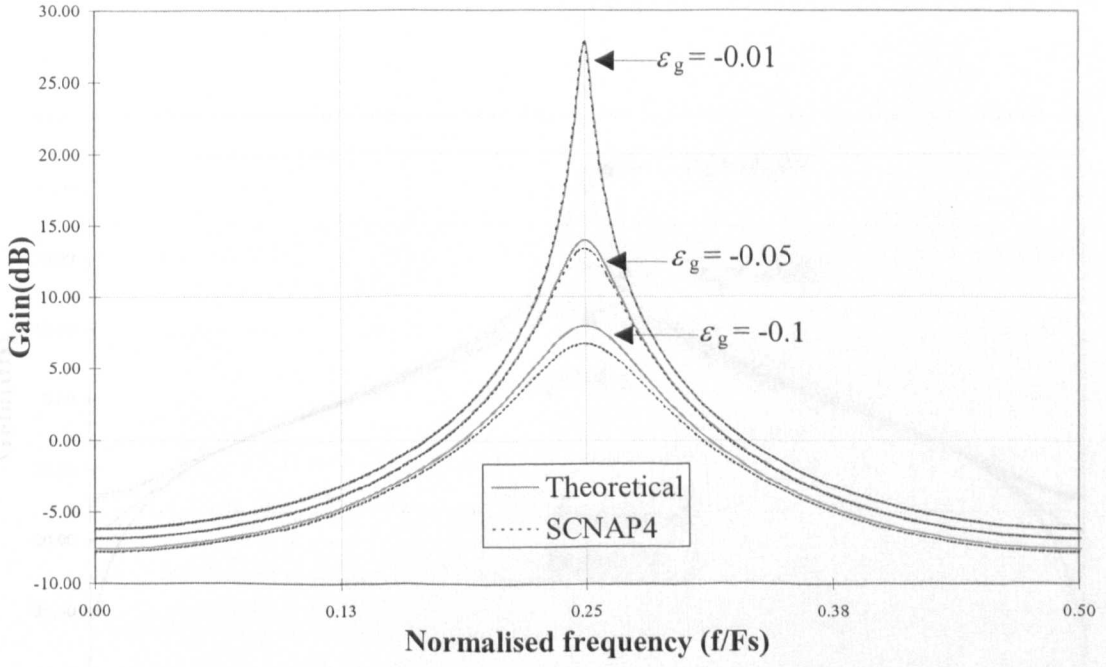


Figure 6.14 Frequency response of pseudo-2-path Forward Euler integrator with finite conductance ratio errors

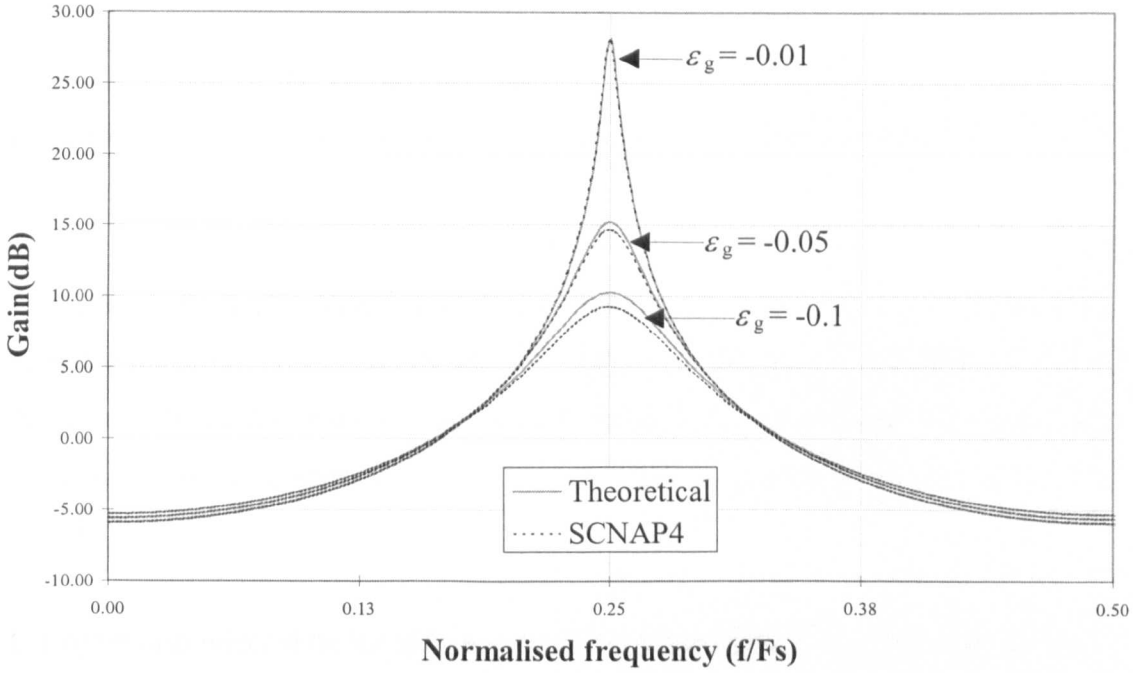


Figure 6.15 Frequency response of pseudo-2-path Backward Euler integrator with finite conductance ratio errors

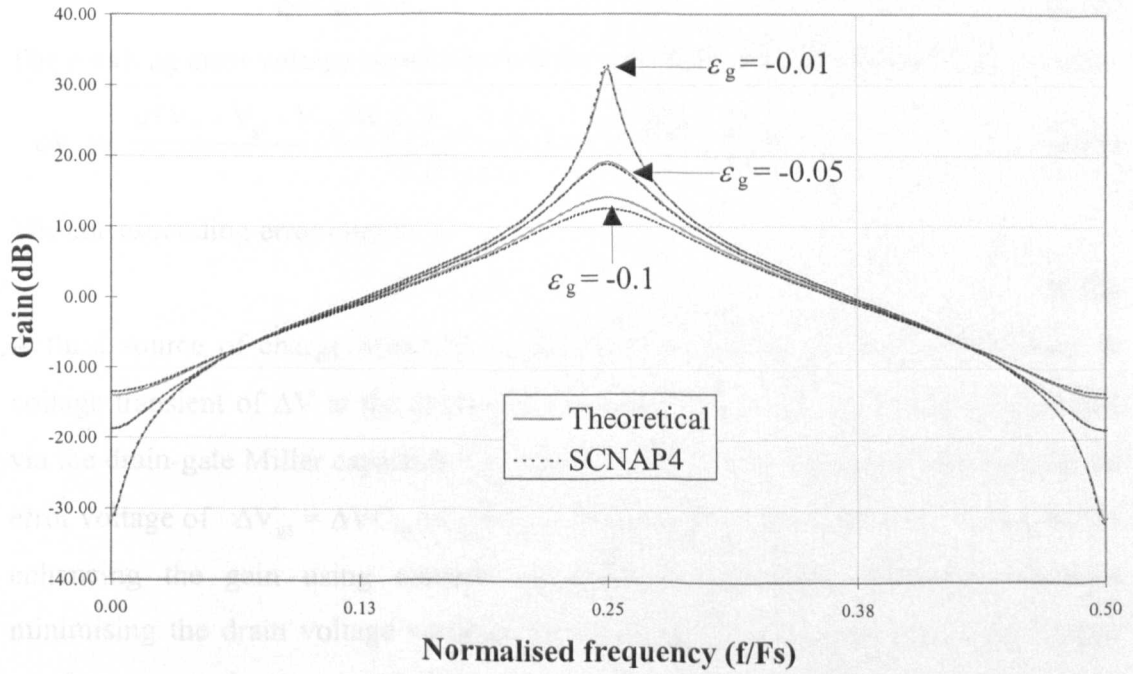


Figure 6.16 Frequency response of pseudo-2-path bilinear Euler integrator with finite conductance ratio errors

6.3.2 Clock-feedthrough and Charge-injection Errors

From the circuit of the second-generation SI memory cell of Fig. 6.12, the channel charge injected by the switch M_S into the gate-source memory capacitor C_{gs} is given by[8]

$$q_{ch} = \alpha(V_H - V_{gs} - V_{TS})W_S L_S C_{ox} \tag{6.12}$$

where V_H is the high voltage level of the clock, V_{gs} is the gate-source voltage of the memory transistor, V_{TS} is the threshold voltage, and W_S, L_S the width and length of the switch. $W_S L_S C_{OX}$ is the switch channel capacitance. The factor α determines the fraction of charge injected, and depends on the capacitance ratios on both sides of the switch.

Charge is also injected by the gate-source overlap capacitance, C_{ov}, and is given by

$$q_{ov} = (V_H - V_L)C_{ov} = (V_H - V_L)\, W_S L_{ovS} C_{ox} \tag{6.13}$$

where V_L is the low voltage level of the clock and L_{ovS} is the length of the overlap at the source side of switch M_S. The total charge injected into the memory capacitor is thus given by

$$q = q_{ch} + q_{ov} \tag{6.14}$$

The resulting error voltage across the memory capacitor with an area of $W_M L_M$ is thus

$$\delta V = \frac{\alpha(V_H - V_{gs} - V_{TS})W_S L_S C_{ox} + (V_H - V_L)W_S L_{ovS} C_{ox}}{W_M L_M C_{ox}} \tag{6.15}$$

The corresponding error current is

$$\delta I = g_m \delta V \tag{6.16}$$

A third source of charge injection occurs when switch M_S is in the OFF state. A voltage transient of ΔV at the drain of the memory transistor is capacitively coupled via the drain-gate Miller capacitor, C_{dg}, into the gate-source capacitor. This induces an error voltage of $\Delta V_{gs} = \Delta V C_{dg}/(C_{dg}+C_{gs})$. This problem can usually be minimised by enhancing the gain using cascode or regulated-cascode[8] topologies. Besides minimising the drain voltage variation of the main memory transistor, input/output conductance ratio is significantly improved while the Miller capacitance is reduced[11].

By accounting for this charge-injection error with $\varepsilon_c = \delta I/I$, and neglecting all other non-idealities, its effect on the small-signal transfer-function of the pseudo-2-path Forward Euler integrator(Fig. 6.7), can be analysed as follows; Beginning in phase t1 of period (n-2), the current in the memory cells at the end of each respective clock phase is given by

t1(n-2)

$$i_{1p}(n-2) = [i_{in+}(n-2)-i_{4n}(n-2)](1-\varepsilon_c) \tag{6.17a}$$

t2(n-1)

$$i_{2p}(n-2) = -i_{1p}(n-2)(1-\varepsilon_c) \tag{6.17b}$$

t1(n-1)

$$i_{3p}(n-1) = -i_{2p}(n-2)(1-\varepsilon_c) \tag{6.17c}$$

t2(n)

$$\begin{aligned} i_{4p}(n) &= -i_{3p}(n-1)(1-\varepsilon_c) \\ &= -[i_{in+}(n-2)+i_{4p}(n-2)](1-\varepsilon_c)^4 \end{aligned} \tag{6.17d}$$

Substituting for $i_4 = -i_o$ and rearranging gives

$$i_{op}(n)+i_{op}(n-2)(1-\varepsilon_c)^4 = (1-\varepsilon_c)^4 i_{in+}(n-2) \tag{6.17e}$$

Assuming $\varepsilon_c << 1$ and taking z-transforms yields the simplified non-ideal transfer-function for the pseudo-2-path Forward Euler integrator as

$$H_{FE}(z)= \frac{(1-4\varepsilon_c+6\varepsilon_c^2)z^{-2}}{1+(1-4\varepsilon_c+6\varepsilon_c^2)z^{-2}} \tag{6.17f}$$

Similarly, it can be shown that the simplified non-ideal transfer-functions of the pseudo-2-path Backward Euler and bilinear integrator are given as:

Backward Euler integrator:

$$H_{BE}(z)= \frac{-1}{1+\varepsilon_c+(1-3\varepsilon_c+2\varepsilon_c^2)z^{-2}} \tag{6.18a}$$

Bilinear integrator:

$$H_{BI}(z)= \frac{1-\varepsilon_c-(1-6\varepsilon_c+15\varepsilon_c^2)z^{-2}}{1+(1-4\varepsilon_c+6\varepsilon_c^2)z^{-2}} \tag{6.19a}$$

To simulate the effect of charge injection in SCNAP4, a simplified macro model for a single memory cell has to be developed. Neglecting channel-length modulation, the drain current that is held after sampling can be expressed as

$$I_d = \frac{\beta}{2}(V_{gs} - V_T + \delta V)^2$$

$$= \frac{\beta}{2}(V_{gs} - V_T)^2 + \frac{\beta}{2}\left[2\delta V(V_{gs} - V_T) + \delta V^2\right] \tag{6.20}$$

The output current is given by

$$i_o = J\text{-}I_d$$

$$= J - \left(\frac{\beta}{2}(V_{gs} - V_T)^2 + \frac{\beta}{2}\left[2\delta V(V_{gs} - V_T) + \delta V^2\right]\right) \tag{6.21}$$

In terms of difference equations, this is equivalent to

$$\begin{aligned} i_o(n) &= -i_{in}(n - 1/2) - \frac{\beta}{2}\left[2\delta V(V_{gs} - V_T) + \delta V^2\right] \\ &= -i_{in}(n - 1/2) - \delta V\sqrt{2\beta J}\sqrt{1 + \frac{i_{in}(n - 1/2)}{J}} - \frac{\beta}{2}\delta V^2 \end{aligned} \tag{6.22}$$

To obtain more insight from the unwieldy form of (6.22), a Taylor series expansion of i_{in} yields

$$i_o(n) = -\left[\delta V\sqrt{2\beta J} + \frac{\beta}{2}\delta V^2\right] - i_{in}(n - 1/2)\left[1 + \delta V\sqrt{\frac{\beta}{2J}}\right] + i_{in}(n - 1/2)^2\left[\frac{\delta V}{8}\frac{\sqrt{2\beta}}{\sqrt[3]{J}}\right] + \cdots \tag{6.23}$$

From (6.23), it can be seen that charge injection results in offset, gain and non-linearity or distortion errors as indicated by the first, second and higher order terms respectively. Ideally, $\delta V = 0$, and (6.23) reduces to the familiar $i_o(n) = -i_{in}(n\text{-}1/2)$ of an ideal memory cell.

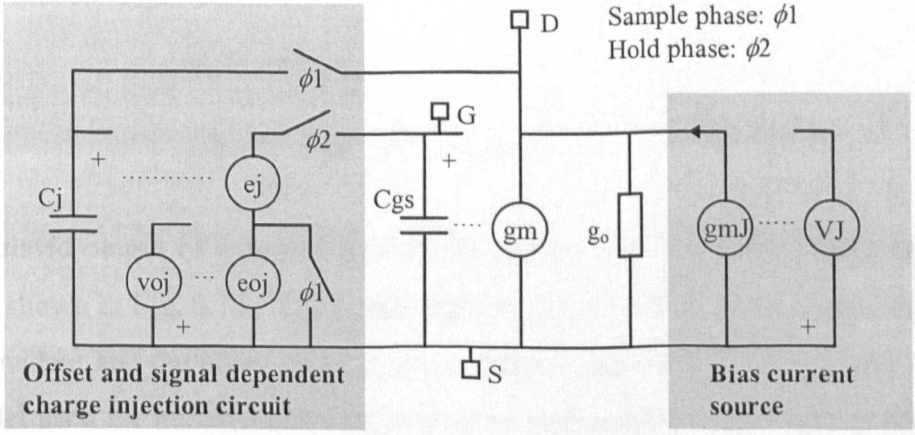


Figure 6.17 Charge injection macromodel of memory cell

It was decided to incorporate only the offset and gain errors into the memory cell macromodel given that SCNAP4 is capable of simulating only linear systems. This is a reasonable assumption, as for small signals the error function is linear to a first order approximation. With large signals, g_m and the charge injected, q, will vary non-linearly to produce harmonic distortion(see Fig. 6.40).

The operation of the charge injection model of Fig. 6.17, neglecting the effect of g_o is described as follows: During the sampling phase(ϕ1), the circuit is diode-connected with the drain(D) and gate(G) shorted. Capacitor Cj is charged up by the bias current J and i_{in} to the ideal voltage of V_{gs}^{i}. Throughout this time, the offset, Vos = -vojeoj, is shorted to ground. During the hold phase(ϕ2), Cgs charges up to $V_{gs} = ejV_{gs}^{i}+Vos$, and the drain current becomes $I_d = g_m V_{gs}$. Because the bias current J is always connected to the drain, the output current is therefore given by

$$\begin{aligned} i_o &= J-I_d \\ &= J-g_m V_{gs} \\ &= J-g_m(ejV_{gs}^{i}+Vos) \\ &= J-ej(i_{in}+J)-g_m Vos \\ &= J(1-ej)-g_m Vos- i_{in}ej \end{aligned} \tag{6.24}$$

By defining ej = 1-ε_c, (6.24) becomes

$$i_o = \varepsilon_c J-g_m Vos-i_{in}(1-\varepsilon_c) \tag{6.25}$$

Clearly, (6.25) is a linear approximation of (6.23), where the offset and gain errors are governed by eoj and ej = 1-ε_c respectively. Equating (6.25) to (6.23) yields

$$\begin{aligned} \varepsilon_c &= -\delta V\sqrt{\frac{\beta}{2J}} \\ eoj &= \frac{1}{g_m}\left[\delta V\sqrt{\frac{\beta J}{2}}+\frac{\beta}{2}\delta V^2\right] \end{aligned} \tag{6.26}$$

The simulated output of a second generation memory cell using the charge injection model is shown in Fig. 6.18. The signal dependence(ε_c = 0.05) of the charge injection error is evident and the effect of an injected offset(Vos = 0.05V) error is also shown. The model used for mirror-connected outputs to realise filter coefficients is shown in Fig. 6.19. Both the bias current source and g_m are scaled by k.

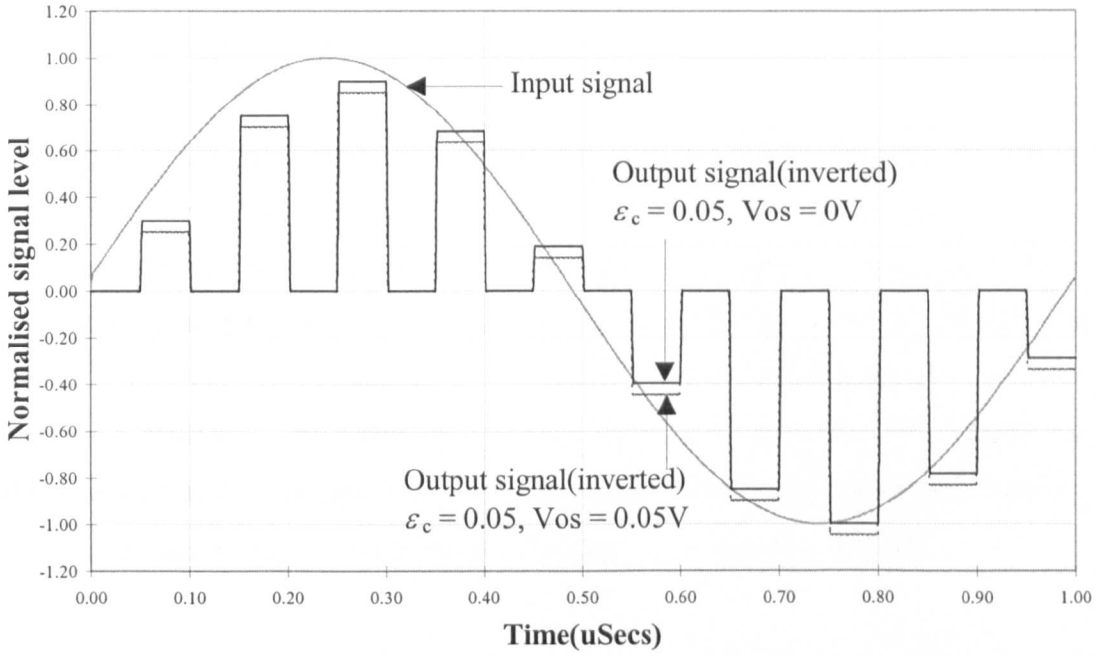


Figure 6.18 Simulated output current of a memory cell based on the charge-injection model

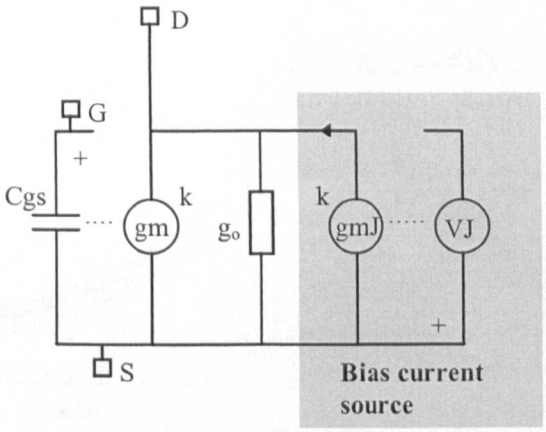


Figure 6.19 Macromodel for mirror-connected output transistors

The three pseudo-2-path integrators were simulated with SCNAP4 using the models just described for different values of ε_c. In a small-signal AC simulation, the DC voltage sources will be shorted to ground, nullifying the effects of the offset. To account for the effects of the offset voltage, an impulse response of the network has to

be obtained in a transient simulation and processed by FFT. However, both approaches will yield almost identical results in the frequency domain as the offset component will appear as just a peak at DC.

The results of the simulations are plotted together with the respective theoretical transfer functions of (6.17~6.19) in Figs. 6.20~6.22. It can be seen that the results are in close agreement. The effect of charge injection errors on the frequency response of the pseudo-2-path integrators is to attenuate the resonant gain without affecting the resonant frequency. This is similar to the effect of finite conductance ratio errors of the previous analysis. The difference observed between the simulated and theoretical results worsens as ε_c increases. This is a consequence of discarding the higher order ε_c terms which become significant as the assumption $\varepsilon_c << 1$ becomes invalid.

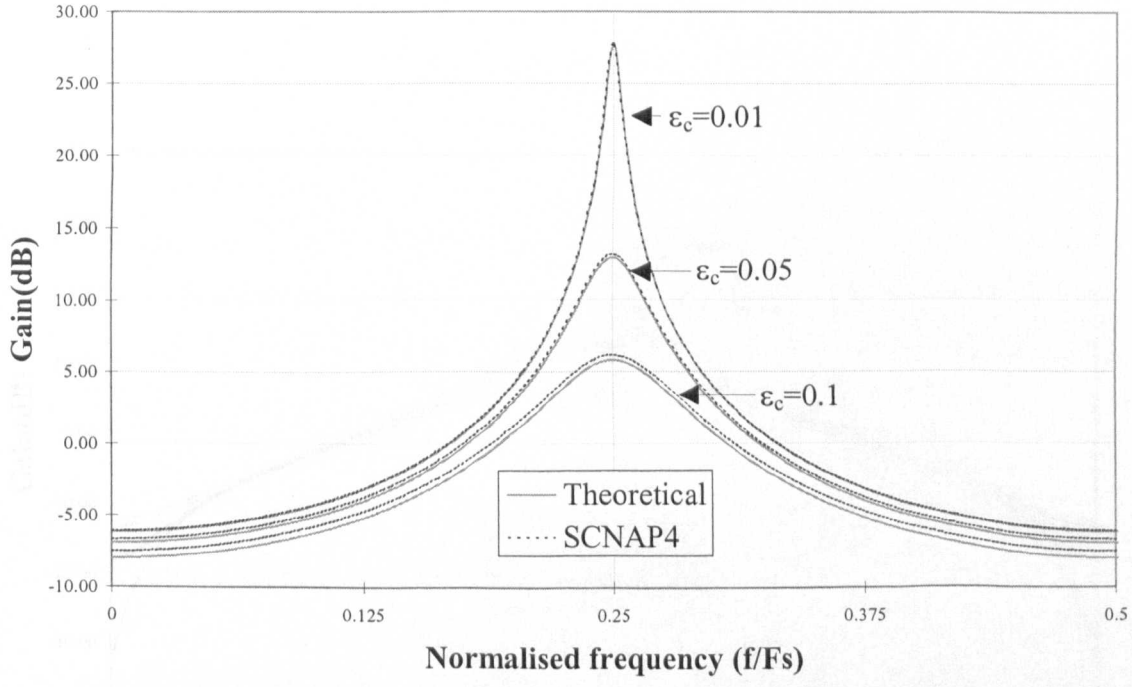


Figure 6.20 Frequency response of the pseudo-2-path Forward Euler integrator with charge injection errors

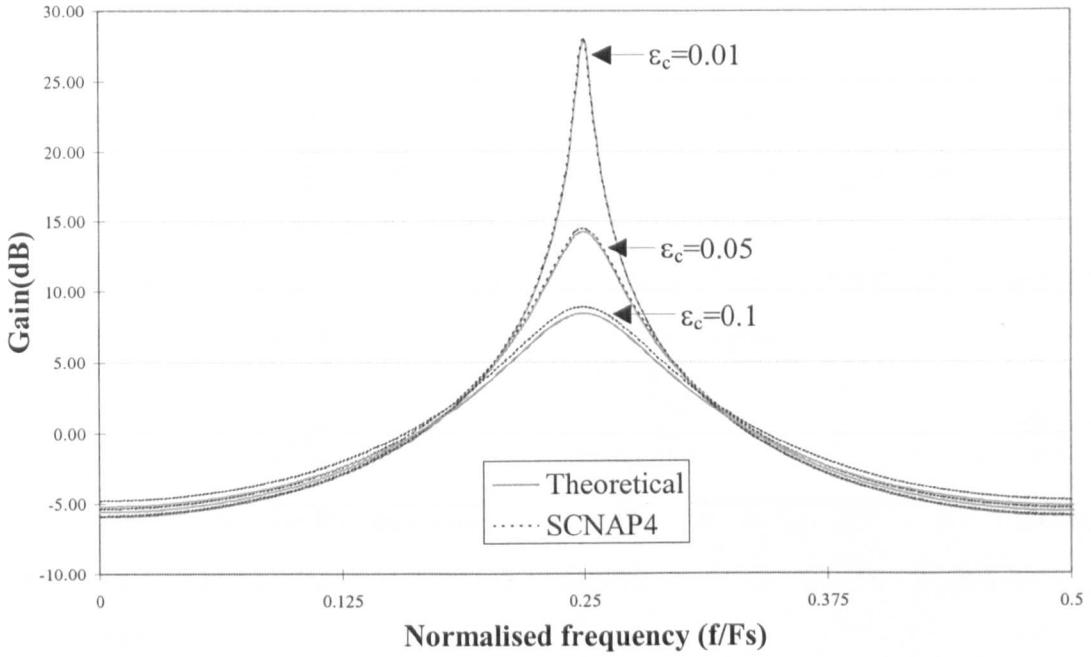


Figure 6.21 Frequency response of the pseudo-2-path Backward Euler integrator with charge injection errors

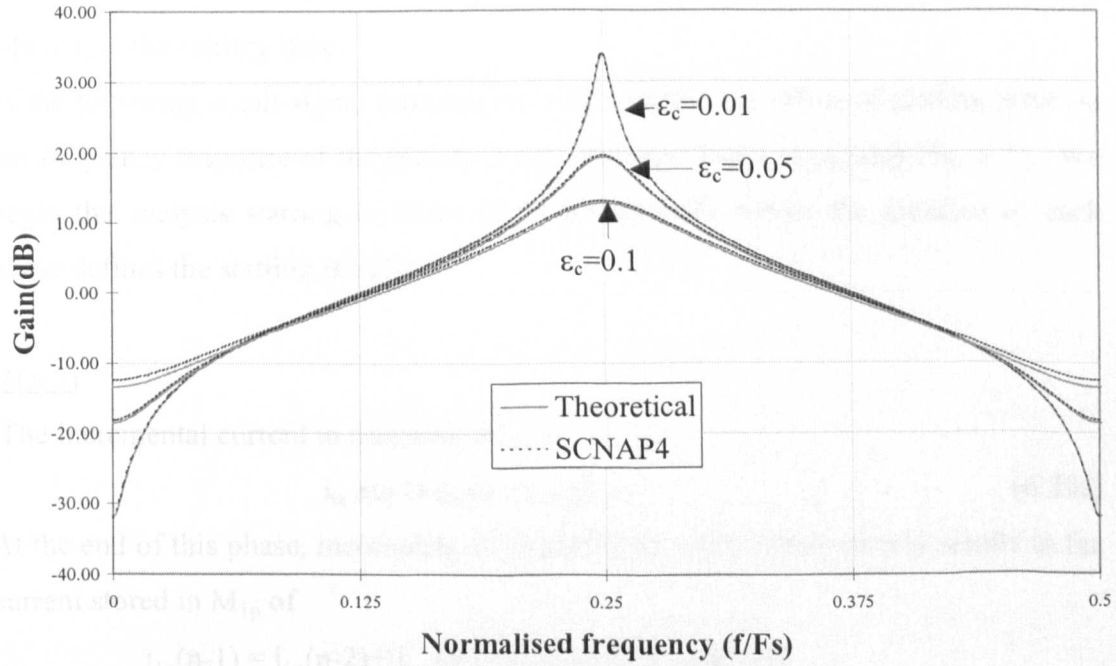


Figure 6.22 Frequency response of the pseudo-2-path bilinear integrator with charge injection errors

6.3.3 Settling Errors

Settling errors originate from incomplete charging of the memory capacitor C_{gs} within the duration of the sampling phase. This results in an error in the output current, which is sampled by subsequent stages. It has been shown[8] that the dynamics of a second-generation SI memory cell can be described by a second order lowpass transfer function with the pole frequency and Q-factor given by

$$\omega_o = \sqrt{\frac{g_m}{r_S C_{gs} C_{ds}}} \quad \text{and} \quad Q = \frac{\sqrt{g_m r_S C_{gs} C_{ds}}}{C_{gs} + C_{ds}} \tag{6.27}$$

where r_s is the switch-ON resistance of transistor M_S in Fig. 6.12. For stability reasons, an overdamped($Q<0.5$) response is desired, in which case, the settling error ε_s is given[8] by

$$\varepsilon_s = \frac{1}{2\sqrt{1-4Q^2}}\left[\left(1+\sqrt{1-4Q^2}\right)\exp\left(-\frac{1-\sqrt{1-4Q^2}}{2Q}\omega_o t_s\right)\right.$$
$$\left.-\left(1-\sqrt{1-4Q^2}\right)\exp\left(-\frac{1+\sqrt{1-4Q^2}}{2Q}\omega_o t_s\right)\right] \tag{6.28}$$

where t_s is the settling time.

In the following small-signal analysis, we will consider the effect of settling error on the frequency response of the pseudo-2-path Forward Euler integrator(Fig. 6.7). We begin the analysis starting in phase t1 of period (n-2), where the duration of each phase defines the settling time t_s.

t1(n-2)

The incremental current in transistor M_{1p} is

$$i_{in+}(n\text{-}2)\text{-}i_{4n}(n\text{-}2)\text{-}i_{1p}(n\text{-}2) \tag{6.29a}$$

At the end of this phase, incomplete charging by the incremental current results in the current stored in M_{1p} of

$$i_{1p}(n\text{-}1) = i_{1p}(n\text{-}2)+[i_{in+}(n\text{-}2)\text{-}i_{4n}(n\text{-}2)\text{-}i_{1p}(n\text{-}2)](1\text{-}\varepsilon_s)$$
$$= \varepsilon_s i_{1p}(n\text{-}2)+(1\text{-}\varepsilon_s)[i_{in+}(n\text{-}2)\text{-}i_{4n}(n\text{-}2)] \tag{6.29b}$$

t2(n-1)

The incremental current in transistor M_{2p} is

$$-i_{1p}(n-1)-i_{2p}(n-2) \tag{6.29c}$$

At the end of this phase, incomplete charging by the incremental current results in the current stored in M_{2p} of

$$\begin{aligned} i_{2p}(n-1) &= i_{2p}(n-2)+[-i_{1p}(n-1)-i_{2p}(n-2)](1-\varepsilon_s) \\ &= \varepsilon_s i_{2p}(n-2)-(1-\varepsilon_s)i_{1p}(n-1) \end{aligned}$$

Rearranging,

$$i_{1p}(n-1) = \frac{\varepsilon_s}{1-\varepsilon_s} i_{2p}(n-2) - \frac{1}{1-\varepsilon_s} i_{2p}(n-1) \tag{6.29d}$$

t1(n-1)

The incremental current in transistor M_{3p} is

$$-i_{2p}(n-1)-i_{3p}(n-1) \tag{6.29e}$$

At the end of this phase, incomplete charging by the incremental current results in the current stored in M_{3p} of

$$\begin{aligned} i_{3p}(n) &= i_{3p}(n-1)+[-i_{2p}(n-1)-i_{3p}(n-1)](1-\varepsilon_s) \\ &= \varepsilon_s i_{3p}(n-1)-(1-\varepsilon_s)i_{2p}(n-1) \end{aligned} \tag{6.29f}$$

Rearranging,

$$i_{2p}(n-1) = \frac{\varepsilon_s}{1-\varepsilon_s} i_{3p}(n-1) - \frac{1}{1-\varepsilon_s} i_{3p}(n) \tag{6.29g}$$

t2(n)

The incremental current in transistor M_{4p} is

$$-i_{3p}(n)-i_{4p}(n-1) \tag{6.29h}$$

At the end of this phase, incomplete charging by the incremental current results in the current stored in M_{4p} of

$$\begin{aligned} i_{4p}(n) &= i_{4p}(n-1)+[-i_{3p}(n)-i_{4p}(n-1)](1-\varepsilon_s) \\ &= \varepsilon_s i_{4p}(n-1)-(1-\varepsilon_s)i_{3p}(n) \end{aligned} \tag{6.29i}$$

Rearranging,

$$i_{3p}(n) = \frac{\varepsilon_s}{1-\varepsilon_s} i_{4p}(n-1) - \frac{1}{1-\varepsilon_s} i_{4p}(n) \tag{6.29j}$$

By back substitution and some rearranging, we obtain

$$i_{out+}(n) = (1-\varepsilon_s)^4 i_{in+}(n-2)+4\varepsilon_s i_{out+}(n-1)-[6\varepsilon_s^2+(1-\varepsilon_s)^4]i_{out+}(n-2)+ 4\varepsilon_s^3 i_{out+}(n-3)-\varepsilon_s^4 i_{out+}(n-4) \tag{6.29k}$$

From (6.29k), it can be seen that the settling error produces residual, or memorised errors related to signals from earlier clock cycles in addition to attenuating the input

signal. Taking z-transforms and after some simplification yields the transfer-function of the pseudo-2-path Forward Euler integrator as

$$H_{FE}(z) = \frac{(1-4\varepsilon_s+6\varepsilon_s^2)z^{-2}}{1-4\varepsilon_s z^{-1}+(1-4\varepsilon_s+12\varepsilon_s^2)z^{-2}} \tag{6.29l}$$

The system poles are given by

$$z_p = 2\varepsilon_s \pm j\sqrt{1-4\varepsilon_s+8\varepsilon_s^2} \tag{6.29m}$$

Clearly, settling error displaces the poles from the imaginary axis by $2\varepsilon_s$ apart from attenuating the gain at resonance. The non-ideal transfer-function of the pseudo-2-path Backward Euler and bilinear integrators can similarly be derived as:

$$H_{BE}(z) = \frac{-1+\varepsilon_s+3\varepsilon_s(1-\varepsilon_s)z^{-1}-3\varepsilon_s^2 z^{-2}}{1-4\varepsilon_s z^{-1}+(1-4\varepsilon_s+12\varepsilon_s^2)z^{-2}} \tag{6.30a}$$

$$H_{BI}(z) = \frac{(1-6\varepsilon_s+15\varepsilon_s^2)(1-z^{-2})}{1-6\varepsilon_s z^{-1}+(1-4\varepsilon_s+21\varepsilon_s^2)z^{-2}-2\varepsilon_s(1-4\varepsilon_s)z^{-3}+\varepsilon_s^2 z^{-4}} \tag{6.31a}$$

To verify the analyses, simulation was performed for different values of ε_s obtained using (6.27) and (6.28) for the overdamped condition. The results are shown in Figs. 6.23~6.25 for both the theoretical and simulated responses. Settling error thus attenuates the gain and lowers the resonant frequency. This is detrimental to narrowband bandpass systems where stability of the passband centre frequency is crucial. Therefore, adequate time must be provided for settling($>7\tau$ where $\tau=1/\omega_0$)[8] in order to minimise these errors. This imposes an upper limit on the highest achievable clock frequency. The error between theoretical and simulated responses at larger values of ε_s for the bilinear integrator is mainly due to the simplification of an otherwise large and unwieldy non-ideal theoretical transfer-function. It should be noted that ε_s = 0.01 represents an error of 1% while most practical circuits are designed to settle to within 0.1%.

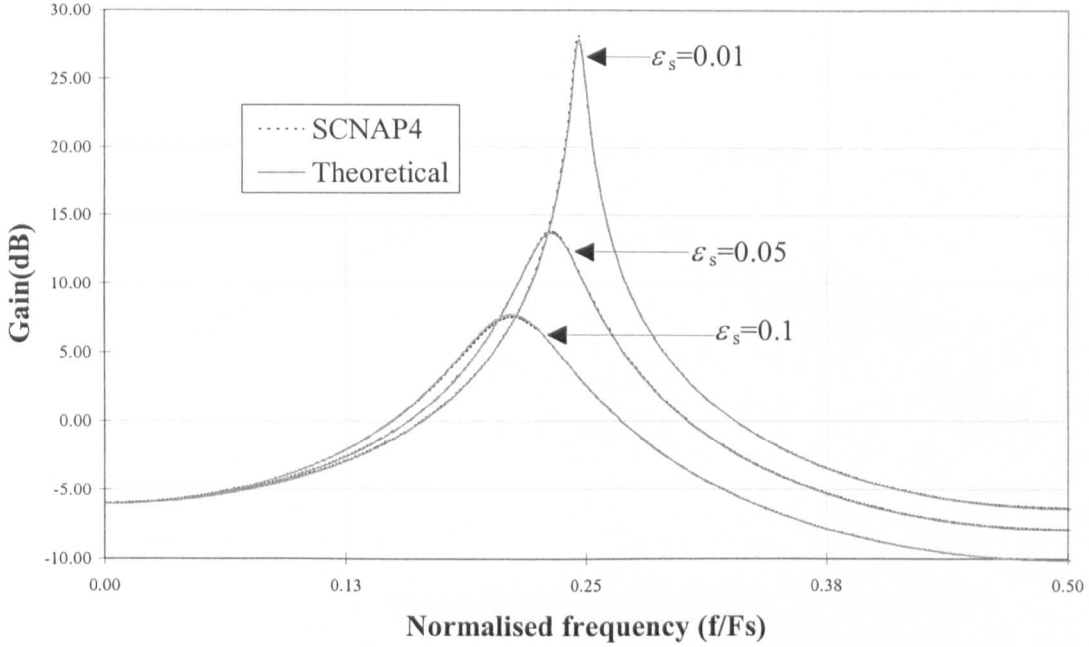


Figure 6.23 Frequency response of the pseudo-2-path Forward Euler integrator with settling errors

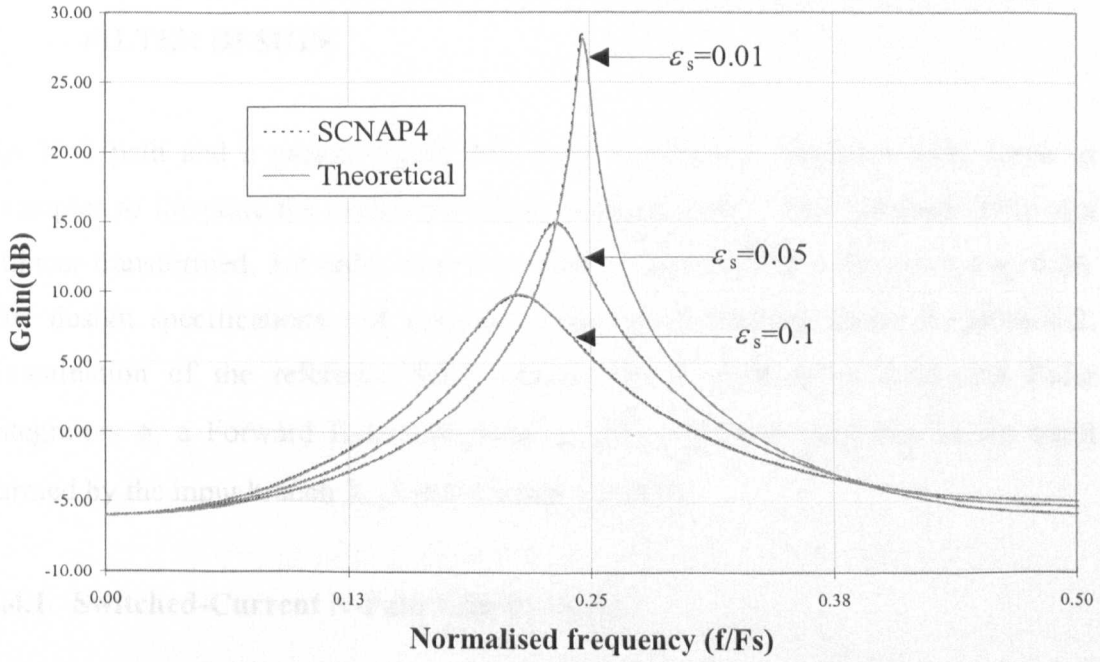


Figure 6.24 Frequency response of the pseudo-2-path Backward Euler integrator with settling errors

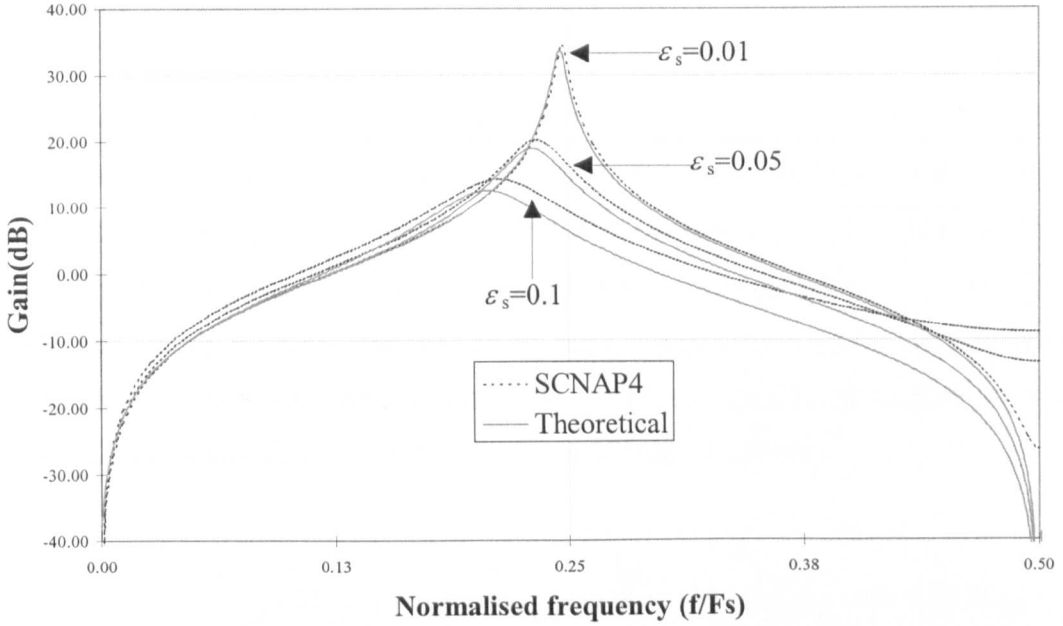


Figure 6.25 Frequency response of the pseudo-2-path bilinear integrator with settling errors

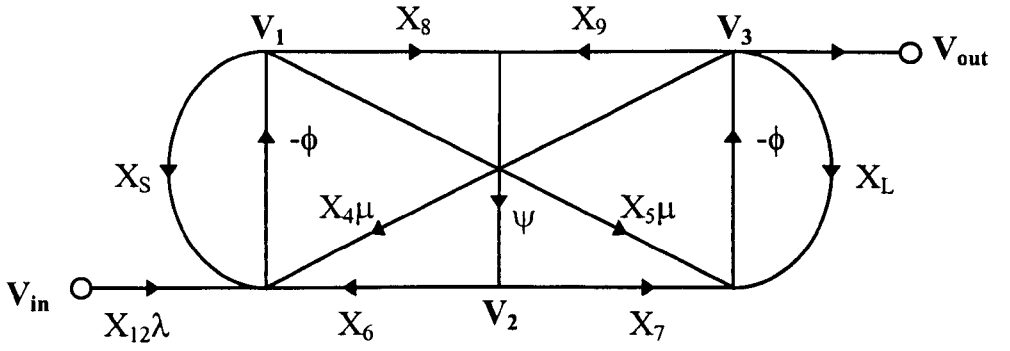
6.4 SWITCHED-CURRENT N-PATH AND PSEUDO-N-PATH LADDER FILTER DESIGN

An N=2 path and a pseudo-2-path 6th order narrowband bandpass filter serve as examples to illustrate the usefulness of the proposed cells. The z-domain SFG of a bilinear-transformed, 3rd order elliptic lowpass reference filter is shown in Fig. 6.26. The design specifications and transistor ratio coefficients are listed in Table 6.2. Examination of the reference SFG shows that it consists of Backward Euler integrators ϕ, a Forward Euler integrator ψ, and a bilinear integrator at the input formed by the input branch $X_{12}\lambda$ and the first ϕ branch.

6.4.1 Switched-Current N-Path Ladder Design

The transformation process is achieved by simply replacing the integrators within the SFG by their corresponding transformed versions(Figs. 6.3-6.5). The feed-through signals represented by branches with the factor $\mu=(1-z^{-1})$ are connected to the respective summing nodes immediately following the input sampling switches. To

replace the λ input branch by the transformed bilinear integrator, the output of the bilinear integrator has to be connected to the summing node of the first Backward Euler integrator instead of the integrating input. The resulting z→ -z transformed path filter is shown in Fig. 6.27 without the bias circuits to highlight the connectivity. To achieve the z→ $-z^2$ transformation for a bandpass response, two path filters in parallel are sampled in a time interleaved manner as shown in Fig. 6.28. For a two phase clock, this simply involves opposite phase sequences for both paths. A sample-and-hold is required for each path as the bilinear input stage samples on both phase t1 and t2. Each path is sampled at 10MHz for an overall rate of 20MHz.



$$\phi = k\frac{1}{1-z^{-1}},\quad \psi = k\frac{z^{-1}}{1-z^{-1}},\quad \mu=(1-z^{-1}),\quad \lambda=(1+z^{-1})$$

Figure 6.26 SFG of bilinear-transformed, 3rd order elliptic lowpass reference filter

Table 6.2 Design specifications and transistor ratio coefficients of the prototype lowpass filter

Design specifications of 3rd order lowpass prototype filter					
Passband Edge	1kHz		Passband Ripple		0.5dB
Stopband Edge	2kHz		Stopband Attenuation		30dB
Transistor ratios					
X_4	0.092297	X_7	0.079797	X_{10}	0.038763
X_5	0.177828	X_8	0.045229	X_{11}	0.038763
X_6	0.057488	X_9	0.032585	X_{12}	0.027926
Transistor Spread:	35.8		Clock Frequency:		10MHz

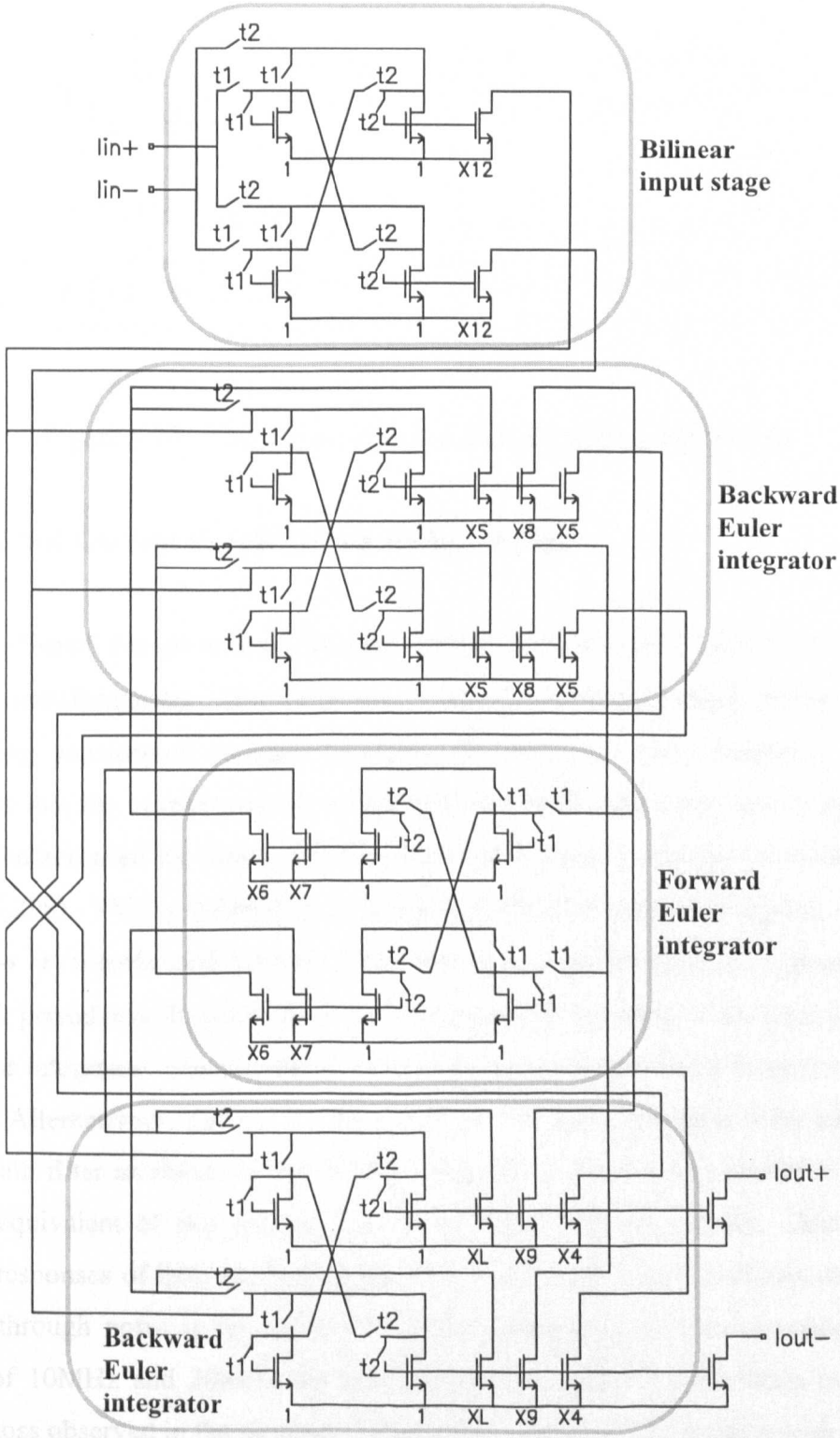


Figure 6.27 Switched-current highpass path filter by z→ -z transformation

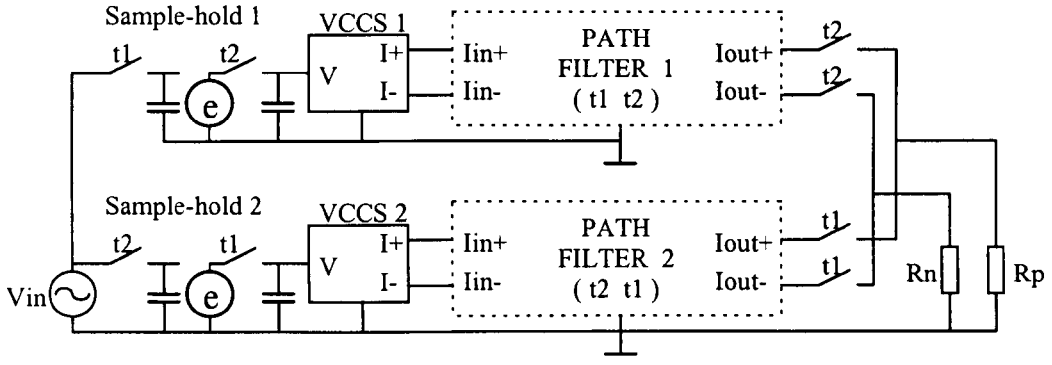


Figure 6.28 Structure of the N=2 path switched-current filter

6.4.2 Switched-Current Pseudo-N-Path Ladder Design

The pseudo-N-path design is more straight-forward as each cell in Figs. 6.7-6.9 performs the $z \rightarrow -z^2$ transformation. The integrators within the SFG are simply replaced by their corresponding transformed versions following the rules previously described. The only exception is that the output polarity of the Forward Euler integrator has to be reversed, which can be achieved by simply crossing the output signal pairs(shown shaded in Figs. 6.29a and 6.29b). This is required as the integrator circuit is non-inverting(Fig. 6.7), while a proper $z \rightarrow -z^2$ transformed Forward Euler integrator transfer-function is inverting(Table 6.1). A full period sample-and-hold circuit is required at the input if the filter is preceded by a bilinear integrator. The simplified schematic less the bias current sources is shown in Fig. 6.29a. Alternatively, the $(1-z^{-2})$ circuit of Fig. 6.10 can be cascaded at the output of the pseudo-2-path filter as shown in Fig. 6.29b. Both filters have to be clocked at 20MHz to fulfill the equivalent of two time-interleaved, 10MHz sampled circuits. The simulated amplitude responses of both the N-path and pseudo-N-path filters are shown in Fig. 6.30. Clock-feedthrough noise is far removed from the passbands, as the harmonics occur at multiples of 10MHz and 20MHz for the N-path and pseudo-N-path filters respectively. The slight loss observed in the passband is due to the sin(x)/x hold-function with a first zero at 20MHz. Although the filters can have either a bilinear input stage or an FIR output stage of $(1-z^{-1})$ or $(1-z^{-2})$ for the N-path and pseudo-N-path types respectively, the latter is preferred in view of dynamic-range scaling requirements. This is illustrated by Fig. 6.31, which shows the output level of the integrators within the filter after dynamic-range scaling

for the bilinear input stage case. It is obvious that the bilinear integrator output will saturate well in advance of the other integrators due to the huge gain peak in the centre of the passband. This problem can be circumvented by replacing the bilinear integrator at the input by FIR stage at the output, as illustrated for the pseudo-2-path case in Fig. 6.29b.

6.4.3 Sensitivity and Non-Ideal Factors

Several non-ideal factors affecting the N-path and pseudo-N-path filters are considered next. It is well known that the sensitivity of bandpass filters increases with the Q-factor[10]. For a directly realised narrowband bandpass filter, the Q-factor is approximately $Q_{BP} \approx (2\omega_o/B)Q_{LP}$, where ω_o is the centre frequency of the bandpass response and B is the bandwidth[10]. With $\omega_o >> B/2$ for narrowband bandpass filters, $Q_{BP} >> Q_{LP}$. Thus, as the N-path and pseudo-N-path filters use a lowpass reference, they do not suffer from the problems associated with high Q's as in a directly realised bandpass filter. For instance, transistor spread in the first two designs is 35.8 and in the latter, 68.24.

The overall passband sensitivity of the N-path and pseudo-N-path filters to deviations in the transistor ratios are compared to a conventional, directly realised bandpass filter of equivalent specifications in Fig. 6.32. Superiority is clearly exhibited over the conventional bandpass filter, which apart from having a high overall sensitivity, is extremely sensitive at the passband edges. This is illustrated in Fig. 6.33, which shows the effect on the amplitude responses for a +1% deviation in all the transistor ratios. The amplitude response of the N-path and pseudo-N-path filters are virtually unaffected while distortion of the passband shape, and more seriously, a frequency shift is observed for the conventional bandpass filter.

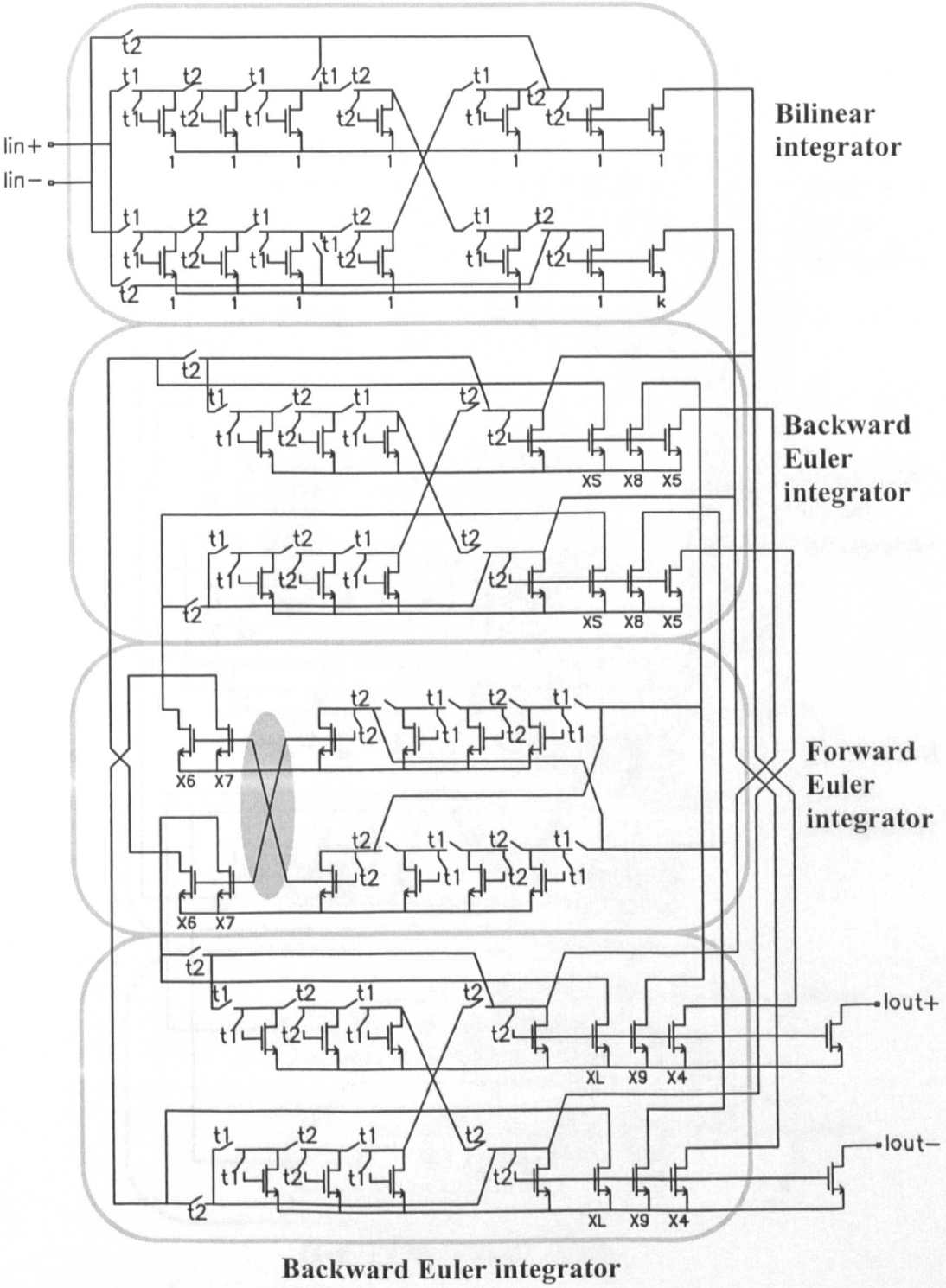


Figure 6.29a Switched-current 6th order pseudo-2-path bandpass filter with bilinear integrator input stage (Version 1)

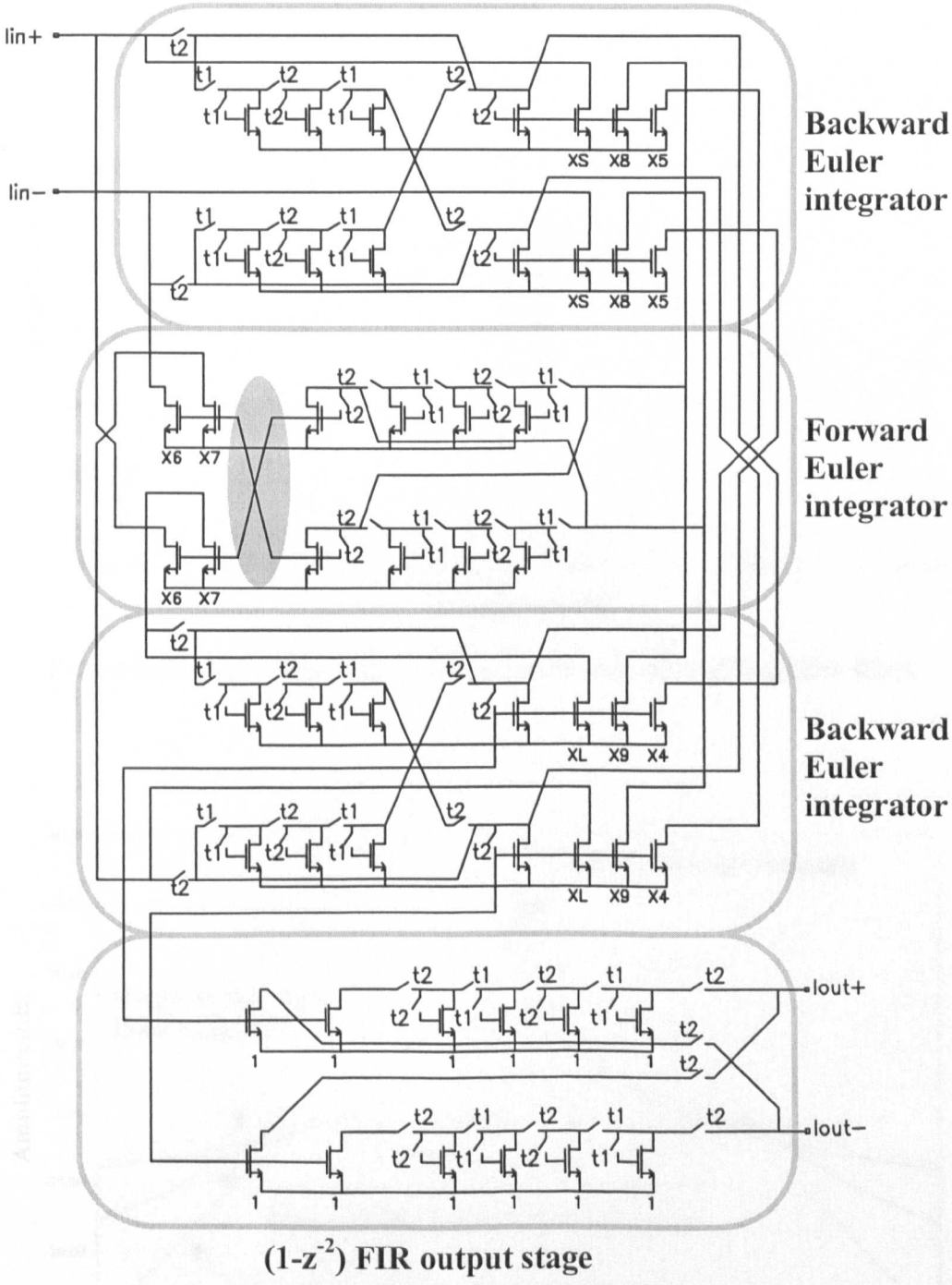


Figure 6.29b Switched-current 6th order pseudo-2-path bandpass filter with $(1-z^{-2})$ FIR output stage (Version 2)

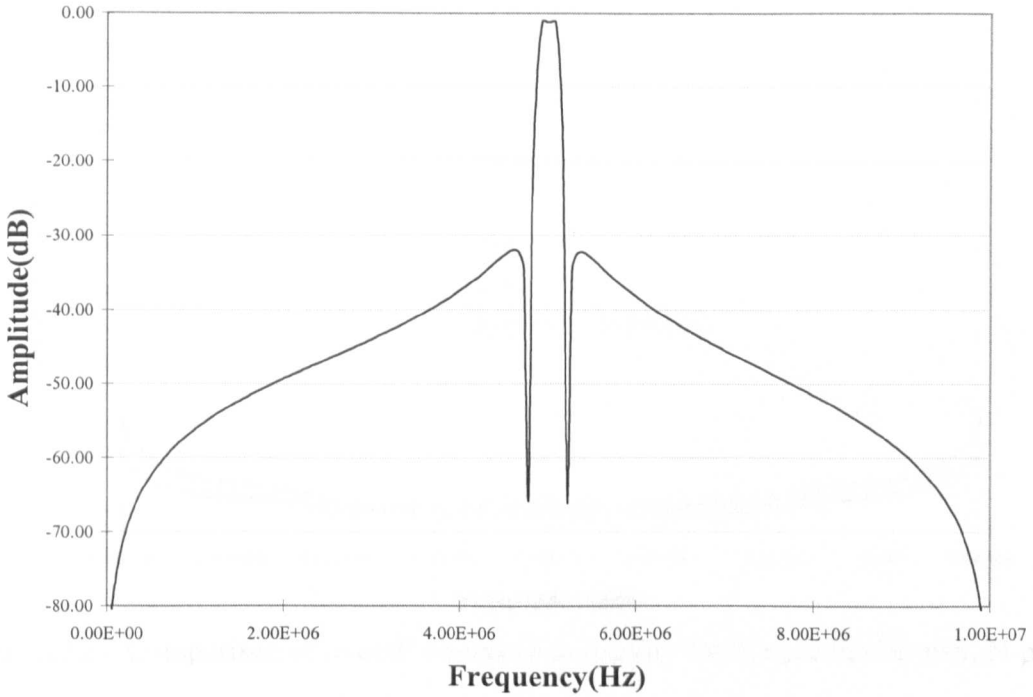


Figure 6.30 Ideal amplitude response of the narrowband bandpass filters

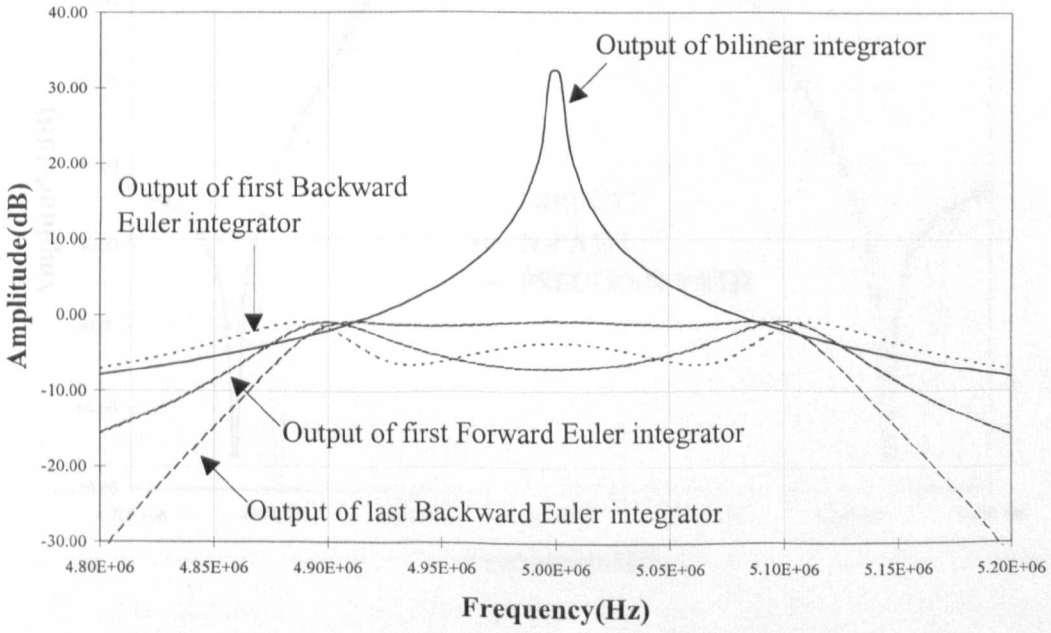


Figure 6.31 Dynamic-range scaled output level of integrators within the pseudo-N-path filter realisation(Version 1) with a bilinear integrator input stage

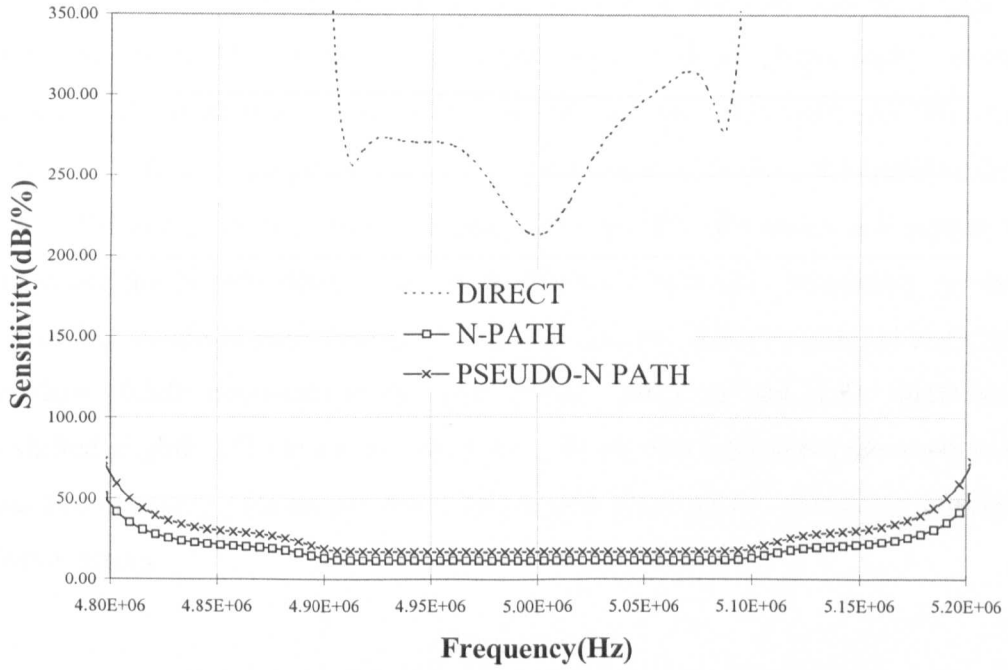


Figure 6.32 Comparison of overall passband sensitivity for the pseudo-N-path, N-path and a direct bandpass realisation

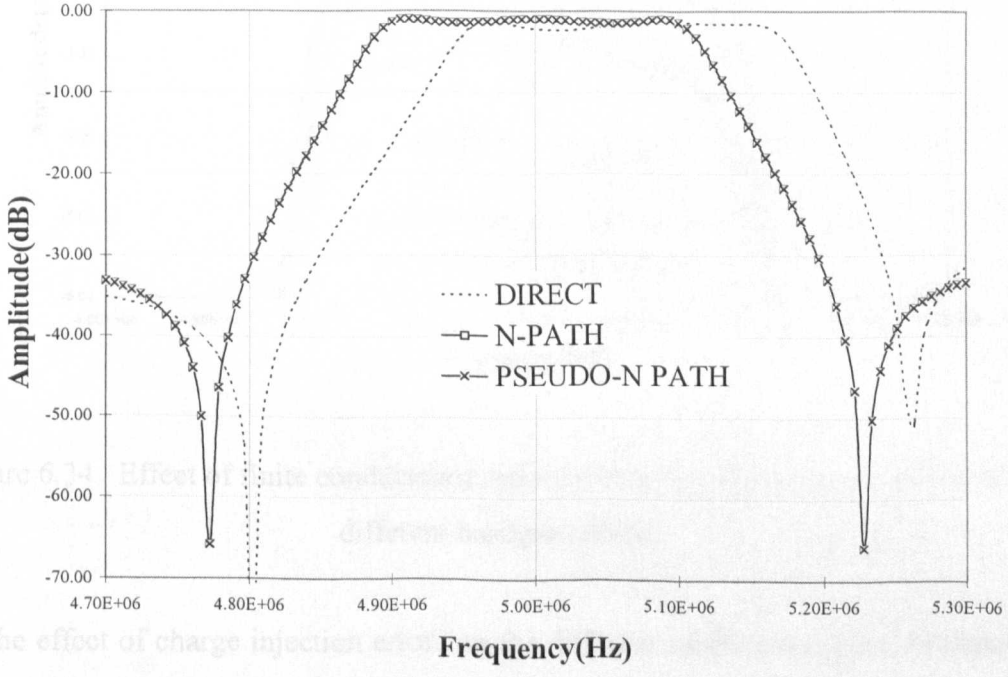


Figure 6.33 Effect of +1% deviation in transistor coefficients on amplitude responses

Pseudo-N-path SC filters are known to be particularly affected by the finite gain of the amplifiers[3,5]. In SI, this is equivalent to the effect of finite output/input conductance ratio (g_O/g_m) of the transistors, which should ideally be zero. The different filter versions were simulated with $\varepsilon_g = -2g_O/g_m$ set at 0.1%. The simulated amplitude responses shown in Fig. 6.34. Version-2 of the pseudo-N-path filter suffers the most attenuation in the passband while the N-path filter is the least affected. It is also interesting to note that version-1 of the pseudo-N-path filter is more robust that the direct realisation and differs by only less than -0.5dB compared to the N-path filter. The passband of the direct bandpass filter is shifted slightly off the centre frequency. In all, this highlights the need to realise the actual circuits using gain enhancement techniques and memory cells[8] to minimise the transmission errors.

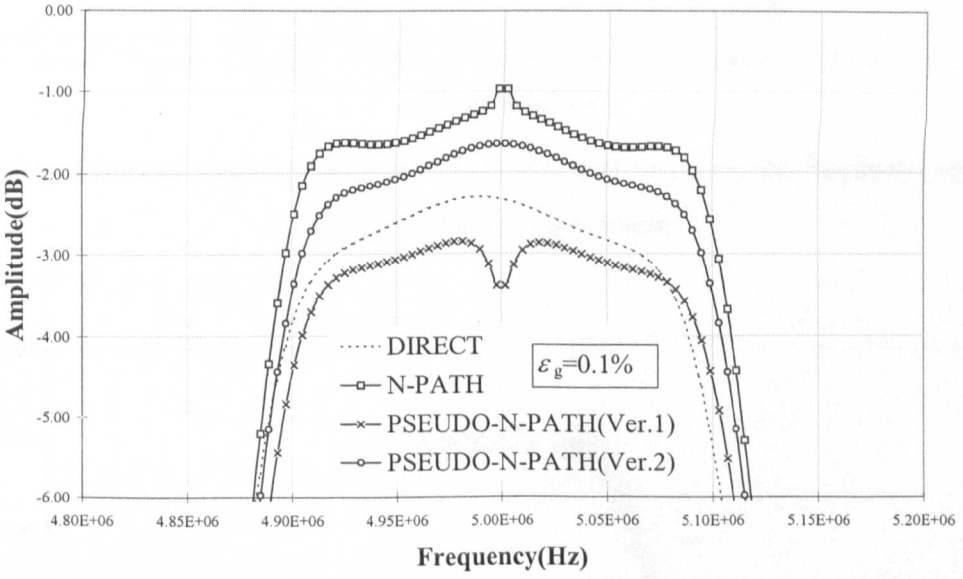


Figure 6.34 Effect of finite conductance ratio errors on the frequency response of the different bandpass filters

Next, the effect of charge injection errors on the different realisations were simulated with ε_c = 0.1%. The results in Fig. 6.35 indicate a superior N-path filter while the other realisations are -0.5dB lower in comparison. This again illustrates the weakness of circulating-delay type pseudo-N-path structures to cumulative errors against the N-path design. Error correction memory cells[8] used in conjunction with dummy transistors

should sufficiently reduce the injected charge, as will be demonstrated in the following section for a cascoded S^2I memory cell with $\varepsilon_c < 0.05\%$.

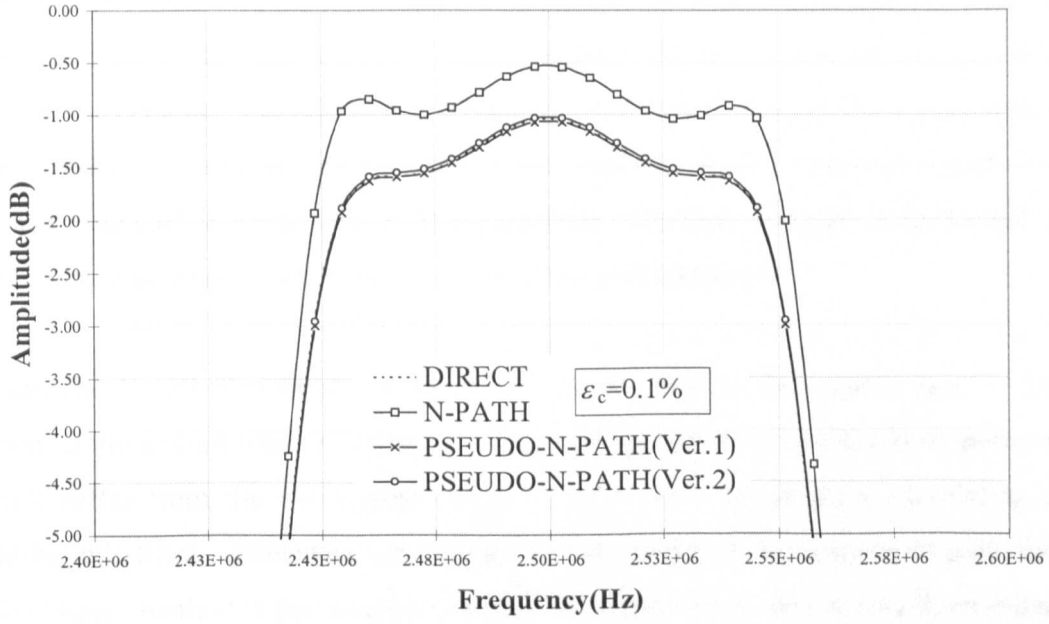


Figure 6.35 Effect of signal dependent charge-injection errors on the frequency response of the different bandpass filters

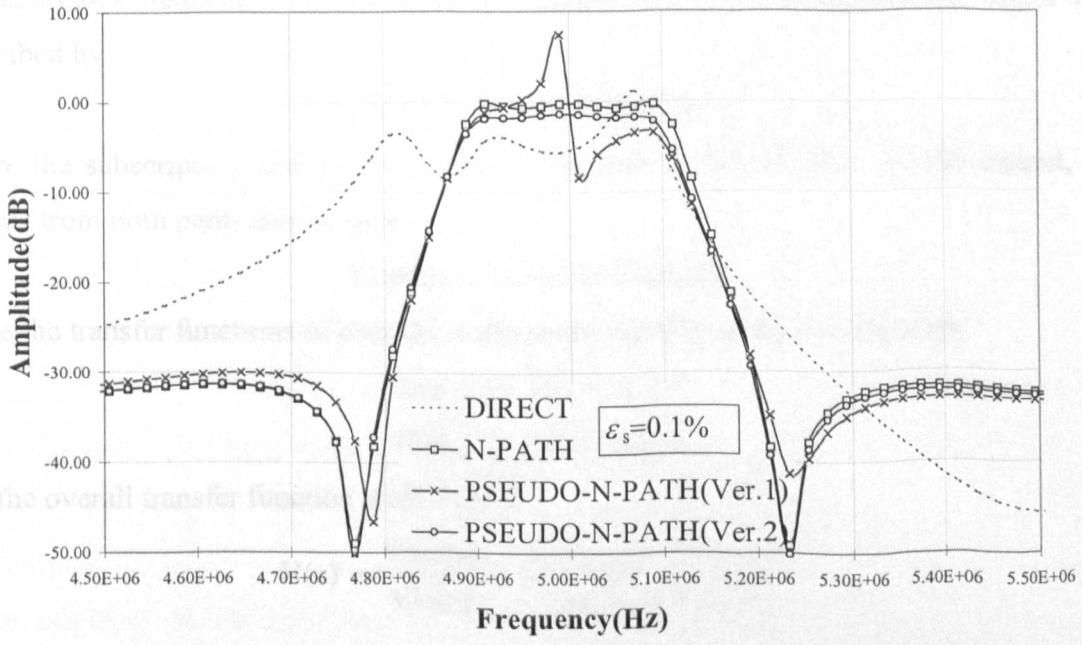


Figure 6.36 Effect of settling errors on the frequency response of the different bandpass filters

Effect of settling errors with $\varepsilon_s = 0.1\%$ can be seen in Fig. 6.36. The frequency response of the direct realisation is severely distorted, affecting both the passband and stopband, rendering the design virtually useless. The distortion in the passband of the version-1 pseudo-N-path filter is caused by a shift in the resonant peak of the bilinear input stage, resulting in mismatched cancellation. This is another negative aspect of having a bilinear integrator at the input. The difference in having a $(1-z^{-2})$ FIR stage at the output instead of the input bilinear integrator can be seen in the response of the version-2 pseudo-N-path filter, where no such distortion exist in the passband. The best response is due to that of the N-path filter, where both distortion and attenuation are minimum.

Thus far, the N-path realisation seems to deliver the best overall performance. This is expected as the overall transfer function is the same as that of each individual path, which does not suffer from the cumulative errors as much as a single path, circulating delay pseudo-N-path filter. However, one important advantage of the pseudo-N-path method over the N-path method is the absence of mirror-frequency noise that results from mismatch between path filters. The generation of mirror-frequency noise imposes a major limitation on the viability of N-path realisations, and will thus be examined next. From Fig. 6.28, it can be seen that for a 2 path structure, the overall sampling frequency, Fs, is twice that of the path clock frequency, Fsp. The input sequence Vin is a time-interleaved, vector sum described by

$$Vin(z) = Vin_1(z)+Vin_2(z)$$

where the subscripts 1 and 2 denote path 1 and path 2 respectively. At the output, the signals from both paths sum to give

$$Vout(z) = Vout_1(z)+Vout_2(z)$$

Since the transfer functions of both the paths are nominally equal, we can write

$$Vout_1(z) = H(z)Vin_1(z)$$

$$Vout_2(z) = H(z)Vin_2(z)$$

and the overall transfer function works out to

$$H(z) = \frac{Vout(z)}{Vin(z)} = \frac{Vout_1(z) + Vout_2(z)}{Vin_1(z) + Vin_2(z)}$$

Consider the case when there is asymmetry between the path filters. A mismatch error in path 2 will alter its transfer function to become $H_2(z) = (1+\varepsilon)H(z)$, which gives

$$\frac{\text{Vout}(z)}{\text{Vin}(z)} = \frac{H(z)\text{Vin}_1(z) + (1+\varepsilon)H(z)\text{Vin}_2(z)}{\text{Vin}_1(z) + \text{Vin}_2(z)}$$

This can be expressed as

$$\text{Vout}(z) = H(z)[\text{Vin}(z) + \varepsilon \text{Vin}_2(z)]$$

When both paths are matched, ε=0, and Vout(z) = H(z)Vin(z). Since each individual path is clocked at the lower sampling frequency of Fsp, a mismatch in the gain of path 2 thus generates attenuated spectral content at $nF_{SP} \pm f_{in}$, where (n=1, 2, ...,$\lceil N/2 \rceil$), $\lceil N/2 \rceil$ denotes the integer part of N/2 and f_{in} is the input signal frequency[10]. Ideally, these signals are equal in magnitude and cancel out due to a phase shift of π for a 2-path structure. Fig. 6.37 shows the characteristics of mirror-frequency rejection for the N-path and pseudo-N path filters.

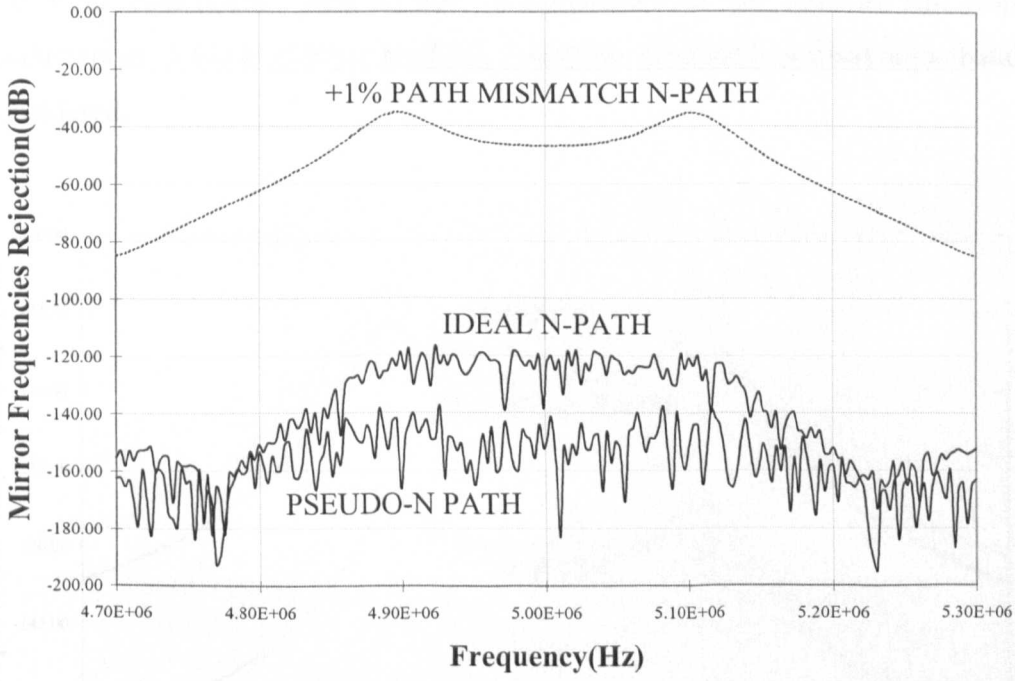


Figure 6.37 Mirror frequencies rejection in the vicinity of the passband region

Input signal frequency was swept from 4.7MHz-5MHz and 5MHz-5.3MHz while plotting the output from 5MHz-5.3MHz and 4.7MHz-5MHz respectively. Under perfect matching conditions for the N-path filter, the rejection in the passband is -120dB. This level of rejection deteriorates drastically to about -40dB when a mismatch of +1% is introduced in one of the path filters. When the structure of the path filter is complex, as in this case of a

third order z→-z transformed filter, the relationship between mismatch and the level of rejection is difficult to quantify. This is because the magnitude response sensitivity of the different components is topology dependent. However, for the simple case when mismatch is directly related to gain, such as for scaled output mirror transistors, the level of rejection is determined by $20\log_{10}(\varepsilon/N)$. Thus, if the passband sensitivity is low, as in this case, the level of mirror frequencies rejection can be approximated by $20\log_{10}(0.01/2)$ = -46.02dB for a 0dB reference level(Fig. 6.37). Although no path mismatches are possible in the pseudo-N-path filter since there is only one physical path, its rejection characteristic is plotted for comparison, this shows a level of -140dB.

Finally, noise simulations were performed to compare the different filters. A $1nA/\sqrt{Hz}$ drain-referred noise current was used as a unit reference. The noise generators associated with the filter coefficients were scaled in proportion to the root of the respective transconductances. Effects of noise foldback within the arbitrarily defined noise-bandwidth were considered.

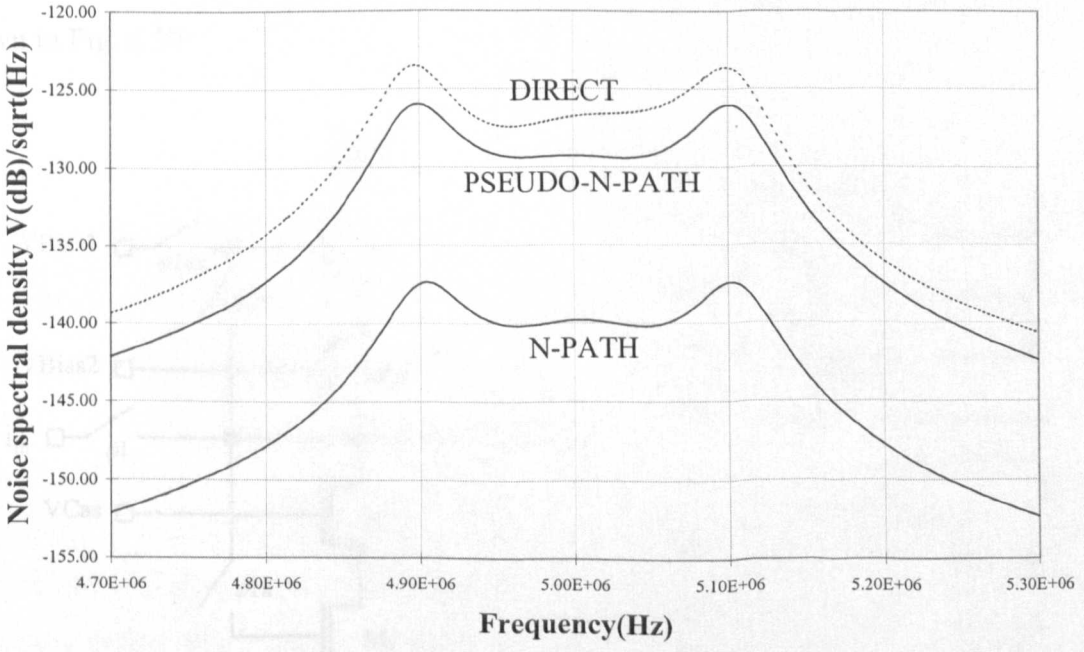


Figure 6.38 Simulated noise spectral densities with an arbitrary, fixed noise-bandwidth for the pseudo-N-path, N-path and a direct bandpass realisation

Fig. 6.38 shows the typical simulated noise spectral densities comparing the N-path, pseudo-N-path and a conventional bandpass filter. The direct realisation has the highest noise level within the passband while the N-path filter has a noise level that is about 11dB lower compared to the pseudo-N-path filter.

6.5 CIRCUIT IMPLEMENTATION ISSUES

6.5.1 Memory Cell

The first step towards a circuit level implementation is to design an optimised memory cell. As seen from the simulations in the previous section, the non-ideal errors will have to be kept well below 0.1% to achieve a reasonably accurate response. An S^2I[12] type memory cell was chosen to minimise both clock-feedthrough/charge-injection errors. Dummy transistors were attached to both the coarse and fine sampling switches to further reduce the injected charge. To minimise finite conductance ratio errors, the output resistance of the memory cell was increased using fixed bias cascode transistors. The memory cell is shown in Fig. 6.39.

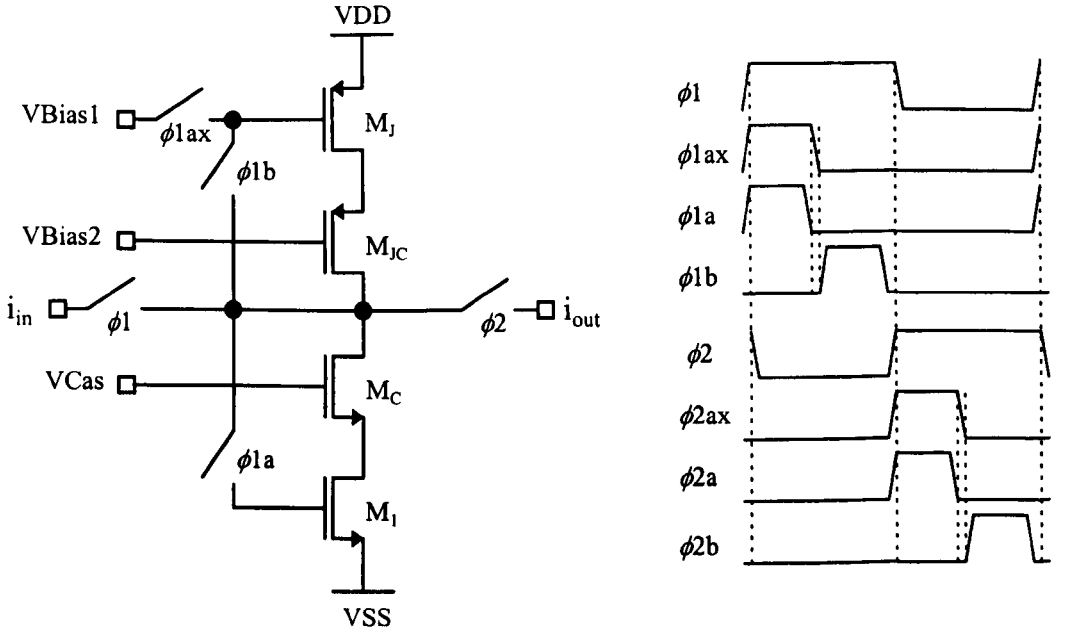


Figure 6.39 Cascoded S^2I memory cell and clock waveforms

The current transfer clock phases are overlapping to minimise transient glitches while the voltage sampling clock wave forms have to be non-overlapping. Designing an optimised cell is a complicated procedure involving many trade-offs[8] and careful considerations have to be given to ensure that the transistors stay saturated at all times. For the transistors in the bias chain M_J and M_{JC}, the critical condition arises during the 'coarse' sampling phase (ϕ1a) when the input signal is at a maximum:

$$VDD\text{-}V_{gs1} > V_{dsatJ}+V_{dsatJC}$$

$$VDD\text{-}[V_T+(V_{gs}\text{-}V_T)_1\sqrt{1+m}\,] > (V_{gs}\text{-}V_T)_J+(V_{gs}\text{-}V_T)_{JC}$$

where the modulation index is defined as the ratio of the input current to bias current, m = i_{in}/J. Therefore, the transistors in the bias chain stay saturated provided

$$(V_{gs}\text{-}V_T)_J < VDD\text{-}V_T\text{-}(V_{gs}\text{-}V_T)_1\sqrt{1+m}\text{-}(V_{gs}\text{-}V_T)_{JC}$$

A second critical condition occurs during the hold phase(ϕ2) when the first memory cell is sinking the maximum current from a second memory cell connected in cascade[8]. Thus in phase ϕ2, the second memory cell will be diode connected and have a minimum drain current. This minimum gate voltage of the second cell, V_{gs2}, will have to be high enough to ensure transistors M_1 and M_C of the first cell, which are sinking maximum current, stays saturated:

$$V_{gs2} > V_{dsatC}+V_{dsat1}$$

$$V_T+(V_{gs}\text{-}V_T)_2\sqrt{1-m} > \sqrt{1+m}\,[(V_{gs}\text{-}V_T)_1+(V_{gs}\text{-}V_T)_C]$$

Therefore, in this situation, transistors M_1 and M_C of the first cell stay saturated provided

$$(V_{gs}\text{-}V_T)_1 = (V_{gs}\text{-}V_T)_2 = (V_{gs}\text{-}V_T) \le \frac{V_T-(V_{gs}-V_T)_C\sqrt{1+m}}{\sqrt{1+m}-\sqrt{1-m}}$$

The supply voltage VDD was set at 3V (VSS=0V). VBias1 was chosen to be mid-rail at 1.5V, which will ensure that the current summing node stays close to 1.5V during the 'fine' correction phase, ϕ1b. Using models from an AMI double metal 1.0μm digital CMOS process, the transistor dimensions designed for a bias current of approximately 100μA and a maximum modulation index of m = ±0.8 is given in Table 6.3. The memory cell was simulated in HSPICE and the normalised DC transfer characteristic curves are shown in Figure 6.40.

Table 6.3 Specifications of the SI memory cell

Transistors	(W/L) in μm
Bias current, M_J	42/2
Bias cascode, M_{JC}	80/1
Memory cascode, M_C	30/1
Main memory, M_1	50/4
Current transfer switches	20/1
Sampling switches	3/1
Bias current	100μA
VDD(VSS=0V)	3V
VBias1	1.5V
VBias2	1.2V
VCas	1.8V

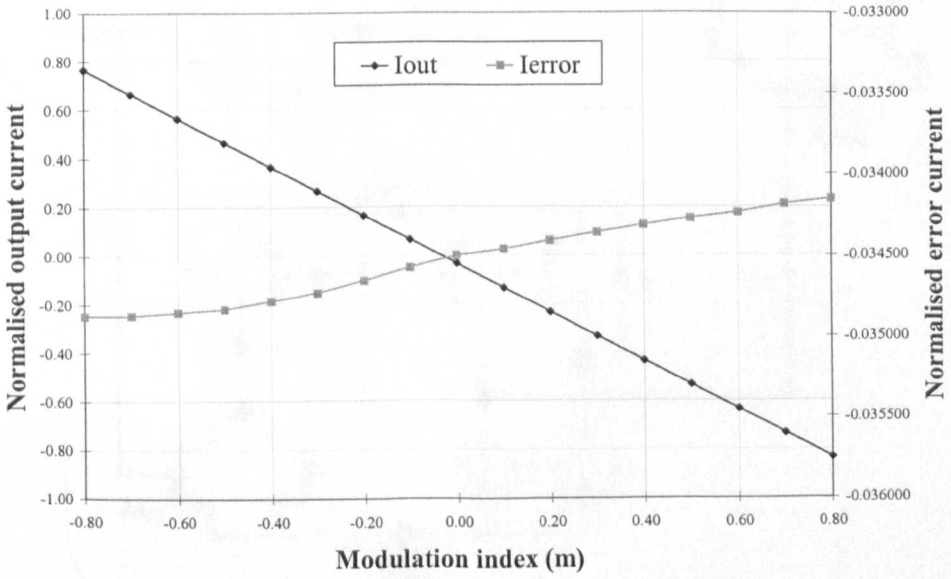


Figure 6.40 DC transfer characteristics of the cascoded S^2I memory cell

6.5.2 Common-mode Control

The proposed N-path and pseudo-N-path cells are all fully-balanced and therefore require some form of common-mode control circuitry. One option is a common-mode feed-forward(CMFF) circuit[15] as shown in Fig. 6.41. The circuit operates by sensing the differential gate voltage at the output of the integrators using half size transistors M_{CP} and

M_{CN}. The ideal common-mode current drawn will be 2(0.5J) = J when only differential signals are present. This current is then mirrored by the PMOS transistor M_{MIR} to two outputs biased by currents of magnitude J. Thus, ideally, both the generated common-mode currents I_{CM} will be zero. When undesired common-mode signals are present, they will be sensed by M_{CP} and M_{CN} and I_{CM}s of the appropriate polarity generated to cancel them out when both the outputs of the integrator and CMFF circuit are summed.

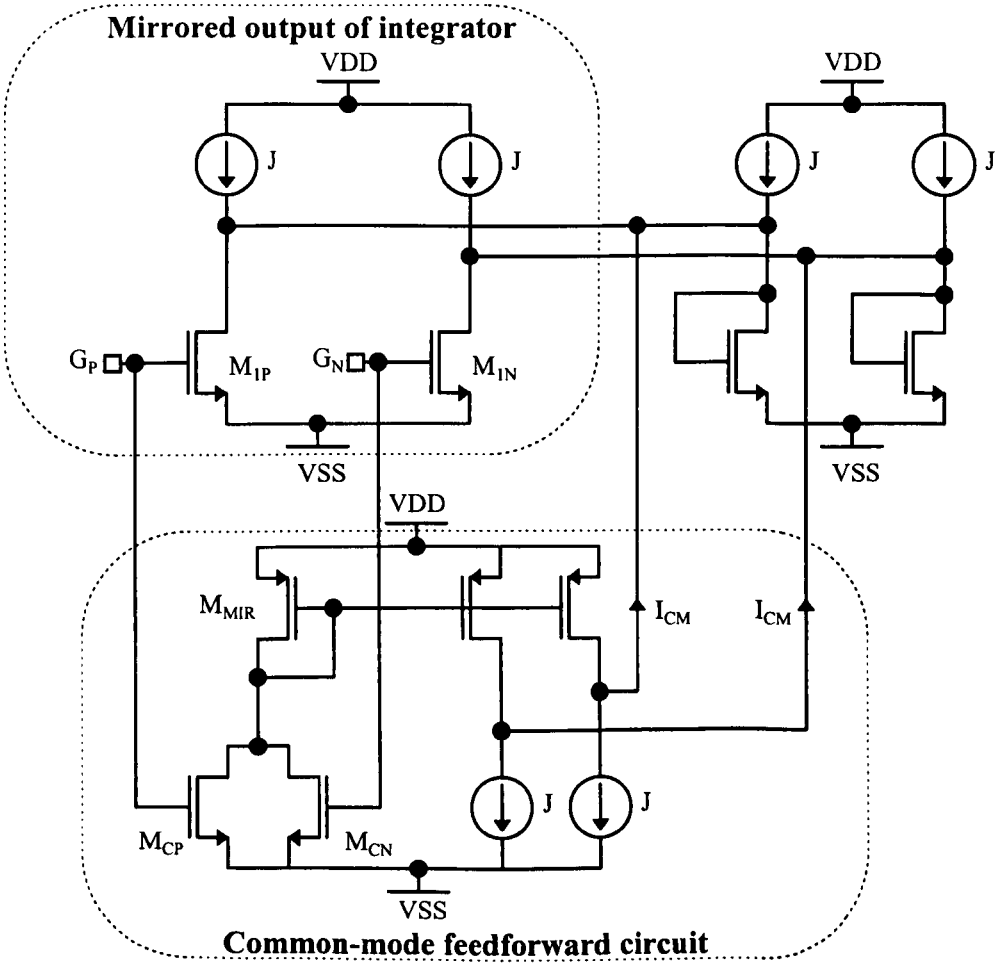


Figure 6.41 Common-mode feedforward correction scheme

There are several disadvantages with this scheme. Firstly, the common-mode signals that are present in the integrator itself are not eliminated. This might shift the bias point of the memory cells and cause some transistors to cutoff if the common-mode signals become too large. Secondly, correction of common-mode levels is afforded only to one output balanced pair. To correct more than one output, which is usually the case for filters with

multiple coefficients, current mirrors will be required for each additional output. Another option is to use a common-mode feedback circuit as shown in Fig. 6.42.

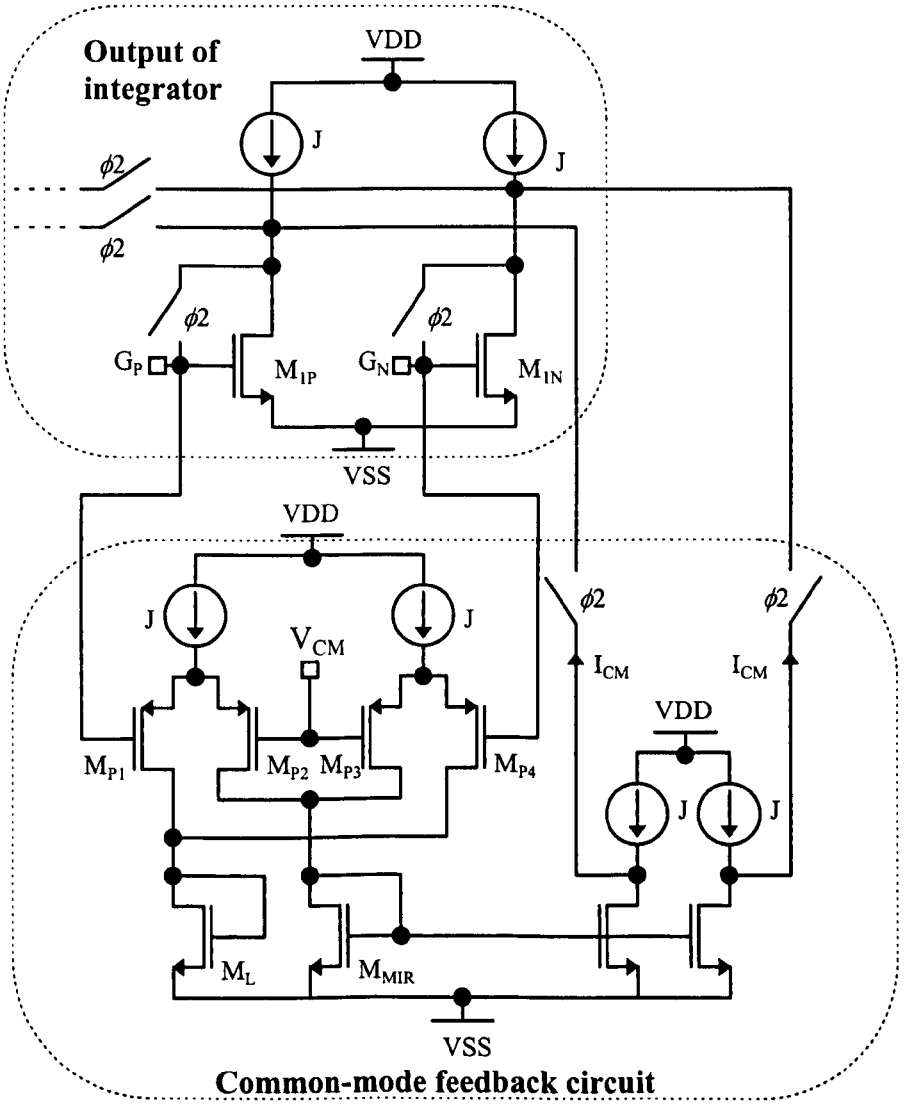


Figure 6.42 Common-mode feedback correction scheme

Transistors M_{P1} to M_{P4} form two PMOS differential pairs biased by currents J. V_{CM} sets the desired common-mode voltage level, which is usually the diode-connected memory cell gate voltage with zero input. With only differential signals present, an increase in current in M_{P1} is met by a proportional decrease in M_{P4}. Thus, equal currents flow in M_{P1} and M_{P3} and similarly, in M_{P2} and M_{P4}. The current that flows to the load M_L and the current mirror M_{MIR} are thus equal to J. Since the two mirror outputs are biased by currents of magnitude J, the output currents of the CMFB circuit, I_{CM}, are ideally zero. If the common-mode level

is increased during sampling(phase $\phi 2$), this will be reflected by an increase in the common-mode gate voltages of G_P and G_N. This will be sensed by M_{P1} and M_{P4}, which reduces the current to the load M_L while increasing the current to M_{MIR}. The increase in mirrored current will make both I_{CM}s negative, reducing the common-mode currents to transistors M_{1P} and M_{1N} of the integrator. Therefore, the current that is sampled is free from unwanted common-mode signals. Any additional mirror transistors that are connected to gates G_P and G_N to realise filter coefficients will also be free from common-mode signals. Thus, only one CMFB circuit is needed at the output of each integrator to ensure that no common-mode signals remain in the integrator and get propagated to subsequent circuits. For the differential pairs, high output impedance cascodes are required for the bias current sources to maintain a high common-mode rejection ratio(CMRR). A sufficiently large CM loop gain has to be provided by the transconductance of the differential pairs to ensure effective feedback correction. To adapt this to S^2I cells of Fig. 6.39, a complementary type CMFB circuit will be required to operate during the 'fine' sampling phases($\phi 1b$ and $\phi 2b$).

6.5.3 A 6th Order Pseudo-2-Path SI Bandpass Filter

The Version-2 pseudo-2-path filter structure of Fig. 6.29b was designed using cascoded S^2I cells of Fig. 6.39 and CMFB circuits of Fig. 6.42 are attached to the outputs of the three constituent integrators. Before proceeding with simulation, the coefficient transistors at each integrator output has to be settle-scaled to ensure their combined gate areas are the same as that of a single optimised cell while realising the required filter coefficient ratios. For the optimised unit memory cell of Fig. 6.39, W_{M1opt}=50μm and L_{M1opt}=4μm. This gives the ratio $R_{opt} = W_{M1opt}/ L_{M1opt} = 12.5$ and area $A_{opt} = W_{M1opt}L_{M1opt} = 200\mu m^2$. To find the scaled dimensions W_{M1} and L_{M1} for the transistors connected at the output of the first Backward Euler integrator, the two inequalities that must be satisfied are $A_{opt} = W_{M1}L_{M1}(1+X_S+X_8+X_5)$ and $W_{M1} = R_{opt}L_{M1}$. Therefore,

$$W_{M1} = \sqrt{\frac{A_{opt}R_{opt}}{1+X_S+X_8+X_5}} \quad \text{and} \quad L_{M1} = \frac{W_{M1}}{R_{opt}}$$

and the scaled widths of the coefficient transistors are $W_{M1}X_S$, $W_{M1}X_8$ and $W_{M1}X_5$, with a common gate length of L_{M1}. This procedure has to be repeated for the bias transistors too,

as they sample in the 'fine' memory phases(ϕ1b and ϕ2b). The outputs of the remaining integrators have to be similarly scaled.

The circuit was simulated in HSPICE by impulse excitation and the output was processed by FFT in MATLAB. The reason for adopting this approach is that the passband is centered around a quarter of the sampling frequency. This low signal-to-clock frequency ratio makes the peak-to-peak output signal levels difficult to determine if the conventional way of performing transient sweeps at different input signal frequencies were carried out. The response obtained is plotted together with a SCNAP4 simulation in Fig. 6.43. Charge-injection models with an error of ε_c = 0.045%, obtained from the gradient of an approximated best-fit line to the error characteristics in Fig. 6.40, was used in the SCNAP4 simulation.

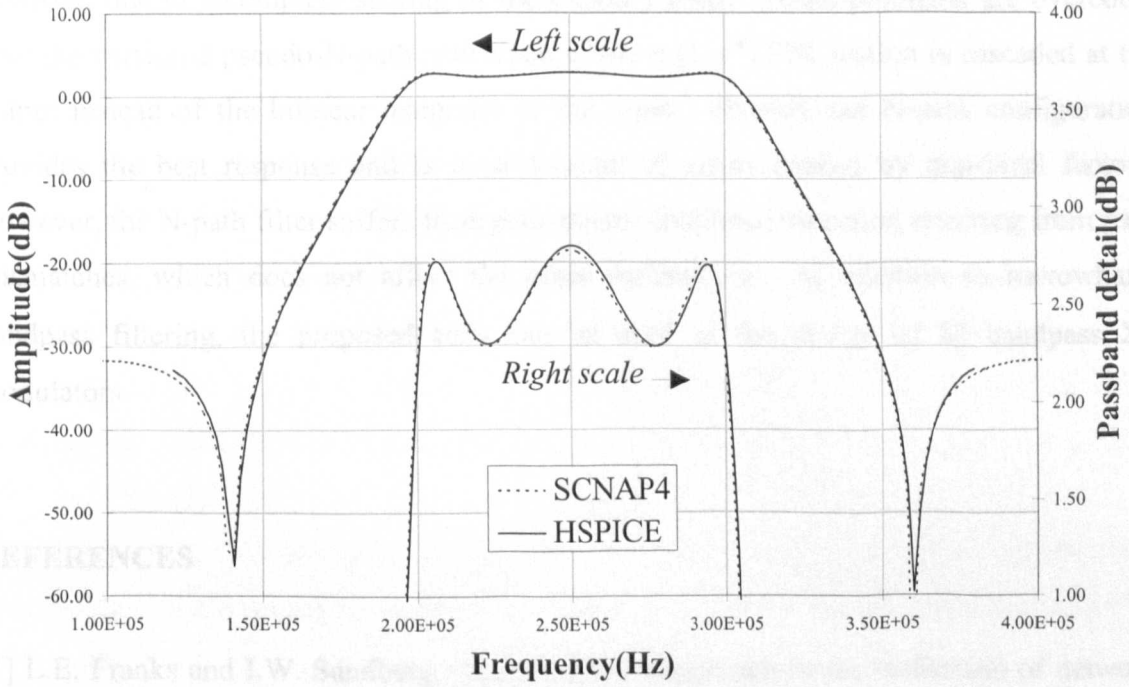


Figure 6.43 Simulated frequency response of a 6th order pseudo-2-path(Version-2) bandpass filter

6.6 CONCLUSIONS

Novel switched-current N-path and pseudo-N-path cells have been presented which perform the $z \rightarrow -z$ and $z \rightarrow -z^2$ transformations respectively. These allow the design of bandpass filters from lowpass reference filters by a simple one-to-one cell replacement procedure. Bilinear-transformed structures with transmission zeros are accommodated, as illustrated by examples of 6th order narrowband bandpass filters that require only standard bi-phase clocks. There is no clock-feedthrough noise in the passbands of the resulting bandpass filters. Detailed analyses of the structures for both ideal and non-ideal conditions have been given and verified by simulations. The effects of finite conductance ratio and charge-injection errors are to attenuate the gain without affecting the resonant frequency. It was also shown that settling errors result in both attenuation and lowering of the resonant frequency. Of the two pseudo-N-path filter realisations, having a bilinear integrator at the input prevents proper scaling for maximum dynamic range and produces distortion in the passband due to incomplete settling of the memory cells. These problems are overcome with the version-2 pseudo-N-path realisation where a $(1-z^{-2})$ FIR section is cascaded at the output instead of the bilinear integrator at the input. Overall, the N-path configuration provides the best response and is most tolerant of errors caused by non-ideal factors. However, the N-path filter suffers from poor mirror-frequency rejection resulting from path mismatches, which does not affect the other realisations. In addition to narrowband bandpass filtering, the proposed cells can be used in the design of SI bandpass $\Sigma\Delta$ modulators.

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CHAPTER 7:
CONCLUSIONS

The work presented in this thesis is about the design, synthesis and software development of switched-current filtering systems. The aim as stated in the beginning was to "investigate and develop novel switched-current circuits and building blocks and to study their suitability as filtering systems for implementation into the filter and equaliser compiler XFILT". The extent to which these objectives were achieved and some suggestions for future avenues of research will now be discussed in this final chapter.

7.1 DISCUSSION OF RESULTS AND CONCLUSIONS

In the design of high order switched-current filters, apart from being constrained to the use of low sensitivity ladder structures, component value spread and circuit area could be deciding factors concerning the feasibility of a realisation. Improved SI filter structures have been obtained by making modifications to existing SI filters derived by general matrix methods. The modified Left-decomposition designs were shown to have improved sensitivity characteristics over the conventional designs. Existing Right-decomposition type designs are preceded by a bilinear integrator. This was shown to make dynamic-range scaling impossible as the bilinear integrator will saturate well before the integrators in the filter. Simple modifications were made to the input arrangements to circumvent this problem. For the design of very high order SI filters, a prototype manipulation technique that is applicable to matrix-derived bilinear-LDI structures was used in the design of a 21st order SI lowpass filter with a spread and area of 13.63 and 3266.7 units respectively. This represented a reduction in the spread of 99.94% and area of 99.83% from an otherwise unrealisable design. For wideband filter design, SI structures derived by the LU-UL and UL-LU decompositions were introduced. These were shown to have the lowest average sensitivity in the passband for large relative bandwidths of typical 6th order bandpass designs. The UL-LU design was also shown to have superior sensitivity and implementation efficiency for lowpass filters.

There are very few switched-current allpass filters reported in the literature. Existing ones used for group delay equalisation have either been implemented using cascade

biquads or Euler integrator based ladder structures[2,6]. The proposed allpass filters are based on bilinear integrators. The advantages are that bilinear integrators do not suffer from excess phase lag and can be directly used to realise bilinear-transformed filters. The derivation procedure can proceed from either the s-domain or directly in the z-domain via respective continued-fractions expansions. Matrix-methods are then applied to derive the different SI allpass structures. It was shown that the amplitude response is completely insensitive to deviations in the elements of the singly-terminated reactive ladder, but only sensitive to the remaining elements that make up the allpass filter. From comparisons of different realisations, the bilinear integrator based design and cascade biquad design generally have the best amplitude and group delay sensitivities respectively, while the Euler integrator based design fared poorly. Both the gain and group-delay are however affected by non-ideal factors. For finite conductance ratios, the most affected design is the single-sampling bilinear integrator based structure. The group-delay response of the cascade biquad design is least affected. For small-signal signal dependent charge injection errors, the group-delay response of the Euler integrator based design is most affected, while overall, the double-sampling bilinear integrator based design is least affected. For settling errors, the amplitude response of both the Euler integrator and the single-sampling bilinear integrator based designs are more affected than the cascade biquad design. The group-delay response of all the designs are relatively robust to settling errors.

Novel switched-current decimators and interpolators, based on polyphase FIR networks and bilinear transformed ladder structures, have been proposed. These are derived by a multirate transformation procedure that allows the final structure to operate at the lower sampling frequency. Available time for settling is thus maximised and low sensitivity in the passband is maintained by the ladder structure. Additional zeros created by the FIR network are used to cancel the undesired poles in the stopband. Any shift caused by component deviations will result in partial cancellation and a higher level of aliasing to the passband. Of the two decimator structures, the FIR-IIR Cascade(FIC) version possesses superior sensitivity characteristics but requires more delay circuits. The Multiple Feed-In(MFI) decimator suffers from higher sensitivity due to a closer degree of coupling between

the FIR and ladder structures, but requires a lower number of delays to implement. Complementary interpolator structures are derived by direct transposition, avoiding the need for redesign. However, the resulting topologies are more sensitive than the decimators, especially in the stopband. A major drawback of this design procedure is the need to derive the symbolic transfer function, the terms of which are well known to increase rapidly with system order and decimation/interpolation factor. This makes the task of designing systems of high order or decimation/interpolation factor a formidable challenge.

A family of novel fully-balanced N-path and pseudo-N-path SI cells has been proposed for the design of narrowband bandpass filters. These are based on the transformation of Forward Euler, Backward Euler and bilinear integrators. The N-path cells perform the $z \rightarrow -z$ transform and converts an integrator into a differentiator. Two of these cells connected in parallel have to be clocked in a time interleaved manner to obtain a 2-path resonator. The pseudo-N-path cells perform the $z \rightarrow -z^2$ transform, based on the circulating delay principle and convert an integrator directly into a resonator. Since only one physical path exists, no mirror-frequency noise components are generated. In both the N-path and pseudo-N-path cases, the centre of the passband is fixed at a quarter of the clock frequency, providing frequency stability for narrow bandpass responses. In addition, clock-feedthrough noise in the passband is avoided. From the analyses and simulations of non-ideal effects, it was shown that both finite conductance ratios and small-signal charge injection errors result in attenuation without any frequency shifts. Settling errors however, cause both attenuation and a lowering of the resonant frequency. A $(1-z^{-2})$ FIR section was also introduced to replace the input bilinear resonator that prevents proper dynamic range scaling for Right-decomposition type designs. The simulated results of different 6th order bandpass filters indicate superior performance from the N-path design. However, it suffers from poor rejection of mirror-frequencies resulting from path mismatches which does not exist for pseudo-N-path designs. This work represents a first attempt to systematically design N-path and pseudo-N-path SI filters.

Many of the switched-current circuits, building blocks and techniques described herein have to a large extent been implemented into the filter and equaliser compiler XFILT.

In the present state of affairs, the switched-current technique has not made a significant impact on the microelectronics industry. State-of-the-art SI circuits have yet to demonstrate the same level of linearity and noise performance as that of their switched-capacitor(SC) counterparts. In addition, continual research effort on low-voltage[21] and digital process compatible[22] SC circuits will further erode the acceptance rate and penetration of SI circuits. The potential of SI circuits for mixed-signal integration has also not been fully realised due to a lack of systematic design tools. In all, these highlight the need and vast scope for further research of the switched-current technique.

7.2 RECOMMENDATIONS FOR FUTURE WORK

1. Simple, low order decimators and interpolators with a sampling rate change of an integer factor of 2 were used for illustration in Chapter 5. Examples with higher integer decimation and interpolation factors have been demonstrated[7]. This can be extended to structures that are capable of sampling rate changes with non-integer(rational) factors, which can currently be implemented by cascading decimators and interpolators with different integer decimating and interpolating factors. Complete multirate and narrowband SI filtering systems such as the SPFT[6] filter could be built and demonstrated using the proposed decimators and interpolators. Significant improvements in terms of sensitivity and operating speed can be expected since the proposed structures are based on low sensitivity ladders and operate entirely at the lower clock frequency. Another area worth investigating is multirate design techniques that avoid the need to derive the symbolic transfer function. This would overcome the barrier to high order designs encountered by the present technique. One possibility could be the use of optimisation techniques, such as genetic algorithms, to evolve the coefficients of the structures.

2. The N-path and pseudo-N-path resonators proposed in Chapter 6 could be used in the design of bandpass sigma-delta modulators. In [19], SI bandpass sigma-delta modulators were implemented using resonators where the resonant frequency is sensitive to the feedback factor R. This choice was due to stability constraints. A shift away from the nominal frequency translates directly to a decrease in the signal-to-quantisation noise ratio. The resonators proposed in Chapter 6 can be used instead, where the resonant frequency is locked at a quarter of the sampling frequency provided adequate settling time is afforded for the memory cells. A disadvantage, however, will be the overheads incurred by the common-mode control circuitry required by the fully-balanced configuration.

3. Complex filters[17,18] have magnitude responses that are not restricted to be symmetrical around the zero frequency(DC) axis. This is because the poles and zeros are implemented by complex-valued coefficients, allowing arbitrary location in the z-plane. In comparison, real filters can only implement complex-conjugate poles and zeros, thus constraining their magnitude responses to be symmetrical about DC. Quadrature(I and Q) channels are found in many communication systems. For a prescribed bandpass filter order N, two separate filters will be required as there are two channels, making the total order 2N. By definition, complex filters process signals in phase-quadrature and to realise the same Nth-order bandpass response, a single Nth-order complex filter can be used instead of two separate filters. This will consist of two identical, and coupled real lowpass filters of order N/2. Therefore, compared to the conventional approach, implementation efficiency is doubled, as both area and power dissipation are approximately halved. A similar argument can be extended to the case of quadrature bandpass $\Sigma\Delta$ modulators[20], where in addition, the noise shaping notches can be shifted away from the unused band to be used only in the desired band.

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Starting with equation (3.9) as

$$(1-z^{-1})\left[\frac{2}{T}\mathbf{C}+\frac{T}{2}\left(1+4\frac{z^{-1}}{\left(1-z^{-1}\right)^{2}}\right)\Gamma+\left(1+2\frac{z^{-1}}{1-z^{-1}}\right)\mathbf{G}\right]\mathbf{I}=(1+z^{-1})\mathbf{J} \qquad (A.1)$$

Divide both sides by z^{-1}

$$(\psi^{-1}\mathbf{A}+\phi\mathbf{B}+\mathbf{D})\mathbf{I}=(\psi^{-1}+2)\mathbf{J} \qquad (A.2)$$

where

$\mathbf{A} = (2/T)\mathbf{C}+(T/2)\Gamma+\mathbf{G}$

$\mathbf{B} = 2T\Gamma$

$\mathbf{D} = 2\mathbf{G}$

$\psi = z^{-1}/(1-z^{-1})$

$\phi = 1/(1-z^{-1})$

Factorising $\mathbf{A}=\mathbf{A}_l\mathbf{A}_r$

$$(\psi^{-1}\mathbf{A}_l\mathbf{A}_r+\phi\mathbf{B}+\mathbf{D})\mathbf{I}=(\psi^{-1}+2)\mathbf{J} \qquad (A.3)$$

Multiplying both sids by $\mathbf{A}_l^{-1}$ gives

$$[\psi^{-1}\mathbf{A}_r+(\phi\mathbf{B}+\mathbf{D})\mathbf{A}_l^{-1}]\mathbf{I}=\mathbf{A}_l^{-1}(\psi^{-1}+2)\mathbf{J} \qquad (A.4)$$

Rearranging,

$$\psi^{-1}(\mathbf{A}_r\mathbf{I}-\mathbf{A}_l^{-1}\mathbf{J})=\mathbf{A}_l^{-1}[-(\phi\mathbf{B}+\mathbf{D})\mathbf{I}+2\mathbf{J}] \qquad (A.5)$$

Let intermediate variable $\mathbf{W}$ be defined as

$$\mathbf{W}=\psi^{-1}(\mathbf{A}_r\mathbf{I}-\mathbf{A}_l^{-1}\mathbf{J}) \qquad (A.6)$$

Then, (A.5) becomes

$$\mathbf{W}=\mathbf{A}_l^{-1}[-(\phi\mathbf{B}+\mathbf{D})\mathbf{I}+2\mathbf{J}] \qquad (A.7)$$

Multiplying both sides by $\mathbf{A}_l$,

$$\mathbf{A}_l\mathbf{W}=-(\phi\mathbf{B}+\mathbf{D})\mathbf{I}+2\mathbf{J} \qquad (A.8)$$

Rearranging (A.6) gives

$$\mathbf{A}_r\mathbf{I}=\psi\mathbf{W}+\mathbf{A}_l^{-1}\mathbf{J} \qquad (A.9)$$

Therefore, (A.8) and (A.9) represent a system of two inter-related first order equations in ψ and ϕ; which can easily be implemented using SI Forward and Backward Euler integrators.

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