University of Glasgow

Germanium on silicon photonic devices

Kevin Gallacher

October 2013

A thesis submitted for the degree of

Doctor of Philosophy (Ph.D.)

In the

College of Science & Engineering

School of Engineering

Declaration of Authorship

I, Kevin Gallacher, declare that this thesis titled “Germanium on silicon photonic devices” and the contributions presented in it are my own. I confirm that:

- This work was made wholly or mainly while in candidature for a research degree at this University.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all main sources of help.
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

Signed: _____

Date: _____

Abstract

There is presently increased interest in using germanium (Ge) for both electronic and optical devices on top of silicon (Si) substrates to expand the functionality of Si technology. It has been extremely difficult to form an Ohmic contact to n-Ge due to Fermi level pinning just above the Valence band. A low temperature nickel process has been developed that produces Ohmic contacts to n-Ge with a specific contact resistivity of $(1.6 \pm 0.4) \times 10^{-7}$ Ω-cm^2, which to date is a record. The low contact resistivity is attributed to the low resistivity NiGe phase, which was identified using electron diffraction in a transmission electron microscope. Light emission from Ge light emitting diodes (LEDs) was investigated. Ge is an indirect bandgap semiconductor but the difference in energy between the direct and indirect is small (~136 meV), through a combination of n-type doping and tensile strain, the band structure can be engineered to produce a more direct bandgap material. A silicon nitride (Si_3N_4) process has been developed that imparts tensile strain into the Ge. The stress in the Si_3N_4 film can be controlled by the RF power used during the plasma enhanced chemical vapour deposition. LEDs covered with Si_3N_4 stressors were characterised by Fourier transform infrared spectroscopy. Electroluminescence characterisation (EL) revealed that the peak position of the direct and indirect radiative transitions did not vary with the Si_3N_4 stressors due to the device geometries being too large. Therefore, nanostructures consisting of pillars smaller than a micron were investigated. Photoluminescence characterisation of 100 nm Ge pillars with Si_3N_4 stressors show emission at much longer wavelengths compared to bulk Ge (> 2.2 μm). In addition, the EL from Ge quantum wells grown on Si was also investigated. EL characterisation demonstrates two peaks around 1.55 and 1.8 μm, which corresponds to the radiative recombination between the direct and indirect transitions, respectively. This result is the first demonstration of EL above 1.45 μm for Ge quantum wells. Finally, the fabrication of Ge-on-Si single-photon avalanche detectors are presented. A single-photon detection efficiency of 4 % at 1310 nm wavelength was measured at low temperature (100 K). The devices have the lowest reported noise equivalent power for a Ge-on-Si single-photon avalanche detector (1×10^{-14} WHz$^{-1/2}$).

Publications

Journal papers

K. Gallacher, P. Velha, D. J. Paul, I. MacLaren, M. Myronov and D. R. Leadley (2012). "Ohmic contacts to n-type germanium with low specific contact resistivity." Applied Physics Letters 100(2).

K. Gallacher, P. Velha, D. J. Paul, S. Cecchi, J. Frigerio, D. Chrastina and G. Isella (2012). "1.55 μm direct bandgap electroluminescence from strained n-Ge quantum wells grown on Si substrates." Applied Physics Letters 101(21).

R.E. Warburton, G. Intermite, **K. Gallacher**, D.J. Paul, M. Myronov, D.R. Leadley, N.J. Pilgrim, L.J.M. Lever, Z. Ikonic, R.W. Kelsall, and G.S. Buller (2013).” Ge-on-Si single-photon avalanche diode detectors: Design, fabrication, and characterization at wavelengths of 1310 and 1550nm” IEEE Transactions on Electronic Devices (accepted).

Conference papers

K. Gallacher, P Velha, D. J. Paul, I. Maclaren, M. Myronov, DR. Leadly (2013) “Low Specific Ohmic Contacts to n-type Germanium Using a Low Temperature NiGe Process” The Electrochemical Society, Meeting Abstracts.

P. Velha, **K. Gallacher**, D. Dumas, D Paul, M. Myronov, DR. Leadley. (2013) “Long wavelength > 1.9 um germanium for optoelectronics using process induced strain”. ECS Transactions.

P. Velha, **K. Gallacher**, D. Dumas, D.J. Paul, M. Myronov, DR. Leadley. (2013) “Direct Band-gap Electroluminescence from Strained n-Ge Light Emitting Diodes” ECS Transactions.

K. Gallacher, P. Velha, D. J. Paul, S. Cecchi, J. Frigerio, D. Chrastina and G. Isella (2012). “1.55 μm electroluminescence from strained n-Ge quantum wells on silicon substrates” IEEE Group IV photonics.

P. Velha, **K. Gallacher**, D. Dumas, D.J. Paul (2012). “Direct band-gap electroluminescence from strained n-doped germanium diodes” Conference on Lasers and Electro-Optics (CLEO).

P. Velha, **K. Gallacher**, D. J. Paul, S. Cecchi, J. Frigerio, D. Chrastina and G. Isella (2012). “Tuning the electroluminescence of n-Ge LEDs using process induced strain” IEEE Group IV photonics.

Acknowledgments

First and foremost, I would like to thank my supervisor Prof. Douglas Paul for his support and guidance over the course of my PhD. I am very grateful for all his suggestions and advice even when they sometimes arrived over the course of a few beers.

I would like to thank Dr. Barry Holmes, Dr. Gary Ternant, Dr. Philippe Velha, Dr Antonio Samarelli, and Dr James Grant for all their fruitful discussions that helped me get back on track with the research when things went wrong.

I would like to thank my fellow PhD candidates that have made the last few years a fun time. Especially Dr Christopher Martin and Dr Douglas Macfarlane who provided plenty of banter and distractions that kept me relatively sane.

I need to thank all the staff at the James Watt Nanofabrication centre for ensuring the smooth and efficient running of the cleanroom that allowed me to fabricate the devices for this PhD.

I would like to acknowledge the financial support provided by EPSRC who funded the work presented here.

Many thanks to all my family and friends for all their support during the somewhat stressful last few years. I am especially grateful to my mum and dad who have supported me endlessly over the course of my academic career and continue to do so. Lastly, to Anne I love you very deeply and I am very grateful that you have stuck by me.

Table of Contents

List of Figures

List of Tables

1 Introduction

1.1 Introduction

Integrated circuits (IC) based on silicon (Si) have been revolutionizing the world for more than fifty years. In 1965, Gordon Moore stated that the number of transistors that could be incorporated into ICs would increase at an exponential rate over time [1]. This historical trend is known as “Moore’s law”. The aggressive scaling of metal-on-silicon field effect transistors (MOSFETs) since 1970, has allowed the number of transistors on an IC to double approximately every two years. As transistors have become smaller, they also become cheaper and consume less power. The overall cost of an IC is dependent upon the Si footprint. Therefore, smaller feature size directly corresponds to a reduction in cost. Aggressive scaling has reduced gate lengths such that transistors have also become faster (shorter transit time of carriers) and because of this increase in speed and the number of transistors, it has enabled more functionality per unit area of Si. The industries ability to follow Moore’s law has been the driving force of a virtuous circle as presented in Figure 1.1 [2]. Scaling leads to an improved performance to cost ratio that helps fuel market growth, which in turn leads to more investment into new technologies, which allows more aggressive scaling and thus the cycle repeats.

Figure 1.1. An illustration of the virtuous cycle of the semiconductor industry.

1.2 Transistor scaling

However, as transistor size has continued to be aggressively scaled, the benefits of an increased number of transistors on chip is starting to be outweighed by the increased power dissipation from the passive metal interconnect layers used for data transmission, signalling, and clocking. The increasing amount of metal interconnects for the latest microprocessors has reached the point where faster clock speeds leads to severe heating from the increased power dissipation and thus there is an increase in attenuation from the copper tracks. Therefore, since 2005 there has been a shift away from increasing clock speeds to multi-core architectures to sustain Moore's law with the performance increase now sought from parallelism [3]. Aside from the severe power dissipation there is also a bottleneck from the propagation delay that is resistance-capacitance (RC) related.

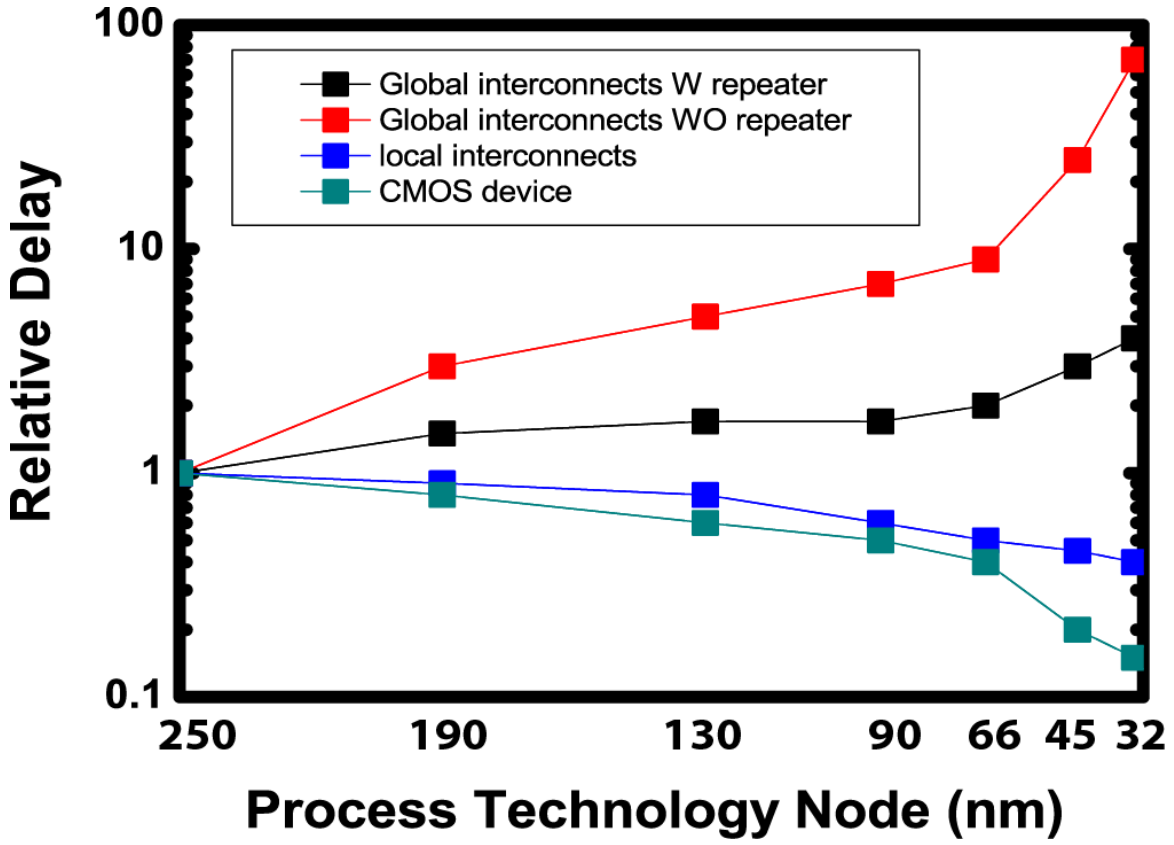

Figure 1.2. A comparison between the gate, local, and global interconnect delays versus the process technology node, plotted from data in reference [3].

This is depicted in Figure 1.2, which compares the delay associated with the transistor, local interconnects, and global interconnects as a function of the process technology node. It is clear that as the technology node decreases the delay is dominated by global interconnects. This is due to the length of the metal interconnects at the global level being fixed by the chip size; therefore, there is an exponentially increase in the RC delay as global interconnects do not keep pace with scaling.

1.3 Multi-core architectures

However, shifting towards a multi-core architecture can only avoid interconnect problems in the short term as more and more cores are added on chip, power dissipation and latency of metal interconnects will become a fundamental roadblock to future performance increases. An example of this bandwidth problem is witnessed from the cell processor contained within Sony's PlayStation 3 games console that contains nine cores on-chip. Chip-to-chip communication between the discrete graphics processor and memory runs at 25 GBps, which is challenging to copper interconnects. This is a situation where optical chip-to-chip interconnects would be beneficial [4]. Therefore, the greatest impact for Si photonics could potentially be optical interconnection between digital electronic chips, as this would address the communication bottleneck of VLSI electronics [5].

1.4 Optical communication

Optical communication is the backbone behind telecommunications systems for long haul networks. This is due to the considerable lower attenuation of optical fibres over long distances compared to copper wire and this has enabled the rapid growth of the internet. In addition, since photons of different wavelengths do not interact with each other this allows a technique called wavelength division multiplexing (WDM) to be employed. The ability to transmit multiple wavelengths of light within a single optical fibre increases the bandwidth substantially. A comparison of the bandwidth provided by a number of electronic and photonic technologies is presented in Figure 1.3. It is clear that there is a market transition

point between communication distance and the required bandwidth. For the displacement of electrical interconnection by optical, the requirement is high bandwidth over short distance applications. The switch to optical communications presents good value when it will provide lower cost compared to increasing the number of parallel electronic channels. The MIT Microphotonics roadmap suggests this occurs around 1.2 $Gbits^{-1}m^{-1}$ [6]. It is clear from Figure 1.3 that the bus technologies used on the computer backplane and in display videos are areas that could benefit the most from the improved performance by optical communication as well as SDRAM, which is at present using multiple parallel channels in the bus to achieve the present performance.

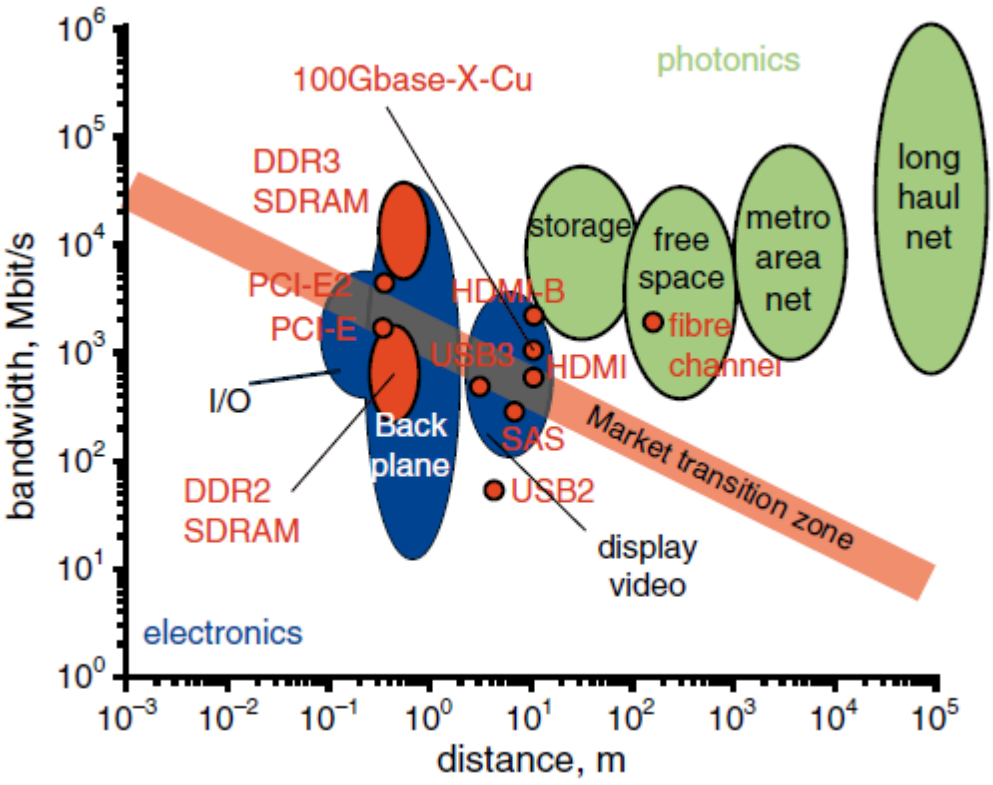

Figure 1.3. A comparison of the bandwidth versus the communication distance for existing electronic and optical communication technologies [6].

1.5 Optical interconnects

Mature long-haul optical fibre technology is already being investigated for short scale rack-to-rack (1-100 m) and board-to-board (0.5-1 m) applications. However,

for chip-to-chip (1-50 cm) and on-chip (< 1 cm) the current technology used in WDM would have to be significantly redesigned. One way of implementing this cost efficiently would be to have all the required photonic components integrated onto a single Si chip. There is an opportunity to take advantage of the huge investments that have been made in complementary metal oxide silicon (CMOS) microelectronics fabrication technologies, which has resulted in processes that offer yields significantly greater than any alternative materials for photonics. Thus, large-scale integration of Si photonic devices that are monolithically integrated with electronic circuits in the same platform at ultrahigh density is feasible [7].

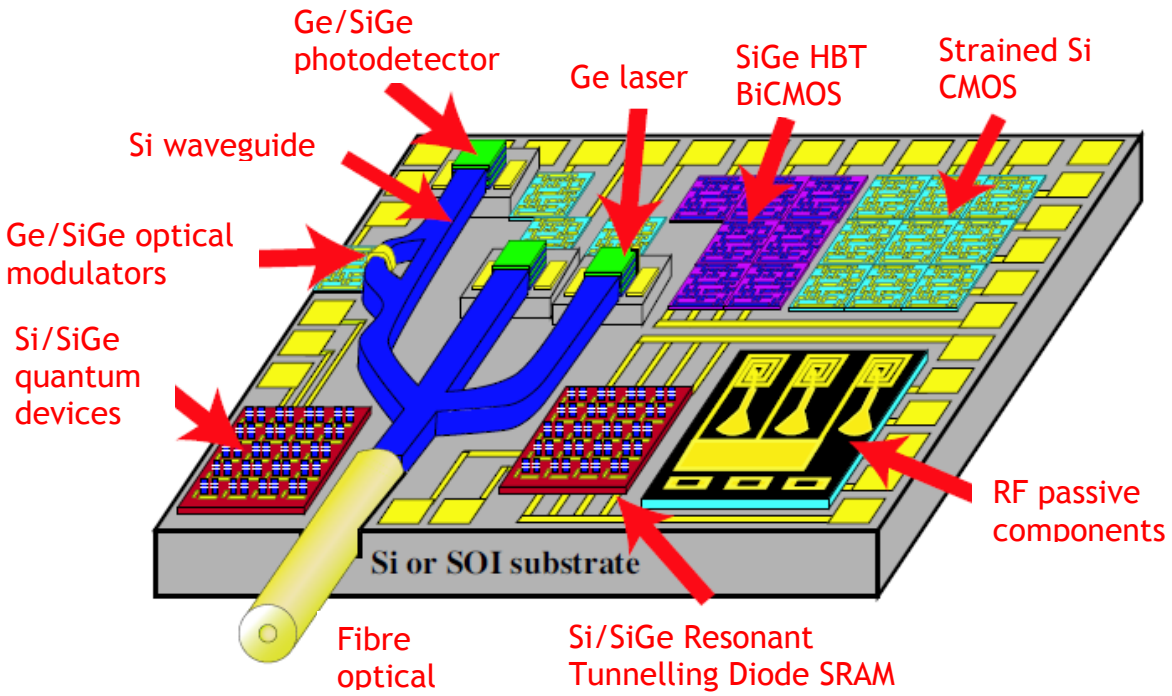

Figure 1.4. A schematic diagram of the envisioned system on chip of the future, where CMOS electronics and Si photonic components such as waveguides, modulators, emitters and detectors are all integrated onto a single Si chip [8].

The components required for the integration of chip-to-chip or on-chip optical photonics along with CMOS electronics are depicted in Figure 1.4, which shows the system on chip of the future, where CMOS electronics and Si photonics consisting of a laser, modulator, waveguide and detector all integrated on the one chip. A fortuitous development was the emergence of silicon-on-insulator (SOI) as

the platform of choice for high-performance CMOS. SOI also offers an ideal platform for creating planar optical circuits. The strong optical confinement offered by the high index contrast between Si (n = 3.45) and SiO_2 (n = 1.45) makes it possible to reduce the footprint of photonic circuits. Such lateral and vertical dimensions are required for economic compatibility with IC processing. The case for Si photonics is also more advantageous than just compatibility with CMOS. Si has excellent material properties that are important in photonic devices. These include high thermal conductivity (~10 × higher than GaAs), high optical damage threshold (~100 × higher than GaAs), and high third-order optical nonlinearities (~100 × higher than optical fiber) [4]. Si is also highly transparent from 1.1 to 7 μm [9]. Furthermore, the lack of two-photon absorption at wavelengths greater than 2.25 μm renders silicon an excellent nonlinear optical material in the mid infrared (IR). At the same time, entirely new functionality can be realised when electronics and photonics are combined onto the same chip.

1.6 Silicon photonics

The first Investigation into Si photonics was established by the work of Soref and colleagues more than 20 years ago [10, 11]. Since then Si photonics has been regarded as one of the most promising solutions to the communication bottleneck facing CMOS based integrated circuits. As a result, the integration of Si photonics components into an integrated chip using CMOS platform has been pursued by several companies with a view to obtaining the performances of optics at the same price of the electronics. For server clusters and data storage centre applications, Luxtera and Kotura have already made commercially available silicon photonics-based 100 Gigabit (Gb) optical transceivers[12] [13]. Intel has demonstrated end-to-end Si photonics integrated link at 50 Gb/s using a single optical fibre [14]. Generally, these photonic integrated chips consist mainly of III-V lasers integrated on silicon [15, 16], Si optical modulator [17-20], and fully integrated germanium (Ge) detector [21-23]. One of the key components that has still to be realised is an efficient monolithic light source on Si.

1.6.1 Silicon based lasers

1.6.1.1 Raman and rare earth doping

There have been several demonstrations of lasing on Si but very few have proven to be adequate for integrated Si photonics. Lasing from Si has been achieved through stimulated Raman scattering. It requires optically pumping and to overcome the optical losses created by free carrier absorption requires a lateral p-i-n junction that is reverse biased to sweep out carriers from the central Si waveguide. This is not a suitable approach for integrated photonics [24, 25]. Another technique to obtain lasing through Si has been demonstrated through rare-earth doping. Since light amplification was demonstrated in optical fibres by Erbium (Er) doping, it has been seen as an avenue to achieve lasing by Si. However, Si is not a suitable host for Er. Therefore, Si nanocrystals formed in rich Si oxide are commonly used as an effective host for Er atoms [26]. Both photoluminescence and electroluminescence have been demonstrated [9, 27] but the optical gain from such extrinsic emitting materials is small [28] due to the limited Er solubility. In addition, lasing has only been shown in very low loss resonators such as toroidal structures [29]. Since these Er doped Si nanocrystals are formed in an oxide, injecting carriers for lasing can only done under very high electric fields via tunnelling [30], therefore this approach is not suitable for an efficient electrical pumped on-chip Si laser.

1.6.1.2 III-V lasers on silicon

An alternative method to achieving an efficient laser on Si is through epitaxially growth of III-V compounds such as GaAs and InP, which are direct bandgap semiconductors and therefore are very efficient light emitting materials. There are difficulties associated with this approach such as the large lattice mismatch that results in misfits and dislocations that cause optical losses. This has been overcome by lattice matching to a SiGe buffer grown on Si [31]. However, the most advanced lasers demonstrated on Si to date have come from a hybrid approach that makes use of SOI wafer bonding technology. The III-V lasers are

initially grown on SiO_2 and then transferred to a Si substrate and have demonstrated impressive performance [15, 16]. Although fundamentally both approaches using III-V semiconductors are not ideal since they are not CMOS compatible because they are dopants within Si.

1.6.1.3 Germanium on Silicon

Recently work by MIT based on tensile strained Ge epitaxially grown on Si has shown to be an exciting route to achieving a CMOS compatible laser for Si photonics. The first Ge on Si continuous-wave laser was demonstrated in 2010 by optically pumping [32] and this was closely followed by the first electrically pumped laser in 2012 [33]. Although the optically and electrically pumped lasers demonstrated very high thresholds before the onset of lasing, it provides a very novel approach to realise an efficient laser on Si. Ge has already been incorporated into state of the art CMOS production as SiGe source and drain regions in p-MOSFETs to increase channel strain and improve mobility in Si transistors [34].

1.7 More-than-Moore

Besides optical interconnects there is much more applications that could benefit from low cost Si photonics integrated with CMOS electronics. More-than-Moore is the combined research effort to give more functionality from a CMOS system on chip (SOC). One likely application is the so-called lab-on-a-chip in which both reaction and analysis are performed on a single device. Such sensors, along with integrated intelligence and wireless communication circuitry, may form nodes of an intelligent sensor network or environmental monitoring. Another potential area for Si photonics is at mid-infrared wavelengths. Where potential applications envisaged for this technology include chemical and biological sensing, trace gas detection and environmental monitoring. Figure 1.5 shows the dual trend between digital functions (“More Moore”) and functional diversification (“More-than-Moore”).

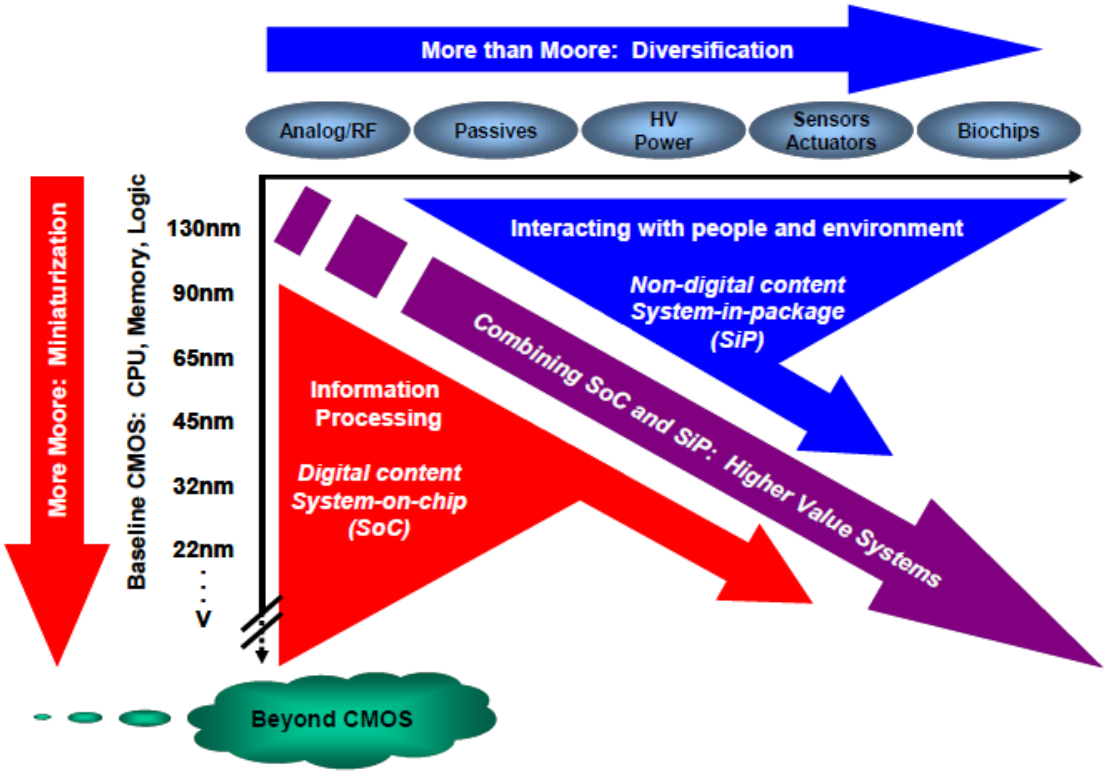

Figure 1.5. The combined need for digital and non-digital functionalities in an integrated system is translated as a dual trend in the ITRS: miniaturization of the digital functions (“More Moore”) and functional diversification (“More-than-Moore”) [35].

1.8 Integration of Germanium on Silicon

To take advantage of the mature CMOS foundry technology and reduce the overall cost of Si photonic chips, integrating Ge expands the spectral active range of Si. There is a trade-off though since Ge has a lattice constant that is 4 % larger compared to Si. When Ge is grown directly on Si misfits and threading dislocations form that are detrimental for photonic devices by acting as a loss mechanism. The maximum Ge film that can be grown on Si without threading dislocations forming is governed by the critical thickness, which is roughly 2 nm as depicted in Figure 1.6, which is a plot of the critical thickness of a SiGe layer grown on Si as a function of the Ge content [34]. This limit maybe tolerated in electronic devices such as the proposed Ge MOSFET but for photonic devices, substantially thicker films are needed for guiding at 1.55 μm wavelength and above. This requirement increases for detection at these wavelengths where ~1-2 μm of Ge will be needed due to

the absorption coefficient. Depositing films of such thicknesses results in 10^8-10^9 threading dislocations per centimetre squared. To reduce the threading dislocation density (TDD) a number of different growth techniques have been investigated.

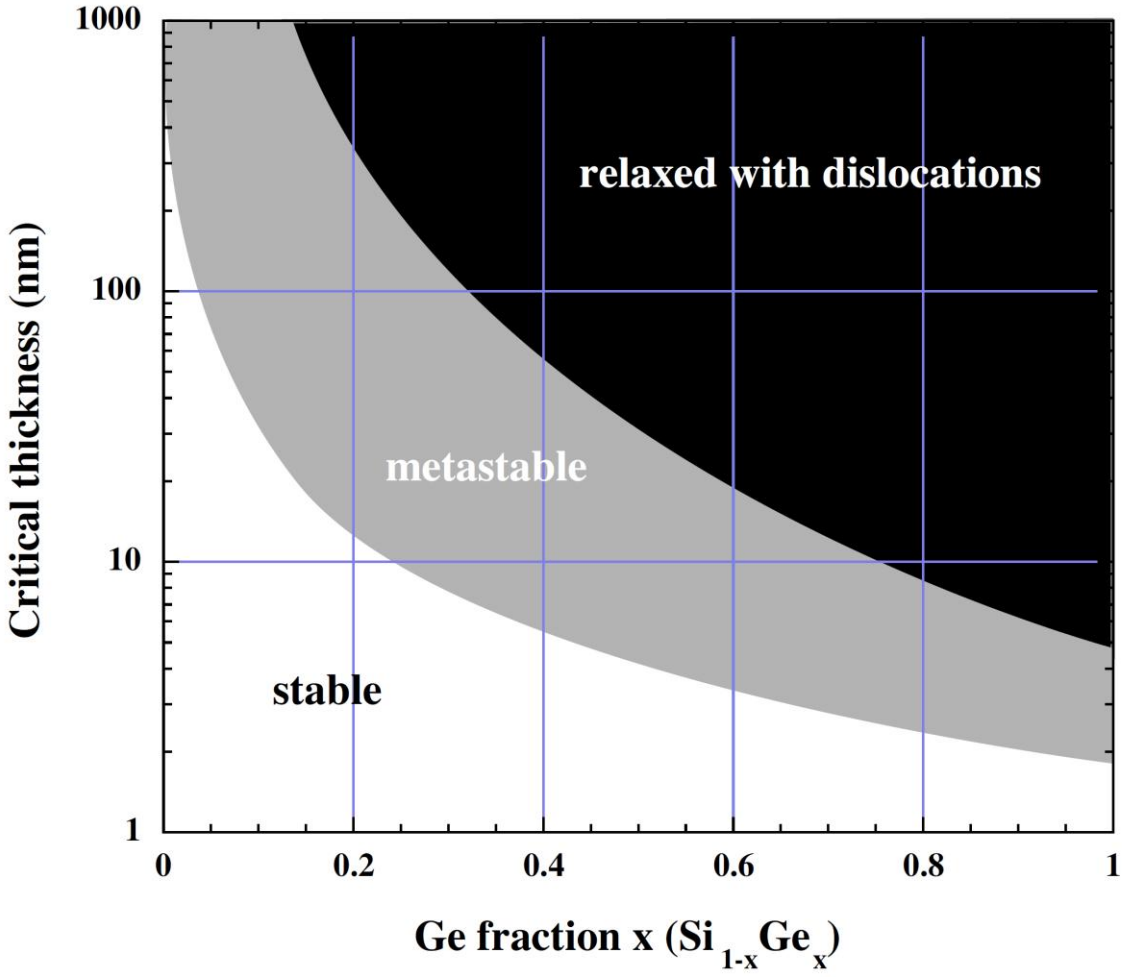

Figure 1.6. The critical thickness plotted as a function of the Ge content for pseudomorphic $Si_{1-x}Ge_x$ layers grown on bulk (100) silicon [34].

1.9 Germanium epitaxy on silicon

1.9.1 Molecular beam epitaxy

There are a number of techniques available for epitaxially growing Ge-on-Si. Molecular beam epitaxy (MBE) was the original technique used for the growth of SiGe alloys on Si in the late 1970s [36]. However, due to the high particle count

within the growth chamber that forms from material growth on the walls of the chamber that over time falls off and contaminates future growths this method produces low yield and is not ideal for mass production and has been used mainly for research purposes.

1.9.2 Chemical vapour deposition

An alternative to MBE is chemical vapour deposition (CVD). This has been the principal growth technique used in Si foundries since the 1960s due to the higher yield compared to MBE. There has been significant research and investment into this technology and as a result, there are high purity gas sources readily available for Si and Ge epitaxy. Source gases available include SiH_4, Si_2H_6, SiH_2Cl_2, and GeH4. In-situ doping can be achieved through AsH_3, PH_3, and B_2H_6. A variety of CVD growth techniques have been developed for high quality Ge and SiGe epitaxy since the 1980s.

1.9.2.1 Atmospheric pressure CVD

Early Ge/SiGe epitaxy by CVD was performed at atmospheric pressure and involved a hydrogen prebake at 1100 ℃ to volatilise contaminating species such as water, oxygen, or carbon. The high growth temperatures used for the epitaxial growth of Si cannot be tolerated for Ge. At such high temperatures, there is significant surface roughness [37] and diffusion of Ge into Si. Therefore, to compromise between an adequate growth rate and the prevention of roughness occurring from relaxation of a metastable strained layer the growth temperature was reduced below 800 ℃. Even with a decrease in growth temperature, atmospheric pressure CVD has inherent problems that make it less popular for growing high quality Si and Ge epitaxial films. At atmospheric pressure the chamber condition cannot avoid impurities from ambient and therefore necessitates high temperature pre-bake and growth that causes auto-doping [38] where dopants diffuse from doped regions from the substrate into the epitaxial layer. As the growth temperature is reduced lower background pressures are required to maintain an oxide-free Si surface.

1.9.2.2 Ultra-high vacuum and reduced pressure CVD

Ultra-high vacuum CVD (UHVCVD) overcomes the problems associated with atmospheric pressure CVD, where the base chamber is usually within the range of 10^{-8}-10^{-9} mbar when idling and 10^{-3} mbar during growth. At ultra-high vacuum, the contamination level can be minimised and high quality Ge can be grown at relatively low temperatures (400-700 ℃). Another method similar to UHVCVD is reduced pressure CVD (RPCVD), where the base pressure during growth is higher than UHCVD but lower than atmosphere and can achieve similar quality growth with similar threading dislocation densities [39, 40]. The most recent development for epitaxial Ge growth has been low energy plasma enhanced chemical vapour (LEPECVD), which can achieve very high growth rates (7 nm s^{-1}) ideal for growing thick strain relaxed virtual substrates [41].

1.9.3 Techniques to reduce threading dislocations

Whilst there has been numerous growth techniques developed, there is still the fundamental issue of the lattice mismatch between Si and Ge. One solution is to gradually grade a SiGe buffer from Si to pure Ge concentration. This method relies upon a fully relaxed SiGe buffer layer to confine all the dislocations and provides a virtual substrate for high quality Ge growth that results in very low TDD of roughly 10^{-6} cm^{-2} [42]. The only drawback to this approach is that it is time consuming and costly since most of the growth is for the thick buffer layer (~10 μm) and not for the active Ge region. In addition, some photonic devices simply cannot incorporate buffer layers into the design, such as the Ge-on-Si single photon avalanche detector, which will be discussed in chapter 6. An alternative method for reducing the TDD is the two-step growth method [43, 44]. A thin Ge buffer layer (~ 30 nm) is first grown at a low temperature (< 400 ℃). The low temperature growth prevents the formation of islanding by plastically releasing lattice strain energy with misfit dislocations at the Si/Ge interface when the thickness of the Ge is greater than the critical thickness. The result is a very high TDD (~10^{8}-10^{9} cm^{-2}) that enables the next higher temperature layer to be grown on a relaxed substrate. There are three modes of hetero-epitaxial growth: Volmer-

Weber, Frank-van der Merwe, and Stranski-Krastanow. Volmer-Weber is island growth (3D), Frank-van der Merwe is layer-by-layer growth (2D), and Stranski-Krastanow proceeds initially as layer-by-layer, followed by islands formation and these are depicted in Figure 1.7.

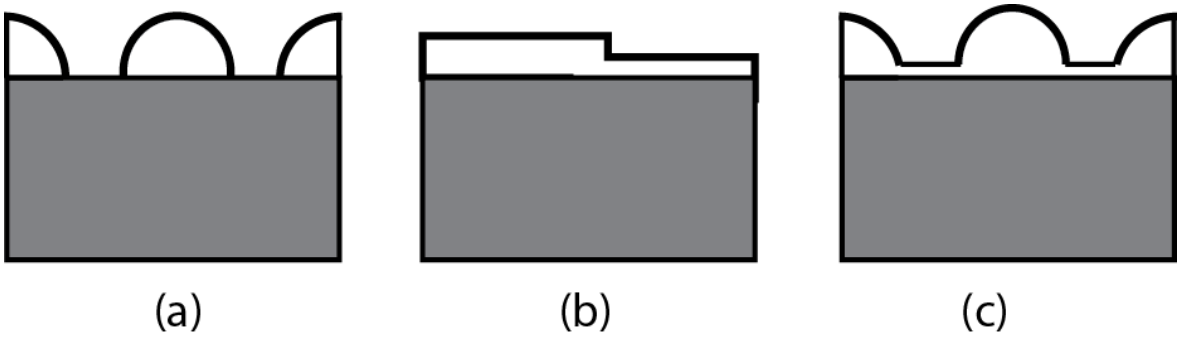

Figure 1.7. An illustration of the three possible growth mechanisms for hetero-epitaxial growth of semiconductors; (a) Volmer- Weber, (b) Frank-van der Merwe, and (c) Stranski- Krastanov.

A thicker Ge is then grown at a higher temperature (~ 750 °C) for a quicker growth rate and higher quality. The last step is cyclic annealing at high temperature to lower the TDD by an order of magnitude to ~ 10^7 cm^{-2} [44]. Another approach to reducing the TDD is to grow Ge selectively in small trenches. A Si or SOI substrate is covered with silicon oxide (SIO_2). Patterning and then removing areas of oxide for Ge to be grown is then done. Dislocations cannot glide over the full area due to the oxide, also dislocations at the Si/Ge interface tend to grow at an angle and annihilate at the oxide. This allows very low TDD of ~ 10^6 cm^{-2}.

1.10 Thermal-mismatch between Ge and Si

Due to the lattice mismatch between Ge and Si, compressive strain is expected for Ge epitaxially grown on Si. However, after growth tensile strain develops in the Ge due to the difference in the thermal expansion coefficients between Ge and Si. When Ge is grown on Si at high temperature and subsequently cooled to room temperature, both Ge and Si shrink at different rates. This corresponds to the Ge developing a biaxial tensile strain as illustrated in Figure 1.8.

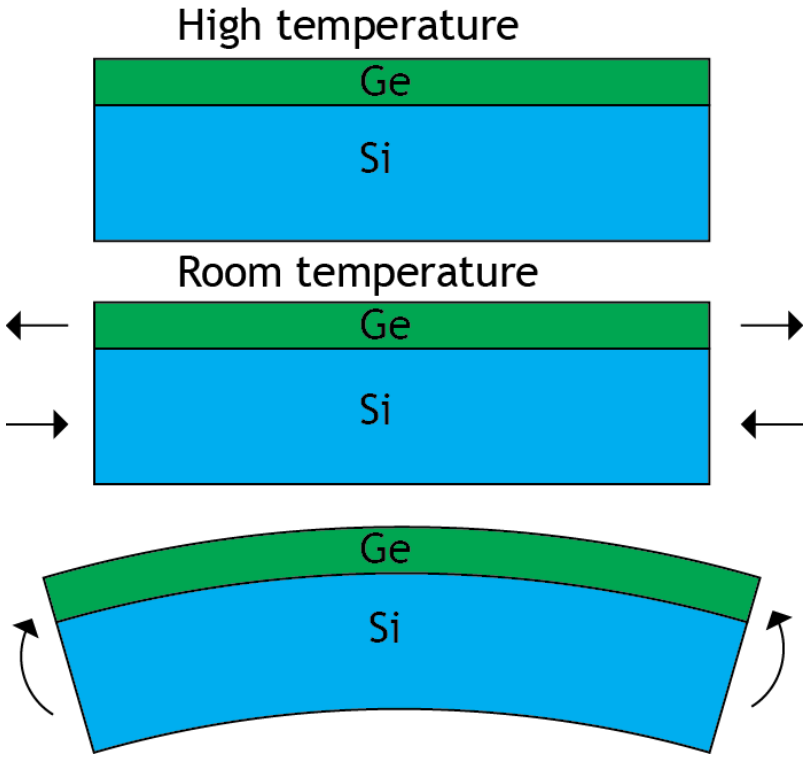

Figure 1.8. (a) An illustration of the tensile strain that develops in Ge grown on a Si substrate at high temperature and then cooled to room temperature where the strain develops from the difference in thermal expansion coefficients.

The amount of tensile strain that develops in the Ge can be calculated by the equations that describe thermal expansion. The thermal expansion coefficient of a material is defined as

$$\alpha = \frac{d\epsilon}{dT} \tag{1.1}$$

where ϵ is the strain and T is the temperature

$$\epsilon(T) = \epsilon(T_0) + \alpha.\Delta T \tag{1.2}$$

The first part of equation (1.2) is assumed to be negligible and the last part caused by thermal expansion. When Ge is deposited on a Si substrate at high temperature, and subsequently cooled to room temperature, the difference between the thermal expansion coefficients of Ge and Si creates strain (see Figure 1.8). Compatibility requires that both the Ge and Si have the same length. As the Si is

very thick compared to the Ge, it is a good approximation to assume that the Si contracts to the size it would have attained in absence of the Ge. With this assumption, the strain of the Si can be expressed

$$\epsilon_{Si} = -\alpha_s . \Delta T \tag{1.3}$$

where α_s is the coefficient of thermal expansion for the Si. The Ge then experiences the same strain because it is attached to the Si, hence

$$\epsilon_{Ge\ attached} = -\alpha_s . \Delta T \tag{1.4}$$

however if the Ge was free, its strain would be

$$\epsilon_{Ge\,free} = -\alpha_{Ge} . \Delta T \tag{1.5}$$

where α_{Ge} is the coefficient of thermal expansion for the Ge. The difference between the strain with and without attachment to the substrate is the thermal mismatch strain

$$\epsilon_{mismatch} = \left(\alpha_{Ge} - \alpha_{si}\right) . \Delta T \tag{1.6}$$

The thermal expansion coefficients for Ge and Si are 5.9 x10^{-6} and 2.6x10^{-6} °C^{-1}, respectively. By convention, tensile stress is positive and compressive stress is negative. Since $\alpha_{Ge} > \alpha_{si}$ tensile strain develops. For a growth temperature of 800 °C this corresponds to ~ 0.25 % tensile strain [44] in the Ge. In turns out that tensile strain actually has an advantageous effect upon the band structure of Ge. Tensile strain transforms Ge into a direct bandgap semiconductor, which improves its ability to generate and absorb light and this will be discussed in more detail in chapter 4.

1.11 Ge-on-Si photonic devices

From the growth methods and techniques discussed, high performance Ge-on-Si photodetectors and modulators have been realised. However, one of the missing components is still an efficient laser on Si. Even though Ge is an indirect bandgap semiconductor, it can be shown with tensile strain and n-type doping. One of the last things is a single photon avalanche detector that incorporates Si as the high multiplication region.

1.12 Organisation of the Chapters

The chapters are organised as follows:

Chapter 2 discusses fabrication techniques and processes employed to fabricate the devices presented in this thesis. This will cover electron beam and ultra-violet lithography. Subtractive processes such as wet and dry etching of Ge and Si. Metal deposition by sputtering and electron beam evaporation to form electrical contacts will be presented. Finally, device packaging such as bonding to a chip carrier and wire bonding will be discussed.

Chapter 3 investigates Ohmic contacts to n-Ge. One of the current limiting factors preventing Ge from being integrated into future CMOS technology, where its higher intrinsic carrier mobility compared to Si would potential allow for faster field effect transistors has been the formation of high resistivity Schottky contacts on n-Ge regardless of the metal work function. This is also an issue for Ge-on-Si optoelectronic devices where it would be desirable to have low resistivity Ohmic contacts to p and n type Ge to minimise heating and ensure device stability.

Chapter 4 presents characterisation analysis of fabricated n-Ge light emitting diodes (LED) and nano-pillars. Ge is known as a poor light emitter due to its indirect bandgap structure, where photon emission relies upon a phonon-assisted process and is therefore very inefficient compared to III-V direct bandgap semiconductors. By tensile straining Ge, it has the effect of changing its band

structure into a more direct bandgap semiconductor. This chapter looks at the optical emission of n-Ge LEDs and nano-pillars that have been covered with high stress silicon nitride films.

Chapter 5 looks at Ge quantum wells grown on Si for light emission. Ge quantum wells with SiGe barriers provide type 1 band alignment. It is envisioned that a Ge multi quantum well structure will allow a reduction in the threshold current required for lasing. The band structure from modelling is presented followed by the fabrication of LEDs for characterisation.

Chapter 6 describes efforts to fabricate Ge-on-Si single photon avalanche detector (SPAD) diodes. Commercially available SPADs for telecommunication wavelengths are formed from relatively expensive InP. Ge has comparative absorption coefficients to InP at a wavelength of 1.55 μm. This is due to its direct band absorption edge at room temperature (0.80 eV). The design of the Ge-on-Si SPAD followed by the fabrication and then the single photon detection efficiency of the devices will be presented.

Chapter 7 concludes the thesis and suggestions for future work are discussed.

2 Fabrication Techniques

2.1 Introduction

This chapter provides a description of the fabrication techniques that were employed in order to fabricate the Ge-on-Si photonic devices discussed in the subsequent chapters. As integration with CMOS is one of the key drivers all fabrication processes developed were designed to be compatible for both the Si and Ge material systems.

2.2 Fabrication

The fabrication topics covered are sample-preparation, lithography, metallization, etching, and dielectric passivation. As the devices fabricated are on the micro and nanometre scale, processing was undertaken within a cleanroom environment. The reason for this is to minimise the probability of device failure from environmental contaminants, such as dust, airborne microbes, and chemical vapours. Therefore, fabrication performed in the controlled setting of the James Watt Nanofabrication Centre (JWNC), which houses a mixture of class 10, 100, and 1000 cleanrooms. This number represents the classification on the maximum amount of particles larger than 0.5 μm found in a cubic feet per air.

2.2.1 Sample Preparation

2.2.1.1 Wafer cleaving

Before device fabrication, the Ge-on-Si wafers were cleaved into the required sample size, which for this work was 1-cm^2 chips. The benefit of working with small sample sizes is that the devices fabricated during the course of this work are novel. This provides plenty of material for device optimization. Since the Ge used during the course of this work was epitaxially grown on top of Si (100) wafers,

all cleaving was performed at 90 degree angles along the <111> crystallographic plane. Wafers were cleaved by a wafer scriber or cut by a diamond saw. To protect the surface of the wafer from contaminates created during cleaving, a polymer that is soluble in acetone was applied.

2.2.1.2 Germanium and Silicon cleaning

After cleaving, the sample surface is thoroughly cleaned to prepare it for lithography. The standard solvent clean that was used to remove impurities and residues from the Ge surface was a 5 minute soak in acetone whilst under ultrasonic agitation, followed by a rinse in isopropyl alcohol (IPA), and then lastly, a nitrogen (N_2) blow dry. One of the main differences between cleaning Ge and Si surfaces is that the RCA standard cleans (SC1 and SC2) usually used for Si are not compatible with Ge . Si forms a thin passivating oxide (SiO_2) in Hydrogen peroxide (H_2O_2), which limits the etch rate in solutions that contain no hydrofluoric acid (HF). Ge on the other hand has an oxide (GeO_2) which is water soluble [45], therefore Ge in H_2O_2 etches at a significant rate [46]. As an alternative to the RCA clean, a cyclic buffered HF (5:1) and deionised water (DI) clean was used.

2.2.2 Lithography

In semiconductor device fabrication, lithography is the process of transferring a desired pattern onto a substrate, from which an additive or subtractive process can then take place. Devices are built-up one layer at a time. There are a number of lithography methods available; nanoimprint [47], electron-beam [48], photo [49] and x-ray [50] lithography to name just a few. Each method has its own advantages and disadvantages. For the devices fabricated during the course of this work, only electron-beam and photolithography were used. The minimum feature size that is achievable by each method is dependent upon the wavelength associated. The JWNC operates a Vistec VB6 UHR EWF electron-beam tool, which is capable of producing extremely small features ≤ 10 nm [51-53]. Photolithography in the JWNC is performed by a Karl Suss Microtec MA6, which

uses an ultra violet (UV) light source and an i-line filter (365 nm wavelength). This setup is suitable for feature sizes larger than 0.5 μm.

2.3 Photolithography

2.3.1 Negative and positive tone photoresists

To transfer a desired pattern to an underlying substrate requires the use of a polymer that is sensitive to photon radiation, also known as a photoresist. Photoresists fall into two distinct categories, positive or negative tone. This describes how the chemical composition of the resist is altered after exposure to radiation. For a positive tone resist, the exposed area becomes soluble in a developer solution, whereas the opposite occurs for a negative tone resist, the exposed area is cross-linked and becomes solid and is insoluble in the developer.

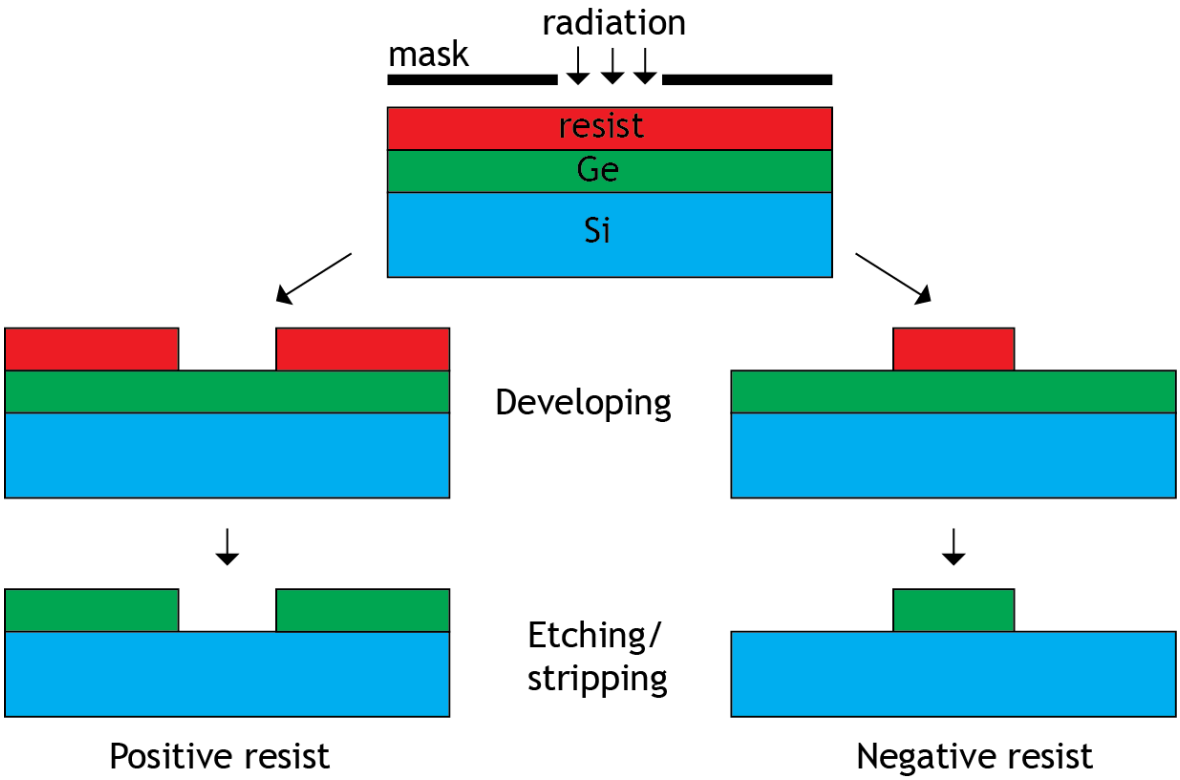

Figure 2.1. A schematic diagram highlighting the difference between positive and negative tone radiation sensitive resists. After exposure of the same pattern and then after a subtractive process such as etching the negative tone resist produces the inverse to the positive tone resist.

This difference between positive and negative photoresist is illustrated in Figure 2.1 for the transfer of the same pattern. After development and a subsequent etch the negative tone resist produces features that are the inverse to the positive tone resist. The majority of the photolithography carried out involved using positive tone photoresists such as the Shipley Microposit S1800 series and the AZ 4500 series. Both of these photoresists are optimised for 365 nm ultraviolet light [54, 55].

2.3.2 Dehydration bake

Before the application of photoresist, it is important that there is no water on the sample surface. Therefore, a dehydration bake is performed in a convection oven for 10 min at 120 ℃. The sample is then cooled back to room temperature inside a laminar flow spinning cabinet for 5 min in a humidity-controlled environment (~ 40%). This is to ensure that the correct level of moisture is reabsorbed onto the sample surface before spinning, which helps with resist adhesion. To further, improve adhesion on Ge and Si surfaces, a surface primer (hexamethyldisilazane) is applied in the same way as photoresist, as depicted in Figure 2.2.

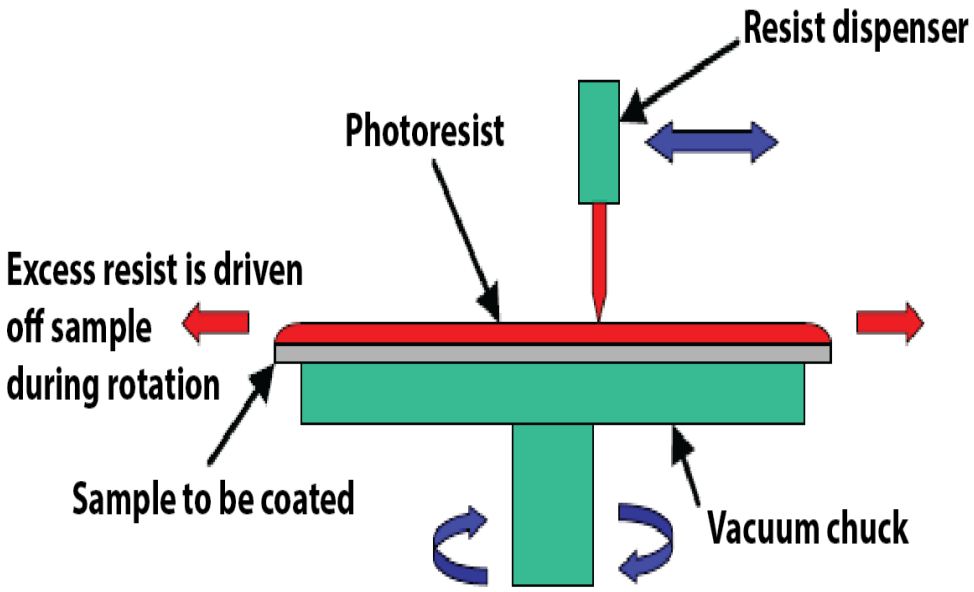

Figure 2.2. A schematic diagram of the standard setup for manual spin coating a radiation sensitive resist.

2.3.3 Spin Coating

It is important to achieve a uniform thickness of resist on the substrate so that features transfer accurately during subsequent additive or subtractive processes. The method for doing this is spin coating. The sample is held in place on a vacuum chuck and then resist is applied manually by a syringe. It is important that there are no air bubbles introduced before spinning. The substrate is then spun for a fixed period and spin speed. This drives off any excess resist and leaves the desired resist thickness. The resist thickness can be calculated by equation (2.1), where k is the spinner constant, p is the resist solid content in percent, and w is the rotational spinner speed.

$$t = \frac{kp^2}{\sqrt{w}} \tag{2.1}$$

The standard process used for spinning the Shipley Microposit S1800 series resists is a spin speed of 4000 rpm for 30 seconds. The thickness can also be identified from the last two numbers in the series name, such as S1818 corresponds to a thickness of 1.8 μm when spun at 4000 rpm.

2.3.4 Prebake

After the photoresist has been applied, a prebake is performed to evaporate the coating solvent and densify the resist. For Shipley photoresists, this corresponds to a softbake on a hot plate set at 85 ℃ for 2 minutes. As the AZ 4500 series resists are thicker, they need a longer softbake time of 5 min at 115 ℃.

2.3.5 Lift-off process for positive photoresists

An issue that can occur whilst using a single layer of positive photoresist is if the next stage of the device fabrication is metallization. After development if the sidewalls of the photoresist are parallel then the deposited metal film will be continuous over the photoresist (see Figure 2.3 (a)) and there will be no separation

between the undesired and desired metal and poor lift-off results. One method to overcome this problem is to soak the top surface of the photoresist in chlorobenzene. This has the effect of hardening the top surface of the photoresist and reducing the development rate, which results in an undercut profile, to aid metal lift-off (see Figure 2.3 (b)). Alternatives that also create an undercut profile consist of a pre exposure developer soak without agitation to harden the top surface and the use of LOR/PGMI resists that act as a bilayer and are isotropically etched during development.

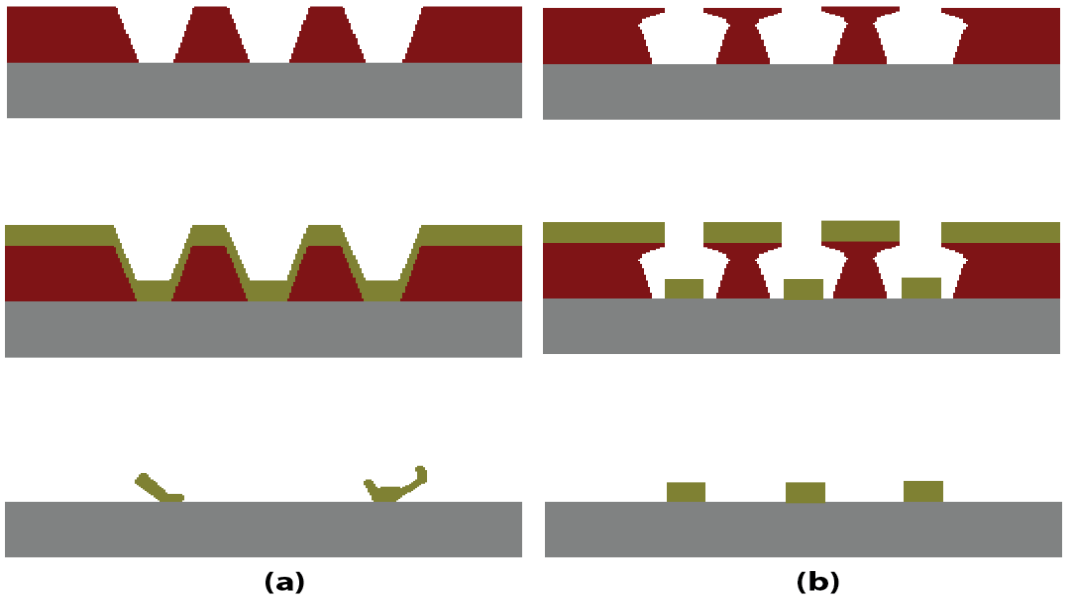

Figure 2.3. Schematic diagram of the lift-off profile for (a) single layer of positive photoresist developed and patterned for metal deposition and (b) chlorobenzene soaked to promote an undercut in the resist profile for metal deposition. In case, (a) poor lift-off results due to the continuous metal film, whereas for (b) desired metal lift-off is achieved.

2.3.6 Mask-aligner and exposure

The basic components involved in photolithography are presented in Figure 2.4. A ultra-violet lamp supplies the radiation that is collimated by a lens and passed through open windows in a chrome mask onto a photoresist covered substrate. The Karl Suss Microtec MA6 mask-aligner/exposure tool handles the alignment between the substrate and photo-mask, and the exposure. There are a number of contact methods available for the MA6 [56].

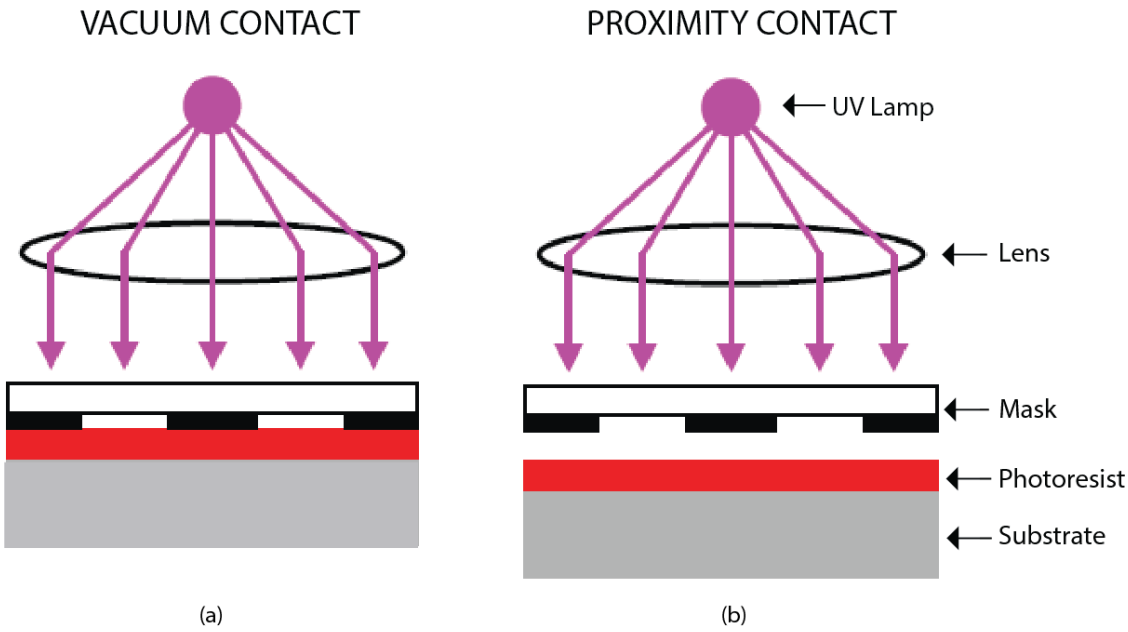

Figure 2.4. The basic components that are involved photolithography. Two different contact methods are compared. (a) Vacuum contact is shown on the left and (b) proximity contact on the right.

The most commonly used contact modes for the MA6 are vacuum and proximity. Vacuum contact is when the photo-mask and resist-covered substrate are brought into intimate contact and exposed. This produces the best resolution levels at the expense of degradation to the mask (see Figure 2.4 (a)). Proximity contact on the other hand eliminates mask damage by introducing a small gap (3 - 50 μm) between the mask and substrate that is set by the user. However, due to the increased separation distance between the mask and photoresist (Figure 2.4 (b)), the pattern resolution is decreased by Fresnel diffraction and can be approximated by equation (2.2) [57]

$$L_{min} = 3\sqrt{\frac{\lambda}{n} \times \left(g + \frac{d}{2} \right)} \tag{2.2}$$

Where λ is the exposing radiation wavelength, n is the resist refractive index, g is the gap spacing between mask and photoresist, and d is the resist thickness. The poor resolution of proximity systems can be overcome by using a collimated optics system between the mask and the wafer, which is known as a wafer stepper commonly employed in CMOS. The UV light is shone through a mask called a

"reticle" in which the patterns are usually 5 or 10 times larger than the features to be printed onto the photoresist. The system optics reduces the size of the features and projects them onto a wafer.

2.3.7 Photo-mask designed by L-edit

Photo-masks for photolithography are created internally in the JWNC by electron beam lithography. The patterns to be transferred are first created by computer-aided design (CAD) software such as L-edit by Tanner EDA. The patterns for each lithography layer are drawn together and then exported as a GDS file. An example of a designed photo-mask is presented in Figure 2.5. Each of the colours in Figure 2.5 represents a single lithography stage and for this particular mask, there is six stages in total. The GDS file is then imported into Layout Beamer where proximity error correction is applied before fracturing.

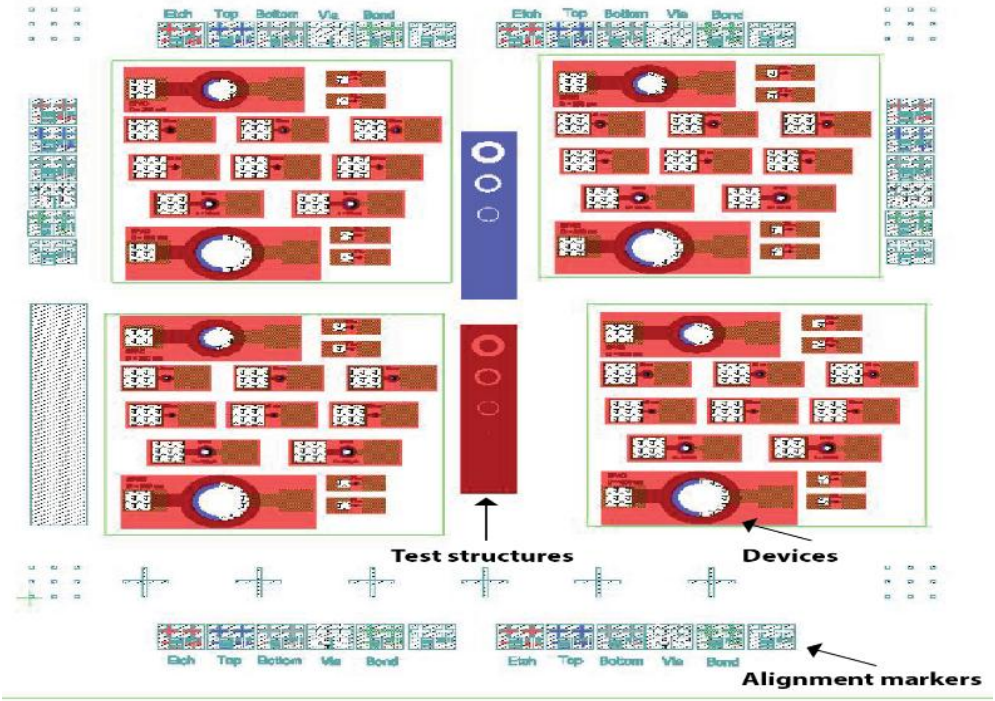

Figure 2.5. An example of a computer aided design photo-mask used during the course of this work. Each colour represents a different lithography stage.

Finally, the output file from Layout Beamer is imported into in-house software called Belle, which sets the required electron spot size and dose for writing. The

photo-mask consists of a quartz substrate coated with chromium and topped with an electron beam resist, where the patterned areas are developed and etched into the chromium.

2.3.8 Alignment between lithography stages

Alignment between photolithography stages is achieved by incorporating metal or dry etched markers. Alignment markers are included at the first lithography stage from which subsequent stages are aligned. The MA6 provides 3 degrees of control between the mask and the sample (x, y, θ). To ensure accurate alignment (1 μm), vernier scales are included along with standard crosses, such as the design shown in Figure 2.6.

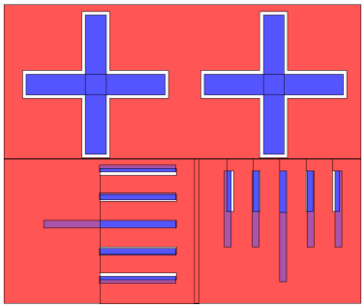

Figure 2.6. An L-edit design of a photolithography alignment marker, the red pattern corresponds to the first lithography layer to be transferred to the sample. The blue pattern represents the next layer to be aligned. The crosses are used for coarse alignment (5 μm) before vernier markers are then used for fine (~ 0.5 μm).

2.3.9 Development

After alignment and exposure, the sample is ready for development. This stage removes the exposed resist (positive resist) or leaves only the exposed areas (negative resist). For the S1800 series, the standard development is an immersion in Microposit MF 319 whilst agitating for 75 seconds, followed by a rinse in reverse osmosis (RO) water. For the AZ 4500 series resists, development is achieved by immersion in a solution of AZ 400K and RO water (1:4) for 3 min.

2.3.10 Post-Bake

After development, a post-bake (hard-bake) is required if the subsequent processing step is a dry or wet-etch, where a 30 min bake at 120 ℃ in a convection oven will stabilise and harden the resist and improve etch masking performance.

2.4 Electron beam lithography

2.4.1 Overview

For devices requiring resolution and alignment less than one-micron, e-beam lithography was used. The fabrication steps involved in e-beam lithography are similar to photolithography in terms of sample preparation, spin coating etc. The main difference is the resist used is sensitive to electrons. As the wavelength of electrons are extremely small (~ 4 pm at 100 keV), the minimum feature size is no longer determined by diffraction. Therefore, this allows extremely small features to be realised compared with photolithography. Electron-beam lithography is a direct write process where a beam of electrons is focussed to pattern each feature instead of a blanket exposure of photons through a photo-mask. This is one of the trade-offs with electron-beam lithography as each feature is written individually it is considerably slower and much more costly compared with photolithography and especially deep UV stepper lithography used in CMOS. However, it does have the advantage of being much more flexible since there are no lithography masks involved. Therefore, designs can be altered without cost, which is extremely important in research where devices are requiring optimization. The patterns for writing are created by L-edit in the same manner that is used to design photo-masks.

2.4.2 Schematic of electron-beam lithography tool

A schematic diagram outlining the main components of an electron-beam lithography tool is presented in Figure 2.7. The electron source is a Schottky

emission gun, which uses a zirconium oxide-coated tungsten cathode that after heating to 1800 K emits electrons that are accelerated up to 100 keV.

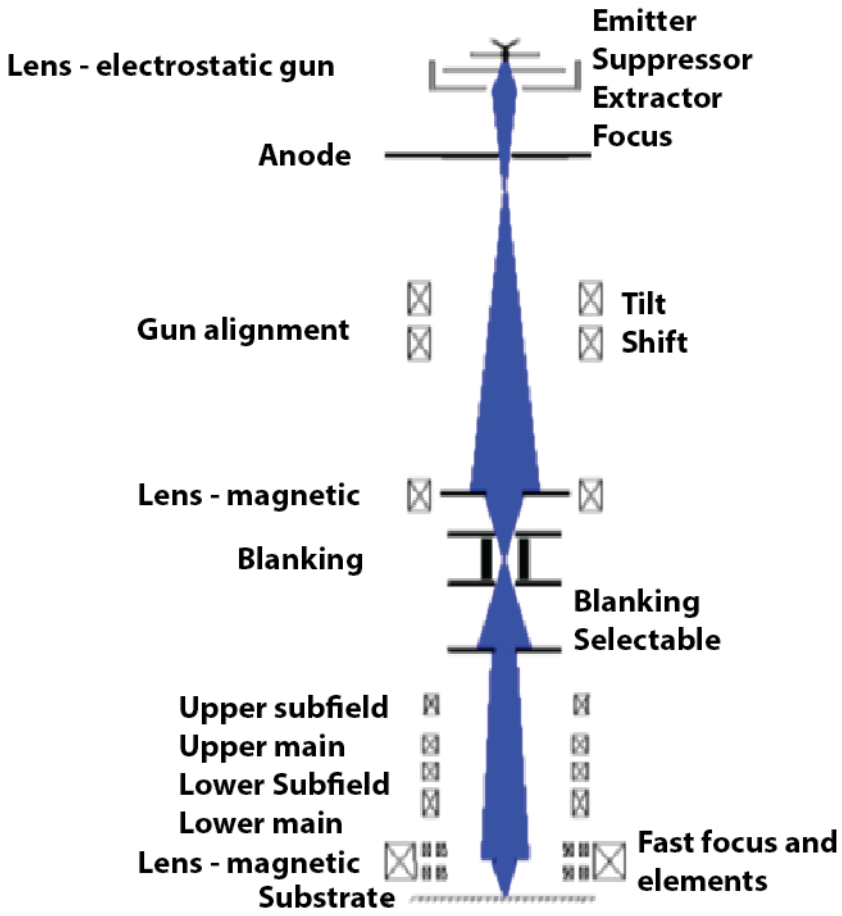

Figure 2.7. A schematic diagram of an electron-beam lithography tool [58].

The higher accelerating voltage produces a smaller spot at the expense of lower beam densities. This results in greater resolution at the expense of increased writing time. The suppressor and extractor create a flow of electrons from a cathode in the emitter through an electrostatic gun lens focussing the beam towards the anode. The electron beam then passes through gun alignment coils, which align the electron beam to the central 2D axis for optimal spot formation. A magnetic lens then focuses the beam and the blanking cell is used to deflect the beam away from the sample. The patterns are generated by different deflectors before a final magnetic lens, which has to be adjusted for a given working distance. This system allows for a selective exposure within a limited region without having to move the substrate. The sample chamber contains a precision

translational stage. This stage is piezoelectrically driven and is controlled by feedback from laser interferometers that measure the x and y travel. The mechanical precision of the stage is off a lower resolution compared to the precision of the beam deflectors and will predominantly determine the field stitching accuracy. The visual representation of the samples are provided by a backscatter detector, which is similar to the operation of a scanning electron microscope. The visual representation can also be used for automatic sensing and alignment markers registration, which is all software controlled. The Vistec VB6 has a digital pattern resolution of 1.25 nm, corresponding to a field size of 1.3 mm^2 and a minimum spot size of 4 nm.

2.4.3 Proximity error correction

The resolution in e-beam lithography is mainly limited by the scattering of electrons in the resist and underlying substrate. First, when the electron beam hits the resist surface it causes additional lateral exposure. Secondly, electrons can back scatter from the substrate and that increases the exposure, which results in feature expansion. These electron scattering effects are known as the proximity effect. Proximity correction can reduce the proximity effect by modulating the exposure dose according to the density of the pattern. This is calculated at the pattern fracturing stage by Layout Beamer. There are standard proximity correction files available for different substrates and e-beam resists.

2.4.4 Electron beam resist

There are several e-beam resists available each with their advantages and disadvantages. Only the electron beam resists used within this work are discussed, poly-methyl methacrylate (PMMA) and hydrogen silsesquioxane (HSQ).

2.4.4.1 PMMA

PMMA is a positive tone e-beam resist that is excellent at producing high-resolution (≤ 20 nm) pattern definition and can be used in various bilayers, which make it the ideal e-beam resist for metal lift-off. There are two types of molecular weight

PMMA available within the JWNC, 2041 and 2010. The process of forming a PMMA bilayer begins with the application of the lower molecular weight variant (2010) that is more sensitive to electron exposure. After the 2010 PMMA has been spun at a spin speed of 5000 rpm for 60 s and given a pre bake at 180 ℃ for 45 min within a convection oven. The second layer (2041) that is less sensitive to electron exposure is applied. After the same spin and pre bake procedure, the bilayer is ready for exposure to e-beam radiation. Figure 2.8 illustrates the resist profile after e-beam exposure and development. Depending on the required resolution a combination of different thicknesses of 2010 and 2041 are available. Methyl isobutyl ketone (MIBK) and IPA developer solutions are optimised for the various thicknesses of PMMA. Development is performed within a temperature controlled water bath set at 23 ℃.

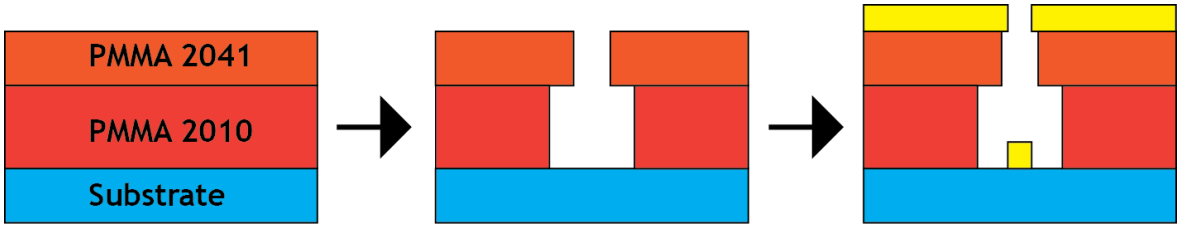

Figure 2.8. A schematic diagram of a PMMA bilayer before and after electron beam exposure. The first PMMA layer (2010) is more sensitive to e-beam radiation compared to the top layer (2041). Therefore, this produces an undercut profile suitable for metal lift-off.

One of the disadvantages with PMMA is its poor etch masking ability that usually results in a 1:1 selectivity between the mask and the etched material. Therefore, for subtractive processes a better alternative is to use HSQ, which has excellent dry etch properties.

2.4.4.2 HSQ

HSQ is a negative tone e-beam resist and the chemical structure consists of Si, oxygen (O_2), and hydrogen (H) atoms that are initially within a three-dimensional cage structure. After exposure to e-beam radiation, the Si-H bonds are broken and the structure resembles SiO_2. The thickness of HSQ can be controlled by diluting in MIBK and the spin speed. The standard process used throughout this work was

a 1:1 MIBK dilution spun at 5000 rpm for 60 s, which results in a film thickness of 300 nm. The unexposed resist is removed during development in tetra-methyl-ammonium hydroxide (TMAH) at 25 % concentration in water at 23 °C for 30 s.

2.5 Metallization

To form electrical contacts to the Ge-on-Si photonic devices requires metallization, which is an additive process. The three most commonly used methods for depositing metals are plating, evaporation, and sputtering. Since metal plating is mainly used for thick film (> 1 μm) depositions and has a relatively low resolution compared to evaporation and sputtering it was not used for the fabrication of the devices in this work.

2.5.1 Electron-beam metal evaporation

Metal evaporation is the process of heating a metal contained within a crucible to a temperature where the metal starts to transform into a gaseous phase. The vaporised metal coats the sample and cools forming a thin film. Heating of the metal can be achieved by a number of methods but most commonly it is done by an electron beam. The e-beam is generated in the same manner as the one used for e-beam lithography. The beam is focussed onto the metal and the interaction between the accelerated electrons and the metal causes the metal to heat and vaporise. The reason why e-beam evaporation is popular is due to the reduced contamination from a combination of local heating and water-cooled sources that prevent the crucible from overheating and causing contamination. This results in a high purity film deposition. A basic diagram of an electron beam evaporator is presented in Figure 2.9. There are two shutters (dashed lines) between the metal crucible and the substrate. The sample chamber shutter is initially closed whilst the crucible is heated to a temperature to begin metal vaporization. The evaporation rate of the metal is monitored by a quartz crystal whose oscillation frequency reduces as additional layers of source material are deposited. Once a stable evaporation rate is reached, the sample chamber shutter opens and exposes the substrate to the metal vapour until the desired film thickness is reached.

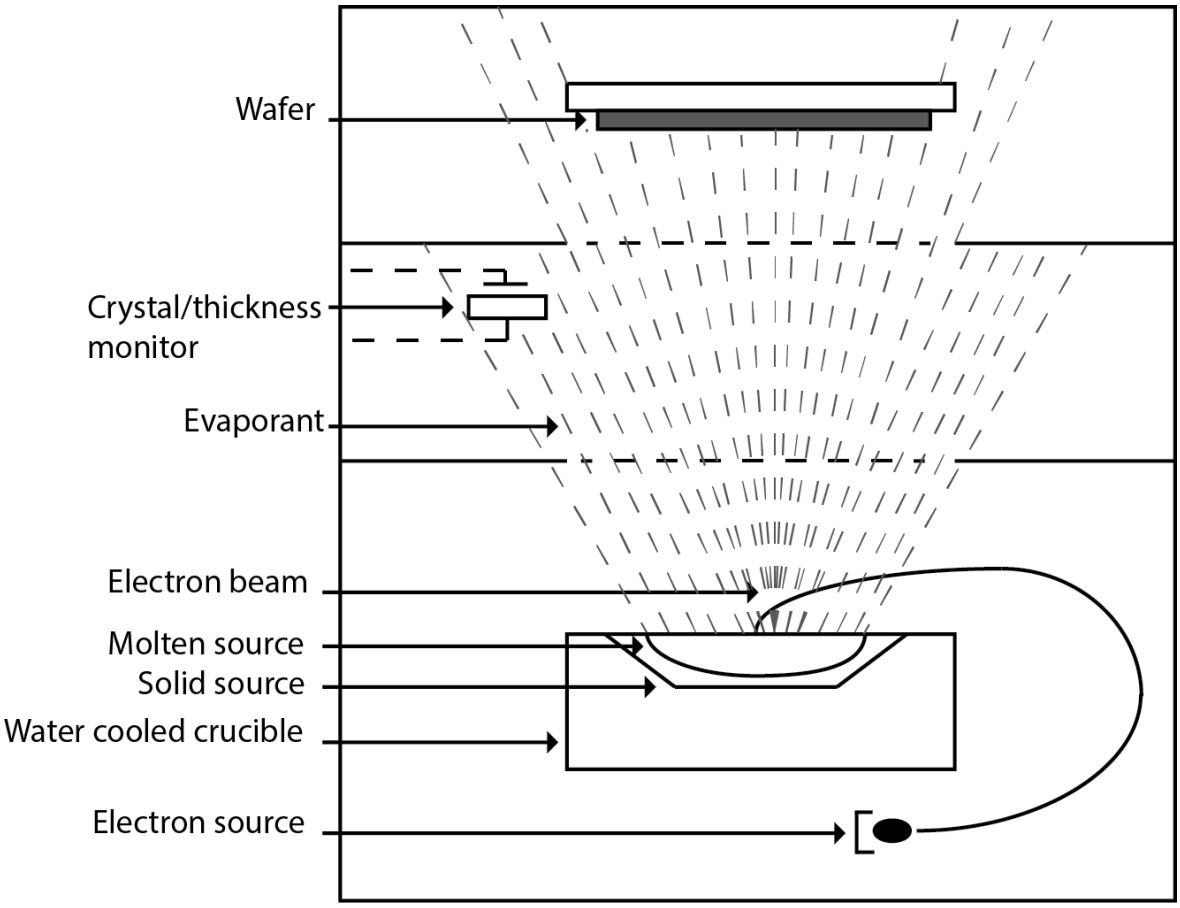

Figure 2.9. A schematic diagram of an electron beam metal evaporator.

The evaporation is done within a high vacuum ($1x10^{-7}$ mbar) to prevent oxidation and particle contamination. The evaporation is directional and therefore it is non-conformal. There are two electron beam evaporators available within the JWNC with a wide selection of metals: Au, Ti, Pd, Pt, Ni, Al, and NiCr.

2.5.2 Metal sputtering

The other method used to deposit metal films during the course of this work was sputtering. Metal sputtering is a physical process, where the metal to be deposited is struck by an argon plasma that sputters fine metal particles into the vacuum of the deposition chamber for substrate coating. The argon plasma is excited by either a DC or RF source. The metal crucible is negatively biased and the plasma sputters neutral atoms away from the crucible towards an anode, where the neutral atoms are deposited on the sample. Since a plasma is required, the

working pressures of sputtering systems are higher (1×10^{-4} mbar). As a result most atoms collide before reaching the sample resulting in a large spread of incident angles. The deposited metallic coating is therefore extremely conformal and is ideal for coating sidewalls. The advantage of a sputtering tool is that materials with a relatively high melting point such as tungsten can be deposited. The sputtering tool within the JWNC was used for sputtering Al bond pads for wire bonding. Since sputtering is conformal, it helps complete electrical contact on mesa-etched devices.

2.6 Etching

As the majority of the fabricated devices in this work are surface normal geometry, they require a mesa etch to define the active area. Etching is a subtractive process and can be achieved by either a chemical water bath (wet etch) or in a plasma (dry etching). The aim of etching is to selectively remove an unmasked material. The advantages and disadvantages of each method will be discussed.

2.6.1 Wet etch

Chemical etchants are very selective for example HF that etches SiO_2 and GeO_2 rapidly (certain solutions ~ 1000 nm/min) has virtually no interaction with the surface of Si or Ge. This is why HF is used to remove native oxides on Ge and Si surfaces before metal deposition for Ohmic contacts. This is one of the advantages of wet etches they are very selective and introduce little damage to the underlying substrate. For a detailed list of wet etchants and target materials please refer to references [59, 60]. Due to the chemical nature of the etchant, etching is usually isotropic; it etches in each direction at the same rate. As a result, etch profiles show an over etch from the desired feature and this is depicted in Figure 2.10, where the target etch material SiO_2 is etched in HF at the same rate in the x and y directions. Wet etching is typically used when high etch rates are required (micromachining), and low surface damage is important.

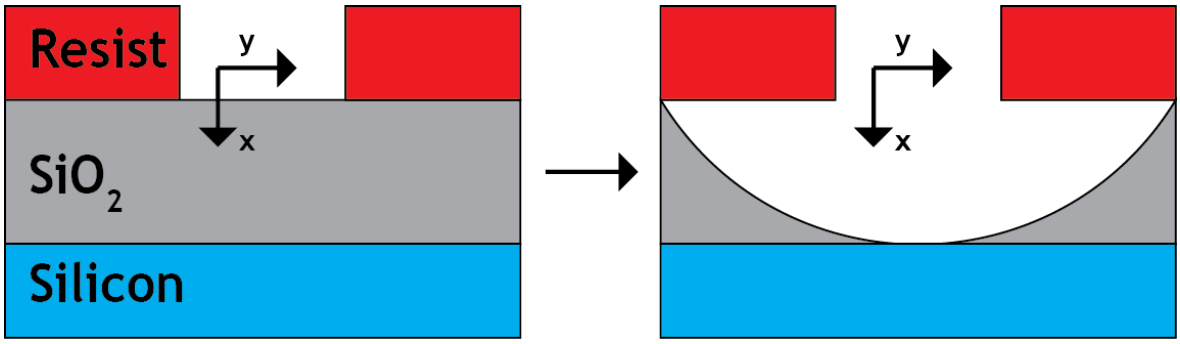

Figure 2.10. An illustration of an isotropic wet etch of SiO_2 by a hydrofluoric acid solution.

2.6.2 Dry etching

When feature sizes are less than one micron the over-etching associated with wet etching becomes severe. Therefore, for etching small features that require vertical sidewalls, dry etching in plasma is used as it can produce completely anisotropic etches. There are two main types of dry etch available within the JWNC, reactive ion etching (RIE) and inductively coupled plasma RIE (ICP-RIE). A schematic diagram for both types of dry etch tool is shown in Figure 2.11 (a) and (b), respectively.

2.6.2.1 Reactive ion etching

Reactive ion etching (RIE) removes undesired material through a combination of chemical and physical interaction with accelerated ions. RIE can provide both highly anisotropic profiles and good selectivity between the mask and the target material to be etched. RF power is applied to two parallel plates that control both plasma generation and ion acceleration. The etching rate directly depends on the plasma density. Increasing the RF power has the effect of increasing the self-biasing voltage on the cathode where the sample is located. The consequence is an increase in the ion bombardment energy and hence a deterioration of the etching selectivity and increased sample damage.

2.6.2.2 Inductively coupled plasma

In an ICP-RIE the etch rate is controlled by high energy and reactive radical ion concentration and RF bias. Low plasma pressure will then result in increased etch times. Increasing the RF bias is unattractive, as the high-energy ions cause too much damage in many applications. Therefore, ICP-RIE technique was developed to allow independent control of the density of the plasma and the pressure in the processing chamber. The technique uses one RF source to control the built in potential to accelerate the high-energy ions and a second RF source to control the density of the plasma. The independent control of the plasma density and ion energy allows for fast anisotropic etches in a low pressure environment.

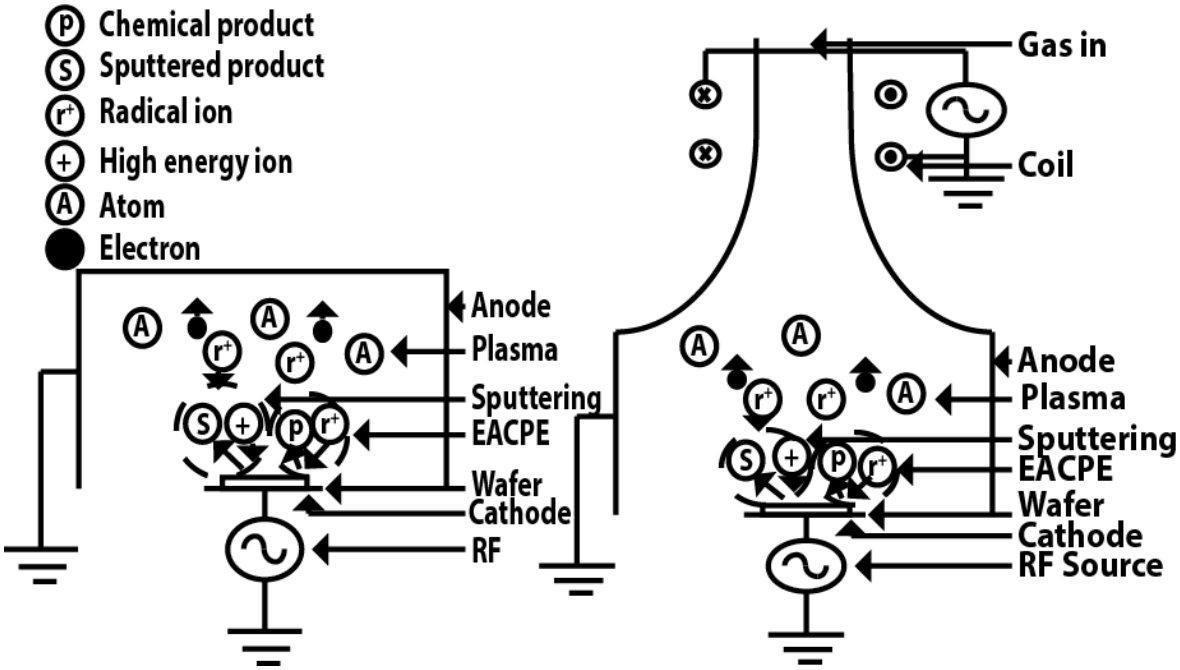

Figure 2.11. Schematic diagram of a (a) reactive ion etching (RIE) tool and (b) inductively coupled plasma RIE dry etch tool.

2.6.2.3 Dry etching Si and Ge

For etching the Ge-on-Si devices discussed in this work, an ICP-RIE was performed using a Surface Technology Systems (STS) etch tool with a mixture of SF_6/C_4F_8 gasses. The full process parameters of the etch are provided in Table 2.1.

Parameter	Value
Gas	SF_6/C_4F_8
Flow (SCCM)	25/90
Platen power (W)	12
Coil power (W)	600
Pressure (mT)	10
Etch rate Ge/Si (nm/s)	4.2/2.2

Table 2.1. Germanium and silicon etching parameters in the STS ICP-RIE tool using SF_6/C_4F_8.

This recipe was originally developed for etching low loss Si waveguides by reducing sidewall roughness. It also etches Ge anisotropically but at a slightly faster rate than in Si. A test etch of its ability to etch Ge anisotropically is shown in a scanning electron microscope image of 70 nm wide Ge ridges etched 500 nm in Figure 2.12.

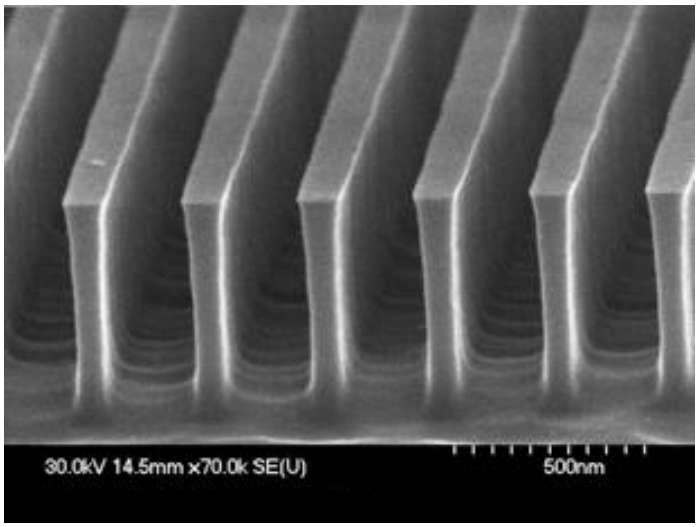

Figure 2.12. A scanning electron microscope image of Ge ridges 70 nm wide etched 500 nm by the STS ICP-RIE tool with SF_6/C_4F_8 gasses.

This process produces anisotropic etching by protecting the sidewalls from etching by depositing a non-reactive film. The bottom surface is exposed and is etched. In this process the etching gas is SF_6 and the passivation gas is C_4F_8. C_4F_8 in the

plasma can form a fluorine-carbon compound that can prevent fluorine from further reacting with the Si or Ge and prevent etching. This process was derived from the Bosch process [61] that is a switching process from etch to passivation, although this can generate very fast etch rates it also leads to scalloping of the sidewalls. Therefore, this is a non-switching process, where both gasses flow at the same time. It generates much slower etch rates, the C_4F_8 protects the sidewalls, and the SF_6 ion bombardment is directional and does not attack the sidewalls.

2.6.2.4 Dry etching SiO_2 and Si_3N_4

Another dry etch process that was commonly used was etching via holes through a passivation layer such as SiO_2 or Si_3N_4. The BP80 RIE tool from Oxford Plasma Instruments was used. The gasses used in the BP80 were CHF_3/N_2.The etch is extremely selective over Ge and metal contacts can be used as an etch stop since it does not etch readily by the gasses.

2.7 Passivation and planarization

For the deposition of dielectrics for passivation or planarization, they were deposited by plasma enhanced chemical vapour deposition (PECVD). The fundamental principles are quite similar to dry etching with a plasma. The energy of the plasma provides the necessary activation energy rather than using high temperatures comparable to the growth temperature of the epitaxial growth of Ge-on-Si. This has the advantage of not affecting the growth quality or causing any dopant segregation from highly doped growth regions. The PECVD conditions can be optimised to be have very low damage to the substrate. For the devices fabricated in this work, mainly Si_3N_4 was used. An even lower processing temperature can be obtained by using ICP-CVD.

3 Ohmic contact to n-Ge

3.1 Introduction

Before discussing the Ge-on-Si photonic devices, one key area that was investigated was the ability to form an Ohmic contact to n-Ge. There is an increased interest in using Ge for both electronic and optical devices on top of Si substrates to expand the functionality of Si technology. Ge integrated with CMOS is being investigated for end-of-roadmap electronic devices where the high mobility of Ge would replace Si as the channel material to potentially allow reduced-power operation [62]. Epitaxial Ge-on-Si is being used as a photodetector for 1.55 μm telecoms [6], and Ni contacts on Ge are being investigated for spintronic devices [63]. All of these applications require low resistivity n- and p-type Ohmic contacts, which are essential for high performance devices and circuits.

For the integration of Ge into such applications, the challenges faced are poor solubility of dopants, large diffusion coefficients, and the incomplete activation of dopants, which have led to high-off currents and low on-drive currents in transistors [64]. The poor device performances have stemmed from the large contact resistances found in the source and drain regions. The large contact resistances to n-Ge have been attributed to Fermi level pinning near the valence band, which results in large Schottky barrier heights (SBH) independent of the metal work function. Low resistive contacts are especially important for cryogenically cooled research devices and for reducing the RC time constant off high frequency devices and the overall resistance. In CMOS, the Contact resistance is now the dominant resistance as scaling has moved below 100 nm gate lengths.

This chapter will start by investigating the theory behind metal-semiconductor junctions. The ideal Schottky–Mott model will be introduced and then I will discuss why this breaks down for Ge. Current literature methods to alleviate Fermi level pinning will be discussed before presenting the Ni-Ge contacts formed in this work. It will then discuss the most common test structures that can be fabricated to

calculate the specific contact resistivity, which is the key parameter for comparing contact technology. The advantages and disadvantages of each test structure will be touched upon before finally, electrical characterization of metal n-Ge contacts fabricated during the course of this work will be presented and compared against literature results.

3.2 Metal-semiconductor junction

3.2.1 Ideal Schottky-Mott barrier

When a metal makes contact with a semiconductor, a barrier is formed at the metal-semiconductor interface. This barrier is responsible for controlling the current conduction. The band diagram for the ideal case of a metal and an n-type semiconductor that are separated is depicted in Figure 3.1 (a).

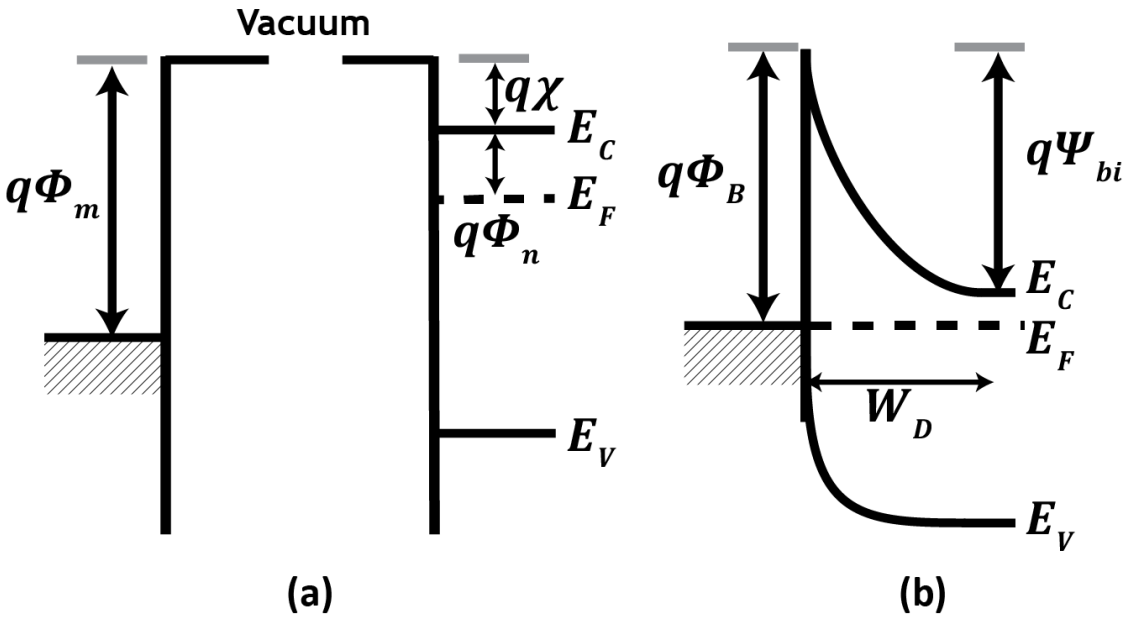

Figure 3.1. Band diagram of an ideal metal-semiconductor contact (a) separated and (b) in contact, where the Fermi level of the semiconductor is lowered relative to the Fermi level of the metal.

The work function of the metal (ϕ_M) describes the minimum energy required to remove an electron from the surface to vacuum and is calculated as the difference in energy from the Fermi level of the metal and vacuum. The work function for

the semiconductor is equal to the electron affinity (χ) plus the semiconductor work function(ϕ_n). As the metal and semiconductor are brought into intimate contact the Fermi levels align and the conduction (E_C) and valence (E_V) energy bands bend in order to reach thermal equilibrium as is shown in Figure 3.1 (b). From this band diagram, the barrier height (ϕ_B) is calculated simply as the difference between the metal work function and the electron affinity.

$$\phi_B = \phi_M - \chi \tag{3.1}$$

Therefore to engineer an Ohmic or Schottky contact to Ge, it should be as simple as changing the barrier height by choosing metals of different work functions to select the required contact. To obtain an Ohmic contact to n-Ge would require an accumulation type contact, where electrons in the metal would encounter the least barrier flowing in and out of the semiconductor, whereas to form a Schottky contact, would require a large ϕ_M. However, in reality, the barrier height for Ge is independent of the metal work function and a depletion contact forms. This effect is known as Fermi level pinning, where the Fermi level of Ge is pinned at a fixed energy in the bandgap, regardless of the majority carrier doping concentration [65, 66]. It is not fully understood what causes Fermi level pinning but the two most widely used theories are surface interface states and metal induced gap states (MIGS).

3.2.2 Fermi Level pinning

3.2.2.1 Interface states

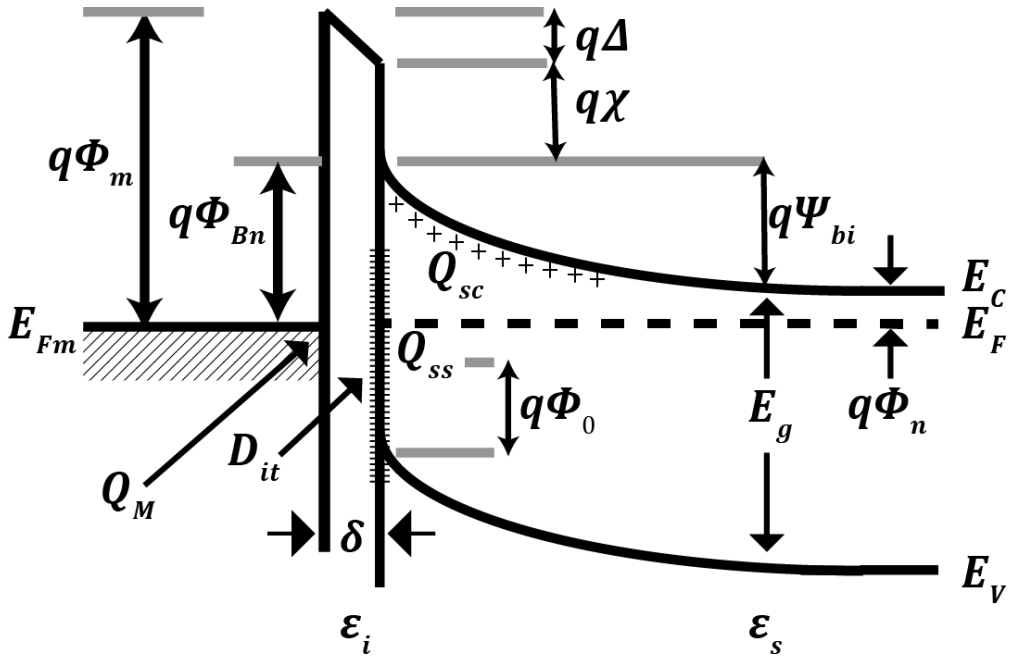

Figure 3.2. Energy band diagram of a metal on n-type semiconductor with an interfacial layer of a few angstroms.

The ideal model does not take into account interface states. An expression for the barrier height that includes interface states can be found by following a few assumptions. The first is that there is intimate contact between the metal and semiconductor but there is also an interface layer $(\delta \approx 4\ \text{Å})$, which is transparent to electrons but can still withstand a potential across it. The second is that the interface states are a property of the semiconductor surface and are independent of the metal. The band diagram for a metal on an n-type semiconductor that includes interface states is presented in Figure 3.2. Above the Valence band, the energy level ϕ_0 is called the charge neutral level (CNL), where the states above are acceptor type and below are donor type. In Figure 3.2, the semiconductor is acceptor type, since the Fermi level is above the CNL. The interface trap charge on the semiconductor is negative and given by

$$Q_{ss} = -qD_{it}\left(E_g - q\phi_0 - q\phi_{Bn}\right) \tag{3.2}$$

Where D_{it} is the interface-trap density. The space charge that forms in the depletion layer of the semiconductor at thermal equilibrium is given by

$$Q_{sc} = qN_D W_D = \sqrt{2q\varepsilon_s N_D\left(\phi_B - \phi_n - \frac{kT}{q}\right)} \tag{3.3}$$

Where the depletion layer width W_D is calculated as

$$W_D = \sqrt{\frac{2\varepsilon_s V_{bi}}{qN_D}} \tag{3.4}$$

V_{bi} is the built in potential, N_D is the doping concentration, ε_s is the dielectric constant of the semiconductor, and kT is the product of the Boltzmann constant and temperature. In the absence of any space-charge effects in the interfacial layer, an equal and opposite charge, Q_M, develops on the metal surface, which can be expressed as

$$Q_M = -(Q_{ss} + Q_{sc}) \tag{3.5}$$

The potential Δ across the interfacial layer can be found from Gauss law' as

$$\Delta = -\frac{\delta Q_M}{\varepsilon_i} \tag{3.6}$$

where ε_i is the permittivity of the interfacial layer, δ is the thickness of the interfacial layer. Another relationship for Δ can be found from the band diagram in Figure 3.1 and expressed as

$$\Delta = \phi_m - (\chi + \phi_B) \tag{3.7}$$

This relationship stems from the fact that the Fermi level must remain constant throughout the system at thermal equilibrium. By equating equation (3.6) and (3.7), and substituting equation (3.5), an expression can be found for the ϕ_B.

$$\phi_m - \chi - \phi_B = \sqrt{\frac{2q\varepsilon_s N_D \delta^2}{\varepsilon_i^2}\left(\phi_B - \phi_n - \frac{kT}{q}\right)} - \frac{qD_{it}\delta}{\varepsilon_i}\left(E_g - q\phi_0 - q\phi_B\right) \tag{3.8}$$

This expression can be simplified by substituting expressions that contain the interfacial properties into equation (3.8)

$$c_1 = \frac{2q\varepsilon_s N_D \delta^2}{\varepsilon_i} \tag{3.9}$$

$$c_2 = \frac{\varepsilon_i}{\varepsilon_i + q^2 \delta D_{it}} \tag{3.10}$$

Equation (3.8) thus reduces to

$$\phi_B = c_2\left(\phi_m - \chi\right) + \left(1 - c_2\right)\left(\frac{E_g}{q} - \phi_0\right) \tag{3.11}$$

There are two limiting cases, when $D_{it} \to \infty$, then $c_2 \to 0$ and therefore

$$q\phi_B = E_g - q\phi_0 \tag{3.12}$$

In this situation, the Fermi level of the semiconductor is pinned by the interface states at the value $q\phi_0$ above the Valence band. Therefore, the barrier height is independent of the metal work function and is determined by the interface states of the semiconductor. When $D_{it} \to 0$, then $c_2 \to 1$ and therefore

$$q\phi_B = q(\phi_m - \chi) \tag{3.13}$$

which is the equation for the ideal barrier height, where interface states play no role. Covalent semiconductors such as Ge give rise to a large density of states due to unsaturated bonds at the surface and therefore suffer from Fermi level pinning at the CNL. An estimation of the Fermi level pinning can be found from the pinning factor that is found from the slope of barrier height versus metal work function.

$$S \equiv \frac{\partial \phi_B}{\partial \phi_m} \tag{3.14}$$

3.2.3 Experimental values of barrier height for metals on Ge

It has been shown experimentally that the pinning factor in Ge is close to the Bardeen limit ($S \approx 0$) [67], resulting in large Schottky barrier heights for metal/n-Ge junctions, which leads to rectifying contacts, regardless of the metal deposited. Dimoulas and Nishimura both investigated a wide range of metal/n-Ge contacts and extracted the barrier heights (0.5-0.6 eV), pinning factor (0.05, 0.02), and CNL (0.09, 0.08 eV) [65, 68]. Figure 3.3 is a plot of the barrier height versus metal work function and it clearly shows that the barrier height is predominately fixed. Nishimura proposes that Fermi level pinning arises due to MIGS and not surface interface states. This assumption was established after observing no change to the barrier height after applying forming gas anneals to passivate the surface interface states.

3.2.4 Metal induced gap states

MIGS is an intrinsic property for the metal/semiconductor interface [69]. It can be explained as a free electron wave function from the metal that penetrates into the semiconductor bandgap, inducing gap states that are either acceptor or donor like states. Depending on the surface state distribution and the Fermi level of the semiconductor, these states will be partially filled and can lead to a positive or negative net surface charge. Although theoretically it is a different explanation on why Fermi level pinning occurs, it has the same result as surface interface states. The Fermi level is pinned at the CNL. Based on these two theories, the

majority of the previous work on Ohmic contacts to n-Ge has focussed on reducing the SBH by alleviating the Fermi level pinning either by insertion of an interfacial layer or by passivating the surface.

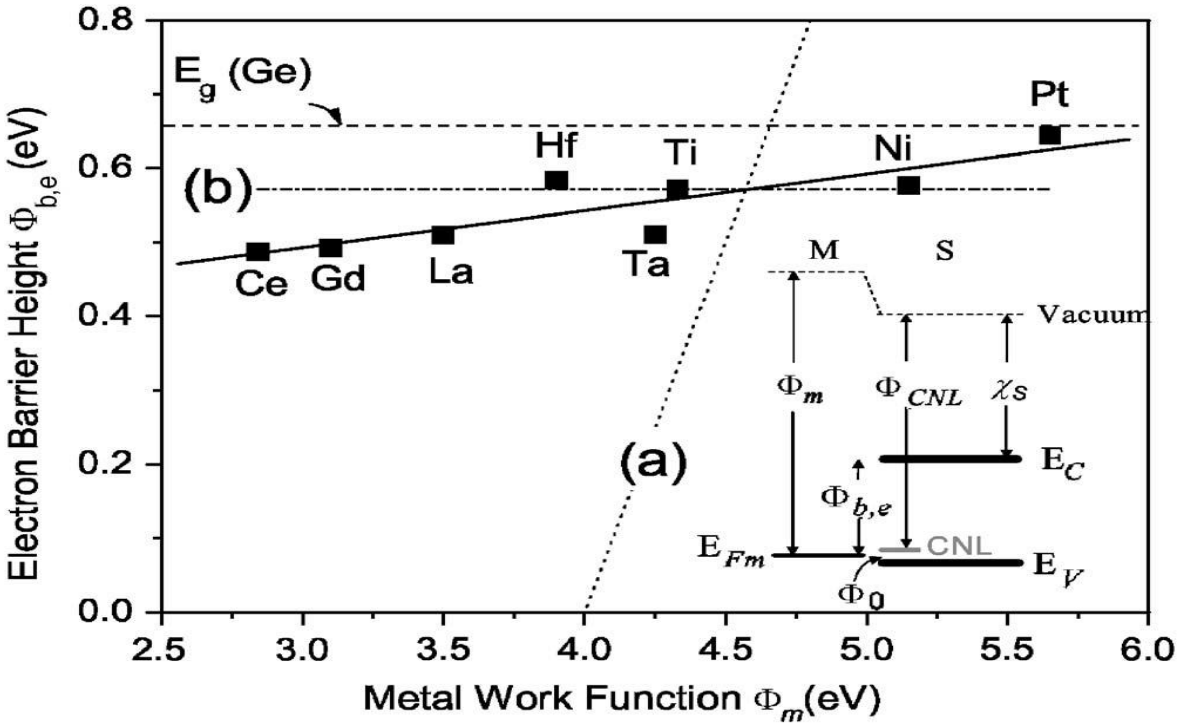

Figure 3.3. (a) Barrier height versus metal work function. The solid line represents a linear fit to the experimental points. The dotted line (a) represents the ideal Schottky limit (S = 1). The horizontal dash-dotted line (b) represents the Bardeen strong pinning limit (S = 0). The inset shows the alignment of the different energy levels at an arbitrary metal-semiconductor interface [65].

3.2.4.1 Insertion of an interfacial layer

Based on the MIGS theory, a number of different methods have attempted to suppress the metal wave function from penetrating into the Ge in order to unpin the Fermi level. They are based on the concept of inserting a thin interfacial layer such as AlO_2 [70], TiO_2 [71], Ge_3N_4 [66], Si_3N_4 [72], or Si [73] between the metal and the n-Ge. They have showed promise in reducing the barrier height and obtaining Ohmic behaviour but specific contact resistivities (ρ_c) have remained large $(>2\times10^{-6}\ \Omega\text{-cm}^2)$, mainly due to the added series resistance of the interfacial layer.

3.2.4.2 Surface passivation

Approaches based on the surface interface states theory consist of terminating dangling bonds at the Ge surface to unpin the Fermi level. One way to implement this is to epitaxially grow lattice matched Fe_3Si (~ 0.565 nm) on Ge to atomically control the interface. Another more commonly used method is to use wet chemical treatments such as ammonium sulphide to sulphur passivate the Ge surface and this demonstrated success in unpinning the Fermi level [74-78]. An illustration of how these approaches reduce the interface trap density by terminating dangling bonds is presented in Figure 3.4.

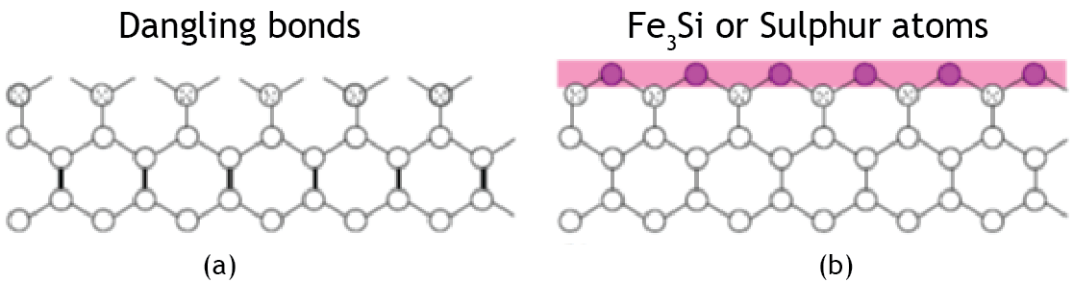

Figure 3.4. A schematic diagram of the side view of the [0 1 1] direction of (a) clean and (b) Fe_3Si or sulphur passivated Ge (001) surfaces.

3.2.5 Ohmic contact to n-Ge regardless of Fermi level pinning

Even in the presence of a large Schottky barrier height due to Fermi level pinning at the CNL (Figure 3.5 (a)) an Ohmic contact can still be engineered. The conventional method to overcome a large SBH relies upon on a large doping density (N_D), as the depletion layer width (W_D) is inversely proportional to N_D, as shown in equation (3.4). A narrow W_D allows tunnelling of electrons through the barrier (Figure 3.5 (b)) and results in metal contacts with good electrical behaviour.

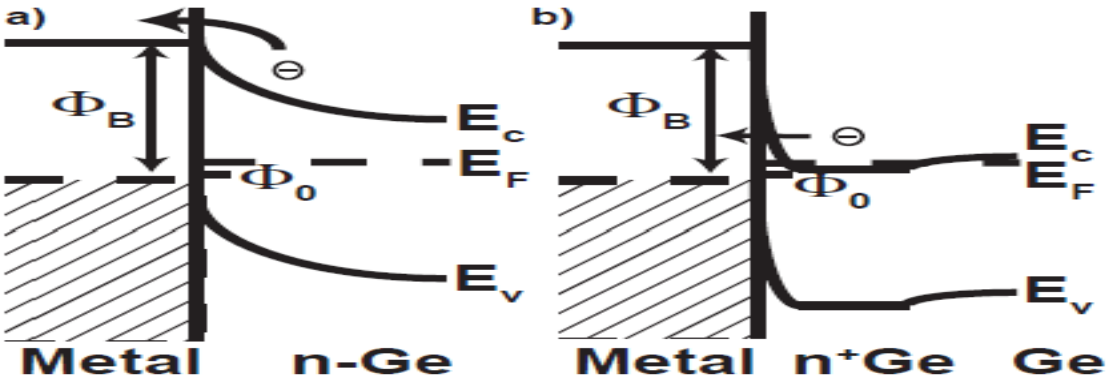

Figure 3.5. (a) The usual case for a metal contact to moderately doped n-Ge where the E_F is pinned near the CNL, which is located just above the valence band and therefore induces a large SBH, regardless of the metal work function. (b) Ideal case where the material is doped sufficiently to reduce the barrier width to allow tunnelling of electrons.

3.2.6 Conduction mechanisms

Dependent upon the doping concentration of the semiconductor there are three conduction mechanisms that can dominate as presented in Figure 3.6. For lightly doped semiconductors, the main conduction mechanism is thermionic emission, where only electrons from the semiconductor that have sufficient energy can overcome the Schottky barrier. The total current density for thermionic emission (TE) under forward bias can be expressed [79]

$$J_{s\to m} = A^* T^2 \exp\left(\frac{-q\phi_B}{kT}\right)\exp\left(\frac{qV}{kT}\right) \qquad (3.15)$$

$$A^* = \frac{4\pi q m^* k^2}{h^3}$$

where A^* is the effective Richardson constant and for n-Ge (100) is $143\ \mathrm{A\text{-}cm^{-2}K^{-2}}$ [80].

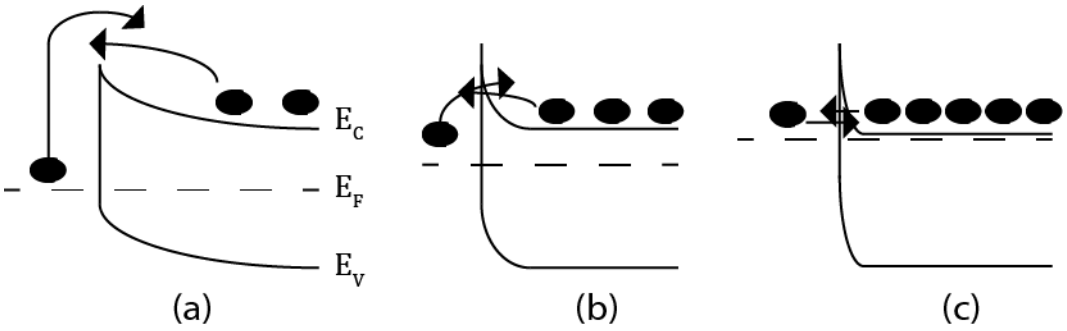

Figure 3.6. The three main conduction mechanisms for depletion contacts on an n-type semiconductor: (a) low-doped with thermionic emission, (b) moderately doped with thermionic/field emission, and (c) highly-doped with field emission.

As the doping concentration increases to an intermediate doping range, thermionic-field emission (TFE) dominates, where electrons are thermally excited to an energy where the barrier is sufficiently thin enough for quantum mechanical tunnelling to take place. The current density due to TFE can be expressed as equation 3.16, where the relative contributions of the components depend upon temperature and doping concentration.

$$J_{TFE} = \frac{A^{**}T\sqrt{\pi E_{00} q(\phi_{Bn} - \phi_n - V_F)}}{k\cosh(E_{00}/kT)} \exp\left[\frac{-q\phi_n}{kT} - \frac{q(\phi_{Bn} - \phi_n)}{E_0}\right] \exp\left(\frac{qV_F}{E_0}\right) \quad (3.16)$$

where $E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{m^* \varepsilon_s}}$ and $E_0 = E_{00}\coth\left(\frac{E_{00}}{kT}\right)$

At extremely high doping concentrations, the depletion width is sufficiently thin that tunnelling occurs close to the Fermi level and therefore this process has a weak temperature dependence compared to TE and TFE. The current density under forward bias for FE can be expressed as

$$J_{FE} \approx \frac{A^{**}T\pi \exp[-q(\phi_{Bn} - V_F)/E_{00}]}{c_1 k \sin(\pi c_1 kT)} \quad (3.17)$$

where $c_1 \equiv \frac{1}{2E_{00}}\log\left[\frac{4(\phi_{Bn} - V_F)}{-\phi_n}\right]$

Each regime can be differentiated in terms of doping density by comparing E_{00} against kT as shown in Figure 3.7 for n-Ge at T = 300 K. When $E_{00} \ll kT$ ($N_D \leq 6\times10^{17}$ cm^{-3}), TE dominates where the probability of electrons tunnelling through the barrier is extremely low and a rectifying contact is formed. As the doping concentration increases, $E_{00} \approx kT$, the contribution of electrons tunnelling increases and the TFE regime becomes the dominant conduction mechanism. When $E_{00} \gg kT$ ($N_D > 1\times10^{20}$ cm^{-3}), FE becomes dominant.

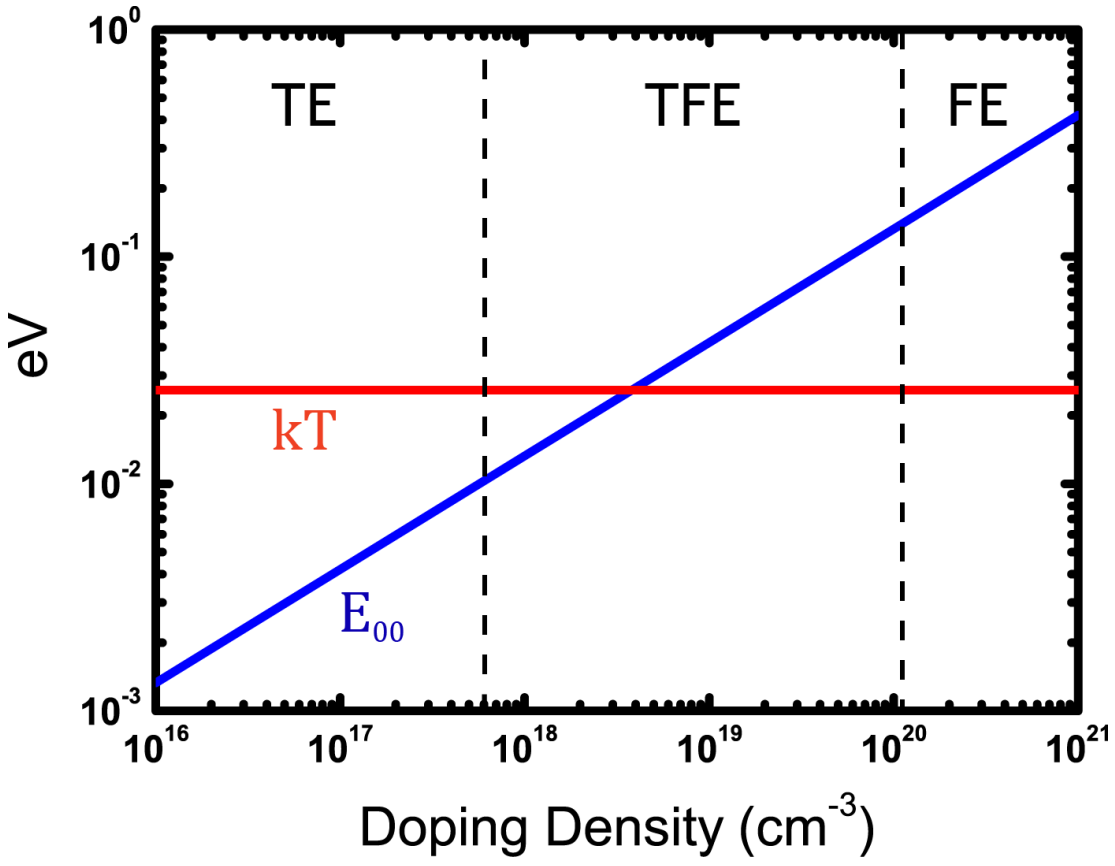

Figure 3.7. The tunnelling characteristic energy (E_{00}) and thermal energy (kT) as a function of doping density for Ge at *T* = 300 K. The black dashed lines indicate the doping densities for each conduction regimen: thermionic emission (TE), thermionic field emission (TFE), and field emission (FE).

3.3 Ge n-type dopant challenges

It is evident from Figure 3.7 to obtain an Ohmic contact to n-Ge, regardless of a large Schottky barrier height then the doping requires being within the TFE or FE regimen. Therefore, a doping concentration of at least $N_D \approx 6\times10^{18}$ cm^{-3} is required. The reason why the majority of the previous work on n-Ge contacts has focussed on unpinning the Fermi level to reduce the Schottky barrier height, compared to narrowing the depletion width through doping, has arisen from the difficulty in achieving sufficiently high doping concentrations. This difficulty stems from the large diffusion coefficients associated with n-type dopants that are many orders of magnitude greater than their p-type counter parts [81] and the difference between the chemical solubility limit and the electrically activated one. As an example phosphorus, which has the highest chemical solubility limit ($\sim 2\times10^{20}$ cm^{-3}) of all the group IV n-type dopants [82], only reaches an electrical activation of $N_D \approx 5\times10^{19}$ cm^{-3} [83] after conventional activation anneals. However, the implantation dose needed to reach this level of electrical activation does severe damage to the Ge, resulting in an amorphous surface [84] and to date no level of annealing has been demonstrated to activate this level of doping. Therefore, for this work it was decided that the n-type doping should be in-situ, whilst the Ge was epitaxially grown on Si, to minimise surface damage and reduce defect formation.

3.4 Epitaxial growth of n-Ge for Ohmic contacts

Collaborators at Warwick University epitaxially grew the n-Ge by using an ASM Epsilon 2000E low-pressure chemical vapour deposition tool. A 650 nm strain relaxed virtual substrate of undoped Ge was directly grown onto a 200 mm p-Si (100) wafer using the two-temperature method [44] (previously discussed in chapter 1) followed by a 830 °C anneal to reduce the threading dislocation density to around 10^7 cm^{-2}. Then, 300 nm of n-type Ge was grown at relatively low-temperatures (< 500 °C) using phosphine as a dopant precursor. The growth conditions were optimised in order to minimise the phosphorous segregation and

to achieve a uniform doping profile across the 300 nm Ge epilayer, and to obtain a high level of electrically activated dopants. The resistivity of the 300 nm n-Ge layer was calculated by electrical measurements using standard four-point probe techniques, and samples all produced nominally identical resistivities ($\sim 0.7\times10^{-3}$ Ω-cm), indicating a doping density of $N_D \approx 3\times10^{19}$ cm^{-3} [85] (see Figure 3.8). This was subsequently confirmed by Hall-effect measurements on mesa etched Hall bar samples with an accuracy of greater than 1 %. Due to this level of dopant concentration, TFE will be the main conduction mechanism and since the W_D is calculated to be narrow (~ 4 nm), quantum mechanical tunnelling of electrons should be the dominate current transport, as shown in Figure 3.6 (b).

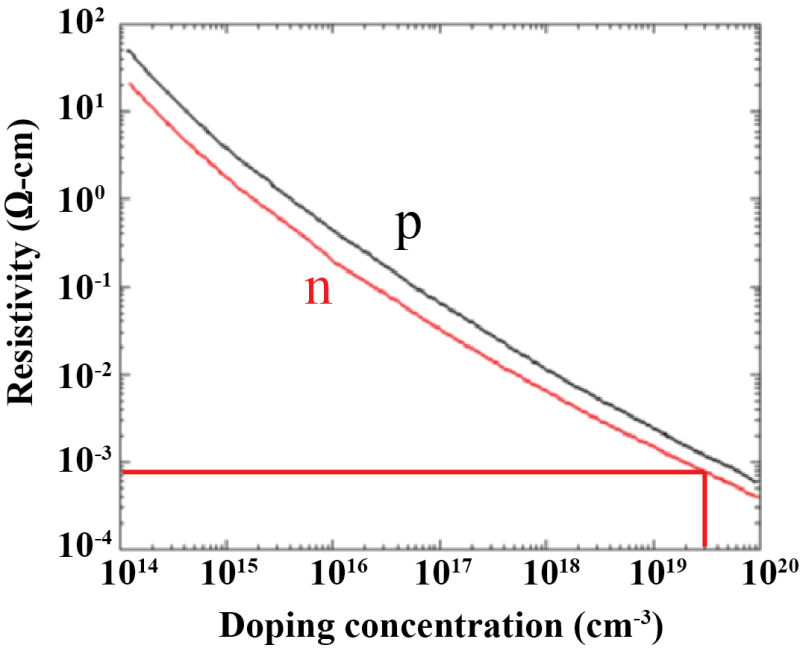

Figure 3.8. The resistivity versus doping density for p and n-type Ge at 300 K [85].

3.5 Metal on n-Ge contacts

As the n-Ge grown by Warwick is at a doping level where conduction should be dominated by TFE it is predicted that an Ohmic contact can be formed, even when there is a large Schottky barrier height. Therefore, it was decided that it would be worthwhile to try direct deposition of metal contacts onto the n-Ge, without using any of the techniques already discussed, such as interfacial layers or surface

passivation. Gaudet carried out a systematic study of 20 transition metals on Ge substrates to identify the optimum metal contact for the integration of Ge into high mobility CMOS. The two germanides that approached the best resistivity phases for current silicide technology in CMOS $(10\ \mu\Omega\text{-cm})$ were NiGe $(22\ \mu\Omega\text{-cm})$ and PdGe $(30\ \mu\Omega\text{-cm})$ [86]. For this work, Ni was chosen over Pd not only because it has a slightly lower resistivity phase but also as the commodity price of Ni is significantly lower (Ni ~ $ 31/kg and Pd ~ $ 12,000/kg) [87]. In addition, Ni starts reacting with Ge at a relatively low temperature (250 °C) [88], is stable over a wide temperature range, has the lowest sheet resistance (R_{sh}), of all the common transition metal-germanium alloys, and does not easily oxidise [86].

3.6 Electrical characterization of the Ni-Ge contacts

To characterise the Ni-Ge contacts and benchmark them against existing literature, it is crucial that the characterisation and metrology correspond to what is commonly used. The specific contact resistivity (ρ_c) is a key parameter for comparing different contact technologies as it is independent of the contact area. To calculate the ρ_c a number of different test structures are available each with their own advantages and disadvantages.

3.6.1 Lateral current flow test structures

Metal-semiconductor contacts fall into two basic categories, current that flows either vertically or horizontally. For the characterization of the Ni-Ge contacts in this work, only lateral current flow test structures were investigated. The main reason behind this choice is that the vertical test structures require ion-implantations to define the vertical contact area. This is difficult to control from the large diffusion coefficients of the dopants as previously discussed and Glasgow University does not have the capabilities to do this. The commonly used test structures that were investigated for this work were the cross-bridge Kelvin resistor (CBKR), the transfer length method (TLM), and the circular TLM (CTLM).

3.6.2 Cross bridge Kelvin resistor

The CBKR test structure allows a direct measurement of the ρ_c, while eliminating the contribution of parasitic resistances [89]. There is one single contact area between the metal and the semiconductor material. The structure consists of four contact pads. Two that are connected to the doped semiconductor and two that are connected to the upper metal arm. Figure 3.9 (a) outlines the basic idea of a CBKR. By applying a current through the semiconductor arm and up through the contact interface into an upper metal layer, a voltage drop can be measured between the two voltage taps and R_c can be calculated from equation (3.18), where ρ_c can then be found from equation (3.19).

$$R_c = \frac{V_2 - V_1}{I} \tag{3.18}$$

$$\rho_c = R_c \times A \tag{3.19}$$

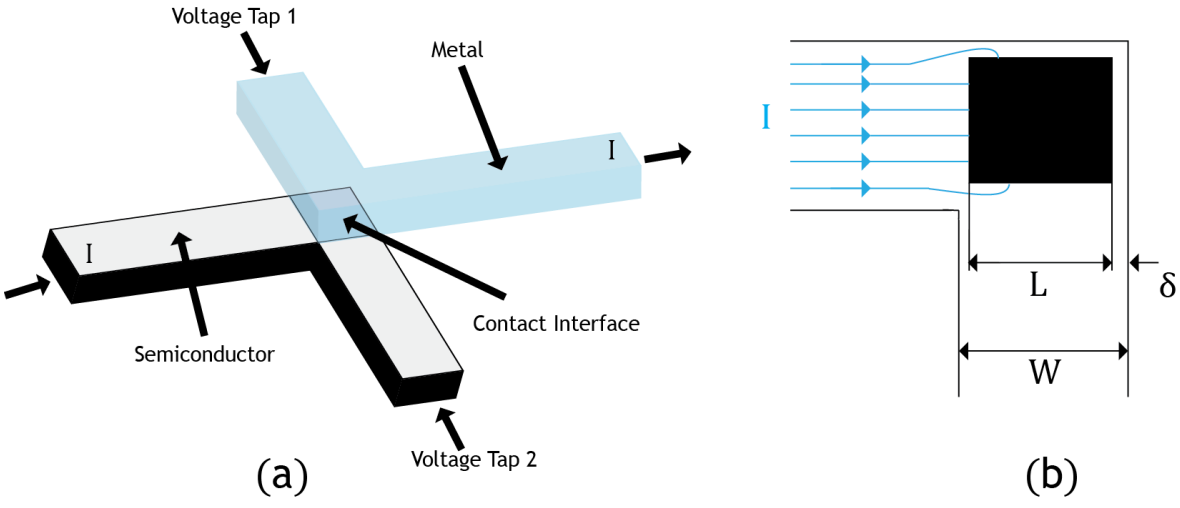

Figure 3.9. (a) A schematic diagram of a four-terminal cross bridge kelvin resistor test structure. (b) The case where there is a misalignment between the contact and the semiconductor arm. The current flows through the contact and the overlap region leading to errors.

Equation (3.19) only accounts for the case where the contact area is the same as the semiconductor arm. In reality, this is difficult to fabricate and there is

normally a misalignment between the contact and the mesa etched sidewall, where W is the width of the semiconductor arm, L is the width of the contact and δ is the misalignment (see Figure 3.9 (b)).

$$\delta = W - L \tag{3.20}$$

The δ misalignment leads to a current that flows around the contact that affects the voltage drop measured and gives rise to a larger ρ_c.

3.6.2.1 CBKR fabrication

CBKR structures require five stages of lithography to fabricate. Electron-beam lithography is required to reduce the δ misalignment to less than 0.1 μm. Etching trenches down to the intrinsic region to define the semiconductor arm. A contact is then deposited by standard lift-off technique. Contact area usually ranges from 0.5 to 20 μm^2 with δ ranging from 0.1 to 0.5 μm. A passivation layer (e.g. SiO_2) is deposited over the semiconductor arm, followed by via-hole etching to the contact. The last stage is to define and deposit the metal upper layer arm. An optical microscope image of a fabricated n-Ge CBKR is shown in Figure 3.10 (a), with a close up of the metal interface seen on the right in Figure 3.10 (b).

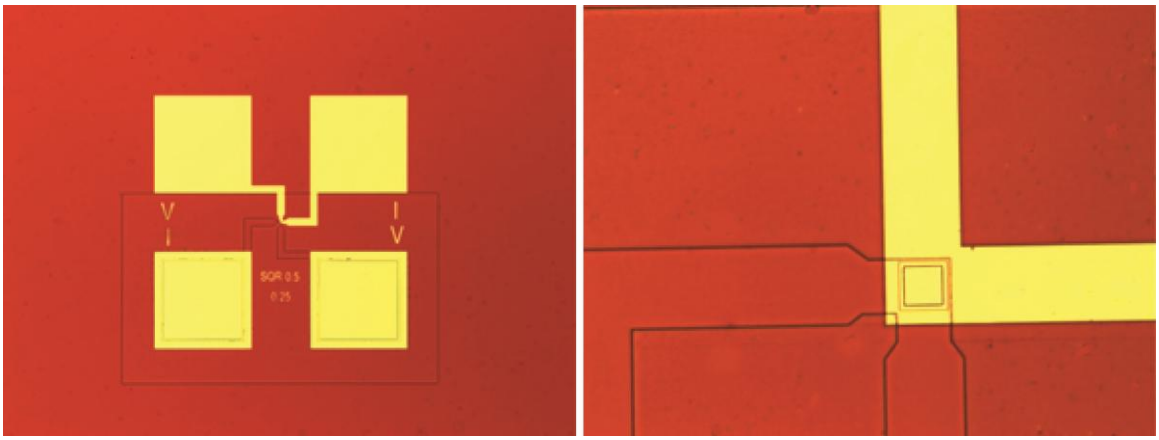

Figure 3.10. (a) An optical microscope image of a fabricated cross bridge kelvin resistor showing the four contact pads. (b) A close up image of the metal interface area.

3.6.2.2 Disadvantages of the lateral CBKR

The biggest disadvantage of the CBKR structure is the δ misalignment between the contact area and the mesa-etched sidewalls. Larger δ leads to higher measured resistance. This δ severely limits the practicality of this structure as its main advantage is meant to be a direct measurement of the ρ_c compared to other test structures that require extrapolation. Thus the actual ρ_c can only be obtained from extrapolating to $\delta = 0$, which therefore requires the fabrication of several CBKR structures with different contact areas and the δ spacing as depicted in Figure 3.11 [90].

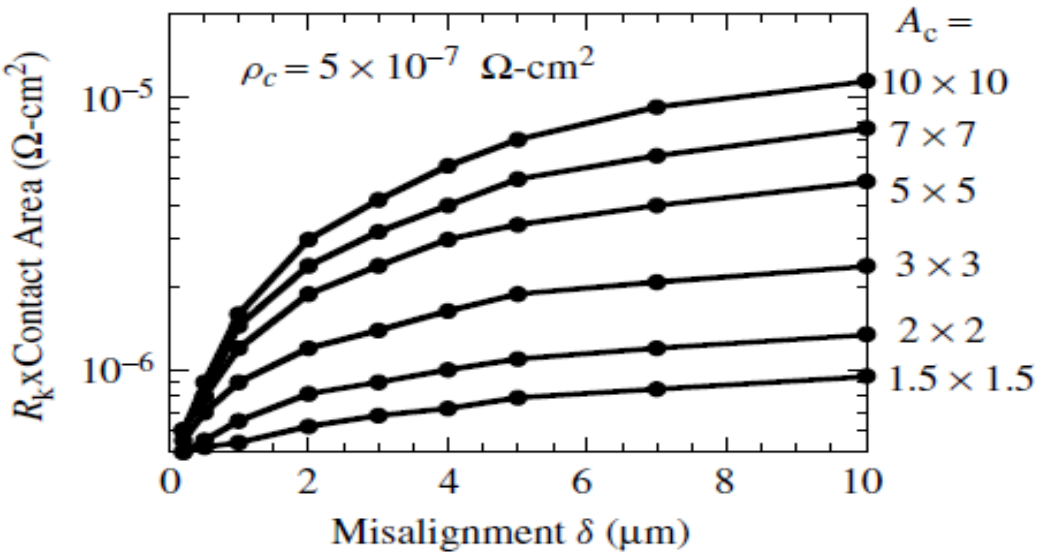

Figure 3.11. The dependence of the contact resistance times the contact area as a function of the δ spacing for the cross bridge kelvin resistor [90].

3.6.3 Transfer length method

The TLM is a planar test structure that consists of numerous identical contacts of width (Z) and length (L), separated by increasing gap spacing (d) as presented in Figure 3.12 (a). The total resistance (R_T) for adjacent contacts is measured and then plotted against gap spacing to extract the R_c. The R_T between any two contacts can be expressed as equation (3.21).

$$R_T = \frac{R_{sh} d}{Z} + 2R_c \tag{3.21}$$

By extrapolating to $d = 0$, this eliminates the contribution of the R_{sh} and only the resistances from the two planar contacts are left, hence $R_T = 2R_c$. The ρ_c can then be calculated from equation (3.19). This structure is far easier to realise compared to the CBKR. It requires only two lithography stages, one to pattern and lift-off the metal contacts and a second stage to isolate the current path by forming a mesa as shown in Figure 3.12 (a) to prevent current crowding.

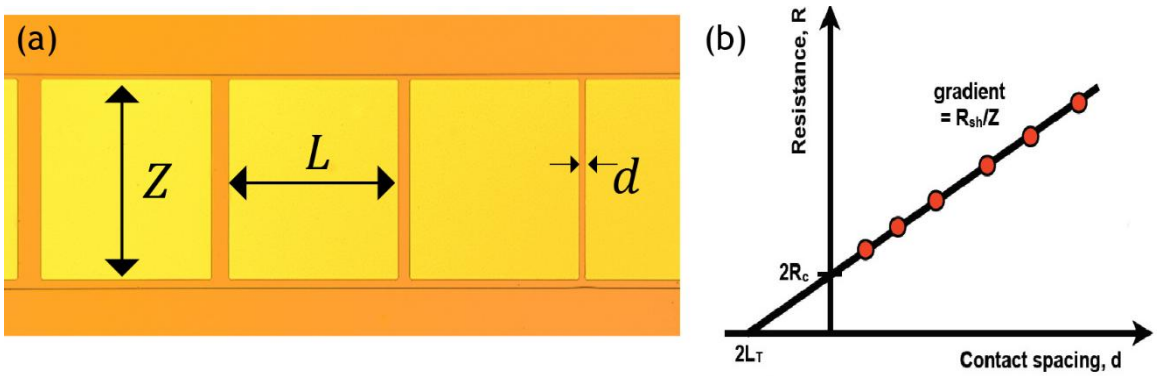

Figure 3.12. (a) An optical microscope image of a fabricated transfer length method test structure. (b) The total resistance for adjacent contacts plotted against the gap spacing.

3.6.3.1 Disadvantages of the TLM structure

One of the issues with the standard TLM structure is the misalignment between the contacts and the mesa, which is required to provide isolation and prevent current crowding. This misalignment (δ), which is also one of the limitations of the CBKR, leads to an incorrect ρ_c. The effect of this can be seen from Figure 3.13 (b) where different δ spacing leads to errors in the extrapolation of the R_c, R_{sh}, and L_T.

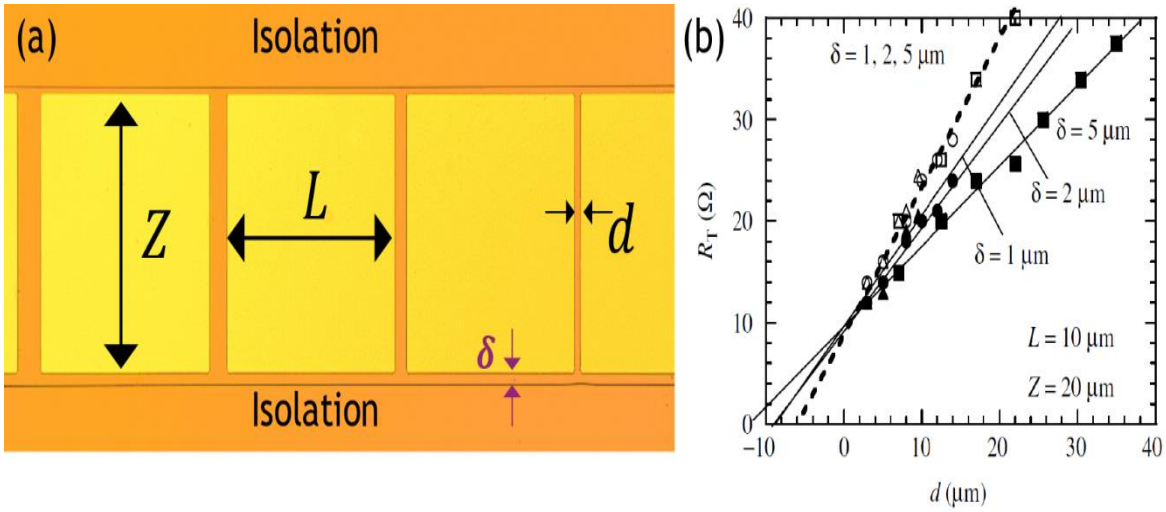

Figure 3.13. (a) A transfer length method structure with current isolation provided by a mesa etch. There is a misalignment (δ) between the edge of the contacts and the mesa. (b) The effect of different δ spacing on the extrapolation [91].

3.6.4 Circular transfer length method

The δ misalignment that introduces errors from the CBKR and TLM structures can be eliminated by using a modified version of the TLM structure, the CTLM. The CTLM is a self-isolating structure, and therefore, no mesa etch is required to prevent current crowding which affects the other structures discussed [92]. The design of the CTLM is presented in Figure 3.14 (a). The structure consists of a metallic outer region and an inner circular contact of radius L. A gap spacing of d separates the inner and outer regions. By measuring the total resistance, R_T, for each gap spacing and using a correction factor C to compensate for the difference between the standard TLM and the CTLM [93], a linear fit can then be applied to the experimental data, where R_c, L_T, and R_{sh} can be extrapolated. Without using the correction factor, there would be an underestimation of the ρ_c .

The R_T between the internal and external contacts can be expressed as equation (3.22).

$$R_T = \frac{R_{sh}}{2\pi}\left[\frac{L_T}{L}\frac{I_0(L/L_T)}{I_1(L/L_T)} + \frac{L_T}{L+d}\frac{K_0(L/L_T)}{K_1(L/L_T)} + \ln\left(1+\frac{d}{L}\right)\right] \tag{3.22}$$

where I and K denote the modified Bessel functions of the first order. For $L \gg 4L_T$, the Bessel function ratios I_0/I_1 and K_0/K_1 tend to unity and R_T simplifies to

$$R_T = \frac{R_{sh}}{2\pi L}(d+2L_T)C \tag{3.23}$$

with

$$C = \frac{L}{d}\ln\left(1+\frac{d}{L}\right) \tag{3.24}$$

The CTLM only requires one lithography step and so can be easily integrated into device fabrication processes as a test structure. Due to the simplicity of the fabrication and the higher accuracy of extracting the ρ_c, CTLM structures were used to characterise the Ni-Ge contacts formed in this work.

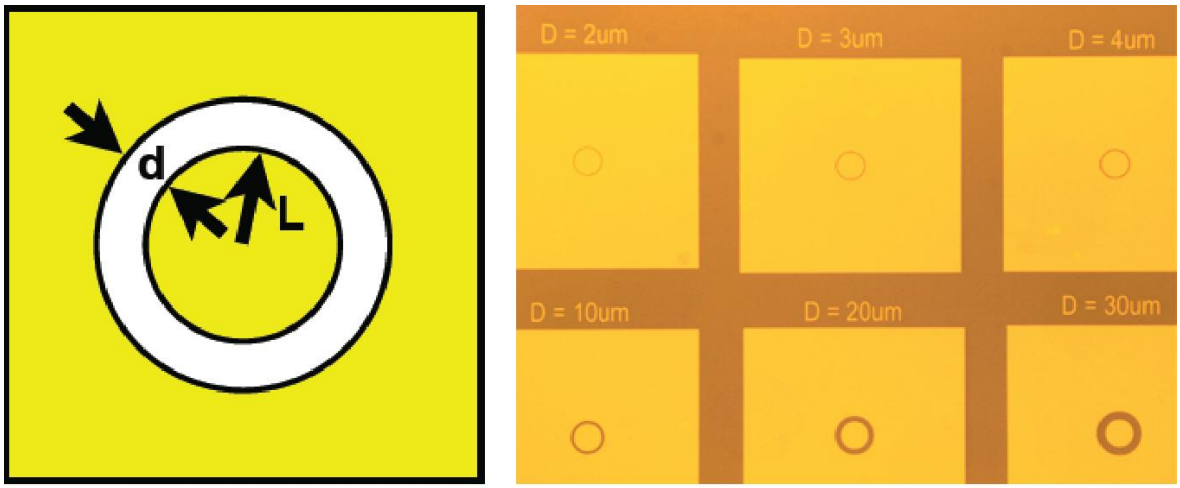

Figure 3.14. (a) A CTLM schematic diagram showing inner circular contact of radius L and a gap spacing of d separating the outer metal contact. (b) A microscope image of fabricated Ni-Ge CTLMs with L = 50 μm and d varied from 1-200 μm.

3.6.4.1 CTLM fabrication

To ensure accurate characterization of the Ni-Ge contacts, the CTLM structures were fabricated by electron-beam lithography. This minimised the errors in gap spacing so that they were < 1 nm and therefore negligible. Scanning electron microscope (SEM) line-width measurements of CTLM structures realised by photolithography, revealed a gap space error of ± 0.6 μm, which leads to errors when extrapolating. 1-cm^2 samples for electrical measurements were prepared by first cleaning in acetone, followed by a rinse in propan-2-ol, and then, the native oxide was removed in a buffered hydrofluoric acid (BHF) solution (5:1). The samples were then immediately placed in a high vacuum (5×10^{-7} mbar) metal deposition system, before 100 nm of Ni was deposited by electron-beam evaporation and patterned by a lift-off process. To promote lift-off of the Ni-Ge CTLMs, a PMMA bi-layer of 8.0 % (2010) / 4.0 % (2041) was used, as described in chapter 2. Along with proximity error correction and curved fracturing in Layout Beamer, this process can provide 30 nm resolutions. Ni films of 100 nm were used initially as it allowed the contacts to be characterised over a wide range of anneal temperatures. All annealing was performed in a rapid thermal annealer (RTA) using nitrogen gas (N_2), and anneal temperatures ranged from 300-600 °C for 30 s.

3.6.5 Ni-Ge electrical characterization

CTLMs had inner contact radii ranging from 50-100 μm, and gap spacing varied from 1-200 μm. All electrical characterization of the CTLMs was carried out using dc current with an Agilent parameter analyser. Four-terminal probing was used to eliminate the parasitic resistance introduced by the probes. Measured current-voltage $(I-V)$ characteristics are shown in Figure 3.15 (a) for a Ni-Ge CTLM (L = 100 μm, d = 150 μm) annealed at 340 °C. At room temperature, the IV characteristic is clearly Ohmic (red line). Ohmic behaviour was also observed for the as deposited unannealed Ni and annealed up to 550 °C before agglomeration of the contact occurred at 600 °C. This suggests that the conduction mechanism is thermionic field emission and to highlight this further, $I-V$ characteristics were measured at 77 K by immersing the CTLMs in liquid nitrogen (LN_2). The $I-V$ at 77 K is shown in Figure 3.15 (blue dash) and is still clearly Ohmic suggesting the tunnelling current must be the dominant transport mechanism. This agrees well with the tunnelling characteristic energy for a doping density of $N_D \approx 3\times10^{19}$ cm^{-3} (see Figure 3.7), which is greater than the thermal energy kT and with a thin depletion width$(W_D \approx 4$ nm$)$, quantum mechanical tunnelling dominates. Figure 3.15 (b) shows a measurement of a L = 100 μm CTLM for a Ni-Ge contact annealed at 340 °C. R_T is plotted against d and a linear fit is applied to the corrected data points to extrapolate the R_c, R_{sh}, and L_T. The specific contact resistivity is then calculated as $\rho_c = R_{sh} \times L_T^2$.

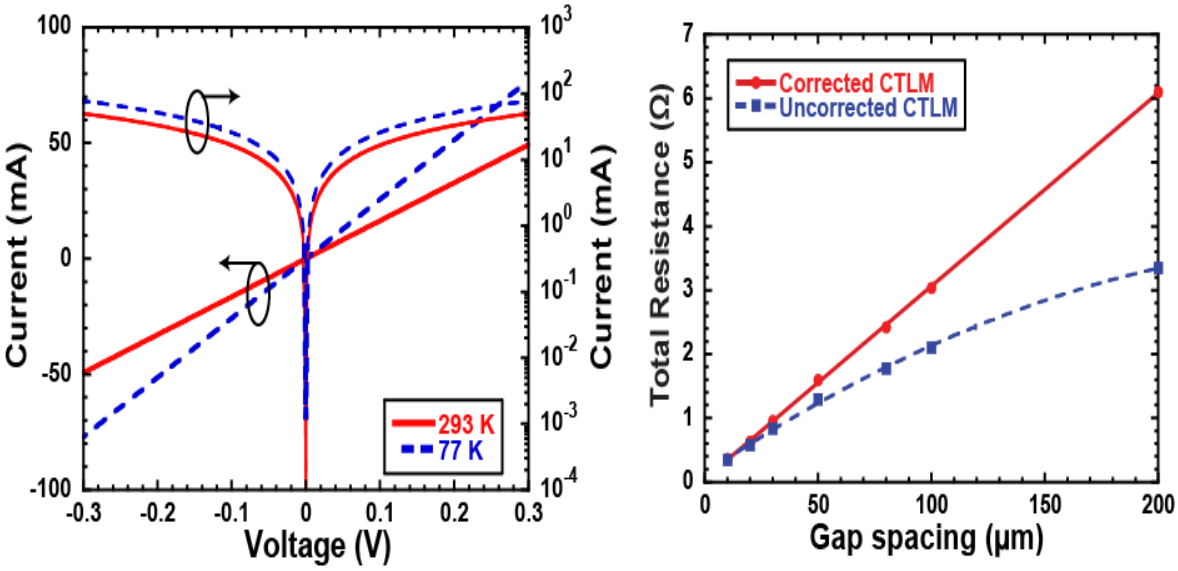

Figure 3.15. (a) The left axis shows the linear current-voltage of the CTLM (L = 100 μm, d = 150 μm) at 293 K (solid line) and at 77 K (dashed line) for a NiGe/Ge contact annealed at 340 °C for 30s, and the right axis is a log plot. (b) R_T as a function of d for the CTLMs. A linear fit is applied the corrected data.

Figure 3.16 shows how the ρ_c varies as a function of anneal temperature. The error bars were calculated by stepping at discrete voltage steps (1000 points) and measuring the R_T at each point and then applying statistical analysis to find the standard deviation. This was done for each set of CTLM structures (L = 50, 75, and 100 μm). The lowest values of $\rho_c = (2.3 \pm 1.8) \times 10^{-7}\ \Omega\text{-cm}^2$ occur at 340 °C with $L_T = 1.2 \pm 0.45\ \mu$m and $R_{sh} = 19.0 \pm 0.2\ \Omega$ [94]. These values are lower than previously published results [66, 69, 70, 72, 73] whilst using a simpler fabrication process.

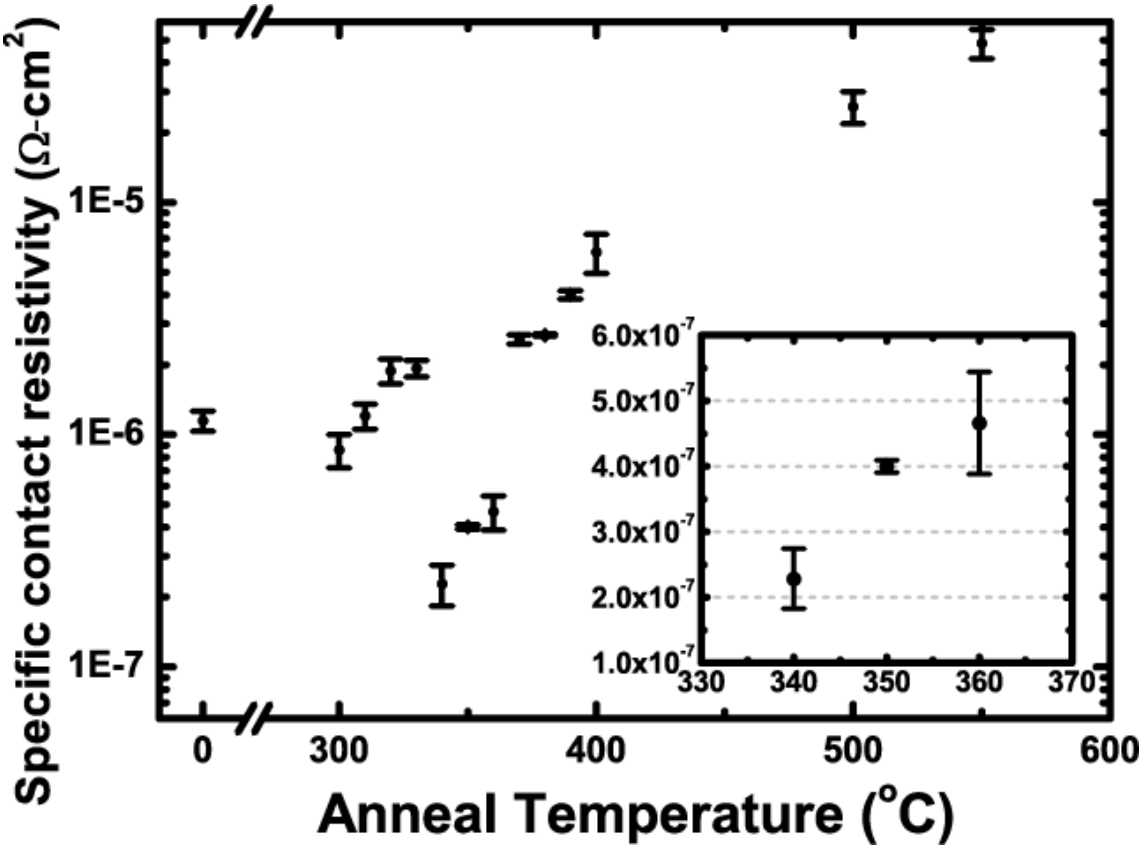

Figure 3.16. The calculated specific contact resistivity for 100 nm Ni on n-Ge contacts over the anneal temperature range 0-600 ℃. The inset shows in more detail the results with the lowest values.

3.6.6 Comparison against other metal Ge alloys

Figure 3.17 shows a comparison of the Ni-Ge alloy against Al and Pt. The NiGe contact annealed at 340 ℃ is an order of magnitude better than the best Pt result and over two orders of magnitude better than the best Al-Ge contact. Above 400 ℃ agglomeration of the Al contact occurred and the contact became Schottky.

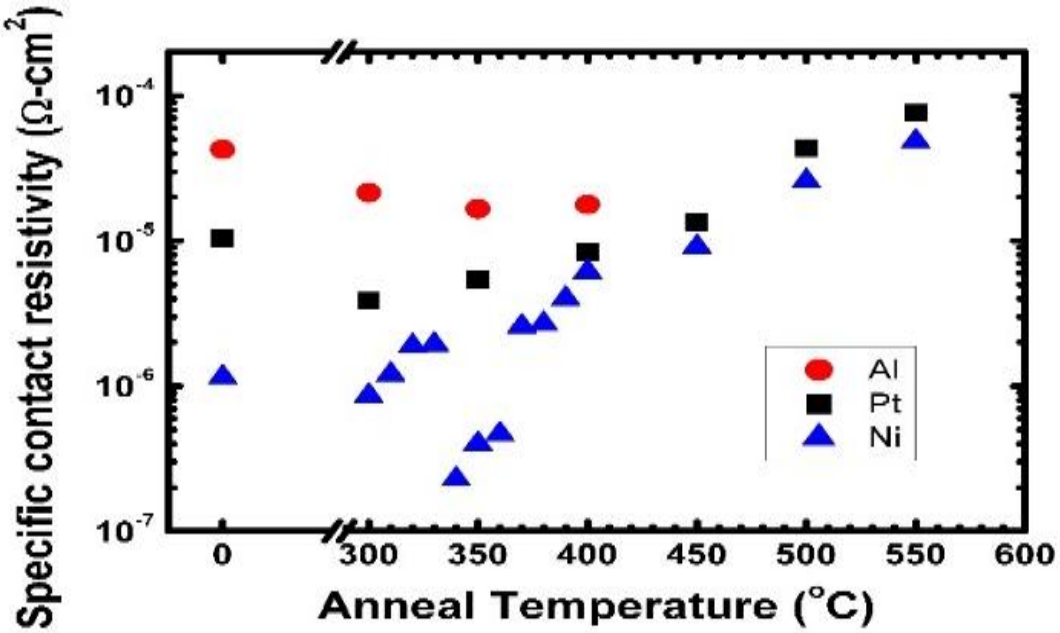

Figure 3.17. A comparison of the extracted specific contact resistivity for Al, Pt and Ni-Ge alloy contacts. Above 400 ℃ agglomeration of the Al occurs.

3.6.7 Phase diagram of Ni-Ge alloys

To understand why the 100 nm Ni-Ge contact annealed at 340 ℃ produces such a low ρ_c it is important to look at the Ni-Ge phase diagram. The phase diagram for Ni-Ge alloys is quite complicated [95, 96] with multiple phases that can grow simultaneously, in particular Ni_5Ge_3 and NiGe [86, 97, 98]. This behaviour is in stark contrast with the sequential growth normally found with thin film reactions with semiconductors, such as Ni on Si. The phase diagram for Ni-Ge alloys is presented in Figure 3.18. The first phase is a Ni rich phase of Ni_5Ge_3 followed by a stoichiometric NiGe phase. Results have shown that NiGe is present after the electron-beam evaporation of Ni onto amorphous and polycrystalline Ge without annealing [97], and the unannealed result in Figure 3.16, suggests NiGe may have formed during the evaporation in the present work. Therefore, NiGe if formed during deposition and isothermal annealing leads to the simultaneous growth of Ni_5Ge_3 and NiGe in the presence of Ni after a critical thickness of 10 -20 nm is reached for Ni_5Ge_3 [97, 98].

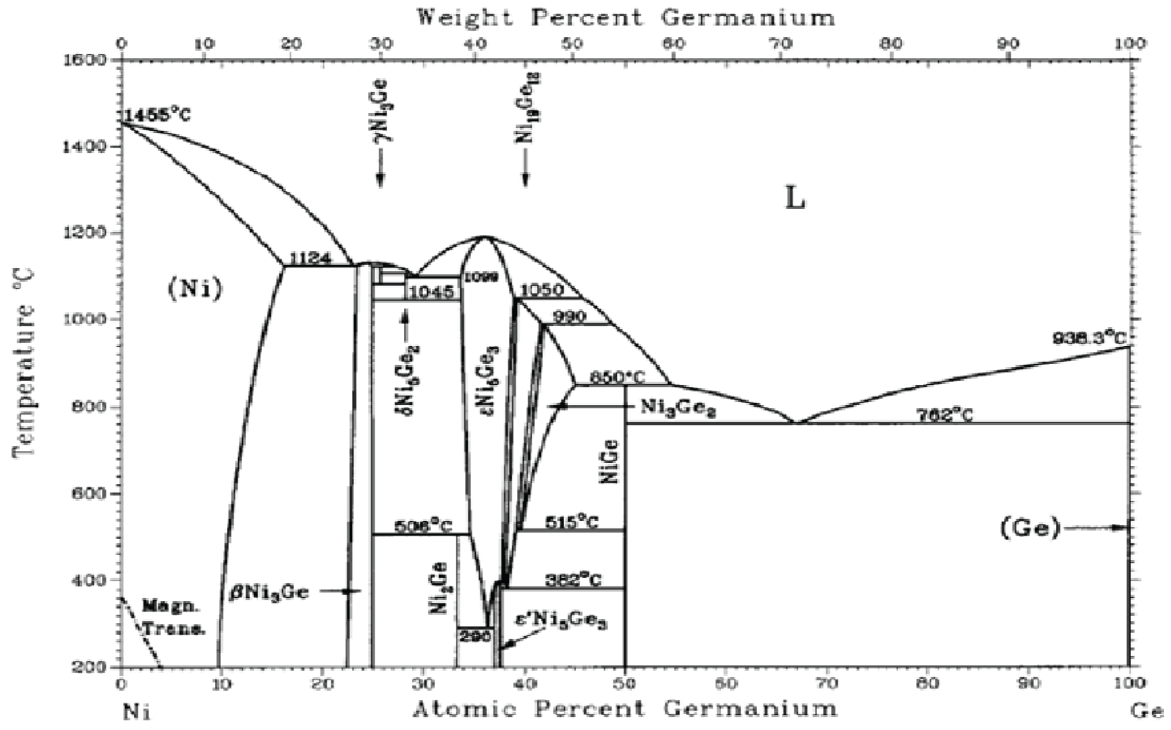

Figure 3.18. The phase diagram for binary Ni-Ge alloy [95].

3.6.8 TEM analysis of NiGe contact

To understand which phase is producing the lowest ρ_c values, transmission electron microscopy (TEM) was undertaken on a sample annealed at 340 ℃ using a FEI Tecnai TF20 operated at 200 kV, with an energy dispersive x-ray spectrometry (EDXS). Dr Ian McLaren from the physics department at the University of Glasgow prepared the sample and took the TEM images. Figure 3.19 shows the typical bright field image showing that the contact consists of two distinct layers. The lower layer in direct contact to the n-Ge was shown by EDXS and diffraction (inset) to be the lower resistivity NiGe phase with an average composition from five quantified spectra of 50 $\pm$ 2 % Ni and 50 $\pm$ 2 % Ge. The upper layer was shown by EDXS to be the higher resistivity Ni_5Ge_3 phase, with the average of five spectra giving 63 $\pm$ 3 % Ni and 37 $\pm$ 3 % Ge in excellent agreement with expectations for Ni_5Ge_3. The diffraction patterns are also consistent with this phase.

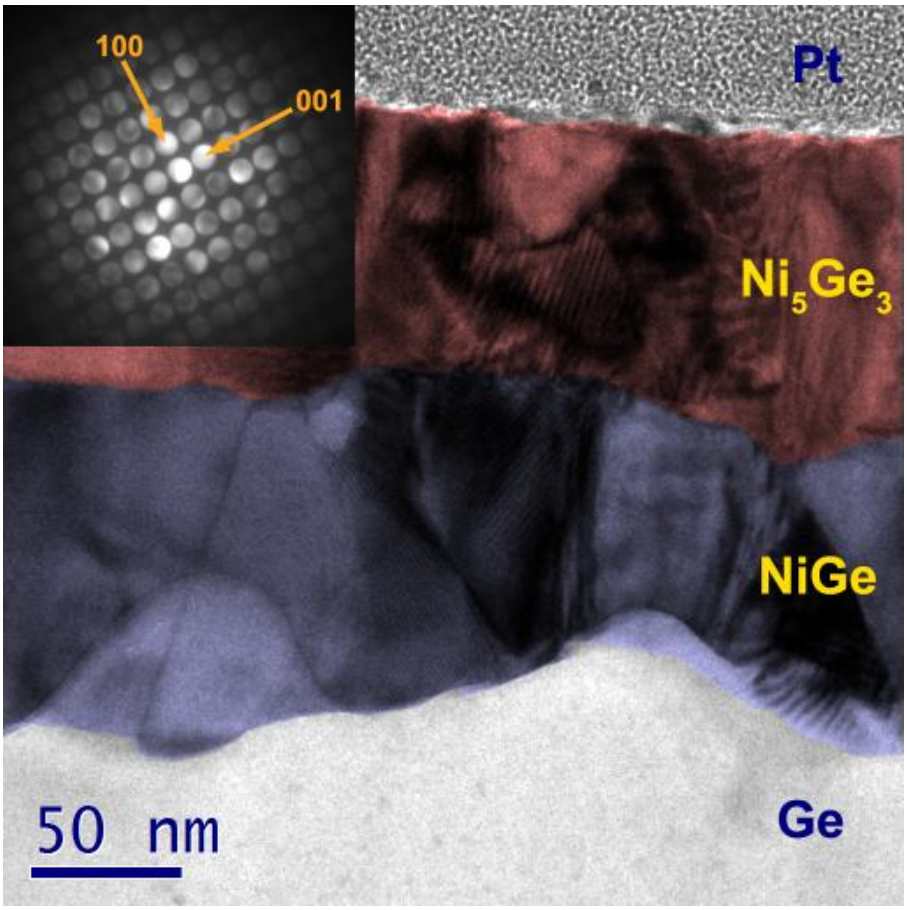

Figure 3.19. A transmission electron microscope bright field image of a Ni-Ge contact annealed at 340 ℃, showing the 2 layers of the contact on the Ge substrate. False colour shading was used to highlight the 2 germanide layers of the alloy contact. The amorphous Pt on top protects the sample prior to preparation by a focused ion beam lift-out process. The insert is a convergent beam diffraction pattern from 1 grain of the lower layer consistent with the [010] zone axis of NiGe in the orthorhombic (Pnma) structure [99].

3.7 Low resistivity NiGe phase

To improve the performance of the NiGe contacts requires methods that produce only the low resistivity NiGe phase as well as to obtain a smooth NiGe/n-Ge interface at the nanoscale level. Two different approaches were proposed, both based on the concept of achieving only the low resistivity NiGe phase. The first approach is a two-step rapid thermal anneal (RTA), where after the first anneal (varied from 250-340 ℃ for 60 s), any remaining Ni is selectively etched in a diluted hydrochloric acid (HCl) solution and then subsequently annealed for a second time (fixed at 340 ℃ for 30 s) to transform the Ni_5Ge_3 into NiGe [87].

Table 3.1 shows the etch rate of Ni and NiGe within HCl:H_2O (1:7) at different temperatures. At 60 ℃ the selectivity between Ni and NiGe approaches ~ 100 times. The second method is a Ni/Ge/Ni contact with the middle amorphous Ge acting as a diffusing layer to form the stoichiometric NiGe phase, since NiGe is formed through the diffusing of both Ni and Ge species compared to Ni_5Ge_3, which is formed solely by Ni species diffusing [100].

HCl:H_2O (1:7) Temperature ℃	**Etch Rate Ni (nm / min)**	**Etch rate NiGe (nm / min)**	**Selectivity**
30	1.56	0.16	10
45	4.06	0.18	23
60	23.66	0.24	99

Table 3.1. The selective etch using HCl:H_2O (1:7) to remove any remaining Ni after the first anneal. A second anneal then follows to transform the Ni_5Ge_3 phase into NiGe.

3.7.1 Electrical characterization of improved NiGe contact

Contact fabrication and electrical characterization for the low resistivity NiGe contacts followed the same process as the 100 nm Ni-Ge contacts. However Instead of depositing 100 nm of Ni, either 20 nm of Ni for the two-step RTA process or NiGeNi (20/20/20 nm) was deposited by electron-beam evaporation and patterned by a lift-off process. By reducing the Ni thickness, it should lead to the detriment of Ni_5Ge_3 at a faster rate. Samples were produced using electron beam lithography to negate gap space errors in the CTLM structures. All annealing was performed in a RTA using N_2. Figure 3.20 shows the characterisation of a 50 μm CTLM structure for a NiGeNi/n-Ge contact annealed at 340 ℃ for 30 s.

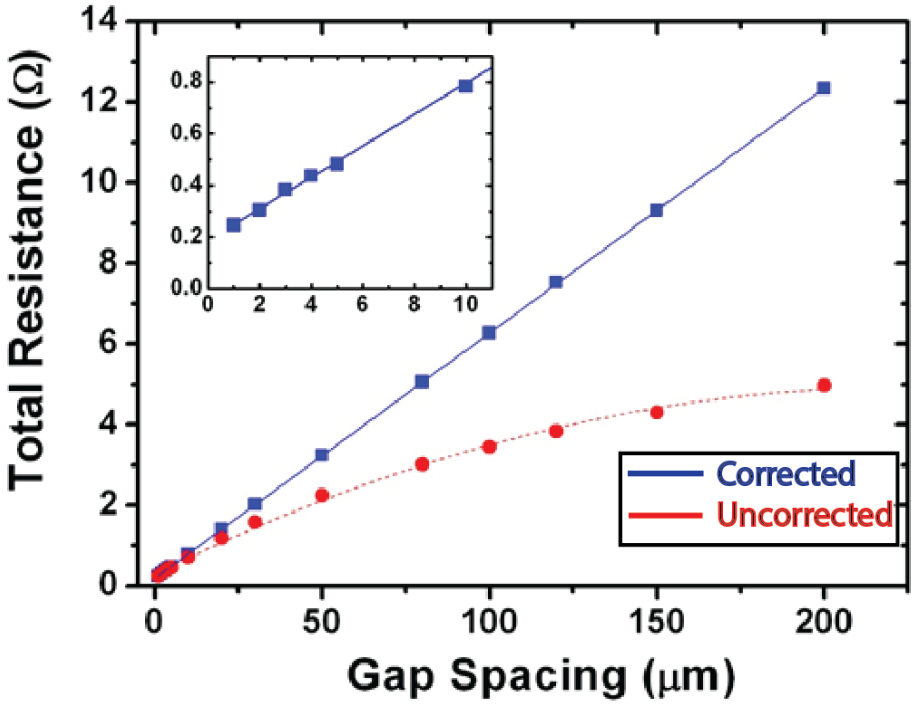

Figure 3.20. The total resistance as a function of gap spacing for a NiGeNi (20/20/20 nm) n-Ge contact annealed at 340 °C for 30 s. The inset shows the extrapolation of the linear fit to the x and y-axis, which allows extraction of the R_c, R_{sh}, and L_T.

Figure 3.21 presents the extracted ρ_c for the two-step RTA process and NiGeNi contact scheme. The effect upon changing the temperature of the first RTA for the two-step process is evident Figure 3.21. At lower temperatures, less Ni reacts with the Ge and is subsequently etched by the selective etch. The change in ρ_c is thus related to the removal of unreacted Ni. It has to be stated that to electrically probe the two-step RTA contacts, a metal capping layer was required and this was either 100 nm of Pt or Pd. This made a significant contribution to the ρ_c and therefore some investigation is required in determining the optimum capping layer and pre-clean treatment before deposition. The best results came from the NiGeNi contact scheme, annealed at 340 °C for 30s with $\rho_c = (1.68 \pm 0.4) \times 10^{-7}\ \Omega\text{-cm}^2$. This is an improvement upon the 100 nm Ni film annealed at 340 °C.

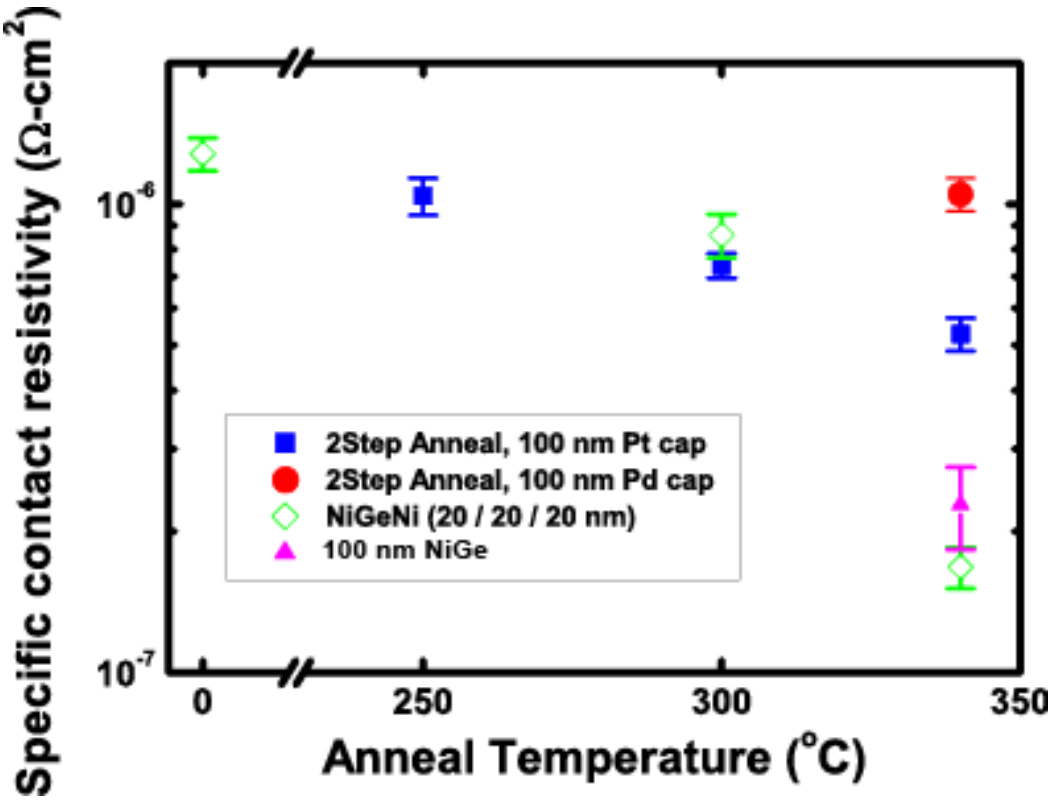

Figure 3.21. The specific contact resistivity for the two-step RTA process with either 100 nm Pt cap layer (squares) or 100 nm Pd (circles) and the NiGeNi (diamonds) contacts. For comparison, the 100 nm Ni contact annealed at 340 ℃ is also shown (triangle).

3.8 Comparison with literature

Method	Reference	Substrate Doping (cm^{-3})	ρ_c (Ω-cm^2)
Conventional contact with ion-implantation and standard activation anneal			
P with Ti/Al P with Ni	[101, 102]	$2\text{-}3\times10^{19}$	$\geq10^{-4}$
Co-implanted P+Sb with Ti/Al	[103, 104]	7×10^{19} 1×10^{20}	2.1×10^{-6} 8.0×10^{-7}
Co-implanted P+Sb with Ni	[104]	7×10^{19}	5.5×10^{-7}
Conventional contact with ion-implantation and laser annealing			
Sb with Al/Ti As with Ni As with Ni P with Ni	[105] [101] [106] [107]	1×10^{20} 6.0×10^{19} 3.0×10^{19} 6.0×10^{19}	7.0×10^{-7} 2.0×10^{-6} 8.0×10^{-7} 2.8×10^{-7}
Fermi level depinning schemes			
Al/TiO_2/n-Ge	[108]	3×10^{19}	1.3×10^{-6}
Ti/ZnO/n-Ge	[109]	2.5×10^{19}	1.4×10^{-7}
Conventional contact on in-situ doped n-Ge (This work)			
P with Ni	[94]	3×10^{19}	$(2.3\pm1.8)\times10^{-7}$
P with NiGeNi	[110]	3×10^{19}	$(1.6\pm0.4)\times10^{-7}$

Table 3.2. A comparison of the best metal contact technologies to date on n-Ge.

Table 3.2 compares the best contact technologies to date on n-Ge. Conventional contacts on n-Ge doped by ion-implantation with a standard activation anneal, show relatively large ρ_c ($\geq10^{-4}$ Ω-cm^2). This is due to a combination of the Fermi level pinning and the low electrical active dopants caused by defects due to the high implantation dose required. These defects act as acceptor states and therefore, reduce the electrically active n-type doping concentration [111]. To overcome the low electrical active doping concentration, a co-implantation of phosphorus and antimony was investigated and yielded higher doping densities ($N_D \geq 7\times10^{19}$ cm^{-3}) and lower ρ_c ($\geq5.5\times10^{-7}$ Ω-cm^2). To date the best results are from ion-implantation with laser annealing ($\approx2.8\times10^{-7}$ Ω-cm^2) an interfacial layer of ZnO ($\approx1.4\times10^{-7}$ Ω-cm^2), and a NiGeNi on in-situ doped Ge

$((1.6\pm0.4)\times10^{-7}\ \Omega\text{-cm}^2)$. The Ti/ZnO/n-Ge contact works by unpinning the Fermi level and the ZnO series resistance is reduced by doping. This is quite a difficult contact scheme to implement, as an ultra-thin ZnO layer (1.5 nm) is required. Comparison of different contact schemes on n-Ge against the NiGe and NiGeNi contacts formed on in-situ doped Ge show that in-situ doping during epitaxial growth is an attractive way to achieve low ρ_c, which is most likely due to the high electrically active dopant concentration due to the minimised defects that are introduced by ion-implantations.

3.8.1 Future Techniques

To achieve an even lower ρ_c than the NiGeNi contact scheme formed in this work will require larger doping densities. This could be achieved by ion-implantations with laser annealing as shown from [105] but it has already been discussed that implantations cause surface defects (p-type vacancies) and laser annealing is an expensive technology to implement. A simpler method could be to use a spin on dopant on the n-Ge surface and then deposit the Ni before an activation anneal. Whilst simultaneously annealing the contact and activating the dopants this has the effect of dopant segregation at the NiGe/Ge interface, which has been shown to increase the doping density and reduce the Schottky barrier height quite significantly [112]. This is also known as the “snow plough effect”.

3.9 Summary

It has been difficult to achieve an Ohmic contact to n-Ge due to severe Fermi level pinning that occurs just above the Valence band. This produces a large Schottky barrier height regardless of the chosen metal work function. This has been one of the major roadblocks to the integration of Ge on Si for CMOS electronic and photonic devices. The conventional method to overcome a large barrier height is to dope sufficiently to produce a thin Schottky barrier to allow tunnelling of electrons and form an Ohmic contact. However, it has been shown that it is relatively difficult to achieve a sufficient dopant concentration by ion-

implantation that produces defects that act as acceptor states and lowers the electrically activated dopant concentration. In this work, it was shown that by doing in-situ during the chemical vapour deposition growth; a large dopant concentration can be achieved. From this sufficiently doped n-Ge a low temperature nickel process has been developed that produces Ohmic contacts with specific contact resistivities down to $\rho_c = (1.68 \pm 0.4) \times 10^{-7}\ \Omega\text{-cm}^2$ for anneal temperatures of 340 ℃. The low contact resistivity is attributed to the low resistivity NiGe phase, which was identified by using electron diffraction in a transmission electron microscope. Electrical results indicate that the linear Ohmic behaviour of the contact is from quantum mechanical tunnelling through the Schottky barrier formed between the NiGe alloy and the heavily doped n-Ge.

4 Ge-on-Si light emission

4.1 Introduction

Si photonics is a growing field where the potential for integration with CMOS electronics is the driving force [6]. There are a number of potential applications for Ge-on-Si photonics, including optical interconnects, spectroscopy in healthcare for analysing blood and urine analytes [113] for wavelengths above 1.6 μm. Gas monitoring is also a potential application since CO_2 has a strong absorption line at 2.0 and 2.7 μm wavelengths and CO has strong absorption lines at 1.6 and 2.4 μm wavelengths [114].

For such lab-on-a-chip applications, light emitting diodes (LEDs) or lasers, and photodetectors are required at these wavelengths. Tensile straining Ge modifies its band structure transforming it into a direct bandgap semiconductor. There has been many several approaches to imparting tensile strain into Ge mostly based on free-standing membranes that are difficult to fabricate and contact electrically and have potential problems from the challenge in heat sinking the devices to maintain a constant temperature for constant wavelength emission [115, 116]. An alternative approach is to use process-induced strain, where deposited stressors of silicon nitride, produce strain in the underlying semiconductor [117].

This chapter will investigate the ability to strain Ge in order to make it an efficient light emitting material. Ge is normally associated as a poor light emitting material due to its indirect bandgap structure. Techniques that can be applied to engineer the band structure of Ge through a combination of degenerate n-type doping and tensile strain to become more direct band gap will be discussed. Straining of Ge through high stress Si_3N_4 liners and the development of this process will then be presented. The fabrication of n-Ge light emitting diodes (LED) covered with high stress Si_3N_4 will be presented along with optical characterization results. It will be shown that the devices are too large to adequately strain by high stress S_3iN_4 films and therefore features below a micron are realised through nano-pillars. Photoluminescence measurements of the pillars will show that the emission

wavelength has shifted to longer wavelengths compared to bulk Ge, indicating tensile strained Ge.

4.2 Basics of semiconductor light emission

Interband light emission from a semiconductor is generated by radiative recombination between an electron from the conduction band combining with a hole in the valance band. This process is depicted in Figure 4.1 for a direct and indirect bandgap semiconductor. The interband transition must conserve momentum, therefore in the direct bandgap case there is a high probability that radiative recombination will occur since the conduction band minima and valence band maxima occur at the same point (k=0). However, in the indirect bandgap case, a phonon is required to conserve momentum, therefore this is a much slower process, and so non-radiative processes dominate recombination.

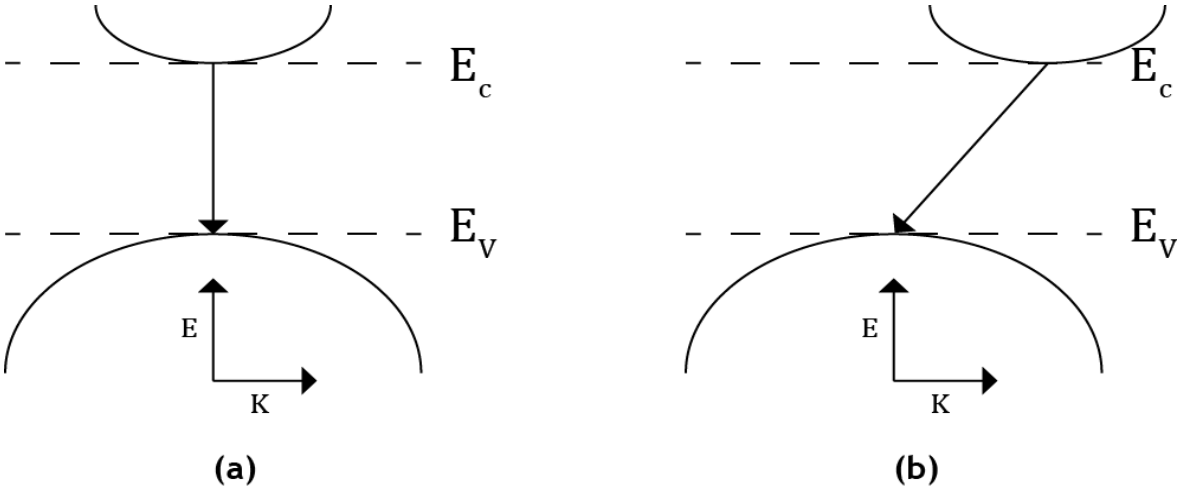

Figure 4.1. A schematic diagram of an Interband transition for (a) a direct bandgap semiconductor and (b) an indirect bandgap semiconductor.

4.3 Ge band structure

Ge has an indirect band structure (see Figure 4.2) and so radiative emission is dependent upon an extremely inefficient phonon-assisted process. However, the direct interband radiative transition in Ge is a fast process with radiative recombination rates that are nearly five orders of magnitude higher than that of

the indirect transition [118]. The direct gap emission of Ge is comparable to that of the direct III-V materials. The challenge is then to increase the number of electrons available for the direct transition. Fortunately, this is possible as the difference between the indirect and direct is only 136 meV as shown in Figure 4.2.

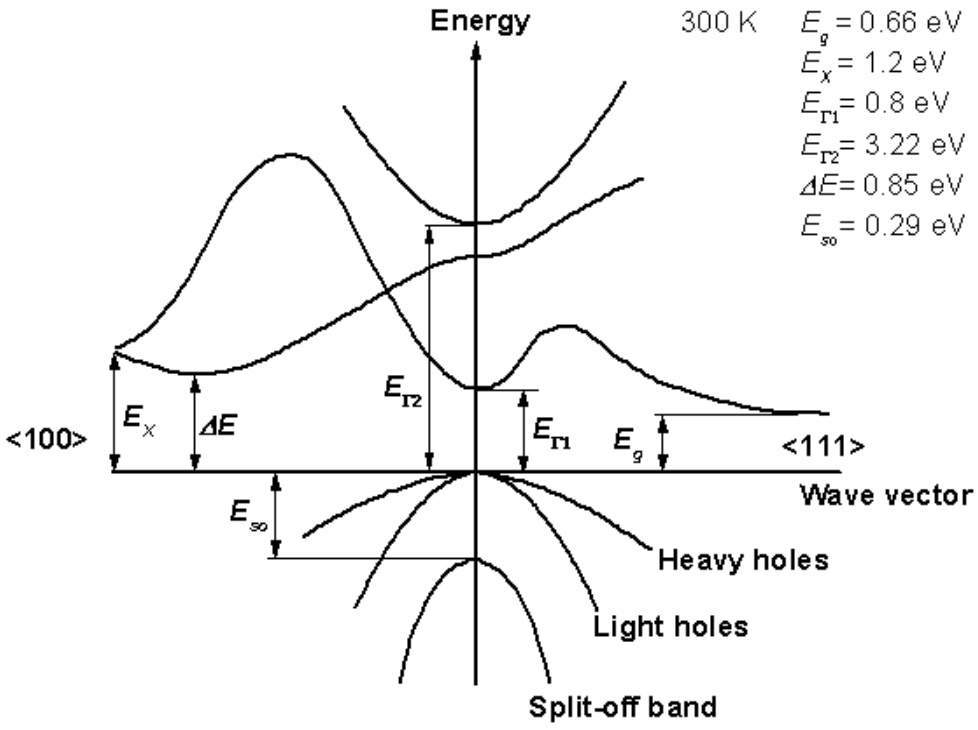

Figure 4.2. Ge band structure at 300 K [119].

In addition, it is clear from Figure 4.2 that the Valence band (E_V) consists of a light-hole (LH), a heavy-hole (HH), and a split-off band. The LH and HH bands are degenerate at the Γ point (k = 0), which is the maximum of the valence band. In Ge, the lowest energy point of the conduction band occurs at the L point (k=<111>). It is evident that there are two energy gaps $E_{\Gamma 1}$ and $E_{\Gamma 2}$ between the conduction band and the valence band at the Γ point. Since $E_{\Gamma 2}$ is significantly larger in energy compared to $E_{\Gamma 1}$, there is hardly any electrons found at these energy levels so that their contribution can be neglected.

4.3.1 Ge band structure under injection

The electron and hole distributions of Ge at equilibrium under no strain are depicted in Figure 4.3. The interband optical transitions require excess carriers that can be injected by either electrical or optical pumping. There are a non-negligible amount of electrons in the Γ-valley owing to the small energy difference (136 meV) between the direct and indirect band gap of Ge.

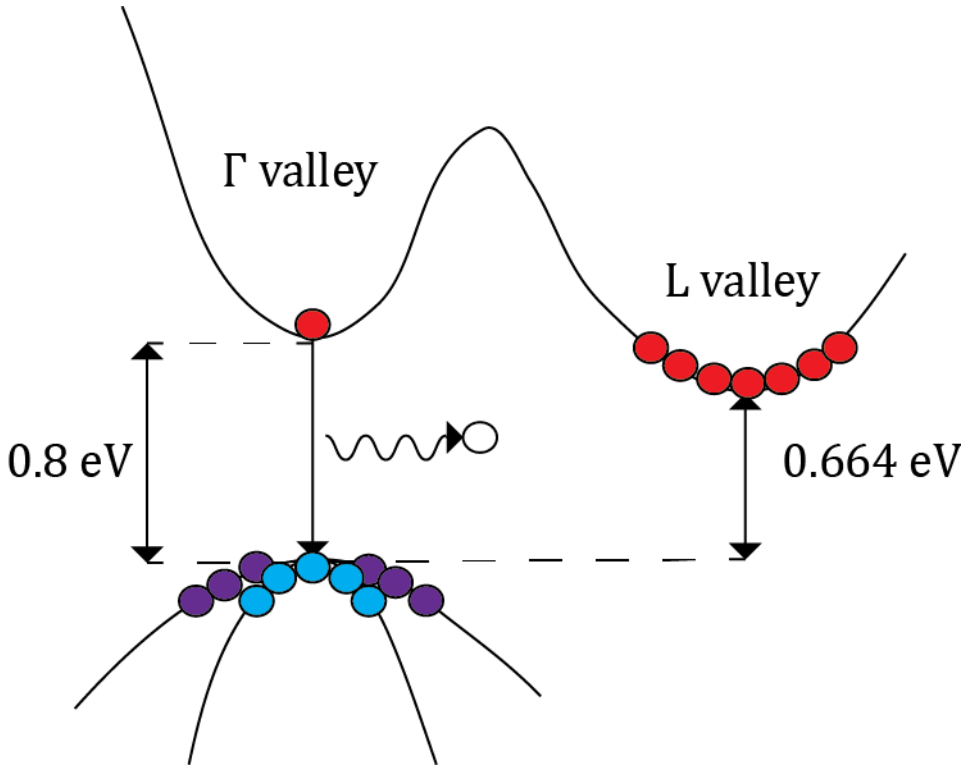

Figure 4.3. A schematic diagram of the electron and hole distribution of intrinsic Ge under no strain at equilibrium.

An excess of electrons in the Γ-valley leads to radiative recombination with the holes in the valence band, which as previously stated is a highly efficient light emission process. However, overall the radiative efficiency remains low due to the majority of injected electrons residing in the L-valleys, which recombine non-radiatively. Therefore, to improve the light emission efficiency in Ge requires more injected electrons to be pumped into Γ-valley for the same carrier injection concentration.

4.4 Ge band structure engineering

A number of approaches to increase the direct recombination efficiency have been investigated. Firstly, degenerate n-type doping of Ge increases the Fermi level so that it resides inside the Γ-valley band [120]. Since the majority of states in the L-valley are filled, electrons injected into the conduction band have far fewer states in the L-valley available that they can scatter into through acoustic phonon scattering thereby increasing the ratio of direct to indirect recombination. Figure 4.4 is a plot of the Fermi level as a function of n-type doping for Ge under 0.25 % tensile strain.

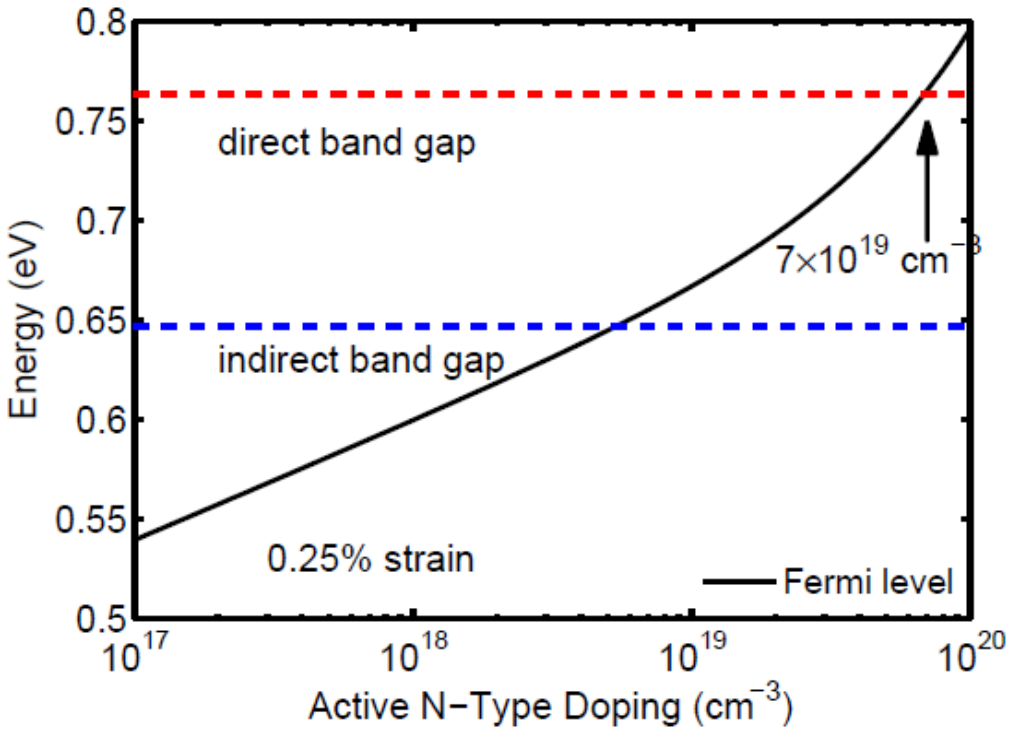

Figure 4.4. The Fermi level as a function of the active n-type doping concentration in 0.25 % tensile strained Ge [120].

4.4.1 Tensile strained Ge

Ge under tensile strain will experience a reduction of the Γ- and the L-valley band energies with respect to the valence band as presented in Figure 4.5. For Ge-on-Si, it is the in-plane component of strain that reduces the energy of both

the Γ-valley and L-valley band edges with respect to the valence band edge [121, 122]. In the valence band, the LH and HH become non-degenerate with the uniaxial component of strain, Due to the different deformation potentials the Γ-valley band energy is reduced in energy more than the L-valley for the same level of tensile strain as shown in Figure 4.5.

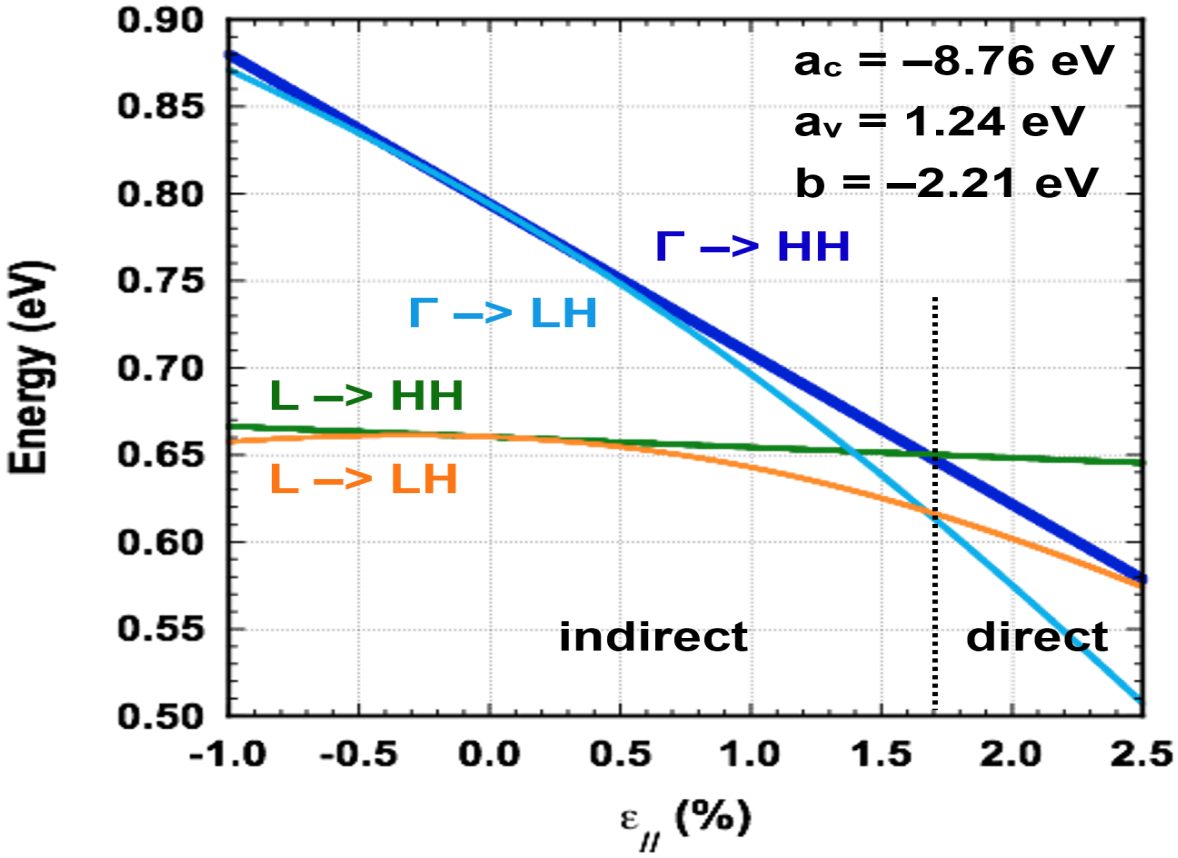

Figure 4.5. A plot of the deformation potentials for the direct and indirect band gaps of Ge under in-plane tensile strain.

The choice of deformation potential is important since it significantly changes the energies of the different transitions. Theoretically, Ge is predicted to become direct bandgap with biaxial tensile strain between 1.7 - 2.5 %, depending on which deformation potential is considered [122-129]. Figure 4.6 depicts the electron and hole distribution for Ge with 1.7 % biaxial tensile strain. For direct bandgap Ge the amount of electrons in the Γ-valley available for radiative recombination increases.

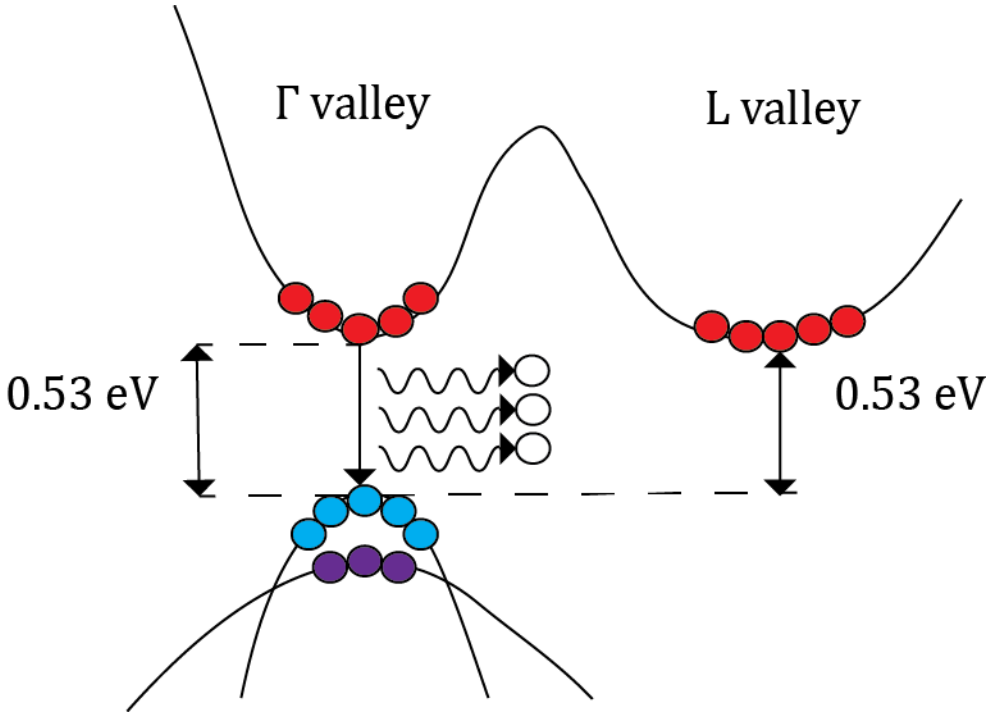

Figure 4.6. A schematic diagram of the electron and hole distribution of Ge with 1.7 % biaxially tensile strain under injection.

4.4.2 Combination of degenerate doping and tensile strain

The strain required to transform Ge into a direct bandgap semiconductor also shifts the output emission to longer wavelengths ($>2.0\ \mu$m). To maintain emission at telecommunication wavelengths requires a combination of degenerate n-type doping and a small level of tensile strain. For the Fermi level to reside in Γ -valley it requires a doping concentration of $N_D = 7\times10^{19}$ cm^{-3} (see Figure 4.4). This level of doping concentration is difficult to achieve as previously discussed in chapter 3. The first optically [32] and electrical pumped [33] Ge lasers were demonstrated by MIT using a combination of degenerate doping and tensile strain. The optically pumped Ge laser emits at a wavelength of 1.6 μm. The waveguides were grown by selective area growth using UHV-CVD. Doping was done in-situ during the epitaxial growth to a doping density of $N_D \approx 1\times10^{19}$ cm^{-3}. After cooling to room temperature, the Ge develops a small amount of tensile strain (0.25 %) due to the thermal mismatch between Ge and Si. The electrically pumped Ge laser was grown by the same method except that a heavily p-doped poly-crystalline Si was

deposited on top to act as a cladding region and also to inject holes into the active Ge region, which in this case had a higher doping concentration ($N_D \approx 4\times10^{19}$ cm^{-3}), achieved by delta doping [130]. The current density to achieve lasing was extremely high (> 300 kA cm^{-2}). Due to the high injection current densities required to fill all available states in the L-valley it is suggested that this could be improved by increasing the doping concentration to reduce the threshold requirements but this would also lead to an increase in free carrier absorption.

4.5 Engineering direct bandgap Ge

To achieve an efficient electrically pumped Ge laser will likely require reaching direct bandgap Ge. Therefore, greater levels of tensile strain than what is produced from the thermal mismatch after growth (~ 0.25 %) are required. Although with increasing tensile strain the corresponding emission redshifts from telecommunication wavelengths, there are still a number of potential applications. Above 1.6 μm including spectroscopy in healthcare for analysing blood and urine analytes [113]. Gas monitoring is also a potential application since CO_2 has a strong absorption line at 2 and 2.7 μm wavelengths and CO has strong absorption lines at 1.6 and 2.4 μm wavelengths [114]. Theoretical modelling of Ge in the literature has predicted extremely large optical gain and low current density thresholds for lasing as the amount of tensile strain is increased [32, 33, 115, 131, 132]. An optical gain larger than 3000 cm^{-1} is predicted for a carrier density of $N_D = 1\times10^{18}$ cm^{-3} and 3 % biaxial tensile strain. This optical gain is larger than the one calculated for GaAs using the same formalism and is much larger than the experimental free-carrier absorption losses [129]. Most approaches to achieving high levels of tensile strain in Ge have been based on membranes.

4.5.1 Tensile strained Ge membranes

Ge freestanding membranes under mechanical stress were investigated with a measured biaxial tensile strain of 0.7 % [132] and 1.9 %, respectively [116]. Another membrane approach is presented in Figure 4.7 where instead of stressing

mechanically, a tungsten stressor is evaporated onto the back of the membrane that results in 0.76 % biaxial tensile strain. Modelling of this structure shows that by increasing from 0.25 to 1 % biaxial tensile strain the threshold current density for lasing decreases from 503 to 151 kA/cm^2 [115]. Therefore, it can be concluded that by increasing the level of tensile strain in Ge it will provide more optical gain and lower thresholds for Lasing.

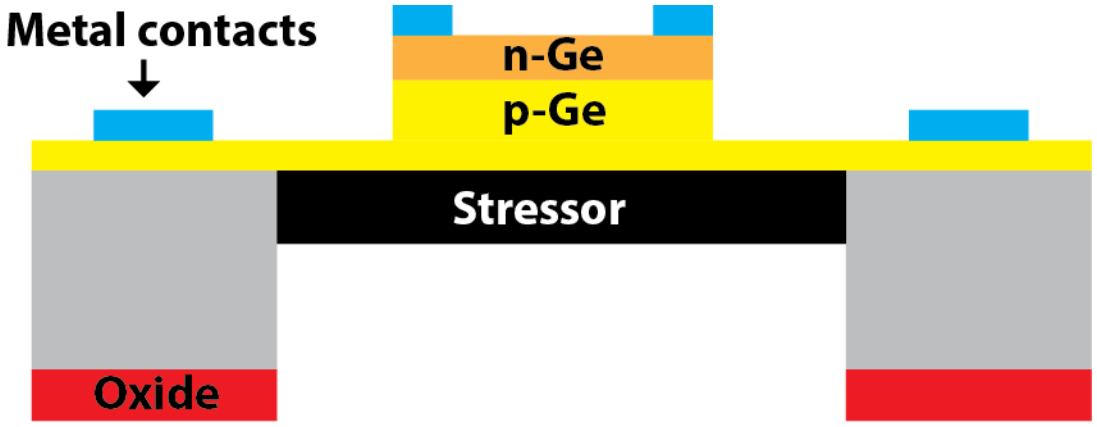

Figure 4.7. A schematic diagram of a highly strained Ge membrane with a tungsten stressor evaporated onto the backside.

4.5.2 Ge membrane disadvantages

The Ge membrane approach to impart high levels of tensile strain would be challenging to fabricate in Si foundries. There would also be some difficulty to contact electrically and potential problems from the challenge in heat sinking the membranes to maintain a constant temperature for constant wavelength emission [115, 116]. Another difficulty with this approach is that thinner membrane films (< 50 nm) are required to increase the strain in the Ge. At such thicknesses, the membrane would not be very robust to mechanical damage. Overall, it would be challenging to realise a stable electrically pumped Ge laser that could be integrated with other Si photonic components. A more simple and robust process would be to use process induced strain, which is currently already used in many commercial CMOS production processes, where deposited strain liners of Si_3N_4, produce uniaxial tensile strain in the channel of MOS transistors to increase the mobility and performance of the device [117].

4.5.3 High stress silicon nitride

An alternative approach to strain Ge is by using process-induced strain, where a highly compressive Si_3N_4 film is deposited over the Ge to impart tensile strain. The stress induced by Si_3N_4 can be used with all types of semiconductor materials and with many different types of device geometry. All deposited films with different lattice constants from the substrate will produce some level of stress in the underlying substrate, typically within a finite distance from the surface. Figure 4.8 demonstrates the stress in a deposited film of Si_3N_4 versus the plasma enhanced chemical vapour deposition (PECVD) RF power. The film stresses obtained ranged from 1.7 to -3 GPa, where the positive sign is tensile stress and the negative sign is compressive stress. The choice of the RF power will influence the deposition rate, stress, and quality of the film. By measuring the refractive index, the quality of the deposited film can be controlled. An excess of Si or N will increase or decrease the refractive index respectively, and result in an amorphous phase as it diverges from the stoichiometric proportions. In the range of RF power that provides a stress between -1.7 to +3 GPa, the refractive index of the deposited film did not change by more than 5 % in value. In order to characterise the stress in the Si_3N_4 film a simple measurement using a surface profiler was undertaken, which provides a resolution of 100 MPa [27].

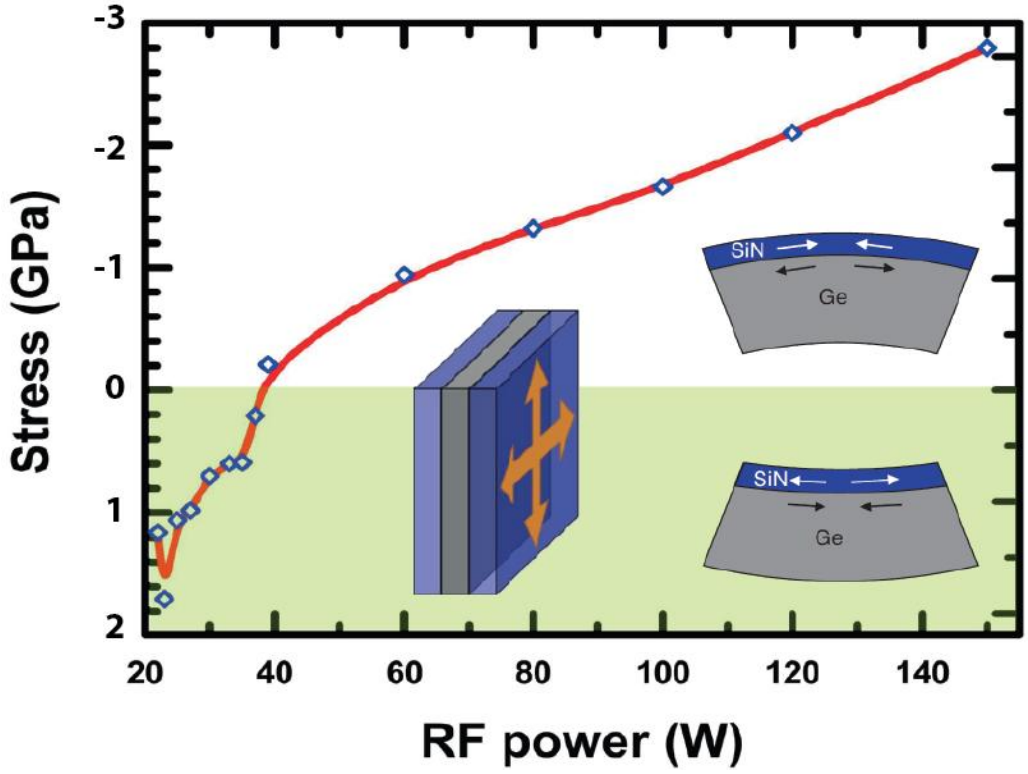

Figure 4.8. The measured stress in a 300 nm thick silicon nitride film as a function of the RF power used during the plasma enhanced chemical vapour deposition.

A blank Si wafer was measured to determine the initial curvature, which directly corresponds to the stress already present in the wafer. After the deposition of the high stress Si_3N_4 film, the curvature was remeasured (see Figure 4.9) and both profiles were used to extract the stress (σ) of the Si_3N_4 film, using the following equation

$$\sigma = \frac{1}{6}\left(\frac{1}{R_{post}} - \frac{1}{R_{prev}}\right)\frac{E}{1-\nu}\frac{t_s^2}{t_f} \tag{4.1}$$

where R_{prev} and R_{post} are the radius of curvature of the substrate before and after the Si_3N_4 deposition respectively. E is the Young's modulus of the substrate, ν is the Poisson coefficient of the substrate, t_f is the thickness of the deposited film, and t_s is the substrate thickness. This equation is derived from the Stoney equation [133] and assumes a linear dependence of the stress applied on the

substrate with the film thickness. Therefore, the stress can be modulated by depositing varying thicknesses of Si_3N_4.

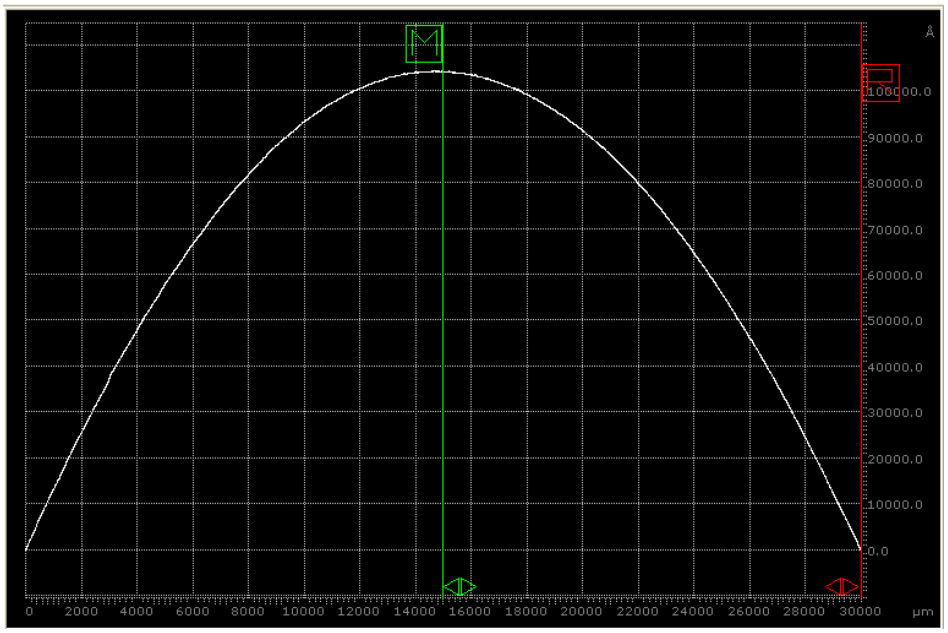

Figure 4.9. The curvature profile measured after the deposition of a high stress PECVD Si_3N_4 (RF= 150 W) film onto a Si substrate.

4.6 Germanium light emitting diode

To investigate the light emission of Ge with Si_3N_4 stressors, light emitting diodes (LED) were fabricated. The Ge epitaxially grown by collaborators in Warwick University to develop Ohmic contacts to n-Ge (chapter 3) was also used to fabricate the n-Ge LEDs. This material was ideal for fabricating LEDs, since it was a p-i-n structure (see Figure 4.10 (a)) with the n-Ge region highly doped ($N_D = 3\times10^{19}$ cm^{-3}), which has been shown to improve the direct band radiative recombination by filling available states in the L-valley. In addition, it has the benefit of being in-situ doped during the epitaxial growth. There will be substantially less defects compared to what would be introduced by the high-energy bombardment that is used for ion implantation, which would introduce non-radiative recombination centres, which are detrimental to light-emitting devices. There is already has a small level of tensile strain in the Ge (0.25 %) due to thermal mismatch at growth. The layer structure for the Ge light emitting diode

is shown in the cross-sectional schematic of Figure 4.10 (a). The devices to be covered with the Si_3N_4 stressors were designed as cylindrical mesas for surface normal characterization and varied from 25 - 500 μm in diameter (see Figure 4.10 (b)).

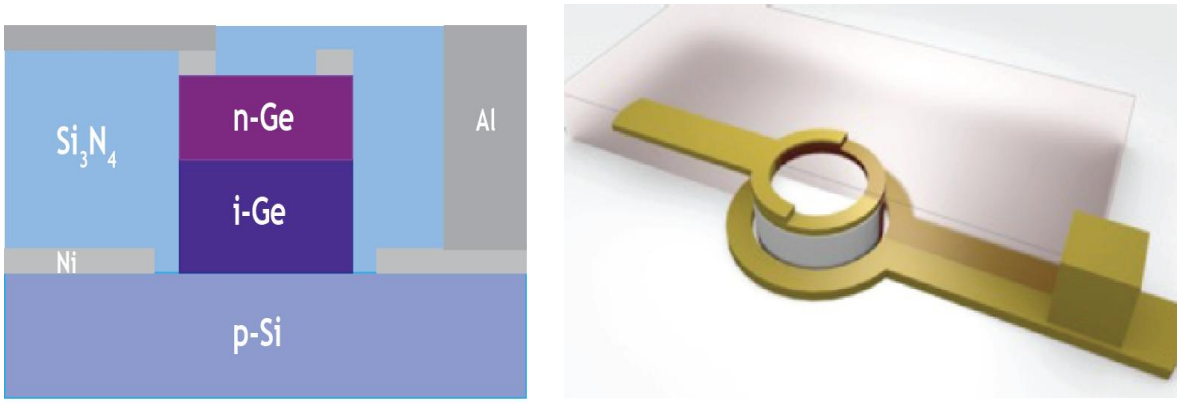

Figure 4.10. (a) A cross sectional schematic of a Ge LED showing the layer structure. (b) A 3-D model of the bulk n-Ge LED.

4.6.1 Fabrication of the Ge LED

The process flow to fabricate the n-Ge LED is presented in Figure 4.11. A process sheet detailing the parameters used in each step is supplied in **Error! Reference source not found.**. The first stage after cleaving a sample of the correct dimension (1 cm^2) is to pattern and lift-off top Ni contacts of 50 nm that were e-beam evaporated. A dry etch mask was then patterned by photolithography before the structures were etched anisotropically using SF_6/C_4F_8 in an ICP-RIE tool to an etch depth of 1 μm. After dry etching, the etch mask was removed and the bottom contact stage was defined before 50 nm of Ni was evaporated. After lift-off, the top and bottom contacts were subsequently annealed in N_2 using an RTA at 340 °C for 30 s. This process produces low resistivity contacts to both Si and Ge. The LEDs were then covered with Si_3N_4 deposited using a PECVD tool, using a mixture of $SiH_4/NH_3/N_2$/He gasses. The proportion and quantities of gas in the chamber were identical for all depositions. The plasma power was varied from 40 - 150 W (0 to - 3 GPa) to induce tensile strain into the Ge.

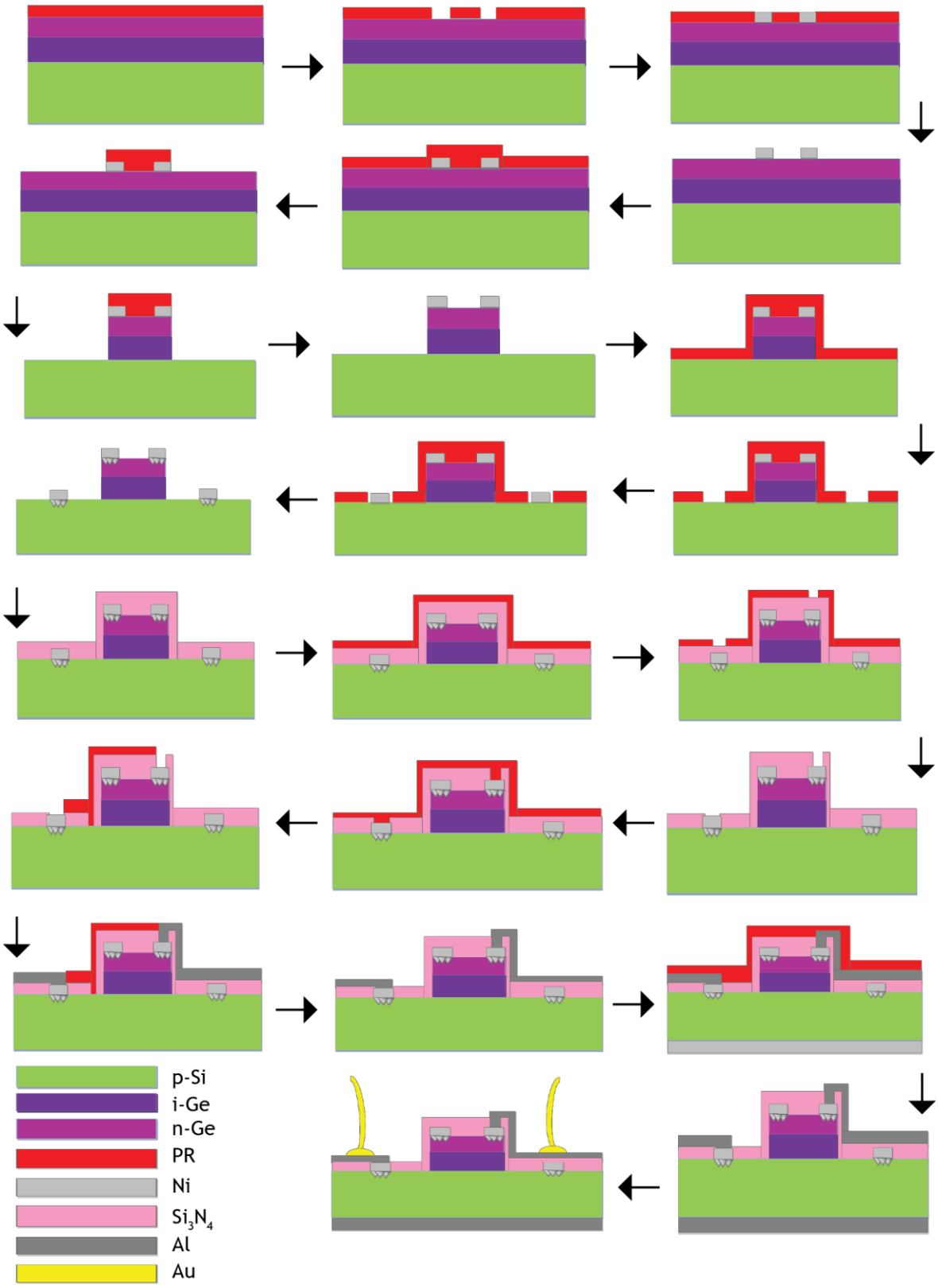

Figure 4.11. A schematic diagram of the fabrication steps to realise the n-Ge light emitting diode.

Via holes were then patterned before etching in an RIE tool with the gases CHF_3/N_2 were the Ni contacts were used as an etch stop. The last stage of lithography was to pattern and lift-off 1 μm of Al bond pads that were sputtered coated. A back mirror of 200 nm of Al was then evaporated. As the emission of the device will be spontaneous and the Si is optically transparent to wavelengths greater than 1.1 μm, the mirror should reflect any photons to the surface for emission. After the deposition of the mirror, the samples are cleaved and wire bonded to a chip carrier for characterization by continuous-wave and pulsed excitation. An optical microscope image of fabricated n-Ge LEDs are presented in Figure 4.12 (a). The $I-V$ characteristics for a 300 μm diameter device is presented in Figure 4.12 (b) and it clearly shows diode behaviour.

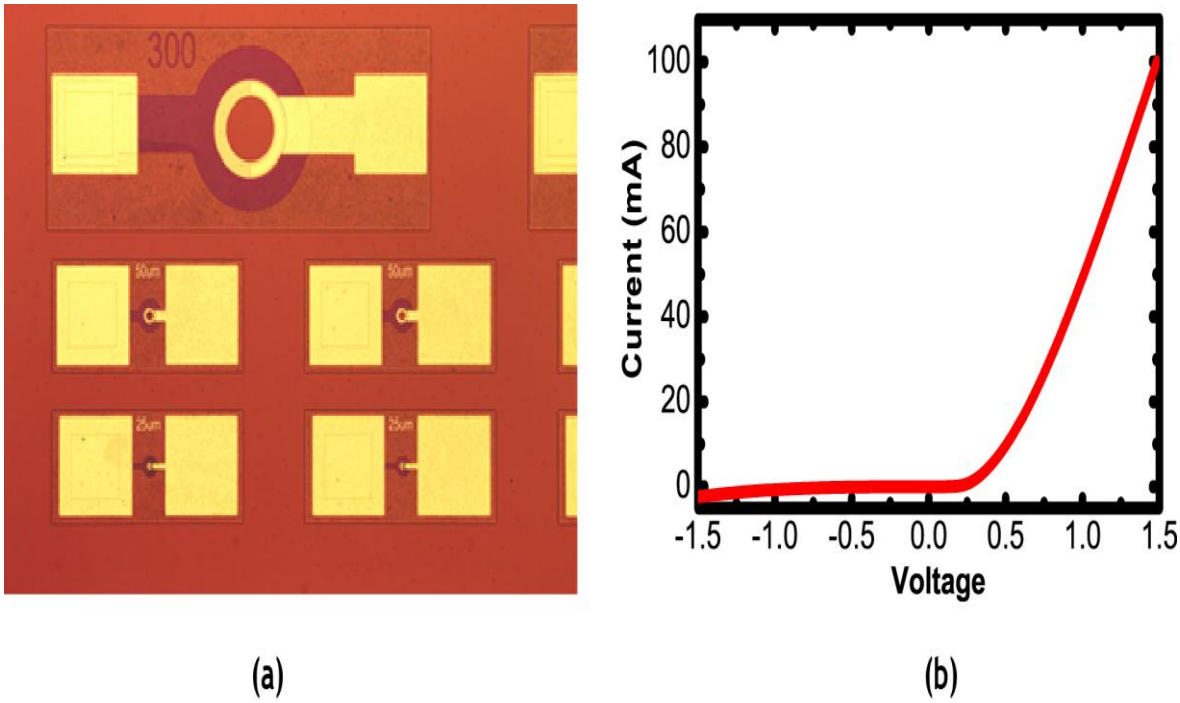

Figure 4.12. (a) Optical microscope image of fabricated n-Ge LEDs. (b) The current-voltage characteristic of a 300 μm diameter n-Ge light emitting diode.

4.7 Characterization of the n-Ge light emitting diode

4.7.1 Characterization setup

The setup for optically characterizing the Ge LEDs is shown in Figure 4.13. Electroluminescence from the device under test is collected by a parabolic mirror and focussed onto a second parabolic, which then focusses the emission into a Bruker Vertex 70 Fourier transform infrared (FTIR) spectroscopy system for analysis. A calcium fluoride (CaF) beam-splitter and a Peltier cooled extended InGaAs detector with a detection range of 0.85 to 2.5 μm were used to obtain the spectra from the devices. Initial interferograms were obtained in rapid scan mode with the measurements being the average of 1000 individual scans to improve the signal to noise level. Step-scan FTIR measurements were then undertaken to significantly reduced blackbody emission from the devices by pulsing at 10 KHz with duty cycles ranging from 1-10 %. The setup for step-scan uses an external lock-in amplifier and the bias to the LEDs was supplied through an Agilent pulse generator, which can supply a maximum current of 2 A. The duty cycle is tuneable from 0.1 to 95 %. A lower duty cycle allows the sample to dissipate the Joule heating between pulses.

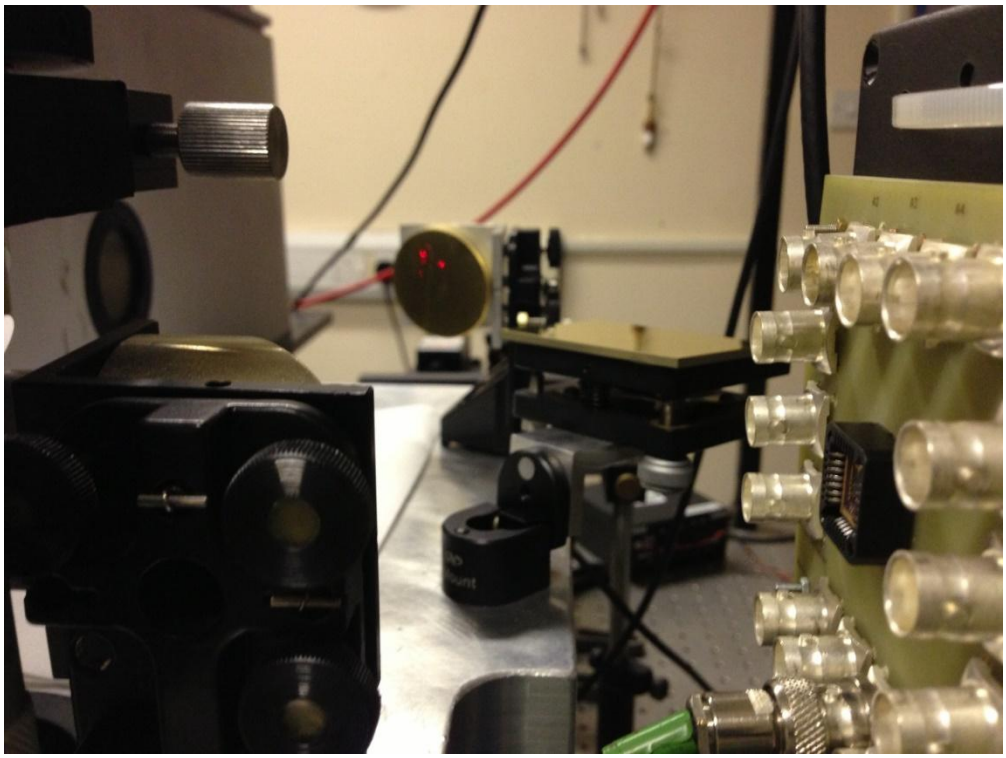

Figure 4.13. Fourier transform infrared (FTIR) electroluminescence characterization setup for pulsed and continuous-wave excitation. Parabolic mirrors collect and focus the emission from the device into a Bruker Vertex 70 FTIR system.

4.7.2 Characterization results

From the fast and step scan measurements undertaken on the n-Ge LED samples with different Si_3N_4 stressors, any shift in the output wavelength from bulk Ge under 0.25 % tensile strain (1.59 μm) indicates an increase in tensile strain. Figure 4.14 shows the electroluminescence spectrum obtained from a fast scan measurement of a 25 μm diameter Ge LED covered with 300 nm of high stress Si_3N_4 deposited with an RF power of 150 W.

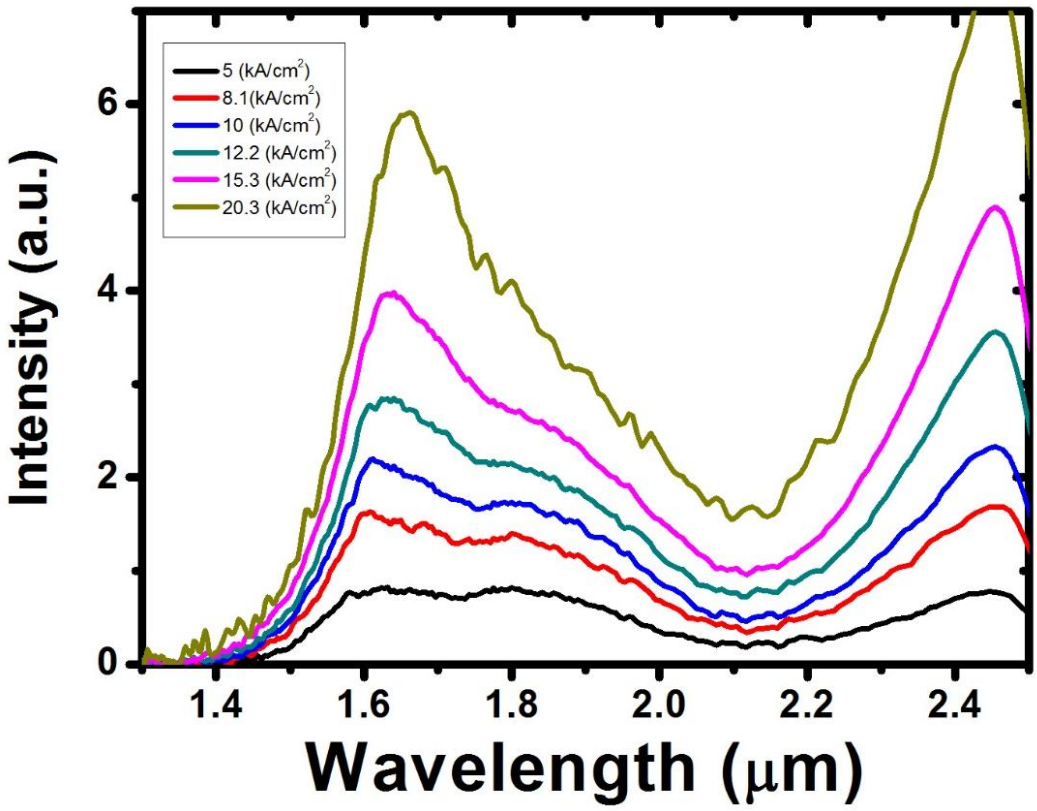

Figure 4.14. The electroluminescence of a bulk 25 μm diameter n-Ge light emitting diode covered with a Si_3N_4 stressor (RF=150W) as a function of continuous wave excitation at room temperature.

It is clear from Figure 4.14 that there are three peaks evident from the spectra. The peak observed at the detector cut-off at 2.5 μm corresponds to blackbody emission of the device from Joule heating. Continuous wave measurements demonstrate that a significant amount of the emission is from heating for current densities above 10 kA/cm^2. This is further demonstrated by measuring in step-scan configuration for a pulsed rate of 10 kHz and a duty cycle of 10 % as shown in Figure 4.15. In step scan configuration the contribution of the blackbody is significantly reduced. The broad peak at 1.8 μm corresponds to the radiative recombination from the indirect transition between the L-valley and the HH band. Finally, the peak at ~ 1.6 μm corresponds to the direct transition between the Γ -valley and the HH band. In the direct recombination case, the linewidth is narrower and more intense compared to the indirect transition.

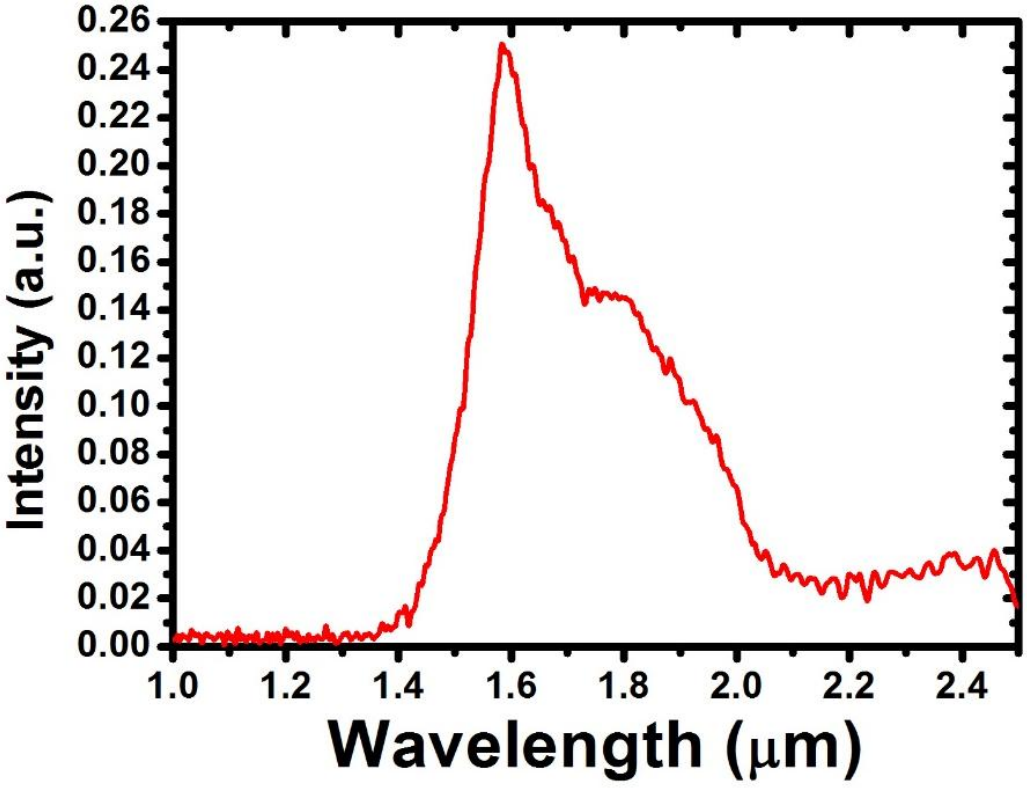

Figure 4.15. Electroluminescence of a 25 μm diameter n-Ge LED measured by step scan configuration with a 10 kHz pulsed signal and 10 % duty cycle at room temperature.

A comparison of the central peak position of the direct transition electroluminescent peak for 25 μm n-Ge LEDs covered with different depositions of Si_3N_4 is shown in Figure 4.16. It is clear that there is no substantial change between the output emission from the Si_3N_4 stressor deposited at an RF power of 50 and 150 W, which suggests that there is negligible strain induced in the Ge LED. A red shift in emission is observed at high current densities due to joule heating, which has the effect of reducing the bandgap.

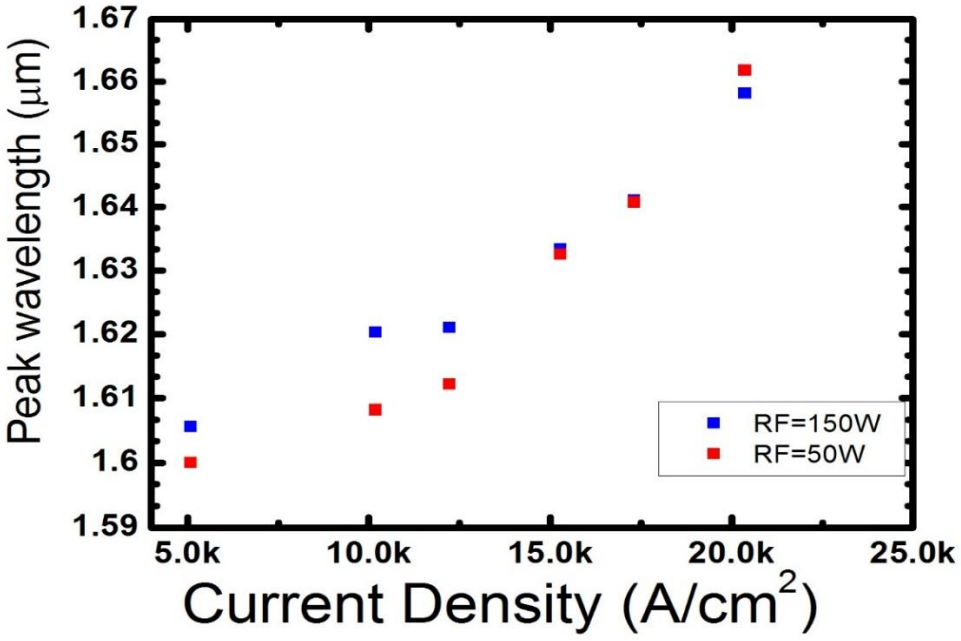

Figure 4.16. A comparison of the central position of the direct (Γ-valley to HH) electroluminescence peak as a function of current density at room temperature for 25 μm diameter n-Ge LED covered with a Si_3N_4 stressor (RF= 50 or 150W).

4.8 Ge nanostructures

As no significant shift was observed in the output emission of the LEDs at low current densities this indicates that geometrically, they are too large to induce any strain from the Si_3N_4 stressors. Therefore, smaller geometries are required (< 10 μm) to adequately strain. Thus, the focus shifted to nanostructures consisting of Ge pillars less than 1 μm.

4.8.1 Nanostructure fabrication

The pillars were patterned by electron-beam lithography using HSQ. The structures were etched using SF_6/C_4F_8 by ICP-RIE (chapter 2) down to the Si substrate. After dry etching, the HSQ mask was removed by HF. Figure 4.17 is an SEM image of 100 nm square pillars. The pillars were then covered with high stress PECVD Si_3N_4 (RF = 60 W). There was no cracking or delamination of the Si_3N_4 over the pillars observed by SEM.

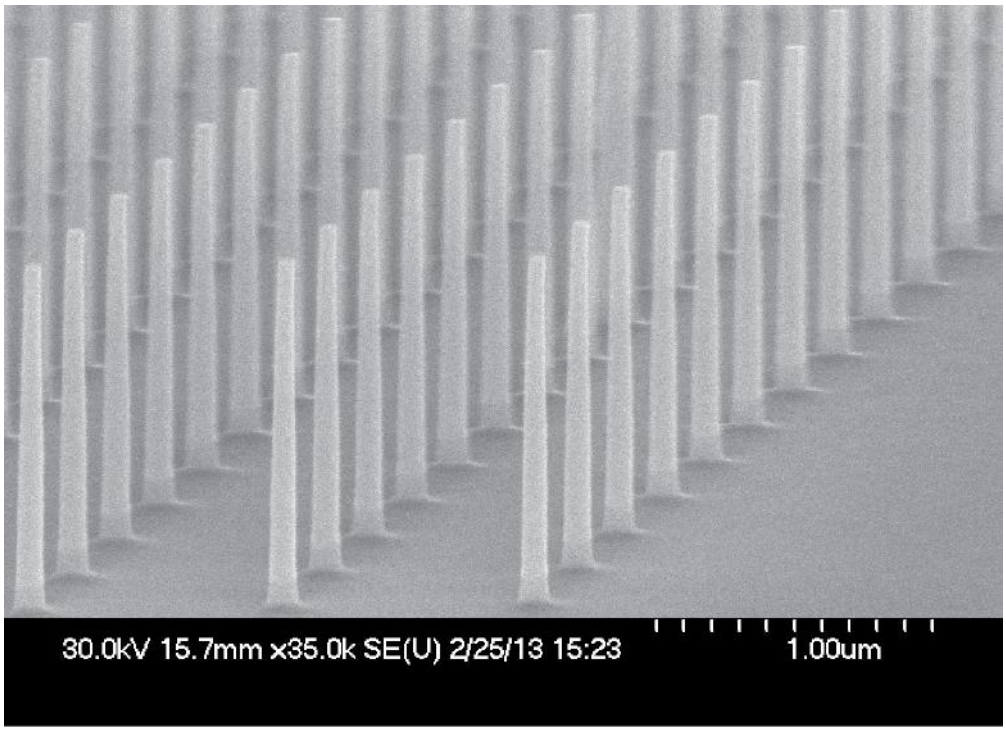

Figure 4.17. A scanning electron microscope image of 100 nm square Ge pillars etched 1 μm into the Si substrate.

4.8.2 Characterization of the nanostructures

The pillars were characterised by Dr Philippe Velha using a photoluminescence (PL) set-up with a doubled-frequency solid state Nd:YAG laser emitting at 532 nm wavelength with 300 mW of power, which was focused onto the sample by a parabolic mirror down to a spot size of 1 mm. As the spot size of the laser used for PL was 1 mm in diameter the pillars were repeated over a 1 mm^2 area. This mirror was oriented to also collect the PL from the sample and focus it onto another parabolic mirror to collimate the light into FTIR spectroscopy system for analysis. Step scan measurements were used to discriminate against ambient blackbody by modulating the laser with a mechanical chopper at 1 kHz and with a duty cycle of 50 %. A LN_2 cooled cryostat was used to measure the PL from the pillars at a range of temperatures from 15-200 K and the obtained spectrum measured with an extended Peltier cooled InGaAs detector is shown in Figure 4.18. It is clear that when the temperature is reduced the PL emission increases and this is due to a reduction in the non-radiative scattering mechanisms.

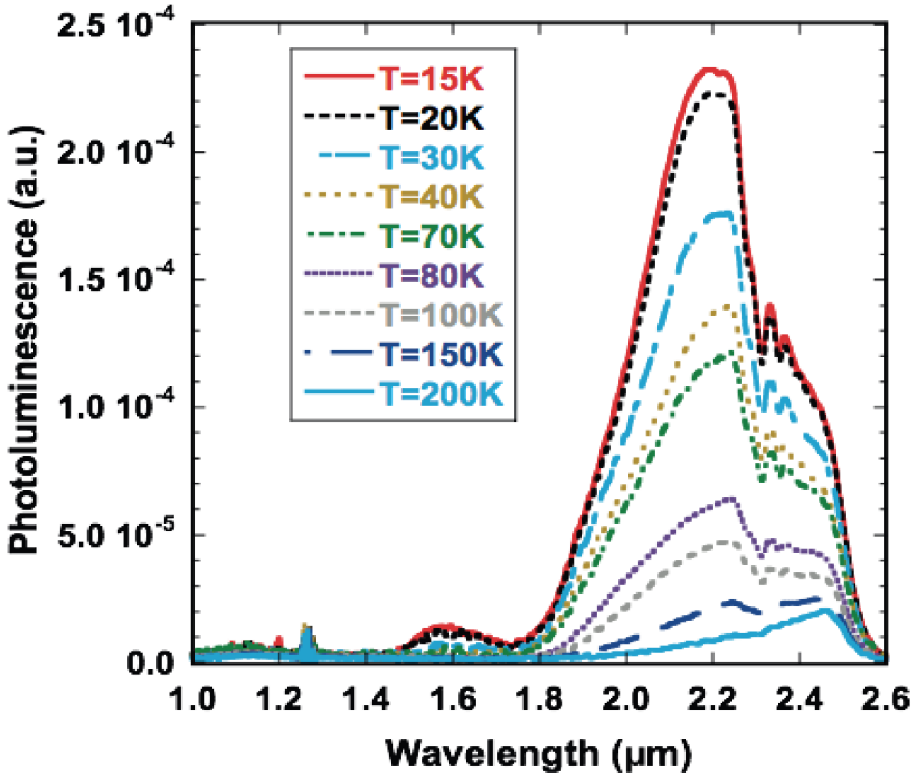

Figure 4.18. The photoluminescence spectrum obtained by Fourier transform infrared step-scan measurements for 100 nm pillars covered with 300 nm of Si_3N_4 stressors (RF = 60 W) at temperatures ranging from 15-200 K.

Figure 4.19 is a comparison of the EL measured from a 25 μm diameter n-Ge LED and the PL measured from the 100 nm square n-Ge pillars both in step-scan configuration covered with 300 nm thick high stress Si_3N_4. It is clear that the emission of the n-Ge pillars has shifted to longer wavelengths (> 2.2 μm wavelength) compared to the n-Ge LED and this indicates that the Ge pillars have been strained by the high stress Si_3N_4.

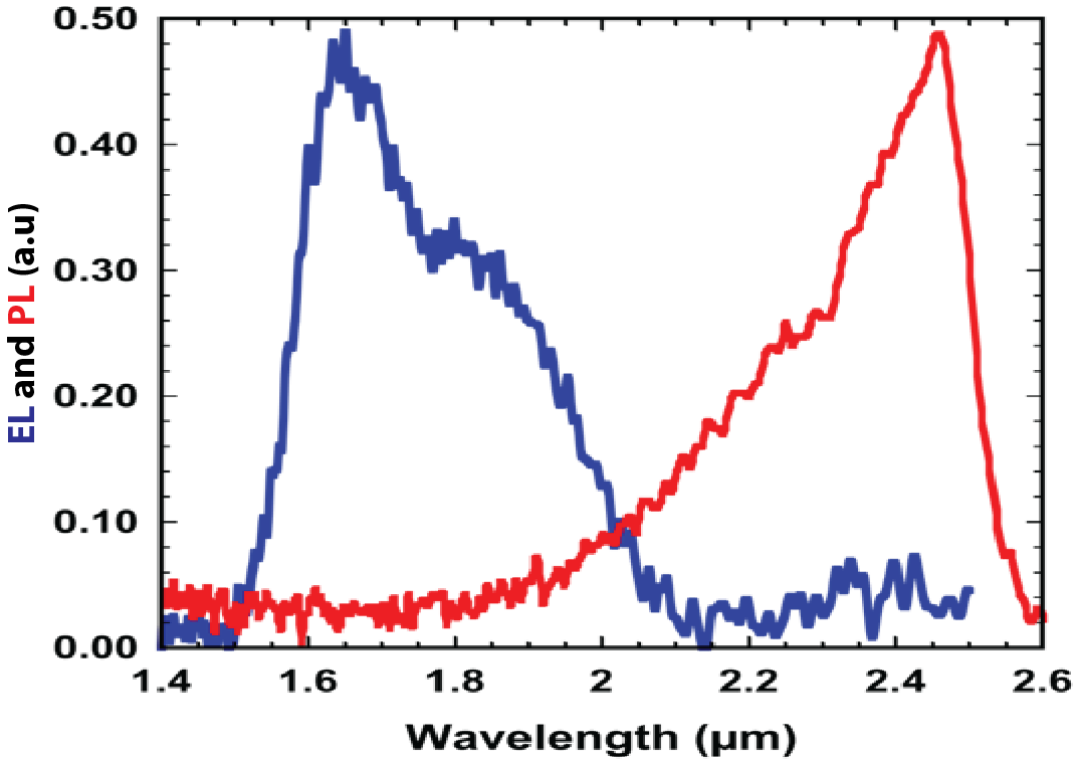

Figure 4.19. A comparison of the electroluminescence (EL) measured from the n-Ge LED (blue) and the photoluminescence (PL) of 100 nm square pillars both covered with high stress silicon nitride films.

4.9 Future work

The level of strain in the Ge pillars will have to be characterised by Raman microscopy, where a shift to the left in the longitudinal optical phonon of bulk Ge (301 cm^{-1}) indicates tensile strain that can be calculated. Increasing the level of strain within the Ge will require optimizing the geometry of the nanostructure and the stress of the Si_3N_4 deposited. Once direct bandgap Ge has been achieved, waveguide geometry such as ridge waveguide, microdisks, and ring resonators will be the most interesting in terms of producing a laser. Only low RF power Si_3N_4 has been deposited so far on the pillars to prevent delamination and cracking of the Si_3N_4 film, therefore more strain could be potentially transferred with different deposition parameters. Ideally modelling by finite element analysis software such as COMSOL should allow optimization of the level of strain transferred, which can be experimentally confirmed by micro Raman spectroscopy. In addition, the strain induced is an additive process therefore can increase the strain by other process

induced techniques such as the lattice mismatch between Ni_5Ge_3 and Ge that results in tensile strain [134]. This could be implemented by annealing Ni deposited on Ge at 300 °C. Another approach is to deposit Ti on the backside of the Si substrate and anneal to form TiSi that adds a small amount of tensile strain (0.05 %) into the Ge [126].

4.10 Summary

It has been shown that although Ge is an indirect bandgap semiconductor the difference between the direct and indirect is very small (~36 meV). Methods to make Ge a better light emitting material for lasing have consisted of degenerate n-type doping and tensile strain. It has been shown that tensile strain is probably the best approach to producing large optical gain to lower threshold for lasing. In this work a process to induce tensile strain in Ge by depositing Si_3N_4 stressors has been developed. From electroluminescence characterization of fabricated n-Ge LEDs ranging from 25 to 500 μm in diameter covered with various Si_3N_4 stressors, there was no significant shift observed in the optical emission. Only peaks that can be attributed to 0.25 % tensile strained Ge due to the thermal mismatch between Si and Ge during growth were observed, corresponding to the indirect transition between the L-valley and the HH band at 1.8 μm and the direct transition between the Γ-valley and the HH band at 1.6 μm. This indicates the process is only valid for sub-micron devices. Therefore, 100 nm square pillars were fabricated by electron beam lithography and strained by Si_3N_4 stressors. Photoluminescence of the pillars demonstrates clear modification of the optical properties of the strained material with emission at wavelengths longer than 2.2 μm observed. At present only Si_3N_4 films deposited at relatively low PECVD RF powers have been investigated suggesting that optimisation of the process could potentially enable LEDs, lasers and photodetectors to operate well above 2 μm wavelength and potentially at strain levels where Ge becomes a direct bandgap material.

5 Ge quantum wells on Si

Another possible avenue for the realization of an efficient electrically pumped laser on Si is through Ge quantum wells. Quantum wells are routinely used to enhance the light emitting performance of III-V photonic lasers [135-137]. This is due to the beneficial density of states that arises from the reduced dimensionality that results in a reduction of the current density required to obtain population inversion. Another advantage of moving to a quantum well design is that Auger recombination is reduced. This is important as it is expected to be a dominate non-radiative recombination process for Ge due to the relatively small bandgap [138]. In addition, moving to a Ge/SiGe quantum well structure forms a type-1 band alignment (see Figure 5.1(a)) for a Ge quantum well sandwiched between Ge rich $Si_{1-x}Ge_x$ barriers ($x \geq 0.8$) grown on a relaxed substrate of SiGe [139]. Comparatively bulk Ge-on-Si produces a type-2 band alignment (see Figure 5.1 (b)) where only holes are confined. Therefore, quantum wells should provide better confinement of carriers in the active region and greater recombination efficiency.

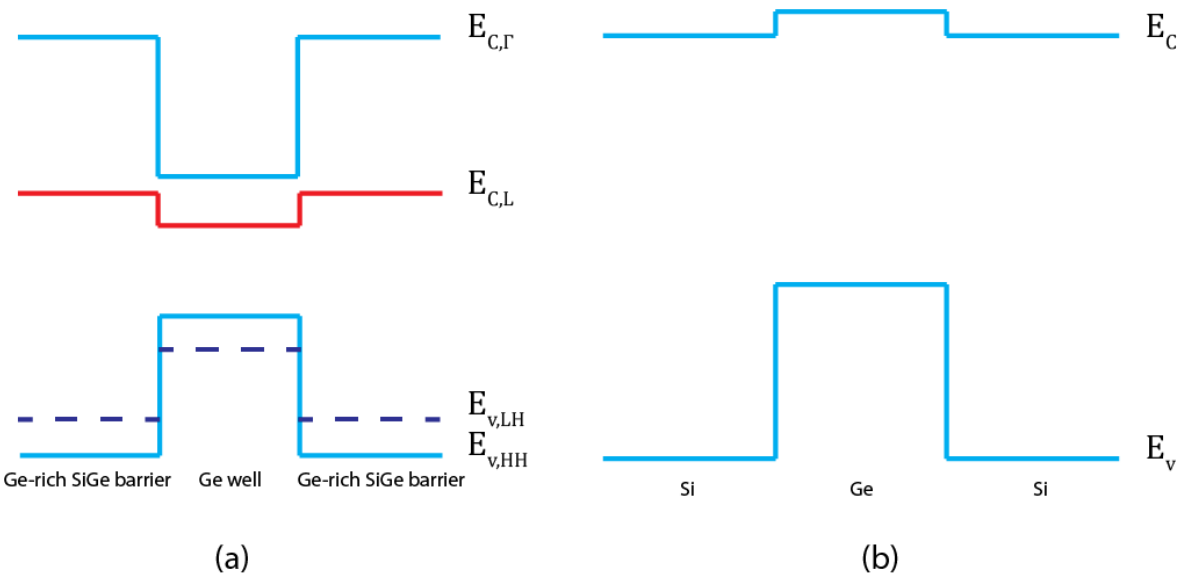

Figure 5.1. (a) A schematic diagram (not to scale) of the band alignment for (a) a compressively strained Ge quantum well sandwiched between tensile strained SiGe barriers on a relaxed SiGe buffer and (b) a Si/Ge/Si double heterostructure.

However, one disadvantage of moving to a quantum well structure is the thin active layer that provides poor optical confinement compared to bulk films. This can be overcome by moving to a multi quantum well (MQW) design that offers a practical solution to the mode-overlap problem by increasing the effective thickness of the active region [140]. Ge/SiGe MQW structures have demonstrated strong light modulation based on the quantum-confined Stark effect from a p-i-n diode design [141-143]. From this successful design, an NIR surface illuminated photodetector has also been realised using the strong absorption of the direct transition in Ge QWs [144-146]. However, to date there has not been allot of research into the light emission of Ge quantum wells. The majority of the previous publications regarding light emission from Ge quantum wells have only demonstrated photoluminescence through optical pumping [147-150]. There has only been one single result of electroluminescence, which demonstrated emission at 1.45 μm wavelength [151]. Therefore, it is worthwhile to investigate the light emitting properties of n-Ge/SiGe MQWs as an alternative route to an efficient electrically pumped laser on Si.

This chapter will introduce how quantum wells are formed and carrier transport through barriers by quantum mechanical tunnelling. It will be shown that when a barrier is extremely thin, multiple quantum wells can couple to form a miniband. The n-Ge/SiGe MQW band structure and corresponding subband states will be presented before photoluminescence and electroluminescence characterisation of fabricated MQW LEDs will be given. Optical characterization will show there is two peaks evident around 1.55 and 1.8 μm wavelength, which correspond to recombination between the direct and indirect transitions, respectively. The emission wavelength of the device can be tuned by roughly 4 % by changing the current density through the device. The devices have potential applications in the fields of optical interconnects, gas sensing, and healthcare.

5.1 Quantum Well

A quantum well is formed when a thin layer of a semiconductor material with a narrow bandgap is sandwiched between two layers of a wider bandgap. This

creates a heterostructure and if the layer of the narrow bandgap is thin enough (≤ 10 nm) then it is susceptible to quantization effects, which produce distinct subband states. This is illustrated in the textbook example of an infinitely deep square well that is presented in Figure 5.2. This is a purely idealised example where the barriers have potential infinite in height and are infinite in length. Outside the quantum well, the wave function must be zero and inside the quantum well, the time independent Schrödinger equation is equal to equation(5.1), where ψ is the wavefunction, m is effective mass, E is total energy, k is the wavenumber, $\hbar$ is the reduced planks constant and z is the position of the particle in the quantum well.

$$\frac{\partial^2\psi(z)}{\partial z^2} + k^2\psi(z) = 0 \tag{5.1}$$

$$k^2 = \frac{2mE}{\hbar^2} \tag{5.2}$$

A solution to this equation must form bound states and a non-degenerate energy spectrum therefore, equation (5.3) can be chosen as an appropriate solution, where L is the length of the quantum well.

$$\psi(z) = A\sin(kL) + B\cos(kL) \tag{5.3}$$

By using continuous boundary conditions, the wave function vanishes at the walls of the well and $k_n L = n\pi$. Thus, the energy of each state can be found from equation (5.4), where n is the quantum number and labels the states. The normalised wave function describing each state is found from equation (5.5). It is clear from Figure 5.2 that by confining a particle to a region of space it produces discrete energy levels, which are known as the subbands [152].

$$E_n = \frac{\hbar^2\pi^2 n^2}{2mL^2} \tag{5.4}$$

$$\psi(z)_n = \sqrt{\frac{2}{L}} \sin\left(\frac{n\pi}{L} z\right) \tag{5.5}$$

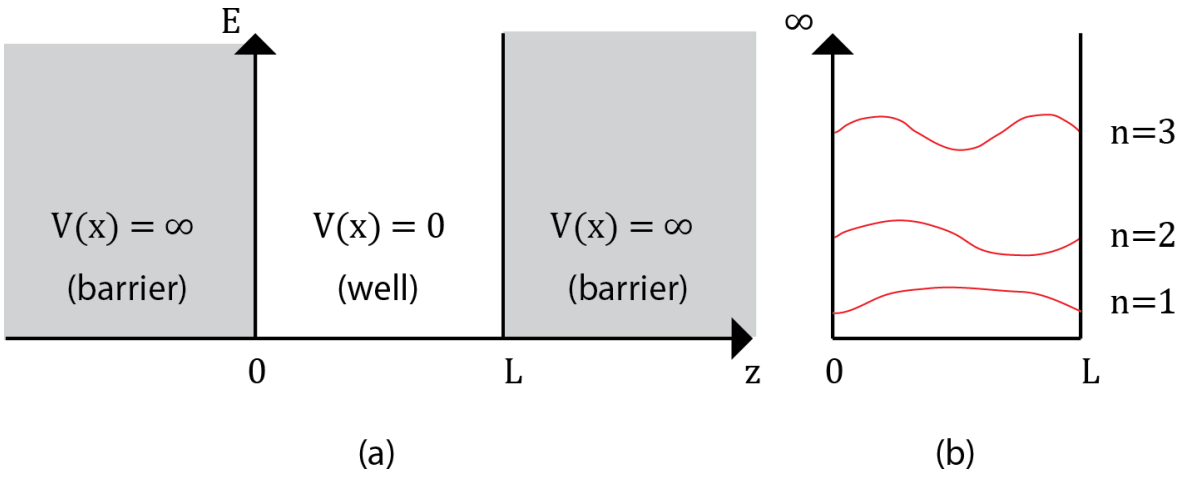

Figure 5.2. An illustration of an (a) infinitely deep square well and (b) its corresponding subband states.

5.2 Quantum mechanical tunnelling

5.2.1 Single barrier

Classically a particle encountering a barrier that has a potential energy greater than the energy of the particle, the particle would be reflected back of the barrier. Quantum mechanically however there is a finite probability that the particle will pass straight through the barrier as depicted in Figure 5.3. This is a purely quantum mechanical effect, which is due to the wave nature of particles and is known as quantum mechanical tunnelling [152].

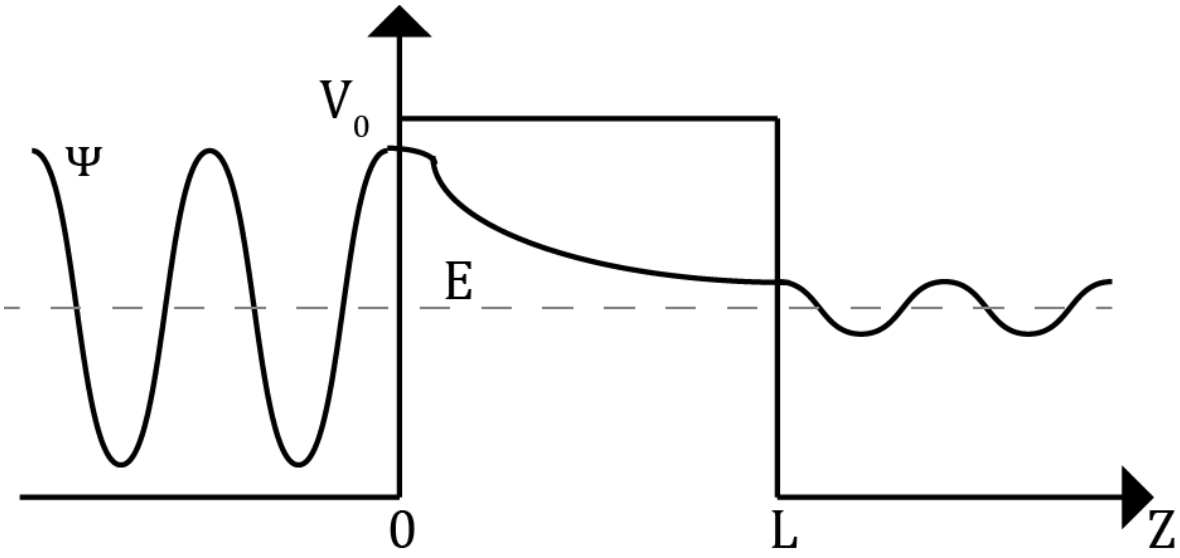

Figure 5.3. An illustration of quantum mechanical tunnelling through a single barrier of potential greater than the particle energy.

For the single barrier case as pictured in Figure 5.3, the probability of transmission can be shown after derivation as

$$T = \left[1 + \frac{1}{4} \frac{V_0}{E(V_0 - E)} \sinh^2(k_2 L) \right]^{-1} \tag{5.6}$$

$$k_2 = \sqrt{\frac{2m^*(V_0 - E)}{\hbar^2}} \tag{5.7}$$

If $E \ll V_0$ then equation (5.6) can be simplified as

$$T \approx \frac{16E}{V_0} e^{-(2k_2 L)} \tag{5.8}$$

Therefore, in order to obtain a high probability of tunnelling through a thin barrier, a small potential barrier height, and light effective mass are required.

5.3 Coupling between quantum wells

When thin barriers separate multiple quantum wells, there is a finite probability that a carrier can be found in any of the quantum wells and there is an overlap of the wave functions. As the number of coupled quantum wells increases (≥10), the overlapped wave functions form a miniband and this is the basis for the n-Ge/SiGe MQW structure investigated in this work.

5.4 Ge/SiGe multi quantum wells

The design for the n-Ge/SiGe MQWs investigated in this work is presented in

Figure 5.4. The design consists of 10 periods of tensile strained n-Ge quantum wells. Collaborators in Como grew the n-Ge multi quantum well structure by LEPECVD. The heterostructures were grown upon a p-Si (100) substrate with a resistivity of 1 Ω-cm. Before growth, the substrate was first degassed at 316 ℃ for 10 min before loading into a low-energy plasma-enhanced chemical vapour deposition (LEPECVD).

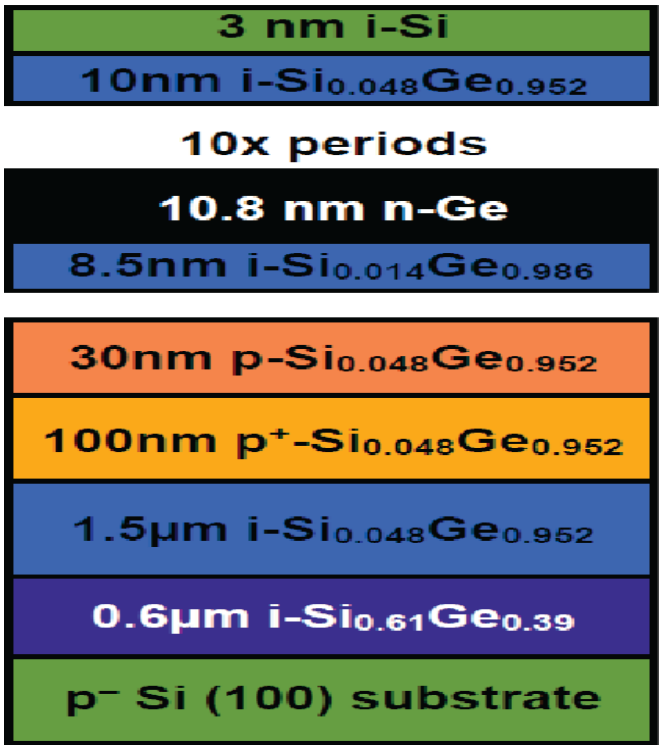

Figure 5.4. The heterolayer design for the Ge/SiGe multi quantum well.

A 2.1 μm thick buffer with the first 600 nm relaxed layer of $Si_{0.61}Ge_{0.39}$ was grown followed by 1.5 μm relaxed $Si_{0.048}Ge_{0.952}$. Since there is a large lattice mismatch between Ge and Si a relaxed buffer is required to form a fully relaxed virtual substrate on which Ge/SiGe heterostructures can be grown without threading dislocations forming. Next 100 nm of p-$Si_{0.048}Ge_{0.952}$ ($N_A = 3\times10^{18}$ cm^{-3} doped from B_2H_6) was grown as required for an Ohmic bottom contact. A 30 nm spacer of $Si_{0.0.48}Ge_{0.952}$ ($N_A = 5\times10^{17}$ cm^{-3}) was grown before the active quantum well region. The active region consists of 10 periods of strained 11.2 nm n-Ge quantum wells ($N_D = 1\times10^{19}$ cm^{-3} doped with PH_3) and 8.5 nm $Si_{0.014}Ge_{0.986}$ barriers. A final cap of 10 nm of $Si_{0.048}Ge_{0.952}$ followed by 3 nm of Si was grown to produce a Schottky top contact that would allow hot electron injection into the Γ-valley with the aim of producing more efficient direct recombination. Whilst the PH_3 was only switched on during the growth of the quantum wells, due to segregation effects, all the heterolayers grown after the first quantum well will be doped with significant fractions of the n-type doping level [153].

5.5 X-ray diffraction analysis of Ge MQW

The Ge concentrations (and quantum well thicknesses) for all heterolayers were measured after growth using x-ray diffraction (XRD) by colleagues in Como and this is shown in Figure 5.5 (a). A series of satellite peaks can be seen, which indicates high crystal quality and abrupt interface between the Ge quantum wells and SiGe barriers. The present thin buffer resulted in a tensile strain of 0.13 % as measured by XRD (Figure 5.5 (a)) after the sample was cooled to room temperature and the modelling of the bands and subband states has taken account of this strain [128].

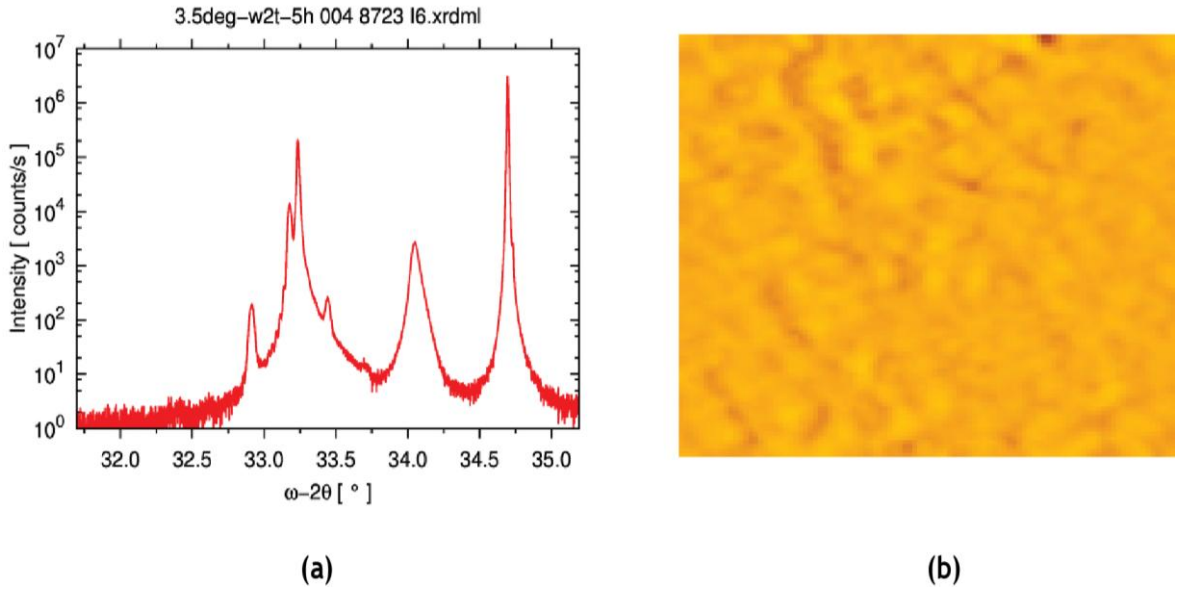

Figure 5.5. (a) X-ray diffraction $\omega - 2\theta$ through the (004) reflection of the Ge/SiGe MQWs. (b) Surface image of a blank Ge MQW sample measured with atomic force microscopy.

For this strain relaxed buffer Ge concentration, the calculated Matthews and Blakeslee critical thickness is 283 nm [154]. The surface morphology of the samples was analysed after growth by atomic force microscopy, (see Figure 5.5 (b)) where the root mean square roughness was approximately 1.5 nm over a 35 μm^2 area.

5.6 Band modelling of Ge/SiGe MQW

The band structure was calculated using a self-consistent Poisson-Schrödinger solver with the deformation potentials from Reference [128] and the results for a single quantum well are shown in Figure 5.6. An 8-band k.p model was used for the hole bands and the Γ-valley whilst a 1 band tool was used to find the L- and Δ-valley bands and subband states.

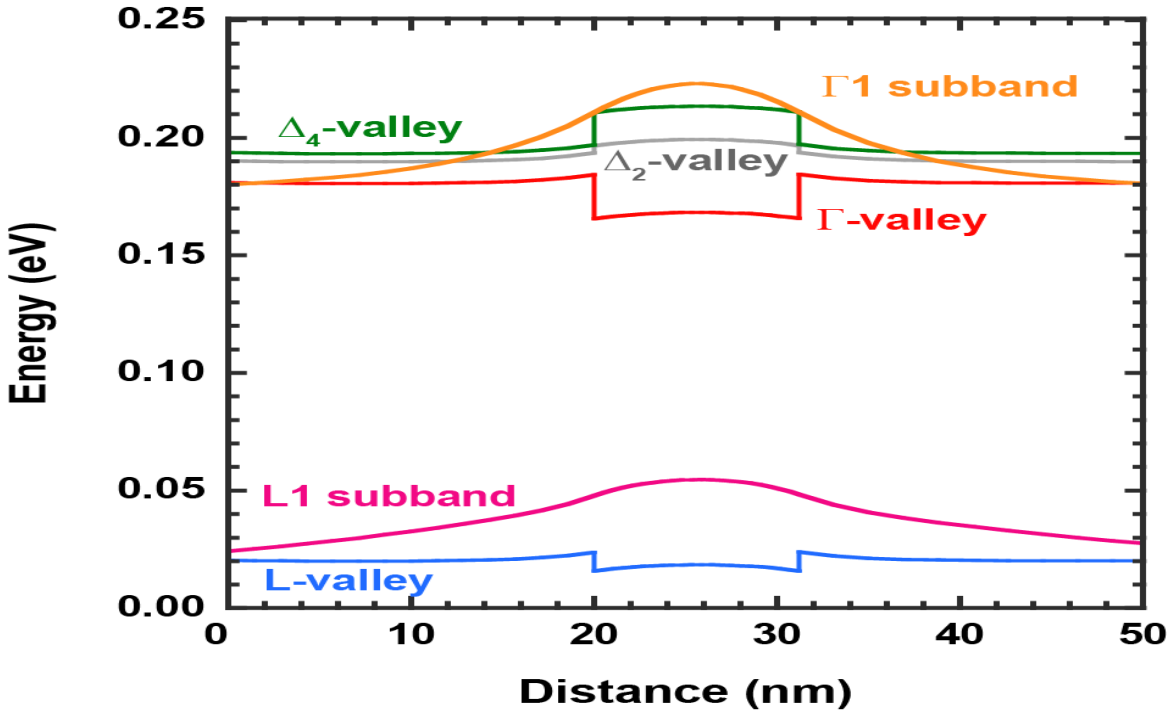

Figure 5.6. The conduction bands for a single quantum well in the device as calculated by self-consistent Poisson-Schrödinger solver at 300 K. The confined subband states for the L- and Γ-valleys are also plotted.

For both the L- and Γ-valleys, only a single subband for each valley is confined in the quantum well. The L-valley subband state is very weakly confined in the quantum well due to the small conduction band discontinuity of only 8 meV. At room temperature, confinement due to the L-valley quantum well is unlikely to be observed. The Γ-valley is below both Δ-valley bands due to the tensile strain in the substrate. The Γ-valley quantum well has a discontinuity of 19 meV with a single confined state that due to the low effective mass of 0.038 m_0 (where m_0 is the free electron mass), the subband states in each quantum well overlap to form a miniband with width calculated to be 8.4 meV. Modelling of the valence band demonstrated that the ground state is the heavy-hole (HH) and the lowest subband is the HH1. The tensile strain is therefore not great enough to move the light-hole (LH) band above the HH band. The calculated lowest direct transition is $\Gamma 1$ to HH1 at 0.817 eV (1.52 μm wavelength) and the indirect $L1$ subband to HH1 is 0.663 eV (1.89 μm wavelength).

5.7 Fabrication of the n-Ge MQW LED

Fabrication followed the same process used to fabricate the bulk Ge LEDs (see Figure 4.11). Cylindrical mesas ranging from 25 to 500 μm in diameter (Figure 5.7) were defined by photolithography and then etched down anisotropically using a fluorine based chemistry in an inductively coupled plasma reactive ion etch tool as previously discussed. In order to accurately stop within the doped p-SiGe bottom contact region an interferometer was used whilst etching. 50 nm of Ni was deposited by electron-beam evaporation for the bottom contact and this was patterned by lift-off and subsequently annealed at 340 ℃ for 30 s in a rapid thermal annealer (RTA) [94]. As previously described in chapter 3, Ni on Ge forms the lowest electrical resistivity phases out of all the transition metals, therefore is an appropriate metal contact to p-Ge. The process provides bottom Ohmic contacts with $\rho_c \approx 4\times10^{-8}$ Ω-cm^2 measured from CTLM test structures. A simulation of the Ge/SiGe MQW structure and a measured interferometer signal from a dry etch test compare well as shown in Figure 5.8.

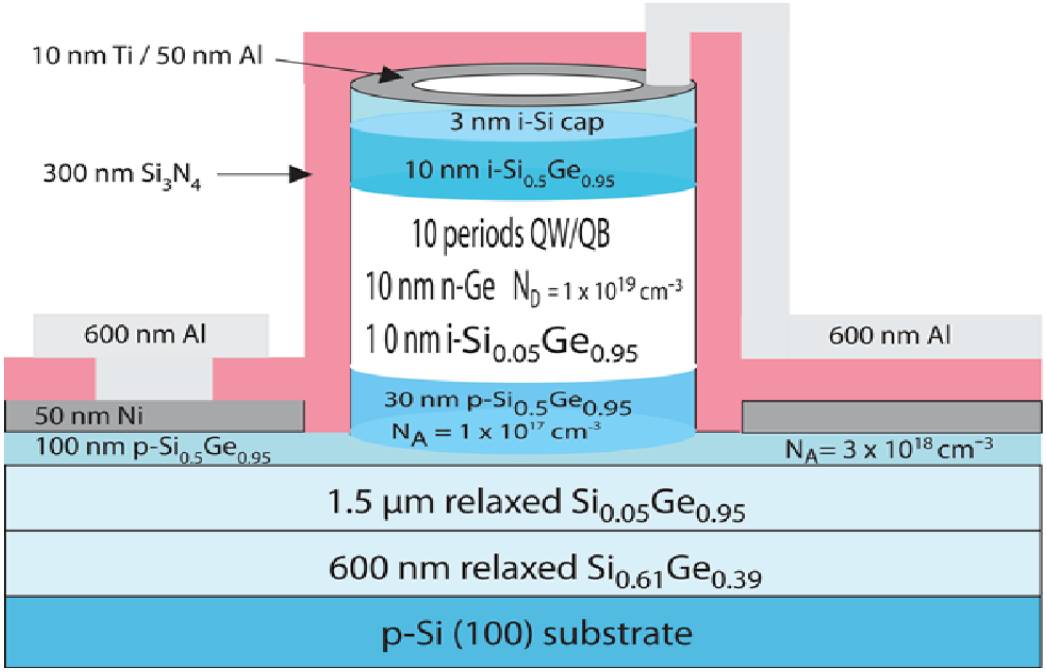

Figure 5.7. (a) Cross sectional schematic of cylindrical LED showing layer thicknesses and doping concentration. Top contact is purposely Schottky to allow injection of hot electrons into the Γ-valley for more efficient direct recombination.

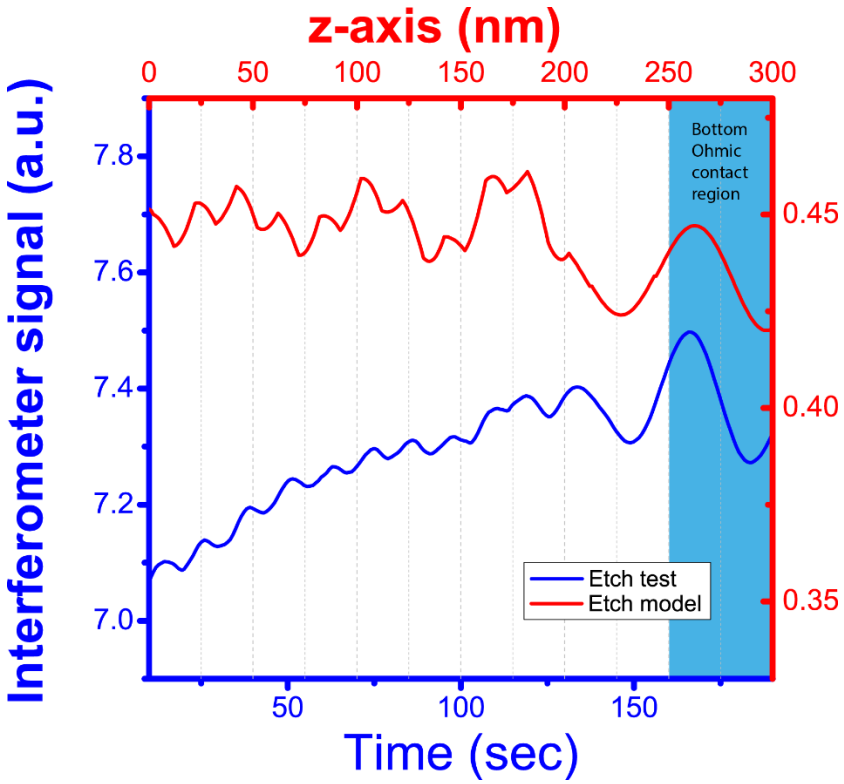

Figure 5.8. A comparison of the interferometry signal measured during a test etch versus the etch model for the Ge quantum wells.

An unannealed top contact of 10 nm of Ti followed by 50 nm of Al was deposited to produce a Schottky top contact, which may inject hot carriers above the conduction band edge. The entire structure was then passivated with Si_3N_4 and via holes were etched to allow interconnects to the contacts. Bond pads of 600 nm of Al were deposited and finally, the device was wire bonded to a chip carrier in order to connect the LED to an external power supply for characterisation. The current-voltage characteristics for a 300 μm MQW n-Ge/SiGe LED are shown in Figure 5.9. Larger currents flow when the device is forward biased with electrons being injected into the conduction band from the Schottky top contact. The dark current is comparable to some of the best reported from Ge on Si photodetectors [155].

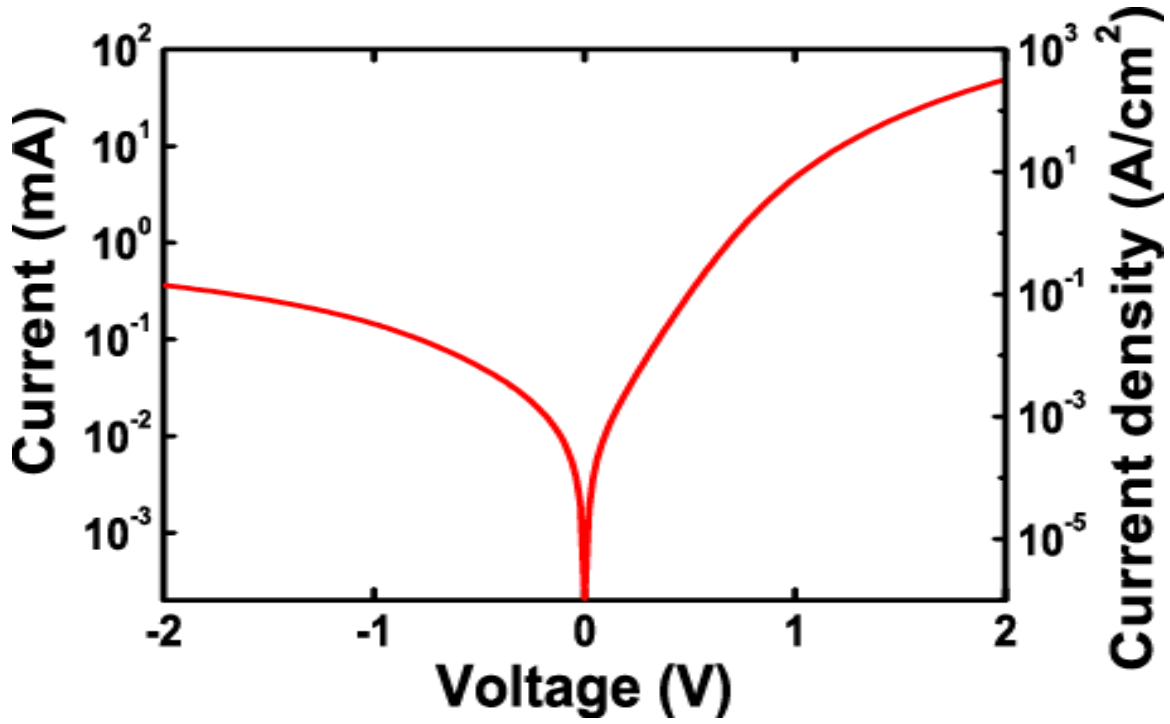

Figure 5.9. The current-voltage characteristics for a 300 μm MQW n-Ge/SiGe LED at room temperature.

5.8 MQW n-Ge/SiGe LED characterization

The setup to characterise the bulk n-Ge LEDs was also used to characterise the MQW n-Ge/SiGe LEDs. Both the PL and EL were measured. All measurements were undertaken in surface normal geometry, which corresponds to xy-polarization (TE polarization). The selection rules for such polarization allow the following transitions: $\Gamma 1$ to HH1, $L1$ to HH1, $\Gamma 1$ to LH1, and $L1$ to LH1 [128].

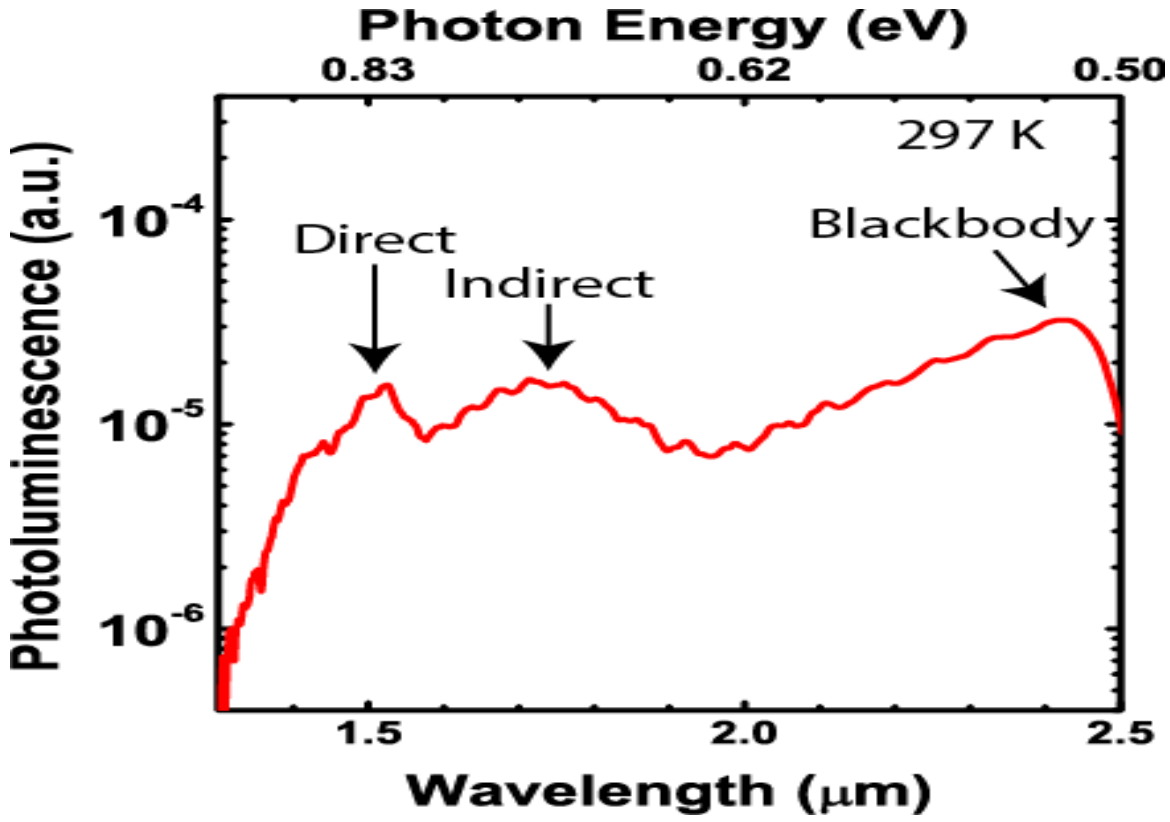

Figure 5.10. The photoluminescence of the MQW n-Ge/SiGe material at room temperature using a 580 nm pump source.

Figure 5.10 shows the PL for 580 nm CW excitation. Comparison with the band structure modelling of Figure 5.6 indicates that the sharper peak just above 1.5 μm is the Γ-valley to HH1 transition and the broader 1.8 μm peak is the L-valley to HH1 indirect transition. Above 2 μm is blackbody emission under CW illumination. Figure 5.11 shows the electroluminescence as a function of current density under CW conditions at room temperature.

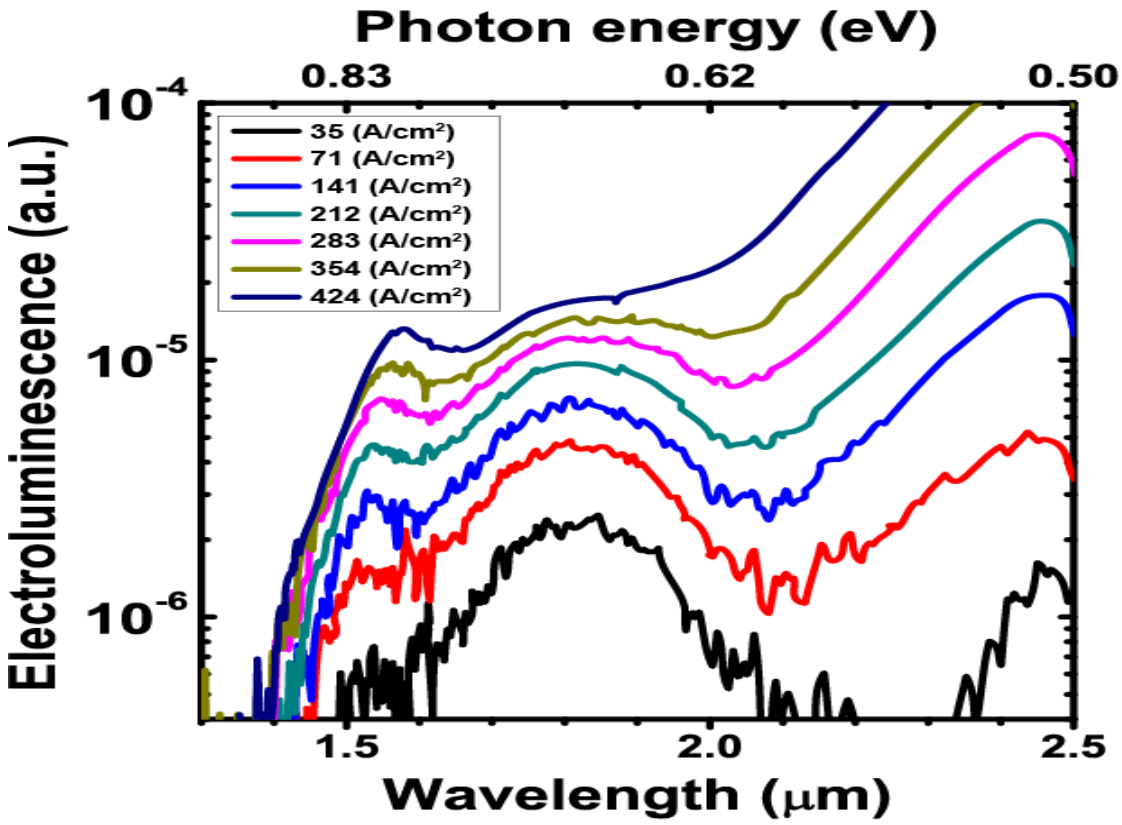

Figure 5.11. The electroluminescence for a 300 μm MQW n-Ge/SiGe LED at room temperature as a function of continuous wave excitation currents.

As the current is increased, the direct bandgap (Γ-valley to HH1) electroluminescence increases compared to the indirect (L- valley to HH1) transitions. In addition, the blackbody contribution demonstrates significant increases as the current is increased, which is clearly visible beyond 2 μm wavelength. Figure 5.12 demonstrates the total electroluminescence-current (LI) data from the LEDs. Below 210 A/cm^2, the gradient of the LI curve is below 1 whilst above this point, the gradient increases to 1.5 and it is clear that blackbody emission from Joule heating of the sample starts to become more significant in the measured electroluminescence power.

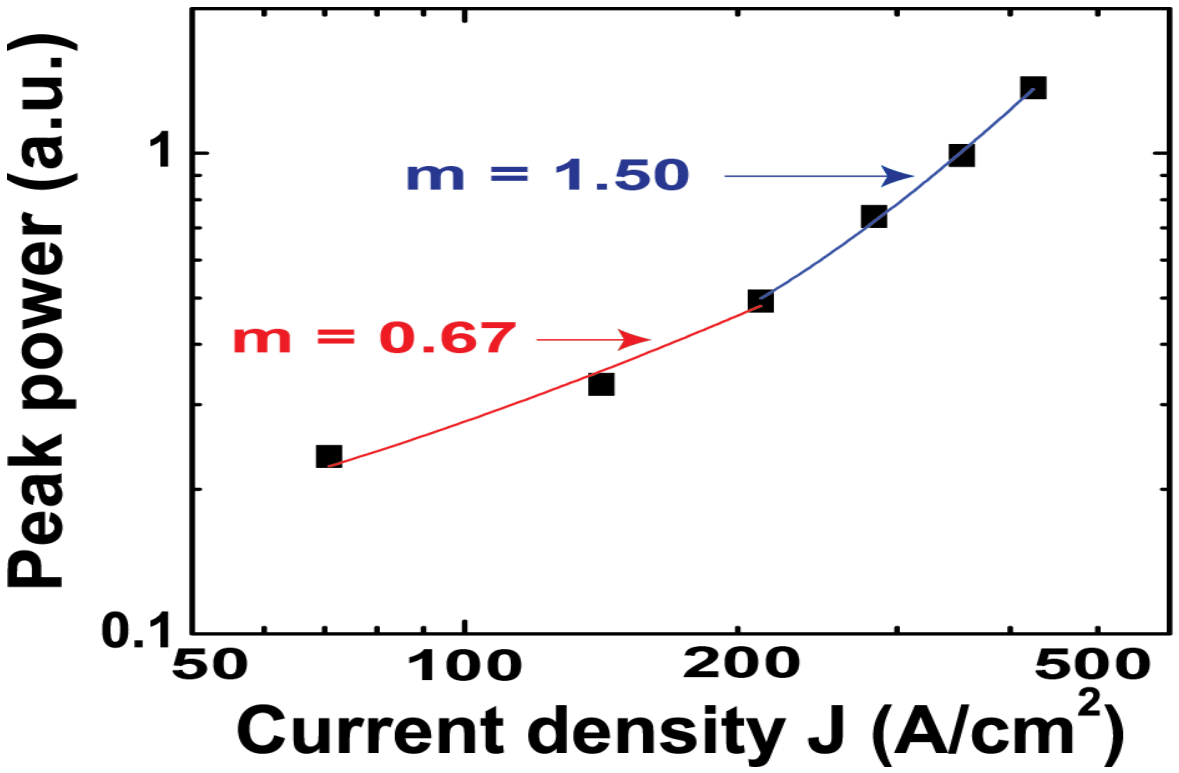

Figure 5.12. The electroluminescence versus current density plot of the device at room temperature.

Previous publications have indicated that heating can help excite carriers from the L-valley to the Γ - valley and increase the electroluminescence efficiency and output power [151, 156, 157]. A similar effect is observed in the present devices as the ratio of the emission from the direct bandgap compared to the indirect bandgap emission increases with increasing current density but the use of the longer wavelength detector in this work also demonstrates the resulting strong spectral contribution of the blackbody emission at longer wavelengths.

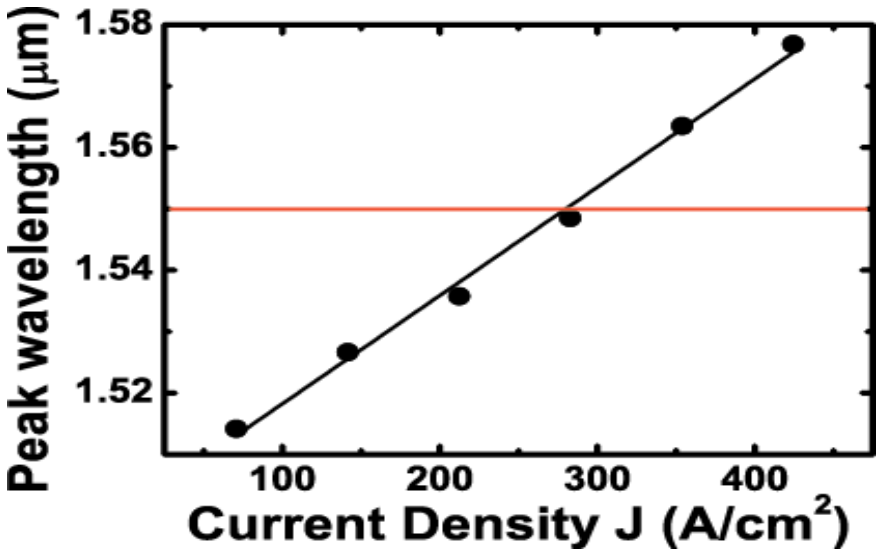

Figure 5.13. The central position of the direct bandgap (Γ-valley to HH1) electroluminescent peak as a function of current density at room temperature. The line is a linear fit to the data.

Figure 5.13 shows the shift in the direct bandgap recombination peak as a function of current density. As the current density is increased to 420 A/cm^2, the emission wavelength is increased by around 4 % as shown in Figure 5.13. The clear redshift of the direct bandgap recombination peak as a function of increasing current density demonstrates the Joule heating of the device with the resultant reduction in the direct bandgap (the indirect bandgap is also reduced by the heating). The bandgap dependence of Ge was modelled by Varshni [158] and the expected variation is inverse linearly proportional to the temperature when the semiconductor is well above the Debye temperature of 374 K for Ge. Assuming that confinement and strain effects of the MQW n-Ge/SiGe structure does not depend on temperature, a temperature increase of approximately for the highest injection current was estimated. To explain the Varshni coefficient relate the dependence of semiconductor band gaps on temperature by

$$E_g(T) = E_0 - \alpha T^2 / (T + \beta) \tag{5.9}$$

Where α and β are fitting parameters, which are characteristics of a given material. For Ge α = 5.82×10^{-4} and β = 296 [158]. Curve fits to the blackbody part of the spectra in Figure 5.11 indicate that the electron temperature is above

400 K for current densities of 300 A/cm^2 and above thereby indicating that the bandgap is decreasing with a linear variation of temperature. From the shift in the EL peak with current density and by using the Varshni coefficient for the direct gap of Ge and assuming that confinement and strain effects of QW structures do not depend on temperature, an approximate temperature increase for the highest injection current was estimated. As Joule heating in semiconductors results in a near linear temperature rise with current density, the linear variation of wavelength with current density in Figure 5.13 therefore agrees with the Varshni model for the bandgap for temperatures above the Debye temperature [158]. At 300 A/cm^2, the direct recombination electroluminescence is at the important 1.55 μm wavelength for telecoms applications.

5.9 Summary

Ge quantum wells for an efficient light emitter on Si have been investigated. The present n-Ge quantum well devices have a narrow direct recombination peak (≈ 80 nm full width half maximum) followed by the drop in electroluminescence to near zero levels at higher energies. This can be explained by the sharp two 2D density of states, which results in only the Γ -valley to HH1 and L -valley to HH1 recombination transitions being observed under electroluminescence, unlike the bulk Ge devices. Such 2D radiative transitions are ultimately expected to produce higher gain and lower thresholds if a laser can be produced [159]. The quantum well structures also provide a natural design for confining (and guiding) the mode and therefore the expectation is that this approach is interesting to produce practical Ge electroluminescent LEDs and lasers on silicon substrates. Fourier transform infrared spectroscopy characterisation revealed two peaks at 1.55 and 1.8 μm wavelength that corresponds to the Gamma to HH and L to HH. The devices show better performance at higher temperature and this is from more carriers been thermally excited into the Gamma for efficient direct recombination.

6 Ge-on-Si single-photon detectors

6.1 Introduction

Previous chapters investigated the possibility of integrating Ge-on-Si to produce an efficient light emitter. This chapter will investigate Ge-on-Si single photon avalanche detectors (SPAD). A number of emerging applications such as quantum key distribution [160], time of flight ranging[161], and remote gas sensing [162] all drive the requirement for efficient, low-noise, and high sensitivity infrared single-photon detectors. Whilst Si single-photon avalanche diodes (SPADs) perform effectively at wavelengths below 1 μm, efficient detection at wavelengths greater than this remains problematic. Particular demand is placed on single-photon detectors efficient at the low-loss optical fibre wavelength regions (1.3 and 1.55 μm), which operate close to room temperature.

Commercially available InGaAs/InP SPADs suffer from various drawbacks that limit their sensitivity and practicality: gated operation, long dead time, high dark count rates (DCRs), afterpulsing, and low operating temperatures. InGaAs/InP APDs operated above breakdown for single-photon detection were first reported in 1996 [163]. Subsequently, custom-designed InGaAs/InP SPADs have been fabricated and characterised [164]. More recently, novel designs that incorporate negative feedback to quench the avalanche current passively have been realised [165]. The effects of afterpulsing, where dark events are induced by the slow release of carriers trapped during previous avalanche events, remain a significant operational issue. The afterpulsing probability can be reduced by limiting the charge passing through the device via electrical gating, such that the detector is only active for a short window around the expected photon arrival time [166, 167]. For applications such as laser ranging and time-resolved photoluminescence, however, a long temporal detection window may be required for more comprehensive measurements. For this reason, free-running InGaAs/InP SPADs have been investigated, although the overall detection efficiency is reduced by this approach [165, 168]. An alternative to InGaAs is Ge that has comparative

absorption coefficients at wavelengths up to ~1.55 μm at 300 K [169], which can be seen in Figure 6.1.

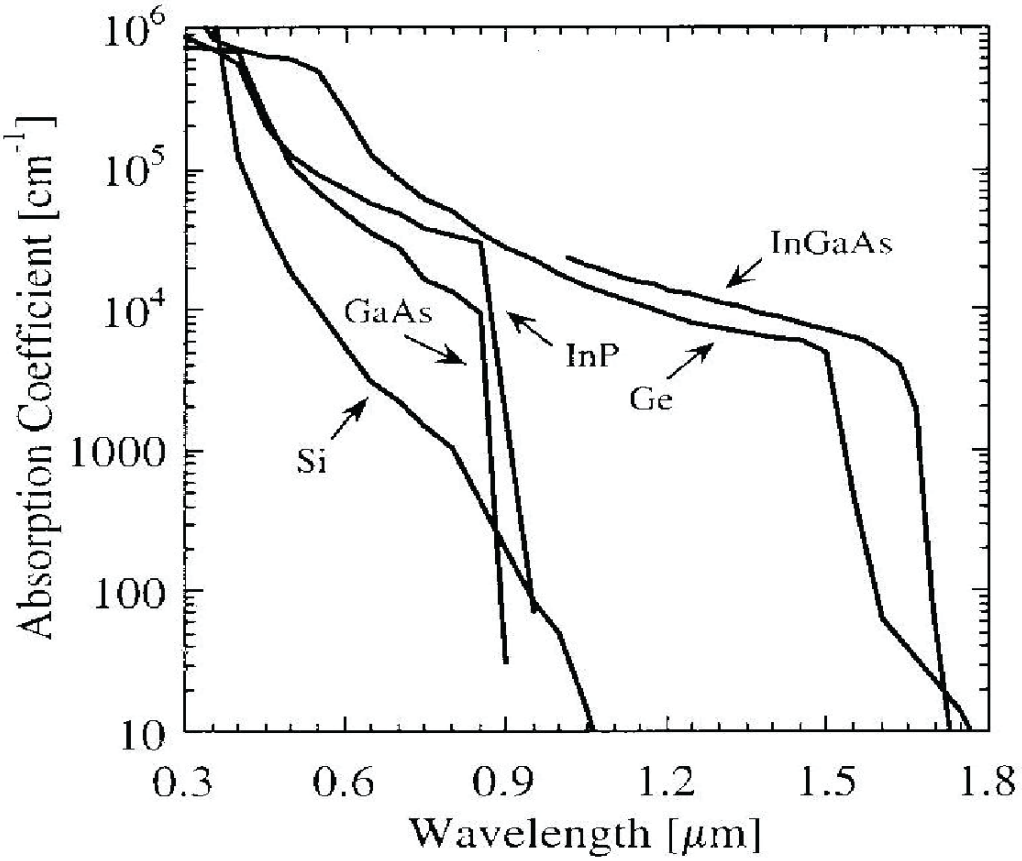

Figure 6.1. A comparison of absorption coefficient for several semiconductors including Ge at 300 K [170].

This chapter will provide a brief literature review of the most recent homojunction Ge and Ge-on-Si SPADs in order to benchmark the devices fabricated during the course of this work. The design of the Ge-on-Si SPADs, which are based on a separate absorption, charge sheet, and multiplication (SACM) region will be presented. This will be followed by the fabrication of the SPADs along with single photon characterization that was performed by collaborators in Herriot Watt University. Characterization results will show that at 100 K, a single photon detection efficiency (SPDE) of 4 % at 1310 nm wavelength was measured with a dark count rate of ~6 Mega counts per second. This result is the lowest reported noise equivalent power for any Ge-on-Si single-photon avalanche diode detector (1×10^{-14} WHz$^{-1/2}$) to date. The first report of 1.55 μm wavelength detection

efficiency measurements with such a device are presented and were more than an order of magnitude lower due to the reduced Ge absorption coefficient at these lower temperatures. A jitter of 300 ps was measured, and preliminary tests on afterpulsing showed only a small increase (a factor of 2) in normalised dark count rate when the gating frequency was increased from 1 kHz to 1 MHz.

6.2 Homojunction Ge SPADs

A number of investigations into homojunction Ge SPADs showed that there was significant dark count rates (DCR) due to band-to-band tunnelling, which is associated with having a high-field multiplication layer within a narrow bandgap. Afterpulsing was also a serious issue in these homojunction devices. A SPAD that combines a Ge absorption layer and a larger bandgap Si multiplication layer potentially offers low DCRs and noise operation across the telecommunications wavelengths. A Ge-on-Si SPAD also opens up the significant potential for on-chip integration with other silicon photonics components, which is a major driver for the integration of Ge-on-Si [171].

6.3 Ge-on-Si photodetectors

Due to the advancement of epitaxially growth techniques (discussed in chapter 1), thick Ge layers (> 1 μm) ideal for photodetectors can be epitaxially grown on Si with low TDD. As a result different types of Ge-on-Si photodetectors have been investigated and have shown high performance against their III-V counterparts; APDs [172-174], p-i-n detectors [175], and metal-semiconductor-metal detectors [176]. However, the demands of efficient single-photon detection using Ge-on-Si places challenging constraints on the design, growth, and fabrication. To date there has only been a few reports of Ge-on-Si SPAD characterization that have appeared in the literature, most notably by Lu et al., where a SPDE of up to 14 % at 1.31 μm was measured [177]. However, these devices had a very high DCR (> 10^8 Hz), where it is likely that the device has insufficient time to recharge before another dark count is triggered, resulting in an underestimate of the DCR for a given bias. Further evidence of this recharge issue is shown as the gating frequency

was increased from 1 kHz to 100 kHz where there is a notable decrease in the DCR that is the opposite as what is expected with afterpulsing. In addition, the SPDE was measured with an incident photon flux of 1 photon per pulse, thus giving a high probability of multi-photon pulses per incident on the device, potentially leading to an overestimation of the SPDE. Another report of a Ge-on-Si device claiming single-photon sensitivity was published by Aminian et al [178]. However, the detection efficiency in Geiger mode was measured only by analysis of the photocurrent above breakdown, which cannot be regarded as a valid single-photon counting characterization method.

6.4 Ge-on-Si SPAD design

The Ge-on-Si SPAD designed by collaborators from Herriot Watt University is presented in Figure 6.2. It is based on a separate absorption, charge, and multiplication (SACM) structure. There are several advantages of using Si as the high electric field multiplication region. Since Si has a larger bandgap than Ge, it should provide lower dark current from band-to-band tunnelling. In addition, Si should have fewer defects compared to Ge, which should lead to less after-pulsing. Afterpulsing refers to dark counts that originate from emitted carriers that were trapped during previous impact ionization events. This is the limiting factor for III-V SPADs operated at high frequencies. The SACM structure works as follows; Infrared photons are absorbed in the Ge absorption layer and create electron-hole pairs. The electrons are accelerated towards the Ge-Si interface and, once inside the high-field Si multiplication region, may undergo impact ionization. If the electric field is held above the avalanche breakdown threshold, further impact ionization of both holes and electrons can create a self-sustaining avalanche current, which is easily detectable. This avalanche current can only be extinguished by taking the device below the breakdown field, which can be achieved by various quenching approaches [163].

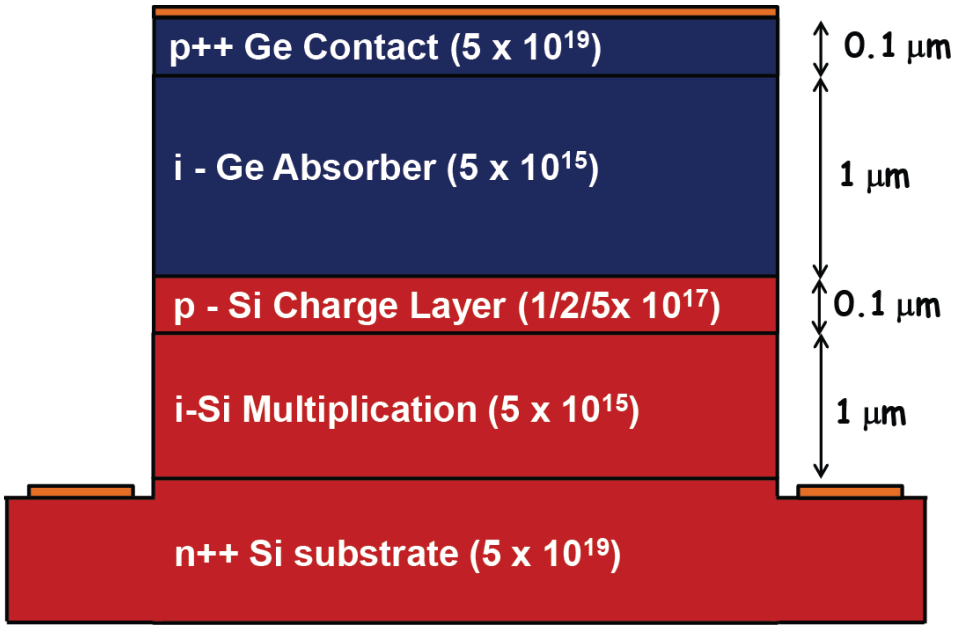

Figure 6.2. The designed Ge-on-Si SPAD based on a separate absorption, charge sheet, and multiplication region (SACM), showing layer thicknesses, and doping concentration.

The design is similar to the structure reported by Kang et al. [173]. The differences are our structure is designed with a thicker multiplication region and a different doping concentration of the charge sheet layer. The thicker multiplication layer increases the probability of a primary carrier triggering a self-sustaining avalanche current. This increased layer thickness also increases the voltage difference between punch-through (when the electric field extends into the Ge absorber) and avalanche breakdown voltage. This voltage difference becomes important when operating devices at lower temperatures since the breakdown voltage shifts with temperature whilst the punch-through voltage remains virtually unchanged, since it only depends on the doping of the charge sheet layer. If there was only a small difference between punch-through and breakdown, at lower temperatures the device may reach breakdown before punch-through has occurred, significantly reducing the SPDE at the design wavelengths of 1.31 and 1.55 μm.

6.5 Modelled electric field profile of the Ge-on-Si SPAD

Before growth, collaborators at Herriot Watt modelled the 2D electric field profile through the structures by Silvaco ATLAS. One of the main considerations was the doping concentration within the charge sheet layer. In SACM structures under reverse bias, the charge sheet must ensure that the electric field in the smaller bandgap Ge remains low (to avoid tunnelling) and well below its breakdown (~ 100 kV/cm), whilst the field in the multiplication layer is greater than the breakdown field in Si (~ 300 kV/cm) to provide impact ionization. Figure 6.3 shows the simulated electric field at 95 % of the breakdown voltage for three different charge sheet doping densities of 1×10^{17} cm^{-3}, 2×10^{17} cm^{-3}, and 5×10^{17} cm^{-3}. With a doping density of 1×10^{17} cm^{-3} (black line in Figure 6.3), the field in the Ge is above breakdown, therefore tunnelling and impact ionization would increase the DCR.

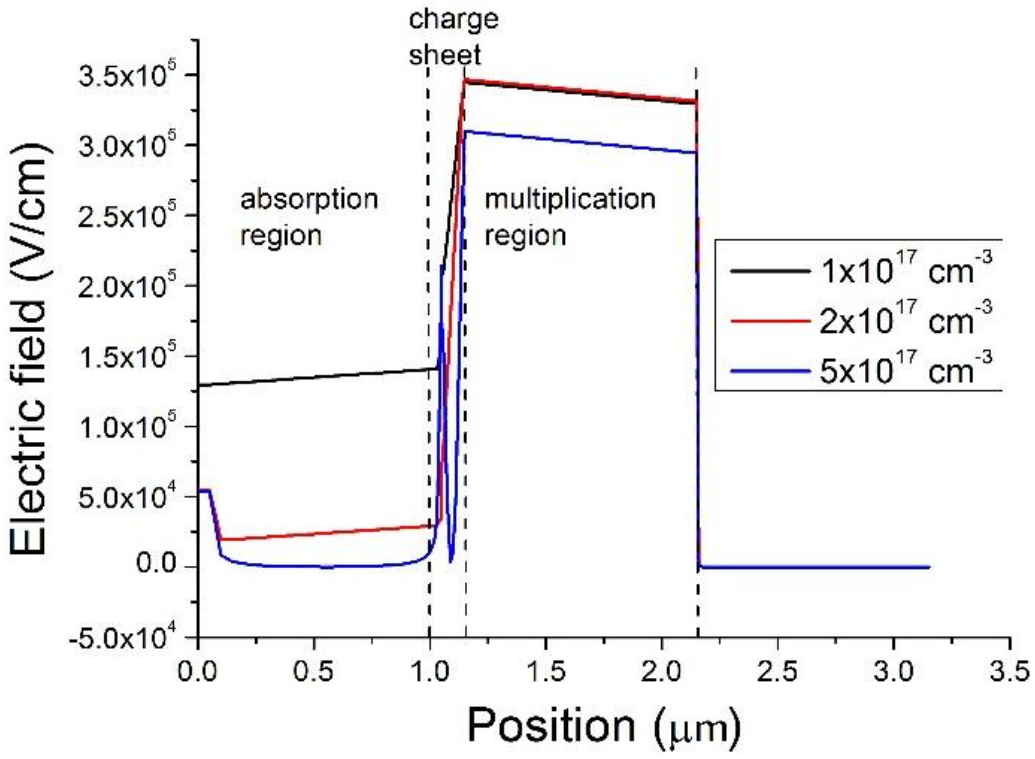

Figure 6.3. The simulated 2D electric field profile through the device for three different charge sheet doping densities. The x-axis corresponds to the distance from the top contact.

A doping concentration of 5×10^{17} cm^{-3} (blue line) results in too much of the electric field being dropped across the charge sheet and consequently the Ge is not depleted and therefore no photo-generated carriers will drift to the multiplication region to initiate an avalanche. However, a doping density of 2×10^{17} cm^{-3} (red line), depletes the Ge absorption region with a moderate electric field such that photo-generated carriers will drift into the multiplication region. Figure 6.4 is the simulated reverse bias $I-V$ characteristics and for a doping concentration of 2×10^{17} cm^{-3} in the charge sheet region the expected breakdown voltage is approximately -37 V.

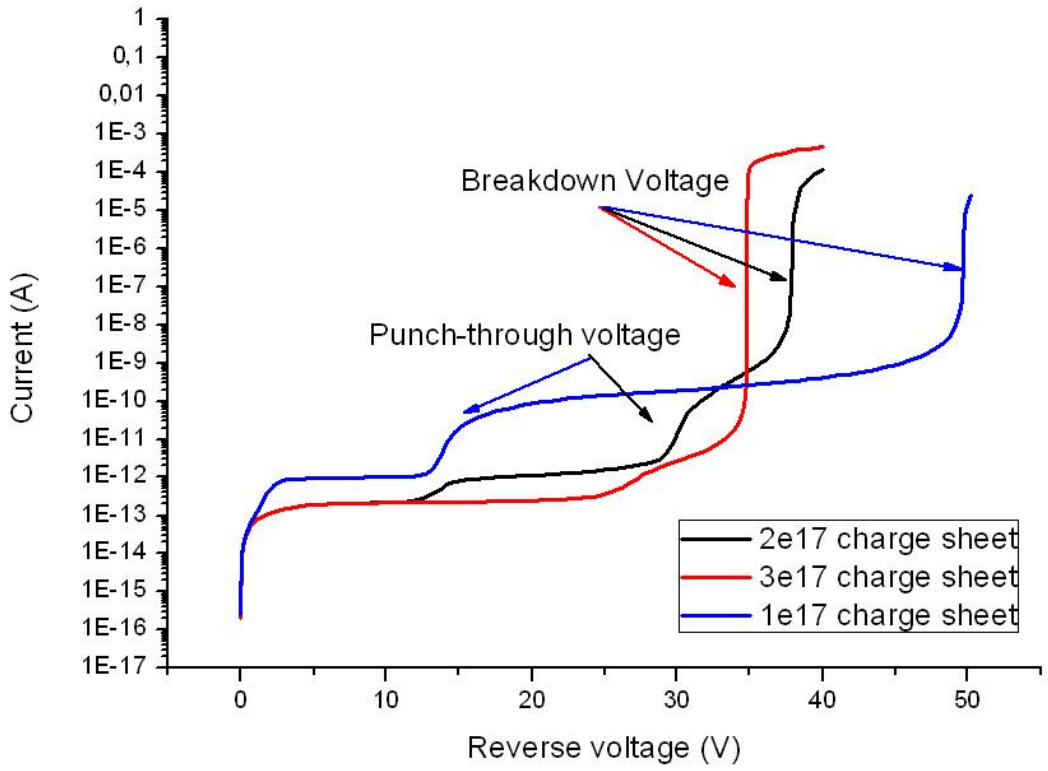

Figure 6.4. The simulated current-voltage characteristics of the Ge-on-Si SPAD for different doping concentrations within the charge sheet region.

6.6 Ge-on-Si SPAD growth

Collaborators at Warwick University grew the designed SPAD wafers (see Figure 6.2) each containing a different dopant concentration within the charge sheet region to account for growth tolerances. The structures were grown by reduced-pressure chemical vapour deposition on highly doped n-type Si substrates. 1 μm

thickness of intrinsic Si was grown to form the multiplication region. A low temperature Ge seed layer of 50 nm was grown followed by a high temperature growth of intrinsic Ge. Finally, a highly boron-doped (5×10^{19} cm^{-3}) p-Ge layer was grown.

6.7 Ge-on-Si SPAD fabrication

Fabrication of the SPAD structures followed the same mesa design used for the bulk and MQW Ge LED structures as previously discussed. Mesa geometry was required to confine the electric field profile within the active region of the device. A planar SPAD design provides lower dark currents but the implantation required to define the active area and floating guard ring would be difficult to achieve with this structure due to the high activation anneal temperature required. This would cause detrimental diffusion of dopants and Si and Ge at the interfaces. The minimum device size was limited by the laser spot that could be focussed by Herriot Watt's single photon characterization setup and this meant that fabricated devices were greater than 20 μm in diameter. Therefore, cylindrical mesas, ranging from 25 to 500 μm in diameter, were defined and etched anisotropically down to the highly doped Si substrate, by an inductively coupled plasma (ICP) reactive ion etch tool using fluorine-based chemistry (SF_6/C_4F_8) as previously described in chapter 2. Ni was chosen for the top and bottom Ohmic contacts, as it is known to form the lowest electrical resistivity phases for silicides and germanides [94, 179]. As previously shown in chapter 3, due to Fermi level pinning just above the Valence band, an Ohmic contact to p-Ge is straightforward. However, for the same reasons why Ni was chosen as the metal contact to n-Ge it also makes the ideal candidate for metal contact to p-Ge. It is a shallow diffuser, does not oxidise easily, and has the lowest electrical resistivity phases out of all the transition metals.

6.7.1 Single layer anti-reflection coating

The structures were then passivated with PECVD Si_3N_4 that also acts as a single layer anti-reflection (AR) coating designed for 1.31 μm wavelength. The perfect

single layer AR coating for a semiconductor can be calculated by using the following two equations

$$(d = \lambda_0 / 4n_f) \tag{6.1}$$

$$n_f = \sqrt{n_0 n_s} \tag{6.2}$$

Where d is the thickness of the AR coating, λ_0 is the wavelength of incident light, n_f is the ideal refractive index of the AR coating, and n_0 is the refractive index of air and n_s is the refractive index of substrate. Therefore, the ideal single layer AR coating for Ge at 1.31 μm wavelength light should have a refractive index of $n_f = 2.07$ and a thickness of $d = 158.2$ nm. PECVD Si_3N_4 that is available within the JWNC has a refractive index of ~ 2.0, and the film thickness can be accurately controlled. Since the SPAD structures are also characterised at 1.55 μm, the single AR coating performance at this wavelength was investigated. From Figure 6.5 it is clear that a single layer AR coating designed for 1.31 μm performs worse at 1.55 μm wavelength but the amount of reflected light is still only 3.5 %. For these prototype devices, this is adequate and in the future multi-layer AR coatings can be employed that will provide greater broadband performance.

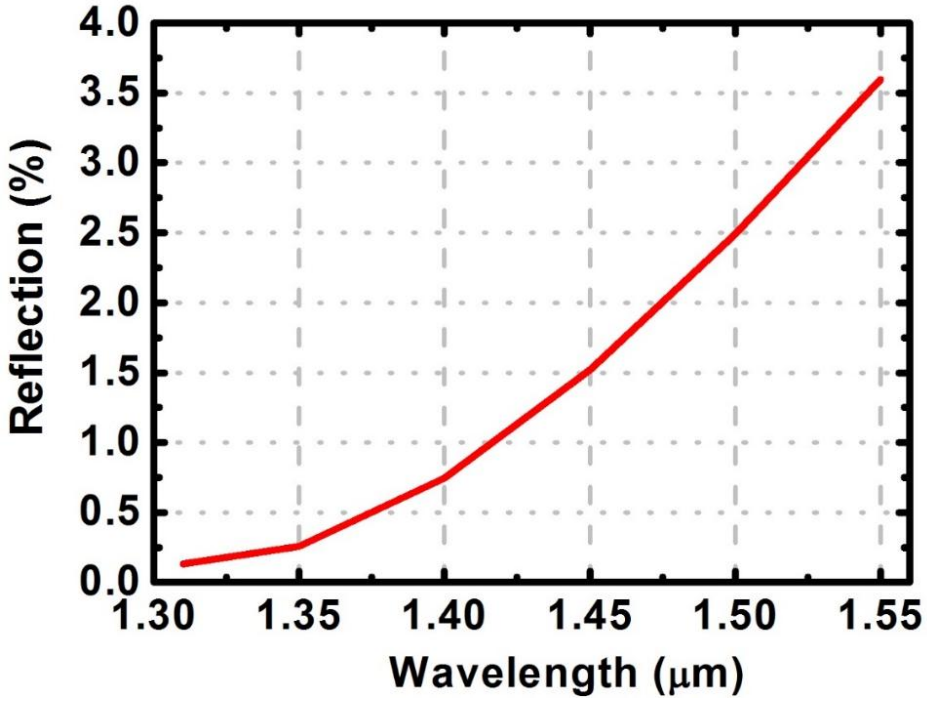

Figure 6.5. The calculated reflection versus wavelength for a silicon nitride single layer anti-reflection coating quarter wavelength matched to 1.31 μm wavelength on Ge.

6.7.2 ICP-PECVD Si_3N_4 planarization

One of the challenges of fabricating the SPADs was dealing with the large mesa height of 2.3 μm. In order to facilitate the next stages of the fabrication such as via interconnects and bond pads, the devices were planarised with ICP-PECVD Si_3N_4. Since ICP-PECVD Si_3N_4 is deposited at room temperature it is well below the glass transition temperature of photo, and e-beam resists, therefore it can be incorporated into a lift-off process. Figure 6.6 (a) and (b) show optical microscope images of patterned and successfully lifted off areas of Si_3N_4 from a test sample. This process is well suited compared to other planarization techniques that would interfere with the single layer AR coating.

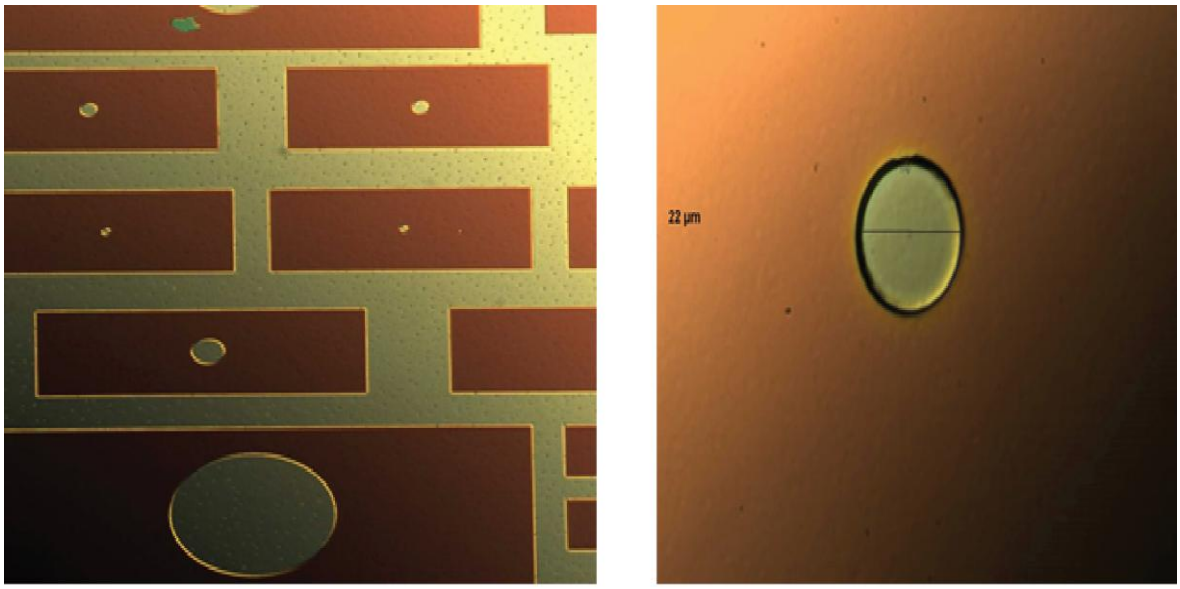

Figure 6.6. An optical microscope image of (a) patterned ICP-PECVD Si_3N_4 and (b) a close up of a 25 μm diameter circle lifted off.

After the patterning and the lift-off of 1.5 μm of ICP-PECVD Si_3N_4, via holes were etched in CHF_3/N_2 to allow interconnects to the contacts and then bond pads of 1.2 μm of Al were sputtered.

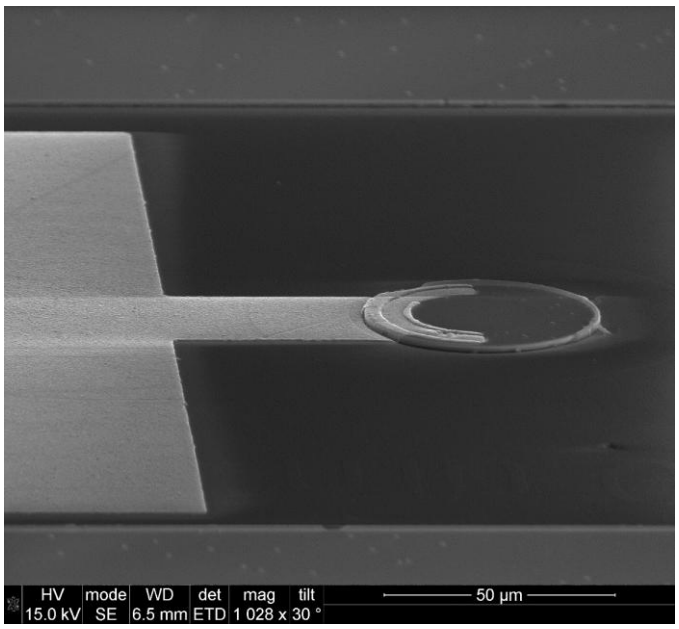

Figure 6.7. A scanning electron microscope image of a sputtered Al top bond pad on the Ge-on-Si SPAD.

As previously described in chapter 2, sputtering allows coating of sidewalls that ensures bond pads will be electrically connected. Figure 6.7 is an SEM image of an Al top bond pad sputtered on a Ge-on-Si SPAD. It is clear there is a complete connection of the Al along the side of the mesa. The final stage of the fabrication was to cleave the samples and wire bond them to a 3 x 3 mm header package used by Herriot Watt University.

6.8 Characterization of the Ge-on-Si SPAD

Prior to sending the fabricated SPADs for single photon characterization at Herriot Watt University, I carried out current-voltage $(I\text{-}V)$ characteristics under dark and photo-illumination at 1.31 μm wavelength. An $I\text{-}V$ for a 25 μm diameter SPAD with designed 2×10^{17} cm^{-3} doping concentration in the charge sheet region under dark and illumination is shown in Figure 6.11.

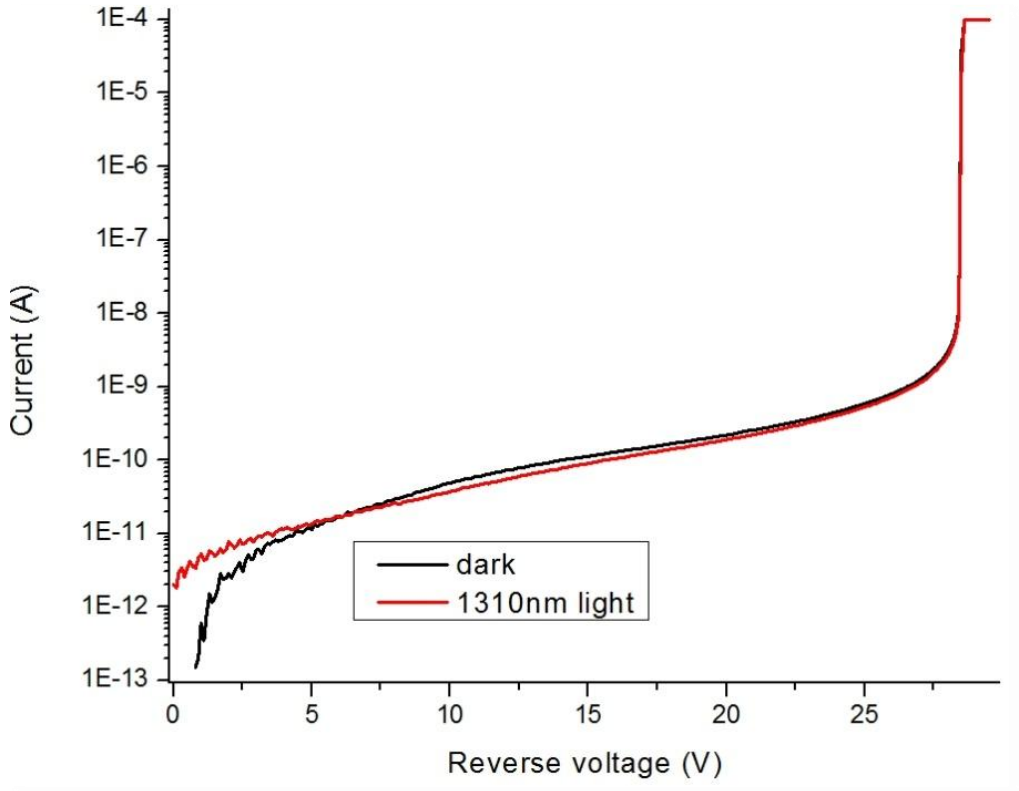

Figure 6.8. The reverse bias current-voltage characteristics at room temperature for a 25 μm diameter Ge-on-Si SPAD under dark and 1.31 μm wavelength light illumination.

It is clear that there is no photocurrent generated under 1.31 μm illumination and the breakdown of the devices has shifted to a lower voltage than modelled (-37 V). This behaviour was also observed for SPADs fabricated from the other wafers with different charge sheet doping concentrations. The most likely reason why no photocurrent was generated is due to the doping concentration in the charge sheet layer being incorrect. As previously discussed the charge sheet controls the strength of the electric field in the Ge. To confirm this was a doping concentration problem a 1 cm^2 blank chip from the wafer with 2×10^{17} cm^{-3} doping concentration was sent for secondary ion mass spectrometry (SIMS) analysis. It is clear from Figure 6.9 that the boron concentration within the charge sheet layer is over two orders of magnitude greater than designed and from Figure 6.10 it is obvious that there is a significant phosphorous tail within the Si absorption region that is caused by dopant segregation from the high temperature growth.

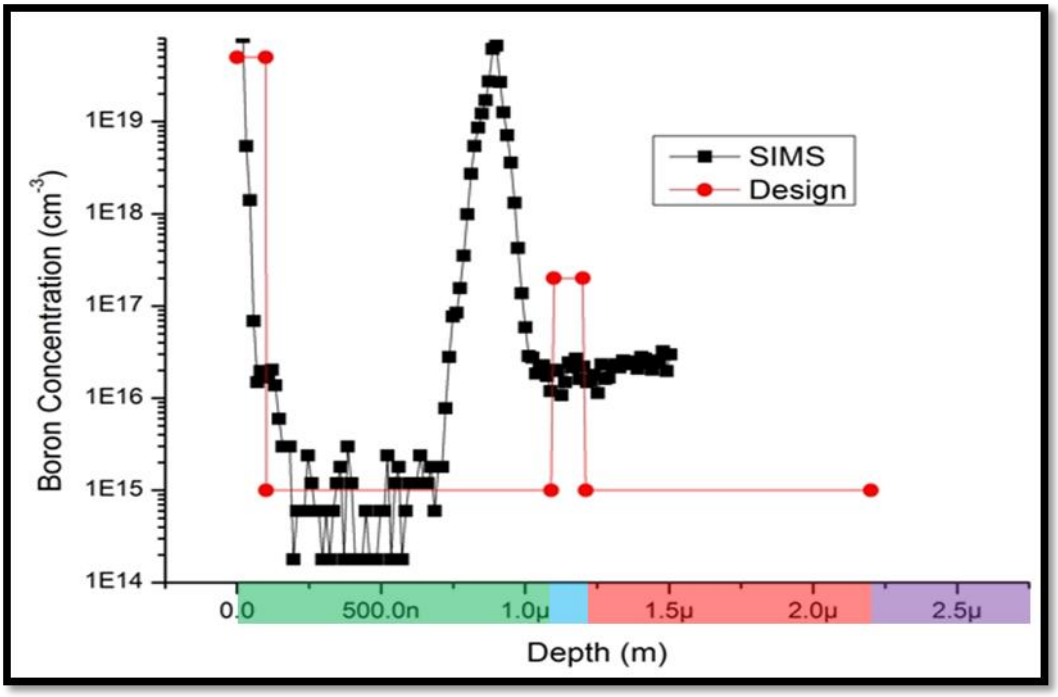

Figure 6.9. Secondary ion mass spectrometry (SIMS) analysis of the boron concentration throughout the Ge-on-Si SPAD. The designed doping concentration is also plotted. Overlay colours on the x-axis represent different regions of the structure: Ge absorption (green), p-Si charge sheet (blue), i-Si multiplication (red), and n-Si substrate (purple).

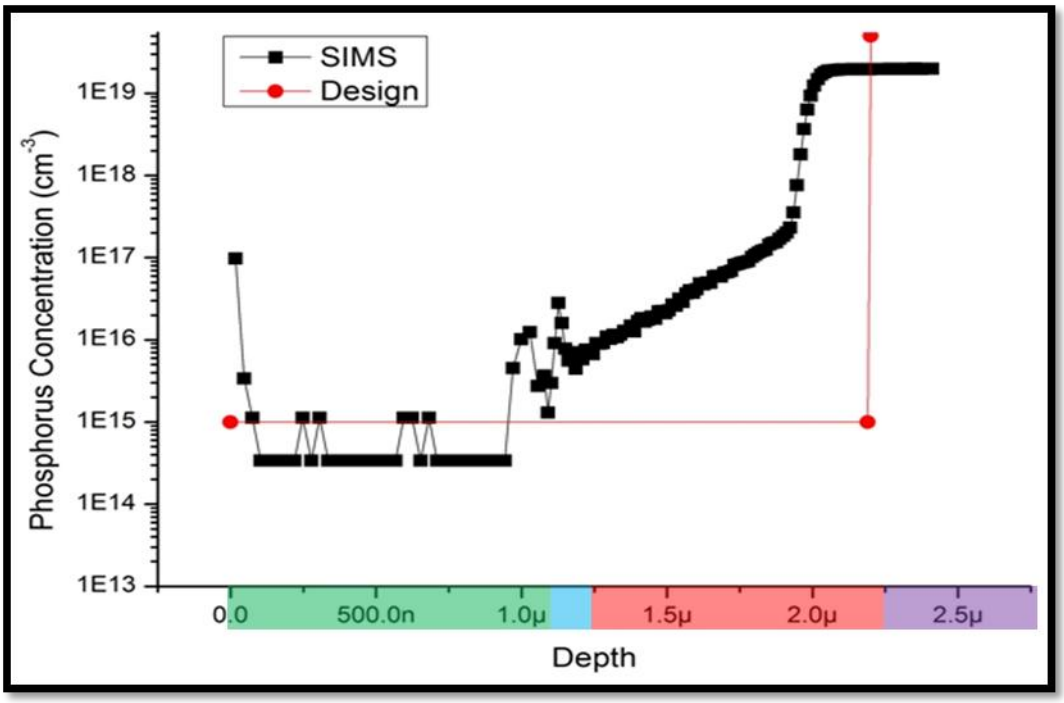

Figure 6.10. Secondary ion mass spectrometry (SIMS) analysis of the phosphorous concentration throughout the Ge-on-Si SPAD. The designed doping concentration is also plotted. Overlay colours on the x-axis represent different regions of the structure: Ge absorption (green), p-Si charge sheet (blue), i-Si multiplication (red), and n-Si substrate (purple).

6.9 Second generation growth of Ge-on-Si SPADs

After optimization by Warwick University, a second generation of wafers were grown. SPADs were fabricated using the same process as detailed for the first generation. Figure 6.11 shows the $I-V$ characteristics for a 25 μm diameter device from the second generation with a designed charge sheet doping density of 2×10^{17} cm^{-3} under dark conditions and illumination at various temperatures. A LN_2 cryostat was used to control the temperature from 100 to 300 K. There is a clear difference between the reverse $I-V$ characteristics at room temperature for the first generation of fabricated SPADs that breakdown at – 27 V and the second generation, which breakdown at -36 V. This matches well with the modelled breakdown for these devices (see Figure 6.4), indicating the doping concentration within the charge sheet was as designed. To confirm that the Ge depleted, photocurrent measurements were performed at 100 K under 1.31 and

1.55 μm wavelength illumination. The results are shown within the inset of Figure 6.11 and it is clear that the device is generating a photocurrent.

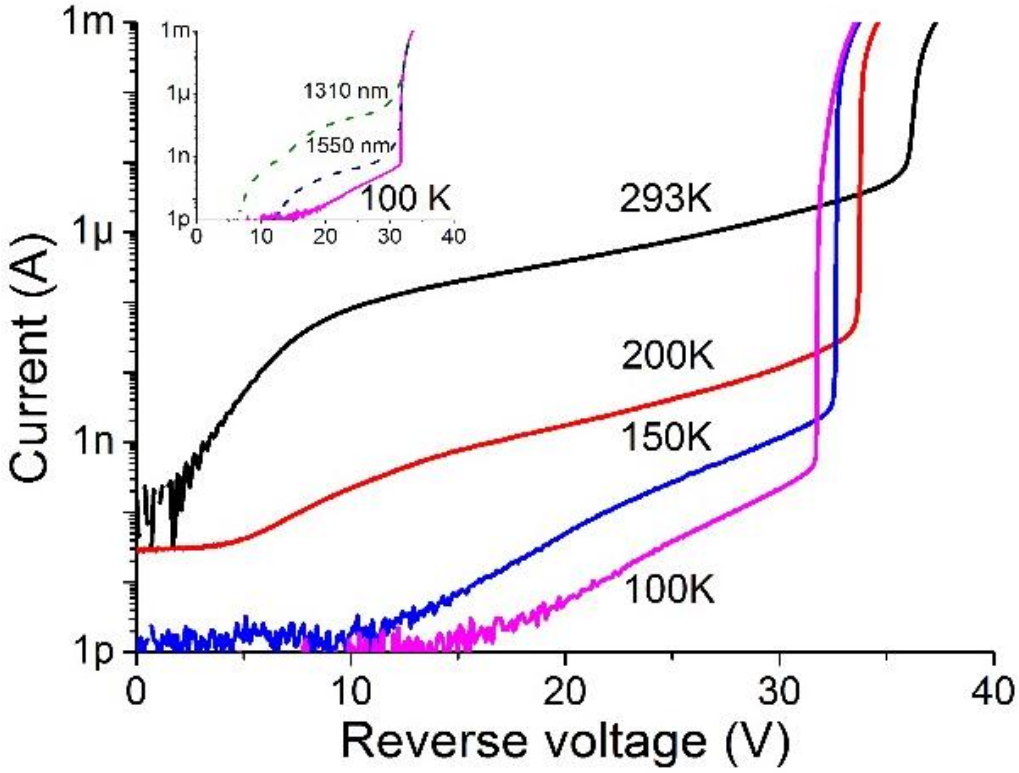

Figure 6.11. The reverse bias current-voltage characteristics at temperatures between 100-300 K for a second-generation 25 μm diameter SPAD with a designed charge sheet doping concentration of 2×10^{17} cm^{-3} under dark conditions. The inset shows the dark current at 100 K (solid magenta line) and the photocurrent under 1.31 μm (dashed green line) and 1.55 μm (dashed blue line) wavelength illumination.

6.10 Single Photon characterization

6.10.1 Single photon setup

As it was clear that the second generation of Ge-on-Si SPADs were generating a photocurrent under 1.31 and 1.55 μm wavelength illumination, they were then sent to Herriot Watt University for single photon characterization. The single photon characterization setup that Herriot Watt uses is illustrated in Figure 6.12. The Ge-on-Si SPADs characterised were illuminated by <<1 photon/pulse photon flux at 1.31 and 1.55 μm wavelengths in accordance with accepted techniques of

time-correlated single-photon counting, as described, for example, by Becker [180].

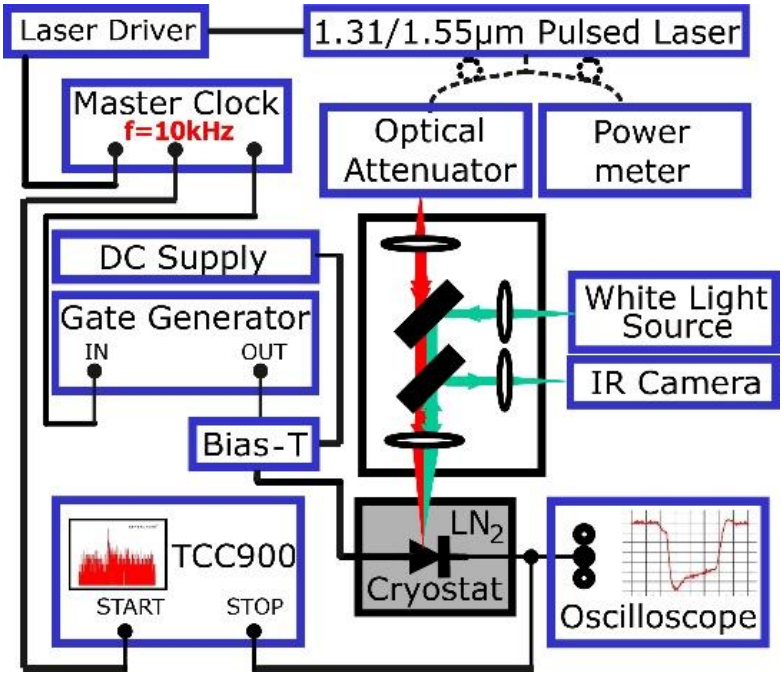

Figure 6.12. A diagram of the components used in the single photon characterization setup performed by Herriot Watt University.

The devices were mounted in a liquid nitrogen cryostat enabling stable temperature tuning between 77-300 K. All the characterisation took place at temperatures below 150 K in order to reduce the dark current. Pulsed picosecond semiconductor laser diodes were used to test the detection efficiency at both 1.31 and 1.55 μm. These were coupled into single-mode fibre (SMF-28) and into a 50/50 fibre splitter; one output was used to constantly monitor the optical power, the other passed through an optical attenuator to ensure a photon-flux of < 0.1 photons per pulse (on average) was incident on the device. For characterization purposes, the devices were operated in gated-mode, and DC biased a few volts below the breakdown voltage (V_{bd}). An electrical pulse, typically 10 ns duration biased the device above V_{bd}, into the so-called "Geiger" mode of operation. When an avalanche was initiated (by either a dark count or photo-generated

event), the avalanche current persisted until the end of the gate when the voltage was brought back below V_{bd}.

In the future, Herriot Watt are planning on moving to an active quenching circuit, which would quench the avalanche current more rapidly, hence minimizing the charge flow per event, thus reducing the probability of trapped carriers that cause afterpulsing [163]. The output pulse from the device was split to enable oscilloscope traces to be recorded whilst simultaneously providing the stop signal for the photon-counting card (Edinburgh Instruments TCC900). The start signal was provided by a master clock that has three outputs: one for the TCC900, another for the laser driver, and the final output for the gate generator. For each operating condition, two photon-counting histograms were recorded; one in completely dark conditions, and one with an attenuated laser pulse coincident with the gate on the detector. The DCR and SPDE can be extracted from these histograms by summing the counts within a certain region of interest. Since the gate-on and gate-off times result in the device not being at a constant bias for the whole gate duration, only a portion from the centre of the histograms was considered- this portion has a flat background level showing that the bias was stabilised and gives a true value for both SPDE and DCR. Other methods, such as using a photon-counter over a pre-determined gate period, may under-estimate DCR and over-estimate SPDE (since it is difficult to ascertain the effects of afterpulsing with a gated photon-counter which does not possess the necessary timing resolution).

6.10.2 Single Photon detection efficiency

Figure 6.13 shows the bias-dependent SPDE and DCR for a 25 μm diameter device operated at 100 K. This device had a dark current of ~ 0.5 nA measured at 95 % of V_{bd}. The SPDE depends mainly on the photon absorption probability in the depleted absorption region, the probability of electron drift into the multiplication region, and the avalanche triggering probability in the multiplication region. Whilst the first two phenomena are unlikely to be strongly dependent on the excess bias, the avalanche triggering probability increases

linearly with excess bias, before saturating. In Figure 6.13 it can be observed that the SPDE increases linearly with excess bias due to the increasing field within the device. At 10 % excess bias, a SPDE of 4 % at 1.31 μm wavelength is measured. This shows a significant improvement when compared with strained SiGe/Si MQW structures (only 0.001 % at 1210 nm wavelength) [181]. These results show a good agreement with the SPDE obtained with a commercially-available, planar geometry, homojunction Ge APD operated in Geiger mode, where an SPDE of between 4 % and 30 % was reported at 1.31 μm wavelength and a temperature of 77 K [182].

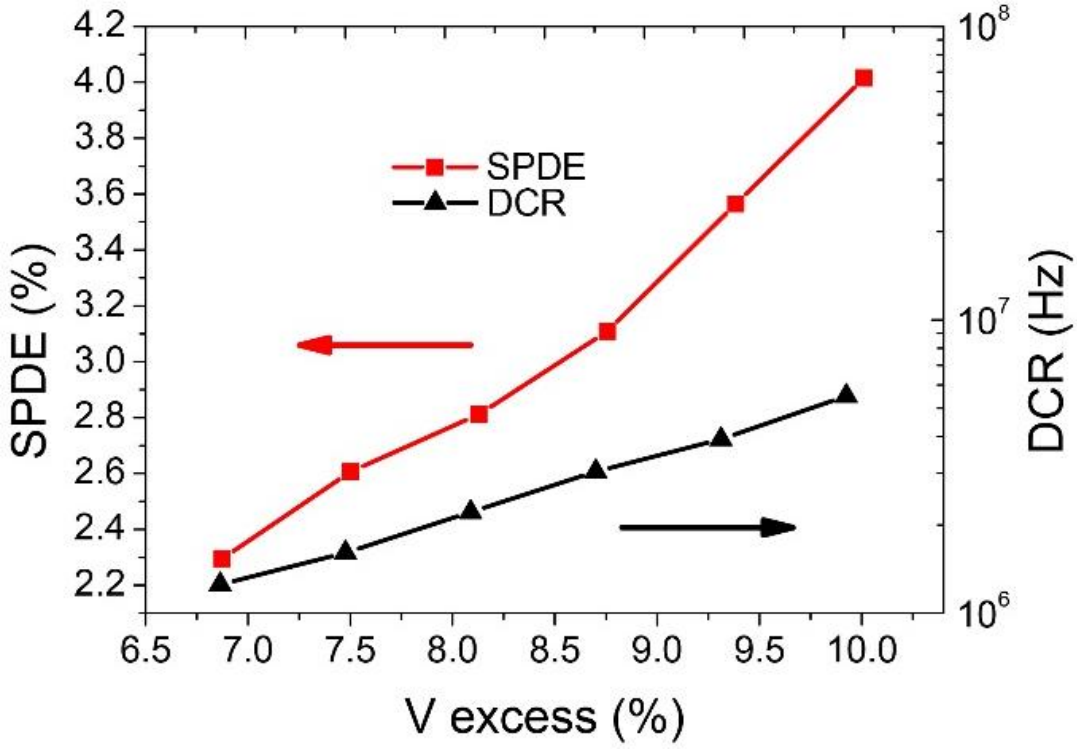

Figure 6.13. The single photon detection efficiency (SPDE) and dark count rate (DCR) as a function of excess bias for a 25 μm diameter Ge-on-Si SPAD at 100 K measured at 1.31 μm wavelength.

These devices exhibit a high DCR that limits the operating temperatures between 100 K and 150 K. Additionally, the high levels of DCR restricted the maximum excess bias applied. As shown in Figure 6.11, a DCR of 10^6-10^7 Hz was obtained at 100 K. Similar values were also obtained using commercially available Ge APDs as SPADs. These Ge homojunction APDs were, however, planar devices, whereas our devices are mesa geometry and thus suffer the deleterious effects caused by the

high density of surface states at the sidewalls. Compared to InGaAs/InP planar SPADs, the DCR is several orders of magnitude higher - DCRs of 10^2-10^3 Hz are achievable at this temperature [164]. The high DCR is likely to be caused primarily by surface effects. The exponential increase in DCR with increasing excess bias demonstrates that our devices recover fully before the subsequent gate period.

6.10.3 Noise equivalent power

Based on the single-photon measurements the noise equivalent power (NEP) was calculated from equation (6.3).

$$NEP = \frac{h\nu}{SPDE}\sqrt{2DCR} \tag{6.3}$$

NEP is a measure of the sensitivity of a photodetector, the lower the NEP the more sensitive the detector. Overall, the NEP was similar across the range of excess voltages measured. However, 4 % SPDE and an NEP of 1×10^{-14} $WHz^{-1/2}$ at a wavelength of 1.31 μm compares well with other work where NEPs of ~ 1.6×10^{-14} $WHz^{-1/2}$ and 4×10^{-15} $WHz^{-1/2}$ were reported using commercially-available planar all-Ge APDs operated in Geiger mode at a temperature of 77 K [182]. Although it is not explicitly stated by Lu et al. [183], an NEP of ~ $3x10^{-14}$ $WHz^{-1/2}$ at 1310 nm wavelength can be inferred from the quoted SPDE and DCR at a higher temperature of 200 K. However, there remains a performance gap compared to InGaAs/InP SPADs, where NEPs of 1×10^{-17} $WHz^{-1/2}$ and below at 1.55 μm wavelength have been reported at a temperature of 193 K [164, 165].

6.10.4 Jitter investigation

Jitter was investigated at various excess bias levels. The measured jitter was a convolution of the laser pulse width (~ 50 ps), the detector response, and the contribution from the rest of the acquisition system. The minimum jitter at full width half maximum (FWHM) is shown in Figure 6.14 and was measured to be 300 ps at 10 % excess bias. With the same experimental setup, Herriot Watt have previously measured jitter of less than 80 ps with homojunction Si SPAD detectors,

hence it is assumed that the overall measured jitter is dominated by the detector contribution. This value shows a good agreement with the jitter measured previously (~ 100 - 350 ps, 1.31 μm wavelength, laser pulse width = 40 ps) for homojunction Ge APDs operated in Geiger mode [182]. The use of histograms for characterization provides some information on afterpulsing, as well as jitter. If the background levels are the same for both dark and light measurements (as in Figure 6.14), it is an indication that the detector is operating in a regime with negligible afterpulsing.

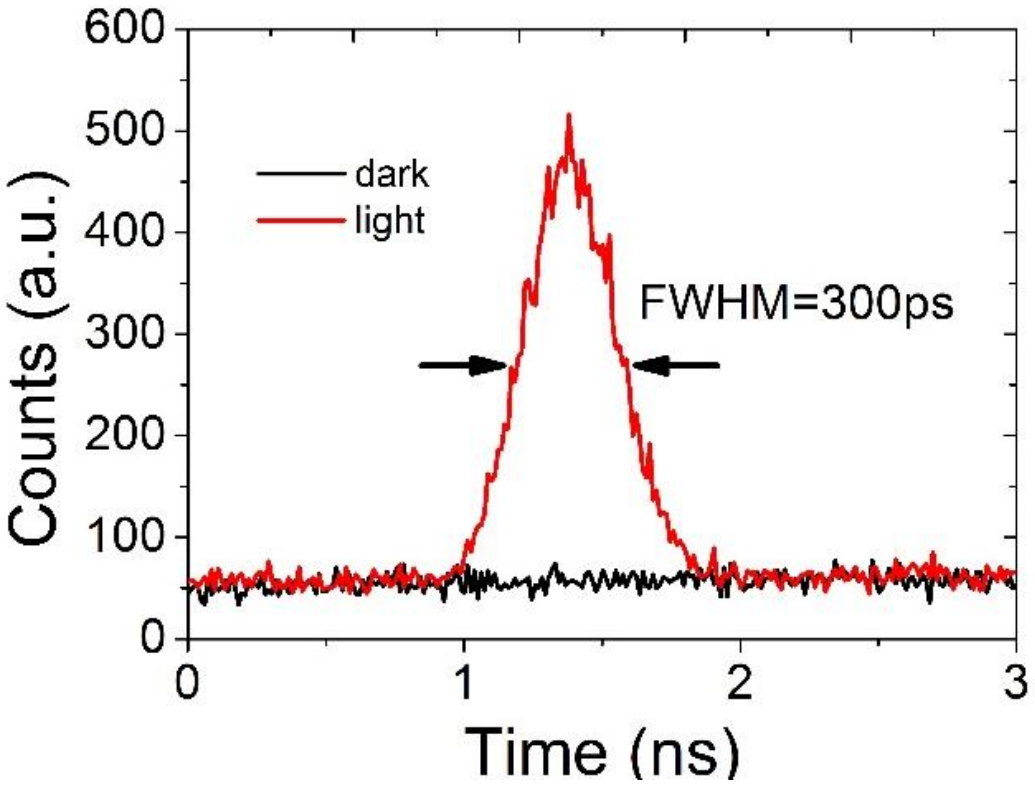

Figure 6.14. The “Dark” and “Light” histograms measured using time-correlated single-photon counting for a 25 μm diameter device at a temperature of 100 K.

6.10.5 Dark count rate as a function of the gating frequency

To study the effect of afterpulsing with these devices the simple method of increasing the gating frequency whilst observing the impact on the DCR was used. A slight increase (~ factor of 2) in the normalised DCR was observed when increasing the gating frequency from 1 kHz to 1 MHz at a temperature of 150 K as shown in Figure 6.15. This behaviour was also observed using two different Ge

homojunction APDs operated in Geiger mode [182]. Although InGaAs/InP SPADs have lower DCR at these temperatures, they show a rapid increase in DCR due to afterpulsing at frequencies above 100 kHz, perhaps highlighting a potential advantage of Ge-on-Si devices [164].

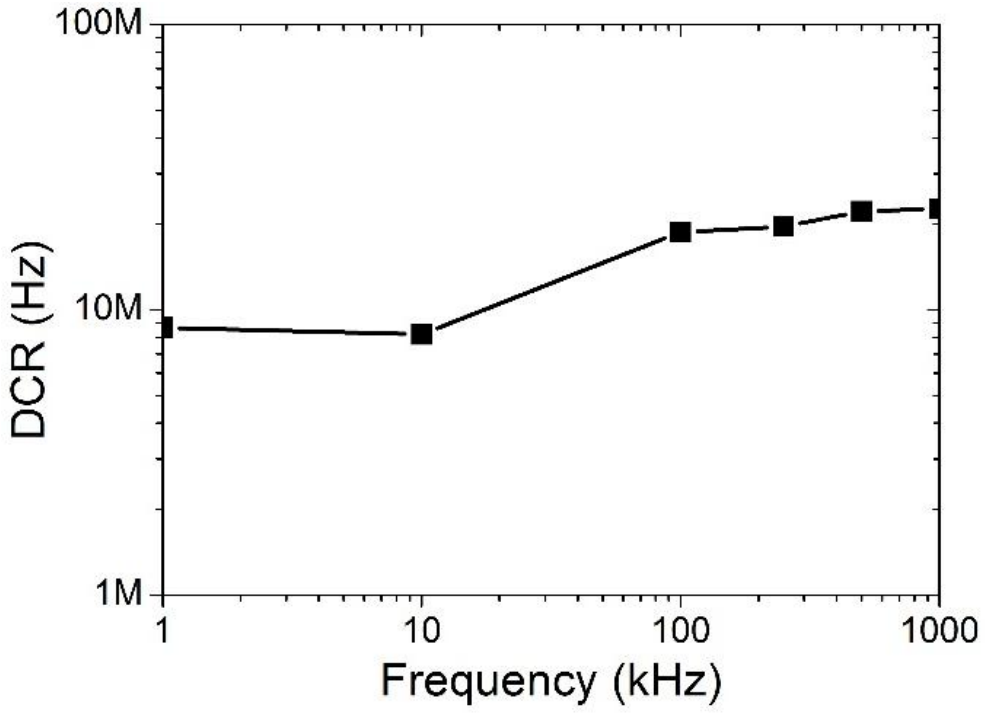

Figure 6.15. The dark count rate (DCR) versus the gating frequency for a 25 μm diameter device at a temperature of 150 K showing dependence of the normalised DCR with gate frequency.

6.10.6 Performance at 1550 nm wavelength

The performance at the longer wavelength of 1.55 μm was measured on a device at 125 K. A SPDE of ~ 0.15 % at 6 % excess bias was measured, resulting in an NEP of 5×10^{-12} $WHz^{-1/2}$ with a jitter of 420 ps (FWHM). The lower SPDE at 1.55 μm wavelength can be explained by the band gap increase of Ge at 125 K and hence the absorption at this wavelength decreases rapidly. Assuming ~ 0.25 % tensile strain in the Ge layer due to thermal expansion mismatch, the direct band gap at 125 K is 0.84 eV, hence the 1.55 μm (0.8 eV) photons lie outside the direct band absorption edge [169]. For this reason there is a factor of > 10 decrease in the SPDE between 1.31 and 1.55 μm wavelength as previously observed with a Ge

homojunction APD operated in Geiger mode at 77 K, where a SPDE of 30 % was measured at 1.31 μm but only 1 % at 1.55 μm wavelength. [182].

6.11 Future improvements

We plan to investigate different passivation techniques for mesa sidewall surface states, as well as planar device geometries in future work. It is also worth noting that reducing the TDD may also help to decrease the dark current [184].Higher excess biases will reduce this value in future optimised devices. As mentioned previously, we expect that process optimization will reduce the DCR to a level that will allow higher temperature operation, which will significantly improve the SPDE at 1.55 μm wavelength.

6.12 Conclusion

In summary, Ge is being investigated as a material for single photon detection at 1.55 μm wavelength due to its absorption coefficients that are comparable to InGaAs. A Ge-on-Si SPAD would allow CMOS compatible SPADs on-chip to take advantage of potential applications such as quantum computing. In this work epitaxial Ge-on-Si SPAD mesa geometry devices were fabricated and characterised in terms of their single photon detection efficiency. The 1.31 μm wavelength performance was comparable to the best homojunction Ge APDs previously reported for Geiger mode operation. The efficiency at 1.55 μm wavelength is an order of magnitude lower due to the reduced absorption coefficient at low temperatures. DCRs of ~ 10^6-10^7 were measured: values which are anticipated to be significantly reduced by optimization of the mesa sidewall passivation or by moving to a planar device geometry. At 100 K the NEP was measured to be 1×10^{-14} $WHz^{-1/2}$ (at λ =1310 nm) and was fairly consistent over the range of measured excess biases. The total measured jitter at FWHM varied with excess bias as expected, but was as low as 300 ps. The contribution of afterpulsing to the DCR at higher gating frequencies was found to be negligible, indicating a potential advantage over the InGaAs/InP materials system.

7 Conclusions and future work

In conclusion, there is much interest in the monolithic integration of photonic devices on a single Si chip to overcome the bottleneck currently faced with existing metal interconnects. Other applications apart from chip-to-chip optical interconnects, consist of providing more functionality with the combination of CMOS electronics and Si photonics to produce lab on chip devices. The ability to take advantage of the large investments made in CMOS electronics will potentially allow a substantial reduction of the cost to produce Si photonic chips. Integration of Ge on top of Si substrates allows for active CMOS compatible photonic devices at the low loss optical fibre wavelengths and beyond. The main challenge is the large lattice mismatch between Ge and Si that results in misfits and dislocations when Ge is grown above the critical thickness. There has been several growth techniques developed to overcome this mismatch such as growing on a fully relaxed SiGe buffer, the two-step growth, and selective area growth, all of which reduce the threading dislocation substantially. The majority of Ge epitaxy to date has been done by chemical vapour deposition at lower growth temperatures compared to Si epitaxy. From these growth techniques high performance Ge-on-Si photodetectors and modulators have been demonstrated.

Once of the fundamental challenges preventing the integration of Ge into a range of devices is the ability to make Ohmic contacts to both n and p type Ge. Ge CMOS is being investigated, where its higher carrier mobilities compared to Si could lead to reduced power operation. However, one of the roadblocks to realizing such devices has been the difficulty to achieve an Ohmic contact to n-Ge because the Fermi level is pinned just above the Valence band. The ideal Schottky-Mott theory for metal-semiconductor contacts breaks down and the Schottky barrier height is independent of the chosen metal work function. It has been shown experimentally that the Fermi level pinning occurs at 0.02 eV just above the Valence band. The normal approach to overcome a large Schottky barrier height is by having a large doping concentration since the barrier width is inversely proportional to the doping. However, it has been difficult to achieve a large doping concentration in n-Ge. The conventional method to dope by ion-implantation introduces allot of defects in Ge that act as p-type acceptor states, which lowers the electrical active dopant concentration. Therefore, this approach is undesirable. In this work a low

temperature Ohmic contact process was developed on n-Ge, which was in-situ doped whilst epitaxially grown by collaborator at Warwick University. The 100 nm Ni contact annealed at 340 ℃ for 30 s in N_2 gas by rapid thermal annealing produces a specific contact resistivity of $(2.3 \pm 1.8) \times 10^{-7}$ Ω-cm^2. Transmission electron microscopy analysis revealed the contact consisted of two germanides that grow simultaneously, which is unusual for thin film reactions with semiconductors that are usually sequential. The high resistivity phase of Ni_5Ge_3 grows until a critical thickness of ~20 nm is reached before the low resistivity NiGe phase starts to grow to the detriment of the Ni_5Ge_3. To improve the contact required eliminating the Ni rich phase of Ni_5Ge_3. Therefore a NiGeNi (20/20/20 nm) contact scheme was proposed with the idea being that the middle amorphous Ge acts as diffusing species, to transform the higher resistivity phase of Ni_5Ge_3 into NiGe and leave only the low resistivity phase of NiGe. This contact was annealed at 340 ℃ for 30 s. This process was compared to a wide range of contact technologies on Ge and it is comparable to the best result obtained by insertion of a doped interfacial layer of ZnO.

One key Si photonic component that is still missing and is required for the realisation of optical interconnects and lab on chip applications is an efficient electrically pumped laser. The most advanced methods to date have come from III-V lasers bonded by the SOI method, however fundamentally III-Vs are still not ideal as it acts as a dopant within Si and therefore cannot be integrated into Si foundries very easily. An alternative approach that is CMOS compatible is to use Ge. Even though Ge is an indirect bandgap semiconductor and therefore regarded as a poor light emitting material due to its radiative recombination being dependent upon a phonon assisted process. The difference between the direct and indirect is only 136 meV and can be engineered to be more direct by a combination of n-type doping and tensile strain. Large n-type doping has the effect of filling all available states in the L-valley therefore any injected electron must reside in the Gamma that has radiative recombination rates comparable to III-Vs. MIT have demonstrated an optical and electrically pumped Ge laser. However, it required very high thresholds of greater than 300 kA/cm^2 before the onset of lasing. An alternative approach to realise an efficient Ge LED or laser will require higher levels of strain than what is generated purely from the thermal

mismatch between Ge and Si during growth at high temperature and then subsequently cooling to room temperature. Modelling in the literature suggests that when Ge becomes direct bandgap (1.7 – 2.5 % tensile strain) very large optical gain can be achieved for lower injected carrier densities and doping concentrations. The approach used so far to generate high levels of tensile strain in Ge has mostly been membrane based, where a thinner membrane stressed either mechanically or by a metal film can produce high levels of strain. The difficulty with the membrane approach is to generate high levels of strain requires using thin (< 50 nm) membranes. It would be difficult to fabricate the membrane in CMOS Si foundries and regulate the temperature during operation to keep the wavelength of emission fixed. A more robust approach is by using process-induced strain where a Si_3N_4 stressor is deposited on the Ge to impart tensile strain. This process is already used in high-end CMOS lines to impart strain into the Si channel to increase the mobility. A highly compressive Si_3N_4 film deposited by plasma enhanced chemical vapour deposition has been developed, where the stress of the Si_3N_4 is controlled by the RF power used during the deposition. The stress of the film was measured by the curvature method. Ge light emitting diodes 25 to 500 μm in diameter were fabricated and covered with Si_3N_4 stressors. Fourier transform infrared (FTIR) characterization of the electroluminescence (EL) emitted from the devices under continuous wave and pulsed regime revealed that that there were two peaks clearly visible at 1.6 and 1.8 μm. However, there was no shift observed from varying the stress in the Si_3N_4 film and it was established that the devices were too large to adequately strain. Therefore, nanostructures of 100 nm square pillars were fabricated. The photoluminescence of the pillars was measured using step-scan Fourier transform infrared spectroscopy and the laser for optically pumping was 532 nm wavelength. The laser was modulated by a mechanical chopper at 1 kHz and with a duty cycle of 50 %. The photoluminescence spectra revealed emission at wavelengths longer than 2.2 μm indicating tensile strained Ge. The next stage will be to measure the amount of tensile strain in the pillars by Raman microscopy and compare this to finite element modelling that will in the future allow the optimization of the geometries of the Ge nanostructures. Ideally, future structures should be cavity type structures for lasing such as a ridge waveguides, microdisks, and ring resonators.

Another approach to an efficient light emitter on Si is through Ge quantum wells. Quantum wells are regularly used in III-Vs to achieve population inversion more easily compared to bulk devices due to the favourable density of states that arises from the quantization. In addition, another benefit is the reduction of Auger recombination that is likely to be a dominate non-radiative scattering mechanism in Ge due to its small bandgap. Another benefit is the type 1 alignment that occurs for Ge quantum wells sandwiched between SiGe barriers with a Ge concentration of greater than 80 %. This is in stark contrast than the type 2 alignment that occurs for Si/Ge/Si double heterostructure, where only holes would be confined. Overcoming the modal overlap problem can be solved by moving to a multi quantum well structure. There has not been much research into the light emission of Ge quantum wells. There has only been a handful of results with a single result of electroluminescence below 1.45 μm wavelength published. The structure is based on a 10 quantum well design that couples to form a miniband. The idea is that there is a larger discontinuity provided by the Γ-band compared to the L-band. The material was grown by collaborators in Como by low power plasma enhanced chemical vapour deposition. X-ray diffraction analysis reveals the n-Ge quantum wells have 0.15 % tensile strain. Due to selection rules, surface normal geometry mesa devices were investigated. LED devices similar to the bulk n-Ge were fabricated and sizes ranged from 25 to 500 μm. FTIR PL and EL characterization revealed two peaks at 1.55 and 1.8 μm corresponding to the Gamma to HH and L to HH. The devices show better performance at higher temperature and this is from more carriers been thermally excited into the Gamma for efficient direct recombination. Electroluminescence at 1.55 μm represents the first time emission at the important telecommunications low loss window.

Finally, Ge-on-Si single photon avalanche detectors (SPADs) were fabricated and characterised. Commercially available SPADs based on InGaAs suffer from serious after pulsing that limits the gating frequency. Ideally, for most applications require free running SPADs. Ge has an absorption coefficient that is comparable to InGaAs at 1.55 μm wavelength and the large bandgap of Si should provide a high quality multiplication region with very little impurities, which should lead to lower dark currents and less afterpulsing. Collaborators at Herriot Watt University designed the separate absorption, charge sheet, and multiplication (SACM)

structure. The charge sheet region controls the electric field within the Ge and Si. Require a field that will cause any generated electrons in the Ge to drift to the Si multiplication region to undergo impact ionization where one carrier frees another carrier and so on until a current pulse is easily detectable. The SPAD structure was grown by collaborators at Warwick University, the first set of mesa devices fabricated did not breakdown at the modelled voltage. When characterised under illumination at 1310 nm wavelength they showed no photocurrent. The material was sent for secondary ion mass spectrometry analysis and it revealed that the charge sheet doping concentration was two orders of magnitude higher than designed. After growth optimization by Warwick a second generation of wafers were grown. Fabrication was repeated and under illumination the devices showed photocurrent. The SPADs were then sent to Herriot Watt for single photon characterization. A single photon detection efficiency of 4 % and dark count rate (DCR) of 10^6 was calculated. The DCR is considerable, however these devices suffer from the deleterious effect of surface states since they are not planar. The after-pulsing does not seem to increase dramatically with frequency, which might be an advantage over InGaAs, which has to be gated below 100 KHz.

Bibliography

1. Moore, G.E., *Cramming more components onto integrated circuits (Reprinted from Electronics, pg 114-117, April 19, 1965)*. Proceedings of the Ieee, 1998. **86**(1): p. 82-85.
2. IRC, *INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS*. 2012.
3. IRC, *INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS 2007 EDITION INTERCONNECT*. 2007.
4. Jalali, B., *Can silicon change photonics?* Physica Status Solidi a-Applications and Materials Science, 2008. **205**(2): p. 213-224.
5. Miller, D.A.B., *Optical interconnects to silicon*. Ieee Journal of Selected Topics in Quantum Electronics, 2000. **6**(6): p. 1312-1317.
6. Paul, D.J., *Silicon photonics: a bright future?* Electronics Letters, 2009. **45**(12): p. 582-U3.
7. Chen, X., C. Li, and H.K. Tsang, *Device engineering for silicon photonics*. Npg Asia Materials, 2011. **3**(1): p. 34-40.
8. Paul, D.J., *Silicon-germanium strained layer materials in microelectronics*. Advanced Materials, 1999. **11**(3): p. 191-+.
9. Jalali, B. and S. Fathpour, *Silicon photonics*. Journal of Lightwave Technology, 2006. **24**(12): p. 4600-4615.
10. Soref, R.A. and B.R. Bennett, *ELECTROOPTICAL EFFECTS IN SILICON*. Ieee Journal of Quantum Electronics, 1987. **23**(1): p. 123-129.
11. Soref, R.A., *SILICON-BASED OPTOELECTRONICS*. Proceedings of the Ieee, 1993. **81**(12): p. 1687-1706.
12. *Luxtera*.
13. Kotura.
14. Won, R. and M. Paniccia, *Integrating silicon photonics*. Nature Photonics, 2010. **4**(8): p. 498-499.
15. Fang, A.W., et al., *Electrically pumped hybrid AlGaInAs-silicon evanescent laser*. Optics Express, 2006. **14**(20): p. 9203-9210.
16. Van Campenhout, J., et al., *Electrically pumped InP-based microdisk lasers integrated with a nanophotonic silicon-on-insulator waveguide circuit*. Optics Express, 2007. **15**(11): p. 6744-6749.
17. Xu, Q.F., et al., *Micrometre-scale silicon electro-optic modulator*. Nature, 2005. **435**(7040): p. 325-327.
18. Green, W.M.J., et al., *Ultra-compact, low RF power, 10 gb/s silicon Mach-Zehnder modulator*. Optics Express, 2007. **15**(25): p. 17106-17113.
19. Thomson, D.J., et al., *High contrast 40Gbit/s optical modulation in silicon*. Optics Express, 2011. **19**(12): p. 11507-11516.
20. Marris-Morini, D., et al., *Low loss and high speed silicon optical modulator based on a lateral carrier depletion structure*. Optics Express, 2008. **16**(1): p. 334-339.
21. Yin, T., et al., *31GHz Ge n-i-p waveguide photodetectors on Silicon-on-Insulator substrate*. Optics Express, 2007. **15**(21): p. 13965-13971.
22. Vivien, L., et al., *42 GHz p.i.n Germanium photodetector integrated in a silicon-on-insulator waveguide*. Optics Express, 2009. **17**(8): p. 6252-6257.

23. Duan, N., et al., *310 GHz gain-bandwidth product Ge/Si avalanche photodetector for 1550 nm light detection.* Optics Express, 2012. **20**(10): p. 11031-11036.
24. Rong, H.S., et al., *A continuous-wave Raman silicon laser*. Nature, 2005. **433**(7027): p. 725-728.
25. Rong, H.S., et al., *An all-silicon Raman laser*. Nature, 2005. **433**(7023): p. 292-294.
26. Huda, M.Q. and S. Subrina, *Multiple excitation of silicon nanoclusters during erbium sensitization process in silicon rich oxide host*. Applied Physics Letters, 2011. **98**(11).
27. Soref, R., *The past, present, and future of silicon photonics.* Ieee Journal of Selected Topics in Quantum Electronics, 2006. **12**(6): p. 1678-1687.
28. Han, H.S., S.Y. Seo, and J.H. Shin, *Optical gain at 1.54 mu m in erbium-doped silicon nanocluster sensitized waveguide.* Applied Physics Letters, 2001. **79**(27): p. 4568-4570.
29. Polman, A., et al., *Ultralow-threshold erbium-implanted toroidal microlaser on silicon.* Applied Physics Letters, 2004. **84**(7): p. 1037-1039.
30. Nazarov, A., et al., *Light emission and charge trapping in Er-doped silicon dioxide films containing silicon nanocrystals.* Applied Physics Letters, 2005. **86**(15).
31. Groenert, M.E., et al., *Monolithic integration of room-temperature cw GaAs/AlGaAs lasers on Si substrates via relaxed graded GeSi buffer layers.* Journal of Applied Physics, 2003. **93**(1): p. 362-367.
32. Liu, J.F., et al., *Ge-on-Si laser operating at room temperature*. Optics Letters, 2010. **35**(5): p. 679-681.
33. Camacho-Aguilera, R.E., et al., *An electrically pumped germanium laser.* Optics Express, 2012. **20**(10): p. 11316-11320.
34. Paul, D.J., *Si/SiGe heterostructures: from material and physics to devices and circuits.* Semiconductor Science and Technology, 2004. **19**(10): p. R75-R108.
35. Arden, W.B., M; Cogez, P; Graef, M; Huizing, B; Mahnkopf, R, *"More-than-Moore"*. ITRS, 2012.
36. Kasper, E., H.J. Herzog, and H. Kibbel, *ONE-DIMENSIONAL SIGE SUPERLATTICE GROWN BY UHV EPITAXY.* Applied Physics, 1975. **8**(3): p. 199-205.
37. Pidduck, A.J., et al., *EVOLUTION OF SURFACE-MORPHOLOGY AND STRAIN DURING SIGE EPITAXY.* Thin Solid Films, 1992. **222**(1-2): p. 78-84.
38. Srinivasan, G.R., *KINETICS OF LATERAL AUTO-DOPING IN SILICON EPITAXY.* Journal of the Electrochemical Society, 1978. **125**(1): p. 146-151.
39. Hartmann, J.M., et al., *Reduced pressure-chemical vapor deposition of Ge thick layers on Si(001) for 1.3-1.55-mu m photodetection.* Journal of Applied Physics, 2004. **95**(10): p. 5905-5913.
40. Hartmann, J.M., et al., *Reduced pressure-chemical vapor deposition of intrinsic and doped Ge layers on Si(001) for microelectronics and optoelectronics purposes.* Journal of Crystal Growth, 2005. **274**(1-2): p. 90-99.
41. Isella, G., et al., *Low-energy plasma-enhanced chemical vapor deposition for strained Si and Ge heterostructures and devices.* Solid-State Electronics, 2004. **48**(8): p. 1317-1323.

42. Currie, M.T., et al., *Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing*. Applied Physics Letters, 1998. **72**(14): p. 1718-1720.
43. Luan, H.C., et al., *High-quality Ge epilayers on Si with low threading-dislocation densities*. Applied Physics Letters, 1999. **75**(19): p. 2909-2911.
44. Shah, V.A., et al., *High quality relaxed Ge layers grown directly on a Si(001) substrate*. Solid-State Electronics, 2011. **62**(1): p. 189-194.
45. Onsia, B., et al., *A study of the influence of typical wet chemical treatments on the germanium wafer surface*, in *Ultra Clean Processing of Silicon Surfaces Vii*, P. Mertens, M. Meuris, and M. Heyns, Editors. 2005, Trans Tech Publications Ltd: Zurich-Uetikon. p. 27-30.
46. Brunco, D.P., et al., *Germanium MOSFET devices: Advances in materials understanding, process development, and electrical performance*. Journal of the Electrochemical Society, 2008. **155**(7): p. H552-H561.
47. Chou, S.Y., et al., *Sub-10 nm imprint lithography and applications*. Journal of Vacuum Science & Technology B, 1997. **15**(6): p. 2897-2904.
48. Vieu, C., et al., *Electron beam lithography: resolution limits and applications*. Applied Surface Science, 2000. **164**: p. 111-117.
49. Gwyn, C.W., et al., *Extreme ultraviolet lithography*. Journal of Vacuum Science & Technology B, 1998. **16**(6): p. 3142-3149.
50. Silverman, J.P., *X-ray lithography: Status, challenges, and outlook for 0.13 mu m*. Journal of Vacuum Science & Technology B, 1997. **15**(6): p. 2117-2124.
51. Mirza, M.M., et al., *Nanofabrication of high aspect ratio (similar to 50:1) sub-10nm silicon nanowires using inductively coupled plasma etching*. Journal of Vacuum Science & Technology B, 2012. **30**(6).
52. Thoms, S. and D.S. Macintyre, *Linewidth metrology for sub-10-nm lithography*. Journal of Vacuum Science & Technology B, 2010. **28**(6): p. C6H6-C6H10.
53. Cumming, D.R.S., et al., *Fabrication of 3 nm wires using 100 keV electron beam lithography and poly(methyl methacrylate) resist*. Applied Physics Letters, 1996. **68**(3): p. 322-324.
54. Hoshi, Y., et al., *Formation of Tensilely Strained Germanium-on-Insulator*. Applied Physics Express, 2012. **5**(1).
55. Hu, W.X., et al., *Room-temperature direct-bandgap photoluminescence from strain-compensated Ge/SiGe multiple quantum wells on silicon*. Chinese Physics B, 2012. **21**(1).
56. *MA6 user manual*.
57. Oehme, M., et al., *Room-Temperature Electroluminescence From GeSn Light-Emitting Pin Diodes on Si*. Ieee Photonics Technology Letters, 2011. **23**(23): p. 1751-1753.
58. *Vistec Semiconductor Systems (2009). Vectorbeam Series Operation Manual*.
59. Williams, K.R. and R.S. Muller, *Etch rates for micromachining processing*. Journal of Microelectromechanical Systems, 1996. **5**(4): p. 256-269.
60. Williams, K.R., K. Gupta, and M. Wasilik, *Etch rates for micromachining processing - Part II*. Journal of Microelectromechanical Systems, 2003. **12**(6): p. 761-778.

61. Chang, C.L., et al., *Etching submicrometer trenches by using the Bosch process and its application to the fabrication of antireflection structures.* Journal of Micromechanics and Microengineering, 2005. **15**(3): p. 580-585.
62. Pillarisetty, R., *Academic and industry research progress in germanium nanodevices.* Nature, 2011. **479**(7373): p. 324-328.
63. Shen, C., et al., *Spin transport in germanium at room temperature.* Applied Physics Letters, 2010. **97**(16).
64. Shang, H.L., et al., *High mobility p-channel germanium MOSFETs with a thin Ge oxynitride gate dielectric*. International Electron Devices 2002 Meeting, Technical Digest. 2002, New York: Ieee. 441-444.
65. Dimoulas, A., et al., *Fermi-level pinning and charge neutrality level in germanium.* Applied Physics Letters, 2006. **89**(25).
66. Lieten, R.R., et al., *Ohmic contact formation on n-type Ge.* Applied Physics Letters, 2008. **92**(2).
67. Bardeen, J., *SURFACE STATES AND RECTIFICATION AT A METAL SEMI-CONDUCTOR CONTACT*. Physical Review, 1947. **71**(10): p. 717-727.
68. Nishimura, T., K. Kita, and A. Toriumi, *Evidence for strong Fermi-level pinning due to metal-induced gap states at metal/germanium interface.* Applied Physics Letters, 2007. **91**(12).
69. Wager, J.F. and J. Robertson, *Metal-induced gap states modeling of metal-Ge contacts with and without a silicon nitride ultrathin interfacial layer.* Journal of Applied Physics, 2011. **109**(9).
70. Lin, L., J. Robertson, and S.J. Clark, *Shifting Schottky barrier heights with ultra-thin dielectric layers.* Microelectronic Engineering, 2011. **88**(7): p. 1461-1463.
71. Roy, A.M., J.Y.J. Lin, and K.C. Saraswat, *Specific Contact Resistivity of Tunnel Barrier Contacts Used for Fermi Level Depinning.* Ieee Electron Device Letters, 2010. **31**(10): p. 1077-1079.
72. Kobayashi, M., et al., *Fermi level depinning in metal/Ge Schottky junction for metal source/drain Ge metal-oxide-semiconductor field-effect-transistor application.* Journal of Applied Physics, 2009. **105**(2).
73. Martens, K., et al., *Contact resistivity and Fermi-level pinning in n-type Ge contacts with epitaxial Si-passivation.* Applied Physics Letters, 2011. **98**(1).
74. Maeda, T., et al., *Sulfur passivation of Ge (001) surfaces and its effects on Schottky barrier contact.* Materials Science in Semiconductor Processing, 2006. **9**(4-5): p. 706-710.
75. Yamane, K., et al., *Effect of atomically controlled interfaces on Fermi-level pinning at metal/Ge interfaces.* Applied Physics Letters, 2010. **96**(16).
76. Thathachary, A.V., et al., *Fermi level depinning at the germanium Schottky interface through sulfur passivation.* Applied Physics Letters, 2010. **96**(15).
77. Zhou, Y., et al., *Investigating the origin of Fermi level pinning in Ge Schottky junctions using epitaxially grown ultrathin MgO films.* Applied Physics Letters, 2010. **96**(10).
78. Ikeda, K., et al., *Modulation of NiGe/Ge Schottky barrier height by sulfur segregation during Ni germanidation.* Applied Physics Letters, 2006. **88**(15).
79. *Physics of semiconductor devices.*

80. Hutin, L., et al., *Schottky Barrier Height Extraction in Ohmic Regime: Contacts on Fully Processed GeOI Substrates*. Journal of the Electrochemical Society, 2009. **156**(7): p. H522-H527.
81. Satta, A., et al., *P implantation doping of Ge: Diffusion, activation, and recrystallization*. Journal of Vacuum Science & Technology B, 2006. **24**(1): p. 494-498.
82. Simoen, E., et al., *Ion-implantation issues in the formation of shallow junctions in germanium*. Materials Science in Semiconductor Processing, 2006. **9**(4-5): p. 634-639.
83. Satta, A., et al., *Diffusion, activation, and regrowth behavior of high dose P implants in Ge*. Applied Physics Letters, 2006. **88**(16).
84. Benourhazi, K. and J.P. Ponpon, *IMPLANTATION OF PHOSPHORUS AND ARSENIC IONS IN GERMANIUM*. Nuclear Instruments & Methods in Physics Research Section B-Beam Interactions with Materials and Atoms, 1992. **71**(4): p. 406-411.
85. Cuttriss, D.B., *RELATION BETWEEN SURFACE CONCENTRATION AND AVERAGE CONDUCTIVITY IN DIFFUSED LAYERS IN GERMANIUM*. Bell System Technical Journal, 1961. **40**(2): p. 509-+.
86. Gaudet, S., et al., *Thin film reaction of transition metals with germanium*. Journal of Vacuum Science & Technology A, 2006. **24**(3): p. 474-485.
87. Brunco, D.P., et al., *Observation and suppression of nickel germanide overgrowth on germanium substrates with patterned SiO2 structures*. Electrochemical and Solid State Letters, 2008. **11**(2): p. H39-H41.
88. Zhu, S.Y., et al., *Temperature dependence of Ni-germanide formed by Ni-Ge solid-state reaction*. Fifth International Workshop on Junction Technology. 2005. 85-88.
89. Loh, W.M., et al., *AN ACCURATE METHOD TO EXTRACT SPECIFIC CONTACT RESISTIVITY USING CROSS-BRIDGE KELVIN RESISTORS*. Ieee Electron Device Letters, 1985. **6**(9): p. 441-443.
90. Ono, M., A. Nishiyama, and A. Toriumi, *A simple approach to understanding measurement errors in the cross-bridge Kelvin resistor and a new pattern for measurements of specific contact resistivity*. Solid-State Electronics, 2002. **46**(9): p. 1325-1331.
91. SCHRODER, D.K., *SEMICONDUCTOR MATERIAL AND DEVICE CHARACTERIZATION*. 2006.
92. Marlow, G.S. and M.B. Das, *THE EFFECTS OF CONTACT SIZE AND NON-ZERO METAL RESISTANCE ON THE DETERMINATION OF SPECIFIC CONTACT RESISTANCE*. Solid-State Electronics, 1982. **25**(2): p. 91-94.
93. Klootwijk, J.H., C.E. Timmering, and ieee, *Merits and Limitations of Circular TLM structures for contact resistance determination for novel III-VHBTs*. Icmts 2004: Proceedings of the 2004 International Conference on Microelectronic Test Structures. 2004, New York: Ieee. 247-252.
94. Gallacher, K., et al., *Ohmic contacts to n-type germanium with low specific contact resistivity*. Applied Physics Letters, 2012. **100**(2).
95. Massalski, T.B., *Binary Alloy Phase Diagram*. 1986: ASM INTERNATIONAL.
96. Liu, Y.Q., D.J. Ma, and Y. Du, *Thermodynamic modeling of the germanium-nickel system*. Journal of Alloys and Compounds, 2010. **491**(1-2): p. 63-71.
97. Nemouchi, F., et al., *Simultaneous growth of Ni5Ge3 and NiGe by reaction of Ni film with Ge*. Applied Physics Letters, 2006. **89**(13).

98. Nemouchi, F., et al., *A comparative study of nickel silicides and nickel germanides: Phase formation and kinetics*. Microelectronic Engineering, 2006. **83**(11-12): p. 2101-2106.
99. Pfisterer, H. and K. Schubert, **NEUE PHASEN VOM MNP(B31)-TYP*. Zeitschrift Fur Metallkunde, 1950. **41**(10): p. 358-367.
100. HABANYAMA, A., C.M. COMRIE, and K.J. PONDO, *IN SITU REAL-TIME RUTHERFORD BACKSCATTERING SPECTROMETRY STUDY OF NICKEL/GERMANIUM INTERACTION*. 2011. 2011.
101. Martens, K., et al., *Record low contact resistivity to n-type Ge for CMOS and Memory Applications*, in *2010 International Electron Devices Meeting - Technical Digest*. 2010, Ieee: New York.
102. Oh, J., et al., *Mechanisms for Low On-State Current of Ge (Si Ge) nMOSFETs: A Comparative Study on Gate Stack, Resistance, and Orientation-Dependent Effective Masses*. 2009 Symposium on Vlsi Technology, Digest of Technical Papers. 2009, Tokyo: Japan Society Applied Physics. 238-239.
103. Thareja, G., et al., *Electrical Characteristics of Germanium n(+)/p Junctions Obtained Using Rapid Thermal Annealing of Coimplanted P and Sb*. Ieee Electron Device Letters, 2011. **32**(5): p. 608-610.
104. Bin, Y., et al. *Low-Contact-Resistivity Nickel Germanide Contacts on n+Ge with Phosphorus/Antimony Co-Doping and Schottky Barrier Height Lowering*. in *Silicon-Germanium Technology and Device Meeting (ISTDM), 2012 International*. 2012.
105. Thareja, G., et al., *High Performance Germanium N-MOSFET with Antimony Dopant Activation Beyond 1x10(20) cm(-3)*. 2010 International Electron Devices Meeting - Technical Digest. 2010.
106. Firrincieli, A., et al., *Study of ohmic contacts to n-type Ge: Snowplow and laser activation*. Applied Physics Letters, 2011. **99**(24).
107. Shayesteh, M., et al., *Atomically Flat Low-Resistive Germanide Contacts Formed by Laser Thermal Anneal*. Electron Devices, IEEE Transactions on, 2013. **60**(7): p. 2178-2185.
108. Lin, J.Y.J., A.M. Roy, and K.C. Saraswat, *Reduction in Specific Contact Resistivity to n(+) Ge Using TiO2 Interfacial Layer*. Ieee Electron Device Letters, 2012. **33**(11): p. 1541-1543.
109. Manik, P.P., et al., *Fermi-level unpinning and low resistivity in contacts to n-type Ge with a thin ZnO interfacial layer*. Applied Physics Letters, 2012. **101**(18).
110. Gallacher, K.F., et al., *Low Specific Ohmic Contacts to n-type Germanium Using a Low Temperature NiGe Process*. Meeting Abstracts, 2012(43): p. 3242-3242.
111. Markevich, V.P., et al., *Vacancy-group-V-impurity atom pairs in Ge crystals doped with P, As, Sb, and Bi*. Physical Review B, 2004. **70**(23).
112. Mueller, M., et al., *Schottky-barrier height tuning of NiGe/n-Ge contacts using As and P segregation*. Materials Science and Engineering B-Advanced Functional Solid-State Materials, 2008. **154**: p. 168-171.
113. Jackson, M., M.G. Sowa, and H.H. Mantsch, *Infrared spectroscopy: a new frontier in medicine*. Biophysical Chemistry, 1997. **68**(1-3): p. 109-125.

114. Rothman, L.S., et al., *The HITRAN 2008 molecular spectroscopic database*. Journal of Quantitative Spectroscopy & Radiative Transfer, 2009. **110**(9-10): p. 533-572.
115. Nam, D., et al., *Electroluminescence from strained germanium membranes and implications for an efficient Si-compatible laser*. Applied Physics Letters, 2012. **100**(13).
116. Sanchez-Perez, J.R., et al., *Direct-bandgap light-emitting germanium in tensilely strained nanomembranes*. Proceedings of the National Academy of Sciences of the United States of America, 2011. **108**(47): p. 18893-18898.
117. Thompson, S.E., et al., *Uniaxial-process-induced strained-Si: Extending the CMOS roadmap*. Ieee Transactions on Electron Devices, 2006. **53**(5): p. 1010-1020.
118. Sun, X.C., et al., *Room-temperature direct bandgap electroluminesence from Ge-on-Si light-emitting diodes*. Optics Letters, 2009. **34**(8): p. 1198-1200.
119. Cardona, M. and F.H. Pollak, *ENERGY-BAND STRUCTURE OF GERMANIUM AND SILICON - K.P METHOD*. Physical Review, 1966. **142**(2): p. 530-&.
120. Sun, X.C., et al., *Toward a Germanium Laser for Integrated Silicon Photonics*. Ieee Journal of Selected Topics in Quantum Electronics, 2010. **16**(1): p. 124-131.
121. Vandewalle, C.G., *BAND LINEUPS AND DEFORMATION POTENTIALS IN THE MODEL-SOLID THEORY*. Physical Review B, 1989. **39**(3): p. 1871-1883.
122. Pollak, F.H. and M. Cardona, *PIEZO-ELECTROREFLECTANCE IN GE GAAS AND SI*. Physical Review, 1968. **172**(3): p. 816-&.
123. Kleiner, W.H. and L.M. Roth, *DEFORMATION POTENTIAL IN GERMANIUM FROM OPTICAL ABSORPTION LINES FOR EXCITON FORMATION*. Physical Review Letters, 1959. **2**(8): p. 334-336.
124. Vandewalle, C.G. and R.M. Martin, *THEORETICAL CALCULATIONS OF HETEROJUNCTION DISCONTINUITIES IN THE SI/GE SYSTEM*. Physical Review B, 1986. **34**(8): p. 5621-5634.
125. Fischetti, M.V. and S.E. Laux, *Band structure, deformation potentals, and carrier mobility in strained Si, Ge, and SiGe alloys*. Journal of Applied Physics, 1996. **80**(4): p. 2234-2252.
126. Liu, J.F., et al., *Deformation potential constants of biaxially tensile stressed Ge epitaxial films on Si(100)*. Physical Review B, 2004. **70**(15).
127. Menendez, J. and J. Kouvetakis, *Type-I Ge/Ge1-x-ySixSny strained-layer heterostructures with a direct Ge bandgap*. Applied Physics Letters, 2004. **85**(7): p. 1175-1177.
128. Paul, D.J., *8-band k.p modeling of the quantum confined Stark effect in Ge quantum wells on Si substrates*. Physical Review B, 2008. **77**(15).
129. El Kurdi, M., et al., *Band structure and optical gain of tensile-strained germanium based on a 30 band k center dot p formalism*. Journal of Applied Physics, 2010. **107**(1).
130. Camacho-Aguilera, R.E., et al., *High active carrier concentration in n-type, thin film Ge using delta-doping*. Optical Materials Express, 2012. **2**(11): p. 1462-1469.
131. Huo, Y.J., et al., *Strong enhancement of direct transition photoluminescence with highly tensile-strained Ge grown by molecular beam epitaxy*. Applied Physics Letters, 2011. **98**(1).

132. El Kurdi, M., et al., *Control of direct band gap emission of bulk germanium by mechanical tensile strain*. Applied Physics Letters, 2010. **96**(4).
133. Stoney, G.G., *The tension of metallic films deposited by electrolysis*. Proceedings of the Royal Society of London Series a-Containing Papers of a Mathematical and Physical Character, 1909. **82**(553): p. 172-175.
134. Peng, C.Y., et al., *Micro-Raman Studies on Nickel Germanides formed on (110) crystalline Ge*, in *Sige, Ge, and Related Compounds 3: Materials, Processing, and Devices*, D. Harame, et al., Editors. 2008. p. 249-253.
135. Iga, K., F. Koyama, and S. Kinoshita, *SURFACE EMITTING SEMICONDUCTOR-LASERS*. Ieee Journal of Quantum Electronics, 1988. **24**(9): p. 1845-1855.
136. Nakamura, S., et al., *InGaN-based multi-quantum-well-structure laser diodes*. Japanese Journal of Applied Physics Part 2-Letters, 1996. **35**(1B): p. L74-L76.
137. Levine, B.F., *QUANTUM-WELL INFRARED PHOTODETECTORS*. Journal of Applied Physics, 1993. **74**(8): p. R1-R81.
138. Coldren, L.A., S.W. Corzine, and M.L. Mashanovitch, *Diode Lasers and Photonic Integrated Circuits*. 2011: Wiley.
139. Virgilio, M. and G. Grosso, *Type-I alignment and direct fundamental gap in SiGe based heterostructures*. Journal of Physics-Condensed Matter, 2006. **18**(3): p. 1021-1031.
140. Sun, G., R.A. Soref, and H.H. Cheng, *Design of a Si-based lattice-matched room-temperature GeSn/GeSiSn multi-quantum-well mid-infrared laser diode*. Optics Express, 2010. **18**(19): p. 19957-19965.
141. Lever, L., et al., *Optical absorption in highly strained Ge/SiGe quantum wells: The role of Gamma ->Delta scattering*. Journal of Applied Physics, 2012. **112**(12).
142. Kuo, Y.H., et al., *Strong quantum-confined Stark effect in germanium quantum-well structures on silicon*. Nature, 2005. **437**(7063): p. 1334-1336.
143. Chaisakul, P., et al., *Quantum-confined Stark effect measurements in Ge/SiGe quantum-well structures*. Optics Letters, 2010. **35**(17): p. 2913-2915.
144. Fidaner, O., et al., *Ge-SiGe quantum-well waveguide photodetectors on silicon for the near-infrared*. Ieee Photonics Technology Letters, 2007. **19**(17-20): p. 1631-1633.
145. Chaisakul, P., et al., *Ge/SiGe multiple quantum well photodiode with 30 GHz bandwidth*. Applied Physics Letters, 2011. **98**(13).
146. Chaisakul, P., et al., *10-Gb/s Ge/SiGe Multiple Quantum-Well Waveguide Photodetector*. Ieee Photonics Technology Letters, 2011. **23**(20): p. 1430-1432.
147. Bonfanti, M., et al., *Direct gap related optical transitions in Ge/SiGe quantum wells*. Physica E-Low-Dimensional Systems & Nanostructures, 2009. **41**(6): p. 972-975.
148. Chen, Y.H., et al., *Room temperature photoluminescence of tensile-strained Ge/Si0.13Ge0.87 quantum wells grown on silicon-based germanium virtual substrate*. Applied Physics Letters, 2009. **94**(14).
149. Chen, Y.H., et al., *Quantum-confined direct band transitions in tensile strained Ge/SiGe quantum wells on silicon substrates*. Nanotechnology, 2010. **21**(11).

150. Carroll, L., et al., *Quantum-confined direct-gap transitions in tensile-strained Ge/SiGe multiple quantum wells*. Applied Physics Letters, 2011. **99**(3).
151. Chaisakul, P., et al., *Room temperature direct gap electroluminescence from Ge/Si0.15Ge0.85 multiple quantum well waveguide*. Applied Physics Letters, 2011. **99**(14).
152. Harrison, P., *Quantum Wells, Wires and Dots: Theoretical and Computational Physics of Semiconductor Nanostructures*. 2005: Wiley.
153. Suet, Z., et al., *Si/SiGe n-type resonant tunneling diodes fabricated using in situ hydrogen cleaning*. Applied Physics Letters, 2007. **90**(20).
154. Paul, D.J., *The progress towards terahertz quantum cascade lasers on silicon substrates*. Laser & Photonics Reviews, 2010. **4**(5): p. 610-632.
155. Osmond, J., et al., *Ultralow dark current Ge/Si(100) photodiodes with low thermal budget*. Applied Physics Letters, 2009. **94**(20).
156. Cheng, S.-L., et al., *Room temperature 1.6 microm electroluminescence from Ge light emitting diode on Si substrate*. Optics express, 2009. **17**(12): p. 10019-24.
157. Wu, P.H., et al., *Above-room-temperature photoluminescence from a strain-compensated Ge/Si0.15Ge0.85 multiple-quantum-well structure*. Applied Physics Letters, 2012. **100**(14).
158. Varshni, Y.P., *Temperature dependence of the energy gap in semiconductors*. Physica, 1967. **34**(1): p. 149-154.
159. Liu, J.F., et al., *Direct-gap optical gain of Ge on Si at room temperature*. Optics Letters, 2009. **34**(11): p. 1738-1740.
160. Takesue, H., et al., *Quantum key distribution over a 40-dB channel loss using superconducting single-photon detectors*. Nature Photonics, 2007. **1**(6): p. 343-348.
161. Warburton, R.E., et al., *Enhanced performance photon-counting time-of-flight sensor*. Optics Express, 2007. **15**(2): p. 423-429.
162. Sakaizawa, D., et al., *Development of a 1.6 mu m differential absorption lidar with a quasi-phase-matching optical parametric oscillator and photon-counting detector for the vertical CO(2) profile*. Applied Optics, 2009. **48**(4): p. 748-757.
163. Cova, S., et al., *Avalanche photodiodes and quenching circuits for single-photon detection*. Applied Optics, 1996. **35**(12): p. 1956-1976.
164. Pellegrini, S., et al., *Design and performance of an InGaAs-InP single-photon avalanche diode detector*. Ieee Journal of Quantum Electronics, 2006. **42**(3-4): p. 397-403.
165. Yan, Z.Z., et al., *An ultra low noise telecom wavelength free running single photon detector using negative feedback avalanche diode*. Review of Scientific Instruments, 2012. **83**(7).
166. Yuan, Z.L., et al., *High speed single photon detection in the near infrared*. Applied Physics Letters, 2007. **91**(4).
167. Namekata, N., S. Adachi, and S. Inoue, *1.5 GHz single-photon detection at telecommunication wavelengths using sinusoidally gated InGaAs/InP avalanche photodiode*. Optics Express, 2009. **17**(8): p. 6275-6282.
168. Warburton, R.E., M.A. Itzler, and G.S. Buller, *Improved free-running InGaAs/InP single-photon avalanche diode detectors operating at room temperature*. Electronics Letters, 2009. **45**(19): p. 996-U56.

169. Dash, W.C. and R. Newman, *INTRINSIC OPTICAL ABSORPTION IN SINGLE-CRYSTAL GERMANIUM AND SILICON AT 77-DEGREES-K AND 300-DEGREES-K*. Physical Review, 1955. **99**(4): p. 1151-1155.
170. Palik, E.D., *Handbook of Optical Constants of Solids*, Elsevier.
171. Doylend, J.K. and A.P. Knights, *Design and simulation of an integrated fiber-to-chip coupler for silicon-on-insulator waveguides*. Ieee Journal of Selected Topics in Quantum Electronics, 2006. **12**(6): p. 1363-1370.
172. Kang, Y., et al., *Epitaxially-grown Ge/Si avalanche photodiodes for 1.3 mu m light detection*. Optics express, 2008. **16**(13): p. 9365-9371.
173. Kang, Y.M., et al., *Monolithic germanium/silicon avalanche photodiodes with 340 GHz gain-bandwidth product*. Nature Photonics, 2009. **3**(1): p. 59-63.
174. Kang, Y., et al., *High Performance Ge/Si Avalanche Photodiodes Development in Intel*. 2011 Optical Fiber Communication Conference and Exposition. 2011, Washington: Optical Soc America.
175. Osmond, J., et al., *Ge-on-silicon vertical PIN photodetectors*, in *Silicon Photonics Iv*, J.A. Kubby and G.T. Reed, Editors. 2009, Spie-Int Soc Optical Engineering: Bellingham.
176. Ang, K.W., et al., *Novel NiGe MSM photodetector featuring asymmetrical Schottky barriers using sulfur co-implantation and segregation*. Ieee Electron Device Letters, 2008. **29**(7): p. 708-710.
177. Zhiwen, L., et al., *Geiger-Mode Operation of Ge-on-Si Avalanche Photodiodes*. Quantum Electronics, IEEE Journal of, 2011. **47**(5): p. 731-735.
178. Aminian, M., et al., *A Ge-on-Si Single Photon Avalanche Diode Operating in Geiger Mode at Infrared Wavelengths*, in *Advanced Photon Counting Techniques Vi*, M.A. Itzler and J.C. Campbell, Editors. 2012, Spie-Int Soc Optical Engineering: Bellingham.
179. Kittl, J.A., et al., *Silicides for 65 nm CMOS and beyond*, in *Comos Front-End Materials and Process Technology*, T.J. King, et al., Editors. 2003, Materials Research Society: Warrendale. p. 267-278.
180. Becker, W., *The bh TCSPC Handbook*. 2010.
181. Loudon, A.Y., et al., *Enhancement of the infrared detection efficiency of silicon photon-counting avalanche photodiodes by use of silicon germanium absorbing layers*. Opt. Lett., 2002. **27**(4): p. 219-221.
182. Tosi, A., et al., *Germanium and InGaAs/InP SPADs for single-photon detection in the near-infrared*, in *Advanced Photon Counting Techniques Ii*, W. Becker, Editor. 2007, Spie-Int Soc Optical Engineering: Bellingham.
183. Lu, Z.W., et al., *Ge on Si and InP/InGaAs Single Photon Avalanche Diodes*, in *Infrared Sensors, Devices, and Applications and Single Photon Imaging Ii*, D. LeVanPaul, et al., Editors. 2011, Spie-Int Soc Optical Engineering: Bellingham.
184. DiLello, N.A., D.K. Johnstone, and J.L. Hoyt, *Characterization of dark current in Ge-on-Si photodiodes*. Journal of Applied Physics, 2012. **112**(5).