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University
of Glasgow

Remotely Interrogated MEMS pressure sensor

A dissertation submitted to the School of Engineering

University of Glasgow

In fulfilment of the requirements for the degree of

Doctor of Philosophy

By

Amr Ibrahim

December 2011

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Abstract

This thesis considers the design and implementation of passive wireless microwave readable pressure sensors on a single chip. Two novel-all passive devices are considered for wireless pressure operation.

The first device consists of a tuned circuit operating at 10 GHz fabricated on SiO₂ membrane, supported on a silicon wafer. A pressure difference across the membrane causes it to deflect so that a passive resonant circuit detunes. The circuit is remotely interrogated to read off the sensor data. The chip area is 20 mm² and the membrane area is 2mm² with thickness of 4 μm. Two on chip passive resonant circuits were investigated: a meandered dipole and a zigzag antenna. Both have a physical length of 4.25 mm. the sensors show a shift in their resonant frequency in response to changing pressure of 10.28-10.27 GHz for the meandered dipole, and 9.61-9.58 GHz for the zigzag antenna. The sensitivities of the meandered dipole and zigzag sensors are 12.5 kHz and 16 kHz mbar, respectively.

The second device is a pressure sensor on CMOS chip. The sensing element is capacitor array covering an area of 2 mm² on a membrane. This sensor is coupled with a dipole antenna operating at 8.77 GHz. The post processing of the CMOS chip is carried out only in three steps, and the sensor on its own shows a sensitivity of 0.47fF/mbar and wireless sensitivity of 27 kHz/mbar. The MIM capacitors on membrane can be used to detune the resonant frequency of an antenna.

Publications

Conference contributions

1. Amr Ibrahim; Cumming, D. R S, "**An X-band compact micromachined dipole antenna for remote sensing applications**," *Antennas and Propagation Conference (LAPC), 2010 Loughborough*, vol., no., pp.317, 320, 8-9 Nov. 2010.
2. Amr Ibrahim; Cumming, D. R S, "**A micromachined 10 GHz meander dipole antenna on high resistivity silicon substrate for remote sensing applications**," *Antennas & Propagation Conference, 2009. LAPC 2009. Loughborough*, vol., no., pp.345, 347, 16-17 Nov. 2009.

Journal article

- Amr Ibrahim, D.R.S. Cumming, "**Passive single chip wireless microwave pressure sensor**", *Sensors and Actuators A: Physical*, Volume 165, Issue 2, February 2011, Pages 200-206.

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Chapter 1

1. Introduction

This chapter illustrates the motivation for this research. The aim and main objectives are discussed and a summary of the thesis is given.

1.2 Background

Pressure sensors are widely used in many applications. For example in the automotive industry, measuring and monitoring the air inside a tire requires a wireless device to increase the portability or even to make the sensor implantable in tire layers. Also, pressure sensors play key part in controlling and monitoring great number of everyday applications ranging from physiological monitoring in medical technology, fluid flow and displacement in industrial uses, and in military applications. A pressure sensor uses a diaphragm that deflects in response to pressure change. Most pressure sensors record the pressure change by connecting the device to an electronic device, and an antenna in wireless applications to transmit or receive this information. The main types of pressure sensors are piezoresistive, capacitive, and inductive-capacitive whose detection relies on resonant frequency shift.

Generally, sensors are classified into two main operation categories: Active and passive sensors. In active sensors, the sensor is placed in close proximity to electronic circuitry which requires power to operate its parts, and therefore a battery is needed for its operation. In passive sensors, the main parts are limited to passive components such as capacitors and inductors without any power consumption. The read out circuit could be directly wired to the battery in the case of active sensors or wirelessly in both active and passive sensors.

Silicon based sensors have benefited from the rapid growth of the micro-electro-mechanical industry or MEMS technology. One particular criteria of sensing was discovered in [1] when applying mechanical stress to a resistor changes its electrical properties. However the first complete, small silicon based pressure sensor device was realised in [2, 4] after extensive research.

Over the last two decades, CMOS (complementary metal oxide semiconductor) technology has become the most dominate fabrication technology for integrated circuit (ICs). Researchers are trying to improve process yield and reliability, and on the same time maintain small feature sizes and reducing fabrication cost. Now days, CMOS is not only associated with integrated circuits for specific applications, such as the microprocessor, but also for a variety of microsensors and microelectromechanical systems (MEMS). By using CMOS technologies well defined processes, MEMS technology is introduced to CMOS technology so microsensors benefits from integrated circuits on the same chip. CMOS-MEMS based devices offer unique characteristics, such as calibration by digital programming, self-testing, and digital interface. These techniques on the same chip demonstrate the strength of CMOS based MEMS.

From the regular CMOS process sequence, several classes of microsystems can be tailored for specific application, such as magnetic [44], pressure [47], and biomedical [51] applications. Also, the compatibility between MEMS and CMOS can produce the micromachind thin films after CMOS (post CMOS), or before CMOS (pre-CMOS) or during CMOS (intermediate-CMOS). Also, the compatibility between CMOS and MEMS can produce different types of MEMS sensors using well defined passive components in CMOS technology such as resistors and capacitors to produce piezoresistive sensors and capacitive sensor for applications such as pressure and accelerometers.

As discussed, pressure sensors took the advantage of the huge growth of silicon chips in CMOS technology, and the sensor in active mode operation could be placed near a read out circuitry in the same chip. CMOS chips can also offer smaller size of devices, low power consumption, and can be used in radio frequency applications (RFIC), and therefore, allows for wireless operation due to the advances in telemetry technology. Furthermore, wireless telemetry allows for faster rate exchangeable data. Figure 1.1 shows a block diagram of wireless CMOS-MEMS sensor devices.

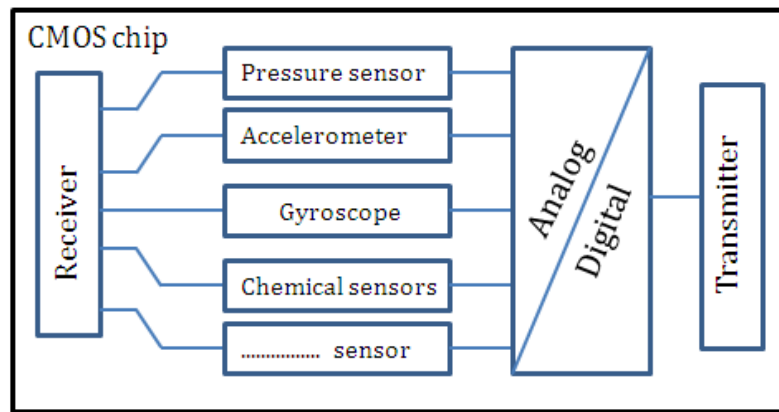


Fig.1.1. Block diagram of a wireless sensor system-on-chip.

The CMOS chip shown in figure 1.1 can be also classed as Radio Frequency Identification (RFID). The technology purpose is to identify an object with RFID tag without wire contacts and line of sight. Information from the object is sent to a wireless reader. The technology is used to track and monitor a physical object wirelessly, were the information are sent to automatic identification and data capture system, which is capable to analyse the information without human interaction.

Until recently, The CMOS-RFID chips use the traditional antenna implementation, which to integrate the radio frequency circuit in one chip and the antenna in another package using standard connectors and impedance transformers. However, moving towards high frequency applications requires the antenna to be implemented on the same chip as the radio frequency circuitry to avoid losses contributed to wire connection, and to insure the antenna to perform with minimum losses at the desired frequency. This method of integration offers fast and low cost transceivers working in short range communication and radio frequency sensing applications. Furthermore, the rapid progress in CMOS technology now allows for entire receivers and transmitters to be implemented on a single semiconductor chip.

The main components of an RFID system are the reader and sensor unit. The reader transmits a continuous RF carrier signal. When a sensor unit enters the RF field of the reader, the sensor receives energy to operate. Once the sensor is energized by the transmitter, it modulates the carrier signal according to the data to be sent. The main advantage of such device is the antenna which can be used to receive power from the reader is also used to transmit information from the sensor.

1.2 Motivation and objectives

The main objectives for developing the device could be summarised as:

- Develop a novel wireless pressure monitoring method for wireless operation.
- Demonstrate miniature, light weight, battery-less pressure sensing device.
- Perform testing evaluation in well controlled environment to investigate feasibility regarding design and fabrication.

Such a device has the ability to bridge the gap between physical world and digital world and promises to have profound impacts on our daily life. The proposed device has huge potential in biomedical and environmental application. The need for miniature telemetry pressure device, with low power consumption is highly desirable to capture real time biological information [66-69] from, for example, patients with Hypertension, heart conditions, muscle monitoring, and head trauma. Furthermore, the device can be used in physical monitoring in a harsh environment which is critical to intelligent control of advanced power generation system such as advanced gas turbine.

A wireless physical sensor traditionally uses coupled lumped elements [73-75] (capacitor and loop inductor/antenna). The proposed device offers an alternative method to using low frequency inductively coupled devices that is to use of microwave signals to read the data from a remote sensor that has been specifically designed to operate at the required frequency.

The main sensing element of the device is a deformable membrane, and the transmitter part is an antenna on top of membrane. Silicon was chosen for fabrication of the device since it is cheap, widely available, and there are many easy to use processes available using MEMS fabrication techniques.

On chip antenna choice must satisfy the need of a miniaturized device. The operation frequency was chosen to be 10 GHz (middle of X-band) since it is widely used in many sensing applications such as RADAR. Furthermore, the wavelength is relatively small in free space, so that there is the possibility of making relatively small single chip devices with appropriate antenna design. The position of the antenna gives the advantage of improved antenna performance.

Another sensing element is considered for the proposed device. Unlike the previous device, coupling the antenna with capacitor sensor is the alternative method to realize such device. The sensor uses a passive element [58-60] offered by many CMOS technology foundries. Metal insulator metal capacitors array is coupled with an antenna working at the same frequency band as the previous device. The capacitive type pressure sensor is used to detune the resonance frequency of the dipole antenna according to capacitance change.

A novel method to fabricate the sensor is also introduced in this thesis, which helps to minimize the post processing steps of the device. The CMOS-MEMS capacitor sensor is realized by etching a significant amount of silicon leaving the array inside the protection layer of the CMOS-MEMS (silicon dioxide/nitride).

1.3. Thesis outline

The remainder of this thesis is divided into six chapters.

Chapter 2 is a review of the literature relevant to design and fabrication of wireless MEMS and CMOS-MEMS pressure sensors.

Chapter 3 describes some design consideration for small size antennas on silicon chips for microwave operation. Different types of on chip antennas are also featured in this chapter, in addition to the design of antennas on HFSS software with results.

Chapter 4 describes in details the fabrication steps of in house devices.

Chapter 5 presents the design and post processing of a CMOS-MEMS pressure sensor using National Semiconductor design kit.

Chapter 6 contains the packaging process, testing methods and architecture for all devices. Also featured in this chapter the results obtained by direct prober and free space measurements.

Chapter 7 draws conclusion and some suggestion for future work.

Chapter 2

2. Literature Review

2.1 Silicon pressure Sensors

A sensor is defined as a device which converts the physical attribute that is to be measured into an electrical signal that can be processed, recorded, or transmitted. The physical parameters can be classified into different groups such as mechanical, thermal, chemical, and electromagnetic [5].

Normally a sensor can be divided into a sensing part and a converting part. For example, in a capacitive pressure sensor the sensing part will be a membrane and the converting part will be the change in capacitance due to membrane deflection.

In the same way as silicon microelectronics has improved the electronics and computer industries with integrated circuits using CMOS and BICMOS technology, silicon micromachining has opened the way for extremely small and accurate sensors and actuators. The advantages of silicon micromachining can be summarized as follows:

- Silicon has excellent mechanical and electrical properties, for example silicon is stronger than steel (yield strength of 7 GPa compared to 4.2 GPa) and light as aluminium (density of about 2.3 g/cm³). Silicon also has good elasticity and has little or no mechanical hysteresis.
- Shaping of Devices using Photolithography and Electron beam lithography offers high precision geometries that can reach the Nano-scale.
- Batch fabrication means that many devices can be made in parallel and that the price per device can be very low.
- The possibility of integration of electronics on the sensor chip as well as the creation of more than one sensor on chip is also an advantage.

However, silicon has some disadvantages. Silicon can be fractured along various planes, meaning that silicon is relatively brittle and sometimes damping mechanisms must be included in the design of a device to overcome this effect. The mechanical properties of silicon are strongly dependent on crystal orientation. This dependency is important for sensor applications (membrane fabrication) and when using a silicon wafer as mechanical support. The thermal properties of silicon are important for packaging and hybrid integration of devices, and must be taken into consideration.

2.1.1 Basic Micromachining Concepts

2.1.1.1. Photolithography

Photolithography is the process of defining a pattern through a structure on to radiation-sensitive polymer deposited on a flat substrate, illuminating it by some source using some pattern (a mask) thereby making the illuminated parts either soluble or insoluble and then removing the soluble parts. Since the actual device will be created by photolithography, this step is the most decisive for creating a “MEMS device”. This can be accomplished by the utilization of an electron or ion beam, a laser, as well as by optical or an x-ray.

For optical photolithography, illumination systems are used to produce an image on the substrate using a photomask. The exposure systems are classified by the optical method that transfers the image from the mask to the wafer.

The first method is to have a mask which is more or less pressed against the photoresist-layer (contact). The second method a mask is close to the substrate (proximity) whereas in the third method a mask is put in a projection system to have a projection of the mask on the photoresist-layer. Figure 2.1 below shows photolithography steps. The lithographic processing used in this project will be discussed in details in chapters 4 and 5.

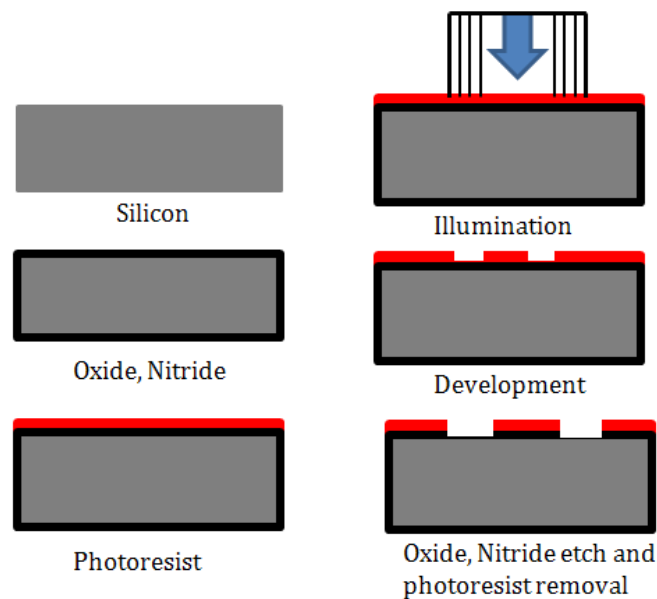


Fig. 2.1. Various steps in a photolithography process.

2.1.1.2 Growth and deposition

To create structures on silicon, other materials are needed for two purposes. The first one is to shield the underlying material during certain processes such as etching, and the second one is to change the electrical and mechanical characteristics related to these materials. Layers can be grown by using part of the underlying silicon layer to create silicon compounds (Silicon dioxide, silicon nitride, polysilicon, and silicides). For example, silicon dioxide can be grown by several mechanisms such as chemical vapour deposition (CVD), or thermal oxidation. Metals and dielectrics are deposited by evaporation or sputter coating.

2.1.1.3. Bulk micromachining

The process was first used for the fabrication of pressure sensors [6]. Bulk micromachining involves the different techniques that use a single-crystal silicon wafer as the structural material itself. Using anisotropic silicon etching and wafer bonding, 3D structures such as pressure sensors, accelerometers, and different resonators have been created. The purpose of this technology is to make structures that are released or undercut by selectively removing a substantial amount of silicon. One of the most important parts of the technology is etching of silicon, either a small layer or entirely through a silicon wafer. There are two etching techniques: wet chemical etching and dry

etching, and it can be distinguished on the basis of the etch profiles they produced: isotropic (etch-speed equal in all directions leading to rounded structures), anisotropic (etching speed highly dependent on the crystallographic directions leading to sharp edges and corners) [7].

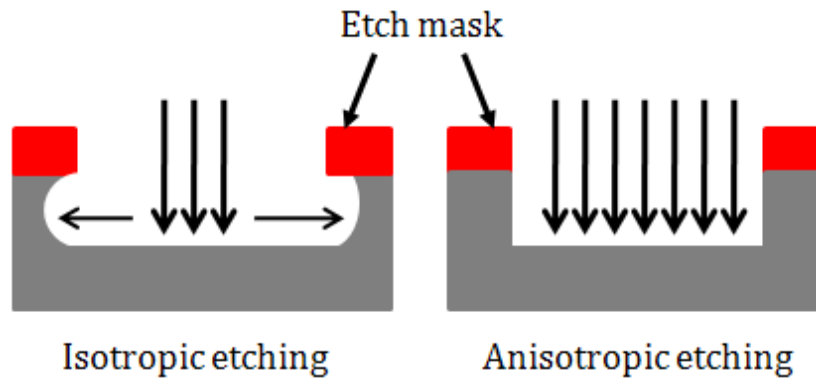


Fig.2.2. Anisotropic and isotropic etching.

Examples of anisotropic wet-chemical etching are etching in potassium hydroxide (KOH), Ethylene-Diamene-Pyrocatechol (EDP), and Tetramethyl Ammonium Hydroxide (TMAH) solutions. EDP is usually processed at temperatures between 110-120 °C. The main advantages of using EDP are the smoothness of the etched surface and high selectivity between SiO_2 and silicon, making SiO_2 an ideal masking material. Recently, EDP has not been used as frequently due to its hazardous nature. It is a highly dangerous nerve toxin and carcinogenic etchant and has recently been banned in most integrated circuit fabrication facilities.

KOH etches are performed around 80 °C, where etching produces a uniform and bright surface. When performed above that temperature, the process can cause non-uniformity in the material. Hydrogen bubbles are formed along the silicon surface causing roughness, but can mostly be removed by agitating the etchant. The main disadvantages of KOH are that it is not compatible with the IC fabrication process and it etches SiO_2 at a rate too fast for it to be used as a mask, making Si_3N_4 a preferred masking material. The last main type of etchant for silicon is in the ammonium hydroxide group, where TMAH or CH_3NOH is the most popular etchant. TMAH is nontoxic, can be handled easily, does not decompose below 130 °C, and shows good selectivity to silicon oxides and nitrides. If the etchant is prepared properly, TMAH can become selective to aluminium, making it fully IC-compatible. The drawback of using

TMAH is its slow etch rate and tendency to cause rough surfaces. For most typical TMAH solutions, the etch rate and the surface roughness are decreased by increasing the TMAH concentration, and at temperatures around 95 °C, TMAH etching produces similar results to KOH etching.

The main drawback of this bulk micromachining technology is that it leads to relatively large area wastage and high cost [8].

Dry etching is a process used to produce microstructures with vertical sidewalls, remove photoresist and sometimes even clean wafers. The etched vertical sidewalls are independent of the crystallographic nature of the material. There are three main dry etching techniques:

- Plasma etching: a halogen gas is introduced into the chamber. A RF signal is applied to the electrodes (anode and cathode) that cause the gas to break into reactive species. These reactive species are directed towards the wafer surface. When the reactive species reach the wafer they react with the surface and etch it away.
- Reactive ion etching (RIE): bombardment of a wafer surface with ions is combined with plasma etching to increase the etch rate.
- Deep reactive ion etching (DRIE): uses high density plasma a couple orders greater in magnitude than that used for RIE to increase the etching rate.

Mask materials used for dry etching include SiO₂, Si₃N₄, and photoresists.

2.1.1.4. Surface micromachining

Surface micromachining is the technique where the silicon substrate is used as support material. Surface micromachining is widely used in MEMS technology, and many devices using this technique are reported in [9-12]. The process involves the processing of different thin films such as polysilicon, silicon dioxide and silicon nitride which can be deposited and etched, building up advanced microstructures. The dimensions of surface micromachined structures are generally one or two orders of magnitude smaller than those of bulk micromachined devices [12, 13], and, with care, surface micromachining is compatible with CMOS such that mechanical functions can be integrated with electronics. Figure 2.3 below shows the surface micromachining steps.

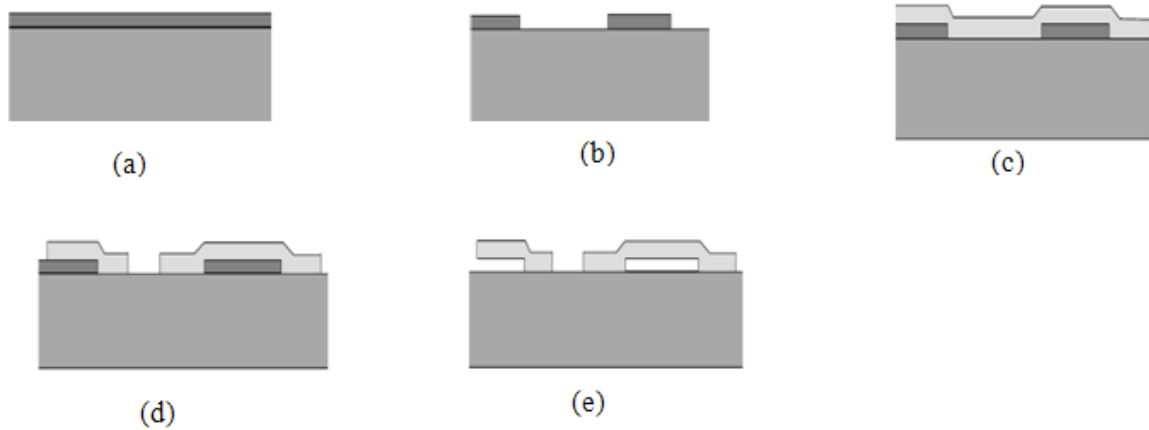


Fig. 2.3. Surface micromachining.

First step (a) a sacrificial layer is deposited on the silicon substrate. Subsequently this layer is shaped using photolithographic and etching techniques (b). Next a layer of the structural material is deposited over the sacrificial layer (c). Again using photolithography and etching the structural layer is shaped and holes are made to allow etching fluid to reach the sacrificial layer in selected areas (d). Finally the sacrificial layer is completely removed by wet-chemical etching thereby releasing part of the structural layer.

Figure 2.4 below shows a pressure sensor membrane using bulk and surface micromachining techniques. Membrane dimensions for the bulk micromachined device are usually larger than surface micromachined membrane [12, 13].

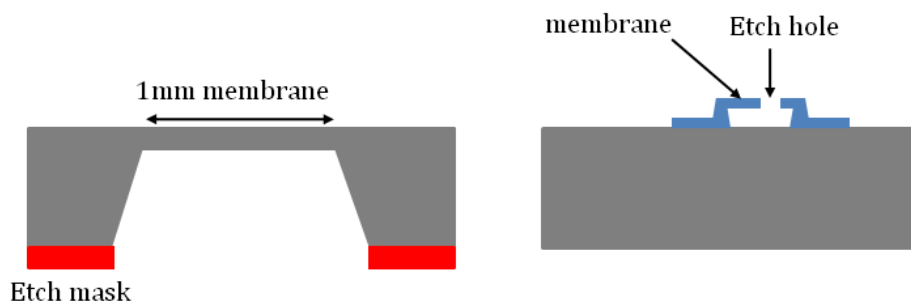


Fig. 2.4. Pressure sensor diaphragm structures fabricated using bulk micromachining with anisotropic etching and surface micromachining sacrificial layer techniques.

We can summarize the advantages of bulk over surface micromachining as follows:

Using etch stop techniques, we can achieve several microns thickness of membrane if needed. Also, it can be used Complementary-Metal-Oxide Semiconductor (CMOS) technology, on chip read out circuitry could be bonded to the micromachined part.

Surface micromachining on the other hand offers certain advantages to pressure sensor design and fabrication as compared to bulk micromachining, and we can summarize them as follows:

- Thin sacrificial layers allow fabrication of capacitor electrodes with small distance between them.
- The thickness of the membrane can be precisely defined and controlled by layer deposition without the need for etch stop techniques.
- Greater sensitivity transducers.
- Allows the use of isotropic etching in combination with great control of dimensions.
- Wafer front side processing is sufficient to create shallow cavities and release micromachined structures.
- Allows plugging small holes and thus sealing cavities, creating vacuum reference pressure pads without the need for wafer bonding.

2.1.1.5. Bonding

To improve the possibilities and complexity of micromachined devices (partly structured) wafers of various materials can be bonded together. Anodic bonding can be applied to a good conducting layer (metal, silicon) and a slightly conducting layer (glass). A voltage applied between the wafer-pair induces a small depletion layer in the glass wafer resulting in a large electrical field over a short distance near the interface of the wafers. The resulting electrostatic force brings the wafers in such close contact that they join together. The technology is available for wafers with surface roughness of less than 1 micron. Silicon fusion bonding is the second type of bonding, which occurs between layers that have a roughness of 1 nanometer or less. Since it needs extremely smooth wafers, a condition which is very difficult to meet, there is a technology which can help to make the process more applicable: Chemical Mechanical Polishing (CMP). Bonding is discussed here briefly for completeness of micromachining steps. In this thesis, no practical work has been done on wafer bonding.

2.1.2 Pressure sensors types

The first sensor fabricated using MEMS techniques was a pressure sensor [14, 15] which has widespread applications in aerospace, biomedical, automobile and defence. The basic principle of a pressure sensor is to measure the mechanical deformation caused in a membrane when pressure is applied. The mechanical deformation is translated into an electrical signal.

There are different principles to sense deformation such as piezoelectricity, piezoresistivity, changes in capacitance, and changes in resonant frequency of a vibrating element in a structure. Piezoelectricity is the ability of some materials to generate an electric potential in response to applied mechanical stress. In order to translate the mechanical deformation or strain into an electrical signal in silicon which is not a piezoelectric material is a difficult task, as the external material must be glued into silicon membrane, and this procedure does not form part of integrated circuit technology. Furthermore, piezoelectricity cannot be used for static pressure sensing due to charge leakage.

A resonant sensor convert pressure into a change of resonance frequency of a vibrating system, or in other words, the frequency of a mechanical beam or membrane is directly related to the extent is stretched. Resonant sensors are noted for their excellent stability and the output signal of this type of sensor can be directly converted into a digital signal, which is the main benefit of these types of sensors, however resonant sensors have complicated structures and hence are expensive. Other disadvantages are they require vacuum sealing and mechanical coupling between the membrane and resonator.

At the moment, piezoresistive pressure sensors are still the most widely used. Piezoresistors may be diffused in the membrane or deposited on top of the membrane. These sensors make use of the change in the resistance of conductors due to the change in their physical dimensions when subjected to stress. Usually, the resistors are connected in a Wheatstone bridge configuration for temperature compensation. The main advantages of a piezoresistive read-out mechanism are the simple fabrication process, the high linearity and the fact that the output signal is conveniently available as a voltage. The main problems are the large temperature sensitivity. Furthermore, because of their inherent low sensitivity, piezoresistive devices are not suitable for

accurate measurement of very low pressure differences. However, because of their low cost a vast majority of commercial pressure sensors today use piezoresistive sensing.

Capacitive sensing is one of the simplest and lowest-power of converting pressure into electrical signal. In principle, a capacitor is an energy storage device made by two parallel conductors or semiconductors plates separated by a dielectric medium. They have several advantages over other pressure sensors, especially at low pressure and their lesser sensitivity to temperature changes offers long term stability.

Piezoresistive sensors are easier to fabricate, and more readily manufactured than capacitive sensors. Also since the capacitance is proportional to area, it is difficult to design small capacitor sensors; thus, piezoresistive sensors can be made substantially smaller. In the next section, we show some examples of silicon based pressure sensors.

2.1.2.1 Piezoresistive pressure sensors

As mentioned previously, piezoresistive pressure sensors were the first to be realized using MEMS technology. The sensing element (resistors) could be diffused or deposited on top of the membrane with an isolation layer, usually SiO₂. The diffusion is carried by dopant atoms, and the deposition is carried in the form of metal, polysilicon, or single crystalline conducting lines. In SOI technology, a single crystalline silicon layer is deposited on top of SiO₂ by silicon fusion bonding, and then structured into the resistor geometry [16]. At higher temperature, above 120 °C, deposited resistors perform better than diffused resistors in terms of drift and noise originating from the parasitic junction to the substrate. On the other hand diffused resistors provide larger sensitivity. The membrane is formed through KOH wet etching and in most cases four piezoresistors are realised in a full Wheatstone bridge arrangement. If the bridge is deflected by external forces the piezoresistive elements are strained and change their resistance values. This resistance change is evaluated by feeding a current to the bridge and measuring the output voltage. The piezoresistive effect is commonly described by the equation:

$$\frac{\Delta R}{R} = \gamma_l \cdot \sigma_l + \gamma_t \cdot \sigma_t \quad (2.1)$$

Where γ_l and γ_t denotes the longitudinal and transversal piezoresistive coefficients and σ_l, σ_t are the corresponding stress values resulting by mechanical strain of the structure and $\Delta R/R$ denotes the relative resistive change. The four resistors are placed in close proximity to the region of maximum stress under deflection. Preferably resistors are placed in a longitudinal configuration and the other two resistors in a transversal configuration i.e., one pair of resistors is exposed to tensile stress under a given deflection of the membrane and the other pair is exposed to compressive stress as shown in figure 2.5 (a). This automatically leads to an asymmetric change of their resistivity as the resistance increase for one pair of resistors and decreases for the other pair of resistors. This configuration introduced to a Wheatstone bridge (figure 2.5 (b)) yields a corresponding bridge voltage that depends only on resistance change.

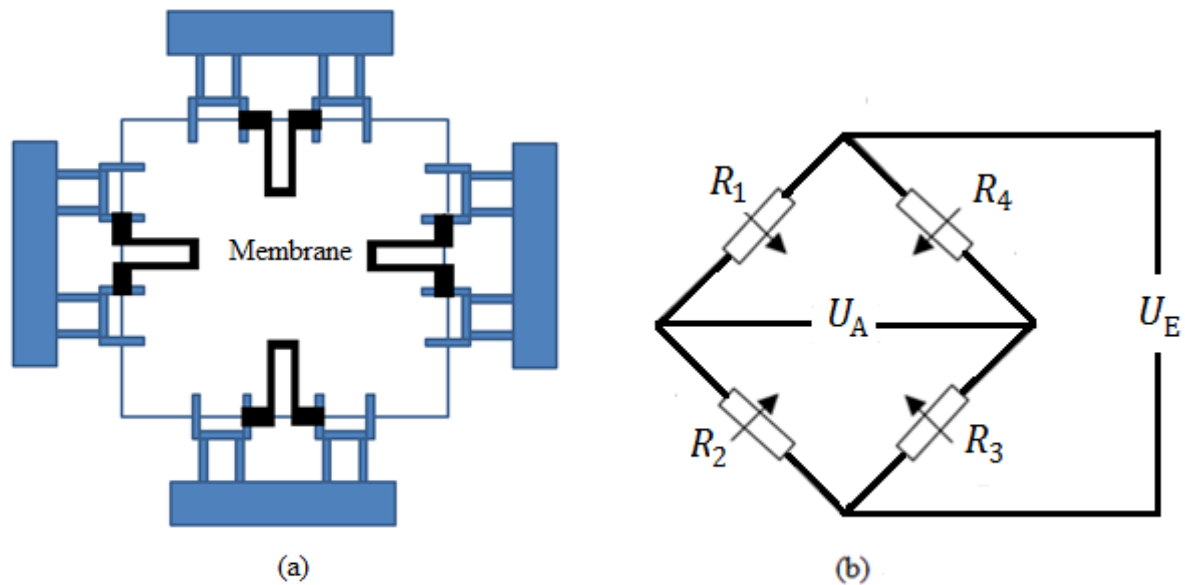


Fig. 2.5. (a) Physical layout of a Wheatstone bridge with metal interconnects (Blue) and poly-silicon resistors (Black) on membrane. (b) Schematic of the Wheatstone bridge. The change in voltage corresponds to pressure.

The relation between the applied strain ε ($\varepsilon = \Delta L/L$) and the change of the resistance of the strain gauge is given by the equation:

$$\frac{\Delta R}{R} = K\varepsilon \quad (2.2)$$

K is the piezoresistive factor and ε is the strain. K is close to value of 2 for metal resistors and 30 for monocrystalline silicon.

At point of balance the ratio $R_1/R_2 = R_4/R_3$. For practical strain gauge applications, the resistors from R1 to R4 have the same value to ensure that the relative changes of the individual bridge arms are proportional to the variation of the output voltage.

When applying pressure to membrane, the output voltage (U_A) starts to vary. Assuming the resistance variation $\Delta R/R_i$ is much smaller than initial resistance value R_i , now we have the following relationship:

$$\frac{U_A}{U_E} = \frac{1}{4} \left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2} + \frac{\Delta R_3}{R_3} - \frac{\Delta R_4}{R_4} \right) \quad (2.3)$$

U_E represents the input voltage. Substituting equation 2.2 into equation 2.3 we find:

$$\frac{U_A}{U_E} = \frac{K}{4} (\varepsilon_1 - \varepsilon_2 + \varepsilon_3 - \varepsilon_4) \quad (2.4)$$

In equations 2.4 we assume $\varepsilon_1 > \varepsilon_2$ and $\varepsilon_3 > \varepsilon_4$.

The need for temperature compensation is for both sensitivity and bridge offset. When temperature variation occurs during the mechanical loading of the strain gauge, an undesired effect (thermal expansion, ε_{th}) occurs on the same time with mechanical strain ε_M . Equation 2.2 becomes:

$$\frac{\Delta R}{R} = K(\varepsilon_M + \varepsilon_{th}) \quad (2.5)$$

Substituting this equation into equation 2.4 we find,

$$\frac{U_A}{U_E} = \frac{K}{4} [(\varepsilon_M + \varepsilon_{th})_1 - (-\varepsilon_M + \varepsilon_{th})_2 + (\varepsilon_M + \varepsilon_{th})_3 - (-\varepsilon_M + \varepsilon_{th})_4] = \frac{K}{4} \cdot 4\varepsilon_M \quad (2.6)$$

Equation 2.6 shows the compensation for strain caused by thermal expansion ε_{th} . This method of compensation could be applied to half bridge, where two piezoresistive are placed on membrane [17].

The need for temperature compensation is for both sensitivity and bridge offset. For example, a low doped silicon resistors start to change its resistance above 100 °C which affects the sensitivity of the same order of magnitude, which makes the temperature compensation necessary. Offset changes are caused by temperature dependent leakage currents through dielectrics. To compensate for leakage current, a constant feed to Wheatstone bridge and measure both the bridge voltage and the difference voltage proportional to differential pressure. However, this technique requires high power consumption which is a major drawback for piezoresistor sensors. An interesting method to compensate for both temperature and bridge offset was demonstrated in [18]. By adding another bridge near the membrane, which has the similar offset components, reduction of the offset and its temperature drift was realized by subtraction of the output of two bridges, resulting in 95% reduction for 95 °C span.

To realize the pressure sensor, the membrane is etched from the back side using KOH as described in 2.1.1.3. The thickness of the membrane is usually several tens of micrometers, and realized using a timed etch stop technique. The main advantage of using this technique is that it does not require doping the membrane with boron. The main problem is in the consistency of producing the same thickness, which affects the overall sensitivity of the device. A boron etch stop provides good control over the membrane thickness, however the highly doped silicon prohibits the use of diffused strain gauges therefore often an electrochemical etch stop is used with a more lightly doped membrane.

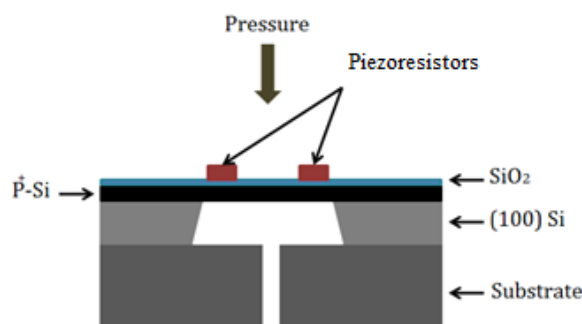


Fig. 2.6. Cross section of bulk micromachined piezoresistive pressure sensor.

Surface micromachining can be used for much thinner membranes by under-cutting from the front side of the wafer. However, membranes released this way cannot consist

of mono-crystalline silicon. The introduction of Si_3N_4 and polysilicon membranes helps the use of mono-crystalline silicon [19, 20].

In general, piezoresistors suffer from low accuracy, poor sensitivity, and a high degree of non-linearity at large deflections. The non-linearity is a result of stretching of the middle of the middle plane which becomes larger at larger deflections. To overcome this problem, membranes with a rigid centre are introduced to increase the membrane stiffness and limit the maximum deflection. A sensitivity of 35 mV/V with non-linearity of 0.05% was reported in [21] using a square rigid centre behind the membrane for a ± 10 kPa pressure range. These figures are larger by 3.5 to 20 times than traditional piezoresistors. A circle shaped centre membrane was studied in [22] for linearity and sensitivity optimization. The membrane thickness was 25 μm with diameter of 600 μm and used to measure a pressure span of 4 MPa. The simulation results in [22] predict a much higher sensitivity and linearity for devices with circular centre membranes. Figure 2.7 shows a square and circle rigid centres behind membrane.



Fig.2.7.linearity enhancing square (a), and circle centre (b) membrane with piezoresistors on top.

2.1.2.2 Capacitive pressure sensors

In principle, a capacitor is an energy storage device made by two parallel conductor plates separated by a dielectric medium such as air. Capacitive pressure transducers require the deflection of the membrane, which causes the distance between the plates to change. This result in a change of capacitance which is a measure of the pressure applied. The capacitor has air as a dielectric, the silicon membrane as one plate and a metal layer as the other plate. Usually, an electronic C/V converter is provided to couple the output with applied pressure.

As discussed previously, in direct comparison with piezoresistive sensors, capacitive pressure sensors have the advantage of high accuracy and show small temperature

dependence of offset and sensitivity, and this device requires no temperature compensation techniques. Another important advantage is the very low power consumption compared to piezoresistors in a Wheatstone bridge configuration which constantly draws current from a voltage source (Fig 2.5). Figure 2.8 shows a simple diagram of a parallel plate capacitor. The distance between the plates is d and dielectric medium of ϵ . The area of the plate is A .

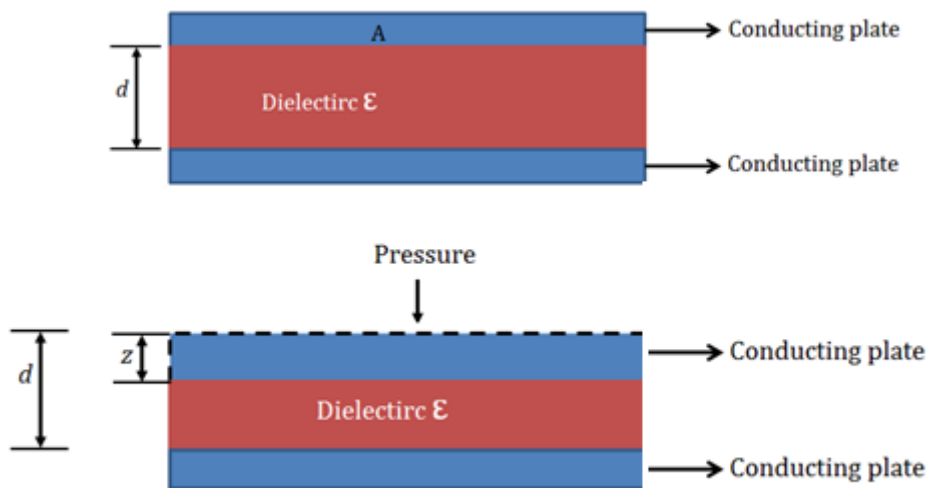


Fig.2.8. Parallel plate capacitor (top) and movement of top plate by distance z after applying pressure (bottom).

The capacitance at zero pressure (P_0) is given by:

$$C(P_0) = \frac{\epsilon A}{d} \quad (2.7)$$

However, when a membrane is deflected by distance (z) is the pressure will change according to:

$$C(P_d) = A\epsilon \int \frac{dz}{d - w(z)} \quad (2.8)$$

Where $w(z)$ is the deflection in z direction. We indicate from the above equation the relationship between the capacitance and deflection is non-linear. To improve linearity, a same technique used on piezoresistive pressure sensors which involves using a rigid centre. In this case, the membrane contains the rigid centre and capacitance includes only the area behind the membrane.

Equation (2.4) can be written as:

$$C = \frac{\epsilon A_{\text{centre}}}{d - \Delta d} \quad (2.9)$$

Where Δd is the pressure dependent deflection of the centre area. A study was carried out in [23] to investigate the linearity of capacitive pressure sensors. One result shows better linearity when the membrane is in full contact with surface behind it. The increasing capacitance is not a result for decreasing distance between plates but of an increase of the touching surface area. Other investigations of capacitance linearity were carried out in [24-26].

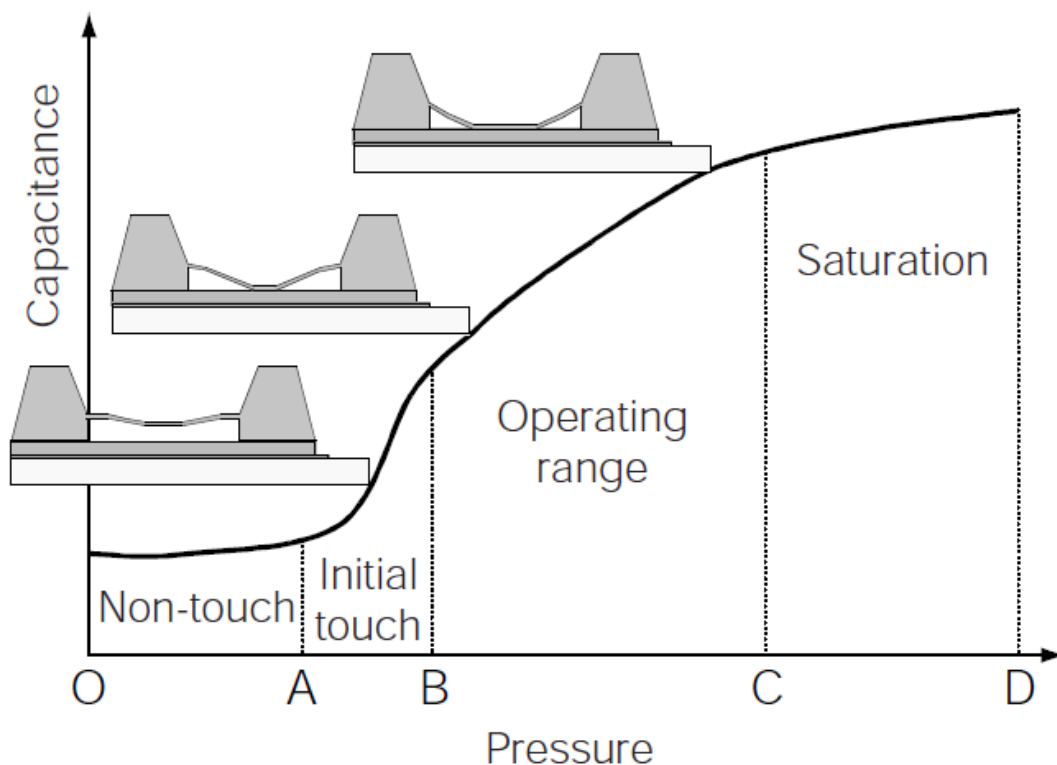


Fig 2.9. Typical pressure-capacitance curve of touch mode capacitive pressure sensor [26].

As shown previously, capacitive pressure sensors are less sensitive to temperature. A pressure sensor working above 500 °C and 700 psi was reported in [27]. An approach to minimize the parasitic capacitance is to fabricate the sensor on fused silica. Surface micromachining on fused silica improves the membrane stress control [28].

A novel fabrication method to fabricate capacitive pressure sensor was shown in [29]. The novel technology uses single crystal silicon as a membrane material and perforated

polysilicon as a back plate for the capacitor. This method allows more stability and high sensitivity for the sensor.

A vacuum sealed absolute capacitor pressure sensor, based on a sandwiched structure was presented in [30]. The sensor was fabricated by a simple three-mask process and sealed in vacuum by anodic bonding. The sensor, which utilizes a combined $\text{SiO}_2/\text{Si}_3\text{N}_4$ layer as the elastic dielectric layers, exhibits high sensitivity, good linearity, and packaged to reduce the effects of environmental temperature and humidity.

The use of a capacitor sensor with a reference capacitor on the edge of the membrane was reported in [31]. The reference capacitor is almost independent of pressure thus the sensor exhibits high linearity. An interdigitated capacitor was introduced in [32], and the design optimized such that the nonlinear part in the relation between the applied pressure and the change in the sensor capacitance is compensated by a corresponding nonlinear pressure dependence of the reference capacitor.

2.1.2.3 Resonant pressure sensor

Resonant sensors require a mechanical actuation, or in other words, an excitation of a sensitive vibration element. Two types of resonant sensors are distinguished; a vibrating membrane and a vibrating structure on top of membrane. For a vibrating membrane, the resonance frequency is dependent on the pressure difference across the membrane. For a vibrating structure, the membrane deflects due to pressure difference and the resonance frequency of the vibrating structure changes as the strain changes across the membrane.

Vibrating pressure sensors have a common element, which is an anisotropically etched membrane fabricated through a timed controlled etch stop or boron etch stop. Several methods are used to excite and detect the vibration. One method is to sputter a piezoelectric thin film such as ZnO, AlN, and PZT. A voltage across the thin film changes the dimensions of the film. The increase in lateral dimensions gives rise to a bending moment in the membrane that can be used to excite bending vibrations of the membrane. One of the first pressure sensors to use this mechanism was reported in [33]. A realization of a resonant pressure sensor by fusion bonding and trench etching was reported in [34]. Another excitation is to use the thermal expansion mechanism to

change the dimensions of a piezoresistive material deposited on top of a membrane [35]. We can summarise the methods of actuating and sensing as follows:

- Electrostatic excitation and detection.
- Piezoelectric excitation and detection.
- Magnetic excitation and detection.
- Electrothermal excitation and detection.
- Optothermal excitation and detection.
- Dielectric excitation and detection.

The use of piezoelectric resonance sensors offers the advantage of driving the resonant frequency to several hundreds of MHz or even to the lower GHz range. The main application for such a sensor is Surface Acoustic Wave Sensors (SAWs).

The problems associated with vibrating membranes are that the resonant frequency of the resonator is not only a function of applied pressure but also depends on the type of gas in the vicinity of the membrane, type of gas and temperature, hence when applying the gas onto membranes, absorption of chemicals and dust and corrosive effects changes the mechanical property of a resonator and automatically changes the resonance frequency of the system.

To solve this problem, sensors have been developed so the membrane itself does not vibrate, but instead a resonator has been integrated on the membrane. One sensor using an integrated resonator on membrane was reported in [36]. It consists of a butterfly shaped resonator on top of 6 μm thick membrane and carried through boron etch stop. An integration of single crystalline resonant strain gauges on a membrane was reported in [37]. The resonator was protected by a cap and operated in a vacuum and thus provides low air viscosity and damping resulting in a high quality factor device. The resonator consists of two parallel beams connected in the middle in an "H" shape as shown in figure 2.10. A constant magnetic field was generated through a constant current applied to one beam according to Lorentz force. The induced voltage at the second beam is used to detect the vibration.

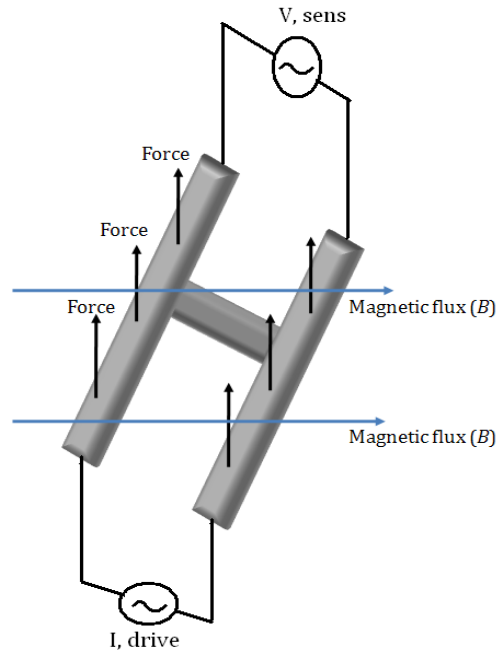


Fig 2.10. Operating principle of an electrodynamically driven H-Shaped resonator (magnetic excitation and sensing) [36].

The concept of integrating a resonator on top of membrane appears to be successful at vacuum as discussed earlier. However, a resonator consisting of monocrystalline silicon appears to be a problem due to the complexity of the fabrication process. Other devices have been fabricated using polysilicon resonators [38, 39] with centre surface behind the membrane to improve linearity.

Another problem with integrated resonant pressure sensors on a membrane is the coupling between parts of a resonator and membrane causing an undesired resonance. To eliminate the mutual coupling between resonator and membrane mechanical isolation is used, which in the other hand, makes the fabrication steps more complicated.

Finally, resonant sensing principles are the least used type of pressure sensors. However, a piezoelectric is used as the basic sensor material, resonant pressure sensors could offer more potential unless the technology associated with piezoelectric material such as quartz is more advanced.

2.2 CMOS-MEMS technology

2.2.1 Introduction

The integration of sensor elements with CMOS or BICMOS circuitry for signal conditioning is an exciting way to offer micro-sensors systems that are precisely tailored to the specific need of customers. In the first approach, this means to sample, amplify, compensate, calibrate and output the pressure sensor signal. The calibration addresses the sensor's transfer function to specified parameters such as zero pressure offset, sensitivity, and linearity. Compensation on the other hand is required for reduction or elimination of temperature effects or supply voltage variation.

CMOS-MEMS refer to silicon integrated MEMS based on integrated circuit (IC) technology combined with micromachining, thin film deposition or electro-deposition [40-43].

MEMS technology is the key to realize sensor and actuator functionality. Silicon is certainly the material of choice due to its excellent electrical and mechanical properties.

The CMOS process is compatible with MEMS technology in the following techniques:

- Bulk micromachining: wet or dry etching, anisotropic or isotropic, front or backside of chip.
- Surface micromachining: Sacrificial oxo-nitride, polysilicon, metal layers.
- Micromachining before adding CMOS circuitry (Pre-CMOS).
- Micromachining inside CMOS foundry (intermediate process).
- Use of IC layers (monocrystalline silicon, polycrystalline silicon, metal and Bump) to form sensors.
- Additional layers compatible with CMOS and wafer bonding.

Micromachining steps can precede or follow the regular CMOS process (pre-CMOS or post-CMOS), or can be performed in-between the CMOS steps (intermediate processing).

2.2.2 Pre, Intermediate, and Post processing of CMOS chips

In the pre-CMOS approach, the sensing elements are constructed before the regular CMOS process sequence. Examples of pre-CMOS are a trench-Hall device sensitive to magnetic induction parallel to the chip surface [44], embedded polysilicon microstructures in a shallow trench then followed by CMOS process [45], and a variety of test structures including MOSFETs, piezoresistive pressure sensors and cantilever beams were successfully fabricated after using silicon wafer bonding to create a substrate that can be inserted into an existing IC fabrication line [46]. All these devices showed capability to be introduced to the microelectronic (IC) processing line, and successfully integrated electronic circuitry to the established microstructures.

As mentioned before, CMOS process could be interrupted for additional thin film deposition or other micromachining steps in intermediate processing. Examples of intermediate CMOS process are pressure sensors for biomedical applications designed and fabricated at Infineon Technologies [47], and also a monolithic accelerometer which incorporates a surface-micromachined polysilicon sensor with bipolar/MOS interface circuitry on a single chip made by analog Devices [48].

Post CMOS is the preferable choice after completion of the standard IC process sequence. For post processing of a chip, two approaches are widely used. First, MEMS structures can be built on top of the finished CMOS substrate, leaving metal layers and polysilicon layers untouched. Examples of this approach are illustrated in Texas instruments digital micro-mirrors [49], Delphi electroplated ring gyroscope [50] and pH sensors [51].

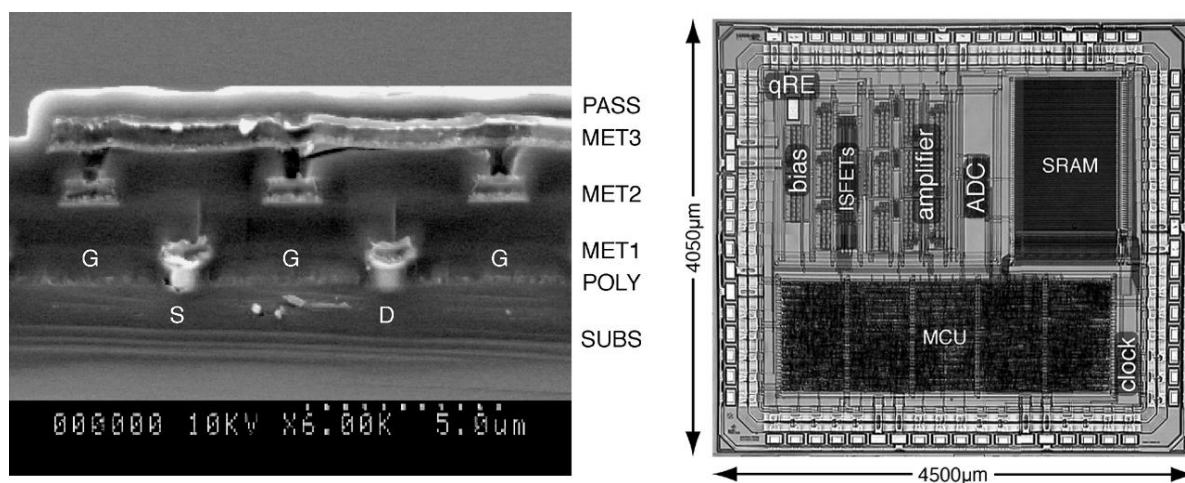


Fig 2.11. ISFET cross section and integrated system-on-chip pH sensor [51].

2.2.3 CMOS-MEMS sensing elements

As discussed earlier, the two main pressure sensing methods are capacitive and piezoresistive and CMOS-MEMS rely heavily on the passive components to establish which component is used as a sensing element. In next section, we briefly investigate resistors, capacitors, and micromachined RF components such as tunable capacitors.

2.2.3.1 Resistors

Resistors are used in analog and mixed circuit blocks. Many foundries offer a wide variety of resistors in a standard CMOS technology process. One method fabricate resistors is to use polysilicon since it is more resistive than metal. This works by blocking the silicide layer that is deposited on top of the polysilicon and creating a region having the resistivity of the doped polysilicon. However this requires an additional mask and corresponding lithography sequence. The resistivity obtained is in the range of fifty to few hundred Ohms per square due to various implants in the process.

Highly doped P-type polysilicon resistors are preferred in mixed signal applications due to their good matching and low parasitic capacitance to the substrate. The reduction of parasitic capacitance to substrate is achieved by fabricating a shallow trench under these resistors, and the ends of the resistor are silicided for low contact resistance to the back end of the line (interconnect), resulting in lower contact resistance than that obtained by directly connecting the metal layer to doped polysilicon. These resistors, as mentioned above, exhibit less capacitance to substrate, in the order of 90 af/ μm^2 for the bottom plate and 100 af/ μm^2 for the fringing capacitance [52].

2.2.3.2 Capacitors

There are three types of capacitors provided by CMOS technology to meet requirements for reduced board level components. The first capacitor is MOS poly-gate capacitor on single crystal silicon, Polysilicon-Insulator-Polysilicon (PIP), and Metal-Insulator-Metal (MIM) capacitors. Each capacitor is used according to the designer's needs for a specific application.

Poly-Poly capacitors are fabricated in a double polysilicon process. The capacitor structure is formed using P^+ doped poly-gate as the bottom plate, a deposited oxide or

nitride layer for as the capacitor dielectric, and the top plate is formed from silicided extrinsic base polysilicon. The quality of the dielectric (field-oxide) is crucial to ensure high reliability and robust breakdown strength. Thermal oxide is not recommended for this process due to roughness round the edges of polysilicon gained during thermal oxidation, yielding high field points that reduce the strength. An alternative is to use plasma enhanced chemical vapour deposition (PECVD) dielectric, but these typically have poor uniformity. The best solution is to use hot thermal oxide (HTO), which has a breakdown voltage in the range of 9-10MV/cm, and is very conformal yielding full thickness coverage at the poly-gate corners where breakdown typically occurs under high electric field. PIP is widely used in low frequency applications (usually in MHz region), and the device could be optimized, reaching quality factor of 30 by using n+/ n+ polysilicon stack. In general, (PIP) capacitors suffer from low quality factors due to high resistivity of the top and bottom plate and capacitive losses at higher frequencies.

(MIM) capacitors take advantage of low resistivity of top and bottom metal layers, and a thick dielectric that physically distances the device from the relatively low resistivity substrate. The requirements that dielectric layer with a large constant material must meet in order to address manufacturing, design and reliability are demanding. Critical parameters like dielectric deposition temperature, uniformity, rate, constant, capacitance thermal and voltage coefficients and leakage must be considered. These capacitors are more preferred by designers due to their higher quality factor at high frequencies. Reliability is an important issue for CMOS (MIM) capacitors. Most foundries are targeting high capacitance by reducing dielectric thickness while still maintaining acceptable reliability at certain voltages. Reliability is determined using a time dependent dielectric breakdown test. The devices are biased at high electric field so the breakdown point is fast reached. (MIM) capacitors are less reliable than PIP capacitors due to PECVD oxide the dielectric material, and PIP capacitors have a higher quality oxide, therefore (MIM) capacitors have to have thicker dielectric (oxide) and low capacitance to reach (PIP) capacitor reliabilities. Thick metal plates offer lower resistance than doped polysilicon, and thicker dielectric reduces the parasitic capacitance between capacitor and substrate. The main drawback for these capacitors is the large area of chip consumed depending on the application.

From low to high frequencies, capacitors are used in many applications ranging from resonators, filters and *LC* tank circuits. These applications require low parasitic capacitance, series resistance and high Q .

2.2.3.3 Tunable capacitors

A tunable capacitor is a device where its capacitance can be tuned electrically, for example through a DC (tuning) voltage. Tunable capacitors are widely used in many applications such as filters, in the frequency-controlling element in the *LC*-Tank of a voltage-controlled oscillator (VCO) and for matching networks. In CMOS technology, tunable capacitors are implemented as p-n junction diodes and using accumulation junction in MOS devices (j-varactor). However, these devices tend to include excessive series resistance (resulting in low Q) and high parasitic capacitance that limit the tuning range.

Tunable capacitors are usually in the parallel-plate formation, and the capacitance is tuned by varying the gap or the overlap area between the plates.

2.2.4 CMOS-MEMS pressure sensors

2.2.4.1 CMOS-MEMS Piezoresistive sensors

As shown previously, etching the silicon substrate to release membranes is the basic concept for a conventional pressure sensor so it is possible to combine it with standard IC technology. As discussed earlier, the best way to realize the sensor is in the Wheatstone bridge form. The simple method to monitor the voltage drop across the bridge is the use of operational amplifier. Figure 2.12 shows a common circuit topology for integrating the sensor with an operational amplifier.

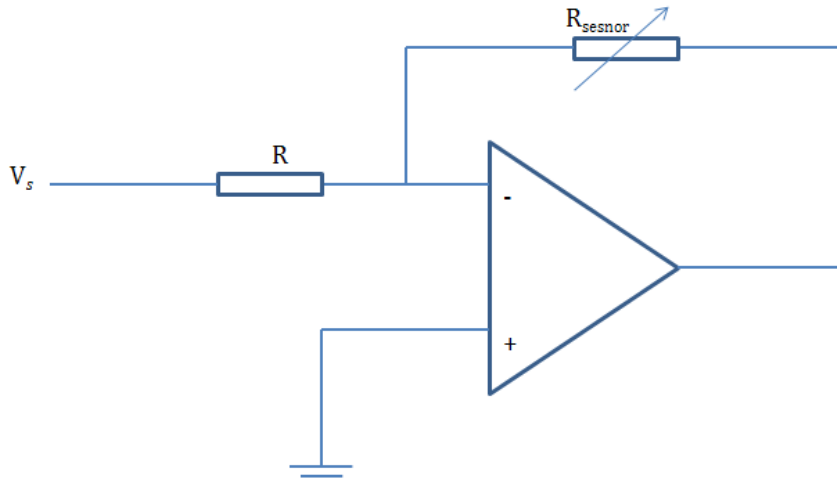


Fig 2.12. Sensors with read-out amplifier.

Piezoresistors strongly depend on temperature which is a major drawback for operation. Another drawback for using piezoresistive sensors is the thermal noise. The thermal noise power is given by:

$$P_{noise} = 4kTR\Delta f \quad (2.10)$$

Where k is the Boltzmann constant, T is temperature and Δf is the signal bandwidth.

When monitoring a voltage drop across a resistor with high input impedance the signal power is given by:

$$P_{signal} = S_{res}I_{const}^2R \quad (2.11)$$

Equation (2.7) shows the need for constant current to compensate for the leakage current. S_{res} represents the sensitivity of the bridge. The signal to noise ratio (SNR) can be increased by reducing the signal bandwidth and increasing the current.

$$SNR = \frac{P_{noise}}{P_{signal}} = \frac{S_{res}I_{const}^2}{4kT\Delta f} \quad (2.12)$$

One of the first piezoresistive pressure sensors with on chip electronics was reported in [53]. The device combines the sensing element with bipolar electronics to provide temperature compensation and to convert the output voltage into frequency. Another example for combining the sensor with integrated electronics is illustrated in [54]. The absolute pressure sensor achieved a linearity error of 0.1% and a temperature dependent offset drift of less than 100 ppm/°C has been measured using a programmable analog circuit. In [55] the total system errors according to temperature change is reduced to less than 0.7% after introducing signal conditioning circuitry. A

method to reduce the noise was reported in [56]. The sensor was part of ring oscillator and integrated with a frequency to digital converter in standard 0.6 μm CMOS technology from austriamicrosystems (AMS).

The power consumption of a CMOS-MEMS piezoresistive pressure sensor is relatively high. A large resistor value is desirable to increase sensitivity. CMOS technology can offer higher resistive device realized in a p - n channel MOS transistor. Figure 2.13 shows a Wheatstone bridge using p channel MOS transistors [57].

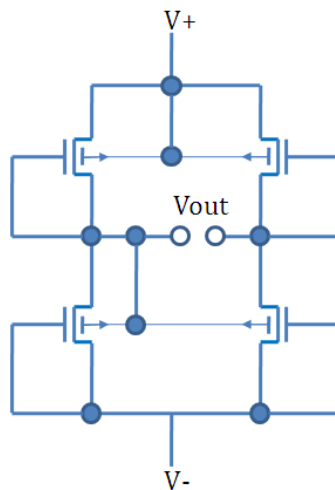


Fig.2.13. P -channel MOS transistors in Wheatstone configuration.

The drawback for this topology is the introduction of flicker noise which predominates at low frequency. An active Wheatstone bridge is more suitable for resonant applications where the low frequency noise can be filtered.

2.2.4.2 CMOS MEMS capacitive sensors

As discussed, capacitive sensors are superior to their piezoresistive sensors in terms of stability and sensitivity. This sensitivity detected by capacitive sensors is very small, and could be in the fF-pF range, and could be susceptible to parasitic effects [58]. In order to detect small signals, a sophisticated and well matched electronic circuitry is required in close proximity to the sensor.

AC modulation (sine or quarter wave) is the common sensing method by continuous time detection. Another AC circuit for capacitive sensors was demonstrated in [59]. The sensor consists of polyimide membrane (top electrode) and a mixture of Cr/Au/Cr as bottom electrode. The sensor was integrated with an RC oscillator as shown in figure

2.14 below. The capacitance change was only 0.1 pF over a pressure range of 0-1 bar, resulting in an oscillation frequency in the range of 206.9- 211 kHz.

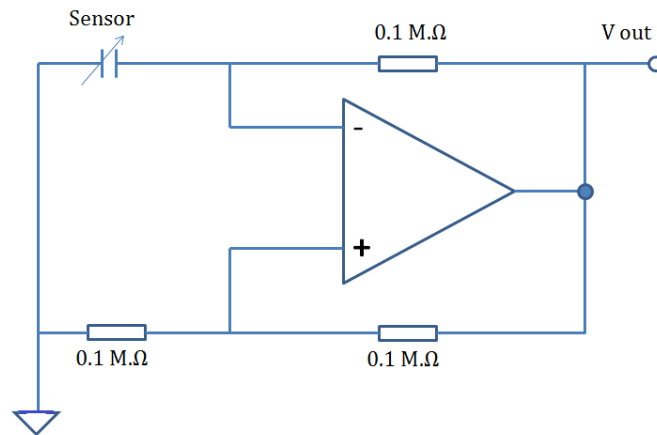


Fig. 2.14. Oscillator circuit for capacitor sensor readout [59].

A CMOS-capacitive sensor with an array of 128 cells is presented in [60] using 0.35 CMOS-technology. Each capacitor cell consists of the membrane and stationary electrode with air gap of 0.65 μm . The membrane consists of a sandwiched structure constructed on a passivation layer (Silicon nitride/ Silicon dioxide) and metal-4 as the top electrode. The bottom electrode was built on silicon substrate with metal-2. The etching holes are sealed under a vacuum chamber. The capacitance to voltage circuitry is shown in figure 2.14. The capacitance change was 10.00 pF to 10.25 pF, corresponding to a voltage variation between 270 and 550 mV. The pressure range was 0-200 kPa, which is ideal for automotive applications.

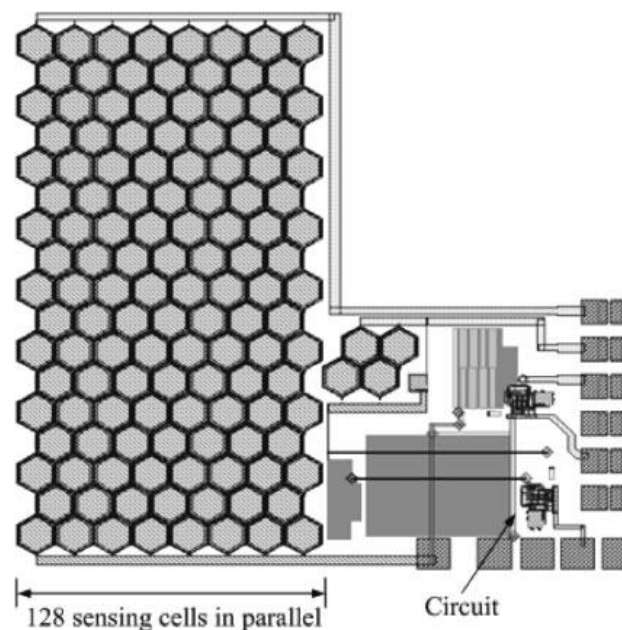


Fig.2.15. Layout of CMOS-MEMS capacitive pressure sensor [60].

As shown, capacitor sensors could be realized in full bridge configuration (usually fixed and changeable capacitors). Another sampling method (Σ - Δ converter) uses the bridge schematic to sample a very small capacitance change, typically in fF range. This technique could offer lower power consumption with small supply voltage as reported in [61]. The circuit has supply voltage of 2.2 V, and power consumption of 0.5 mW. The sensor constructed of standard capacitor provided by CMOS technology (Poly-Cap), in array of 14 capacitors connected in parallel and etched dielectric (0.4 μm silicon nitride) to create movable and static electrodes. The overall area of the device was less than 3mm², and thickness of 0.5 mm. A Σ - Δ demodulator for CMOS-MEMS capacitor pressure sensor is reported in [62].

An accelerometer and capacitor pressure sensor was fabricated on a CMOS chip using novel methods [63]. Figure 2.16 show the fabrication steps to carry out the double sided post processing. The back side of the chip was etched using dry etch. H₂SO₄ and H₂O₂ solutions were used from the back to etch through metal layers and vias to create the suspended structure. RIE isotropic etching was performed on top of the chip using XeF₂ to remove the passivation layers and dielectric layers. The capacitor plates are Metal 2 and Metal 3 of the TSMC 0.35 CMOS process. The measured device sensitivity was 12mV/kPa in pressure range between 0 and 10 kPa.

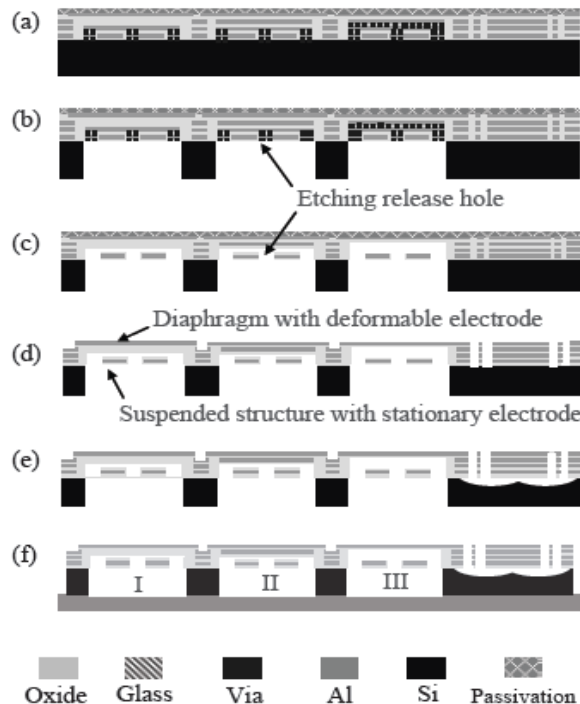


Fig. 2.16. Post processing of CMOS chip as illustrated in [63].

A monolithic capacitive pressure sensor is reported in [64]. The sensor is based on a standard CMOS process and post processing techniques. The capacitor consists of poly gate and n-well as top and bottom electrodes and poly oxide as the dielectric layer. Post processing of the chip was carried out only from the back of the chip, and unlike traditional capacitors, the middle layer was kept as part of the device. This method of sensing offers a large initial capacitance value. Sensing area was 0.64 mm^2 with sensitivity of 46Ff/hPa . The sensor was read by an integrated RC relaxation oscillator and D flip-flop with resulting sensitivity of 3.2Hz/hPa .

2.3. Wireless pressure sensors

2.3.1 Introduction

Smart MEMS devices are able to detect environmental changes (pressure, heat) first and then communicate with a base system for monitoring and analysing information. Wireless pressure sensors are widely used in biomedical and automotive applications. The automotive industry was the first to realize smart devices. The first Tyre Pressure Monitoring System (TPMS) was manufactured by Porsche in 1986. Soon after, the automotive industry, especially cars manufacturing industry was revolutionised by wireless pressure sensors, ranging from air bags to child seat detection and from seat and occupant detection to noise prevention from outside world to inside vehicles.

Physiological pressure needs to be continuously and carefully monitored to control and then treat patient health disorders. Most medical systems have their own performance specifications and integration requirements depending on the location in the body, for example, monitoring pressure in artery, retina, and intracranial. Pressure monitoring on fluids is also of an interest, for example, blood, saline, spinal fluid or others. However they feature some common typical requirements such as: small size, low power consumption or wireless powering and long-time stability. All sensors could be implemented on the same time as developed by UCL in the last five years. Figure 2.17 shows such Body Sensor Network (BSN).

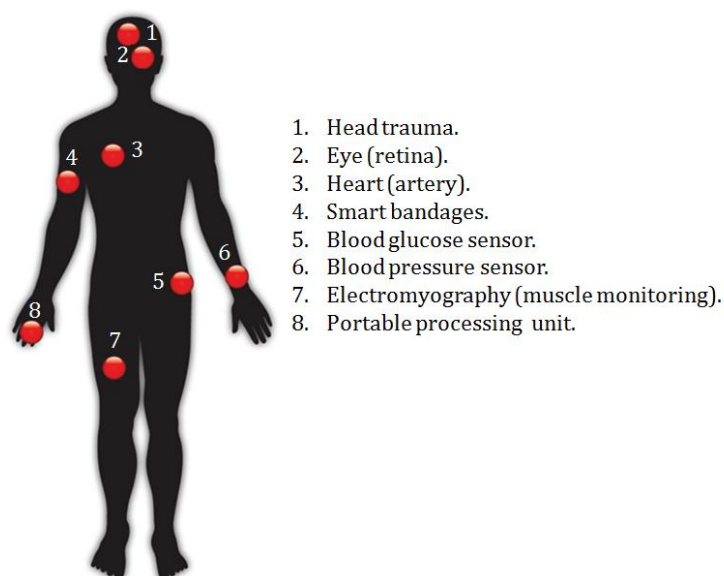


Fig. 2.17. Body sensor network for continuous pressure monitoring [65].

2.3.2 Working principles and examples

The working principles for wireless pressure sensors are illustrated in figure 2.18 below:

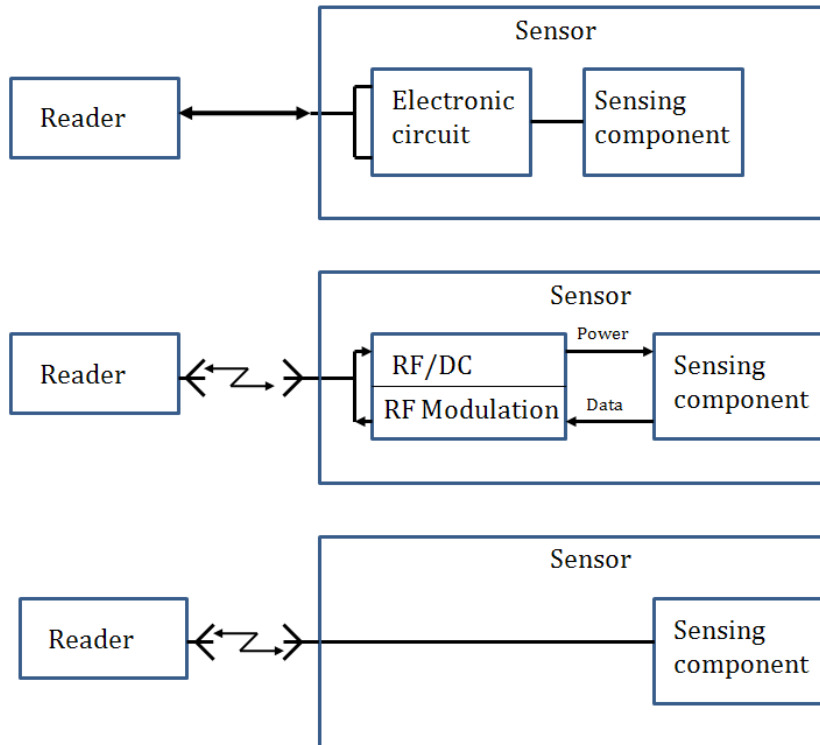


Fig.2.18. Working principle of conventional, active and passive telemetry sensors.

In the conventional method, the read out circuit is usually in the same package or in close proximity to the sensing element. However, integrating the sensor with the readout circuit on the same die is preferable as we will discuss later due to the lower parasitics introduced by wires necessary for off chip readout. The readout circuit could be powered by a battery (wired) or remotely (wireless) by an active or passive telemetry system. The use of a passive pressure sensor is more attractive due to limitation of life time, power, and chemical stability of batteries.

Wireless passive and active pressure sensors are widely used in biomedical applications [66-69]. In an active system, the sensor will be connected to an electronic circuit that requires power to operate its component parts. In a passive system, the sensor will be limited to simple components such as inductors and capacitors, and will need no power.

Active systems are desirable where communication is needed over relatively long distances, or sophisticated wireless technology is required.

An example of an active telemetry pressure sensor with external transmitter is reported in [70]. The device consists of a capacitive type sensor used to tune a Colpitts oscillator as illustrated in figure 2.19.

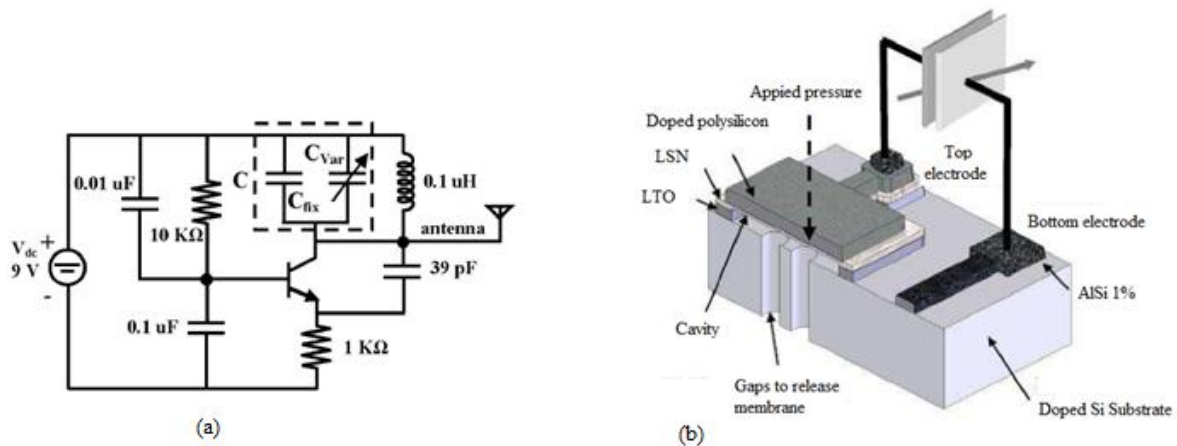


Fig.2.19. Common emitter Colpitts oscillator used in the experiments. C-var is the applied differential pressure (a). (b) 3D-sketch of MEMS capacitor sensor [70].

The change in capacitance was measured between 17.84 and 18.8 pF for pressure range between 0 and 200kPa. This change in capacitance automatically changes the oscillation frequency between 85.5 and 86.7 MHz, for a measured pressure range between 0 and 140 kPa as shown in figure 2.20.

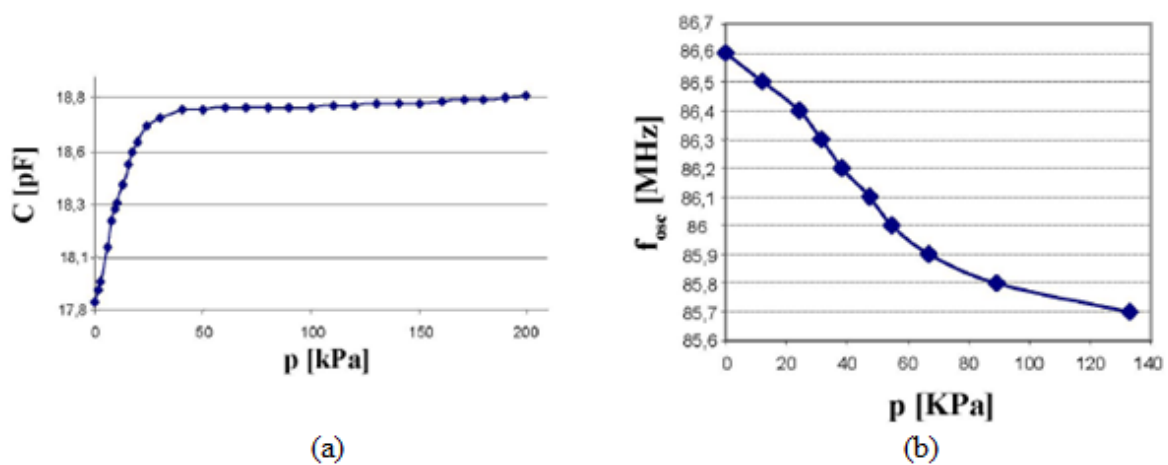


Fig. 2.20. Capacitance change (a) and frequency change with pressure (b) [70].

A wireless implantable cardiovascular pressure monitor integrated with a medical stent was designed and developed using an application-specific integrated circuit (ASIC), designed and fabricated on Texas Instruments 130-nm CMOS process [71]. The sensor uses an external power source of 35 dB.m over 10 cm distance. The pressure resolution was 0.5 mmHg over a range of 0–50 mmHg. The sensor type was a capacitive as a part of a differential cross coupled MOSFETS with active current source as shown in figure 2.21.

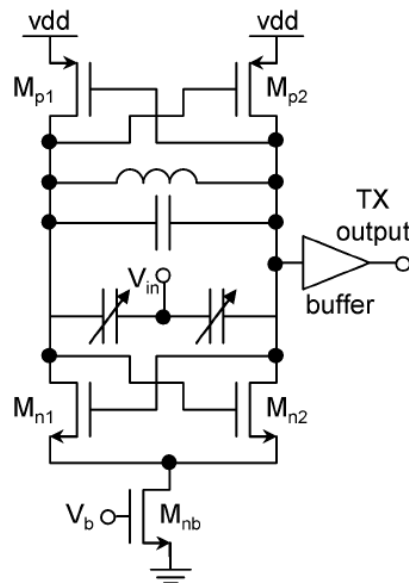


Fig 2.21. Variable capacitors as a part of Cross coupled oscillator [71].

An active pressure sensor on 0.35 CMOS technology from TSMC was reported in [72]. The sensor was realized using post process techniques which employed the etchants to etch the sacrificial layers to release the membranes of the pressure sensor, and then the etch holes in the pressure sensor were sealed by the LPCVD parylene. The system works as follows: the sensor was the gate of NMOS transistors, which is constantly supplied by an AC signal from an oscillator. The signal changes with pressure amplified and then transmitted using a loop antenna as shown in figure 2.22.

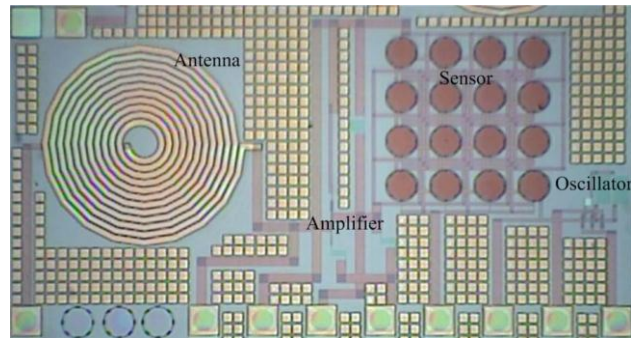


Fig.2.22. A SEM microphotograph of wireless pressure sensor [72].

The pressure sensor had a sensitivity of 0.08 mV/kPa in the 0–500 kPa pressure range and a wireless transmission distance of 10 cm.

Many applications require that sensors should operate on little or no power consumption over extended in-service periods. This is particularly challenging for wireless devices.

Usually passive pressure sensors are inductively coupled capacitor sensors. An electroplated gold (Au) coil behind a thin polysilicon membrane was reported in [73]. The conductor behind the membrane is used as the fixed part of capacitor sensor as illustrated in figure 2.23.

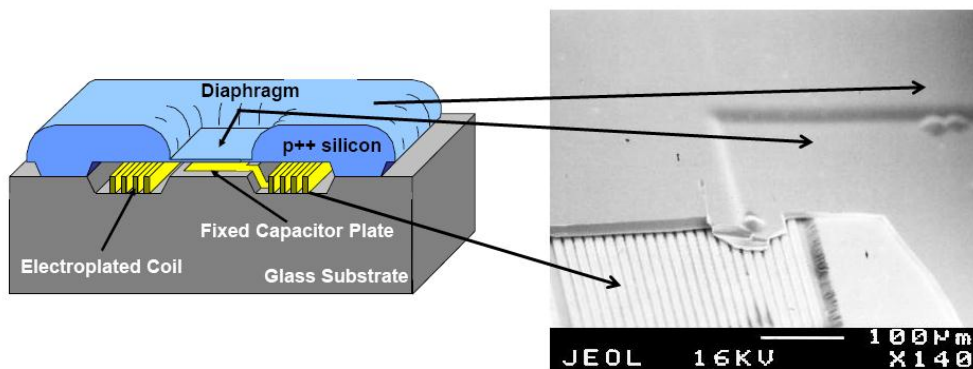


Fig. 2.23. Structure of wireless pressure sensor and a SEM photograph of the fabricated sensor, which is broken to show the electroplated coil inside the sealed cavity [73].

The resonance frequency of the system is given by:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (2.13)$$

The measured change in resonant frequency was between 63 and 76 MHz for pressure range between 0 and 100 mmHg.

An operating system reported in [74] consists of a capacitive pressure sensor, performing pressure to frequency conversion and a spiral loop functioning as an inductor for the LC tank and as a transmitting antenna. A GaAs photodiode is employed to convert the laser beam into electrical energy for powering the device as illustrated in figure 2.24

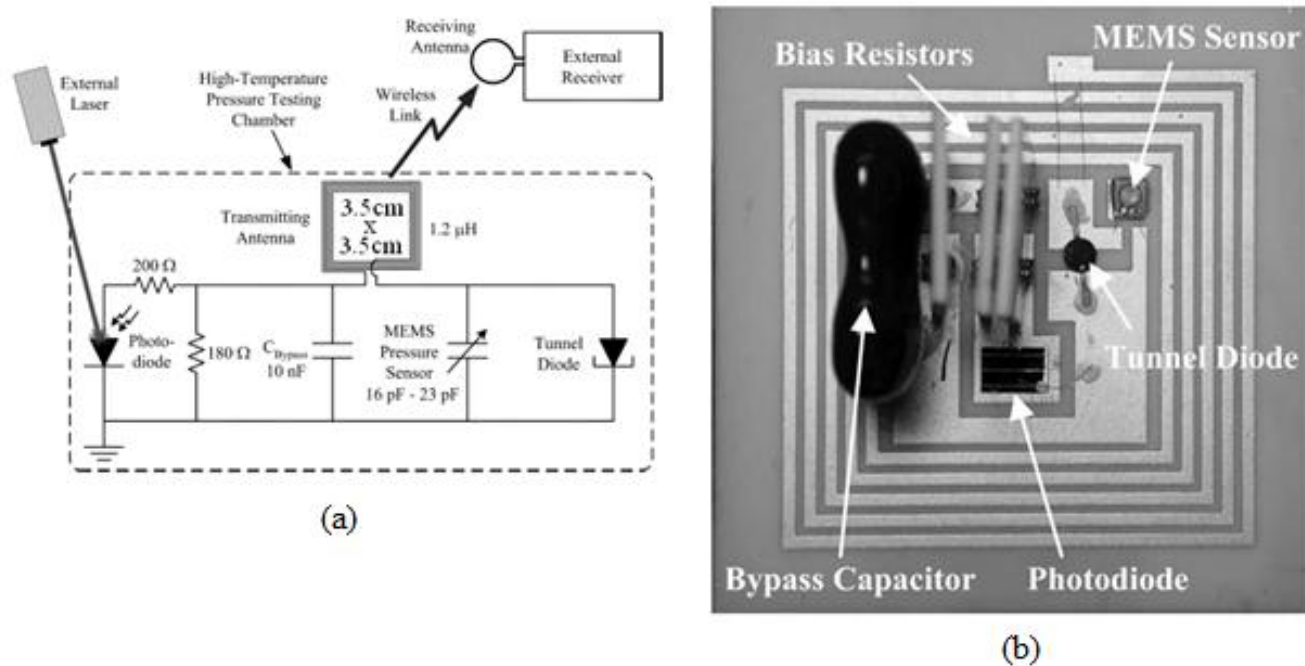


Fig. 2.24. Working principle of the sensor (a) and a photograph of prototype (b) [74].

The device works between 5-35 psi pressure range, and frequency change between 23.5 - 21 MHz and could operate distance of 1.5m with relatively high temperature (240 °C).

A battery free wireless pressure sensor was demonstrated in [75]. The sensor was fabricated through photolithographic methods on DuPont Pyralux AC singleside copper-clad laminate which is an all-polyimide composite of a polyimide thick film on a copper foil with substrate and rolled-annealed (RA) copper foil thickness of 25 μm and 118 μm respectively. The copper foil is coupled with the sensor as an inductor and transmitting the signal at the same time. The capacitor sensor is formed as an interdigitated set of linear parallel electrodes coated with Polyvinylidene Fluoride (PVDF) pressure sensing material on the top. Figure 2.25 shows the sensor and the external coil.

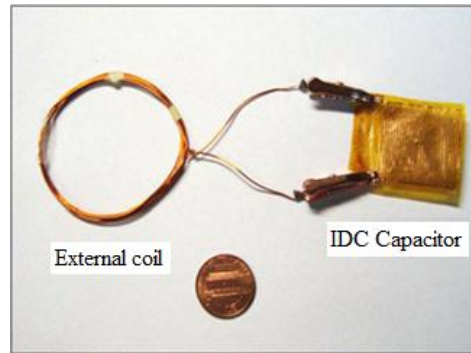


Fig. 2.25. Interdigital pressure sensor with external coil [75].

The sensor performs in the range of 0-60 psi and device sensitivity of 25 kHz/psi.

A pressure sensor working at microwave frequencies is reported in [76]. The sensor works on the principle of electrodynamic transduction. The sensing element is a flexible high resistivity silicon membrane located above a coplanar quarter-wavelength resonator operating in Ka-band (26.5 to 40 GHz). Figure 2.26 shows cross section and 3D sketch of the sensor

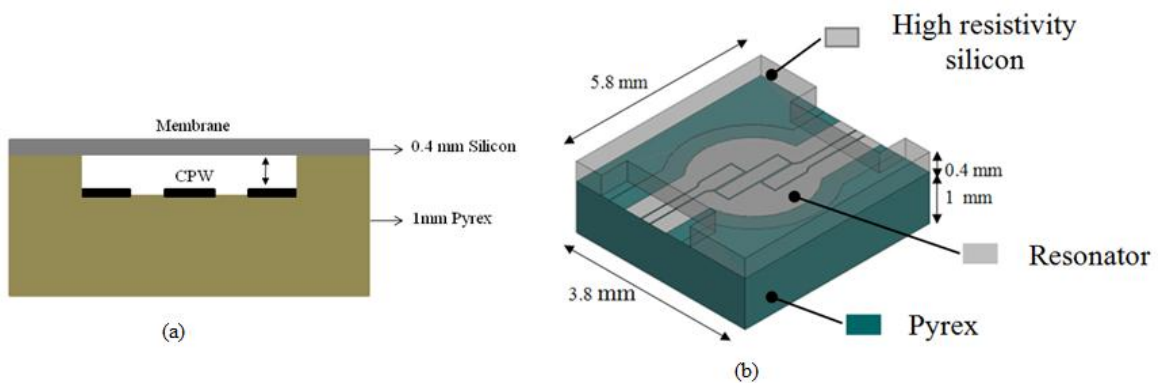


Fig. 2.26. Cross section of the sensor (a) and (b) 3-D view [76].

The measurement results show a resonant frequency change between 27.5-35 GHz for a distance range of 0-60 μm and an overall sensitivity of 370MHz/bar. However, the thickness of the membrane plays a major part in the sensitivity of the device as illustrated in figure 2.27 below.

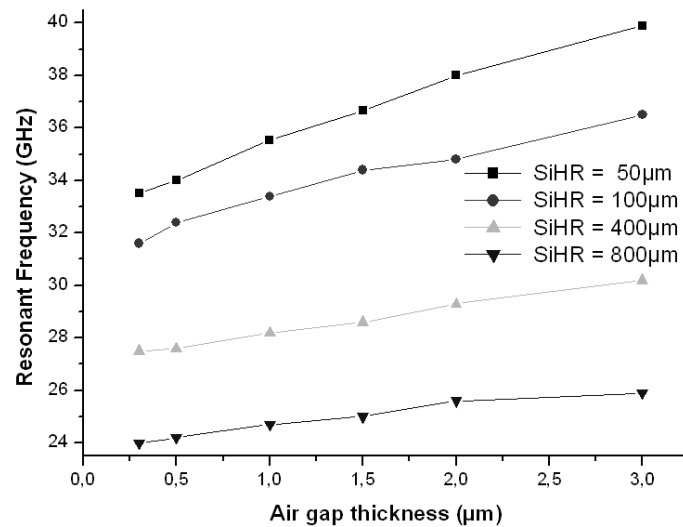


Fig. 2.27. Resonant frequency shift for different membrane thicknesses [76].

A wireless working distance of 100 mm for passive pressure sensors for biomedical applications was reported in [77]. The sensing method was capacitive, coupled with an inductor, which was used as a transmitter. An insulating layer of silicon on glass (SOG) was introduced between the capacitor upper electrode and a high resistivity silicon substrate. The pickup signal processing unit was constructed of MMIC LNA and printed multi loop antenna on Duroid substrate. Figure 2.28 shows the working principle of the sensor.

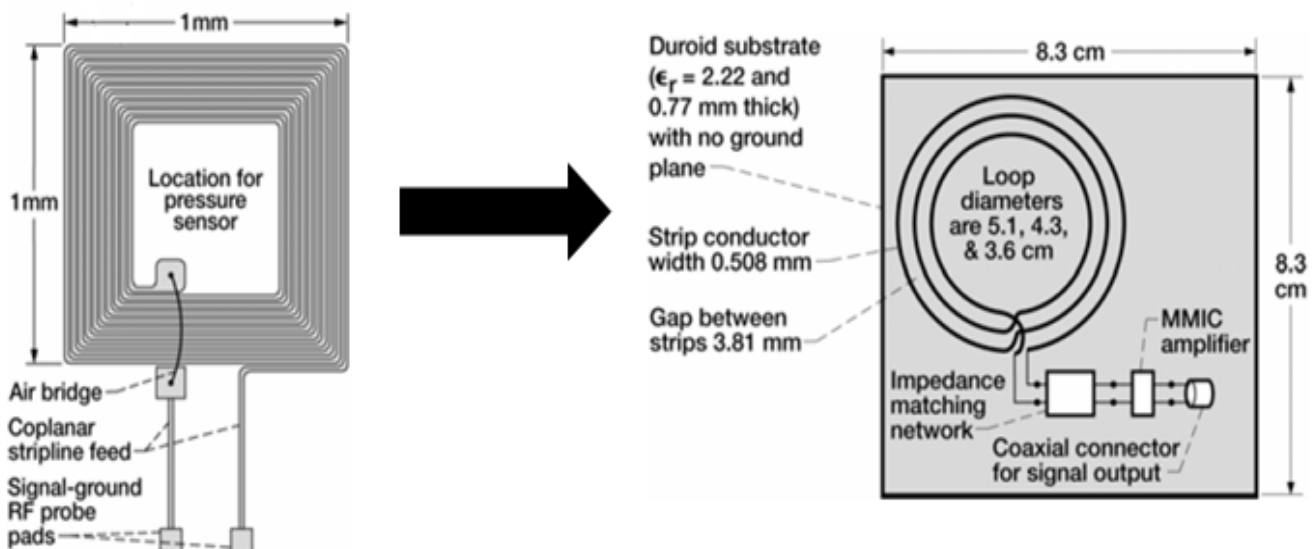


Fig. 2.28. Passive sensor and receiver [77].

The changing capacitance was observed between 0.5–4.0 pF (changed by pressure), leading to a fall in resonant frequency from 670 to 230 MHz ($L=153\text{nH}$).

A novel device, working at communication link at 32 GHz was reported in [78]. The resonator consists of a stacked-patch based on LTCC multilayer packaging technology. The air cavity embedded by a silicon diaphragm deflects due to pressure change. The transducer provides frequency operation between 47-55 GHz. Another prototype was reported by same authors in [78]. The sensor works in a frequency range between 5-8 GHz with improved approximation of silicon membrane deflection. The transmitting part was realized by a patch antenna.

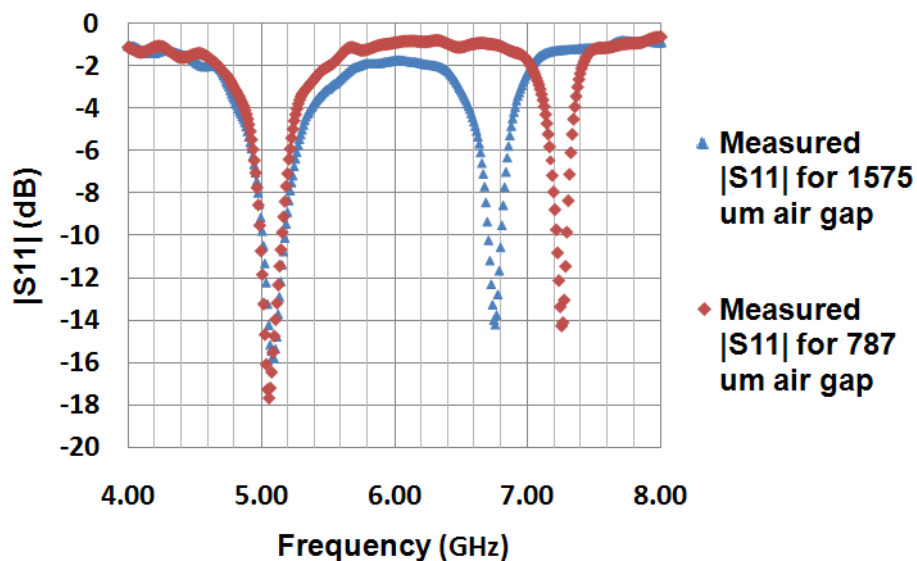


Fig. 2.29. Measured resonant frequency shift with deflecting silicon membrane [78].

Two bio-implantable RF-MEMS strain sensors were demonstrated in [79]. Both sensors were fabricated on low loss and high dielectric constant ($\epsilon_r=8$) Si_3N_4 . The first sensor has dimensions of 340 μm length and width in a coil shape with tow turns resulting in an inductance of 2.84 nH. The second sensor length and width are 270 μm with same number of turns as first sensor. The metallization was chosen to be silver as it is bio-compatible, with thickness of 0.1 μm . Figure 2.29 shows one of the sensors in addition to receiving and transmitting antennas.

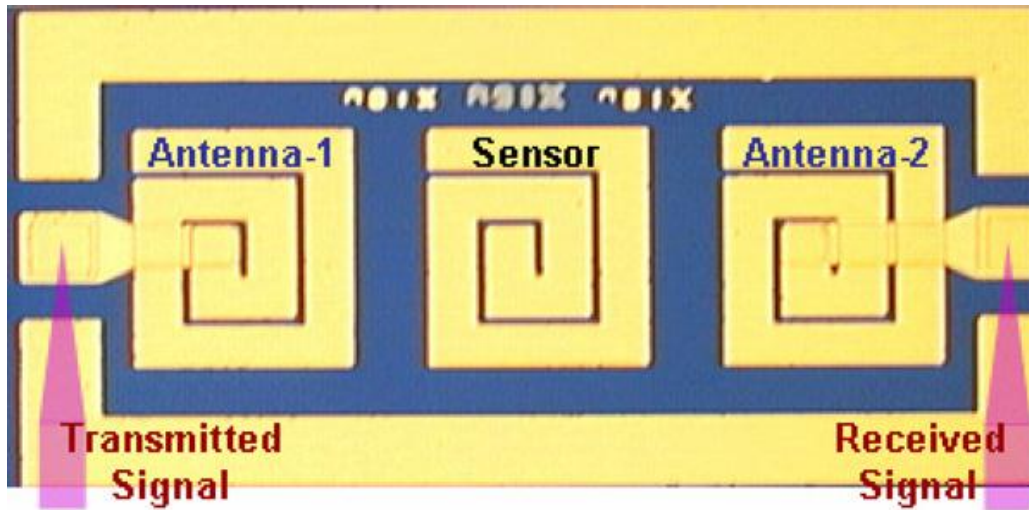


Fig. 2.30. Sensor with on chip antennas for communication. The sensor area is $270 \mu\text{m}^2$. [79].

Different loads were applied to the sensor and resonant frequency shift for the bigger device was 360 MHz for an initial working frequency of 11.5 GHz. The smaller device frequency shift was 330 MHz for an initial working frequency of 13.6 GHz. The loads applied for both sensors range from 0 to 3500 Newtons. An improved quality factor with applied load was observed at the same time.

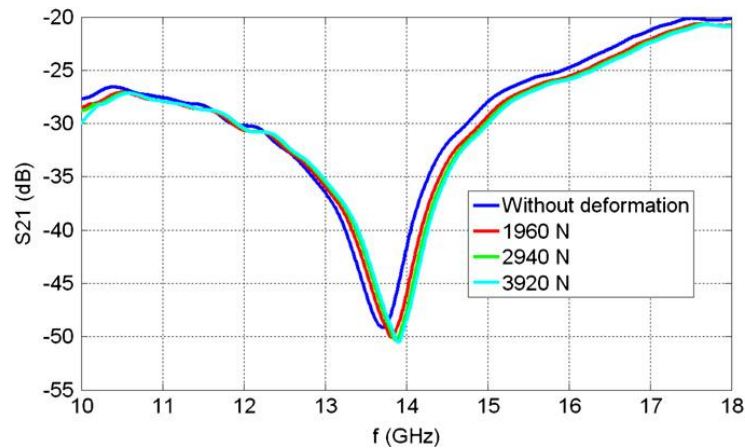


Fig. 2.31. Telemetry measurement of the sensor as shown in [79].

A double sided single chip wireless pressure sensor is demonstrated in [80]. The device implements a double-sided (SOG) process integrating a high-Q inductor and a capacitive pressure sensor on opposite sides of a glass substrate. The device length and width are 0.6 mm and thickness of 0.5 mm. The working distance of the sensor was measured at 3

cm with sensitivity of 3.2 kHz/mmHg for pressure range between 400 and 1000 mmHg. The resonant frequency change was measured between 13 and 11.2 MHz.

2.4 Summary

Most of silicon based pressure sensors use piezoresistive, capacitive, and resonant sensing elements. Piezoresistive pressure sensors are widely used due to linearity and ease of fabrication. Resonant pressure sensors are problematic due to complexity of fabrication, but they offer more prospect if a piezoelectric material is used. Capacitive pressure sensor is more sensitive with only drawback of nonlinearity. Integrating the pressure sensor with active circuitry (CMOS-MEMS) on the same chip has revolutionized the biomedical and automotive markets in terms of mass production and cost.

Wireless pressure sensors are widely used in several applications and continuously on the rise. Silicon based devices offer more prospect due to low cost, and the rapid growth and advance of MEMS technology. The increasing demand for longer life operation of devices has increased the demand for passive telemetry systems, with operational frequency in MHz and even up to several GHz.

Chapter 3

3. On Chip Antenna

3.1. Introduction

Until recently, a traditional antenna implementation on MMICs for co-design with radio frequency front end circuitry would be designed separately from the electronics and manufactured in a different production technology and integrated with the radio frequency electronics through standard connectors and impedance transformers. However, moving towards the higher frequencies of Gigahertz and even Terahertz requires a re-think of the packaging and interconnects. The high demand for smaller, faster, and low cost transceivers working in short range communication and sensor applications means this is becoming an increasingly more significant issue.

Furthermore, rapid progress in CMOS technology now allows for entire receivers and transmitters to be implemented on a single semiconductor chip, and antennas working from 7.4 to 77 GHz have been reported in [81-83].

The free space wavelength of radiated signals is relatively large compared to the typical chip sizes of integrated circuits, for example, a CMOS die of less than 13 mm² was reported for a frequency operation of 10 GHz ($\lambda_0 = 30\text{mm}$ in free space) [84], considering this reported size is for both the front end circuitry and antenna.

In this chapter we define basic antenna parameters, types of antennas used in MEMS and CMOS technology, and methods used to improve the performance of antenna against losses caused by the silicon substrate. Also, we show some antenna parameters, on antenna design consideration, an overview from literature for on chip antenna types, and lastly we introduce the antenna used in this thesis.

3.2. Antenna overview and parameters

An antenna acts to convert guided waves on a transmission line into waves in free space. We can also say that antennas are reciprocal devices which behave the same when transmitting or receiving. In the receiving mode, antennas tend to collect incoming waves and direct them to a common feed point where a transmission line is added. We can find similarity with, for example, an optical wave focused through a lens, where the antenna acts as the lens, focusing the electromagnetic waves. In this section, we define some of the antenna parameters.

3.2.1. Radiation pattern

Radiation patterns describe the spatial distribution of electromagnetic energy intensity S at a given distance r from a transmitting antenna. The same pattern also describes that antenna's directional response to an incoming (received) signal over the same space. An example of a radiation diagram for an antenna, showing main beams and side loops, can be seen in Figure 3.3. This pattern shows a single narrow main beam. Antennas with such capabilities are often used in point-to-point communication. In contrast, antennas with omnidirectional radiation characteristics (in one plane, at least) are often used for broadcasting.

An alternative radiation pattern is a plot of the far-field radiation properties of an antenna, the spacial co-ordinates being defined by the elevation (θ) and azimuth (ϕ) angles. Basically this is a radiation intensity plot in three-dimensional space, being the power radiated in each direction (defined by θ and ϕ).

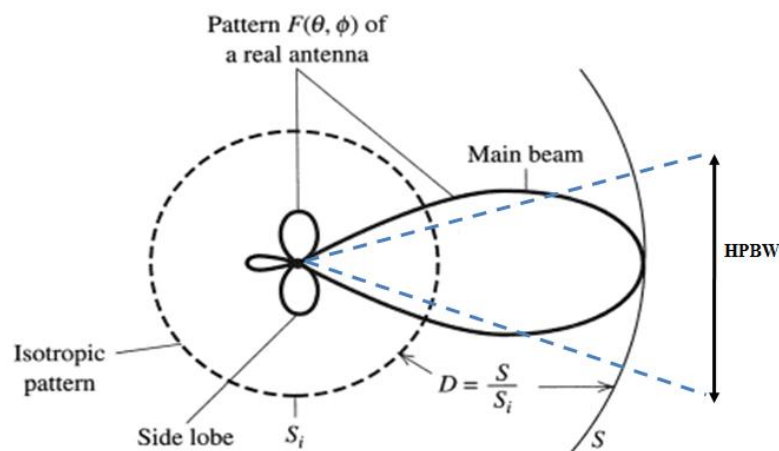


Fig. 3.1. Radiation pattern of a directional antenna.

Consider an isotropic antenna, which radiates equally in all directions. We can define the total power radiated by this antenna as P , where this power is spread over a sphere of radius r . The radiation density S at this distance in any direction is given as

$$S = \frac{P}{Area} = \frac{P}{4\pi r^2} \quad (3.1)$$

The radiation intensity could be written as:

$$S_i = \frac{P}{4\pi} = r^2 S \quad (3.2)$$

From figure 3.3 we can distinguish:

- Main Lobe: This is the radiation lobe containing the direction of maximum radiation.
- Side Lobes: These are the minor lobes adjacent to the main lobe and are separated by various nulls. Side lobes are generally the largest among the minor lobes.
- HPBW The (half power beam width) can be defined as the angle subtended by the half power points of the main lobe.

In most wireless communication systems, side lobes are undesired and should be minimised for a good design.

3.2.2. Directivity

The directivity D of an antenna expresses how much greater the peak radiated power density is for an antenna in comparison to the evenly distributed power from a theoretical ideal isotropic antenna. D can be expressed as follows:

$$D = \frac{S}{S_i} = \frac{4\pi S}{P} \quad (3.3)$$

Where S is the radiation intensity of the antenna, S_i represent radiation intensity of an isotropic source (figure 3.2), and P is the total power radiated from the source.

Sometimes, if the direction of directivity is not specified, the direction of the maximum radiation intensity is implied and the maximum

$$D = \frac{S_{max}}{S_i} = \frac{4\pi S_{max}}{P} \quad (3.4)$$

Directivity is a dimensionless quantity, since it is the ratio of two radiation intensities. Hence, it is generally expressed in dBi. The directivity of an antenna can be estimated from the radiation pattern of the antenna. An antenna with a narrow main lobe has better directivity.

3.2.3. Gain

Gain G is the directivity of an antenna once antenna losses have been taken into consideration. From this definition we can see a direct relation to directivity. We know that directivity is how much antenna concentrates energy in one direction in preference to radiation in other directions. If an antenna radiates all its energy in one direction then the directivity would be equal to the antenna gain and the antenna would be an (ideal) anisotropic radiator.

Since all antennas radiate more in some directions than in others, gain is therefore the amount of power that can be achieved in one direction at the expense of power lost in the other direction. This gain is normally related to the main lobe and is specified in the direction of maximum radiation unless indicated. The relationship between gain and directivity can be written as:

$$G(\theta, \phi) = eD(\theta, \phi) \quad (3.5)$$

3.2.4. Impedance

The input impedance of an antenna is simply the ratio between the voltage and current at the antenna terminals. The ultimate goal is to match an antenna's input impedance to the characteristic impedance of its connecting transmission line. The input impedance of an antenna is expressed by:

$$Z_{in} = R_{in} + jX_{in} \quad (3.6)$$

Z_{in} is the antenna impedance at the terminals, while R_{in} and X_{in} are resistance and reactance of the antenna respectively. The imaginary part X_{in} of the input impedance represents the power stored in the near field of the antenna, whereas the resistive part R_{in} of the input impedance consists of two components, the radiation resistance R_r and the loss resistance R_l . The power associated with the radiation resistance is the power actually radiated by the antenna, while the power dissipated in the loss resistance is lost as heat in the antenna itself due to dielectric or conducting losses.

Frequently, an improvement in one parameter will significantly and adversely affect one or more performance parameter. The real challenge when designing an antenna is to try to enhance all performance parameters simultaneously. Table 3.1 summarises the main antenna parameters.

Usually, an improvement in one parameter will significantly affect one or more performance parameter. Therefore, it is challenging to design an antenna with enhanced performance for all parameter on the same time.

Parameter	Definition
Radiation pattern $(F(\theta, \phi))$	Angular variation of radiation around the antenna including directive, single or multiple narrow beams Omindirectional Shaped main beam
Directivity D	Ratio of power density in the direction of the pattern maximum to the average power density at the same distance on the antenna
Gain G	Directivity reduced by losses on the antenna.
Polarization	The figure traced out with the time by the instantaneous electric field vector associated with the radiation from an antenna when transmitting. Types: Linear, Circular, Elliptical
Impedance Z_A	Input impedance at the antenna terminals
Scanning	Movement of the radiation pattern in free space. Scanning is accomplished by mechanical movement of the antenna in certain direction
System considerations	Size (on chip antenna), environmental conditions, radar cross section

Table.3.1. Some antenna parameters.

3.3 Antenna types

Antennas can be divided into four basic types according to their performance parameter. Historically, researchers divided antennas into different categories for more grasp on specific performance parameter. Table 3.2 shows the antenna types with simplified figures in the order that they are used across the radio spectrum.

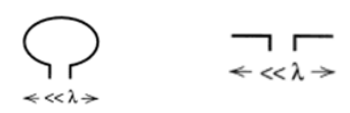
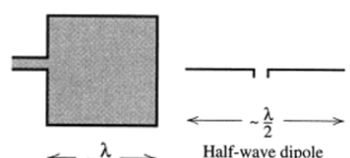


Antenna type	Properties	Example
Electrically small antenna	Very low directivity Low input resistance High input reactance Low radiation efficiency	 Small loop short dipole
Resonant antenna	Low to moderate gain High input resistance Low input reactance Narrow bandwidth	 Microstrip patch Half-wave dipole
Broadband antenna	Low to moderate gain Constant gain High input resistance Low input reactance Wide bandwidth	 Spiral
Aperture antenna	High gain increase with frequency Moderate bandwidth	 Aperture Horn

Table 3.2. Main antenna types.

Electrically small antennas are much less than a wavelength in extent, simple in structure and their properties are not sensitive to construction details.

Resonant antennas are a popular choice when a simple structure with excellent impedance matching over a narrow band of frequencies is required. Such antennas have a broad main beam and low moderate gain. The half wave dipole is the best example of a resonant antenna.

A broadband antenna is used in applications which require a wide frequency range, and has an acceptable performance in terms of pattern, gain and impedance. The spiral antenna is a good example of this type of antenna.

Aperture antennas have an opening through which propagating electromagnetic waves flow. An example is the horn antenna, directing the wave into the connecting waveguide. The aperture is usually several wavelengths long in one or more directions. This type of antenna has high gain, and moderate bandwidth.

3.4. Micromachined antennas

As mentioned, designing for high frequency applications brings a greater challenge of overcoming dielectrics losses and interconnect issues. Several approaches have been demonstrated to overcome these losses. These approaches involve increasing the metallisation of the transmission line and antenna, and maximising the portion of the field that is in the air.

For losses caused by substrate dielectrics, the geometry of the planar silicon chip could be modified. Micro-Electro-Mechanical-Systems (MEMS) technology offers the opportunity of modification either by the addition of layers or bridges to distance the antenna from the substrate, or by removing a substantial amount of the substrate (membrane technology). On top of the silicon die, material with a lower dielectric than silicon could be added, for example silicon dioxide and silicon nitride. Other materials could be added such as polymers, and material could be added to form micro-bridges and micro-beams.

Bulk micromachining is used to remove a large amount of lossy silicon usually by backside etching. However a combination of surface and bulk micromachining is used is commonly used to form membranes of dielectric materials. Such membranes have

found uses for transmission lines, inductors and antennas where the substrate losses are minimized by suspending the printed metallic conductors in air.

The addition of polymer at the top of silicon substrate has been demonstrated in [85]. Figure 3.2 shows a simple way of reducing the losses of passive microwave components manufactured on low resistivity silicon wafers. Benzocyclobutane (BCB) is a popular polymer which could be specifically developed for microelectronic manufacturing. BCB has low losses and relatively low dielectric constant $\epsilon_r = 2.65$ compared to silicon (11.9). The addition of BCB on silicon wafers is highly repeatable and the thickness could easily reach between 20~30 μm . The polymer is highly compatible with photolithography processes and multiple vias could be fabricated to contact the active of the wafer. This technique of dielectric low loss and higher distance from silicon wafers was successfully demonstrated in [86] to improve the quality factor of a suspended inductor.

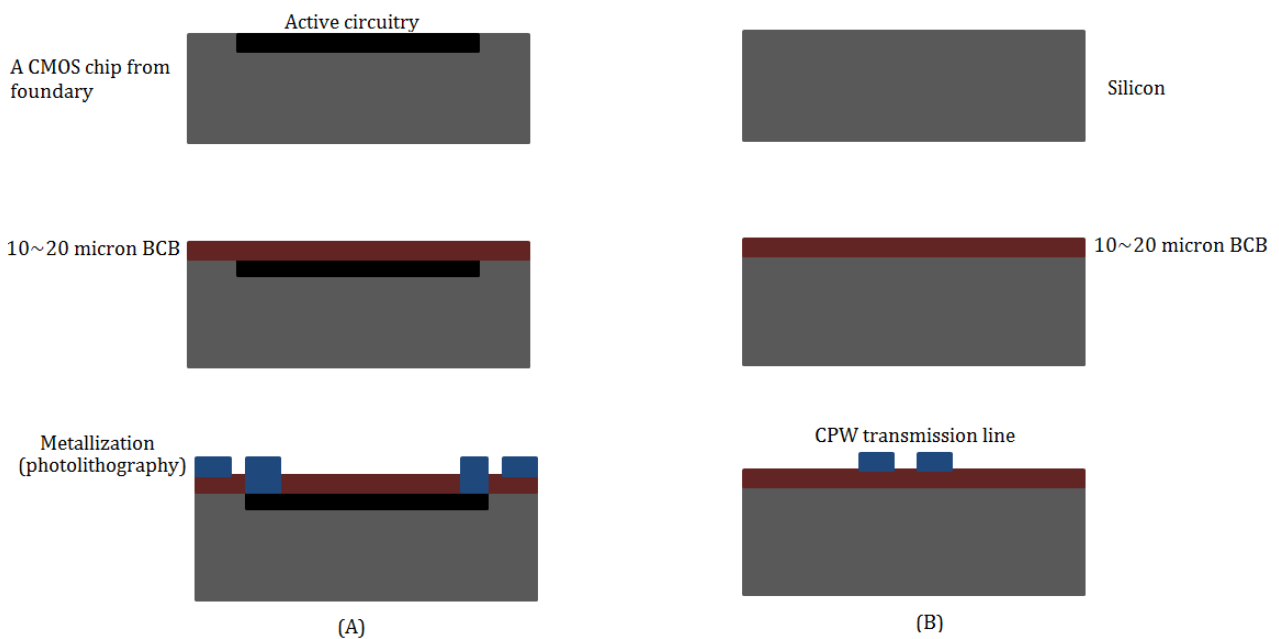


Fig.3.2. (A) Post-processing of CMOS chip and (B) adding BCB on plane Si wafer.

3.4.1. Design consideration

It is very difficult to design on chip antennas with high gain and high directivity due to the practical small size limitations in manufacturing silicon. Other parameters such as efficiency return loss and bandwidth, depending on application, become important. The radiation efficiency is given by [87]:

$$\eta = \frac{p_{rad}}{p_{Accepted}} \quad (3.7)$$

For on chip antennas, the losses caused by the dielectric material are a major factor for low efficiency. As silicon is a nonmagnetic material (permeability $\mu = \mu_0$), the microwave properties of the material is the complex permittivity, which can be written as

$$\epsilon_r \epsilon_0 = \epsilon' - j\epsilon'' \quad (3.8)$$

ϵ_r ranges between 11.7-11.9 at microwave frequencies, and the permittivity of free space ϵ_0 is equal to 8.85×10^{-12} F/m. The high permittivity of silicon is a huge advantage for on chip antennas, thus allowing for size reduction resonant radiators. The factor of $\tan \delta$ represents the ratio of the conduction to displacement currents in the dielectric. The higher the value $\tan \delta$ indicates more losses caused by heat caused by the presence of electric field on material. The effective conductivity is defined as follows:

$$\sigma_e = \sigma_s + \sigma_a \quad (3.9)$$

σ_s and σ_a represents the static and alternating conductivity. σ_a Occurs due to alternating current presence with time-varying electric field. The time variation of the electric field is assumed to be harmonic and represented by the angular frequency ω .

For a low resistivity, loss tangent will be dominated by the static conductivity losses represented by $\tan \delta_e$ and could be approximated by

$$\tan \delta_e \approx \frac{1}{\epsilon' \omega \rho} \quad (3.10)$$

Where ρ is the resistivity of the dielectric. Equation (3.10) is extremely important for designing on chip antenna and microwave resonators. The higher the resistivity of the material the lower loss is expected. The resistivity of CMOS chips usually ranges between 1 and 50 $\Omega \cdot \text{cm}$. For plan silicon wafers a resistivity of 10K $\Omega \cdot \text{cm}$ could be manufactured. This is carried out by reducing the amount of dopant atoms to wafer.

Additional emphasis must be placed on the control of dopants (boron and phosphorous) introduced from the raw materials and components used in the crystal puller. The dopants are tightly controlled by graphite heater and transferred to, and through, the boundary layer of the wafer exactly at the melt-solid interface important for achieving acceptable radial resistivity variation. A very high resistivity Silicon (in the range of 1.6 M Ω .cm) proton and As⁺ are used for implantation as reported in [88].

The thickness of the substrate is crucial for designing on chip antennas. The general rule is derived for antennas on grounded substrates (dipole, patch) [89], the cut off frequency f_c for substrates modes $n=0, 1, 2, \dots$ can be calculated as

$$f_c = \frac{nc}{4d\sqrt{\epsilon_r - 1}} \quad (3.11)$$

Where c is the speed of lights and d is the substrate thickness. When $n=0$ the mode will always propagate, and will be smaller if the substrate is thin enough compared to free space wavelength λ_0 . To ensure no excitation of any higher mode, a thin substrate should be selected so that the cut off frequency for mode $n=1$ is above the frequency of operation.

3.4.2. A review of micromachined-CMOS antennas

3.4.2.1 The Patch

Most of micromachined antennas are patch type. An example for such an antenna is demonstrated in [90] with reported operation frequency of 9.07 GHz. The first method is using SiO₂ membrane with a planar antenna on top. The second technique involves etching a cavity and filling it with silicon dioxide or polymer.

A 16 GHz patch antenna suspended on a 254 μm thick high resistivity silicon substrate and backed by a micromachined low resistivity wafer [91]. The actual membrane is the low conductivity of silicon and micromachining was introduced to suppress substrate modes and to improve the bandwidth of the antenna.

A direct comparison between patch antennas of the same dimensions between high and low resistivity silicon substrates has been demonstrated in [92]. In both cases a membrane behind the antenna were simulated to evaluate the performance of both antennas. The first antenna, built on high resistivity substrate, showed an efficiency of 97% compared to 39.1% for that on low resistivity substrate.

The advantage of the micromachined patch is mainly its characteristic high directivity and the absence of a back lobe, which significantly facilitates packaging of an implemented device. However, a patch antenna is a space-consuming radiator, particularly if implemented on a micromachined membrane with the resulting low effective permittivity of the substrate. An example of large area disadvantage of the patch was demonstrated in [93], where the antenna was fabricated separately on high resistivity silicon and integrated with 0.18 CMOS chip at working frequency of 5.7GHz.

The high directivity of the patch allows for integration with 0.13 CMOS circuitry at V band (60 GHz) as demonstrated in [94].

3.4.2.2. Yagi-Uda

Antenna arrays are commonly used to improve directivity. Such arrays with direct connections to each element using a feed network can be simplified if only a few elements are directly fed. The array is called a "parasitic array" and receives excitation from the near-field coupling of driven elements. Such antennas are called Yagi-Uda antennas, and have a wide range in communication applications (for example, television aerials). End fire Yagi-Uda antennas have generated extensive research on silicon wafers and membranes for high frequency applications.

A Yagi-Uda antenna on $\text{SiO}_2/\text{Si}_3\text{N}_4$ membrane supported by 350 μm silicon substrate was demonstrated in [83]. The antenna operates at 77 GHz and showed good reflection coefficient. Figure 3.3 shows a microphotograph of the front and backside of the antenna.

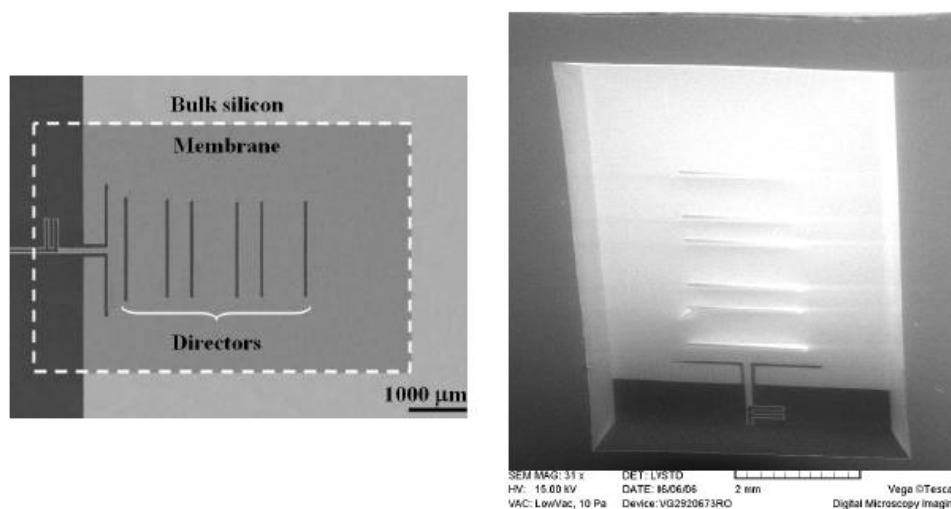


Fig.3.3. Front and backside microphotographs of a Yagi-Uda on chip antenna [83].

A Yagi-Uda antenna was fabricated on a silicon substrate using surface micromachining [95]. The antenna operates at 100GHz, and offers the advantage of limited surface waves, which would negatively affect the performance of the antenna. Its 5 element structure shows a -10dB impedance bandwidth of 12% and a directivity of 8.2dBi at 100GHz.

A similar antenna type was designed and fabricated on 0.18 CMOS technology [96]. Such a device allows a simple CPW-to-coplanar strip-line feed transition and the first metal layer implements a reflector strip. It operates at 60GHz and has maximum antenna power gain of -10 dBi.

The Yagi-Uda on-chip is a highly directional antenna. However, like patch antennas, they tend to consume a large area of silicon die.

3.4.2.3. Square loop Antenna

The square loop antenna could be a good candidate for on chip antennas. This is due to the square shape of the silicon chip when the free space wavelength at the required frequency is larger compared to chip area. However the area inside the loop should be effectively used to accommodate radio frequency front end circuitry [97] as shown in figure 3.4.

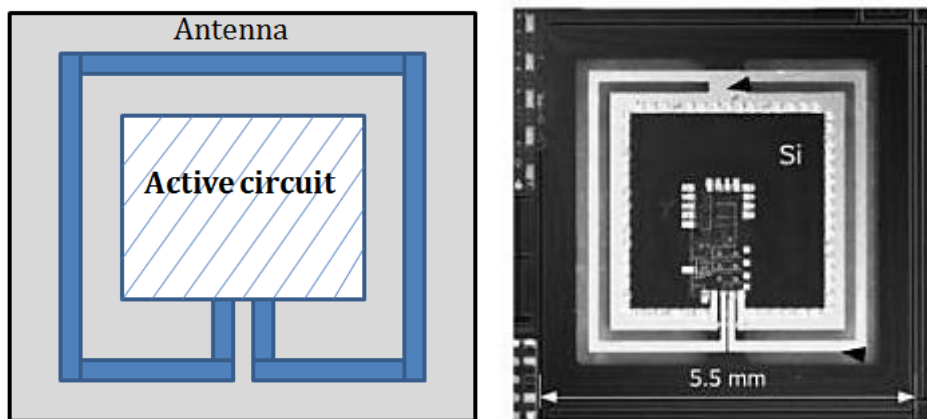


Fig. 3.4. On chip implementation of square loop antenna [97].

The square loop is easy to design since one side length of the square is approximately quarter of a wavelength in free space, and hence, the square loop operates at full wavelength operation frequency.

An example of a micromachined square loop antenna was illustrated in [98]. The antennas operate at frequency 24 and 29.5 GHz with areas of 4.8 x 4.8 and 3.6 x 3.6 mm². Trenches were introduced to minimize the losses caused low current flow on the

ground-plane in the centre of the slot loop as shown in figure 3.5. The membranes were realized using BCB polymer and SiO₂/Si₃N₄ membranes. Further two silicon bridges used for mechanical support of the centre of the substrate. These bridges placed at the maximum expected current (feed point and opposite side of the loop). The measured gain was 1.5 and 1 dBi at frequencies 29.5 and 24 GHz.

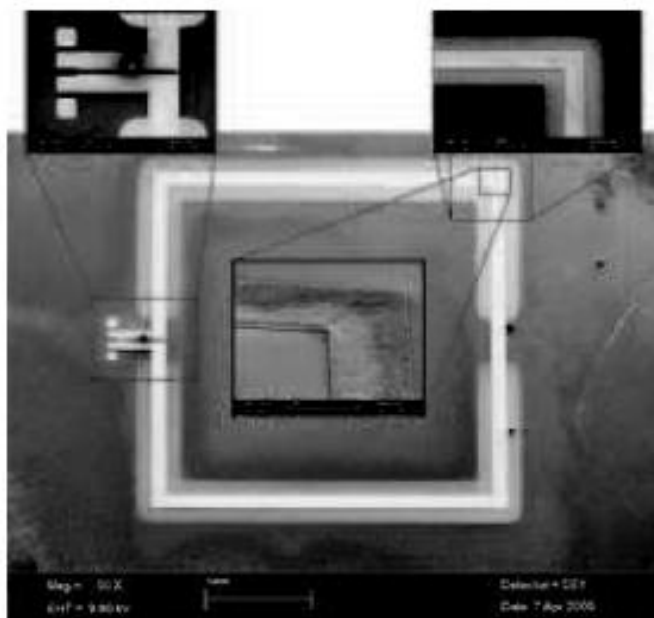


Fig. 3.5. SEM image of the full loop antenna with the oxide/nitride membrane [98].

The drawback of the square loop is the high risk of cross-talk between antenna and RF circuitry and reduced radiation resistance due to induced current in circuit metallization has to be addressed.

3.4.2.4. The dipole

The half wave dipole is a main type of radiator and widely used in RFICs applications. The amplitude of the current in a dipole antenna has the profile of a half-cycle of a sine wave, reaching a peak at the centre, as illustrated in figure 3.6 and the length of a simple dipole from end-to-end is $L = \lambda_0/2$ where λ_0 is the wavelength at the resonant frequency f_c . The dipole could operate at different wavelengths as shown in figure 3.6.

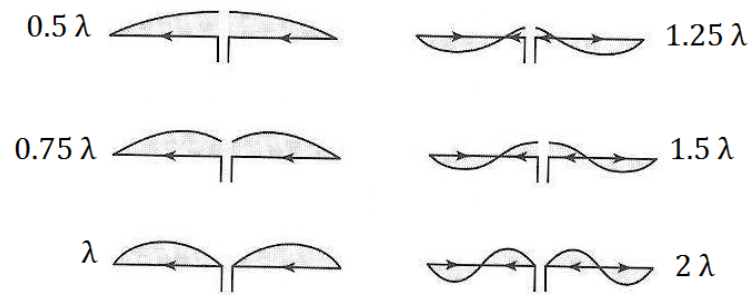


Fig. 3.6. Current distribution of thin wire dipole antenna with centre feed.

The dipole is a balanced structure as both radiator arms are equal. The middle point is a node and main source for excitation, from which current flows and distributed electrical and magnetic fields follows as they propagate towards the dipole ends. The current flow direction is represented by solid arrows in figure 3.6.

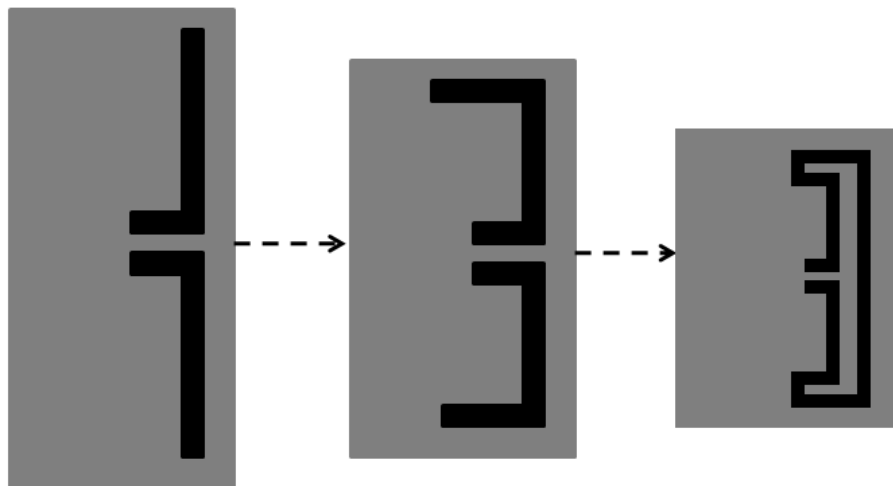


Fig. 3.7. Example of the possible length reduction of dipole antenna. From left: dipole, folded dipole and double folded antenna.

An example of folded dipole antenna was reported in [99]. The antenna was designed and fabricated on $0.8 \mu\text{m}$ SiGe and integrated with an image rejection receiver which operates at 24 GHz. The same RF front end circuitry was integrated with double folded dipole on an area of silicon die of 4.5 mm^2 compared to 7.3 mm^2 [100]. Figure 3.12 shows on chip folded and double folded dipole antenna.

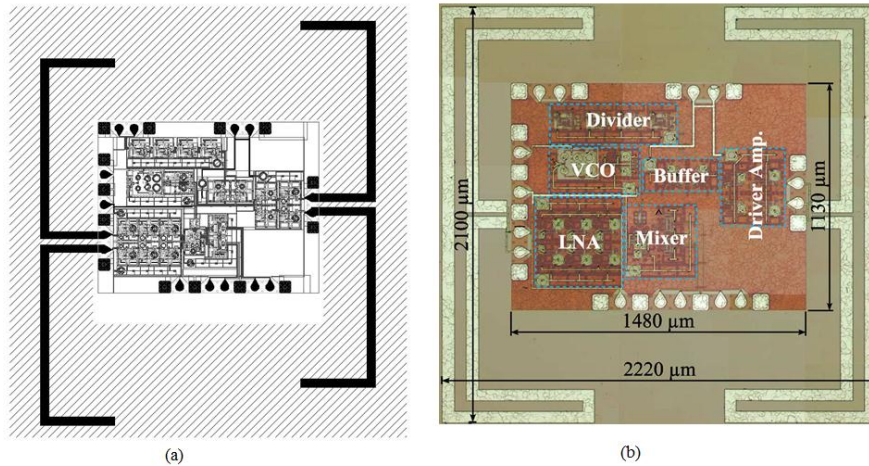


Fig. 3.8. A folded dipole antenna on 7.3 mm² chip (a) and double folded dipole on 4.5 mm² (b). Both devices use optional antennas as transmitter [99, 100].

3.5. On chip antenna measurements parameters

Testing on chip antennas at millimetre wave frequencies is extremely challenging. This is because any cable, probe or connector used to connect the device under test has its own losses and automatically affect the measurement result. The need for special calibration techniques becomes important especially if small changes were carried to experiment setup. Another important and critical issue with on chip antenna is the pitch size between signal and ground pads. This should always be identical to the probes for testing antenna characteristics.

Vector network analyser (VNA) is used for high frequency measurements. It detects and measures the amplitude and phase properties of the signal. The calibration is necessary for repeatable and high accuracy measurements, and carried out using known and perfect parameters for open-short and load provided by manufacture. New generation of VNA allows automatic calibration, as manual techniques are time consuming and various standards should be connected and disconnected several times.

Measurements are extracted from VNA in S-parameters form. S-parameters defined by measuring the voltage travelling waves between, for example, two port networks. For simplification, figure 3.9 shows two port network for further explanation.

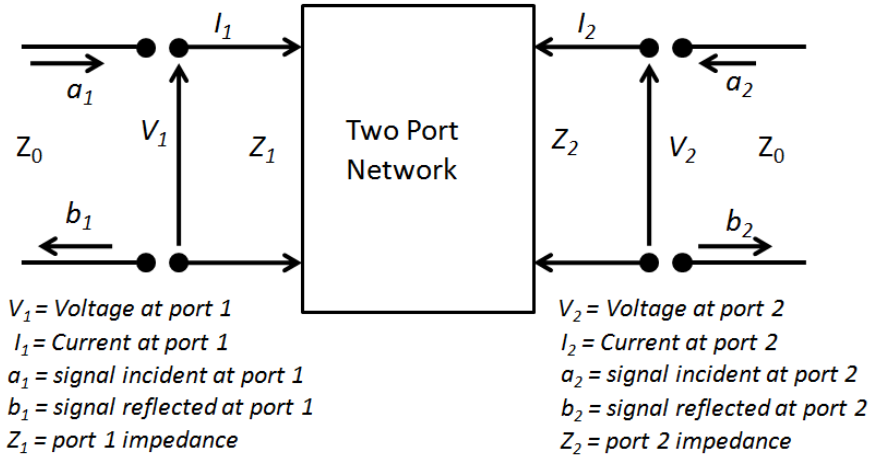


Fig. 3.9. Two port network. Z_0 is the characteristic impedance for port 1 and 2.

The relationship between the input currents, output voltages and the Z-parameter matrix is given by:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (3.13)$$

It is also important to define the incident and reflected signals, which are written as:

$$a_x = \frac{|V_x^+|}{|\sqrt{Z_0}|} \quad \text{and} \quad b_x = \frac{|V_x^-|}{|\sqrt{Z_0}|} \quad (3.14)$$

Now, scattering parameters (S) for two port networks is defined by:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, \quad S_{ij} = \frac{b_i}{a_j}, \quad \text{where} \quad (3.15)$$

- S_{11} = the input reflection coefficient, when port 2 is matched.
- S_{12} = the reverse transmission gain, when port 1 is matched.
- S_{21} = the output reflection coefficient, when port 1 is matched.
- S_{22} = the forward transmission gain, when port 2 is matched.

When characterizing an antenna using S -parameters, reflection coefficient is the most frequently used parameter. Ideally, S_{11} should equal to zero and this simply means that there is no reflected back due to a good match to the characteristic impedance of the feeding structures, usually 50Ω . Figure 3.10 shows a simple lumped element circuit for

antenna and transmitter. The matching between circuits is represented by $Z_{in} = Z_s$ where $Z_{in} = R_{in} + jX_{in}$ and $Z_s = R_s + jX_s$.

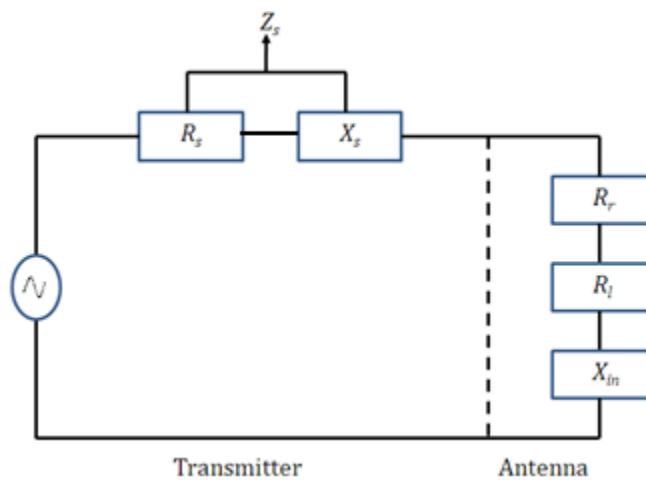


Fig. 3.10. Equivalent circuit of a transmitting antenna.

If the above condition is not fulfilled, some of the power may be reflected back and this leads to mismatch. The reflection coefficient Γ is related to the standing wave ratio (VSWR) (ratio between the voltage maximum and voltage minimum of the standing wave created by the mismatch at the load on a transmission line) according to the equation

$$VSWR = \frac{1 + |\Gamma|}{1 - |\Gamma|} \quad (3.16)$$

And Γ , the reflection coefficient is equal to:

$$\Gamma = \frac{V_r}{V_i} = \frac{Z_{in} - Z_s}{Z_{in} + Z_s} \quad (3.17)$$

Where V_r is the amplitude of the reflected wave and V_i is the amplitude of the incident wave. Another important measurement parameter is the return loss of the antenna, which is given by

$$RL = -20 \log|\Gamma| \quad (3.18)$$

For perfect matching between the transmitter and the antenna, $\Gamma = 0$ leads to $RL = \infty$, which simply means no power is reflected and all power is transmitted. If $\Gamma = 1$, this leads to $RL = 0$ and hence, all the incident power is reflected. For practical reasons, VSWR of 2

or is acceptable since it corresponds to -9.45 dB. This value is usually used to determine the impedance bandwidth of the antenna.

Antenna bandwidth is used to define the bandwidth over which the antenna has acceptable losses due to mismatch. Impedance bandwidth is computed in one of two ways. The first is to assume the lower frequency band of interest is f_L and upper frequency is f_u and let the centre frequency is f_c . The bandwidth is written as a percent of the centre frequency as

$$BW = \frac{f_u - f_l}{f_c} \% \quad (3.19)$$

Or:

$$BW \text{ (ratio)} = \frac{f_u}{f_l} \quad (3.20)$$

f_L and f_u are determined from the return loss of antenna and corresponds to approximately 2:1 VSWR (\sim -10 dB).

3.6. Antenna design

3.6.1. Computer aided program (HFSS)

High frequency surface simulator (HFSS) was used as the main design tool for antenna design in this thesis.

HFSS uses 3D full wave finite element method to verify the electrical behaviour of high-frequency and high speed components. Models can be created with different materials, boundaries and shapes. The basic mesh element used in the software is named tetrahedron which allows the user to mesh any 3D geometry. HFSS is used mainly to evaluate the S -parameters, radiation characteristics and E - H field distributions. HFSS is capable to extract Z and Y parameters from S -parameters. This is important as good impedance match between antenna and probes is required (probes impedance is usually 50Ω).

Design models are created easily in HFSS. More than one material could be implemented in one model. For example, in our design, more than one material is used (Si-SiO₂-Al). HFSS offers the ideal properties of a material, and it could be easily edited

to change important parameters (permittivity, resistivity and conductivity, ect) to meet designer's requirement. The list of materials on the software is relatively high. However, new materials could be added to library.

After creating the model, the boundary conditions are introduced to the model. These include excitation and radiation. There are different methods to excite an antenna, for example, wave port and lumped port. The lumped port method of excitation is used throughout this thesis as it is ideal for our design, and will explained in details as we progress in this chapter. The software accepts GDSII or DXF formats from other software (L-Edit, ADS, ..ect). Furthermore, models could be exported from HFSS.

Radiation boundary also known as (Absorbing Boundary Condition-ABC), allows waves to radiate infinitely into free space. This is normally done by assigning an air box which is placed at least one quarter of a wavelength at frequency of interest and away from any radiating object, as shown in figure 3.11. Radiation boundary method is ideal for structures with no curvature as curves with angles over 30° usually reflect the wave back to structure.

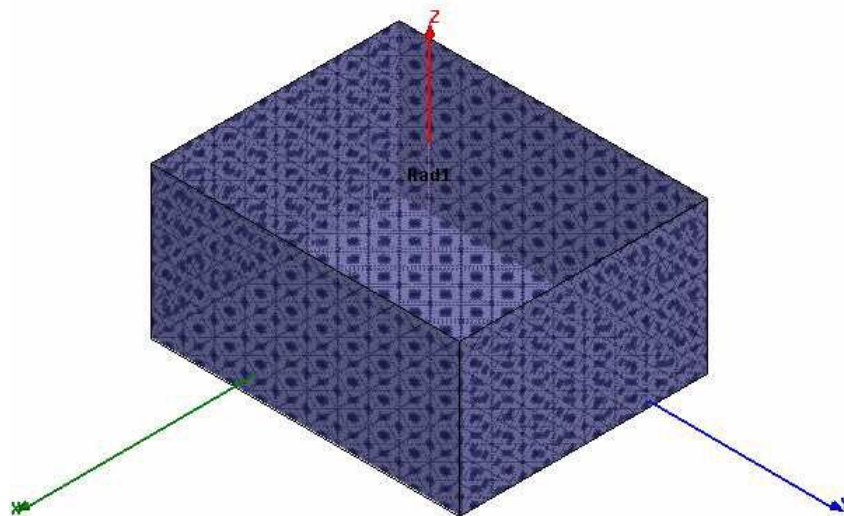


Fig. 3.11.HFSS model with radiation boundary utilizing air box.

After assigning the radiation boundaries and lumped port excitation, the structure is ready for simulation. The process starts with design check for boundaries and excitation in addition to mesh units. After design check, the following process is to select a certain frequency in which, the designer estimate to solve the model. This frequency is called (adaptive frequency). This adaptive frequency should select as a band at the expected

solution frequency. For example, 10 GHz antenna the set for frequency band is between (8-12 GHz) or any other upper and lower frequency band. The selection of frequency band is extremely important especially at high frequency resonance structures. This is due to the function between adaptive frequency and mesh (high frequency leads to larger mesh). It is important to note selecting the adaptive frequency higher than operating frequency will lead to missing the resonance frequency. The final stage in simulation processes is to choose the frequency sweep. There are three options to select from. Types of frequency sweep are

- Discrete – this sweep allows for the highest accuracy as it performs a full solution at every frequency specified in the sweep.
- Interpolative – this sweep estimates a solution for an entire frequency range.
- Fast – this sweeps generates a full field solution for each division within a frequency range. A fast sweep will obtain an accurate behaviour near the resonance.

The fast sweep is used in all designs in this thesis. It is important to select at least 3 concurrent convergent passes for high simulation accuracy.

3.6.2. Design

Size miniaturization was the main drive for choosing the antenna. As discussed in chapter 3, most of on chip antenna are patch and dipole configurations. The dipole antenna in addition to smaller size offers differential feed, and does not require a ground plane as opposed to patch antenna.

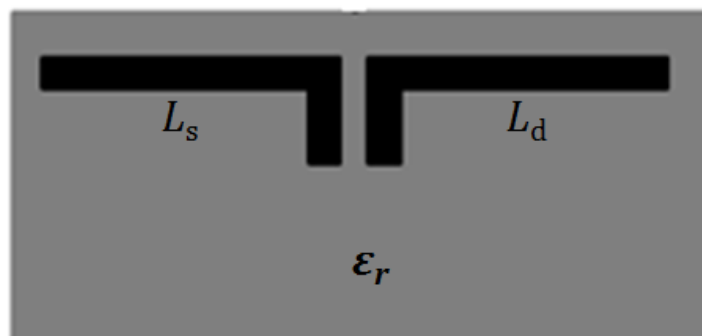


Fig.3.12. A dipole antenna on silicon substrate.

The dipole consists of a metallic strip on solid substrate. For the dipole illustrated in figure 3.12, $L_d = L_s = \lambda_0/4$.

The elementary requirements for designing a simple dipole antenna on the surface of a solid substrate are the length of dipole and effective permittivity of the substrate. The resonant frequency of the dipole is given by:

$$f_c = \frac{c}{2L\sqrt{\epsilon_r}} \quad (3.21)$$

Where f_c is the resonant frequency of the antenna and ϵ_r is the effective dielectric constant of the substrate, c is the speed of light and L is physical length of the antenna (the electrical length is equal to $\lambda_0 = c/f$). It is therefore possible to make a dipole antenna with $L < \lambda_0/2$ ($\lambda_0=30$ mm in free space). Substituting the values of c , ϵ_r , and f_c with 3×10^8 m/s, 11.9, 10 GHz in equation (3.21) results in length L of 4.35 mm.

A reduction on the length of the dipole is achievable by twisting the metallic radiator in figure 3.13. By introducing the meander, the inductance of each arm of the dipole antenna is increased. The total inductance is made up of the sum of the inductances for each meander. The capacitance is little affected unless the meander structure becomes quite dense [101]. It is important to note the total length to obtain resonance is increased over that needed for straight dipole arm. However, the overall length is shorter than original dipole.

Where $S = S:1$ VSWR and BW is normalized bandwidth. Equation (3.19) is another formula for bandwidth extracted from S -parameters.

The use of a meander antenna on silicon substrate has been reported in [102]. The antenna was fabricated on low loss, benzocyclobutene (BCB) membrane. The antenna was integrated with an active circuitry operating at 24 GHz. Figure 3.13 shows the simulation and measured results of the antenna.

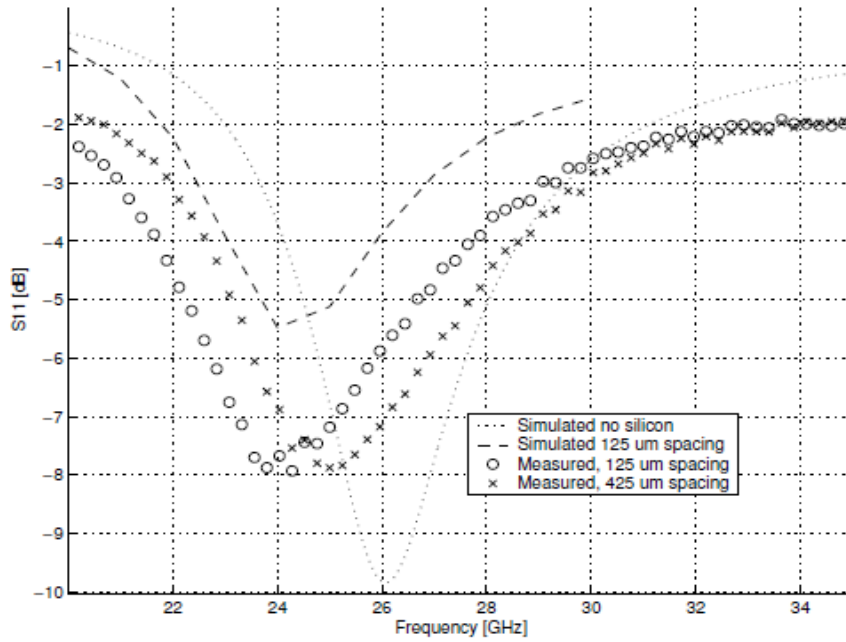


Fig.3.13. Measured and simulated results of meander dipole antenna with different membrane size [102].

In the present design, shown in figure 3.14, the overall antenna length L is 4.25mm, less than the original dipole by 0.1 mm. Table 3.3 shows the parameters of the antenna.

Antenna width	$W_A = 650 \mu\text{m}$
Antenna length	$L = 4.25 \text{ mm}$
Pitch	$a = 400 \mu\text{m}$
Conductor width	$W_C = 200$
Distance between conductors	$W_S = 200 \mu\text{m}$
Distance between arms	$D_M = 250 \mu\text{m}$

Table 3.3. Meander dipole antenna parameters.

The number of turns $N=12$ was chosen as increasing the turns reduces the resonance frequency of the antenna [103]. The characteristic impedance Z_0 of a short terminated line (meander section) is given by:

$$Z_0 = \frac{Z_c}{\pi} \log \frac{2a}{W_c} \quad (3.22)$$

Where Z_c represents the intrinsic impedance of the short line. The input of the short line is expected to be purely reactance [104].

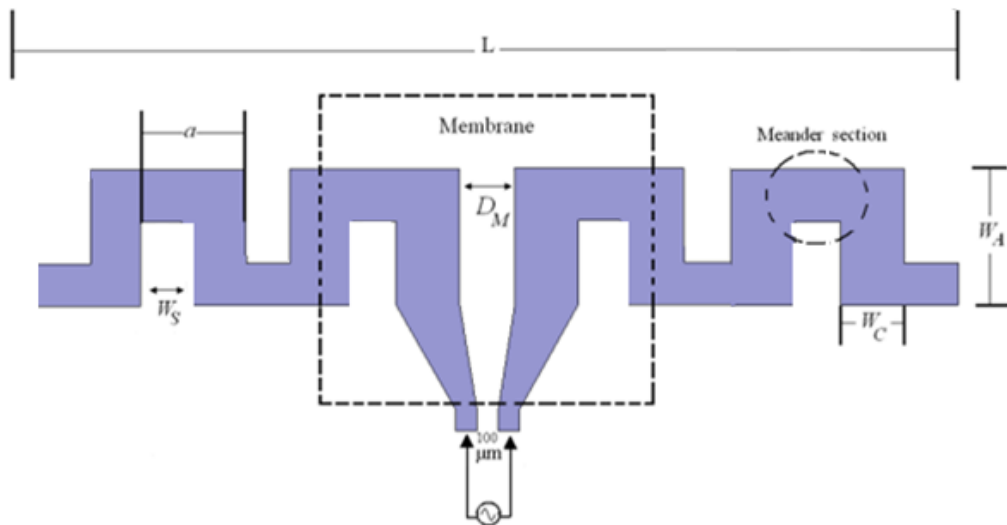


Fig.3.14. Meander dipole antenna.

In HFSS, a cavity behind dotted area shown in figure 3.14 was designed to represent the etched area and only 2 microns of SiO_2 is left to represent the membrane. Al was chosen as a conductor for the antenna, with thickness of 1 μm .

The antenna was excited using a 50 Ω lumped port between antenna arms. The return loss showed a resonant frequency at 10.22 GHz and impedance bandwidth of 32% according to equation 3.19. Figure 3.15 shows the simulated S_{11} for meander antenna.

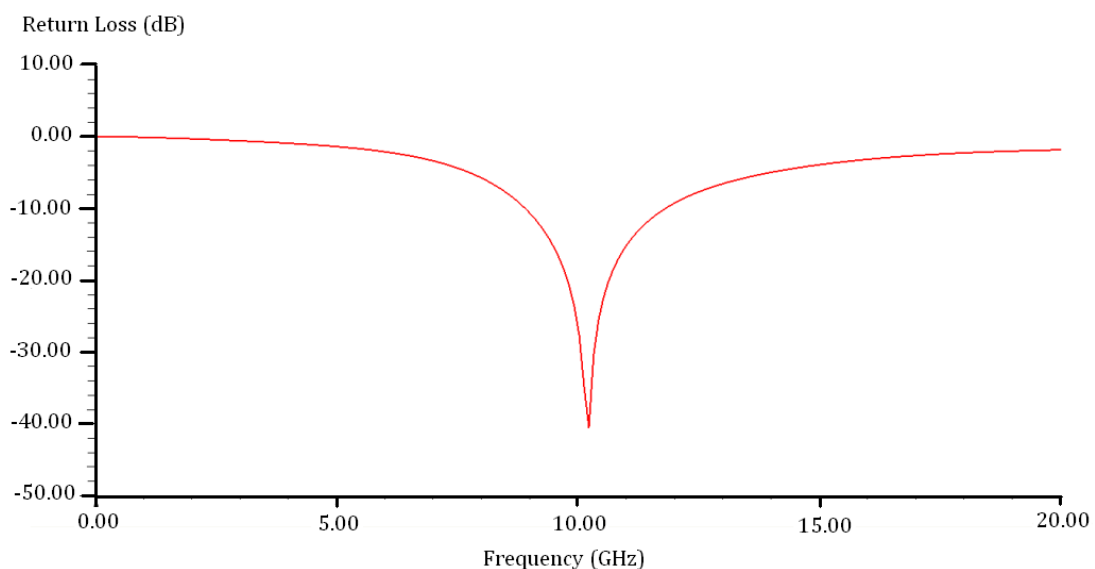


Fig.3.15. Simulated results of meander antenna.

Similarly, another method to design a short-compact dipole antenna is to bend the original shape into a zigzag shape. Zigzag antennas on silicon substrate are very useful for high frequency communications [105], and have been directly printed into gelatine capsule for biomedical application [106]. Figure 3.16 illustrates the antenna along the x-y direction. As shown in the figure, the antenna is composed of 'V' shapes connected in series. Such an array produces maximum radiation in a direction perpendicular to the axis of the structure, and a single broadside beam occurs if the arrays are closely spaced. For this reason, the length of each arm of 'V' should be equal to $\lambda/2$. However, for maximum size reduction, the length of each arm (l_s) is equal to $300 \mu\text{m}$ (0.01λ). Table 3.4 shows antenna parameters.

Antenna width	$W_A = 610 \mu\text{m}$
Antenna length	$L = 4.25 \text{ mm}$
Distance between arms	$D_z = 470 \mu\text{m}$
Section gaps	$W_z = 460 \mu\text{m}$
'V' shape angle	30°
'V' shape trace length	$l_s = 300 \mu\text{m}$

Table 3.4. Zigzag antenna parameters.

Additional parameters as shown in figure 4.6 are $W_B = 100 \mu\text{m}$ and $W_L = 150 \mu\text{m}$.

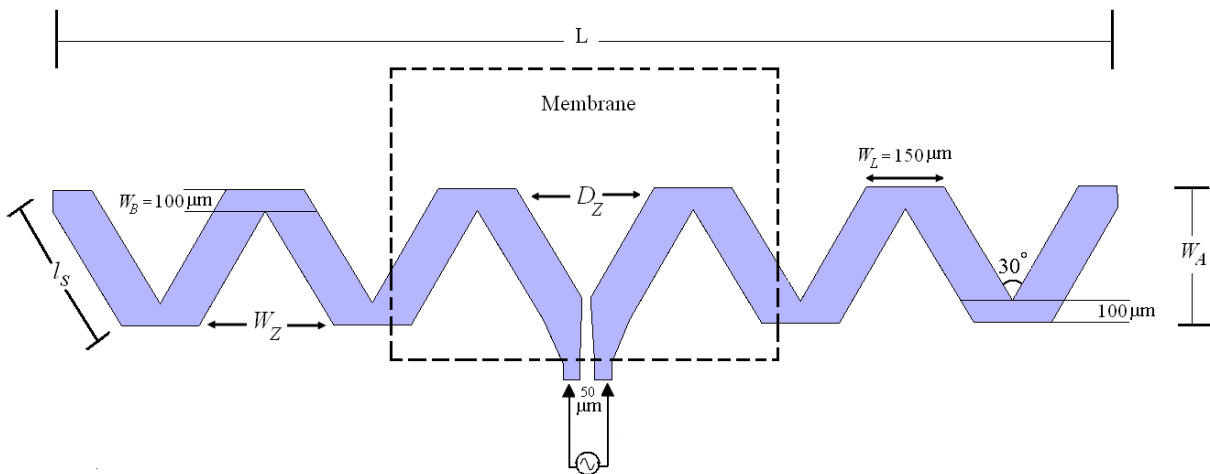


Fig.3.16. A Zigzag antenna.

The choice of substrate characteristics plays a crucial part in designing the antenna. A low resistivity silicon has been proven to be lossy as current accumulate in substrate. The power, which should be radiating away from the antenna, will be lost inside the

substrate. In figure 3.13, the maximum reflection coefficient from experiments is -10 dB. As explained previously, an ideal antenna will transmit all the radiating power, resulting in $S_{11}=\infty$. However, it is not surprising that the value of S_{11} shown in figure 3.13 as resistivity of substrate is relatively low ($=20 \Omega \cdot \text{cm}$) [102].

When designing the zigzag antenna on HFSS, a cavity behind dashed area shown in figure 3.16 was taken into consideration. The material type, thickness of the antenna is the same as when designing meander type antenna on HFSS. The substrate parameters remain the same for both types.

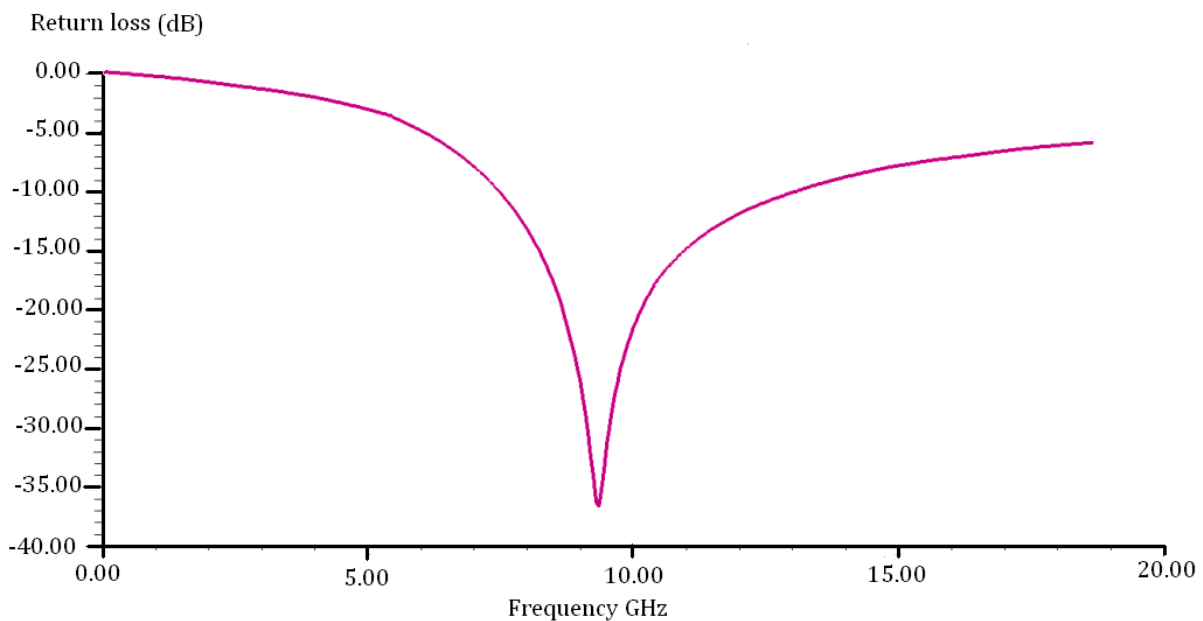


Fig.3.17. simulated S_{11} for zigzag antenna.

The simulation result shows a resonant frequency at 9.4 GHz and return loss of -37 dB. Simulation and experimental results will be explained in details in chapter 6.

3.7. Summary

A review of micromachined antennas were explained briefly in this chapter. Most of design considerations for on chip antenna are also explained such as substrate types, resistivity and thickness. A review of common antenna types used in RFICs is also discussed. This includes Yagi-Uda, square loop, and dipole antennas.

Micromachining provide a lot of solutions for performance degradation. Some techniques are demonstrated in this chapter, such as etching the lossy silicon, or modifying top of the die by adding polymers, microbridges.

The designs of meander and zigzag were introduced in this chapter. The choice allows for further size reduction. Both antennas show excellent performance at frequency of interest (8-12) GHz as demonstrated in figures 3.15 and 3.17. As we progress in this thesis, we show a further enhancement of performance for both antennas using MEMS micromachining.

Chapter 4

4. Device fabrication-micromachining

4.1. Introduction

This chapter describes in details the fabrication of *in situ* passive-single chip wireless pressure sensor operating at X band. The chapter starts by showing the lithographic methods used in this thesis to produce the antennas. MEMS micromachining is also described in details to realize both the pressure sensing element (membrane) and transducer to enhance the performance of the on chip antenna.

4.2. Fabrication

Photolithography and electron beam lithography are used for pattern transfer.

The fabrication of antenna starts with importing the GDSII format from HFSS into Tanner tools (L-Edit) software. An array of devices is then fitted into 101.6 mm diameter, which is the size of chosen silicon wafer. The final layout is used for both photolithography and electron beam lithography. In addition to devices, an etch area is also defined using a different layer with a different GDS number (each layer corresponds to lithographic step). Alignment marks are also attached and “T” shapes used as alignment marks for sawing the wafer into single chips.

Additional processing steps are required to convert the file to a format compatible with the beam writer. First the L-edit GDS II file is transferred to computer employing a program named CATS (computer aided transcription system). Once a series of input parameters are provided along with the GDS II file, CATS fractures the design with sides of maximum length of 6.4 μm . the GDS II file is then converted into readfile which is sent to both the beamwriter control computer and the job layout program BELL (beam exposure layout for lithographic engineers). BELL, which is developed at Glasgow University, can align subsequent layers to the first metallisation layer, provided appropriate metal markers were deposited in the first instance.

The mask design was carried out using Electron Beam Pattern Generator 5 (EBPG5).

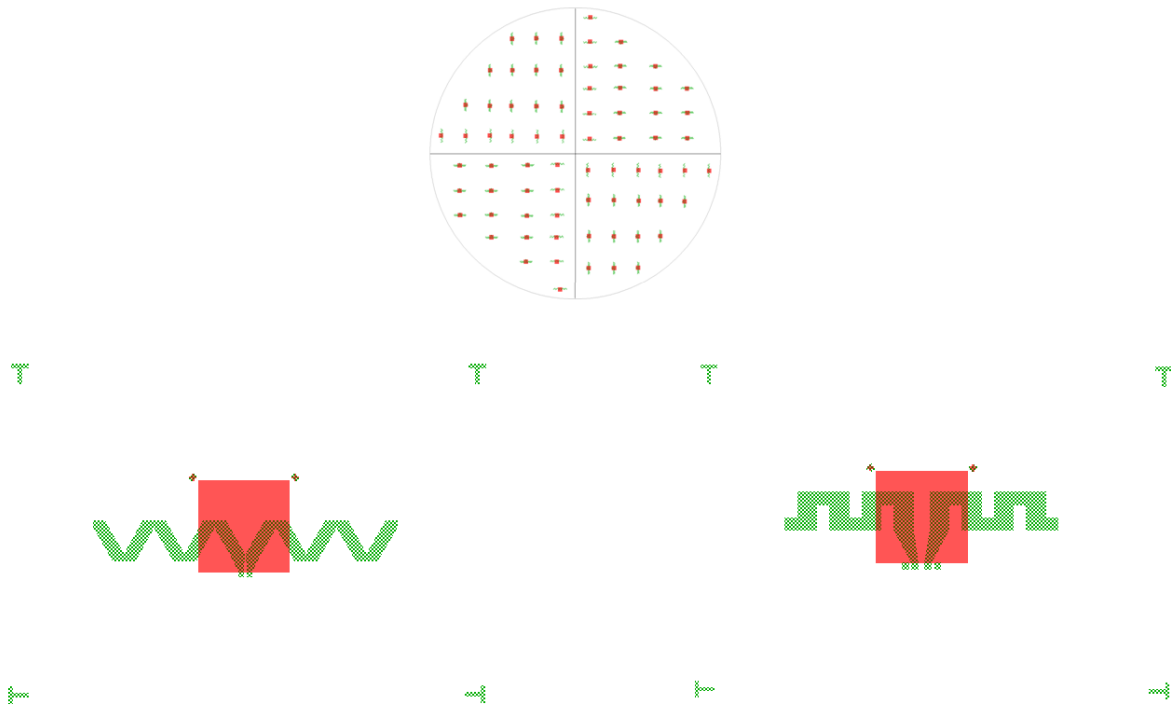


Fig.4.1. Four inch mask (top) and meander, zigzag antenna (bottom). Red area is membrane and four “T” shapes is used for sawing the wafer into 5mm X 4mm chips.

4.2.1. Photolithography

Photolithographic process was used as the first tool to fabricate the antenna and for training purposes, a 20 X 20 mm² piece of silicon was used first, and then a quarter of 4 inch wafer.

The process starts with cleaning the wafer with Acetone and then Isopropanol (IPA) rinse in ultrasonic bath for 5 minutes. To remove the moisture, the samples were placed into 90 °C oven for 15 minutes. After baking the sample, AZ 4562 was spin cast over the sample at 4000 rpm for one minute, resulting in thickness of 6.2 microns. The measured thickness was done using a dummy sample and removing the photoresist using acetone in small area of the sample. Veeco Diktak 6M height profiler was then used to measure the thickness.

The sample is then left for 10 minutes and then baked for 30 minutes in 90 °C to minimize the solvent concentration. Pre-bake is an important procedure in order to:

- Prevent bubbling or foaming by nitrogen during exposure.
- To provide a very good contact between AZ 4562 and substrate.

- To ensure there is no contamination (remaining resist) attached to the mask during exposure.
- To prevent dissolving into another resist (for building up structures using multiple coating).

The antenna pattern was transferred from mask to sample by exposing the sample to UV-light using a Suss Microtec mask aligner with exposure to UV light for 10 seconds and hard contact.

The sample was developed using AZ 400K with concentration of 1:4 in H₂O. The development time was 4 minutes. This was the best concentration/time for AZ 4562 and thus allowing a reasonable high development rate.

A short post-bake (115 °C for one minute) is required to remove the remaining developer. The process was then followed by exposing the sample to oxygen plasma (de-scum) before metallisation. This plasma etch will remove any thin photoresist remaining inside the pattern. The presence of this thin photoresist will cause poor metal adhesion or contact. It is important to note that a 50 Watt power for 2 minutes in oxygen barrel asher is sufficient enough to remove remaining photoresist.

The sample is then subjected to aluminium coating using sputtering. The metal is blanket deposited all over the sample, covering the photoresist and etched areas. Aluminium was chosen as antenna metal since it offers rapid growth, low cost and low temperature deposition (high temperature deposition usually burns the photoresist). Sputtering technique offers better adhesion of aluminium to substrate, low temperature process, in addition to ease and fast fabrication process. The sample is then immersed in hot acetone for 6 hrs, in which the remaining photoresist surrounding the antenna is removed. The metal on pattern wall was gently removed using swab and a direct stream of acetone from a squeeze bottle whilst the sample was still immersed in acetone. Figure 4.2 shows photolithography fabrication process.

Table 4.1 summarizes the photolithography process.

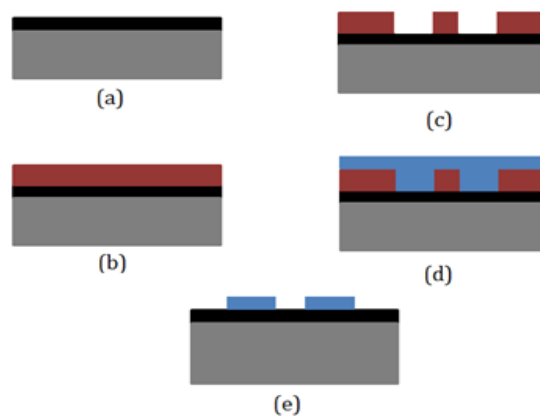


Fig.4.2. Photolithography process (a, b) Oxide growth and AZ4562 deposition. (c, d) Development and Al metallization and (e) lift off.

Process step	Material , parameters
Dielectric coating	LPCVD, 2 microns of SiO ₂
Wafer cleaning	Acetone, IPA rinse in ultrasonic bath for 5 minutes
Dehydration	5-10 minutes in 90 °C oven.
Spin coat	AZ 4562 photoresist, 1 min, 4000 rpm.
Bake	30 min in 90 °C oven.
UV-Exposure	10 seconds, hard contact
Development	AZ developer 400K, concentration of 1:4 in H ₂ O for 4 minutes.
Dehydration	5 min in 90 °C oven.
De-scum	2 min, oxygen barrel asher, 50 watts.
Metallization	One hour of Al sputtering. Thickness of Al is 1 micron.
Lift-off	Hot acetone, 6 hours.

Table 4.1. Photolithography process parameters.

4.2.2. Electron beam lithography

Electron Beam Lithography (EBL) refers to a lithographic process which uses a focused beam of electrons directed towards electron sensitive material (e-beam resist) to form patterns, in contrast with optical lithography, which uses UV-light for the same purpose. In direct comparison to optical lithography, EBL offers higher resolution, avoids light diffraction limits, and design for smaller features (typically few nanometers [107]) due to the shorter wavelength possessed by High energy electrons. EBL simply draws the

pattern over the resist wafer using the electron beam as a drawing pen. However, EBL is a slower process compared to optical lithography.

After the beam has been formed and focused it must be moved (scanned) over a substrate using a beam writing technique. There are two basic beam-writing techniques used in E-Beam lithography systems. The first is a raster technique, in which the beam is scanned over the entire chip area and is turned on and off according to the desired pattern. In the vector technique the beam is scanned only over the pattern areas requiring exposure and the usual approach is to compose the pattern from a list of simple shapes such as rectangles, triangles and parallelograms. Current Vector beam Series systems all use the vector scan method of pattern generation.

The main parts for EBL systems are [108]:

- Electron source: there are two types of sources; thermal field emission and field electron emission. The latter offers large beam size. However, thermal sources offer more stability for long time operation (typically few hours).
- Mechanical stage: The wafer should be positioned under the electron beam. The stage is critical for tilting pattern overlay (aligning a pattern to a previously made one).
- A wafer handling system: this is for loading and loading the sample into the system.

The EBL tool used in this project is VB6 Leica Microsystems lithography. The fabrication of both antennas was carried out on a complete 4 inch wafer.

The electron sensitive material used in our design is polymethylmethacrylate (PMMA). Several tests were carried to determine resolution, beam step size and energy of electrons. The beam step size is an integer multiple of the resolution. This integer is named Variable Resolution Unit (VRU). We can write (beam step size = VRU X resolution). The parameters used is 140 for VRU, dose = 420.000, beam current = 128nA and operational time of 1.499 hrs.

Bi-layer, with different concentrations of PMMA is used for lift-off. The use of bi-layer mainly offers an enhanced under cut and this works as follows: when using one layer of polymer (PMMA), usually the whole structure is removed by acetone due to

metallization on sidewalls of etched area after development. The first layer should have a lower molecular weight and the second a higher molecular weight. When exposing using e-beam, the undercut is formed and hence, avoids metal coating on sidewalls of the pattern. Additionally, bi-layer resists coatings offers simplicity, high resolution, and better yield [109].

The fabrication process starts with wafer cleaning. Higher molecular weight PMMA (2010, 15 %,) was spin cast for 1 minute at 5000 rpm. A baking time of one hour at 180 °C to ensure good contact between substrate and resist. Lower molecular weight PMMA (2041, 4%) was spin cast for one minute at 5000 rpm, and baked for 2 hours at same temperature. The process leads to layer thicknesses of 1.2 µm and 100nm.

After EBL exposure, the wafer is then prepared for development. The wafer was immersed in mixture of Methyl Isobutyl Ketone (MBK) and Isopropanol (IPA) with 1:1 ratio. The temperature of IPA was 23 °C. The development time was 60 seconds.

The wafer is then immersed in HF (1:10) concentration to remove native oxide on the pattern for 2 minutes and cleaned with DI water, then wafer is subjected to plasma etch to remove any remaining PMMA resist, with the same parameters used in photolithography process. Aluminium is then sputtered across the wafer for one hour to achieve the desired thickness of 1 µm. This was done using (Plassys MP 900S sputter coater). The wafer is then immersed in acetone for three hours to remove unwanted metal and remaining PMMA resist. Figure 4.3 shows the fabrication processes and figure 4.4 shows a complete 4 inch wafer including zigzag and meander line dipole antennas. The wafer is then sawed into 5 X 4 mm² chips and prepared for etching.

Table 4.2 shows the process parameters for electron beam lithography.

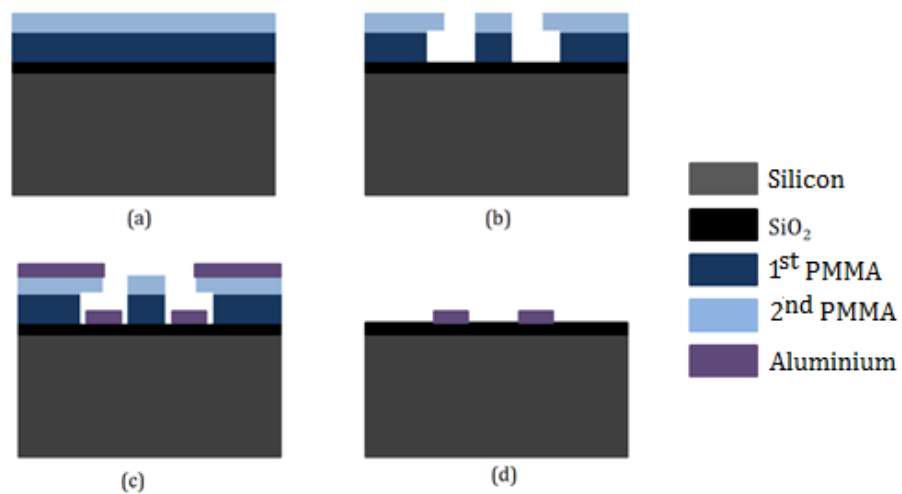


Fig.4.3. PMMA deposition, e-beam exposure and lift-off in (a, b). (c, d) metallization and lift-off.

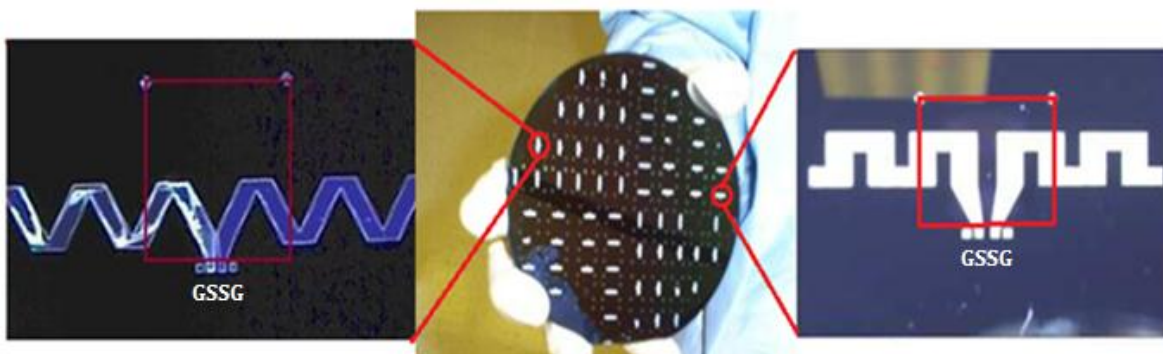


Fig.4.4. Wafer level fabrication of zigzag antenna (left) and meander antenna (right). Both antennas are probed using CascadeMicrotech^R Tungsten tips on top of GSSG pads.

Process step	Material , parameters, time
Dielectric coating	LPCVD, 2 microns of SiO ₂
Wafer cleaning	Acetone, IPA rinse in ultrasonic bath for 5 minutes
Dehydration	5-10 minutes in 90 °C oven.
Spin coat	PMMA (2010, 15 %), 1 min, 5000 rpm.
Bake	1 hour, 180 °C.
Spin coat	PMMA (2041, 4%), 1 min, 5000 rpm.
EBL	VB6 Leica Microsystems lithography, 1.499 hrs.
Development	MBK and IPA with 1:1 ratio, one minute, 23 °C.
De-scum	HF/DI water (1:10), and 2 min in oxygen barrel asher, 50 watts.
Metallization	One hour of Al sputtering. Thickness of Al is 1 micron.
Lift-off	3 hours hot acetone bath.

Table 4.2. EBL process parameters.

4.2.3 Processes comparison

Using photolithography for small features is very difficult due to diffraction limitation during UV light exposure and the resolution is 50 nm at maximum. Photolithography is faster when exposing a large shape, and also high speed on parallel exposure.

EBL has better diffraction limits and could easily reach resolution of 20 nm. EBL is faster when exposing a complex and small patterns, and thus, it is widely used in integrated circuits applications.

The main drawback for EBL is the point by point exposure, i.e. it takes a long time to expose, for example 4 inch silicon wafer. A long exposure time could leave the process vulnerable to beam drift or instability which may occur during the exposure. Also, the turn-around time for reworking or re-design is lengthened unnecessarily if the pattern is not being changed the second time.

4.3. Deep Reactive Ion Etching (DRIE)

The process is a highly anisotropic etch, used to create deep holes and trenches in silicon wafers. DRIE is widely used in IC technologies, for example creating vias between different metal layers.

Inductive-Coupled Plasma (ICP) etching is one of the common methods of Deep RIE etching (DRIE). ICP offers high etch rates due to condensed plasma and good side wall angle control, and does not require any etch stop techniques used in wet chemical etching. KOH etching is highly dependable on the surface orientation of the silicon wafer. For example the angle of the etched area between miller index $\langle 100 \rangle$ and $\langle 111 \rangle$ is 54.7° , and between $\langle 110 \rangle$ and $\langle 100 \rangle$ is 45° . Therefore, ICP etching offers larger membrane area due to sidewalls of 90° regardless of wafer orientation, and automatically gives large sensing area using ICP etching.

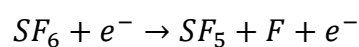
Figure 4.5 shows side walls of membranes using KOH and ICP etching.



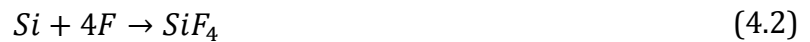
Fig.4.5. Plasma etching (a) and (b) KOH etching.

ICP is well suited for high aspect ratio devices, which could easily reach approximately between 20 to 30:1. A reasonable time for etching is another advantage provided by the process.

Inductive-coupled plasma could be used to etch many materials. The main gas used in plasma etching is Fluorine which could be obtained from CF_4 or SF_6 which are used in plasma etching process. For example, if the main source is SF_6 , fluorine could be released using the following reactions [110]:



For etching silicon, the reaction could be written as:



CF_4 reacts with silicon according to equation:



The plasma is generated by coupling electromagnetic into the gas atoms. In a traditional RIE tool, the energy is provided by an RF electric field operating at 13.56 MHz [111] between two parallel plates. In ICP system, the energy is provided by a coil surrounding the plasma chamber as shown in figure 4.6.

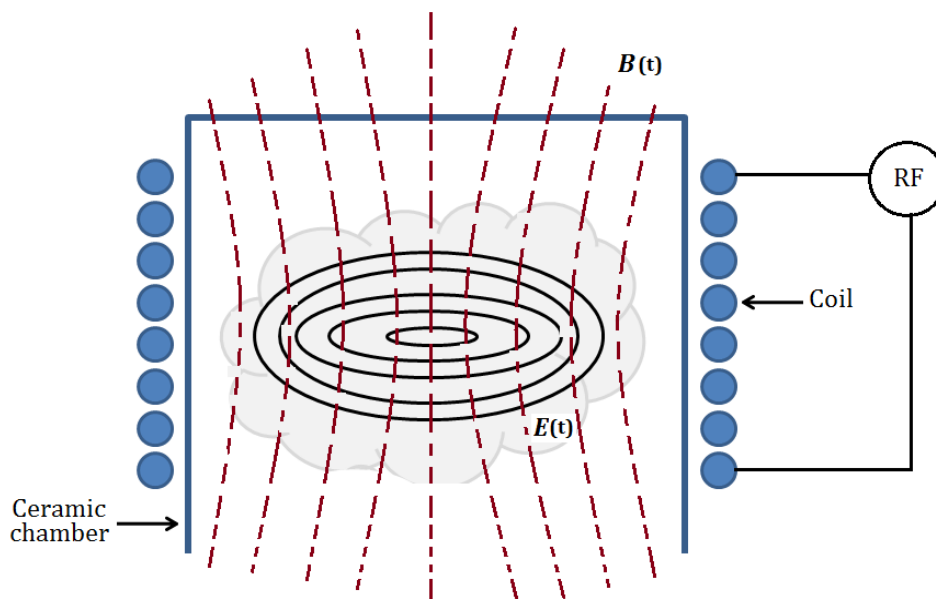


Fig.4.6. ICP coil chamber. The presence of magnetic and electric fields help accelerates charge particle.

Atoms and ions are produced in the plasma due to the acceleration of electrons and ions. Since the chamber is surrounded by two coils, the second coil acts as a transformer which helps speed up the electrons and thereby causing collisions that produce more electrons and ions. The electrons leave the plasma (cloud in fig 4.13) and plasma will develop a positive charge compared to opposite charges in the surroundings. Because of the large voltage difference between plasma and electrons at chamber walls and sample, positive ions at plasma drift towards the walls and sample where they collide with sample to be etched. The vertical movement of ions towards the sample generates isotropic etching profiles.

In modern ICP etching tools, the machine is equipped with a cryogenically cooled wafer holder (cryogenically temperature is the range between 100⁰-170⁰C). The cool wafer holder is able to cool the wafer to liquid nitrogen temperature. At low temperature, O₂ is added to etch gas enables the formation of a very efficient side wall passivation layer. On horizontal surfaces, the removal of the passivation layer is largest. This is due to constant bombardment from energetic ions from the plasma, and the process can be balanced so the side walls remain protected while the horizontal surface is exposed to fluorine.

Ideally, the etching tool should generate high plasma density (>10¹¹/cm³) to achieve a high etch rate whilst operating at low pressure (1-20 mTorr). The source also needs to produce ions uniformly in terms of energy of ions and distribution. This is a main concern for active components in IC technology.

One plasma source is Electron Cyclotron Resonance. In this process, the wafer is subjected to a very low temperature, around -110 °C. This process produces highly vertical walls. However, the main drawback for this process is the low temperature subjected to wafer. This could easily damage the mask protection.

After dicing the 4 inch wafer into 20 mm² chips, the samples were prepared for etching. AZ4562 was used as a photoresist to protect un-etched areas. The resist was spin cast for one minute at 6000 resulting in 5 microns film thickness. A baking time of 30 minutes in a 90 °C oven was followed (pre-bake). Since the thickness of substrate is 300 μm, the expected etch time will be small and the etch rate will be faster. A further protection with AZ4562 was carried using the same procedure, resulting of 10 μm film thickness. Then, UV-exposure was followed to create an opening into substrate using Suss microtec mask aligner. The mask was exposed for 30 seconds using hard contact between mask and substrate and alignment gap of 120 μm. The chips were then developed using same process as explained in photolithography process. The chips were then etched using STS inductive coupled plasma to form the membrane. The etch time was 69 minutes resulting in etch rate of 4.38 μm/min. Figure 4.7 shows a microphotograph of the membrane.

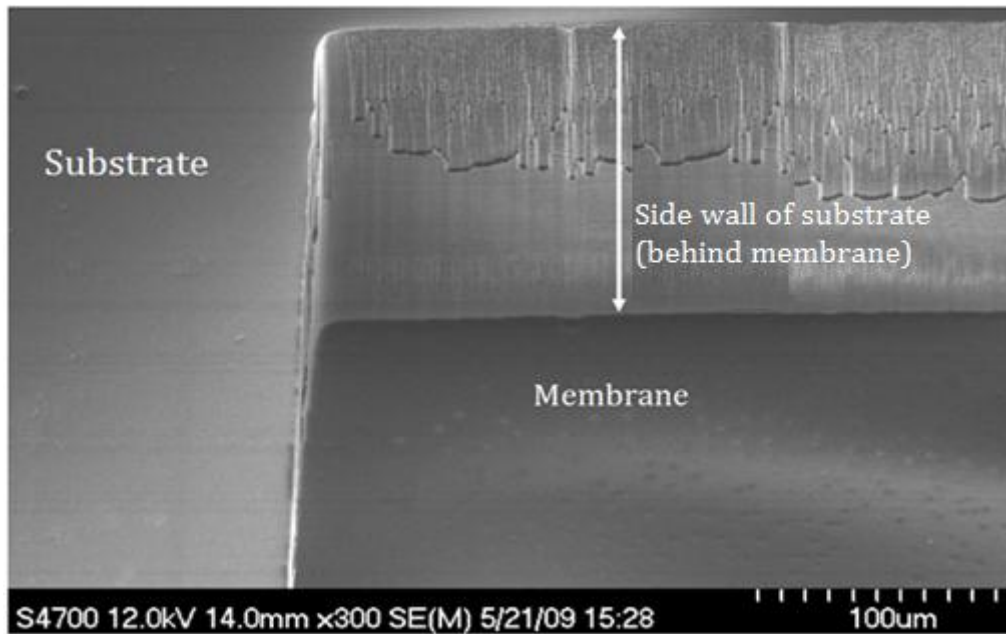


Fig.4.7. SEM microphotograph of back side of membrane.

The measured membrane thicknesses were between 2 μm and 4 μm for some chips. This was beneficial to our pressure experiments as thinner membranes break easily at very small amount of pressure. Figure 4.8 shows a photograph of a zigzag antenna on 2 μm SiO_2 membrane.

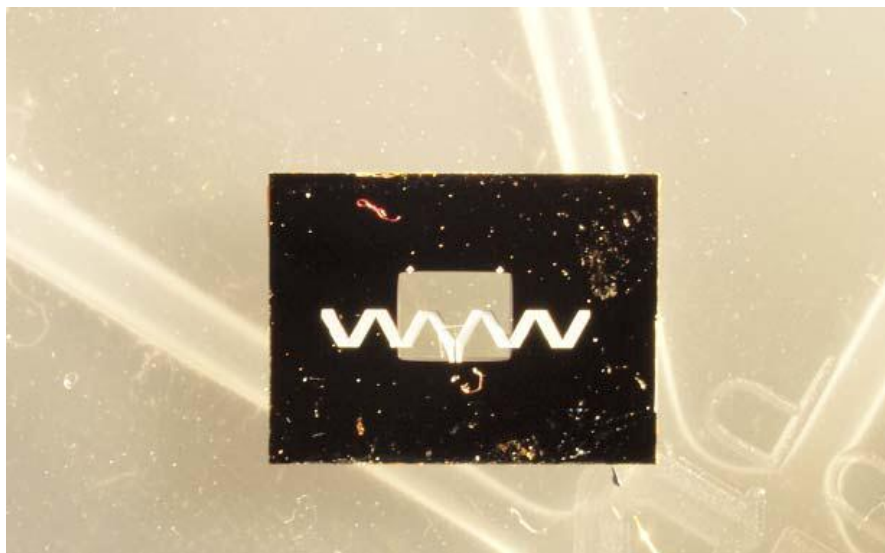


Fig.4.8. A photograph of zigzag antenna on membrane. The antenna is visible on top of transparent SiO_2 .

The depth of etching was measured using a surface Profilometer. As shown, in figure 4.9 (b) and (c) the depth (Z-direction) is 294.45 μm . This leaves around 6 microns of silicon behind the membrane for etch time of 68 minutes. This remaining silicon adds more stiffness to membrane. To achieve larger depth, the samples are kept for further one minute and 90 seconds resulting in membranes with thicknesses between 2~4 μm .

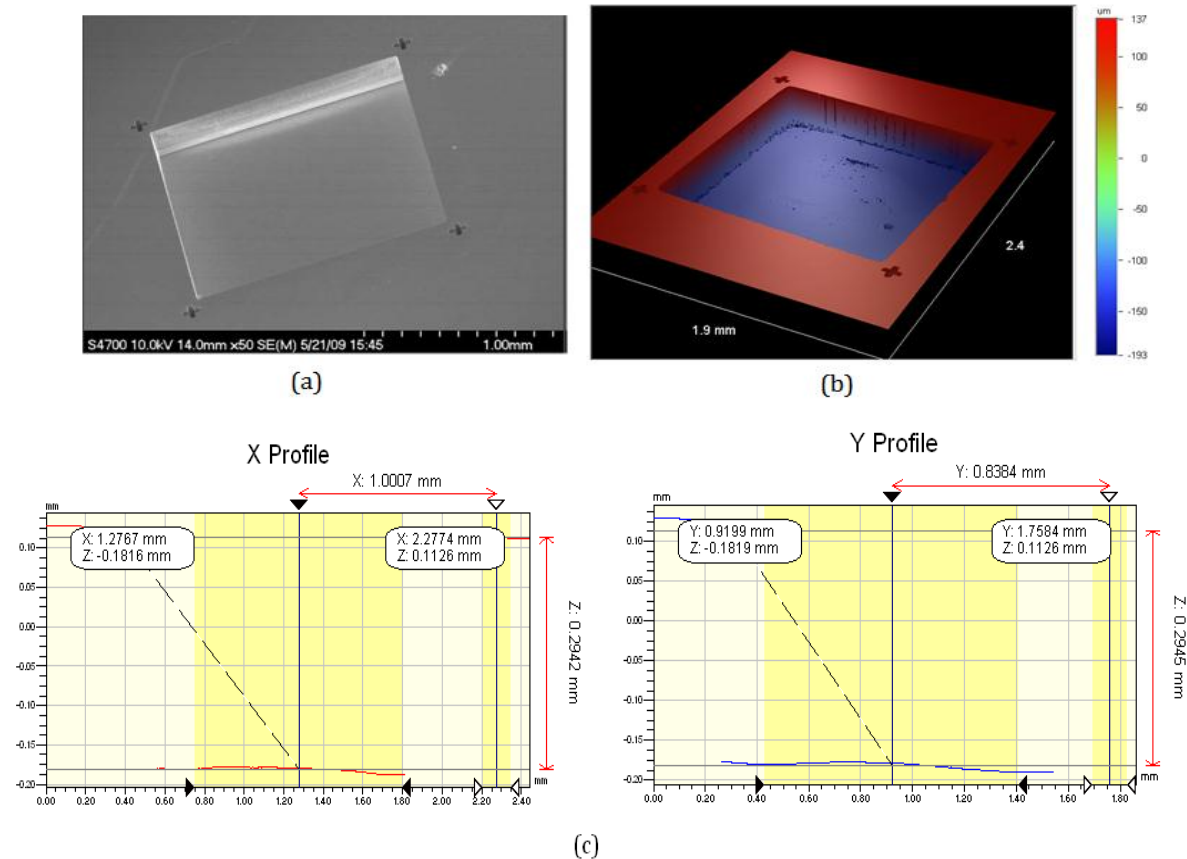


Fig.4.9. SEM of membrane with Profilometer image on same membrane (a, b), and measured depth of etching at z direction in (c).

4.4. Estimated pressure-deflection relation

In this section we estimate the pressure-deflection for a thin film (1.5 μm SiO_2) on top of single crystal silicon (SCS) as shown in the photograph in figure (4.15).

The deformation of thin film under the pressure p is described by the vector field of the displacements $\{u(r), v(r), w(r)\}$ of the individual points $r=(x, y)$ of its middle plane. This displacement is best described in strain components ε_{xx} , ε_{xy} , ε_{yy} and residual strain ε_o . The total displacement is given by [112]:

$$\begin{aligned}\varepsilon_{xx} &= \varepsilon_o + \frac{\partial}{\partial x} u(r) + \frac{1}{2} \left[\frac{\partial}{\partial x} w(r) \right]^2 \\ \varepsilon_{yy} &= \varepsilon_o + \frac{\partial}{\partial y} v(r) + \frac{1}{2} \left[\frac{\partial}{\partial y} w(r) \right]^2 \\ \varepsilon_{xy} &= \varepsilon_o + \frac{1}{2} \left[\frac{\partial}{\partial x} u(r) \frac{\partial}{\partial y} v(r) \right] + \frac{1}{2} \left[\frac{\partial}{\partial y} w(r) \right] \left[\frac{\partial}{\partial x} w(r) \right]\end{aligned}\tag{4.4}$$

The relation between strain and stress σ_o according to Hook's law is given by:

$$\sigma = \varepsilon E\tag{4.5}$$

However, for biaxial stressed material, equation (4.9) becomes:

$$\sigma = \frac{\varepsilon E}{(1 - \nu)}\tag{4.6}$$

Where E is Young's modulus and ν is Poisson's ratio. For a square membrane shown in figure 4.10, positioned at $(x-y)$ plain, the deflection is given by:

$$\begin{aligned}u(x, y) &= A \sin \frac{2\pi x}{L} \cos \frac{\pi y}{L} \\ v(x, y) &= B \cos \frac{\pi x}{L} \sin \frac{2\pi y}{L} \\ w(x, y) &= C \cos \frac{\pi x}{L} \cos \frac{\pi y}{L}\end{aligned}\tag{4.7}$$

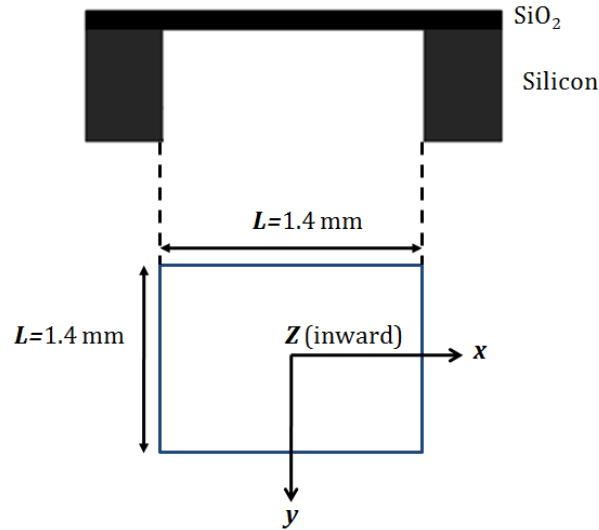


Fig.4.10. Membrane in x - y plane.

This equation shows the maximum deflection for a membrane with side-length L occurs at the middle ($=L/2$).

An approximation to the pressure-deflection law is of the form:

$$P(w_o) = c_1 \frac{\sigma_o h}{a^2} w_o + c_2 \frac{Eh}{(1-\nu)a^4} w_o^3 \quad (4.8)$$

Where h is membrane thickness, L is side length of membrane. The values of c_1 and c_2 are dimensionless coefficients that depend on n and ν . the values of c_1 and c_2 are given by:

$$c_1 = \frac{\pi^4(1+n^2)}{16} \quad (4.9)$$

$$c_2 = \frac{\pi^6}{2(1-\nu^2)} \left(\frac{9+2n^2+9n^2}{256} - \frac{[4+n+n^2-4n^3-3n\nu(1+n)]^2}{2\{81\pi^2(1+n^2)+128n+\nu[128n-9\pi^2(1+n^2)]\}} \right) \quad (4.10)$$

The value of n is important for rectangular membranes, and defined as the ratio between short length " a " and long length " b " of a rectangular membrane. It is therefore recommended to apply equations (4.13) and (4.14) into equation 4.12 for only rectangular membranes, with ratio reaching $a:b=1:2$.

Equation (4.12) becomes

$$P(w_o) = \frac{\sigma_o h}{L^2} w_o + \frac{Eh}{L^4} w_o^3 \quad (4.11)$$

The values of Young's modulus, residual stress, Poisson's ratio are 80 GPa, 0.2 GPa and 0.15 respectively. Figure 4.11 shows an estimated pressure and deflection for 1.5 microns SiO₂ membrane.

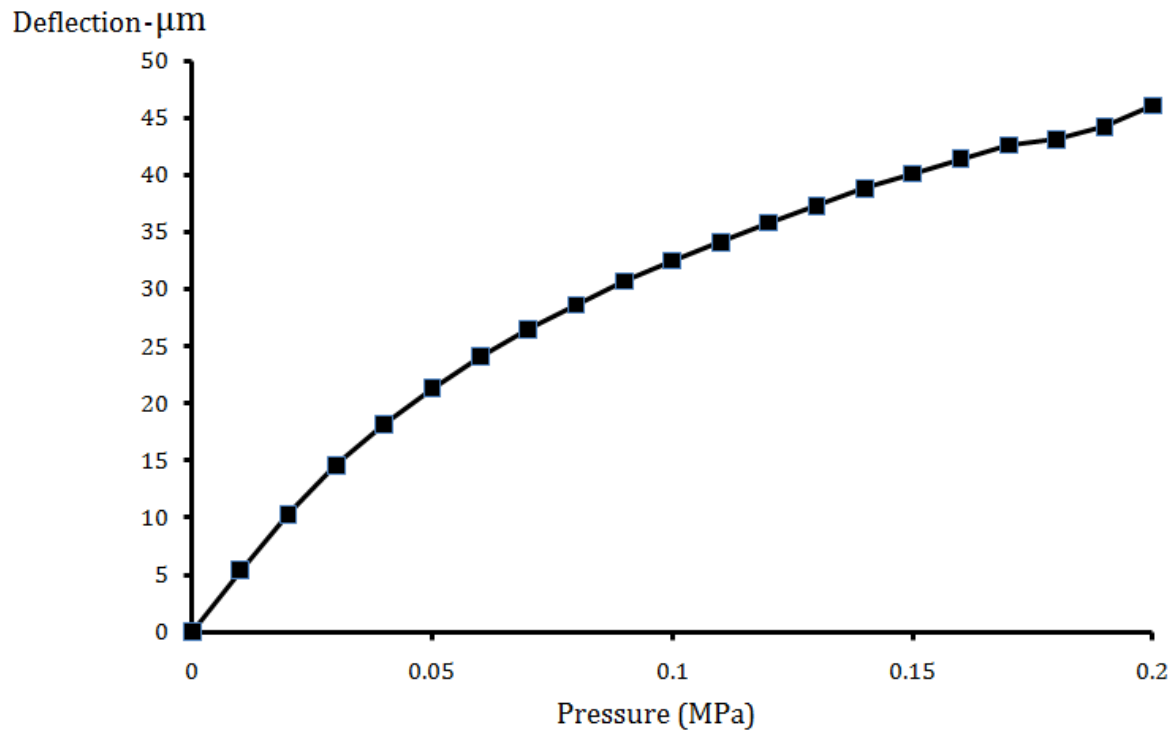


Fig.4.11. Pressure-deflection theoretical estimation for SiO₂ membrane.

We can re-write equation (4.15) as follows:

$$\frac{PL^2}{hw_o} = \sigma_o + E \left(\frac{w_o}{L} \right)^2 \quad (4.12)$$

The above equation corresponds to strain stress relation. E is proportional to the slope of the line and σ_o is proportional to interception with y-axis.

4.5. Summary

A single chip microwave pressure sensor has been designed and fabricated on a single crystal silicon substrate. The novel device consists of two passive resonant circuits: meander and zigzag dipole antennas. Micromachining techniques were introduced for two purposes: to enhance the performance of the antenna and to realize the sensing element on the same chip. The suggested operation frequency of these devices is 10 GHz. In details, we explained the methods of fabrication of the device, that includes photolithography and electron beam lithography. Releasing of 1.5 μm SiO_2 and 4 μm bi-layer (Si/ SiO_2) membranes was also shown in this chapter. An estimation of pressure-deflection of SiO_2 membrane was also introduced in this chapter. The relation between membrane deflection and wireless frequency measurement will be shown in the results chapter of this thesis.

Chapter 5

5. Passive CMOS pressure sensor

5.1. Introduction

In this chapter we discuss a novel CMOS-MEMS pressure sensor. As discussed in the literature review, integrating the sensor and a readout circuitry on the same chip offers cheaper, mass produced, smaller, thinner, and lighter chips. With the rapid growth of Complementary Metal Oxide Semiconductor infrastructure for design tools and foundry service, silicon sensors can be developed with new features and multiple functions on a single chip, resulting in more power efficient devices with vastly improved capabilities.

This chapter describes the tools and techniques to design the passive sensor and the tuned passive circuit (antenna). Both Cadence and HFSS software are used as simulation tools. To conclude a complete layout of the sensor is presented.

5.2. Technology and Tools

5.2.1 Foundry service

This project was the first collaboration between the University of Glasgow and National Semiconductor. The design and fabrication of the chip was carried out using CMOS-7 technology. The CMOS wafer is a standard p -type substrate with heavily doped n regions (wells). The foundry offers:

- The choice of 4 metal layers for interconnects. An additional thick metal layer (copper) is optional. Another optional layer is provided for wire bonding to printed circuit boards (metal BM).
- A stray capacitor (from metal 1 to BM layer).
- Poly-poly (PIP) and Metal-Metal (MIM) capacitors.
- Poly and diffused resistors.

Figure 5.1 shows a cross section of the wafer. Access to National Semiconductor was provided through the University multi project service. By assembling as many designs as possible onto single wafer, the cost for individual design is reduced significantly. National Semiconductor arrange cutting of the wafers into small dies, and additionally fulfils packaging requests.

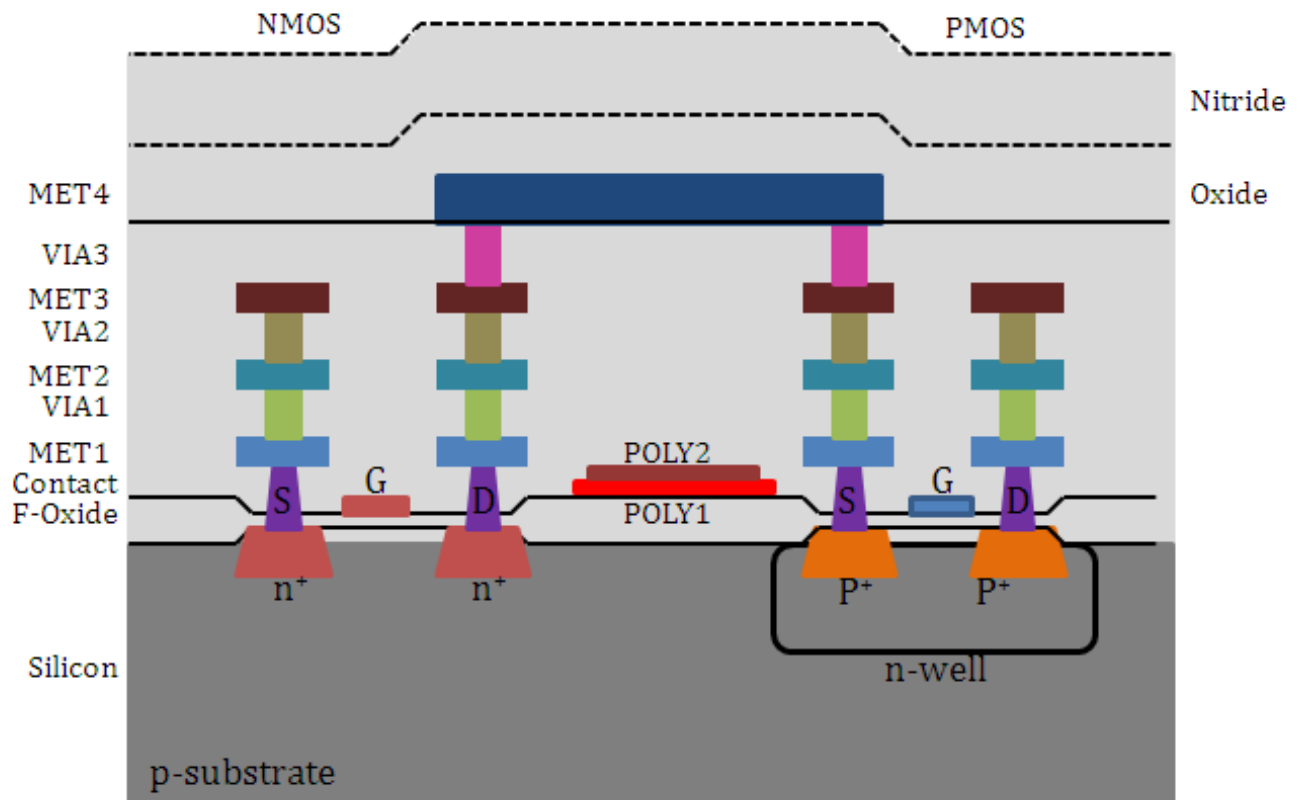


Fig. 5.1. Cross-section through the layers of Nat-Semi's CMOS-7 process.

5.2.2 Computer aided sensor design

Figure 5.2 illustrates the steps to design a sensor array using Cadence software. On schematic editor level design, the sensor array is designed to meet specific requirements by drawing a diagram of components and their connections. The components provided by the technology are: 0.35 gate length MOSFETs, resistors, and capacitors. The circuit is simulated using the Cadence Spectre simulator, which is similar to the original Spice circuit simulator developed by the University of California at Berkeley [113]. Results of simulations are obtained using Cadence Analog Design Environment.

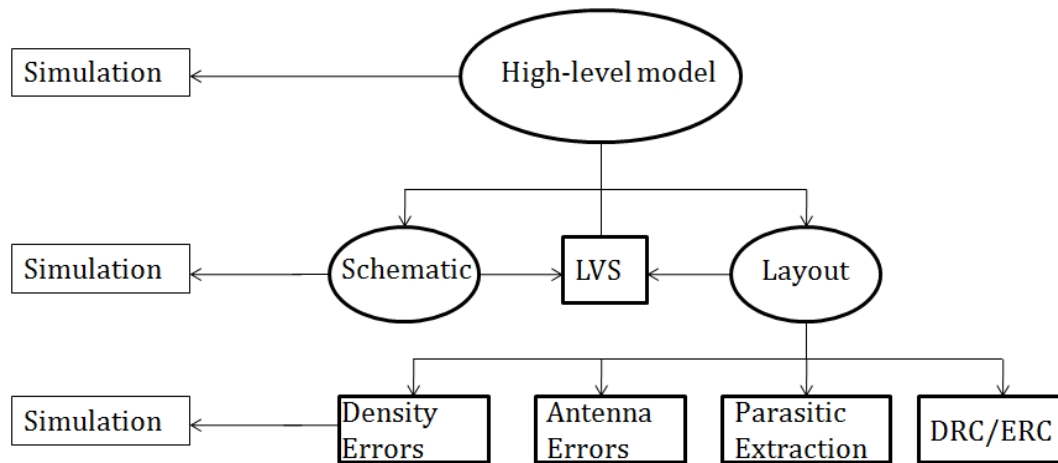


Fig.5.2. CAD-flowchart of CMOS design and layout.

It is important to note that the design would not fulfil its requirements on the first attempt. By changing the topology of the circuit or the small parameters (transistor's length and width, value and type of capacitors and resistors) then the requirements of final design will be achieved after visualising the simulation results.

Once the final simulation results of the design on schematic level matches the final requirements, work can start on the physical design of the schematic (layout). Areas could be defined for specific devices on chip, for example, n -well which incorporate PMOS transistors and some capacitors, diffused areas for resistors, polysilicon and metal layers. National Semiconductor provides defined parameters for devices like NMOS, PMOS, capacitors and resistors (no drawing).

The layout defines the geometries that appear on the mask at the foundry. For example for a PMOS transistor (fig 5.1), the device requirements are [52]

- Surrounded by n -well by a certain distance which could vary from one foundry to another. This margin is enough to ensure the transistor is in the well for all expected misalignment during fabrication.
- The active area (S/D) regions are connected to n -well.
- The gate of the transistor requires its own mask during fabrication.
- The contact window mask provides connection from active and poly areas to the first layer of metal.

Usually analog design layout is more critical than digital layout as parasitic components have a greater effect on analog circuitry. The arrangements of components, devices and connections between them are carried out by hand. Table 4.1 summarizes the main layers used in CMOS-7 technology.

parameters	Thickness (μm)
Top metal	0.9
Metal 3	0.5
Metal 2	0.5
Metal 1	0.5
Oxi-nitride passivation	1
Epitaxial layer	5.5
Silicon substrate	520~575
Silicon nitride	0.6

Table 5.1: Some of NSC process parameters.

There are some layout techniques used by designers to ensure good performance of the chip, for example, transistor folding or fingering techniques which reduce the thermal gate noise voltage.

Another technique is symmetries, and transistor shadowing between transistors especially in the case of differential amplifiers, current mirrors and differential cross coupled oscillators. This is important because, during fabrication of unmatched devices (different orientation), the many steps of wafer processing and lithography behave differently along different axis.

Breaking up a long transistor into small transistors connected in series is also another technique. This gives the advantage of a more compact layout, in addition, reducing the resistance exhibited at the gate.

As seen in table 5.1, modern CMOS technology use between 5 and 7 metal layers as interconnects. Metal layers could be protected using metal shields to reduce noise and parasitic capacitance which could affect devices.

After layout, the design is subjected to a Design Rule Check (DRC) and Electrical Rule Check (ERC). The design rules are introduced by foundries according to their own fabrication processes. For example the minimum distance between two Metal-Insulator-Metal capacitors should be 5 μm apart. Another example is two metal tracks connected by via should overlap the edges of the via by a certain distance. Electric rules are used to check if there are any floating gates of transistors and check any electric shorts in the circuit. Once the layout is checked using DRC and ERC, a direct comparison between schematic level and layout is carried out to ensure all components are matched. When placing a device using a wrong connection, an automatic ERC is performed and the place of the short circuit would be visible. Cadence Assura extraction tool is used to recognise the devices and to create a netlist, which in return, compare the Layout Versus Schematic (LVS) checker. Once the process is successful simulation for the physical circuit is conducted, and results are usually differ from schematic simulations due to parasitic Resistance, Inductance, and Capacitance (*RLC*). Another extraction tool is conducted by de-coupling the circuit to the substrate, which is important to extract the capacitance created by substrate. The last rule check is the “antenna” rule, in which the final design must fulfil the densities required for fabrication. For example, Metal-1 density should cover 30% of the chip as well as Metal-2 and so on. National-Semiconductor provides small squares of all layers to fill the density required, and if, the extracted view simulations fulfil the original requirements, the design is uploaded to the foundry portal and is ready for fabrication.

5.2 Working principle of proposed device

Figure 5.3 shows the basic operation principle of device in schematic form.

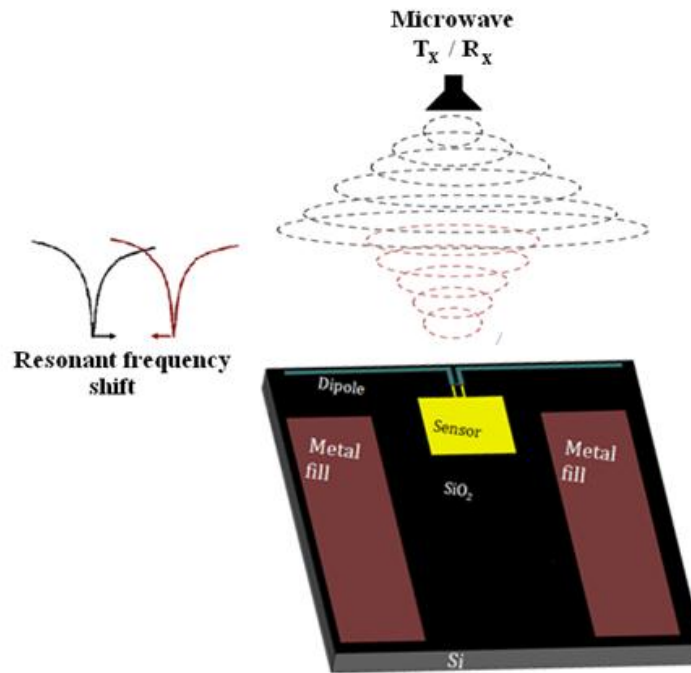


Fig. 5.3. Working principle of the proposed wireless pressure sensor.

The sensor consists of array of MIM capacitors connected in series and parallel, and coupled with a dipole antenna on the same chip. Increased pressure behind the membrane causes it to deflect and the value of capacitance is changed accordingly. This change is used to detune the resonant frequency of the antenna.

The sensor is read by directing a beam of microwave radiation from a horn antenna, towards the sensor and recording the reflected spectrum. By this method, the resonant frequency of the antenna is measured. The design frequency was chosen to be in the microwave X-band (8 – 12 GHz) since it is widely used for a range of microwave technologies including RADAR and telecommunications [114]. The microwave X-band offers relatively small wavelength ($\lambda_0 = 30\text{mm}$) in free space so that there is the possibility of making relatively small single chip devices with appropriate antenna design. The block diagram illustrated in figure 5.4 (a) summarizes the operation principle on chip and (b) a lumped element.

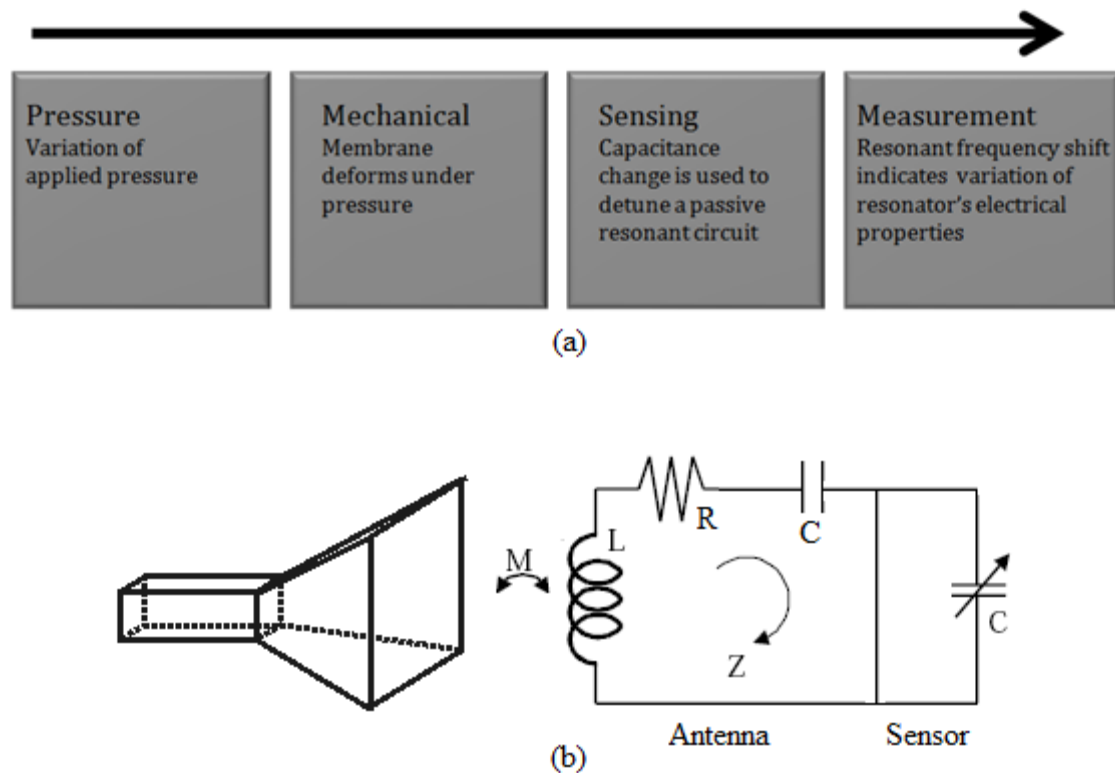


Fig.5.4. Block diagram of passive sensor (a) and electrical equivalent circuit antenna and variable capacitor sensor and its electromagnetic coupling (wireless) with horn antenna (b).

5.3 On chip antenna

On chip antennas are small at higher frequencies, and overcoming problems associated with interconnect and substrate losses are the challenges for designing of wireless applications. These challenges are the main obstacle for designing high frequency on-chip transceivers.

The choice for the antenna was a dipole configuration because of its smaller size, differential feed and consequently to avoid the common mode that needs a ground contact from the bottom of the chip (as opposed to patch antennas), which is difficult to realize in the case of a standard CMOS technology. Most on chip antennas are realized with differential topologies (circular and square loop, and dipoles) due to the ease of integration with active devices, for example, a LNA or PA amplifiers.

The antenna was designed and fabricated using the top metal layer in CMOS-7 process (M4). The resistivity of the CMOS chip was less than $1 \Omega \cdot \text{cm}$. This low resistivity would

become a major challenge to overcome since most of the power supposed to be radiated would dissipate into the substrate.

A specially requested epitaxial layer (heavily used in manufacturing processes of CMOS and Bipolar transistors) was used as an additional layer. $Si_{Epitaxial}$ has a thickness of $5.5 \mu\text{m}$ and have a resistivity of $15 \Omega\cdot\text{cm}$, this is much higher compared to the silicon substrate.

HFSSTM was used to simulate the antenna, however designing or importing the capacitor array into HFSS was found to be very difficult. This is due to the large number of capacitors (600 cells) and interconnects between them, in addition to the presence of metal filling on the chip. Therefore a dummy structure was introduced to represent the capacitor and metal filling. As demonstrated in the previous chapter, all substrate characteristics were imported into HFSSTM, and the structure was simulated using a 50Ω lumped port to excite the antenna.

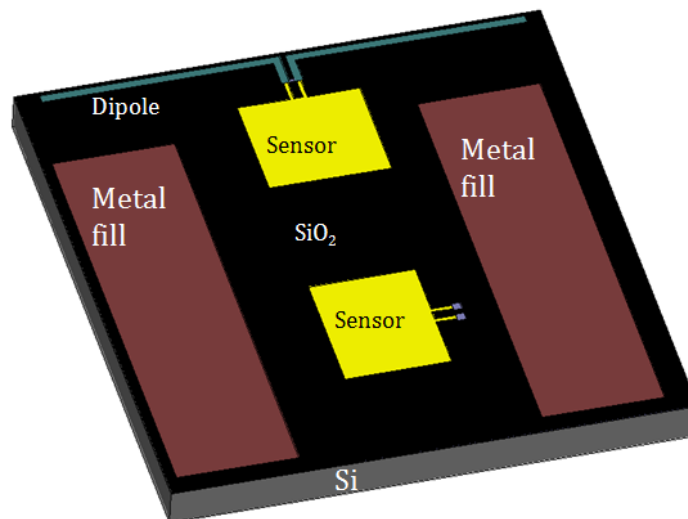


Fig. 5.5. HFSS implantation of sensor array coupled antenna and capacitor sensor.

An air box was defined to the model open space to ensure maximum radiation from antenna with minimum reflected waves. To achieve that, the air box dimensions were set to $(\lambda/4)$ of the resonant frequency of the antenna.

The total antenna length is 3.8 mm with a metallic width of $80 \mu\text{m}$. The antenna was made to operate at approximately 11.5 GHz (towards the upper frequency of X band); however loading the antenna with the sensor lowered the resonant frequency to 8.7 GHz as shown in figure 5.6.

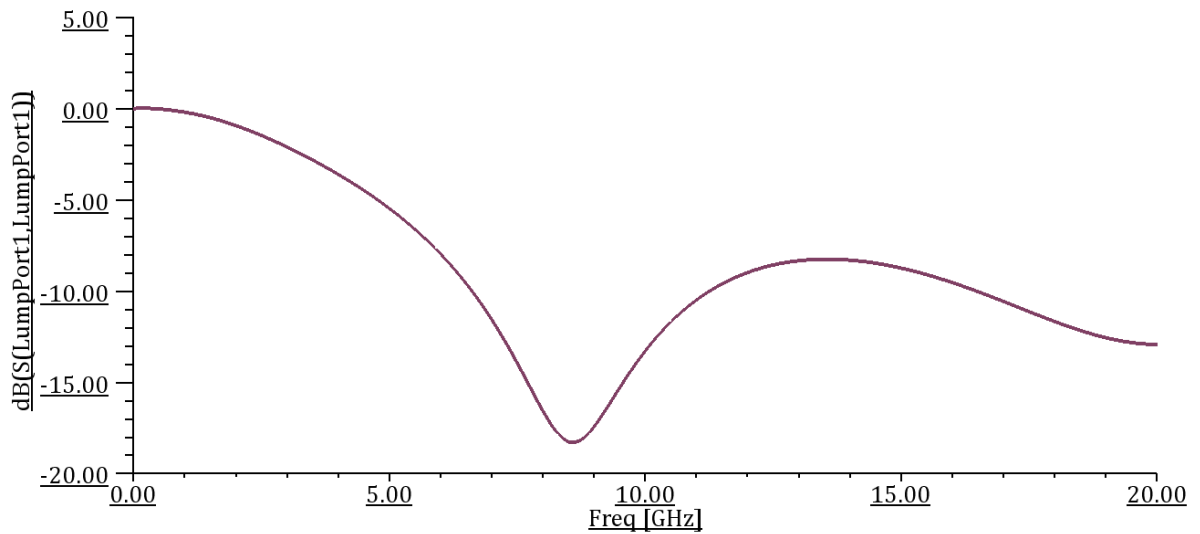


Fig.5.6. Simulated resonance frequency of loaded antenna with dummy cap-sensor.

5.4. Sensor Design and fabrication

5.4.1 Design

The sensor was designed using an array of Metal-Insulator-Metal capacitors on a membrane. The capacitor cell is constructed using Metal-3 and Metal-4 (two top metal layers) and silicon nitride as a dielectric layer. Figure 5.7 (a) shows a sketch of the capacitor structure and (b) illustrates a microphotograph of the capacitor used in this process (shiny lines represent metal electrodes).

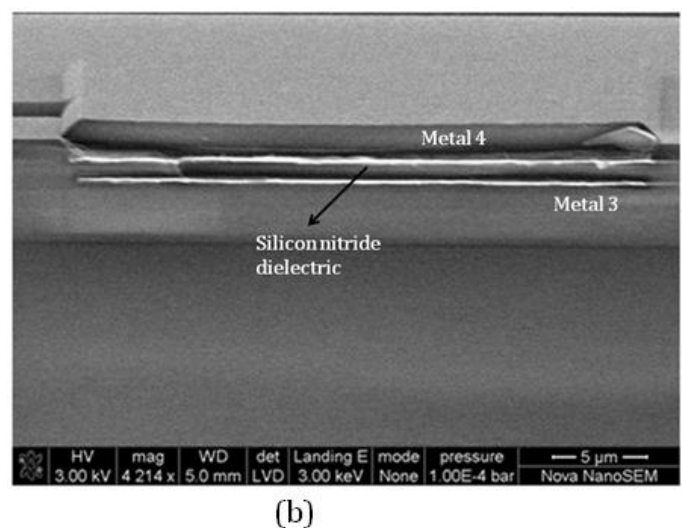
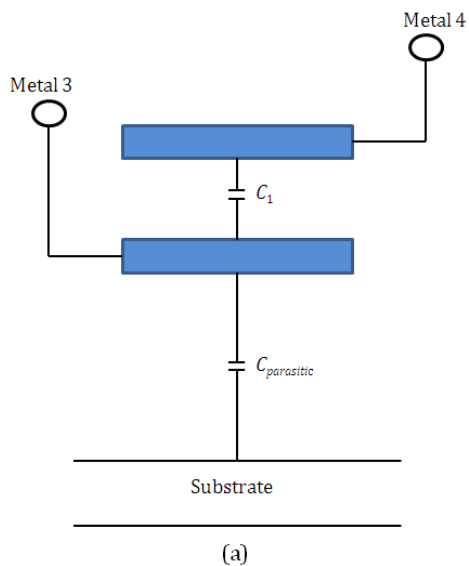


Fig.5.7. (a) Capacitor structure and (b) A microphotograph of MIM capacitors.

A small signal model (lumped element) for MIM capacitor is shown in figure 5.8. In this circuit, losses are expected due to parasitic resistance existing in the electrodes and parasitic capacitance between top and bottom electrodes and ground which is represented by C_{ox-1} and C_{ox-2} respectively.

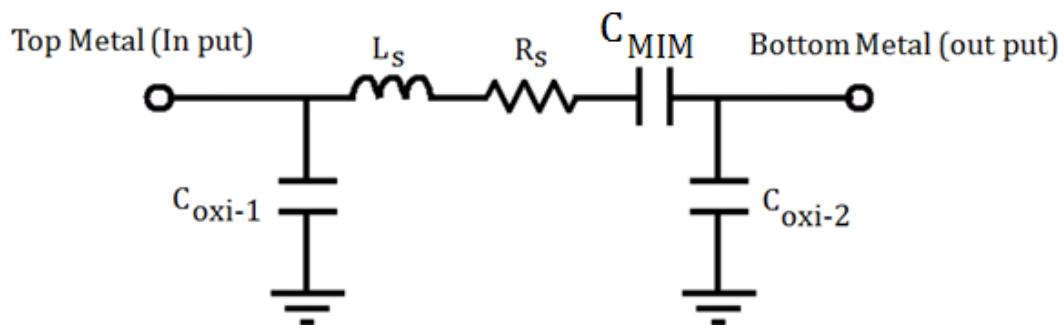


Fig.5.8. MIM capacitor lumped element.

The design should cover two important criteria. The first is to design a large array to provide higher sensitivity. The second target is to design the array with overall small and detectable capacitance. To achieve this, the sensor array was connected in series and parallel, starting from a single $30 \times 30 \mu\text{m}^2$. The membrane area was $1.4 \times 1.4 \text{ mm}^2$ placed in the middle of 4 mm^2 CMOS chip.

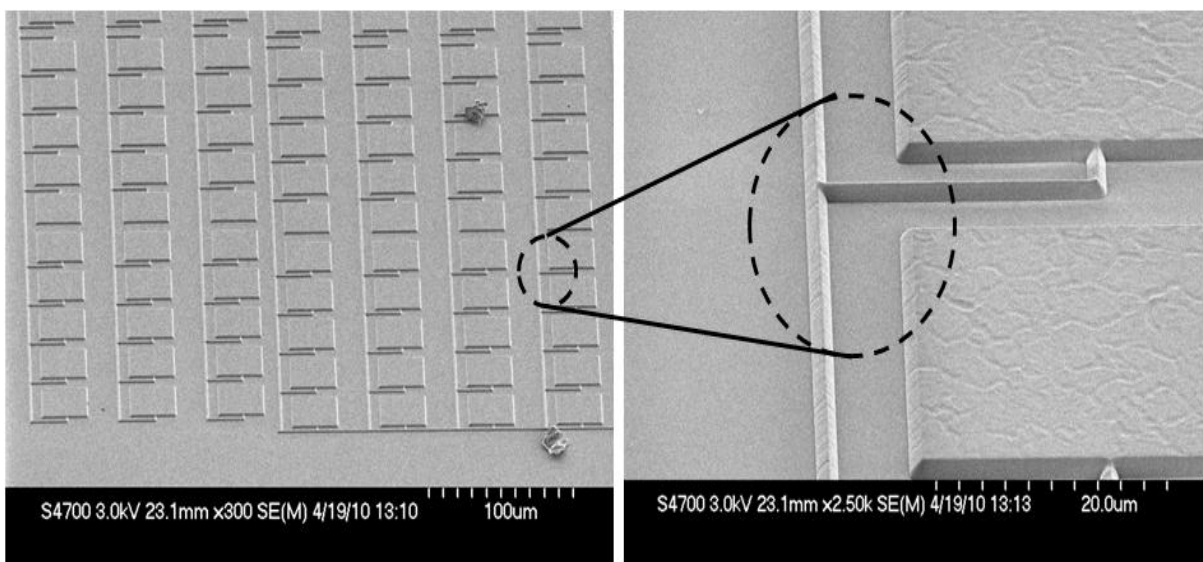


Fig 5.9. Microphotographs of capacitor array.

The layout of the array was corrected several times to achieve a closer matching between schematic and layout. Several techniques were used to reduce the parasitics RLC . The distance between capacitors was $10 \mu\text{m}$ in the x and y directions. The width of

M3 and M4, used for an interconnect between capacitors, was $1\ \mu\text{m}$ (Fig 5.9). The direct contact between antenna and cell array's I/O was M4 with larger width ($50\ \mu\text{m}$) to ensure a good contact and large resistivity. To achieve the density filling requirement, a dummy structure consisting of all metal and polysilicon layers were used to fill empty space on the chip. Additionally, a design for test (DFT) structure was used to establish a direct relation between capacitance and pressure with only I/O $82 \times 90\ \mu\text{m}^2$ analog pads.

In order to test the capacitance of the cells in Cadence software, a low pass filter that consists of (DFT) and $1\ \text{K}\Omega$ (RC) was used. The power gain magnitude frequency response of a first order low pass filter was used to establish the value of the capacitor sensor.

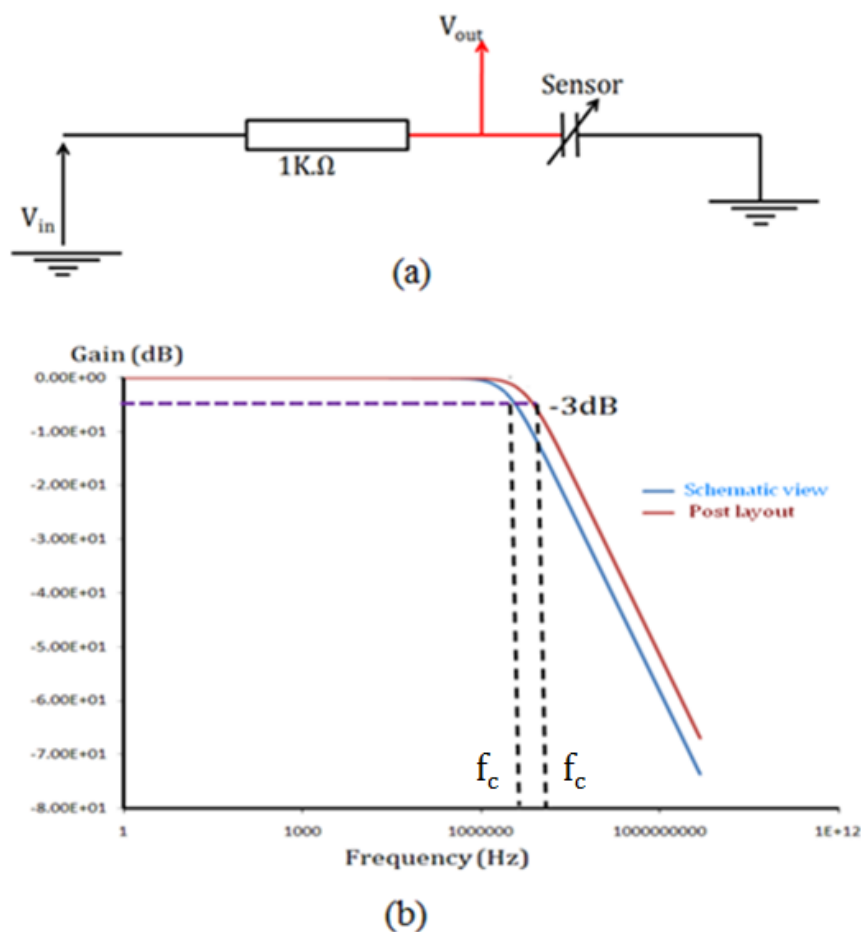


Fig. 5.10. (a) RC circuit to evaluate the sensor and (b) AC response.

The reactance of the capacitor is high at low frequencies and blocks any current flow through the capacitor. After this cut-off frequency point the response of the circuit decreases giving a slope of -20dB/Decade. Signals above this frequency become greatly attenuated, until, at very high frequencies, the reactance of the capacitor becomes so low that it gives the effect of a short circuit condition on the output terminals resulting in zero output. The cut-off frequency occurs at the frequency point where the capacitive reactance and resistance are equal. When this occurs the output signal is attenuated to -3dB ($20 \log (V_{out}/V_{in})$) of the input.

As shown in figure 5.10(b), the difference between simulations (schematic and post-layout) is clear to be seen. This is due, as mentioned earlier, to parasitic (RLC) components. The capacitance was measured using equation (5.1) as

$$C(pF) = \frac{1 \times 10^{12}}{2\pi R f_c} = 3pF \quad (5.1)$$

However, the array capacitance value increases considerably to 5 pF for post layout simulation.

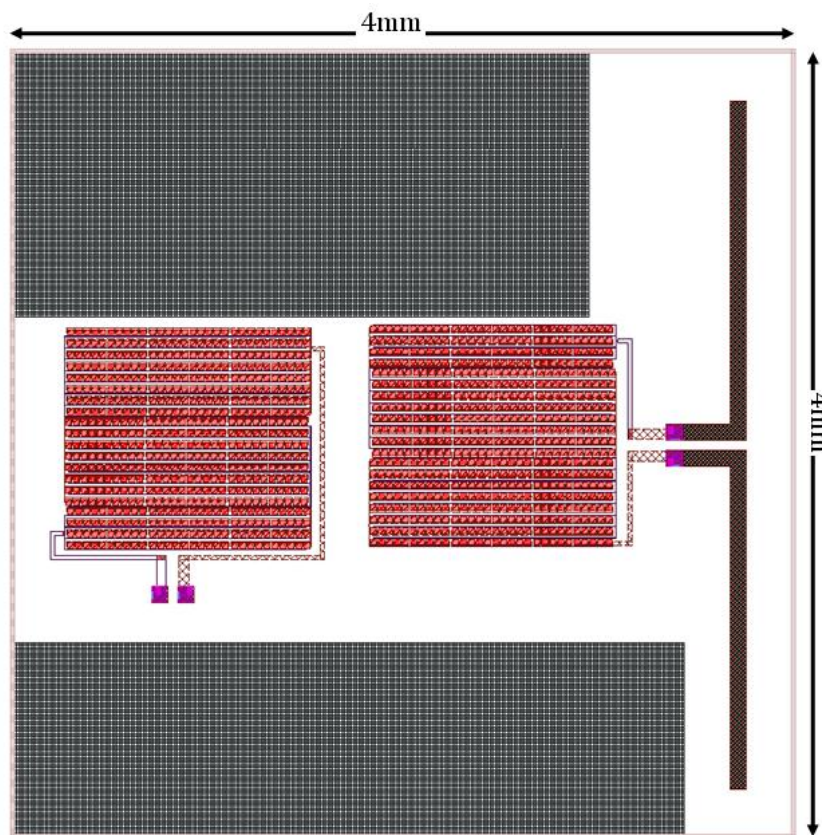


Fig.5.11. Complete layout of chip.

5.4.2 Chip post processing

Traditionally CMOS-MEMS capacitor pressure sensors use the same capacitor and Poly1-Poly2 devices. Usually, front and back post processing of a CMOS chips is required to realise the device (front and back side processing). For the front side fabrication, the process involves removing the passivation layers, and removing the dielectric layers between the electrodes of the capacitor. The back side process involves etching the silicon substrate to form the sensing area.

Here, we fabricated a novel capacitor pressure sensor without any requirement of front side processing and keeping the dielectric silicon nitride between the electrodes. Post processing starts with the chips been cleaned from any possible contamination using Isopropanol-Acetone in an ultrasonic bath for 5 minutes. This procedure ensures the removal of silicon particles that occur as a consequence of the sawing of the actual wafer by the foundry. The chips were dehydrated for 10 minutes in a 90 °C oven. The samples were mounted on 20 x 20 mm² thin glass wafer for better handling and processing. This was achieved by depositing an 8 µm thick layer of AZ4562 on top of the glass wafer through spin coating, and then mounting the chip in the middle as shown in figure 5.12. To ensure good adhesion the structure was baked for 15 minutes in a 90 °C oven.

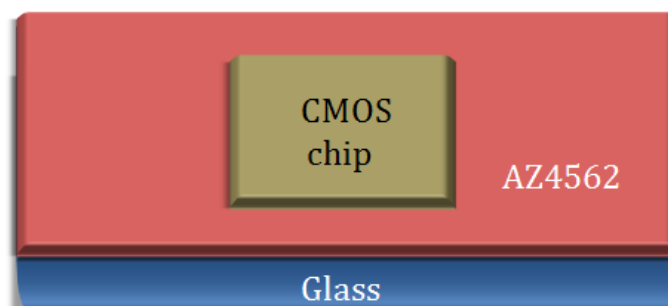


Fig.5.12. Proper handling of a CMOS chip for post processing.

The thickness of the CMOS chips were 516~520 microns. To etch all the way through the silicon using Inductive Coupled Plasma (ICP), a thick mask layer is needed, this prevents the etchant gases attacking other areas on the chip. This was achieved by spin casting AZ 4562 at 8000 rpm for one minute and baking for 30 minutes in a 90 °C oven, the thickness of the photoresist was 4 µm.

The process was repeated six times to ensure a thick layer of AZ 4562, resulting in a final photoresist film thickness of 24 µm. A square pattern was lithographically

transferred using a Suss Microtec mask aligner with exposure to UV light for 40s, hard contact and a 120 μm alignment gap. The chips were immersed in AZ 4000 developer, with concentration of 4:1. The chips are then cleaned with RO water and dehydrated for 4 minutes 90 $^{\circ}\text{C}$. An opening area of 2 mm^2 on the back side of the CMOS chip insures a successful photolithography process. The samples were cleaned using H_2O_2 and dehydrated for 10 minutes at 90 $^{\circ}\text{C}$.

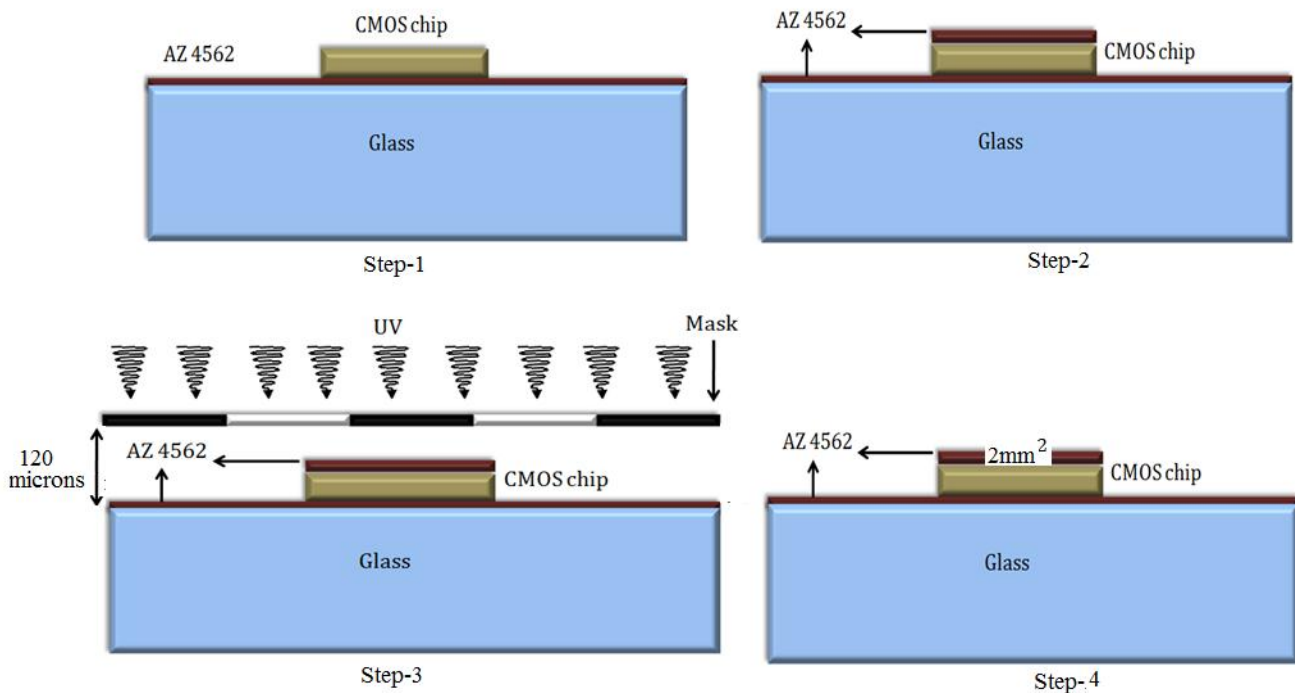


Fig.5.13. Process diagram of photolithography using AZ 4562 as a photoresist.

The samples are prepared for ICP Deep Reactive Etching (RIE) by mounting the devices on a 4 inch silicon carrier wafer. This was done by spinning a thick AZ 4562 as a contact layer between samples and the carrier. Good adhesion was achieved by baking at 120 $^{\circ}\text{C}$ for 20 minutes. The process serves as a hard bake processing step for the samples, to add more strength and greater adhesion for the remaining photoresist. Furthermore, hard baking ensures the remaining photoresist will not be removed by the etching.

Inductive coupled plasma etching was the method of choice since it has several advantages over KOH wet etching. First the etch rate is faster than KOH etching. The second advantage is the etchant area provided by ICP etching is larger than KOH. This is because KOH etch produces side walls of 54.72° for $\langle 100 \rangle$ orientation, compared with almost 90° provided by ICP etching, and hence, a larger sensing area. The samples were etched first for 30 minutes and the depth of etching was measured using Dektak stylus

profilometer. This was an important procedure to determine the etch rate and hence provide a better approximation for the time remaining to release the membrane. The etch rate was $4.16 \mu\text{m}/\text{min}^*$ and since the thickness range was between $516\sim 520 \mu\text{m}$, the overall time for etching was between 124 and 126 minutes, resulting in a membrane thickness ranging between 1 and $4 \mu\text{m}$.

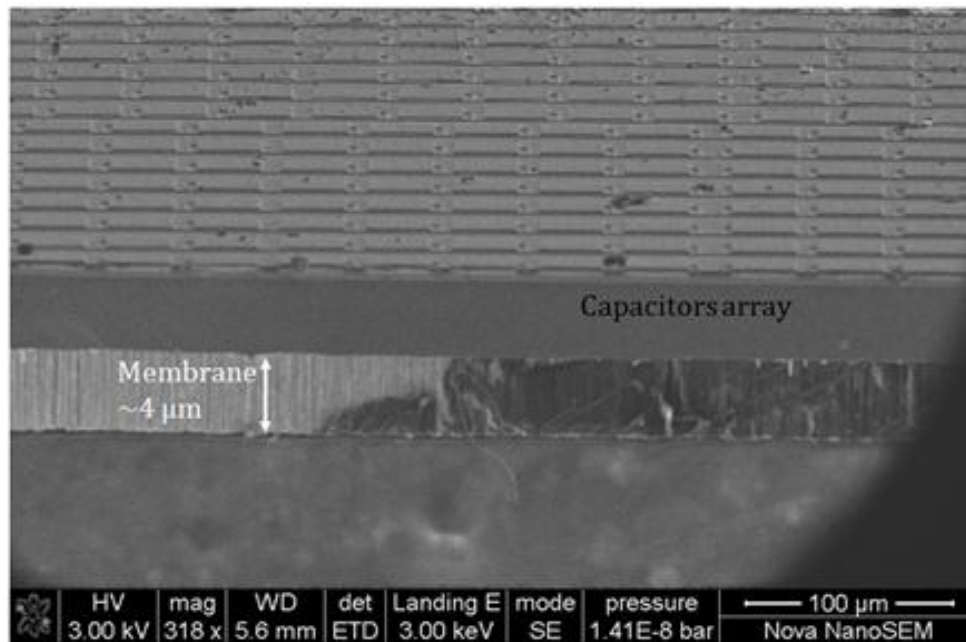


Fig.5.14. A microphotograph of sensor array on $4 \mu\text{m}$ Si/SiO₂ membrane.

To suspend the processed chips from carriers (4 inch wafer and glass), the devices were immersed in hot Acetone for 4 hours. Ultrasonic shake is not an option as it damages the membrane. 1165 microposit is used for further development for one hour to ensure a complete stripping the remaining photoresist.

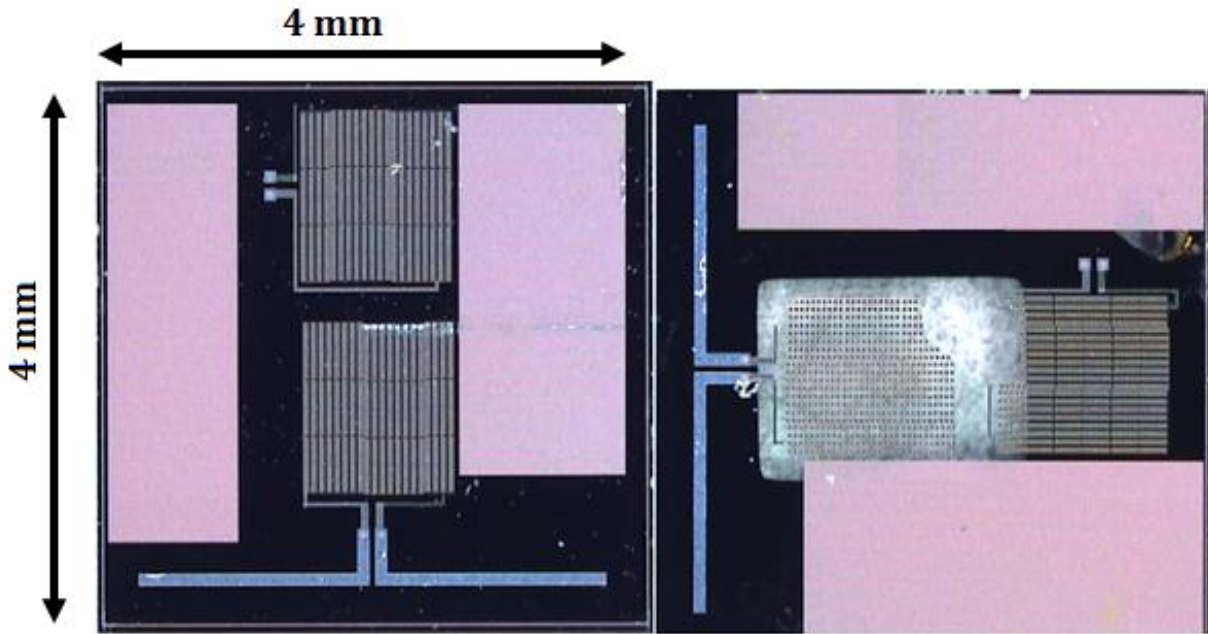


Fig.5.15. Photograph of chip before post-processing (right) and after post-processing (left).

The capacitor array is visible on the figure on the left (brown bars), separated by substrate (black lines). The figure on right shows the array after post processing the CMOS chip, and here, we can see the individual capacitors as dots, on top of transparent silicon dioxide membrane.

5.5. Mechanical properties of composite membrane

It is important to understand the behaviour of a triple layer structure under applied pressure. The presence of un-etched silicon nitride as a dielectric layer for MIM Cap electrodes causes the overall structure to deform resulting in load-deflection bending of the membrane. The capacitance change of the sensor due to membrane bending depends on the mechanical properties of the materials involved, structural dimensions, and the applied pressure. The membrane deflection is assumed to be large since each side length of the membrane is larger than maximum diaphragm thickness. We assume the membrane remains flat when no pressure is applied and the diaphragm is clamped on both sides. The total length of the membrane is equal to $2a$ as shown in figure 5.16 (a). Other important parameters are shown in figure 5.16 (b): h_i , E_i , μ_i , and σ_i correspond to the thickness, Young's modulus, Poisson's ratio, and residual stress of ($i=1, 2, 3... n-1, n$) layer of the multilayer membrane. The composite average strain of the diaphragm is represented by ε_σ .

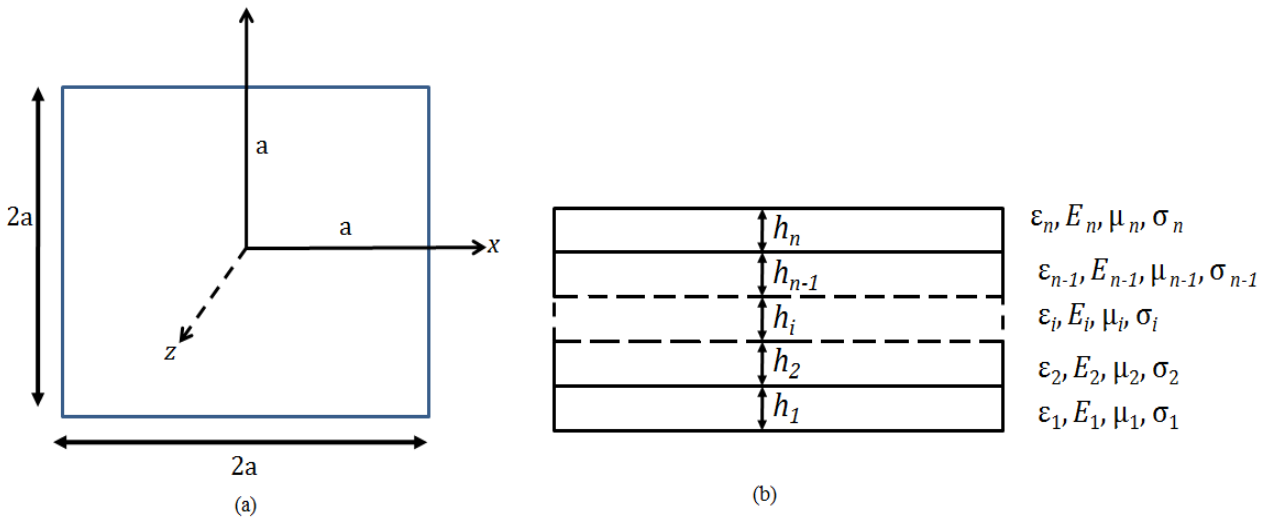


Fig.5.16. (a) Coordinate axis of a square membrane with length equal to $2a$. (b) Parameters of multilayer membrane, where $2a \gg h$.

The relationship between stress and strain is represented by:

$$\sigma_i = E_i \varepsilon_i, \quad i = (1, 2, \dots, n) \quad (5.2)$$

Multiplying equation (4.1) by h_i leads to:

$$\overline{\varepsilon_\sigma} \sum_{i=1}^n E_i h_i = \sum_{i=1}^n \sigma_i h_i \quad i = (1, 2, \dots, n) \quad (5.3)$$

The average strain could be written as:

$$\bar{\varepsilon}_\sigma = \frac{\sum_i^n \sigma_i h_i}{\sum_i^n E_i h_i} \quad (5.4)$$

This leads to average stress $\bar{\sigma}$:

$$\bar{\sigma} = \frac{\sum_i^n \sigma_i h_i}{\sum_i^n h_i} \quad (5.5)$$

Assume u, v, w are the displacement at x, y and z directions. Since the membrane is lying on x - y plane with its middle surface at $z=0$, the total strain $\varepsilon_x, \varepsilon_y$ and shear stress γ_{xy} are given by:

$$\varepsilon_x = \frac{\partial u}{\partial x} + \frac{1}{2} \left(\frac{\partial w}{\partial x} \right)^2, \quad \varepsilon_y = \frac{\partial v}{\partial y} + \frac{1}{2} \left(\frac{\partial w}{\partial y} \right)^2, \quad \gamma_{xy} = \frac{\partial u}{\partial x} + \frac{\partial v}{\partial y} + \frac{\partial w}{\partial x} \frac{\partial w}{\partial y} \quad (5.6)$$

The boundary conditions for a clamped membrane are given by:

$$u(x, y) = u_0 \sin \frac{\pi x}{a} \left(1 + \cos \frac{\pi y}{a} \right) \quad (5.7)$$

$$v(x, y) = u_0 \sin \frac{\pi y}{a} \left(1 + \cos \frac{\pi x}{a} \right)$$

$$w(x, y) = \frac{w_0}{4} \left(1 + \cos \frac{\pi x}{a} \right) \left(1 + \cos \frac{\pi y}{a} \right)$$

u_0 and w_0 represent the maximum displacements in and outside of the plane respectively.

The total load deflection w_0 due to applied uniform pressure at centre of membrane is given by:

$$P = C_1 \frac{(\sum_{i=1}^n h_i)^3 w_0^2}{a^4} \sum_{i=1}^n \frac{E_i}{1 - \mu_i^2} \quad (5.8)$$

$$+ \frac{w_0^3}{a^4} \left[C_2 \sum_{i=1}^n \frac{E_i h_i}{1 - \mu_i^2} + C_3 \cdot f \sum_{i=1}^n \frac{E_i h_i (-1 + 3\mu_i)}{1 - \mu_i^2} + C_4 \cdot f^2 \sum_{i=1}^n \frac{E_i h_i}{1 - \mu_i^2} \right]$$

The relation between deflection w_0 and capacitance change was already illustrated in equation (2.4). C_1 represents the linear parameter between the pressure P and large deflection w_0 under large deformation. C_2, C_3 and C_4 are the non-linear relation between pressure and the cubic term of deflection w_0 . The parameter f depends on material type, and the geometry of membrane. These values could be written as:

$$C_1 = \frac{\pi^4}{72}, C_2 = \frac{65\pi^4}{2048}, C_3 = \frac{\pi^4}{512}, C_4 = \frac{\pi^4}{1024}, f = \frac{\sum_{i=1}^n \frac{E_i h_i (1 - 3\mu_i)}{1 - \mu_i^2}}{\sum_{i=1}^n \frac{E_i h_i}{1 - \mu_i^2}} \quad (5.9)$$

Table 4.2 below shows the parameters used to estimate the relation between pressure and the deflection of composite membrane.

Parameter	Thickness	Young modulus	Poisson ratio
Metal-4	0.9 μm	95 GPa	0.3
Metal-3	0.5 μm	95 GPa	0.3
Silicon nitride	0.6 μm	270 GPa	0.24
Silicon dioxide	$\sim 1\text{-}4 \mu\text{m}$	170 GPa	0.22

Table 5.2 multilayer capacitor parameters.

Figure 5.17 shows the estimated pressure-deflection curve using equation 5.8 and table 4.2. The value of the deflection becomes smaller for thicker membranes.

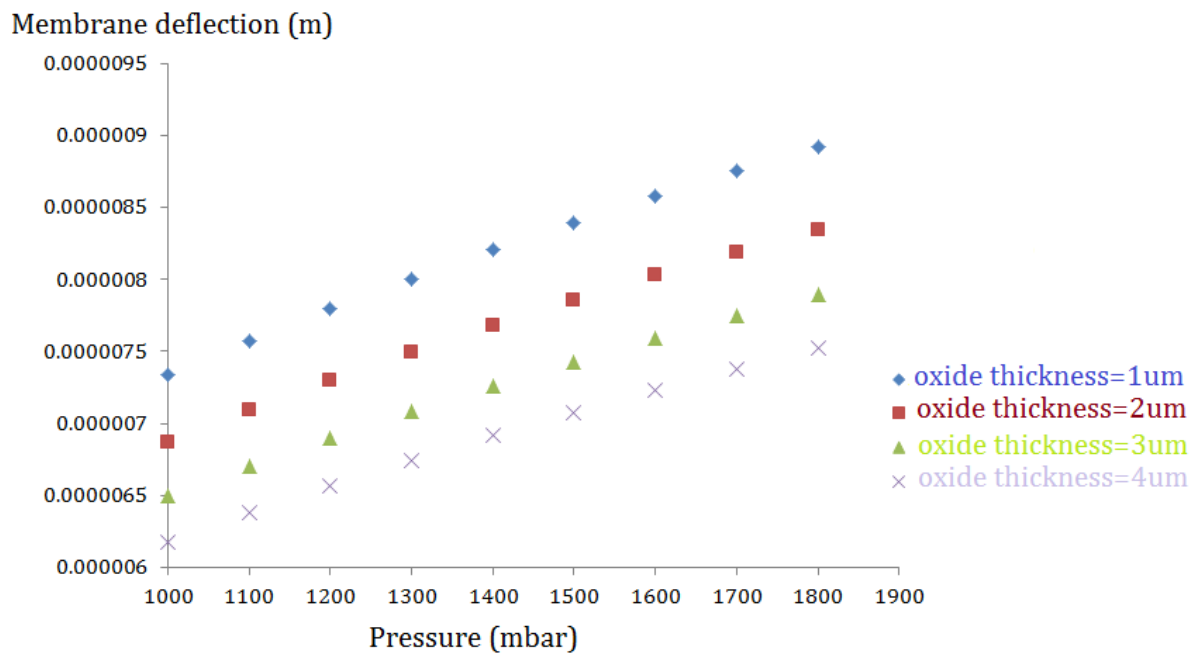


Fig.5.17. Estimated pressure-deflection for composite membrane.

5.6. Summary

In this chapter, the design and fabrication of a passive CMOS-MEMS wireless pressure sensor is presented. An on chip transmitter/receiver circuit (antenna) is tuned using a novel capacitive pressure sensor. The sensor consists of capacitor array covering an area of 2 mm^2 , inside a membrane. Design and layout verification are carried out with Cadence virtuoso using National-semiconductor $0.35 \text{ }\mu\text{m}$ design kit. The final chip area is only 16 mm^2 . Post processing of the CMOS chip is carried out only from the back, unlike traditional post processing (top-bottom) to release a membrane. The fabrication techniques involve optical lithography followed by Inductive Coupled Plasma deep etching. The resulting membranes have supporting silicon thicknesses ranging between 1 and $4 \text{ }\mu\text{m}$. Estimation for the mechanical behaviour of the membrane is also shown, indicating a larger deflection ($7.3\text{-}9.0 \text{ }\mu\text{m}$) with one micron supporting silicon, compared to silicon support of $4 \text{ }\mu\text{m}$ ($6.1\text{-}7.5 \text{ }\mu\text{m}$) for the same pressure range.

Chapter 6

6. Pressure sensor results

In situ pressure sensor and CMOS-MEMS capacitive pressure sensor were designed and fabricated in chapters 4 and 5. The simulation and experimental results from testing are shown in this chapter. The chips are packaged in a simple method and tested to verify their behaviour to pressure. This chapter describes the testing methods for the on chip antenna, the wireless sensing with aided diagrams and finally presents the results.

6.1 Meander and zigzag antennas: simulation and measurement

The Simulation results were obtained for the meander antenna after implementing all of the substrate parameters in HFSS. The testing environment of device was also considered as an additional microwave absorber chuck with very low dielectric. This was added to our design as illustrated in figure 6.1. For simulation a frequency range between 50 MHz and 20 GHz was chosen as the resonant frequency is expected to be 10 GHz. The selected range also shows other resonant frequencies may occur due to surface modes (equation 3.11).

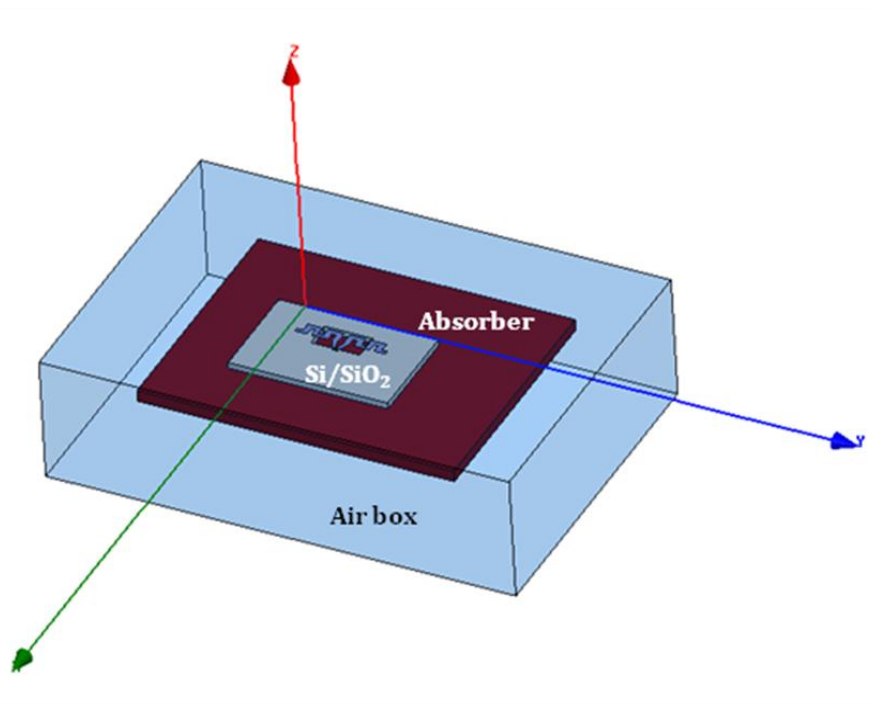


Fig.6.1. HFSS design for a meander antenna.

All substrate and antenna parameters discussed in chapter 4 were implemented in the software for optimum matching. A $50\ \Omega$ lumped port and a microwave absorber were also used to replicate the devices testing environment.

After antenna fabrication, the wafer was then diced into $5 \times 5\ \text{mm}^2$ chips. The chips were tested using an Agilent E8362B network analyzer (VNA). A single chip was placed on a low dielectric material (Styrofoam) to negate any external coupling from the surrounding metallization (figure 6.2).

The experimental results for S_{11} are shown in figure 6.3. To further consider the effect of the silicon substrate presence behind the membrane, experimental results before and after etching were obtained.

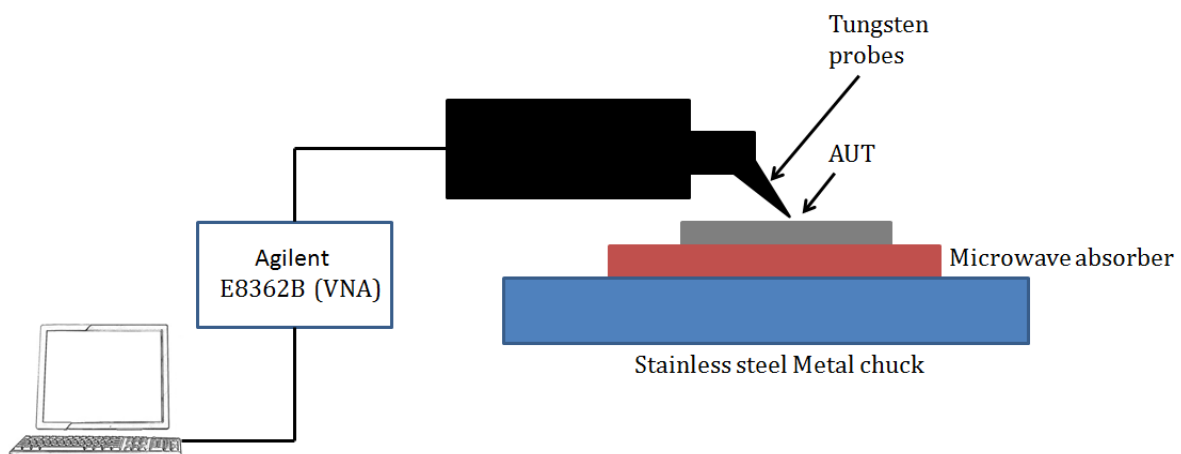


Fig.6.2. Sketch of test equipment for antennas. The antenna under test (AUT) is probed using $50\ \Omega$ impedance tungsten wires.

Simulation and experimental results for meander dipole antenna are shown in figure 6.3.

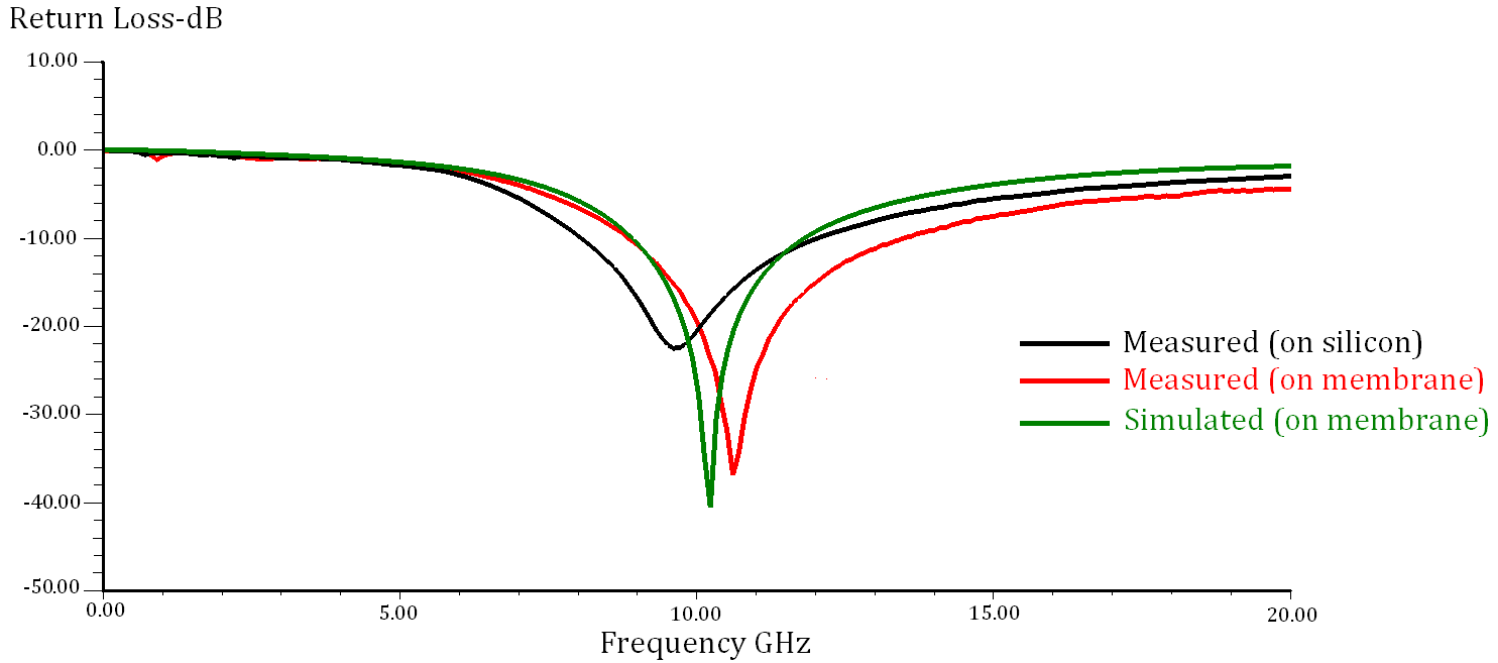


Fig.6.3. Simulated and measured results for the meander antenna.

The characteristic impedance was also extracted from the measurement results. The Smith chart shown in figure 6.4 shows the real and imaginary parts of the meander antenna's input impedance.

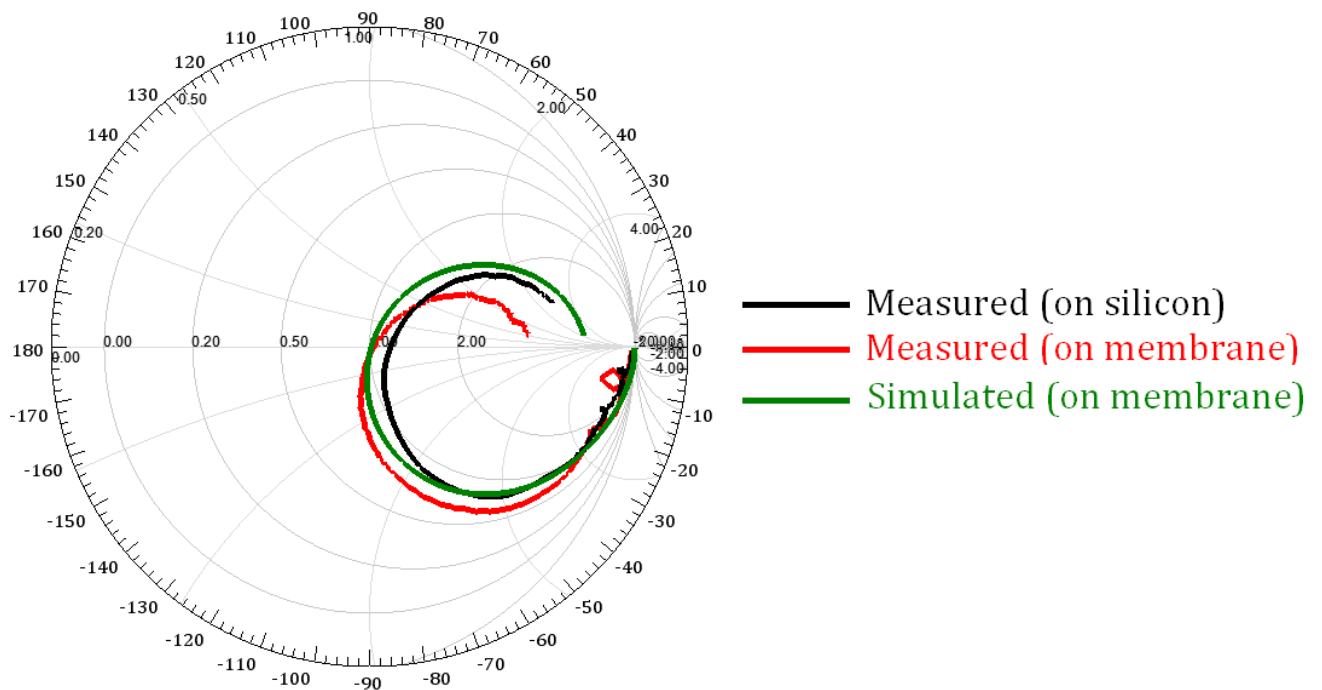


Fig.6.4. Meander antenna response to a normalized to 50 Ω input impedance.

Similarly, the zigzag antenna which was designed in HFSS is shown in figure 7.5 with same characteristics as the meander antenna.

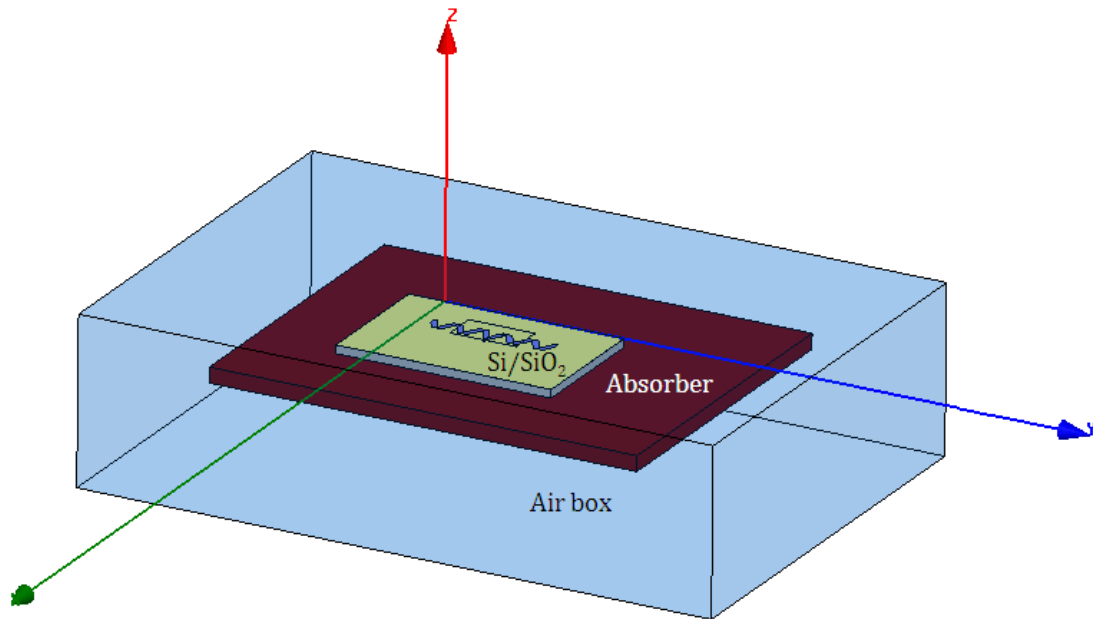


Fig.6.5. HFSS design for zigzag antenna.

Results obtained from the zigzag antenna show a resonant frequency of 10 GHz for measurement on membrane, an increase of 0.4 GHz for the same antenna with the presence of silicon behind antenna. The characteristic impedance is shown in figure 6.7.

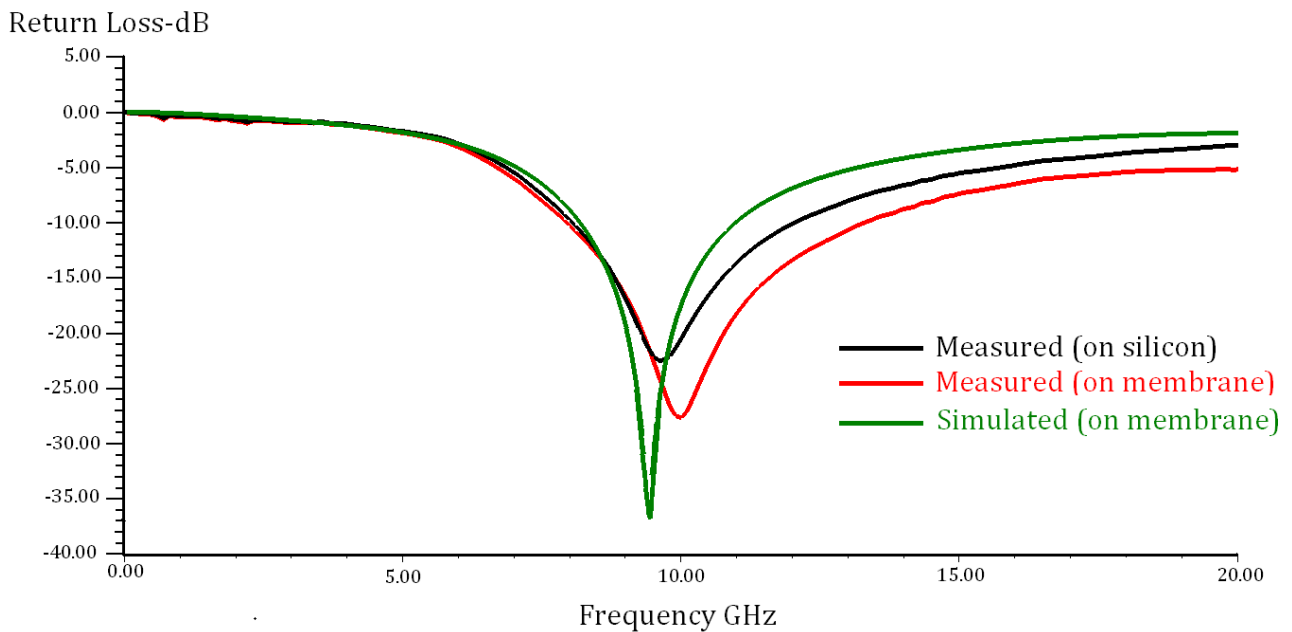


Fig.6.6. Simulated and measured results for the zigzag antenna.

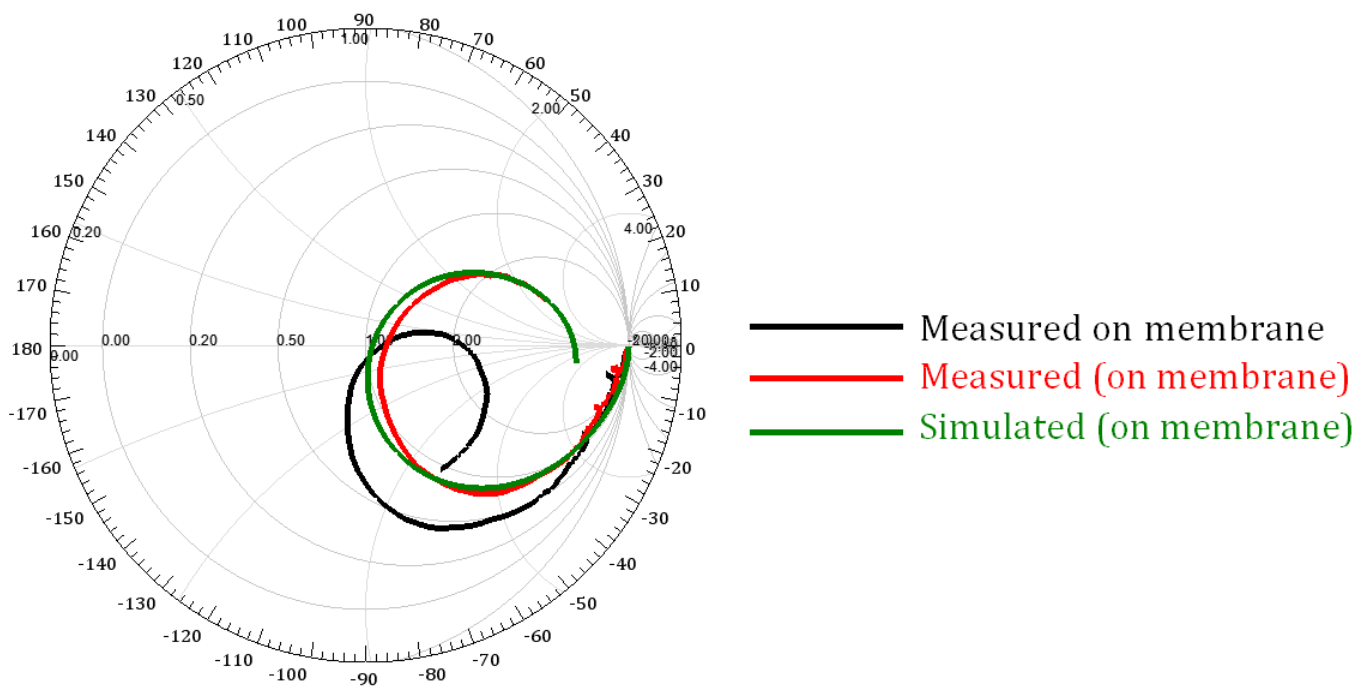
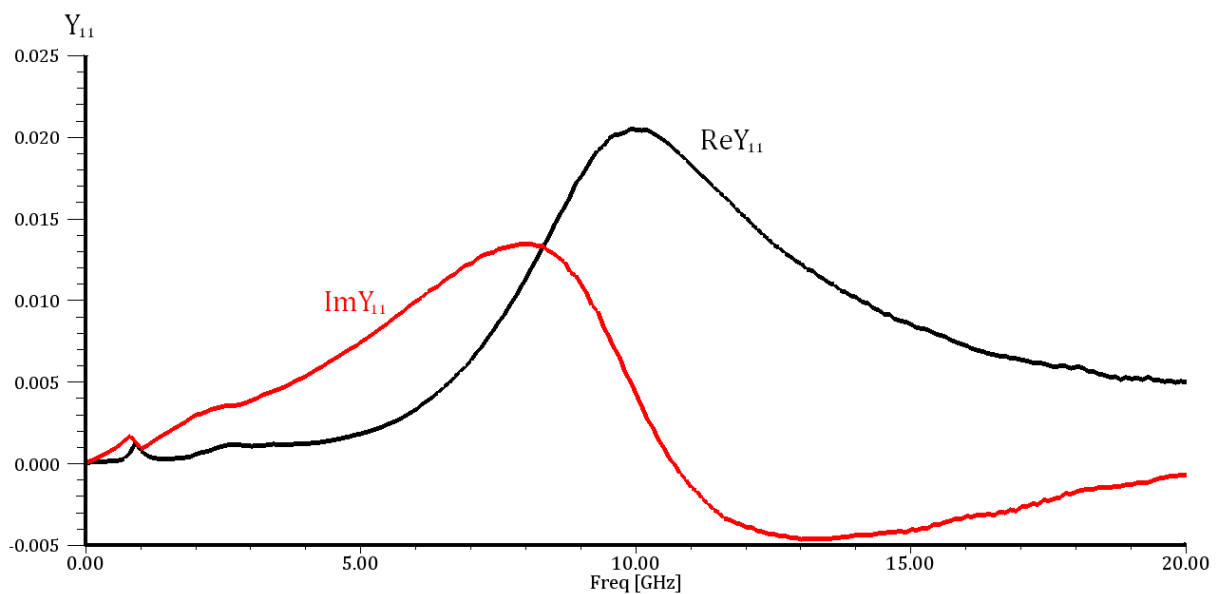


Fig.6.7. Zigzag antenna response to a normalized to 50Ω input impedance.

Another method was used to measure the input impedance of both antennas. As discussed earlier in this thesis, HFSS has the capacity to extract Z and Y parameters from S parameters. Figure 6.8 shows Y_{11} for both antennas.



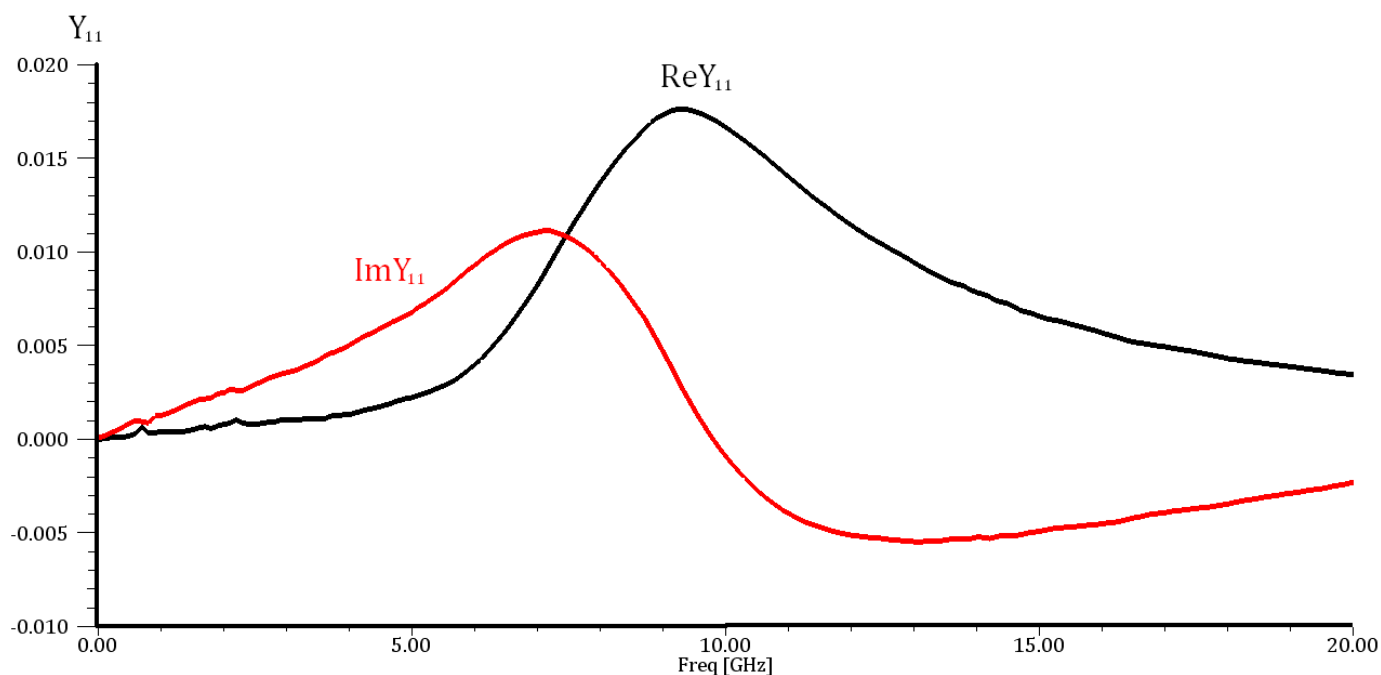


Fig.6.8. Meander (top) and zigzag (bottom) antenna Y parameters.

The real and imaginary parts are calculated using the formula ($Z_{11}=1/Y_{11}$). Table 6.1 summarizes the measured and simulated parameters.

Meander antenna		Parameters		
Result method	Return loss (dB)	F_c (GHz)	Impedance (Ω)	-10 dB-BW %
Simulated on membrane	-40.45	10.22	$50.85 + j 0.435$	32.00
Measured prior etching	-26.80	9.90	$55.95 - j 0.475$	43.20
Measured on membrane	-36.80	10.60	$51.2 + j 0.050$	44.50
Zigzag antenna		Parameters		
Result method	Return loss (dB)	F_c (GHz)	Impedance (Ω)	-10 dB-BW %
Simulated on membrane	-37.40	9.40	$51.4 + j 0.10$	31.00
Measured prior etching	-22.50	9.60	$57.35 - j 3.30$	48.00
Measured on membrane	-27.65	10.00	$56.15 + j 0.09$	52.00

Table 6.1. Simulated and Measured results for micromachined antennas.

There is a slight discrepancy between simulation and measurement results as shown in table 6.1. In general, when designing antenna, the performance of the experimental results usually differ from the simulated results. This can be attributed to different

factors such as design equation error, improper use of the software, fabrication tolerance and interface between antenna and feed cables, and interface between antenna and surrounding environment.

In our design, we attribute this discrepancy to surrounding metal parts of the test equipment and some fabrication tolerance. This includes the resistivity of the substrate, which ranges between 3 K Ω .cm and 5 K Ω .cm in some regions in the wafer. Other factors attributed to fabrication tolerance are

- The thickness of the Aluminium sputtered which varies between devices between 0.7 and 1 μ m
- The effective permittivity of the silicon dioxide deposited during the first step of fabrication. Silicon dioxide has permittivity between 3.7 and 4.
- Membrane thickness, which varies between 1.5 to 4 microns as shown in chapter 4.

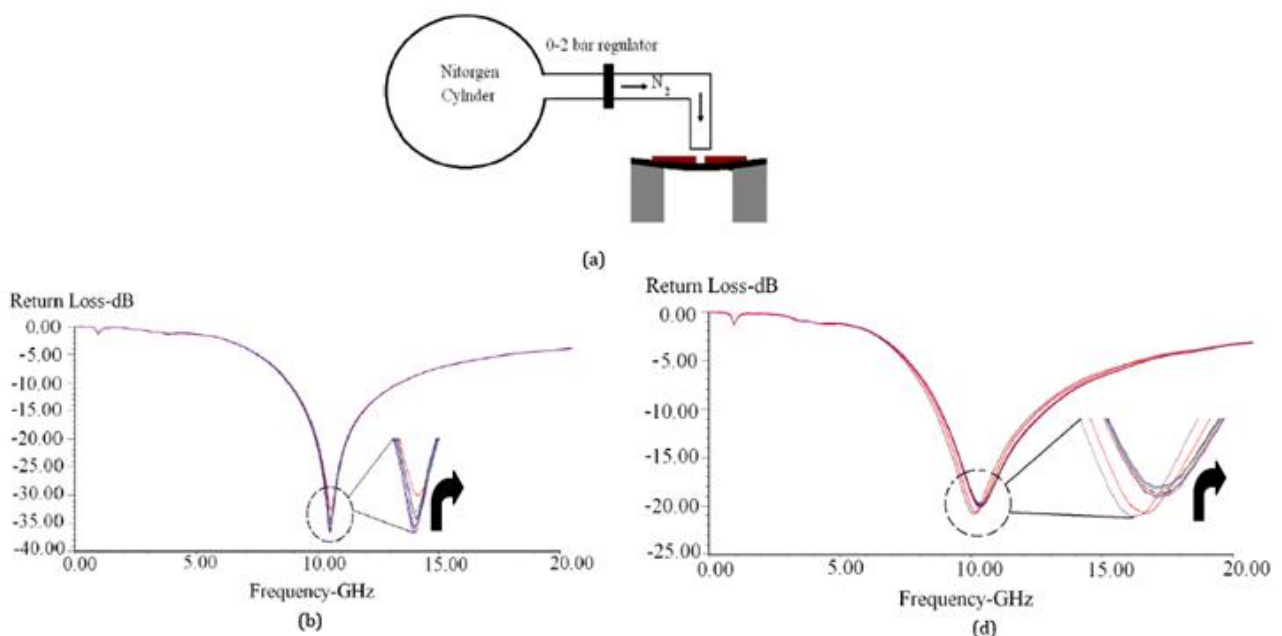
Also from the table, we can observe the close link between the resonant frequency and the presence of silicon behind the antenna. The resonant frequencies of both antennas gradually increase by 0.7 and 0.4 GHz for meander and zigzag antennas respectively. As shown in chapter 4, resonant frequency is inversely proportional to the amount of dielectric constant of material. As the amount of $\sqrt{\epsilon_r}$ in equation 4.1 decreases (by etching), the resonant frequency increases.

Also the effects of etching are clearly shown on impedance bandwidth and the value of return loss. Impedance bandwidth, calculated using equation 3.19 showed an increase from 48 % to 52 % for the zigzag antenna and from 43.20 % to 44.50 % for the meander antenna. Finally, a change of the order of 10 % in $\text{Re}(Z_0)$ is seen between before and after etching. However, as expected, the change in $\text{Im}(Z_0)$ is very large, this is consistent with the change in the return loss.

6.1.1. Pressure measurement

6.1.1.2. Unsuitable measurement

To study the effects of membrane deflection on antennas, a simple un-calibrated experiment was carried out as shown in Figure 6.9 (a). A jet of nitrogen is blown onto the surface of the membrane using a plastic pipette positioned approximately 1 mm from the surface. The gas flow-rate is controlled using a regulator connected to a gas cylinder. The pressure at the output of the regulator is in the range 1.0 to 1.4 bar. Using this simple method, changes in the resonant frequency of 10.6-10.62 GHz for the meander and 10-10.325 GHz for the zigzag antennas were achieved. This is due to mechanical changes in physical dimensions of antennas (W_s , W_z) and gap between feed lines, as illustrated in figures 4.5 and 4.6. As the data in Figure 6.9 (b, c) shows the meander antenna shows a continuous shift in the resonant frequency throughout the experimental pressure range. By contrast, the zigzag antenna shows a more pronounced shift in the frequency for pressure as gas flow increases. At higher gas flow there is little further shift in the frequency (Figure 6.9 (d, e)).



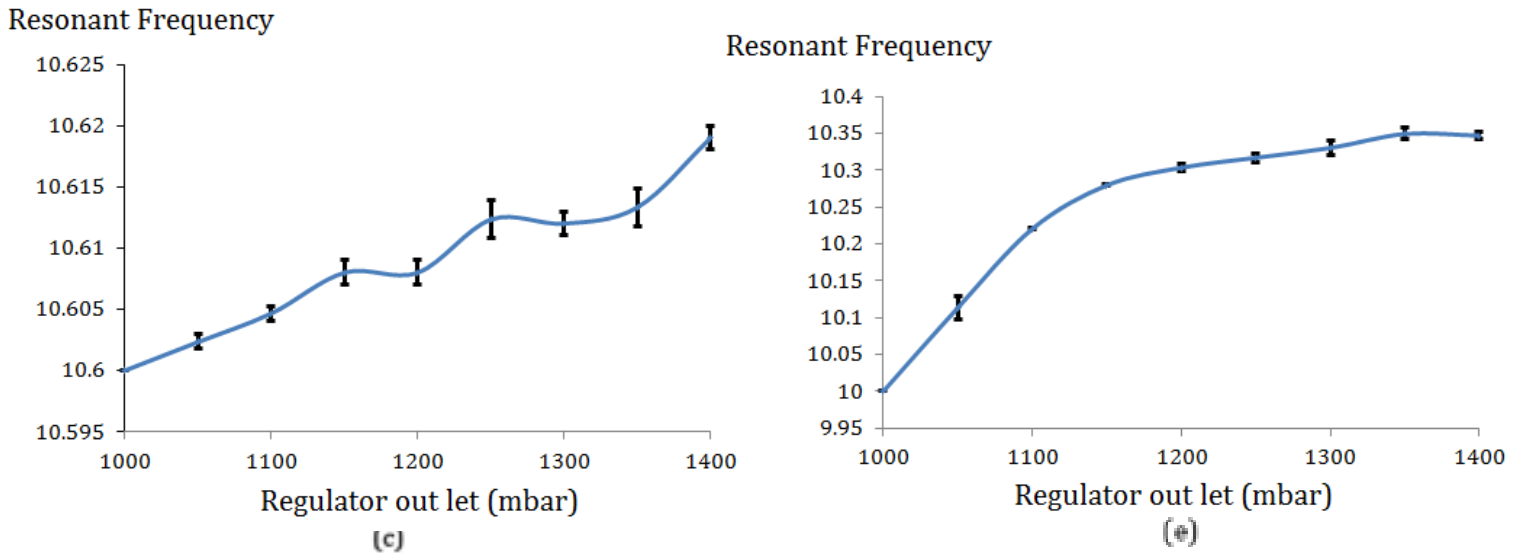


Fig. 6.9. (a) Simple experiment setup. (b) and (c) Resonant frequency shift for the meander dipole antenna. (d) and (e) Resonant frequency shift for the zigzag antenna. The resonant frequency increases with gas pressure, as indicated by the solid arrows.

6.1.1.3. Wireless measurement

Figure 6.10 shows the first calibrated experiment to monitor the pressure frequency relation. A perfectly sealed plastic box was used for this purpose as the device was mounted on top of it. The box was drilled in three positions to provide connections to: an external pressure sensor (Campbell Scientific CS100), a nitrogen source (cylinder) and finally a source to the membrane on device.

A horn antenna, operating at 10 GHz was positioned at a 10 cm distance on top of the device. This distance was controlled using a simple optical rail. The horn antenna is connected to the Agilent E8362B PNA. Inside the network analyser, the illumination power was chosen at -5 dBm and frequency range between 9.5 and 10.5 GHz to monitor the slightest shift in resonant frequency in response to pressure.

The sketch below shows that increasing the pressure using the regulator increases the output (in volts) for the pressure barometer. The calibration starts at 2.7 volts for atmospheric pressure, and ends at 6.5 volts for 1600 mbar. The calibration curve indicates perfect response for the barometer to applied pressure to system.

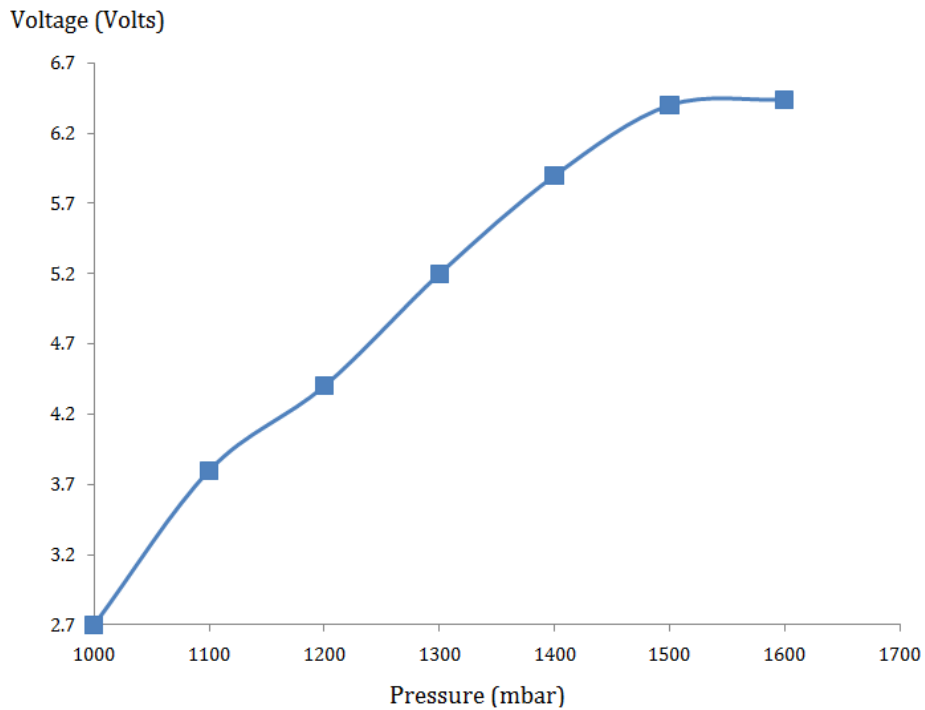
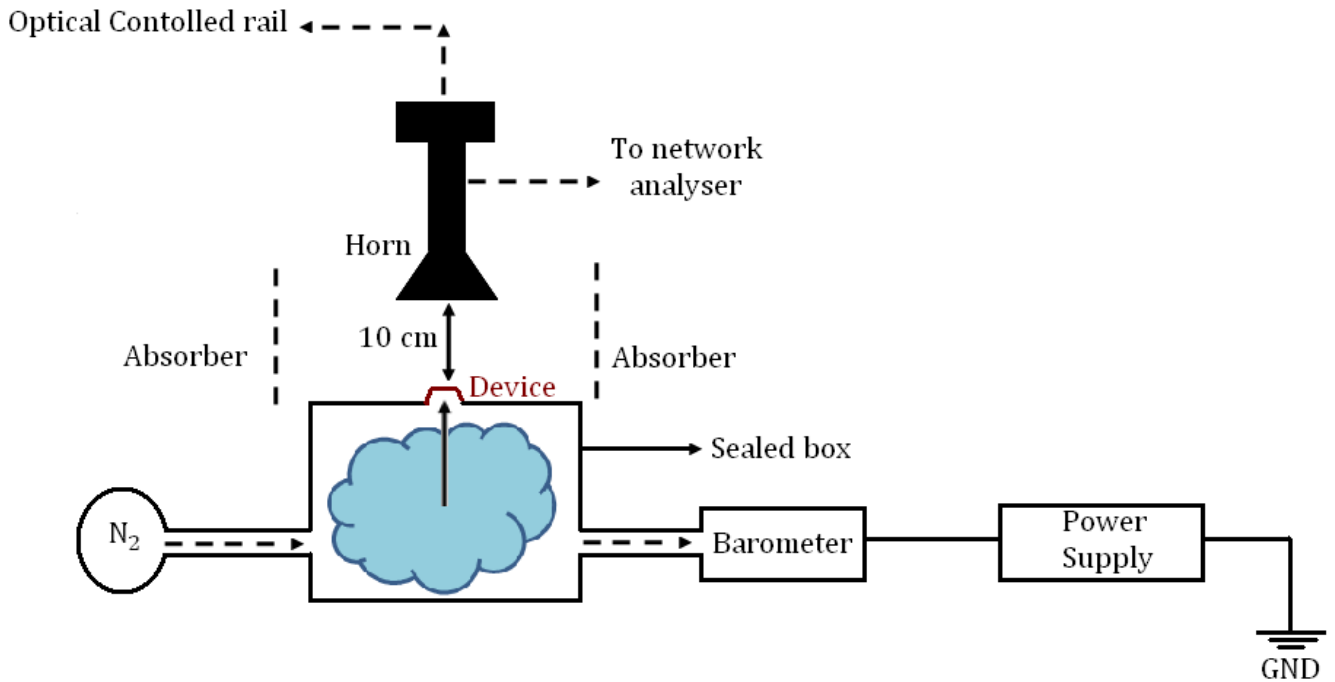
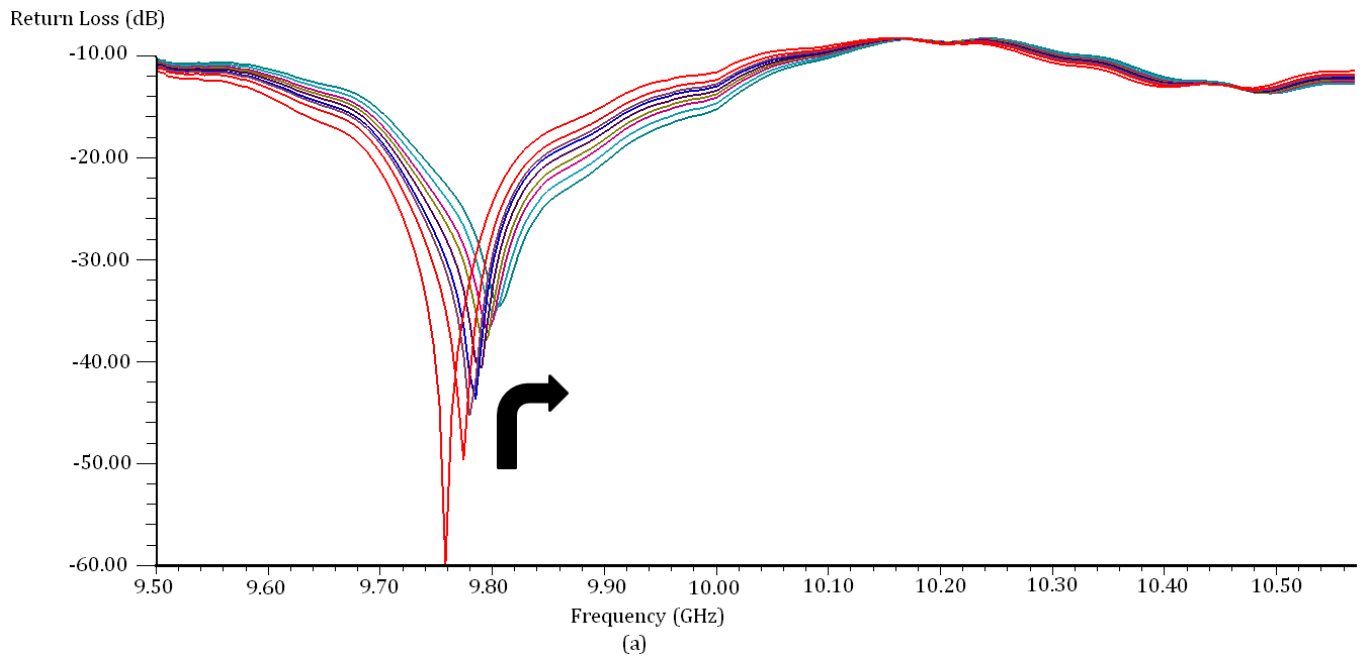


Fig.6.10. Experiment setup for wireless measurement (top) and barometer calibration (bottom).

The results obtained for this experiment are demonstrated in figure 6.11 (a) and (b). The results obtained indicate a resonant frequency shift detected at the horn between 9.75 and 9.90 GHz for a pressure range between 1000 and 1800 mbar. However, the

results obtained using this experiment is inconsistent due to expansion of the box dimensions when the pressure increases.



Resonant frequency
GHz

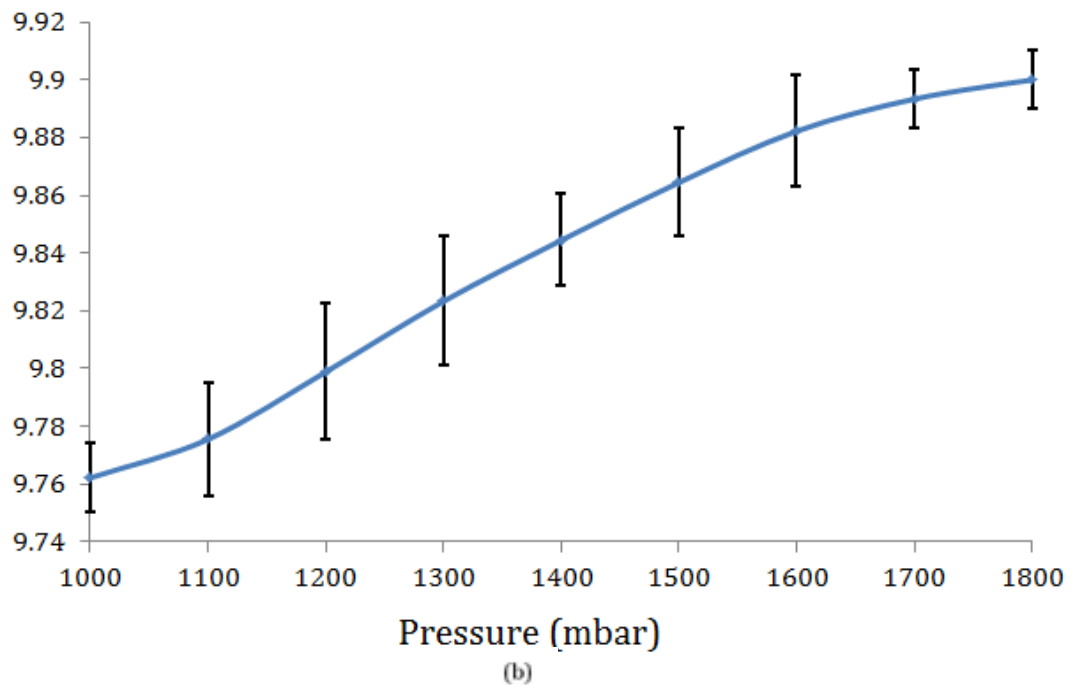


Fig.6.11. Wireless pressure measurement (a) and (b) device sensitivity.

The second experiment starts with the mounting of the devices on a Printed Circuit Board (PCB). The length and width of the substrate was 10 X 5 cm² and its thickness is 1 mm. In the middle of the substrate, an etched area with the same size as the sample was fabricated to allocate the sample. The depth of the etchant area was 310 microns. A hall of 300 X 300 μm² was also fabricated to allow the nitrogen gas to flow directly behind the membrane. Figure 6.12 shows a cross section and 3D sketch of the PCB.

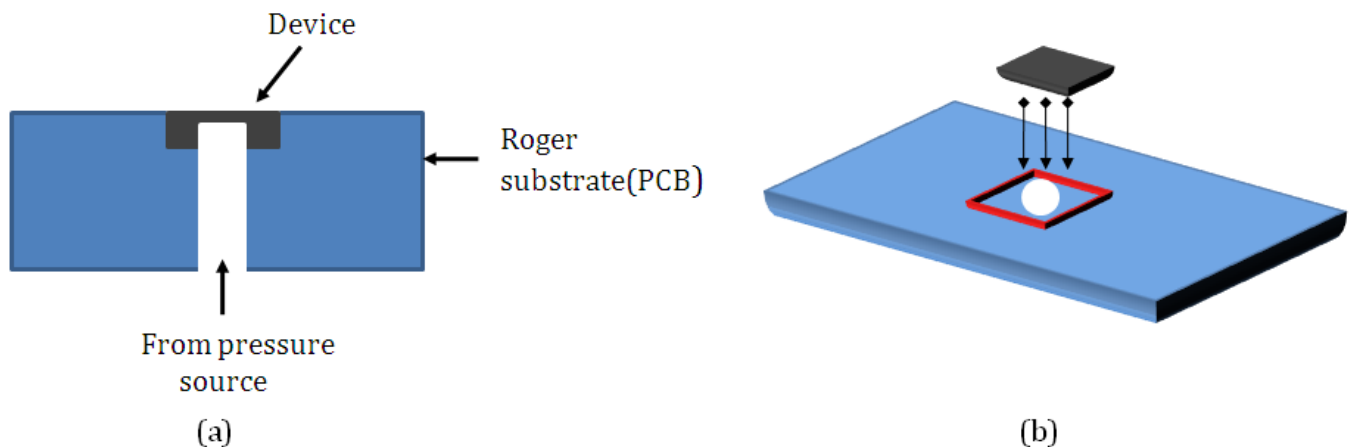


Fig.6.12. A cross section and 3D of PCB with an etched hole.

The distance between the horn antenna and the device was 10 cm. The differential pressure between atmospheric room pressure (1000 mbar) and the back-side of the membrane was accurately controlled by mounting the sensor over an aperture on a sealed copper adaptor. The sensor was surrounded by microwave absorbing foam. The pressure was controlled using a regulator connected to a nitrogen gas cylinder. The pressure in the adaptor was measured using a Barometric sensor (Campbell Scientific CS100). As can be seen from the sketch of the experimental configuration, the sensor membrane is deflected outwards from the chip in this set-up, it is expected that similar results would be obtained if a vacuum was applied behind the membrane and it was deflected inwards.

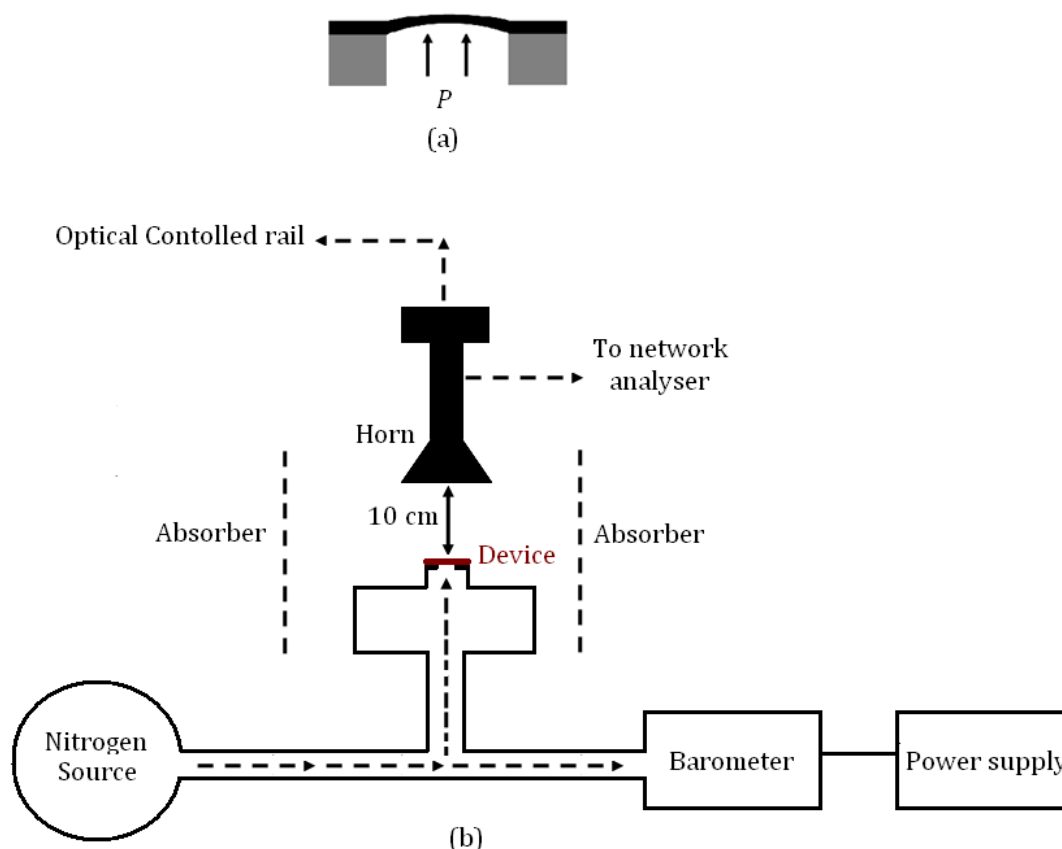


Fig.6.13. (a) The membrane has higher pressure behind the membrane and (b) a sketch of the experimental.

The sensor's calibrated wireless telemetry's repeatability was confirmed by performing three independent measurements of three devices of each design. For each experiment, the interrogation power radiated from the horn was -5 dBm at 23 °C. The results were measured for 120 sec per 50 mbar during which time no drift was observed. Figures 6.14 and 6.15 show devices sensitivities to pressure reflections from the horn antenna. The error bars shown in Figure 6.14 and Fig. 6.15 indicate device-to-device variation that can be attributed to tolerances in the photolithography and membrane etch. The measured shift in the resonant frequency of the meander antenna is between 10.28 GHz and 10.27 GHz in response to a pressure range between atmospheric pressure and 1.8 bar. This gives a device sensitivity of 12.5 kHz/mbar for the device containing the meander antenna. Data acquired from the zigzag antenna device shows a resonance shift from 9.6078 to 9.5809 GHz according to applied pressure, yielding a device sensitivity of 16 kHz/mbar.

Return Loss-dB

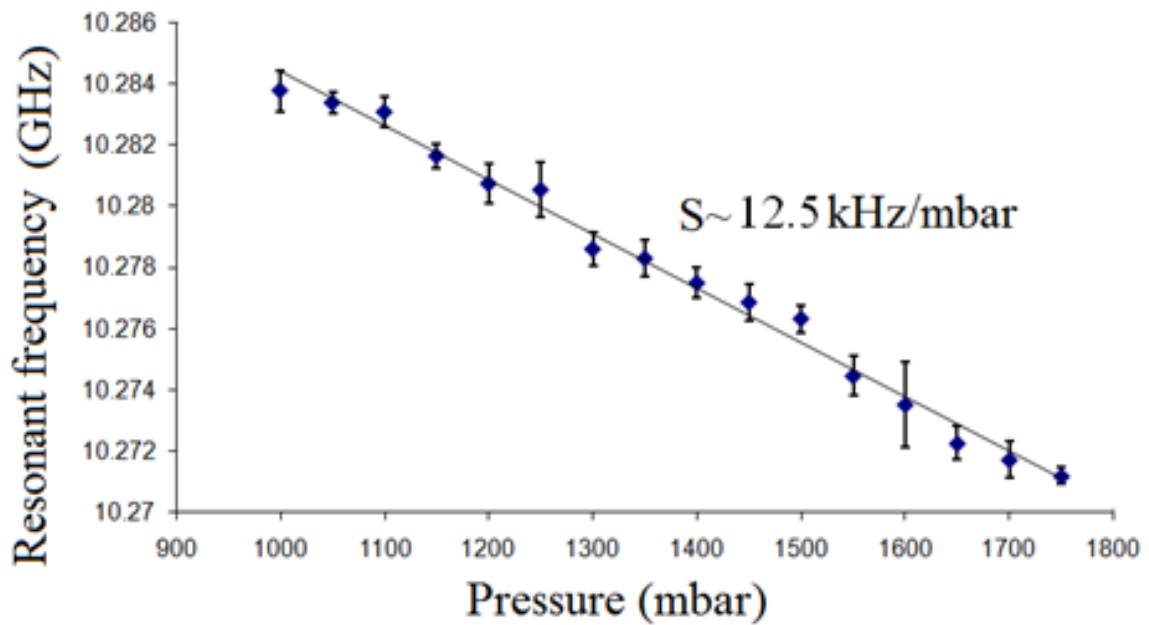
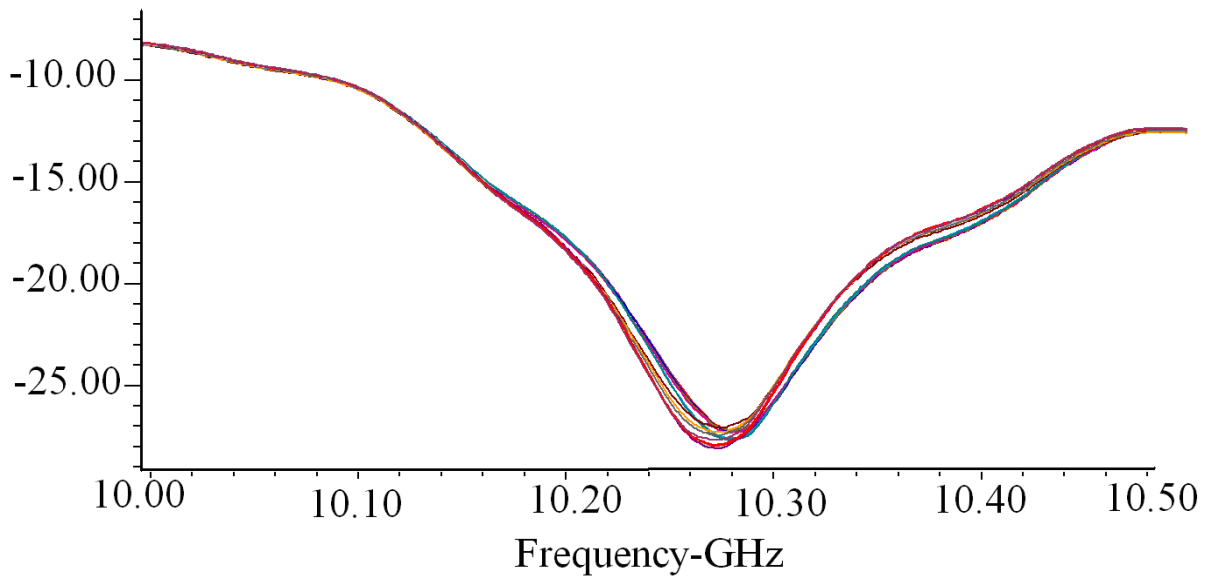


Fig.6.14. Resonant frequency shift detected at horn for meander antenna (top) and device sensitivity (bottom).

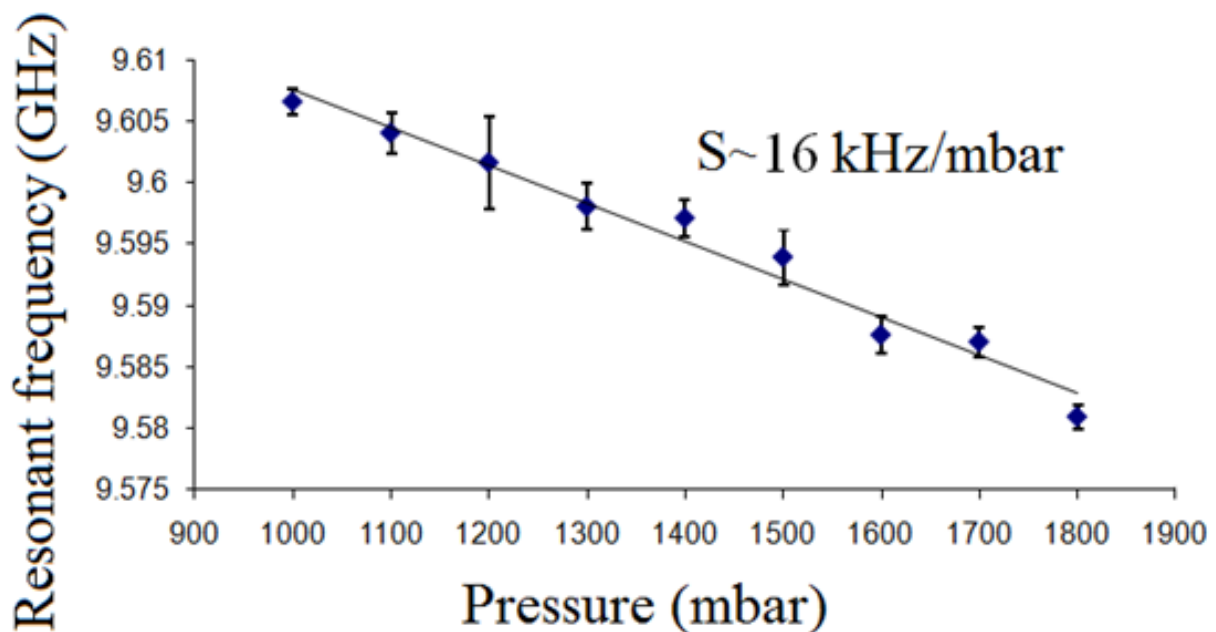
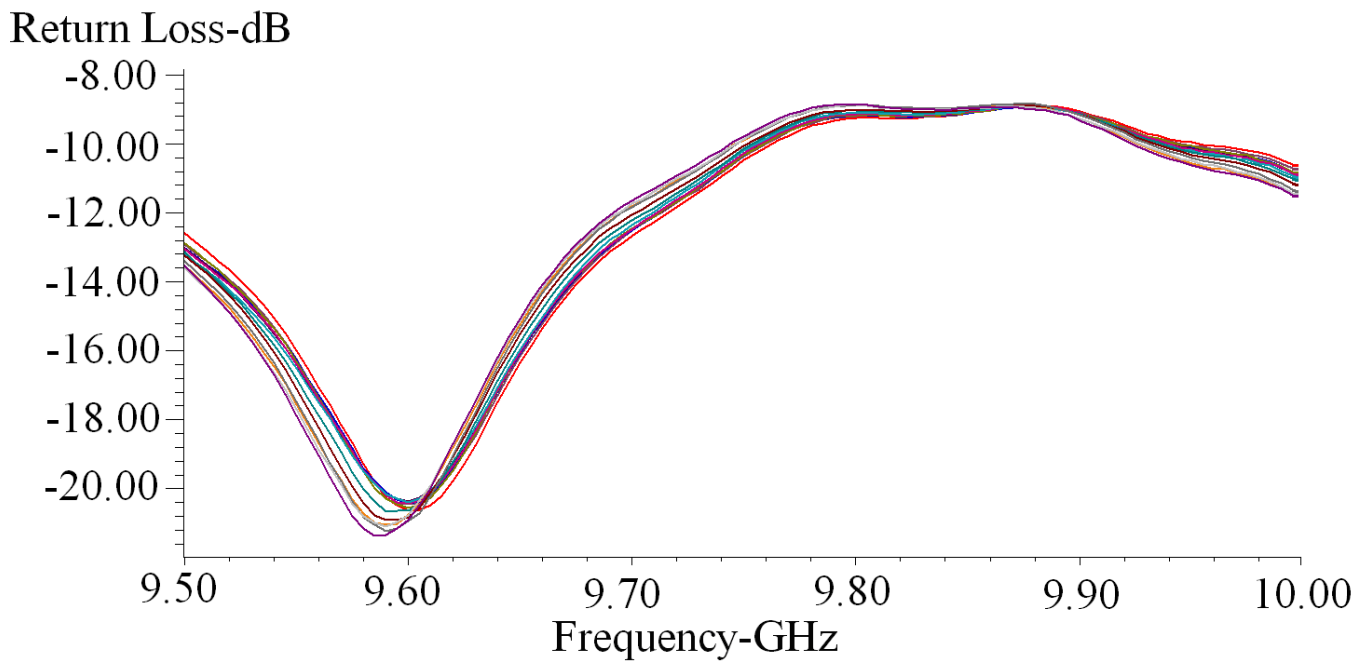


Fig.6.15. Resonant frequency shift detected at horn for zigzag antenna (top) and device sensitivity (bottom).

The performance of the devices is compared with some other passive pressure sensors shown previously in chapter 2. Table 6.2 summarizes the performances of some pressure sensors found in the literature and a comparison with the devices presented in this thesis.

Ref	Device material	Pressure range	Frequency range	Wireless distance
[73]	Silicon	0-100 mmHg	63-76 MHz	N/A
[74]	PCB	5-35 psi	23.5 - 21 MHz	1.5m
[75]	DuPont Pyralux	0-60 psi	25 kHz/psi	N/A
[76]	Silicon	370MHz/bar	27.5-35 GHz	60 μ m
[77]	Silicon on glass	N/A	670 to 230 MHz	100 mm
[78]	LTCC	N/A	47-55 GHz	N/A
[80]	Silicon on glass	400- 1000 mmHg	13-11.2 MHz	3 cm
This work	H.R. Silicon	1000-1800 mbar	10.28-10.27 GHz, 9.6078-9.5809 GHz	10 cm

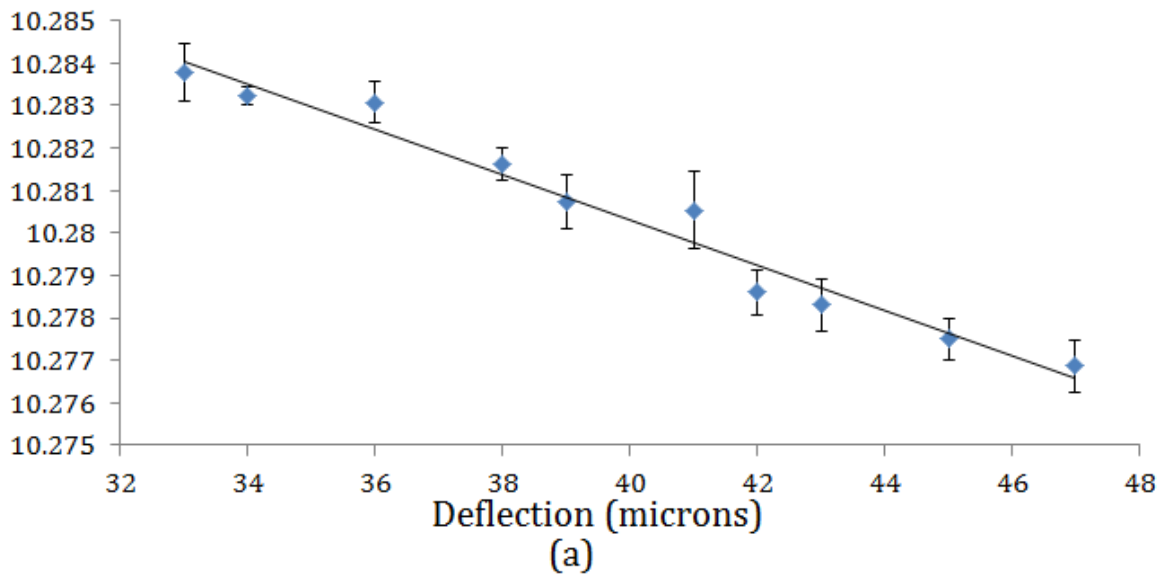
* 1000 mbar = 15 psi = 750 mmHg

Table 6.2. Comparison with some other devices in the literature.

6.1.1.4 Membrane deflection and resonant frequency

In chapter 4, the behaviour of the membrane under pressure was discussed (figure 4.11). For meander and zigzag antenna devices, the direct relation between the wireless resonant frequency and the deflection according to pressure applied to the membrane are shown in figures 6.16 (a) and 6.16 (b) respectively.

Resonant frequency (GHz)



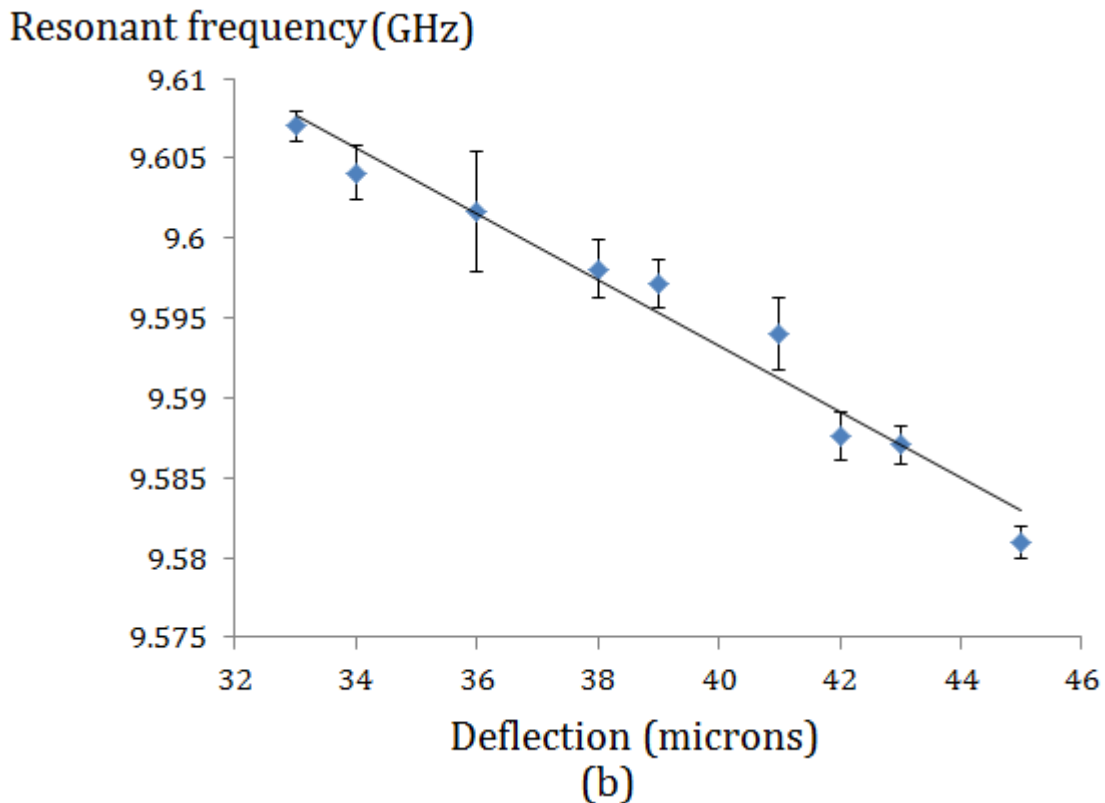


Fig.6.16. Wireless frequency and deflection of the membrane for (a) meander antenna and (b) zigzag antenna.

The results shown in the figures above agree with the measurements in figures 6.14 and 6.15. When increasing the pressure, the resonant frequency detected at the horn decrease, and increases the deflection of the membrane on the same time. Figure 6.16 show that when the deflection of the membrane is large, the resonant frequency detected at the horn decrease. Referring to figure 4.11, increasing the pressure above 0.1 Mpa (=1000 mbar) results in large deflection of the membrane (= 33 microns). After that, the deflection increases by small amounts when increasing the pressure, resulting in sensitivities of 0.5 MHz/microns for the meander antenna and 2 MHz/microns for zigzag antenna. The results shows higher sensitivity for zigzag antenna which agrees with results shown in figure 6.15.

6.2. Simulation and measurement results: On chip capacitor sensor

Figure 5.5 shows the design implementation in HFSS. As discussed previously, importing the capacitor array into HFSS had proven to be very difficult and caused the

software to crash many times. Additionally, if the structure is imported successfully, it will appear only in two dimensions.

To maximize the estimation of the performance of the device, a dummy structure was added and connected to the dipole antenna. Dummy layers for the density layers are also added to the design. All of the substrate parameters are loaded into the software.

The same setup demonstrated in figure 6.2 was used to test the device. Figure 6.17 shows the simulation and measurement results for the device.

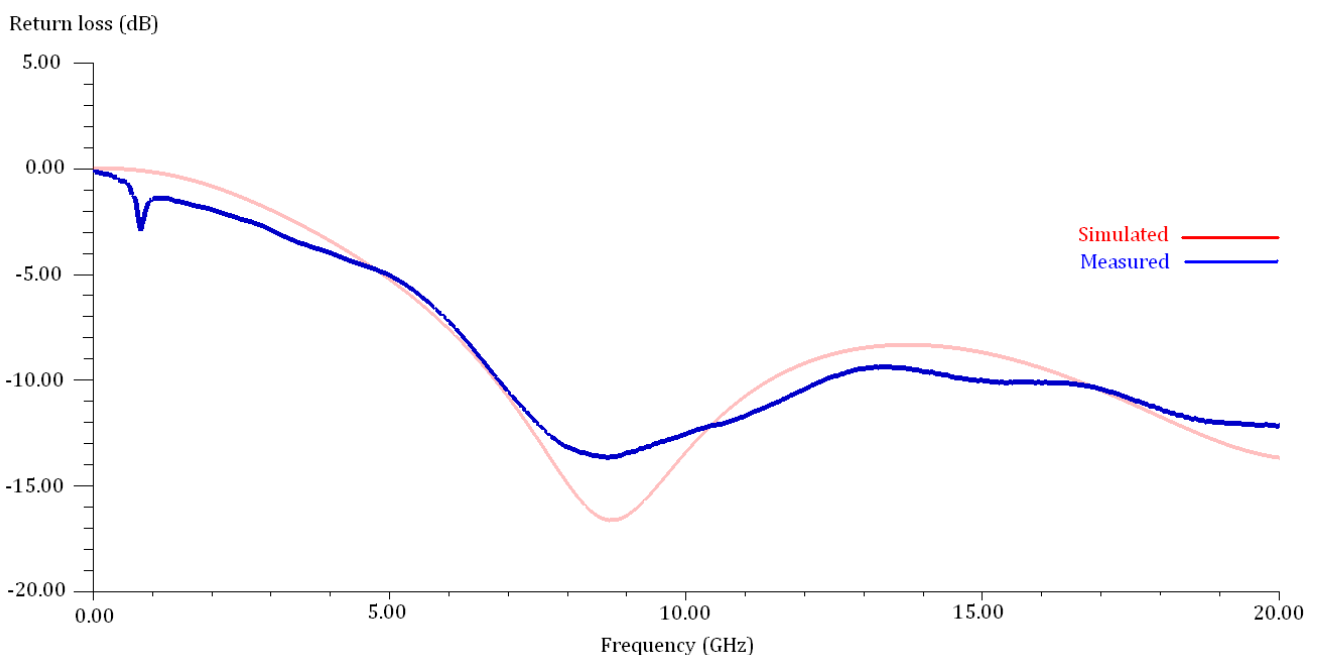


Fig.6.17. Simulated and measured results for dipole antenna-coupled with capacitor array on a CMOS chip.

As expected, both simulation and measurement show lower return loss compared with in-situ devices. We attribute this to the low resistivity of the silicon substrate and the epitaxial layer. The simulated resonant frequency as shown in the above figure is 8.8 GHz, and the measured resonant is 8.77 GHz. The return loss is -16.6 dB, greater by -3 dB for experimental data.

6.2.1. ΔP - ΔC for sensor array:

The de-coupled sensor array illustrated in figure 5.5 is directly tested by probing the on chip signal-ground pads with analyzer E8362B PNA. Figure 6.18 shows experimental

setup. The devices were mounted on a PCB/straight adapter, and put under the probes by a controlled arm. The gas flows through the adaptor directly towards the membrane.

The same pervious pressure calibrator was used to ensure there is no leak in the system. A capacitance change was observed between 1000 and 1800 mbar.

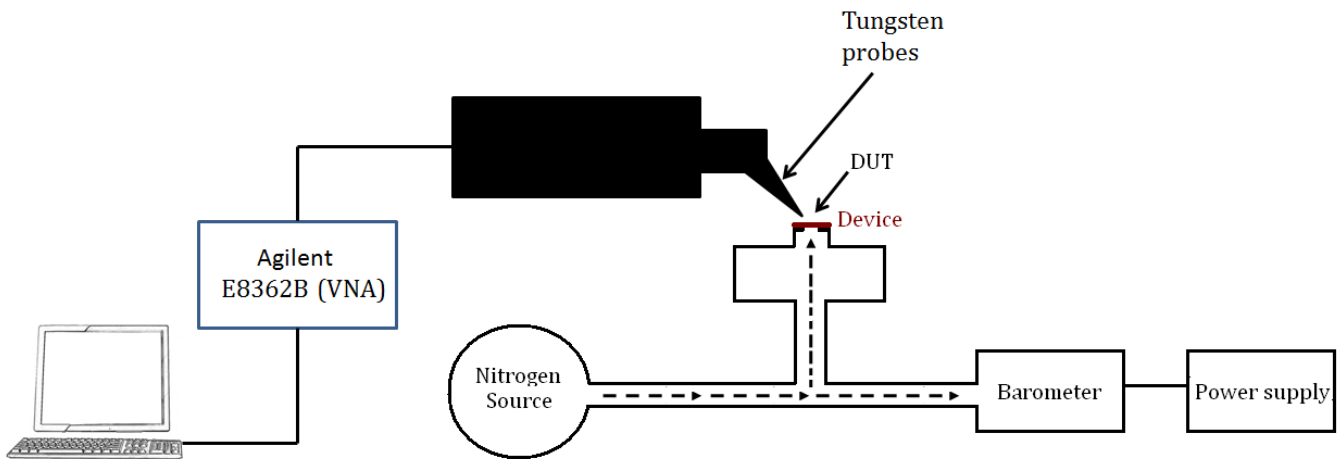


Fig.6.18. Sketch of test equipment for sensor array. Device under test (DUT) is probed using 50 Ω impedance tungsten wires.

The measured S_{11} data is converted to Y_{11} to extract the capacitance values. The etching of the silicon shifts the self-resonance of the array as shown in figure 6.19 from 2.25 to 1.63 GHz and reduces the value of the capacitor array. The self-resonance of the sensor at the above frequencies is due to the self-inductance of each capacitor in series (figure 5.8) in addition to inductance from interconnects.

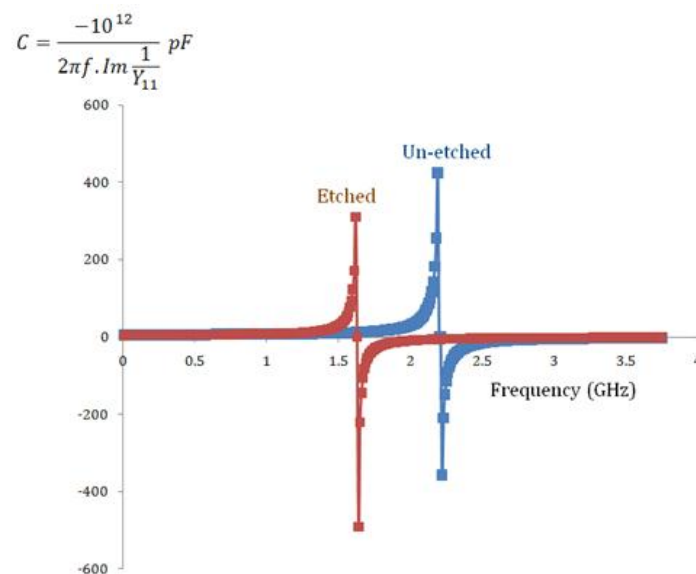


Fig.6.19. RF response of capacitor sensor. The resonance at 1.63 GHz (membrane) and 2.25 (before etching) by series inductance of on-chip metal interconnects.

The pressure-capacitance measurement is demonstrated in figure 6.20 (a). The value of the capacitance was taken at frequency 1.55 GHz. The direct relation between $\Delta P-\Delta C$ is shown in 6.20 (b).

$$C = \frac{-10^{12}}{2\pi f \cdot \text{Im} \frac{1}{Y_{11}}} \text{ pF}$$

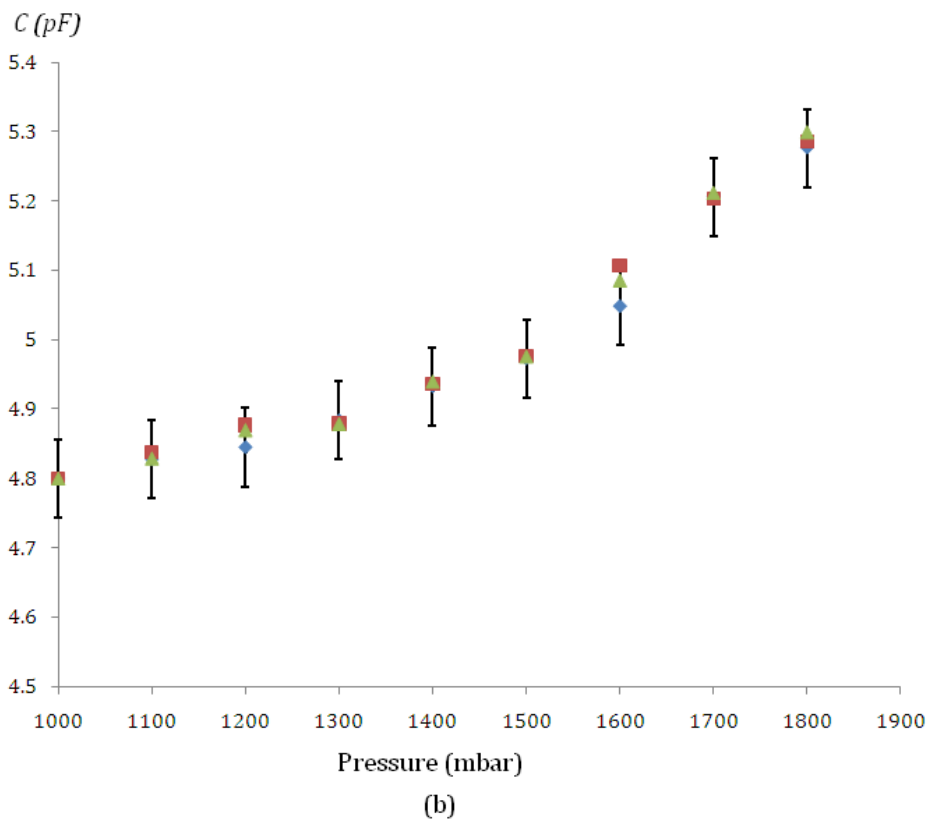
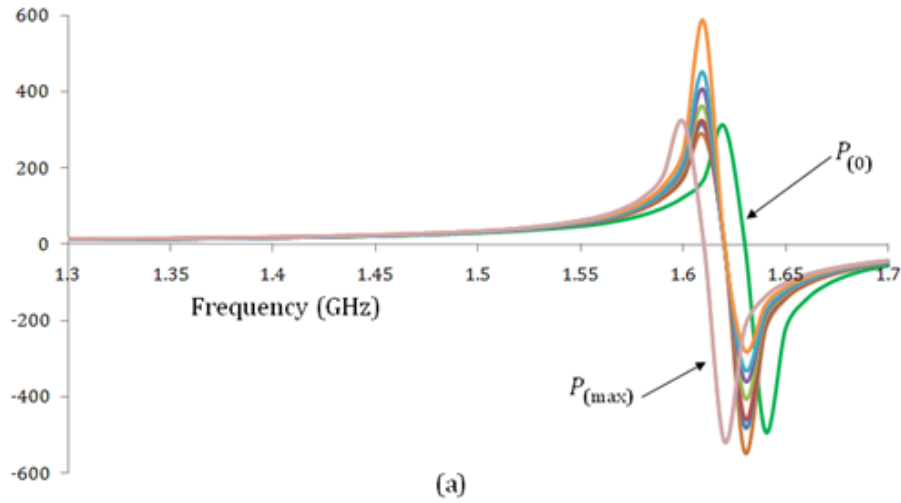


Fig.6.20. Extracted capacitance From S_{11} (a), and (b) $\Delta P-\Delta C$.

Increasing the pressure gradually increases the capacitance value. The sensitivity of the device is 0.47 fF/mbar. The values of the capacitor illustrated in figure 6.19 are taken at frequency of 1.55 GHz, before the self-resonant frequency of the system. The small amount of capacitance change is expected due to the presence of silicon nitride. However, a better sensitivity is expected if front side post processing is present. A good sampling, with active electronics as explained in chapter 2 will give more a robust reading of the sensor.

6.2.2. Wireless measurement

The same setup used for in situ devices experiment was used for measuring the wireless performance of the sensor. The VNA was calibrated to -5 dBm illumination power and a narrow band of frequency between 9.95 and 10.20 GHz to observe the slightest shift in resonant frequency. Three independent measurements are conducted to ensure the repeatability of the results. All experiments are carried out in the same physical environment (room temperature, humidity, and positioning of device and the horn antenna). Figure 6.21 shows one of the S_{11} results for the wireless pressure measurements.

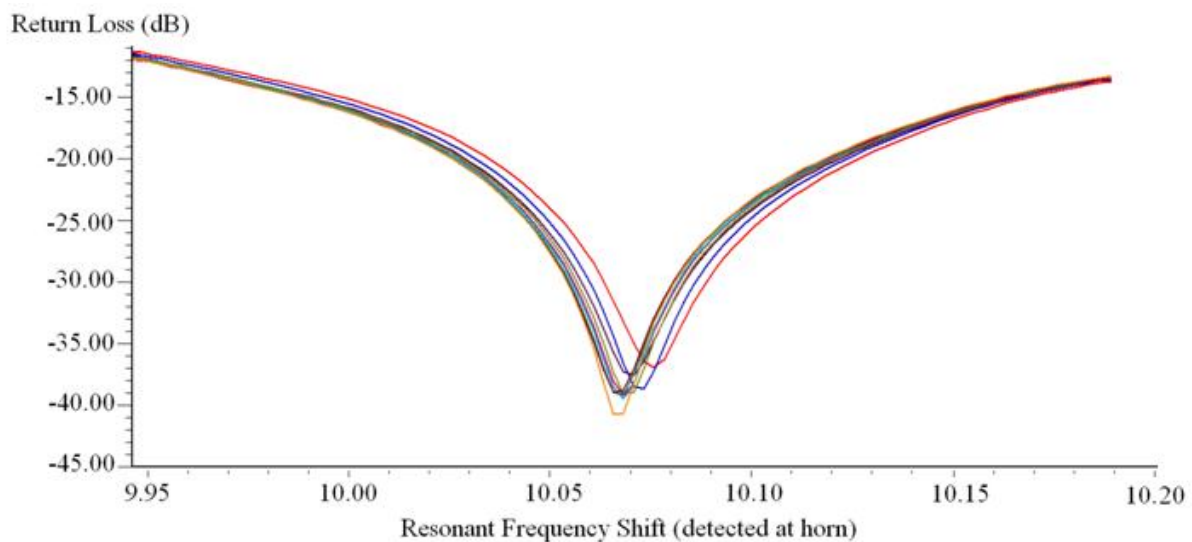


Fig.6.21. Resonant frequency shift detected at horn for Nat-Semi's chip.

The resonant frequency detected at the horn increases gradually when increasing the pressure. The resonant frequency shift is measured between 10.074 and 10.052 GHz for a pressure range between 1000-1800 mbar. This gives a sensitivity of 27 KHz/mbar for the device. The sensitivity of the device shows an increase by 6 KHz/mbar and 11.5

KHz/mbar for devices dependent only on the deflection of the membrane, i.e. tuning by the capacitor sensor offers a greater sensitivity. Figure 6.22 shows the sensitivity of the device.

Resonant frequency (GHz)

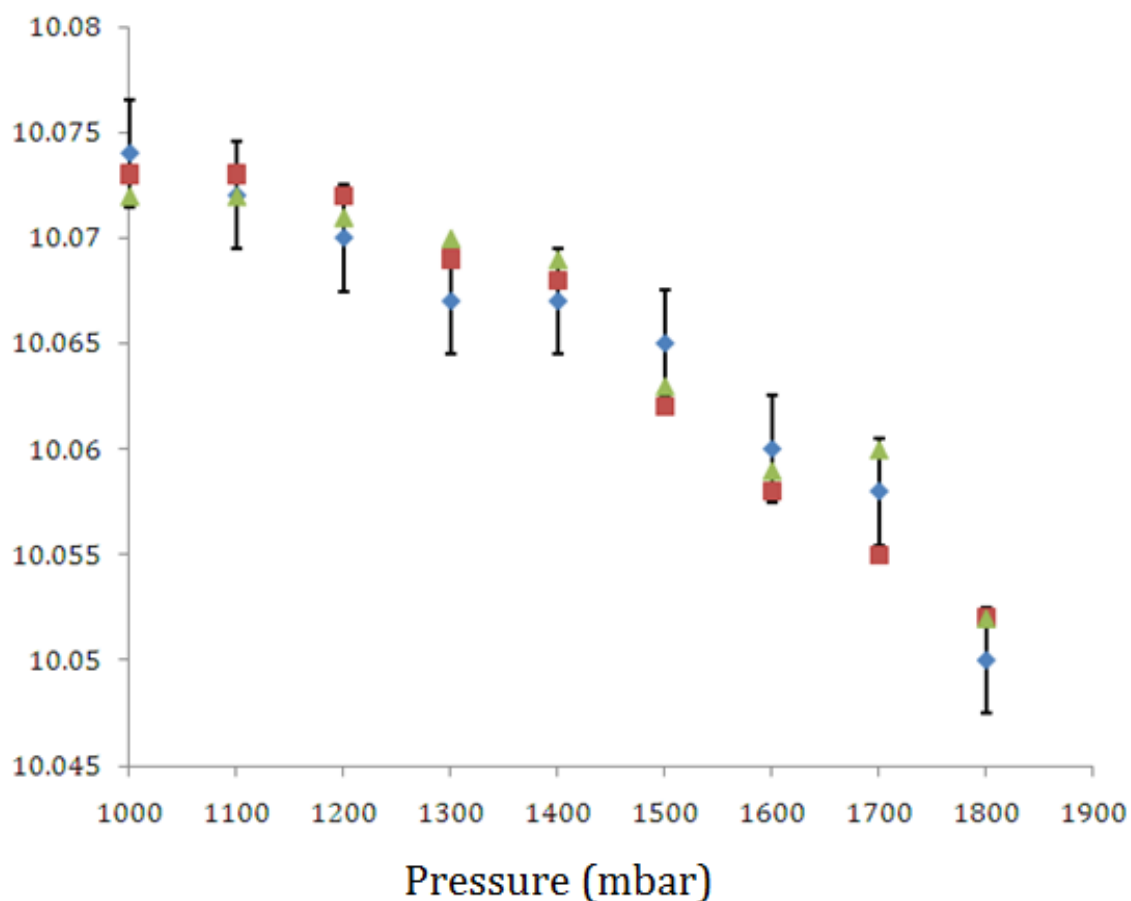


Fig 6.22. Pressure and resonant frequency measurements.

6.2.3. ΔC , ΔF and Membrane deflection:

In chapter 5, the behaviour of the composite membrane under pressure was discussed (figure 5.17). The relation between the deflection and the change in capacitance according to pressure applied to membrane is shown in figure 6.23.

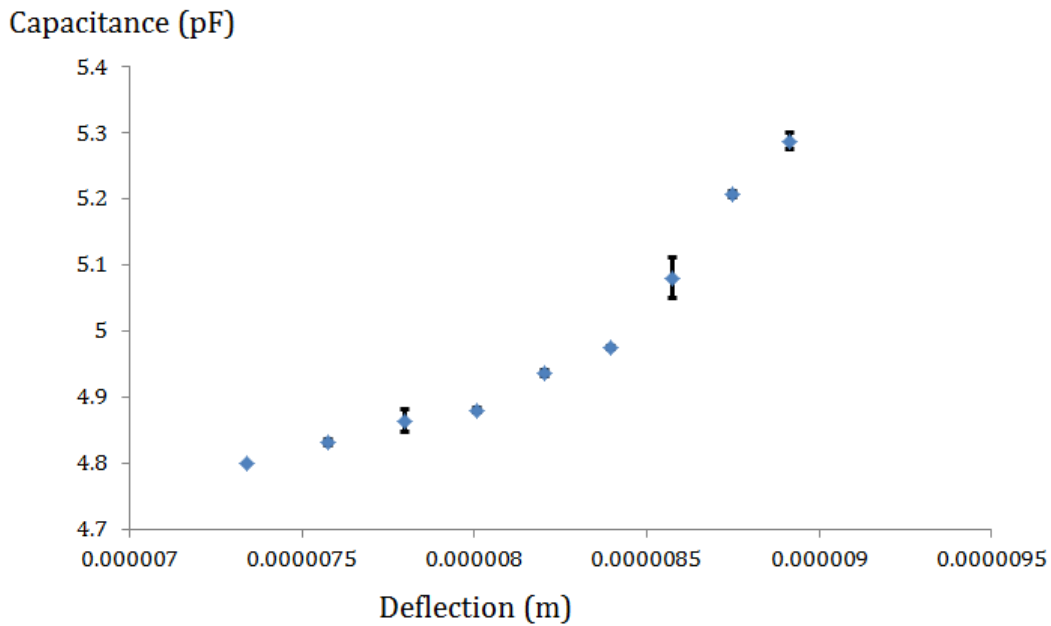


Fig 6.23. Deflection of composite membrane and sensor array capacitance.

The results shows perfect agreement with theory in chapter 5 (figure 5.17) and extracted results for capacitance (figure 6.20). As the pressure increases, the deflection of the membrane also increases. The capacitance of sensor array increases when increasing the pressure. Therefore, the capacitance increases with large membrane deflection. Similarly, the relation between deflection and resonant frequency is shown in figure 6.24. The relation also agrees with theory and measured results in figure 6.22. The resonant frequency decreases when increasing the pressure and therefore, the resonant frequency is expected to decrease when increasing the deflection.

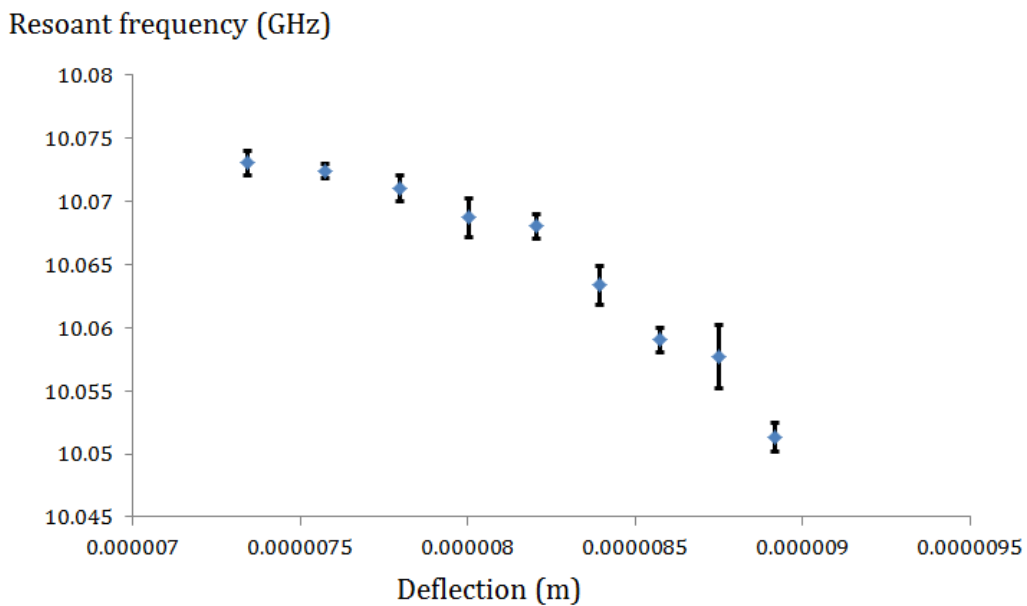


Fig 6.24. Deflection of composite membrane and resonant frequency.

6.2.4. Device limitation

The main drawback of the device is the low self-resonance frequency of the sensor array. The main objective of the sensor is to de-tune the resonant frequency of the antenna at X-band. However, the low self-resonance frequency of the capacitor makes the sensor to behave as an inductor at 10 GHz, due to large area and interconnect between capacitor cells. The frequency response detection of the device measured in figures 6.21 and 6.22 is attributed to membrane stress/strain under pressure, which is coupled to the on chip antenna. In the next chapter, a suggestion for better layout which lower the parasitic effects of the sensor will be presented.

6.3. Summary

The pressure sensor devices were tested. Special arrangements for the experimental setup are carried out to produce the maximum from devices. Prober measurements were used to directly test on chip transmitters. The results showed a working frequency at the band of interest (X-Band). Furthermore, the sensing element has shown a resonant frequency shift towards higher frequencies in the band, which agrees with the theory demonstrated in chapter 3. For devices made entirely in house, a wireless working distance of 10 cm was demonstrated. The deflection of the membrane when applying pressure was used to de-tune the resonant frequency of the on chip transmitter, and this shift was captured by a detecting antenna working in the same frequency band. This shift is between 10.28 GHz and 10.27 GHz for the meander line antenna and 9.6078 to 9.5809 GHz for the zigzag antenna. This gives a sensitivity of 12.kHz/mbar and 16 kHz/mbar for meander and zigzag antennas respectively, for a pressure range between 1000 and 1800 mbar. Also, the relation between the deflection of the membrane and resonant frequency of the antenna was highlighted.

We have also developed a CMOS chip based on similar principle. The chip has two resonant systems. One is a single dipole antenna designed to operate at approximately 10 GHz. A capacitive load is connected to the antenna feed. The capacitor uses the metal insulator metal structure of the CMOS process and is found experimentally to have a self-resonant frequency of approximately 1.63 GHz.

The CMOS device demonstrates sensitivity to pressure at the frequency of both its structures. When probed, the MIM capacitor detunes by 0.47fF/mbar. At 10 GHz the MIM capacitor is beyond its self-resonant frequency and is inductive. However, we observe wireless pressure sensitivity at the antenna resonant frequency of 27 kHz/mbar. Also change in capacitance and resonant frequency with membrane deflection is demonstrated.

In this chapter I have demonstrated two novel wireless readable, unpowered pressure sensitive devices. One device relies on a bespoke process where as the other, whilst where the same in operational principle, uses a foundry CMOS process. The CMOS device explored the use a MIM capacitors to detune a fixed dipole antenna.

Chapter 7

7. Conclusion and future work

This thesis concerned the design and fabrication of a single silicon chip wireless pressure sensor working at X-band frequencies. This has been realized, with much room for improvement. This chapter will review the major finding of this project, and present some suggestions for future work.

7.1. Conclusion

A wireless-passive microwave pressure sensor, with transmitter/receiver unit and a sensing transducer was designed, fabricated and tested.

7.1.1 In house devices

The first device, built entirely at Glasgow University's JWNC includes two types' antenna: meander antenna and zigzag dipole type antenna. These antennas with some parts on the sensing element (membrane) and other parts on solid silicon are excellent candidates for investigation due their inherent properties and operation. Furthermore, these antennas allows for more miniaturization, and offer the simplicity of design and low cost fabrication.

Etching the silicon substrate had shown greater effects on the performance of the antenna during the test phase of this project. One of the major changes is the positive shift in resonant frequency. The increase in resonant frequency agrees with theoretical studies of the dipole antenna. This result gives an advantage on designing chipset antennas, to be built entirely on thin and suspended membranes, allowing for very low dielectric constant (closer to one) and hence an increase in the operational frequency and reduction of antenna size. The measured increase for meander antenna is 0.7 GHz and 0.4 GHz for zigzag antenna.

The probed tests also showed the choice of substrate is crucial when designing on chip antenna. This is shown by S_{11} value, which demonstrates most of the power fed directly to the antenna is radiated.

Wireless pressure measurement results are demonstrated after overcoming some challenging obstacles. First the tests were carried out in room temperature, and second, the test setup should guarantee taking the maximum effect from the chip only. The set up used in this experiment ensures there is no leakage in the system. Also, instead of mounting the chip on a plastic box, the samples are mounted on a PCB and straight adapter. The plastic box setup has proven to collect readings both from the sensor and the expansion and contraction of the box. The working distance was 10 cm from a horn antenna working at the same band of frequency of interest. The resonant frequency shift for device containing the meander antenna is monitored between 10.28-10.27 GHz and between 9.61 and 9.58 GHz for zigzag device. The frequency shift range is 10 MHz and 30 MHz for meander and zigzag devices respectively for pressure range of 800 mbar above atmospheric pressure.

7.1.2 The Nat-Semi CMOS-MEMS chip

The experiments conducted to verify the behaviour of the novel capacitive pressure sensor showed sensitivity of 0.46fF/mbar. This change in capacitance was used to detune the resonant frequency of a dipole antenna operating at X-band. The chip area is 16 mm² and length antenna is 3.8 mm with metallic width of 100 μm.

The CMOS-MEMS post processing involve only two fabrication steps: Photolithography and deep etching. The capacitance was extracted from scattering parameters.

Wirelessly, the device showed a sensitivity of 27 kHz/mbar as a result of resonant frequency shift between 10.074 GHz and 10.052 GHz. The final result was taken after three independent experiments to ensure no external effect (temperature, humidity) on device. The operation distance of the sensor is 5 cm.

7.1.3 Mechanical Packaging

In order to a proper and repeatable free space measurement, it was necessary to develop a robust packaging process. This was done by creating an accurately-milled recess in a PCB, large enough to fit the chips. Behind the membrane, a hole was drilled to allow the flowing gas to be sensed by the membrane.

A brass straight adapter was fitted and glued behind the hole. This insures no gas leak in the system to insure a well calibrated experiment

7.2 Future work

7.2.1 Layout of the sensor

The layout of the capacitor sensor array in the CMOS-MEMS device plays an important role to minimize the parasitic effects of the device, so the sensor behaves as a capacitor at high frequencies.

First, dummy structures should be added for accurate lithography, so the structure won't be affected when tilting the wafer during manufacture.

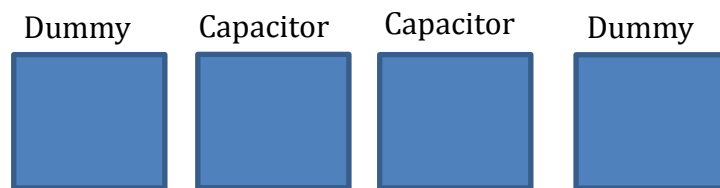


Fig 7.1. Addition of dummy devices to improve symmetry

Also, interconnects between capacitors should be well protected. One method is to add metal shield in each side of the wire. However, adding other metals in close proximity to capacitors will increase the parasitic effects. The solution is to cover the capacitors and interconnects with *P*-Substrate shield. This approach will insure most of the electric field lines emanating from the noisy lines to terminate on ground rather than the signal itself.

7.2.2 CMOS-MEMS Active device

The fabricated devices are suitable for close proximity scanning. For large distance operation, the sensor should be a part of an active circuitry as the block diagram illustrated in figure 7.2 below

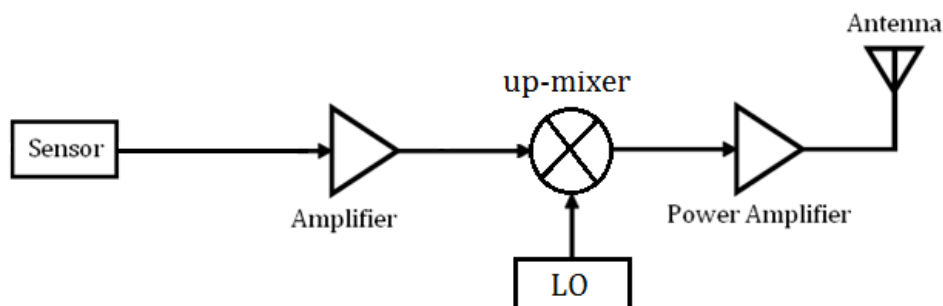


Fig.7.2. pressure sensor as a part of transmitter system.

The above figure shows a configuration of a simple RF transmitter for monolithic integration with CMOS/MEMS pressure sensor. It consists of an amplifier, up conversion mixer, local oscillator, and power amplifier. The on chip antenna is also realized on the same chip.

The differential configuration for the circuit block is usually preferred to minimize the noise figure and common mode. The Gilbert cell mixer is used to up convert the signal coming from amplifier by the mean of local oscillator (LO). There are different topologies for the oscillator which can be used in this circuit. For example, *RC* relaxation oscillator [115], or ring oscillator [116]. Differential cross coupled *LC* oscillator is another type of oscillator which is widely used in CMOS transceivers.

The topology showed in figure 7.2 is expected to perform under high power consumption. Another way to implement the sensor and the active electronics on the same chip is illustrated in the figure below.

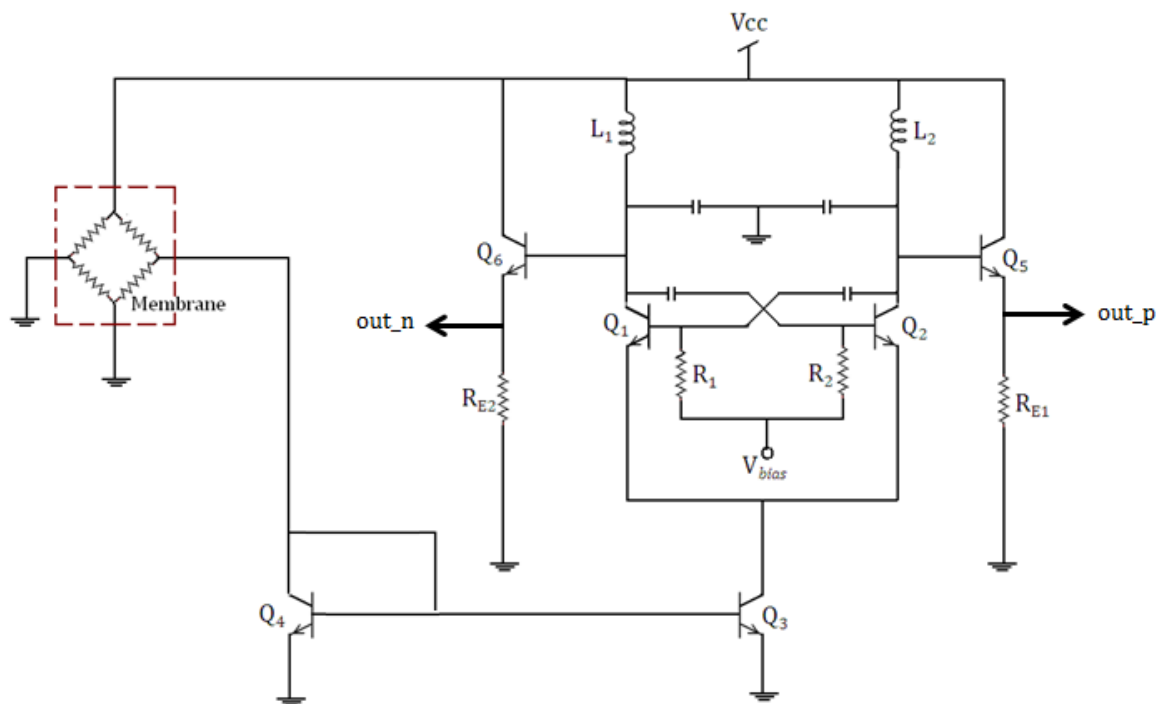


Fig.7.3. LC cross coupled oscillator with piezoresistive pressure sensor.

The figure shows a cross coupled oscillator. The frequency of the circuit is controlled by the value of the LC tank. As pressure is applied to the membrane, the voltage across Q_3 and Q_4 will change, resulting in current change across Q_1 and Q_2 . This will lead to a small change in oscillation frequency sensed at emitter followers Q_5 and Q_6 . The nodes out_p and out_n are directly coupled with an antenna. The main advantage of this circuit is the

low power consumption. As shown the circuit uses SiGe transistors for high frequency operation. However, aggressively scaled CMOS transistor could be used for this circuit (0.18, 0.13 and 0.9 gate lengths). The parasitic capacitance provided by large capacitor array as shown in this thesis would degrade the performance of the *LC* tank. A better choice for sensing element is a piezoresistive sensing element with its input voltage source coupled with V_{cc} supply and its output voltage coupled with a simple current mirror. By this means we can ensure maximum performance by the tank.

7.3. Final remarks

The single chip, unpowered pressure sensor designed and fabricated in this study is suitable for use in biomedical devices. The maximum working distance of the fabricated devices is 10 cm. Therefore, a scanning unit working in close proximity with the sensor is highly desirable. In future simple readers and smaller processing units could be built for use with devices in the V-band using cheap consumer electronic parts.

The new device used electromagnetically safe readout, and doesn't need a line of sight assembly and a pointing system (as opposed to using a laser) at a widely used frequency band.

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