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Case Study of Non-Isolated MMC DC-DC Converter in HVDC Grids

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SUMMARY

DC-DC converters are expected to play a significant role in future DC transmission grids and in providing connection points to HVDC lines. They will facilitate power exchange between two DC systems of different or similar voltage levels, and they may also provide other functions like DC fault isolation and power flow control.

CIGRE has recently established working group B4.76 which is focused on DC-DC converters and this submission provides initial B4.76 recommendation for non-isolated DC-DC converter topology.

This article presents the topology for non-isolated MMC-based DC-DC converter. The initial design study illustrates that such DC/DC converter will have overall semiconductor count comparable to a MMC AC-DC (used with HVDC transmission) converter of similar rating. A full controller schematic is presented and operating principles are discussed.

A 600MW, 320kV/250kV test system with parameters is presented in detail. A model for this converter is developed in PSCAD and a range of responses are presented. The simulation results confirm good responses for full power reversal, for severe DC faults on each DC bus, and for a step change on DC terminal voltage.

It is concluded that this converter is a good candidate for applications in future DC grids, and the test system is suitable for power flow, stability and protection studies of DC grids.

KEYWORDS

DC/DC converters, DC Transmission Grids, HVDC

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I. INTRODUCTION

DC-DC converters are expected to play a significant role in future DC transmission grids and in providing connection points to HVDC lines [1][2]. They will facilitate power exchange between two DC systems of different or similar voltage levels, and they may also provide other functions like DC fault isolation [3] [4].

CIGRE has indicated benefits of DC/DC converters in a number of brochures [1][2], and it has recently established working group B4.76 which is focused on DC-DC converters. This article provides an initial B4.76 recommendation for non-isolated DC-DC converter topology.

The non-isolated MMC DC/DC have emerged recently and there is only limited information on the converter design and control [5][6]. It is known that non-isolated MMC DC/DC potentially offers very cost effective method of interchanging power between two HVDC systems. However the initial studies have been limited to topology development and modelling principles, and much further work is required to demonstrate suitability for applications within HVDC systems.

This submission presents a topology of a MMC-based non-isolated DC/DC converter suitable for applications within DC transmission grids. The design trade-offs will be investigated considering performance requirements for HVDC applications. The controller for the converter will also be analysed.

II. NON-ISOLATED DC/DC TOPOLOGY

A. Basic Performance requirements

The essential requirements for transmission-level DC/DC are listed as:

1. Controllable bidirectional power transfer within rated power,
2. Tolerant to DC faults on either of the two DC terminals. This means that converter should have effective self-protection to DC faults without external devices (no DC Circuit Breakers).
3. Does not propagate DC fault current,
4. Minimise losses and costs.

B. Structure and operating principle

Figure 1 shows the converter topology. It includes 3 lower arms with all HB (half bridge) cells. The upper arms may have mix of HB and FB (full bridge) cells, where rating of FB cells should be at least equal to V_2 voltage in order to provide blocking fault current propagation for V_1 faults. If the system is symmetrical and balanced currents I_1 and I_2 will have only DC components.

III. CONVERTER DESIGN

The converter design equations can be found in [5][6]. Table 1 shows the rated variables for the test system considered, while Table 2 shows the key variables for the upper and lower MMC arms.

Unlike with MMC in HVDC systems, this converter has different currents in upper and lower arms. The DC currents are determined by the power transfer, while AC currents are required to balance energy between upper and lower arms.

The basic converter variables for power levels in the range *0-800MW* are shown in Figure 2. Of primary importance for this DC/DC is the peak current in lower and upper arms (I_{lp} and I_{hp}). For the considered *600MW* converter it is seen that peak current in upper arms is *2.05kA*, while lower arm peak current is *1.57kA*. As a comparison a *600MW 320kV* MMC AC-DC converter would have peak arm current of *1.85kA*, which implies that the proposed DC/DC would have similar overall semiconductor rating as a MMC AC/DC converter. It is also seen that L_2 inductor peak AC current is *0.85kA* and that it is not reducing with lower power levels.

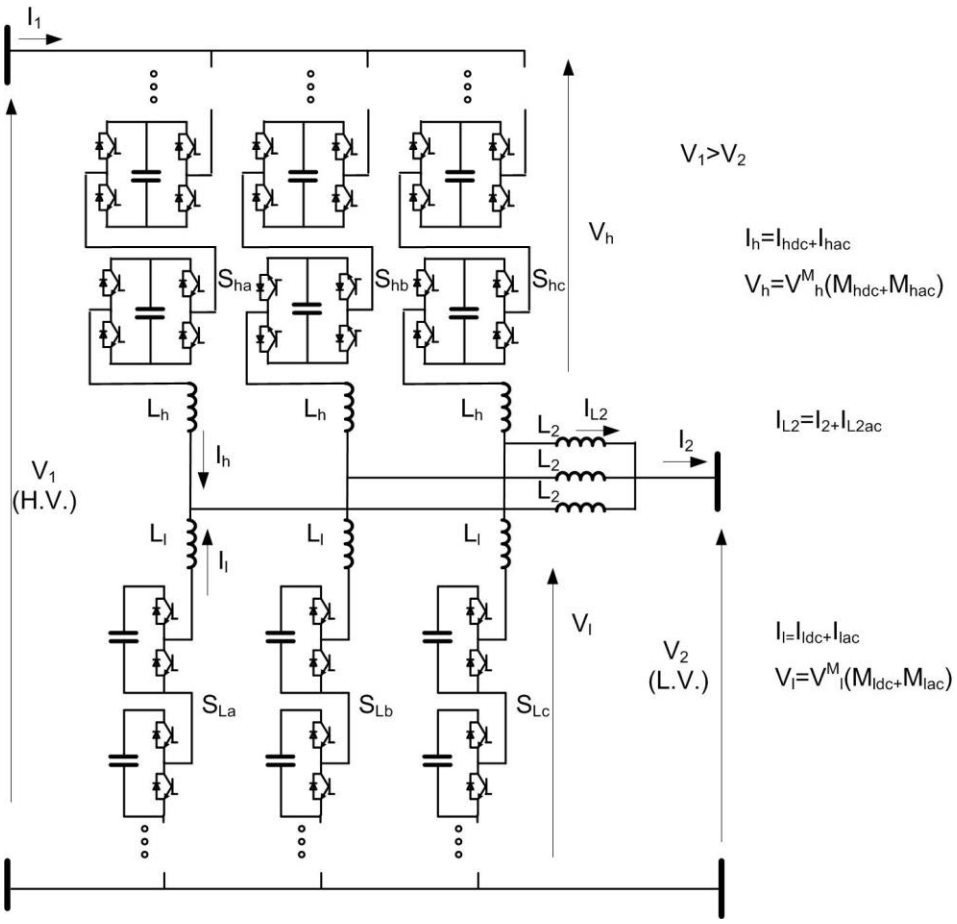

Figure 1. Topology of non-isolated DC/DC converter.

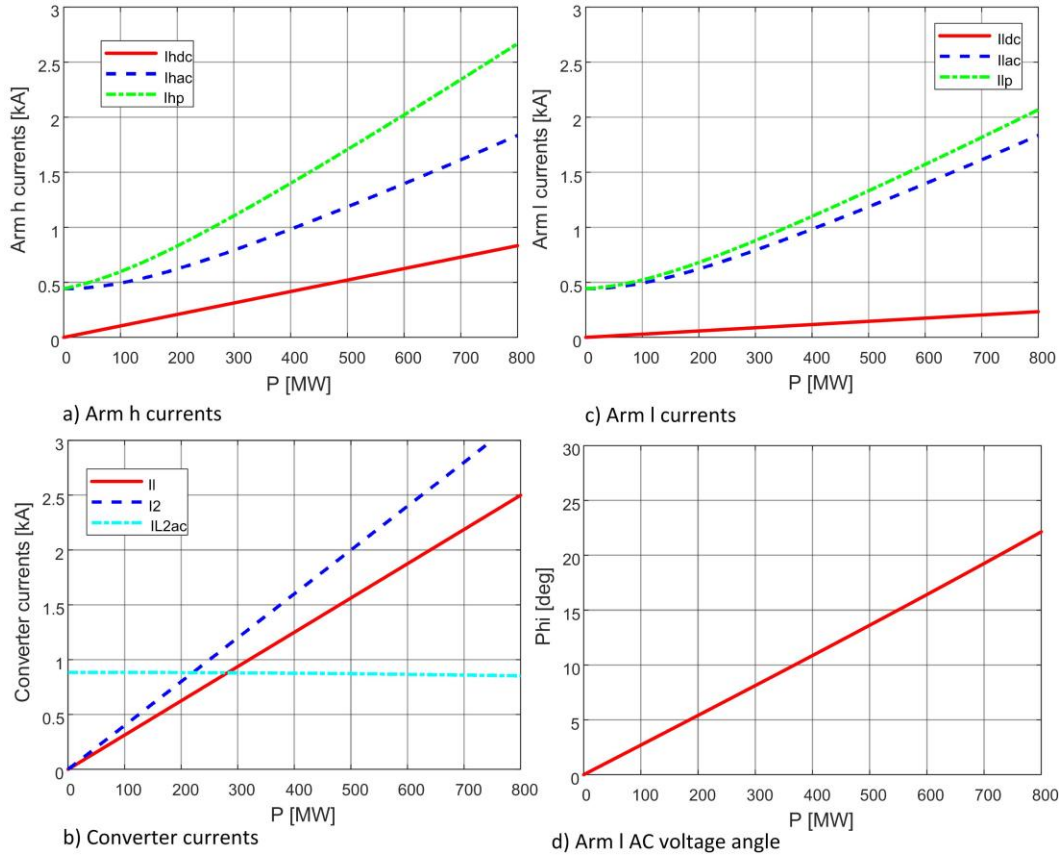

Figure 2. Design variables as power rating is changing (V_1=320kV, V_2=250kV, f=150Hz)

Table 1. DC/DC Tests system

Pdc	f	V_1	V_2	I_1	I_2	L_2
600MW	150Hz	320kV	250kV	1.875kA	2.4kA	0.08H

Table 2 Parameters of MMC arms

MMC	Cells	Rated voltage	Rated DC current	Rated AC current	Number of cells	Cell capacitance	Arm inductance
Arm h	FB, 2kV	V^M_h=320kV	I_{hdc}=0.625kA	I_{hac}=1.53kA	N_{cellh}=160	C_h=2.6mF	L_h=8mH
Arm l	HB, 2kV	V^M_l=320kV	I_{ldc}=0.175kA	I_{lac}=1.53kA	N_{celll}=160	C_l=18mF	L_l=8mH

The peak arm currents can be reduced by using larger L_2 and further cost optimisation would be required. As an example, if significantly larger L_2=*0.35H* is used, then upper arm and lower arm peak currents would be *1.91kA* and *1.46kA* respectively, while L_2 peak current would reduce to *0.21kA*.

The operating frequency of *150Hz* is selected as the initial trade-off between converter size and losses. Higher operating frequency would result in lower values for all passive components and cell capacitors. It would also reduce the AC current in arms leading to lower peak current in semiconductors. However increasing operating frequency would increase converter losses and the final design will be determined using optimisation methods considering the application and priorities.

IV. CONVERTER CONTROLLER

The essential controller requirements for this DC/DC converter are:

1. System stability for all disturbances and inputs,
2. Power reference tracking within rated power,
3. Inner current loops for each arm,
4. Minimise losses,
5. Self protection for DC faults,

The proposed converter controller structure is shown in Figure 3. The maximal voltage (also called capacitor sum voltage) of the upper arms V^M_h is regulated using the DC modulation index of the upper arms. The inner arm DC current feedback loop is also used in order to improve response and to limit current in case of disturbances. Similarly, the maximal voltage of the lower arms V^M_l is regulated using the DC modulation index of the lower arms.

The power flow P_{dc} is controlled using the phase shift between the AC voltages of upper and lower arms θ_L. The AC modulation index is maintained at maximal possible value (so that $0<m_{dc}+m_{ac}<1$) in order to maximise AC voltage which leads to minimal arm currents and therefore minimal losses.

The arm MMC blocking (*DebH, DebL*) is initiated if DC voltage drops below *80%*.

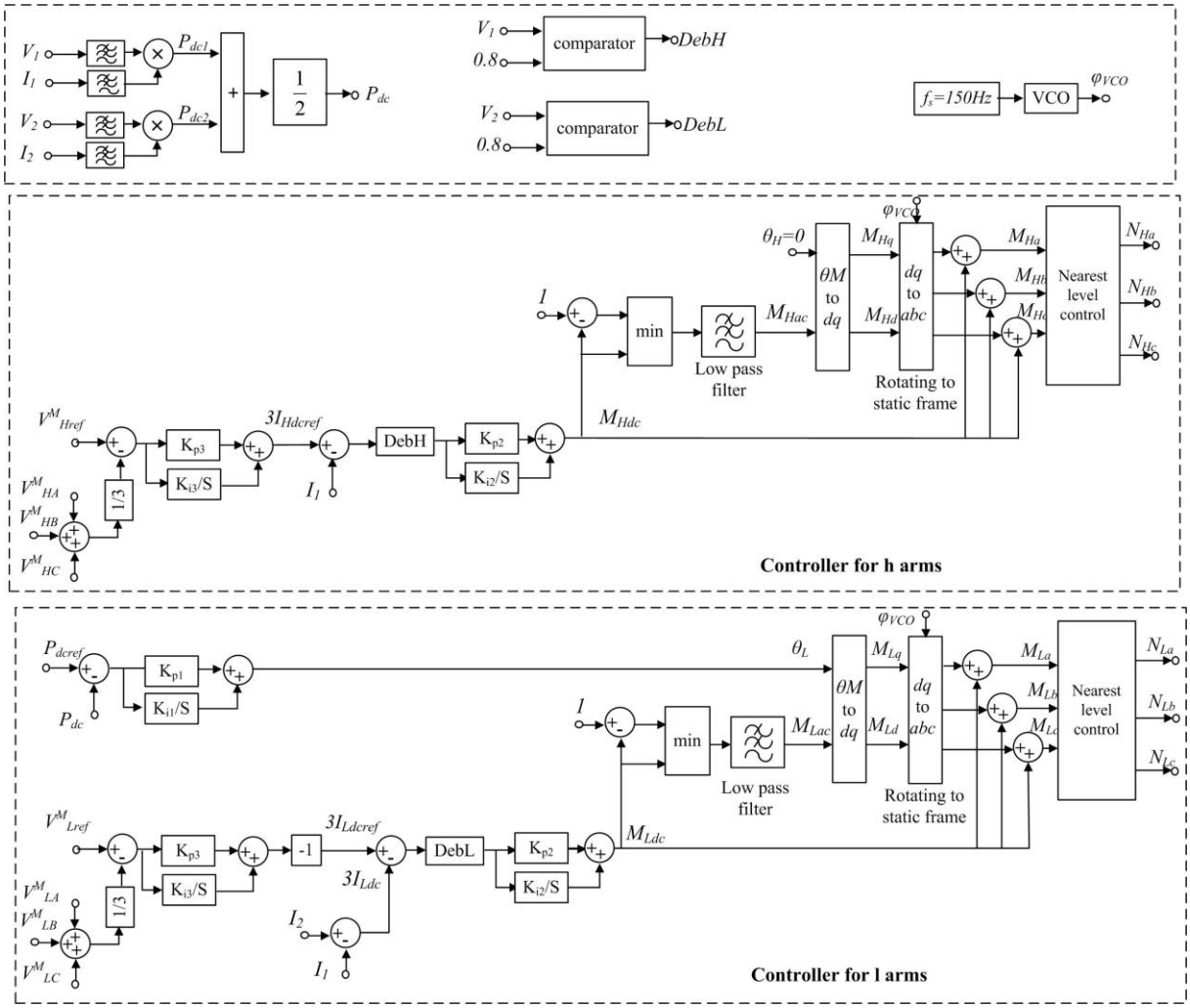

Figure 3. Controller for Non-Isolated MMC DC-DC.

V. SIMULATION RESPONSES

A full model for the DC/DC converter is developed in PSCAD using the average MMC modelling methods [4]. Figure 4 shows the simulated responses for a range of inputs:

1) At 0.5s Full power reversal (*600MW -> -600MW*),

2) At 0.7s V_1 terminal DC fault,

3) At 0.9s, V_2 terminal DC fault,

4) At 1.1s, 10% voltage drop on V_2.

It is seen that the responses meet performance requirements. In particular the control of all 5 variables (2 inner currents, 2 arm voltages and power) is excellent. In case of DC faults the converter is blocked and the fault is not propagated to the opposite DC side. The modulation indices are close to the maximal limits which implies good converter efficiency. The maximal arm voltages are within ±5% in steady-state and within ±*20%* during disturbances.

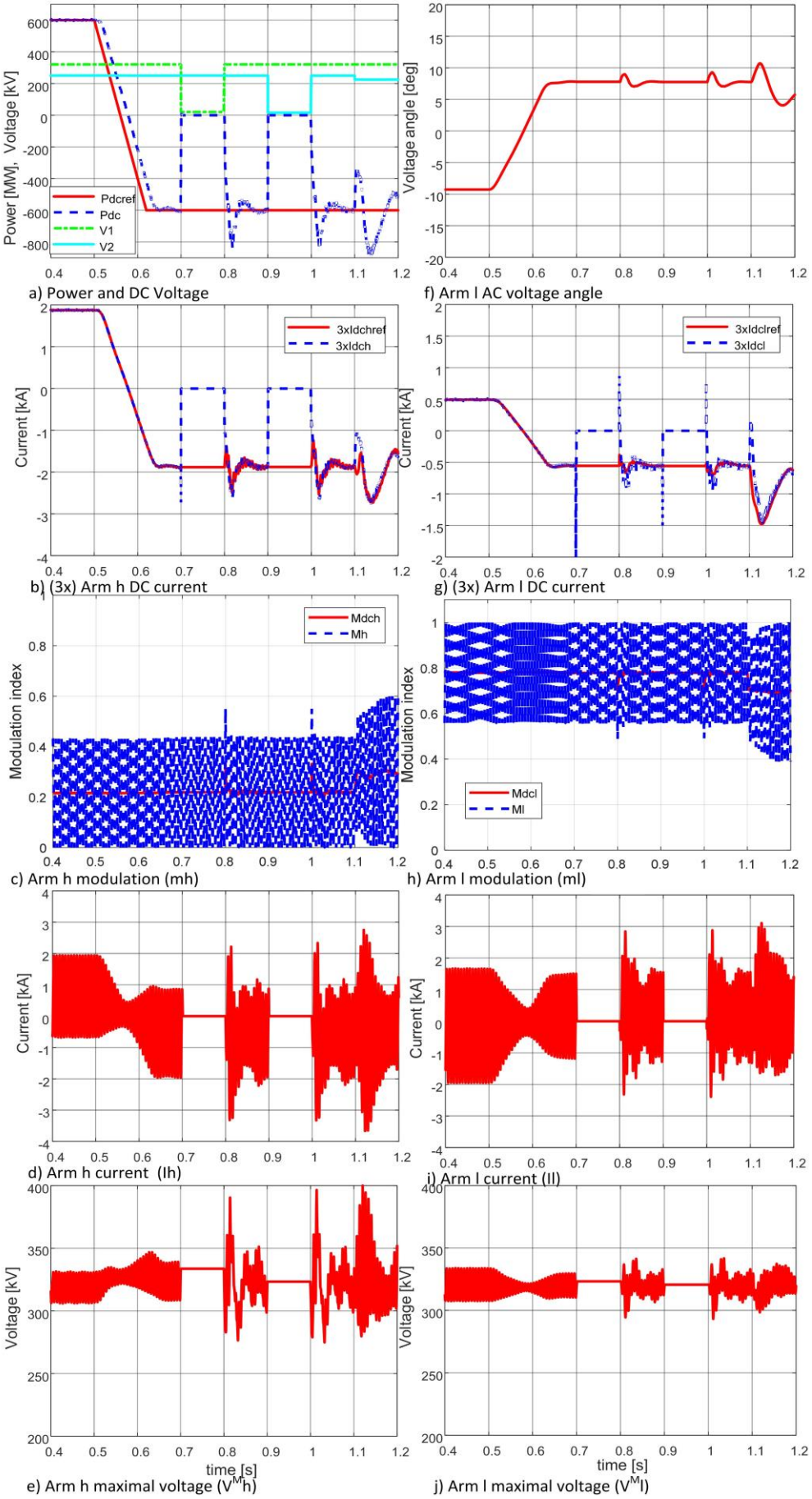

Figure 4. Converter response for power reversal, DC faults and V2 step reduction.

VI. CONCLUSIONS

The case study of *600MW* 320kV/250kV non-isolated MMC DC/DC indicates that the overall semiconductor count will be similar to a 600MW MMC HVDC converter. The use of larger common inductor on LV side may only marginally reduce current rating of the semiconductors.

The analysis of DC/DC converter controller concludes that it is essential to control the following variables: power, 2 maximal arm voltages and 2 arm currents.

The simulation studies have been performed for power reversal, DC faults and DC voltage step change, and the conclusion is that the performance meets the requirements.

It is proposed that this model will be suitable for DC grid power flow, stability and protection studies.

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