Low-Frequency Noise Assessment of Work Function Engineering Cap Layers in High-k Gate Stacks

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Engineering the effective work function of scaled-down devices is commonly achieved by the implementation of capping layers in the gate stack. Typical cap layers are Al_2O_3 for pMOSFETs and La-oxide or Mg for nMOSFETs. Besides introducing a dipole layer at the SiO_2/high-κ interface, the in-diffusion of the metal ions may lead to either passivation or generation of traps in the SiO_2/high-κ layer. This paper uses low frequency noise studies to determine the impact of capping layers on the quality of the SiO_2/HfO_2 gate stacks. The influence on the trap profiles of different types of cap layers, different locations of the cap layer (below or on top of the HfO_2 dielectric) and the impact of different thermal budgets, typically used for the fabrication of Dynamic Random Access Memory (DRAM) logic devices, are investigated. The differences between several metal oxides are outlined and discussed.
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Starting from the 45 nm technology node, the implementation of High-κ/Metal Gate (HK/MG) stacks is common practice for high-performance CMOS devices and circuits.[1] Defects present in the high-κ dielectric (e.g. positively charged oxygen vacancies) will strongly influence the value of the threshold voltage (V_T) of the devices. In order to simplify the process flow, one can choose to implement a single mid-gap work function metal gate like TiN. However, this results in non-optimal V_T values for either n- or pMOSFETs or both. Engineering of the threshold voltage can be achieved by the implementation of different types of thin capping layers, such as e.g. an Al_2O_3 or AlN cap for p-channel devices[2–4] and a LaO_x or MgO_x cap for n-channel transistors.[5–7] The control of the effective work function is related to the formation of dipoles at the interface between the high-κ dielectric and the interfacial SiO_2 layer underneath.[8–10] A schematic illustration of the location of a dipole layer is shown in Fig. 1. The offset of the bands can influence the density of traps in the dielectric determined from low frequency noise measurements. An atomistic model for the band offset was developed based on ab initio calculations and taking into account the coordination of the interfacial oxygen which depends on technological parameters (e.g. deposition technique, surface passivation) and the used thermal budgets.[10] The diffusion of metal ions (Al, La, Mg…) from the cap layer will, depending on their electronegativity (dipole charge transfer) and ionic radius (dipole separation), alter the dipoles resulting in a shift of the band offset.[11]

It has been reported that in the case of a LaO_x cap to engineer n-channel devices, a medium to high temperature anneal can reduce the trap density in the HfO_2 layer[12] due to the defect passivation by the La.[13] On the other hand, for p-channel devices, the use of an Al_2O_3 cap on a HfO_2 dielectric leads to an increase in the trap density.[14] It is therefore important to investigate more in detail the impact of capping layers on the quality and reliability of the gate stack.

A very powerful diagnostic tool to investigate the quality of the gate stack is low frequency noise analysis. The observed $1/f^\gamma$ or flicker noise ($\gamma \sim 1$) typically found for large area transistors can be either due to carrier trapping in oxide traps (so-called Δn origin)[15,16] or caused by mobility (μ) fluctuations (so-called Δμ model).[17] For small-area transistors, the current fluctuations in the time domain result in so-called Random Telegraph Noise (RTN).[18–20] Both RTN and 1/f noise are commonly used techniques to characterize traps in the gate dielectric. In the first case the energy level, the capture cross section and the trap position with respect to the interface can be revealed for individual oxide defects.[19,20] As will be explained below, flicker noise enables to extract the trap density and depth profile in the oxide under certain assumptions, while determination of the energy distribution and capture cross section is less obvious. The methodology used to extract the oxide trap density profile from the 1/f noise performance is discussed in the next section.

The present work reviews the low-frequency noise of High-κ/Metal Gate (HKMG) Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) with emphasis on the impact of the capping layers used for V_T tuning. Attention will be given to both Al_2O_3 cap layer engineering in pMOSFETs, and LaO_x or Mg-based cap layers in n-channel transistors. The influence of different technological parameters will be addressed, with the exception of the choice of the metal gate (TiN, TaN, AlSi….) itself as the impact of this parameter on the 1/f noise performance has recently been reviewed by the authors.[21–23]

Methodology to Determine Trap Parameters from Noise Studies

LF noise measurements have been performed on HfO_2-based gate stacks, with different types of metal-oxide-based cap layers, using $W = 1\ \mu m \times L = 1\ \mu m$ (Al_2O_3 pMOSFETs) or $W = 1\ \mu m \times L = 0.170\ \mu m$ area devices (p- and nMOSFETs) in linear operation (drain-to-source voltage $V_{DS} = -0.05$ V) with the gate voltage V_{GS} stepped from weak to strong inversion. Rather large-area transistors have been selected in order to emphasize the 1/f noise behavior and to reduce the noise variability, induced by the presence of RTN. For each device type, about ten devices per wafer have been measured in order to address the noise variability. The drain current noise Power

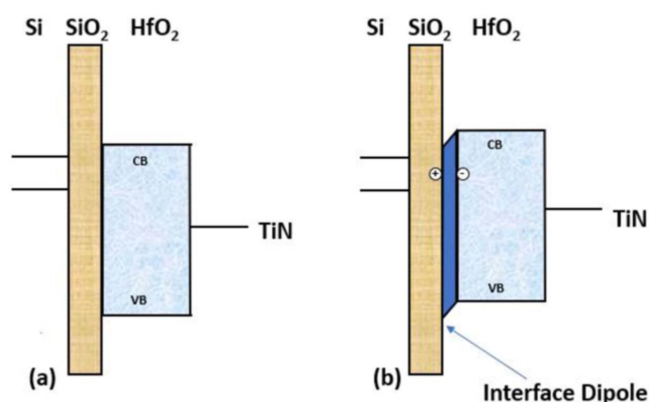

Figure 1. Energy band diagrams of a Si nMOSFET without (a) and with (b) a dipole at the SiO_2/HfO_2 interface.

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Spectral Density (PSD) (S_I) and its normalized value (S_I/I_D^2) have been studied at a fixed frequency f = 10 Hz versus the drain current I_D. The input-referred voltage noise PSD (S_{VG}) is derived from S_I by dividing with g_m^2, with g_m the measured transconductance.

Trap density.—In the case that the noise is dominated by carrier number fluctuations (CNF or Δn), i.e., capturing/emission of carriers by/from traps in the dielectric, the trap density N_{ot} can be calculated from the 1/f noise PSD using:[15,16,24]

$$N_{ot} = \frac{\text{WLC}_{EOT}^2 \alpha_t f S_{VGfb}}{q^2 k_B T} \quad [1]$$

with q the elementary charge, k_B Boltzmann's constant and T the absolute temperature. W and L are the device width and length, respectively, C_{EOT} is the capacitance density (F/cm^2) corresponding with the Equivalent Oxide Thickness (EOT), f is the frequency, S_{VGfb} is the input-referred voltage noise at flatband voltage and α_t is the attenuation factor of the electron wave function in the gate oxide. The latter is for an nMOSFET given by[15,16]

$$\alpha_t = \frac{2}{\hbar}\sqrt{2qm_{ox}\Phi_{it}} \quad [2]$$

with $\hbar$ the reduced constant of Planck, m_{ox} the tunneling effective mass and Φ_{it} the barrier height or conduction band offset. Symmetrical relationships hold for holes in a pMOSFET. It can be seen from Eq. 2 that the α_t value for SiO_2 is different than for a high-κ dielectric. For most of the high-κ devices, CNF is dominating over mobility fluctuations.[19,25-28]

Trap density profile.—If pure elastic tunneling is assumed then the frequency f can be translated into a trap depth z in the oxide according to

$$z = \alpha_t^{-1}\ln[1/(2\pi f \tau_0)] \quad [3]$$

with τ_0 the Shockley-Read-Hall recombination lifetime at the Si/SiO_2 interface, given by

$$\tau_0 = \frac{1}{n\sigma_n v_{thn}} \quad [4]$$

with n the (volume) free carrier density in the inversion layer, v_{thn} the thermal velocity and σ_n the capture cross section for electrons. Usually, a value of 10^{-10} s is assumed. A 1/f noise spectrum can then be converted in an oxide trap density profile as follows: Eq. 1 transforms the noise PSD into an N_{ot} (cm^{-3} eV^{-1}), while Eq. 3 converts the frequency axis into a trap depth with respect to the Si/SiO_2 interface. This approach is illustrated in Fig. 2. The lower the frequency the deeper the trap into the oxide. It should be remarked that for the same measurement frequency the trap depth is larger in n-channel devices than for p-channel devices due to the different tunneling barrier for electrons and holes, respectively.

In case that the capture time τ_c is thermally activated Eq. 4 becomes

$$\tau_c = \tau_0 \exp\left(\frac{E_B}{k_B T}\right)\exp(\alpha_t z) \quad [5]$$

with E_B the energy barrier for capture by an oxide trap. Unless $E_B/k_BT << 1$ one is dealing with inelastic tunneling and the energy level of the trap E_T has to be taken into account for calculating the depth, resulting in the following expression[29]

$$z = \frac{1}{\alpha_t}\ln\left[\frac{1}{2\pi f_0 \tau_0}\,\frac{1+\exp\left(\frac{E_T-E_F}{k_BT}\right)}{\exp\left(\frac{E_B}{k_BT}\right)}\right] \quad [6]$$

with f_0 the corner frequency of the spectrum. As this analysis is only feasible for RTN, the trap density profiles will be derived from the 1/f noise spectra under the elastic tunneling assumption.

Impact Capping Layer on Low Frequency Noise Performance

This section gives a systematic study of the impact of the implementation of capping layers for V_T engineering on the low frequency noise and, therefore, on the quality of the gate stack. Various process conditions will be investigated, including the position of the cap layer in the stack gate, i.e., above or below the high-κ dielectric, and the thermal budget of the post gate stack deposition, implemented in a Dynamic Random Access Memory (DRAM) process flow. During the thermal processing the metal atoms from the capping layer will diffuse and therefore modify the dipoles at the SiO_2/HfO_2 interface by the bond dipole effect.

The work is focussing on HfO_2 gate dielectrics (1.2 nm SiO_2 interfacial oxide and 2 nm HfO_2 with a 5 nm TiN metal gate) using Al_2O_3

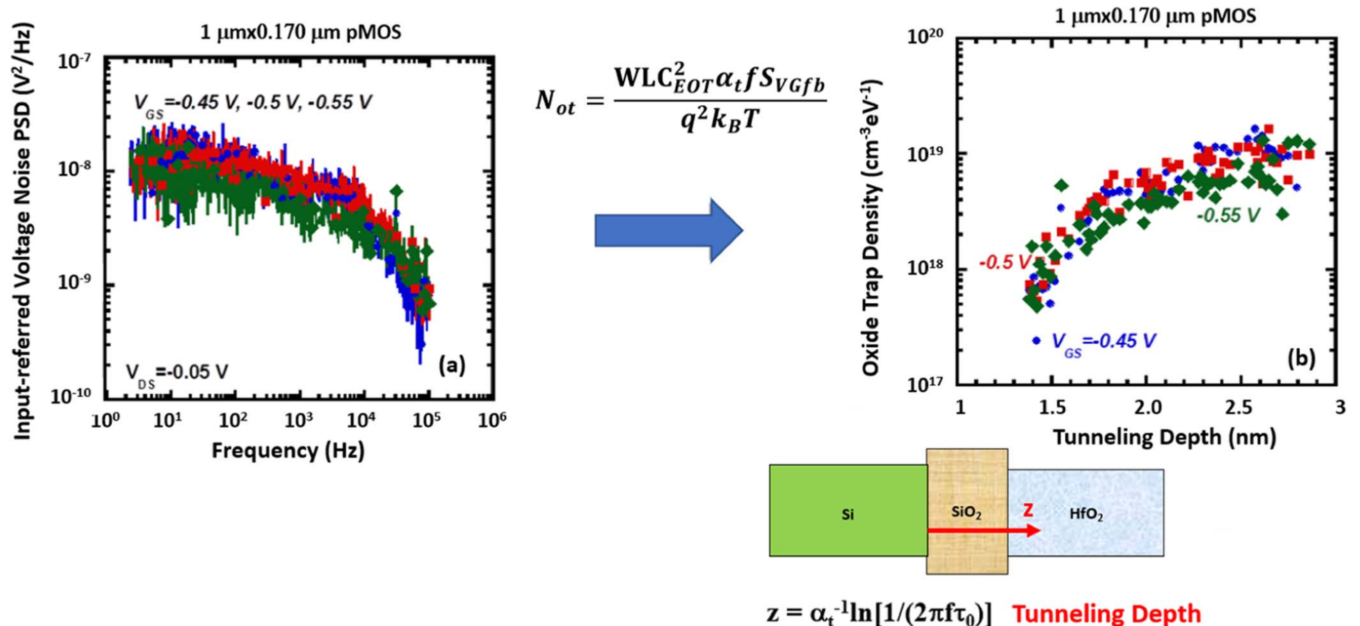

Figure 2. Principle of border trap profiling under the assumption of elastic tunneling to traps in the oxide. The input-referred voltage noise PSD (a) is the basis to calculate from its flatband value the oxide trap density, while the frequency is converted into a depth scale enabling to determine the trap profile (b).

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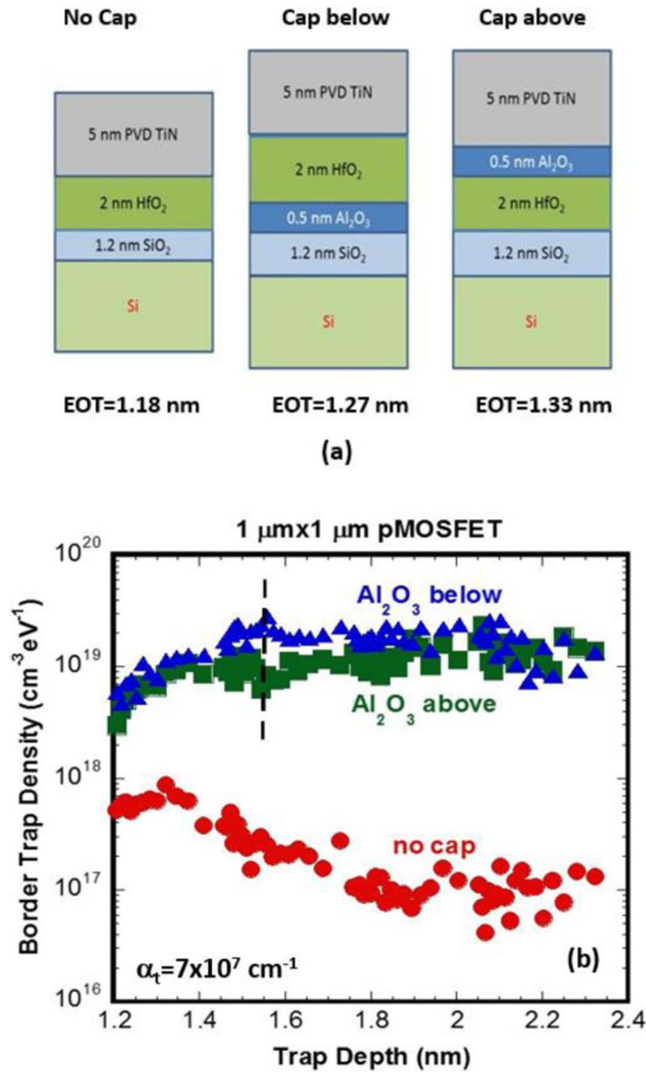

Figure 3. Gate stack configuration for the pMOSFETs without or with a 0.5 nm Al_2O_3 cap layer (a) and (b) corresponding border trap density profile for 1 μmx1 μm pMOSFETs derived from a $1/f^{\gamma}$ spectrum around threshold voltage V_T.

and La-oxide or Mg as a capping layer for p- and n-channel devices, respectively. This gate stack is typically used for DRAM peripheral logic devices.

Al_2O_3 for pMOS work function tuning.—First the location of the 0.5 nm Al_2O_3 cap, i.e., below or above the HfO_2 layer as shown in Fig. 3a, was studied. The corresponding border trap profiles are given in Fig. 3b, taking into account an attenuation factor of 7×10^7 cm^{-1} for the HfO_2 dielectric. In the case of a capping layer underneath the high-κ dielectric, a different attenuation factor has to be used for the cap layer and the dielectric. The depth scale used in Fig. 3b is selected in order to illustrate the trap profile in the gate dielectric. It can clearly be seen that i) the use of a capping layer increases the trap density and ii) an Al_2O_3 layer on top of the HfO_2 dielectric is beneficial compared to the layer below.

The impact of a high temperature anneal, as typically used during DRAM processing, is shown in Fig. 4 for a cap layer on top. This step results in a diffusion of Al into the high-κ layer. The figure indicates that for a capping layer on top of the high-κ dielectric there is up to about 900°C only a slight impact of the anneal temperature on the average border trap density. There is, however, a pronounced increase in both median trap density and spread in the data for higher temperatures. A possible interpretation could be that the anneal effect of the temperature treatment is reduced by the in-diffusion of Al. Another factor which could play a role is the crystallization of the HfO_2 at higher anneal temperatures that could introduce grain boundaries and, hence, more noisy traps.

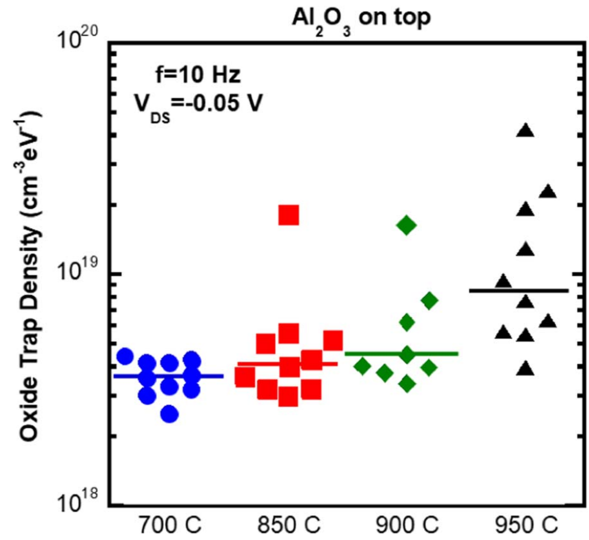

Figure 4. Oxide trap density for DRAM peripheral pMOSFETs with Al_2O_3 cap above the high-κ layer as a function of the diffusion annealing temperature. The noise measurements have been performed in linear operation (V_{DS} = −0.05 V) on 1 μmx0.170 μm pMOSFETs. The oxide trap density has been derived from the S_{VG} at f = 10 Hz in the flatband part of the S_{VG} versus V_{GS} characteristic. The solid lines are referring to the median values.

The used frequency of 10 Hz in Fig. 4 corresponds with a trap depth well located in the HfO_2 layer. By extending the frequency range detailed trap profiles are obtained as shown in Fig. 5 for different anneal conditions. It is clearly seen that the trap density reduces near the SiO_2/HfO_2 interface. A lower trap density is found for a lower anneal temperature. Assuming that the lower trap density corresponds to the SiO_2 IL, one can estimate the position of the interface with HfO_2, to be somewhere between 1.5 and 1.7 nm, as indicated by the

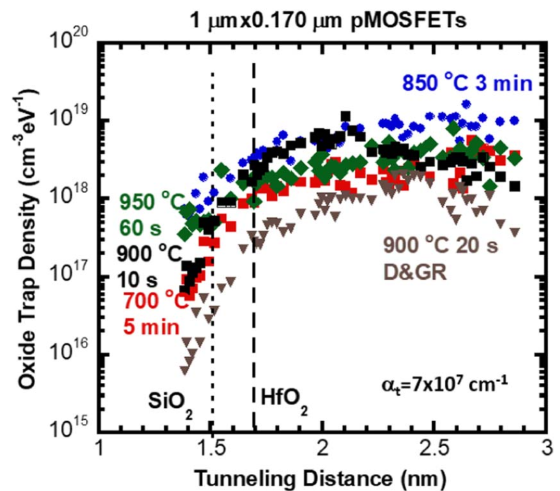

Figure 5. Oxide trap density profile derived from a LF noise spectrum around threshold voltage for DRAM peri pMOSFETs with Al_2O_3 cap layer on top and corresponding with different diffusion anneal temperatures. The dashed and dotted lines indicate the boundaries for the position of the SiO_2/HfO_2 interface.

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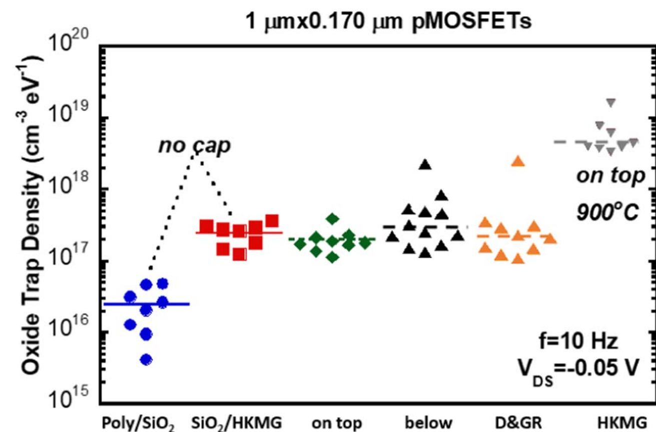

Figure 6. Oxide trap density at f = 10 Hz, derived from the input-referred noise measured in linear operation (V_{DS} = −0.05 V) in the flatband voltage part on 1 μmx0.170 μm pMOSFETs with different gate stack: polysilicon/5 nm SiO_2 references (blue symbols); 5 nm SiO_2 + 2 nm HfO_2 + 5 nm TiN (red symbols); 5 nm SiO_2 + 2 nm HfO_2 + 0.5 nm Al_2O_3 + 5 nm TiN (green symbols); 5 nm SiO_2 + 0.5 nm Al_2O_3 + 2 nm HfO_2 + 5 nm TiN (black symbols); D&GR scheme (orange symbols) and 1.2 nm SiO_2 + 2 nm HfO_2 + 0.5 nm Al_2O_3 + 5 nm TiN (grey inverted triangle symbols). The solid and dashed lines are median values.

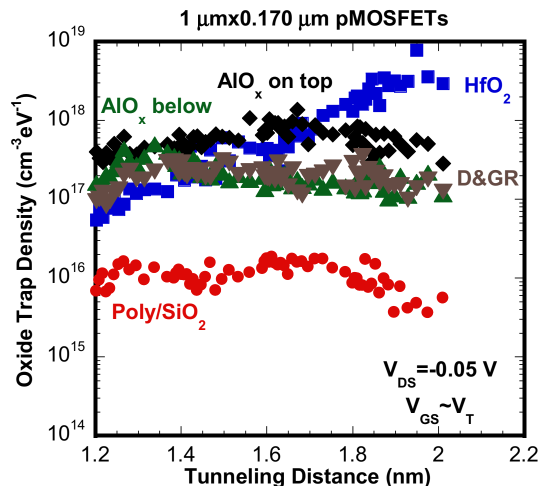

Figure 7. Oxide trap density profile derived from the low-frequency noise spectra of a pMOSFET for each split with 5 nm SiO_2 at V_{GS}∼V_T and V_{DS} = −0.05.

dotted and dashed lines in Fig. 5. It is even a bit lower in Fig. 3b. This allows to estimate an error in the trap density position in the range of 0.3 to 0.5 nm by using the elastic tunneling model of Eq. 3. In other words, using the 1.2 nm SiO_2 thickness as a kind of marker, one can estimate the possible inaccuracy of the trap density derived from 1/f noise, using the procedure derived above. This will become even more clear for the nMOSFET data reported below.

To obtain a good insight in the importance of the position of the capping layer complementary electrical investigations were performed and resulted in the following conclusions:[25] i) the defect density profiles derived from the low frequency noise and charge pumping current are in agreement with what can be expected from traps related to Al diffusion, and ii) the highest peak density of traps depends on the location where the Al_2O_3 cap is inserted, i.e., for a layer below the high-κ there is a higher trap density in the SiO_2 layer, while for a layer on top there is a higher trap density in the HfO_2. Compared to the reference condition without a cap layer, using an Al_2O_3 cap layer results in a slightly higher trap density, slightly lower performances and shorter NBTI lifetime. However, the Al_2O_3 position has only a marginal impact on the NBTI reliability but increased leakage current and reduced LF noise for Al_2O_3 below HfO_2. Overall, preference is given to a top layer

There is a tendency for thick oxide DRAM peripheral (peri) Input/Output (I/O) pMOSFETs to make these devices compatible with the gate stack of the DRAM peri logic devices, implying that one wants to replace the standard thick-SiO_2/polysilicon combination by a SiO_2/HfO_2/ metal-gate stack.[20] Therefore, a comparison is made between the two process options either 5 nm SiO_2/poly Si or 5 nm SiO_2 + 2 nm HfO_2 + TiN metal gate. In the latter case, V_T tuning is performed by a thin Al_2O_3 cap either on top or below the high-κ layer. Figure 6 presents the spread in trap density and its median value while Fig. 7 shows the trap profiles, derived from the 1/f-like noise spectra around V_T. The data confirms previous observations that a high-κ stack has a lower quality than the thick SiO_2, while the additional degradation by inserting an Al_2O_3 cap is limited. There are in Fig. 6 two conditions with a cap layer on top, i.e., one with 5 nm SiO_2 (green symbols) and one with 1.2 nm SiO_2 (grey inverted triangle symbols). As the frequency is 10 Hz (about 2 nm depth) one measures the trap density in the SiO_2 layers in the first case, while this is in the HfO_2 layer for the second condition. This explains the higher trap density for the latter pMOSFETs. A Diffusion and Gate Replacement (D&GR) integration scheme, based on a diffusion anneal step of the SiO_2/HfO_2/Al_2O_3 stack before removing the cap layer and subsequently depositing the metal gate,[30] does not introduce a significant degradation of the SiO_2 in Figs 6 and 7. The advantage of the D&GR process is that the drive-in step can be done simultaneously for the p- and n-channel cap layers.

The different trap profile at longer depths for the HfO_2 case (Fig. 7) may be caused by the possible in-diffusion of Hf from the high-κ dielectric into the underlying SiO_2 layer resulting in the decaying profile toward the interface. Another reason could be the presence of generation-recombination noise causing humps in the 1/f spectra and add to the observed spread from device-to device. The latter may lead to a range of trap densities at each depth. The main goal of the study presented here is to outline the general differences between the SiO_2/poly devices and the other splits so that no further in-depth analyses have been performed. As a general conclusion it can be stated that when the poly/SiO_2 stack is replaced by a high-κ dielectric then preference is given to a top capping layer with a moderate temperature anneal. Compared to Al_2O_3 below the HfO_2 layer there is a reduction in the leakage current and increase in low frequency noise, while the NBTI reliability is not compromised.[25]

La-oxide or Mg caps for nMOS work function tuning.—The improved threshold voltage and device performance by using an ALD La_2O_3 capping layer to tune HfSiON/metal gate nMOSFETs has been reported by several authors.[6,31-34] It was also observed that the presence of the cap reduces the 1/f PSD.[13] This has been interpreted as a reduction by La of the effective trap density in the dielectric either by passivation of the defects or by shifting the energy levels outside the accessible window for 1/f noise through the formation of a dipole.[13,34]

For the first set of experiments reported here, the work function tuning of n-channel transistors is accomplished by either an Atomic Layer Deposition of a LaO_x cap on top of the HfO_2 or the use of a Mg cap, inserted in the TiN metal gate. Both processes are schematically illustrated in Fig. 8. Different thermal anneals are used to control the V_T shift, i.e., 275 mV (Low Thermal Budget - LTB), 175 mV (Medium - MTB) and 125 mV (High - HTB), respectively.

Figure 9 shows the border trap density profile for the three different anneals of the LaO_x cap layer, clearly indicating the impact of the thermal budget. A medium temperature anneal leads to the lowest trap density, while the density increases for higher thermal budgets.

For La there is a correlation between the La diffusion and the trap density. Based on Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) measurements the diffusivity of La in HfSiON has been

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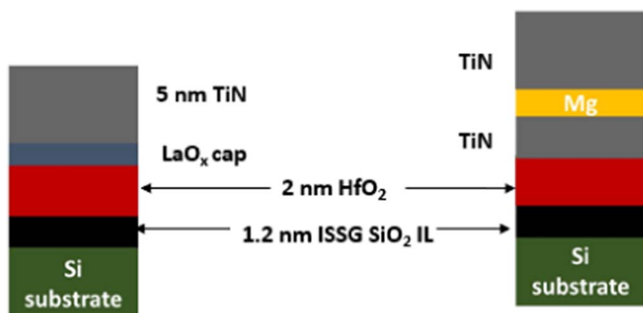

Figure 8. Schematic gate stack structure of the LaO_x cap (left) and Mg cap (right) for the V_T control of nMOSFETs.

reported as

$$D_{La} = 12.5 \times 10^{-10} \exp\left(\frac{1.04\ eV}{k_B T}\right)\ \mathrm{cm^2 s^{-1}} \qquad [7]$$

indicating that La is a rather fast diffuser in these high-κ oxides.[35] These authors observed that besides a thermally activated diffusion mechanism leading to the migration of La from the La_2O_3 capping layer to the HfSiON/SiO_2 interface, there is also a kinetic reaction mechanism acting due to the LaSiO dipoles formation at the interface. Due to the formation of the dipoles there is no La diffusion in the SiO_2 layer.[36]

The strong temperature dependence of the La behavior has also been observed for the Al behavior when Al_2O_3 is used as cap for p-channel devices.[37] The metal diffuses to the interface altering the dipole behavior required for the V_T tuning and it will also introduce additional traps in the HfO_2 layer.

Similar experiments have been performed for devices with a Mg cap. The border trap profiles are shown in Fig. 10a. It can be noticed that with a Mg cap there is a density peak near the SiO_2/HfO_2 interface (Fig. 10a) after the low budget anneal, which is eliminated by a higher thermal anneal (900°C). The trap density in the HfO_2 layer at larger depths is, for the transistors displayed in Fig. 10a, not influenced by the thermal budget of the anneal step.

It is interesting to compare the trap profile behavior for a Mg cap with the process condition when using an As implantation to tune the effective work function, by passivation of the oxygen vacancies (defects).[38,39] Implanting As in a nitrided-metal gate layer (e.g. TiN or TaN) through an amorphous Si buffer layer, as shown in Fig. 11a, releases nitrogen from the metal and passivates the deep traps in the high-κ layer.[40] Ab-initio calculations confirm that nitrogen-passivated defects are shifting to energetically shallower states.[41]

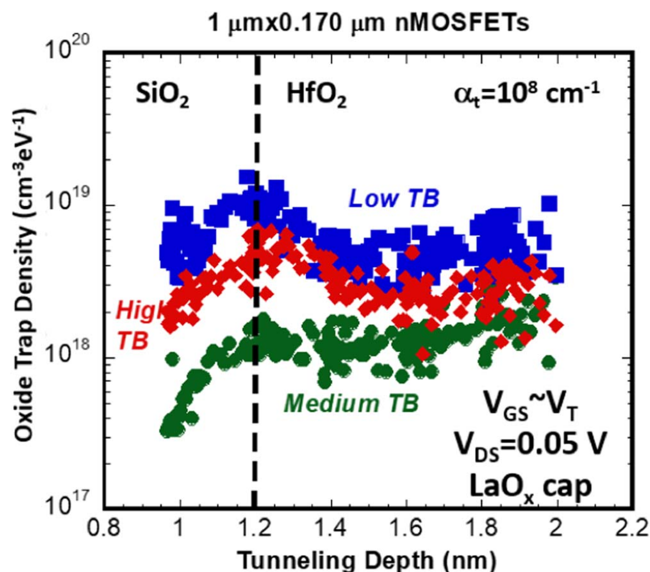

Figure 9. Border trap density calculated from the normalized input-referred voltage noise PSD for DRAM peri nMOSFETs with a LaO_x cap on top of the HfO_2 and corresponding with different diffusion thermal budgets.

The impact of the used tuning technique on the drain current is shown in Figure 11b for both the Mg cap and As implant. It can be noticed that the different curves have the same shape and only show a small impact of the used thermal budget. The shift of the curves to higher gate voltage values for the Mg cap is due to the shift of the threshold voltage (As II LTB = 0.65 V, As II HTB = 0.63 V) compared to the Mg cap (Mg LTB = 0.5 V and Mg HTB = 0.475 V). The influence of the threshold voltage tuning technique on the input-referred voltage noise PSD is given in Fig. 11c. The lowest noise level is observed for the As I/I HTB case, while reducing the thermal budget leads in both cases to an increase of the input-referred voltage noise, for the displayed devices. To calculate the trap density from the S_{VG} values at flatband, the values have to be normalized by the EOT of the stacks. Therefore the trend related to the noise may be different than the trend in trap density. It should be noted that a different trend appears for the Mg cap nMOSFETs when comparing all available data (see Fig. 12). An observed trend for selected devices may deviate from a general trend based on the study of a large number of devices due to the statistics involved. This is especially the case for sensitive parameters such as low frequency noise.

Figure 10b shows for the As implant approach the trap density profile for two different thermal anneals. Compared to Fig. 10a it can be seen that that the density peak, which is not located at the interface in this case but in the HfO_2, anneals out for higher temperatures. Figure 10 allows to conclude that the trap density in the HfO_2, away from the interface with SiO_2 is not sensitive to the thermal budget in both cases, for the selected devices. At the same time, the lower value in the As ion implantation case (5×10^{18} cm^{-3} eV^{-1} compared with $\sim 2.5 \times 10^{18}$ cm^{-3} eV^{-1}) confirms the anticipated N passivation effect. The main influence of the temperature during the post-deposition DRAM anneal is the removal of the defect peak, occurring around the SiO_2/HfO_2 interface for both the Mg and As ion implantation nMOSFETs in Fig. 10. Again, a possible range of the SiO_2/HfO_2 interface between 1.2 to 1.5 nm can be derived from the defect peak position, assuming that it corresponds approximately with this position.

Finally, Fig. 12 gives a comparison of the average trap densities observed for both LaO_x and Mg caps. The used measurement frequency of 1 Hz corresponds with a depth of 2 nm, i.e., located about 0.8 nm in the HfO_2 layer. Within the group of LaO_x cap nMOSFETs the lowest average (and median) trap density is found for the M- or HTB, which also removes the defect peak in Fig. 10. The opposite trend is found for the Mg nMOSFETs in Fig. 12: the lowest median N_{ot} for the LTB, however, corresponding with a larger dispersion; slightly higher values are found for the M- and HTB, which are on the average about 40% smaller than for the reference devices. Overall, compared to La, there may be for Mg a different behavior for the interaction between the metal and the defects (most likely oxygen vacancies) in the high-κ dielectric.

Summary

An overview has been given on the impact of the use of a metal oxide cap layer to tune the threshold voltage of transistors with SiO_2/HfO_2 gate stacks. Both Al_2O_3 (pMOS) and La-oxide or Mg (nMOS) were studied, pointing out their impact on the quality of the gate stacks by influencing the profile of the traps in the dielectric. Beside the type of capping layer, its position in the gate stack and also the thermal budget used during the device fabrication have a strong impact on the final result. The low frequency noise studies pointed out that besides affecting the dipole layer at the interface, key for tuning the effective work function, also the diffusion behavior of the metal during thermal treatments is impacting the passivation of traps and/or generation of additional oxide traps in the HfO_2 layer. A different behavior is observed for Mg compared to La, making the first one more temperature insensitive thereby less impacting the trap profile in the bulk.

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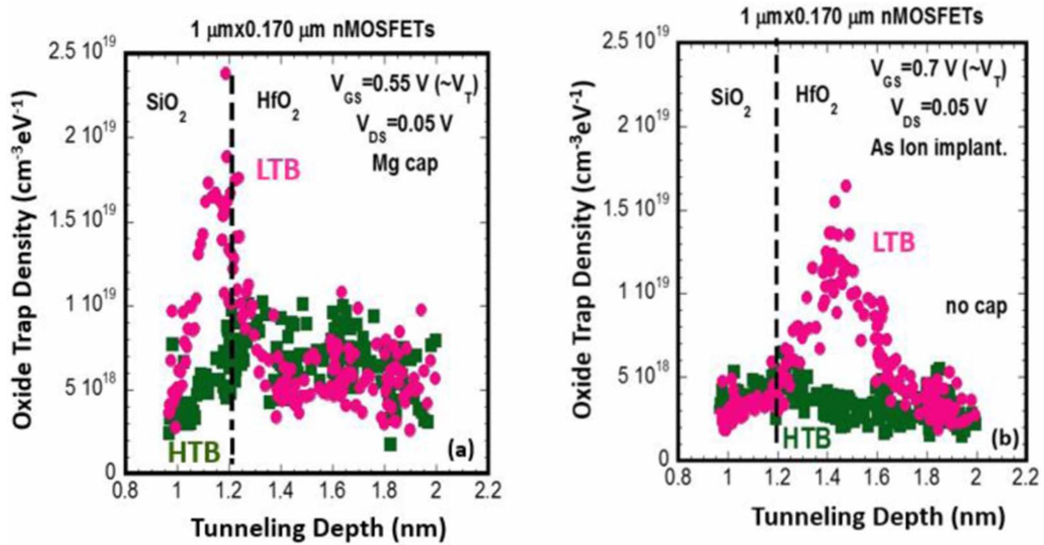

Figure 10. (a) Oxide trap density profile for DRAM peri nMOSFETs with a Mg diffusion shifter and corresponding with a low thermal budget (LTB) or a high thermal budget (HTB). (b) Oxide trap density profile for DRAM peri nMOSFETs with an As ion implantation in the nitrided-metal gate and corresponding with a low thermal budget (LTB) or a high thermal budget (HTB).

Figure 11. (a) Schematic gate stack structure for the As implantation approach (a) and impact of the approach on the drain current in comparison with the Mg cap technique, for different thermal treatments (b). The influence of the As implant and Mg cap conditions on the input-referred voltage noise PSD is also shown for a low and a high thermal budget (c).

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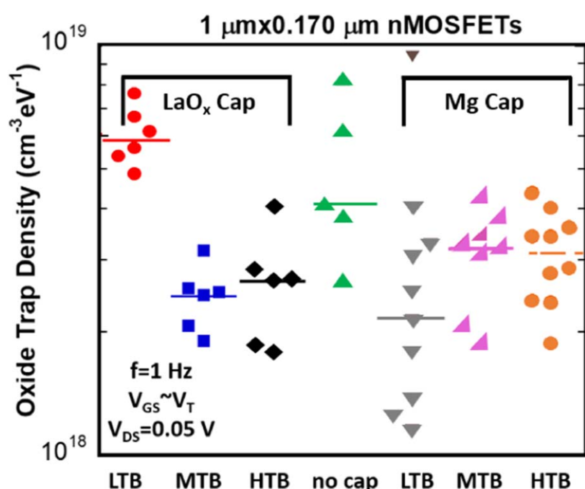

Figure 12. Oxide trap density corresponding with f = 1 Hz (∼ 2 nm depth) for 1 μmx0.170 μm nMOSFETs with LaO_x or Mg cap. Reference HKMG nMOSFETs without cap layer are also included. The solid lines are median values.

For DRAM applications, the best option remains the poly/SiO_2 stack. However, when for a better compatibility with CMOS processing the poly/SiO_2 stack is replaced by a high-κ dielectric then preference is given to a top capping layer with a moderate temperature anneal. Compared to Al_2O_3 below the HfO_2 layer there is a reduction in the leakage current and increase in low frequency noise, while the NBTI reliability is not compromised. Not only the trap behavior studied here, but all the different performance parameters have to be taken into account for selecting the most appropriate threshold voltage tuning approach for a particular application.

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