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FACULTY OF ELECTRICAL ENGINEERING

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MASTER'S THESIS

AREA ALLOCATION FOR YIELD OPTIMIZATION IN INTEGRATED CIRCUIT

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Bibliography / sources:

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K. J. Kuhn et al., 'Process Technology Variation,' IEEE Trans. Electron Devices, vol. 58, no. 8, pp. 2197-2208, Aug. 2011.
S.R. Sarangi et al., 'VARIUS: A Model of Process Variation and Resulting Timing Errors for Microarchitects,' IEEE Trans. Semiconductor Manufacturing, vol. 21, no. 1, pp. 3-13, February 2008.

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Popište vznik náhodných a systematických chyb při výrobě integrovaných obvodů a důsledky na variaci technologických procesů. Navrhněte možnou strategii pro snížení dopadu těchto chyb. Navrhněte vyhodnocovací obvod těchto chyb a navrhněte topologii vhodnou pro ověření strategie rozvržení umístění obvodových komponent na čipu.

Seznam doporučené literatury:

Y. Lin, D. J. Chen, and R. Geiger, 'Yield enhancement with optimal area allocation for ratio critical analog circuits,' IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 53, pp. 534-553, March 2006.
K. J. Kuhn et al., 'Process Technology Variation,' IEEE Trans. Electron Devices, vol. 58, no. 8, pp. 2197-2208, Aug. 2011.
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V Praze, dne ……………………………………..

Martin Košťál

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ABSTRACT

Recent research in yield enhancement techniques and mitigation of device mismatch is presented. Systematic and random mismatch is studied and identified as the cause of device mismatch. Model based on log-normal PDF is introduced. Optimization of IC parameter yield is suggested and conducted with help of a new methodology based on mathematical programming. An algorithm for the impact based area allocation of critical matched devices is shown as well as algorithms for common centroid layout of different sized devices. Newly developed algorithms are presented on binary weighted R-2R DAC as it is a common IC and comparison to other solutions is given.

ABSTRAKT

Práce seznamuje s metodami návrhu pro zvýšení výtěžnosti a omezení chyb ve shodných strukturách. Systematické a náhodné chyby jsou shledány zdrojem neshod mezi strukturami. Je představen model náhodných chyb za využití log-normálové hustoty pravděpodobnosti. Pomocí nové metodologie založené na celočíselném pogramování (celočíselné optimalizaci) je navržena optimalizace parametrické výtěžnosti integrovaných obvodů. Je představen algoritmus generování optimální topologie. Topologie je demonstrována na R2R D/A převodníku a výsledky jsou porovnány s jivým řešením.

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List of Acronyms

DAC ... Digital-to-analog converter

D2D ... Die to die

CDAC ... Capacitive digital-to-analog converter

CMOS ... Complementary Metal-Oxide-Semiconductor

EUV ... Extreme ultraviolet (lithography)

IC ... Integrated circuit

ILP ... Integer linear programming

INL ... Integral non-linearity

LP ... Linear programming

LSB ... Least significant bit

MSB ... Most significant bit

NLP ... Non-linear programming

OPA ... Operational amplifier

PCA ... Programmable capacitor array

R2R ... Resistor ladder in R-2R configuration

WID ... Within die

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Introduction

For years the silicon chip industry is driven by Moor's law. The continuous evolution of chip fabrication technology decreases feature size, improves power efficiency and device density but also introduces new problems and challenges. In latest sub-micron semiconductor technologies impact of process variation becomes more significant. The so called systematic and random mismatch is one of the reasons of malfunctioning chips, thus causing deterioration in yield.[1][2][3][4] To overcome those problems techniques such as double patterning or wide design and polish improvement have to be applied to the fabrication process. The latest development in Intel's 10nm node promises to use EUV lithography to increase both precision and accuracy. Other foundries plan to implement EUV for 7nm+ node. [24] Non of the above improvements in technology is an ultimate solution to the process variation, so engineers are required to adjust their chip for estimated variation. In 2014 under the International Technology Roadmap for Semiconductors 2.0 7 Focus Teams were established to identify future challenges and to issue current ones.[28]

Furthermore process variation and its impact resulting in device mismatch has been studied in [4][5][6]. These works gives us strong understanding in process variation and device mismatch. Some works studied layout strategies for improving the yield of analog IC [9][10][11], but only [12][13] suggested area allocation based yield enhancements.

Usually the area allocation for yield enhancement is limited only to identifying the critical devices of the analog circuit and increasing its area to ease the negative impact of random mismatch. This enhancement is based on the inversely propor-

tional dependency of the standard deviation of device parameters to the square root of the device area [14].

For highly matched components increasing critical device areas may not result in optimal solution, due to increase in power dissipation or parasitics. It is necessary to always consider the trade-off and balance the solution. Balancing area allocation of more critical devices on chip is not well explored and is aim of this work.

In [12].some preliminary ideas for yield enhancement through minimization of the standard deviation of the interested parameter are given. A yield enhancement strategy for feedback network, R-2R ladder and resistor string DAC is presented.

Further in this work ideas of Chen's research group [21] are presented and further optimization is presented.

In Chapter 1 the process variation is explained. It covers topics on both random and systematic mismatch. Second chapter gives overview of R2R allocation strategy to minimize impact of random variation on binary weighted circuit.

Chapter 3 gives an overview of optimization field called mathematical programming.

Chapter 4 studies different layout strategies for minimal systematic device mismatch in R2R DAC.

In chapter 5 R2R DAC architecture and R2R area allocation optimization is described.

Chapter 6 evaluates the proposed layout pattern for R2R DAC. Overall results are given in 7.

Chapter 8 concludes this work and gives thoughts on further work.

1 Process Variation and Mismatch

1.1 Process Variation

If it were not for process variation, this work would have never existed. This work concerns process variation in silicon CMOS processes. The basic understanding of process variation is deviation of parameter of manufactured structure from the intended specifications [15]. Process variation is caused by processing and masking limitation, thus with smaller technology nodes the variation becomes more pronounced. Process variations can be categorized as die-to-die (D2D), concerning the differences from die to die, and within-die (WID), concerning differences of same components on die. If correlation distance of the process variation is considered, global and local variations can be distinguished [14]. Another classification of the process variation is by the cause and predictability of the process variation, co called systematic and random variations [16][17]. The cause for systematic variation is in lithographic aberrations. Random variation arise from doping, crystallographic disorders and edge roughness. The systematic variation is spatially correlated, thus causes devices next to each other to have similar parameter deviation, on the contrary the random variation affects devices without any spacial correlation.

Effect of the process variation is getting more significant with every technology node, which take the silicon industry closer to the limits. To have a better perspective, the common ArF laser used for photo-lithography emits 193nm light, the EUV lithography is using 13,5nm wavelength but is yet to come into commercial application. With use of immersion lithography and double-, quad-patterning the limit s can be pushed further. Next limit to face is atomic radius. Radius of Si atom is 111pm (0,111nm) [32]. Considering for example the 180nm node, that is very popu-

lar for analog designs, 1% miss from feature size means only 16atoms. Process variation is significant challenge especially in analog integrated design due to device mismatch.[18]. The process variation can cause the manufactured chip not fulfilling specification, hence the overall yield gets lower.

The combat against process variation is done by both the silicon foundries and IC designers. The foundries implement techniques mentioned before, but the IC designers must take the process variation into account as well and take advantage of design strategies to mitigate the effects of process variation.

In the following sub-chapters mismatches in ICs and strategies how to combat it are discussed.

1.2 Mismatch in Integrated Circuits

Mismatch is defined as differential performance of two or more devices within the chip [18]. Device mismatch in ICs caused by random or systematic process variations is called accordingly random and systematic mismatch. Random mismatch can be considered stochastic, thus can not be predicted. Systematic mismatch can be considered deterministic and can be predicted.

The mismatch between two devices is a deviation of a parameter from intended ratio between two components [19]. Device mismatch δ is defined as:

$$\delta = \frac{(x_2 / x_1) - (X_2 / X_1)}{(X_2 / X_1)} = \frac{X_1 x_2}{X_2 x_1} - 1 \quad (1)$$

where X_1 and X_2 are the intended parameter values and x_1 and x_2 are the real (measured) parameter values of manufactured components. Device mismatch has to be minimized in ratio critical circuits such as current mirror, differential amplifier, binary weighted and R-2R ladder circuits, because they depend on matched components heavily. The device mismatch given by (1) applies for one specific pair of devices and vary for any different pairs. Observation of device mismatch across

selected amount of sample chips gives important data, which can be further examined. Mean m_δ and the standard deviation σ_δ of the mismatch is given as function of mismatch δ_i:

$$m_\delta = \frac{1}{N}\sum_{i=1}^{N} \delta_i \tag{2}$$

$$\sigma_\delta = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N} (\delta_i - m_\delta)^2} \tag{3}$$

The mean of the device mismatch m_δ is understood as systematic mismatch component and the standard deviation (σ_δ) as random mismatch component. The mean and standard deviation of the mismatch can be utilized to predict worst case device mismatch using three-sigma or six-sigma, as often used in probability theory.

Device matching is crucial in analog integrated circuits and mismatched critical devices directly impact the performance of these circuits. The device mismatch can not be avoided, but can be reduced with proper techniques which usually come with trade-offs in increased complexity in design or in manufacturing. To reduce the mismatch caused by process variation, analog IC design needs to be taken with care of diligence. Especially high attention needs to be paid to layout of critical devices, which have high impact on the overall performance of the IC. Several layout patterns such as common centroid, mirror layout and shuffled layout have been introduced to reduce systematic mismatch [11][20]. Also random mismatch can be mitigated by minimizing the variance by allocating more area for the critical devices, because the standard deviation of any performance parameter is inversely proportional to the square root of the device area [14]. The detail of systematic and random mismatch along with the layout and area allocation strategies will be described in detail in the following chapters.

1.3 Systematic Mismatch

Systematic mismatches are caused by mechanisms such as process variation that influence all of the samples in similar manners. Systematic variations in a single die create gradient error which leads to systematic mismatches. However, this mismatch is not only caused by systematic variations. It can also stem from contact resistances, non-uniform current flow, mechanical stresses and temperature gradients. As in process variation, systematic mismatches also exhibit spatial correlation and emerge as spatial gradients in device parameters.

Because systematic mismatches have spatial dependence, the increasing of device area makes the gradient effect more significant. Reducing the distance among critical devices can also reduce instead of cancel the gradient effect due to high spatial correlation. The main factor affecting the circuit yield related to systematic mismatch is the layout pattern. Essentially, to reduce mismatch caused by spatial gradient, the critical devices in pair should be laid out with balance. Therefore, some existing layout strategies have been introduced to deal with the systematic mismatch. The common centroid layout is the widely used pattern to cope with systematic mismatch [11][19]. The basics of the common centroid pattern is to have a balanced layout topology for all devices with the center point as the device centroids. Fig. 1 shows an example of common centroid layout produced by placing segments of matched devices into an array along one dimension. This type of layout is usually called interdigitated array because the sections of one device interpenetrate the sections of the other like the intermeshed finger of two hands.

Although the common centroid pattern is relatively easy to be implemented, it is only effective to compensate linear gradient. The other layout patterns such as circular symmetry pattern has the potential to cancel nonlinear gradients, but it is not easy to be implemented in most of recent processes. The Nth order central symmetrical layout pattern has been proven mathematically to cancel nonlinear gradi-

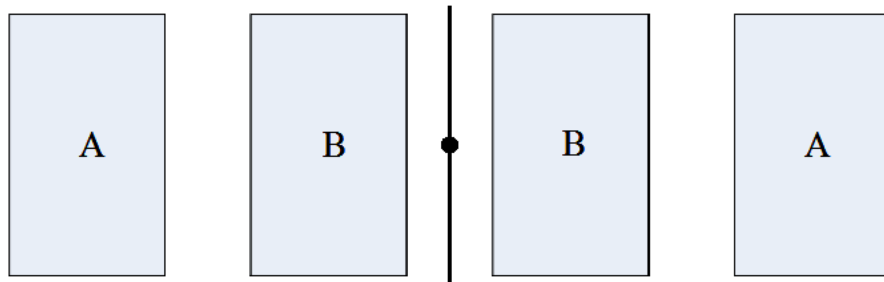

Fig. 1: Integrated array common centroid layout

ents. However, this layout pattern can only be applied for matching two critical devices. The shuffle and shuffle mirror layout pattern have been introduced to compensate linear gradient for matching many integrated devices in a single circuits[20].

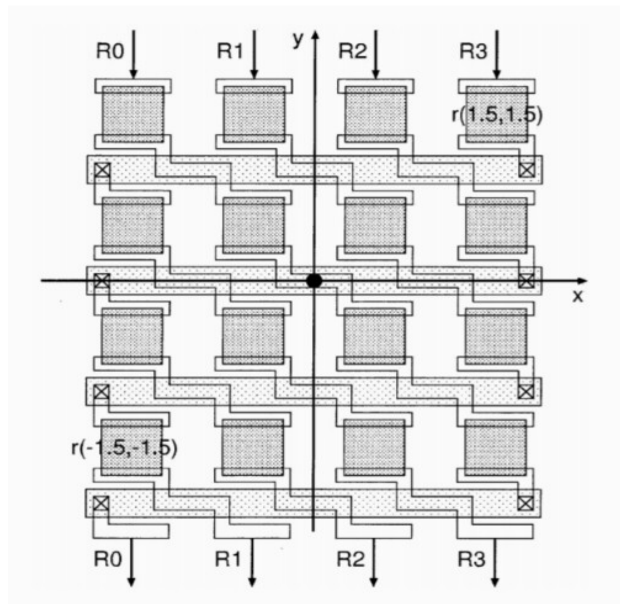

Fig. 2: Shuffle pattern for 4 resistors [20]

1.4 Random Mismatch

The random mismatch represents a portion of the mismatch which is stochastic. The cause of the random mismatch is stochastic processes in manufacturing and inconsistent material properties such as oxide thickness, crystallographic disorders, photoresist edge roughness, impurities, doping concentrations, and

other [19]. There are two types of fluctuation indicated by devices in integrated circuit: fluctuation that occur only along the edges of the device and fluctuation that occur throughout the device. The former is called peripheral fluctuations because they scale with device periphery. The latter is called areal fluctuations because they scale with device area.

The basis for random mismatch modeling was explained with an example in [18]. The peripheral fluctuations in the observed length L depend on the width of the device and likewise for the observed width.

$$\sigma_L^2 \propto \frac{1}{W} \tag{4}$$

$$\sigma_W^2 \propto \frac{1}{L} \tag{5}$$

The local variation of parameters such as sheet resistance, channel dopant concentration, mobility and gate oxide thickness have an area dependency.

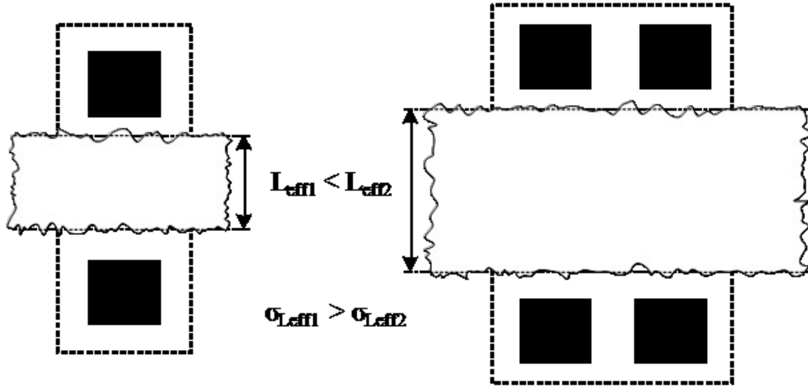

Fig. 3: Periphery fluctuation as the effect of local random variation

$$\sigma_P^2 \propto \frac{1}{WL} \tag{6}$$

Fig. 3 shows the notion of periphery fluctuation in relation to the local random variation. Local random variations decrease as the device size increases since the

parameters averaged over a greater distance or area. This is the basis of most of the random mismatch model used for device sizing in many circuits.

1.5 Pelgrom's Model

The most universal model applied for determining sufficient sizing of CMOS transistors to cope with mismatch due to random process variations is Pelgrom's model[14]. Pelgrom's model for the matching of a process parameter *P,* such as resistance or capacitance, between two critical devices is given by the following equation:

$$\sigma^2_{\Delta P} = \frac{A_P^2}{WL} + S_P^2 D^2 \tag{7}$$

Where $\sigma^2_{\Delta P}$ is the variance of the difference of parameter *P*. The A_P is Pelgrom coefficient, which is area proportional constant usually measured and provided by foundry. The S_P is spacing proportional constant, which is provided by foundries. S_P can be modeled by gradient modeling methods. The *W*, *L* and *D* is width, length and spacing of the devices. The first addend expresses the random variance component and the second systematic component. From this, it is clear, that the device parameter deviation is inversely proportional to square root of the device area.

$$\sigma_P \propto \frac{1}{\sqrt{Area_P}} \tag{8}$$

Assume the sources of systematic mismatches are eliminated, enhancing device matching can be done by increasing the area of critical devices. However, increasing the area of all devices will not generate the optimum solution for matching components, since the larger device area often introduces additional power dissipation and parasitic. It is always reasonable to allocate more area to the devices with heavier weight, impact on the yield, to reduce the performance deviation of the

whole circuit. The question about how to share the chip area among critical devices to get the highest possible yield according to a specific area budget is investigated in this work.

1.6 Area Allocation Strategy Overview

The yield enhancement with optimal area allocation for analog circuits was introduced through minimizing the standard deviation of the interested parameter, such as gain or integral nonlinearity (INL), for the critical devices [12]. It provided different area allocation strategies for some important analog circuits, such as feedback network, R-2R ladder, and resistor string DAC. A statistical model for the effect of contact resistance upon the performance of matching-critical circuits is also provided. In order to achieve significant improvements in parametric yield with less intuition, the layout principles for several representative analog circuits have been introduced as follows:

- *Layout Principle for Ratio-Matched Resistor:* The effects of local random variations in sheet resistance in the ratio matching accuracy of two rectangular resistors are minimized for a given total resistor area if equal area is allocated to the two resistors.
- *Layout Principle for R-2R DACs:* The effects of local random variations in sheet resistance upon the INL for R-2R DACs comprised of rectangular resistors are minimized for a given total resistor area if proportionally more area is allocated to the more significant bits. But the optimal area allocation is dependent upon how the R-2R network is used.
- *Layout Principle for Resistor Strings:* The effects of local random variations in sheet resistance upon the INL for Resistor String DACs comprised of rectangular resistors are minimized for a given total resistor area if equal area is allocated to each of the resistors.

- *Layout Principle for Ratio-Matched Resistors (Including Contact Resistance Effects):* The combined effects of local random variations in sheet resistance, contact resistance and edge variations upon the ratio matching accuracy of two resistors are minimized for a given total resistor area if an equal number of unit cells, connected in a parallel, series, or parallel-series configuration, are allocated to the two resistors.

These layout principles were presented in a case-by-case basis depending on the circuit being analyzed. Moreover, most of the optimum area allocations were provided with the help of simulations only. The sliced simulation results around optimum give a limited view of the true optimum ratio for area allocation strategy. Another significant issue about how to implement the area ratio into a real layout was only presented with near optimum schemes. Further theoretical analyses seem inevitable to make the recommended strategies even convincing. A wider area ratio range needs to be explored to provide a more general rule for device area allocation than before.

1.7 DAC performance metric and yield

The key metric for yield evaluation in this thesis is integral non-linearity (INL). For each input a deviation from ideal linear output is given by

$$INL_i = \frac{I_i - I_0 - i\frac{I_{N-1} - I_0}{N-1}}{\frac{I_{N-1} - I_0}{N-1}} \tag{9}$$

Where I_i is current output of the DAC corresponding to the decimal input of i, I_0 is the minimal output current at zero input and I_{N-1} is the maximum current output. The INL is than the worst value:

$$INL = \max_{0 \leqslant i \leqslant N-1} |INL_i| \tag{10}$$

The DAC chip is considered faulty if the INL is worse than a certain threshold. Than the yield is ratio of faulty to all chips.

As further in this work the focus is on tuning R2R network, it is assumed that voltage reference and operational amplifier of the DAC are ideal, thus have no effect on yield.

1.8 Statistical Description of Variation

Some statistical descriptions for parametric variation are used to model the effect of process variation. The most basic statistical approach is to characterize the distribution of some parameter of interest P over samples of devices or structures, and to estimate some small number of statistical moments to characterize that distribution. Lumped statistics, the commonly used statistical description, is introduced to simplify the model of process variation [15]. In this approach, the detail of the physical sources of this variation is not considered. Instead, the combined set of underlying deterministic as well as random contributions is simply lumped into a combined random statistical description as shown in (11).

$$P = P_0 + \Delta P \tag{11}$$

With P_0 is the nominal value of interest parameter and ΔP is the variation of the parameter of interest. From their causes, ΔP can be further divided as follows [17]:

$$\Delta P = \Delta P_{D2D} + \Delta P_{WID} = \Delta P_{D2D} + \Delta P_{rand} + \Delta P_{sys}. \tag{12}$$

For simplicity, normal distribution is usually used to model the random and systematic variations. The other distributions such as linear, binomial and log-normal distribution have also been used for modeling instead [6][17]. The linear and binomial distribution, however, cannot be considered as the correct distribution in process variation for practical situations and can be applied in the mathematical analysis only.

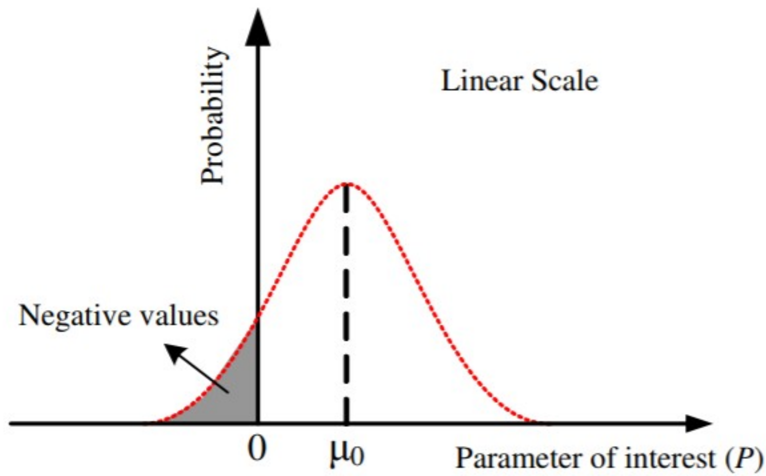

Fig. 4: The probability density function (PDF) of normal distribution in linear scale

Normal distribution, used in many analyses and simulations, is a reasonable approximation to the distribution for modeling process variation. However, in [21], normal distribution is only efficient and accurate enough when the process variations are sufficiently small. It is always possible to get negative physical quantity using a normal distribution model as shown in Fig. 4. In the case where the sample data is quite large or the standard deviation is relatively high, the probability of getting negative physical quantity will be larger. Limiting the negative value to be all zero in normal distribution, however, cannot generate the most practical simulation result.

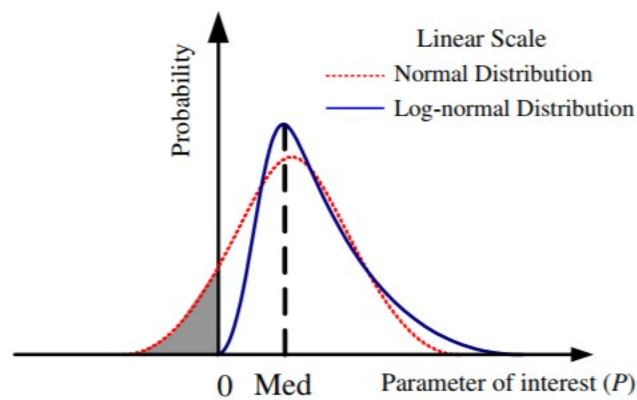

Fig. 5: The PDF of normal and log-normal distribution in linear scale

On the contrary, log-normal distribution has zero possibility of negative device value as shown in Fig. 5. It gives a more practical simulated yield output compare to the other distributions [1]. Log-normal distribution is more realistic distribution for modeling process variation and thus adopted in this thesis. The random variable Y with log-normal distribution is defined as following

$$Y = e^{\mu + \sigma Z} \tag{13}$$

where μ is mean, σ is standard deviation and Z is standard normal variable (random variable with normal distribution).

With log-normal distribution, any device parameter after fabrication is scaled up or down from its nominal value by a scaling factor. Therefore, the parameter of interest P of any device after fabrication can be expressed with the following equation in linear scale:

$$P = \lambda \cdot P_0, \tag{14}$$

where λ is the scaling factor which decides how much is the corresponding variation. In log scale, can be written as follow:

$$P_{dB} = P_{0dB} + \Lambda. \tag{15}$$

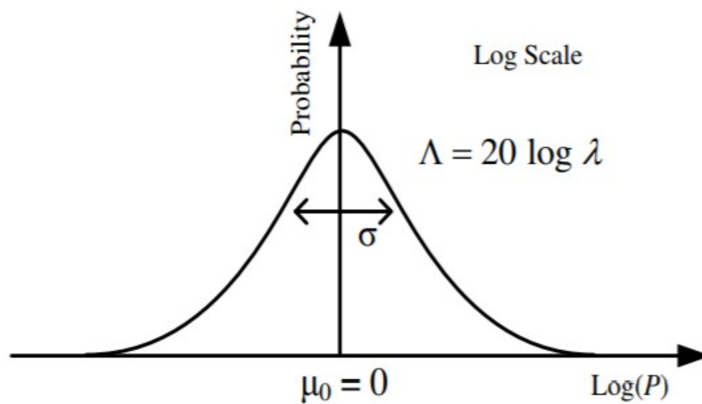

Fig. 6: The PDF of scaling factor in log scale

The log value of λ, Λ, has a normal distribution with zero mean as shown in Fig. 6. With sufficiently small standard deviation, normal distribution behaves like log-

normal one. This can be explained by the following approximation in linear scale derived from the Taylor series for the exponential function:

$$\lim_{\Lambda \to 0} P \cdot e^{\Lambda} \approx P(1+\Lambda) \tag{16}$$

Thus normal distribution with sufficiently small standard deviation can also be used to generate efficient and accurate enough simulations as presented in some former papers.

2 Proposed R2R ladder allocation strategy

This section explains the findings of [21] regarding R2R ladder network and suggests a strategy to mitigate the effect of random variations on matching through area ratios optimization. R-2R resistor network is shown in Fig. 7. For purpose of area allocation strategy ratios *m* and *k* are defined, where *m* is bit to bit area ratio and *k* is inner bit area ratio of the resistors. Tab. 1 shows the value of area ratios proposed in [12] based on simulation.

Tab. 1: Proposed area ratios of R-2R ladder [12]

ratio coefficient	
m	1.7
k	2.2

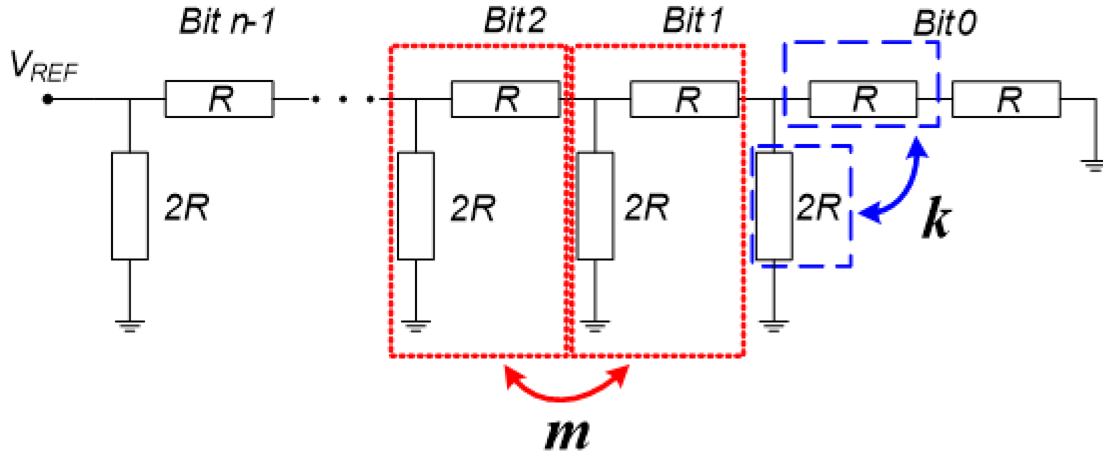

Fig. 7: R-2R ladder circuit, m is bit to bit ratio, k is inner bit ratio

In [21] the area ratios are derived from current ratio of bit 0, example circuit is given in Fig. 8

$$\frac{I_0}{I_1}=\frac{R_{2R0}}{R_{R0}+R_{R'0}}=\frac{2R_N+\Delta_{2R0}}{2R_N+\Delta_{R0}+\Delta_{R'0}} \tag{17}$$

Assuming that the variations of resistances $\Delta_{R0}, \Delta_{R'0}, \Delta_{2R0}$ are very small and using approximation

$$\frac{I_0}{I_1}\approx 1+\frac{\Delta 2R_0}{2R_N}-\frac{1}{2}\frac{\Delta R_0}{R_N}-\frac{1}{2}\frac{\Delta R_0^{'}}{R_N}. \tag{18}$$

from the linear combination of variations the variance is

$$\sigma_{I0/I1}^2=\sigma_{2R0}^2+\frac{1}{4}\sigma_{R0}^2+\frac{1}{4}\sigma_{R'0}^2 \tag{19}$$

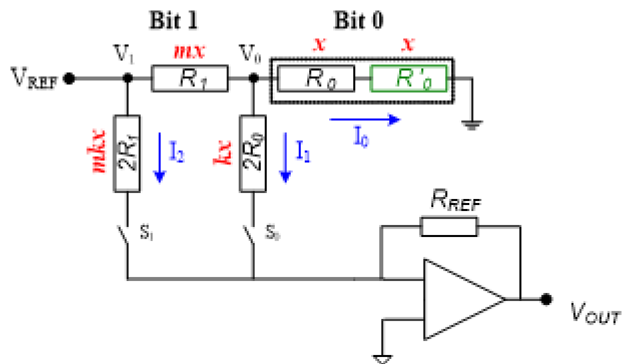

Fig. 8: 2bit R-2R ladder circuit [21]

The variance is inversely proportional to area

$$\sigma_{I0/I1}^2=\alpha^2\left(\frac{1}{A_{2R0}}+\frac{1}{4A_{R0}}+\frac{1}{4A_{R'0}}\right) \tag{20}$$

where α is Pelgrom's area constant divided by a nominal sheet resistance and A_X are areas of the resistors. Assume x is the area of R_0 and R'_0 the total area of bit 0 is

$$A_{bit0}=x(k+2) \tag{21}$$

$$\sigma_{I0/I1}^2=\frac{\alpha^2}{A_{T0}}\left(2+\frac{k}{2}+\frac{2}{k}\right) \tag{22}$$

The global minimum of variance is found at k equals 2. Than bit current ratio I_2/I_1 is calculated to get optimum value of m.

$$\frac{I_2}{I_1}=\frac{R_{2R0}(R_{R1}+R_{R0}+R_{R'0})+R_{R1}(R_{R0}+R_{R'0})}{R_{2R1}(R_{R0}+R_{R'0})} \tag{23}$$

Similarly as in equation (17)

$$\frac{I_2}{I_1}\approx 2-\frac{2\Delta_{2R1}}{R_{2N}}+\frac{\Delta_{R1}}{R_N}+\frac{3\Delta_{2R0}}{2R_{2N}}-\frac{\Delta_{R0}}{4R_N}-\frac{\Delta_{R'0}}{4R_N} \tag{24}$$

and variance becomes

$$\sigma_{I2/I1}^2=\alpha^2\left(\frac{4}{A_{2R1}}+\frac{9}{4A_{2R0}}+\frac{1}{A_{R1}}+\frac{1}{16A_{R0}}+\frac{1}{16A_{R'0}}\right) \tag{25}$$

The total area can be expressed as

$$A_T=x(km+m+k+2)=A_{2R1}+A_{R1}+A_{2R0}+A_{R0}+A_{R'0} \tag{26}$$

and variance becomes

$$\sigma_{I2/I1}^2=\frac{\alpha^2}{A_T}\left(\frac{4}{kmx}+\frac{9}{4kx}+\frac{1}{8x}+\frac{1}{mx}\right)(km+m+k+2)x \tag{27}$$

Than k equals 2 and m is approximately 1.78885 as shown in Tab. 2

Tab. 2: Proposed area ratios of R-2R ladder by derivation for 2bits [21]

ratio coefficient	
m	1.788854382
k	2

2.1 Simulation

Monte Carlo simulation was conducted using Matlab® in order to confirm , that the findings from previous section can be extrapolated for multiple bit R2R ladder, Since finding a mathematical proof requires too complex derivation that is beyond the scope of this theses. In the simulation value of resistor R is calculated by (13,14). The mean was set to zero and standard deviation derived from (7) by neglecting the systematic part, which is dealt with separately. The standard deviation is than

$$\sigma_{Rx} = \frac{A_\rho}{R_{sheet}\sqrt{A_{Rx}}} \tag{28}$$

The coefficients k and m are independent from A_ρ, R_{sheet} and A_T, so the standard deviation was set to 0.1% for a resistor of area A_T.. The simulation was carried out for 5 million samples simulating 8bit R-2R DAC for ranges 1.7<m<1.86 and 2<k<2.5 with step sizes 0.01 and 0.1 for m and k respectively. Previous section focused on obtaining the area ratio coefficients through minimizing the variance, the simulation can easily estimate the parametric yield, as given by (9, 10). To calculate yield condition -0.5 < INL < 0.5 was set. Fig. 9 shows the simulation results and Fig. 10 shows another simulation runs comparing different bit numbers and values of m and k. The simulation confirms the value of m as derived, but suggest value of k to be 2.3 for higher bit counts. The results of previous study Tab. 1[12] are confirmed as well, although with a deviation of 0.09 and 0.1 for m and k respectively.

Tab. 3: Proposed area ratios of R-2R ladder by simulation for 8bits

ratio coefficient	
m	1.79
k	2.3

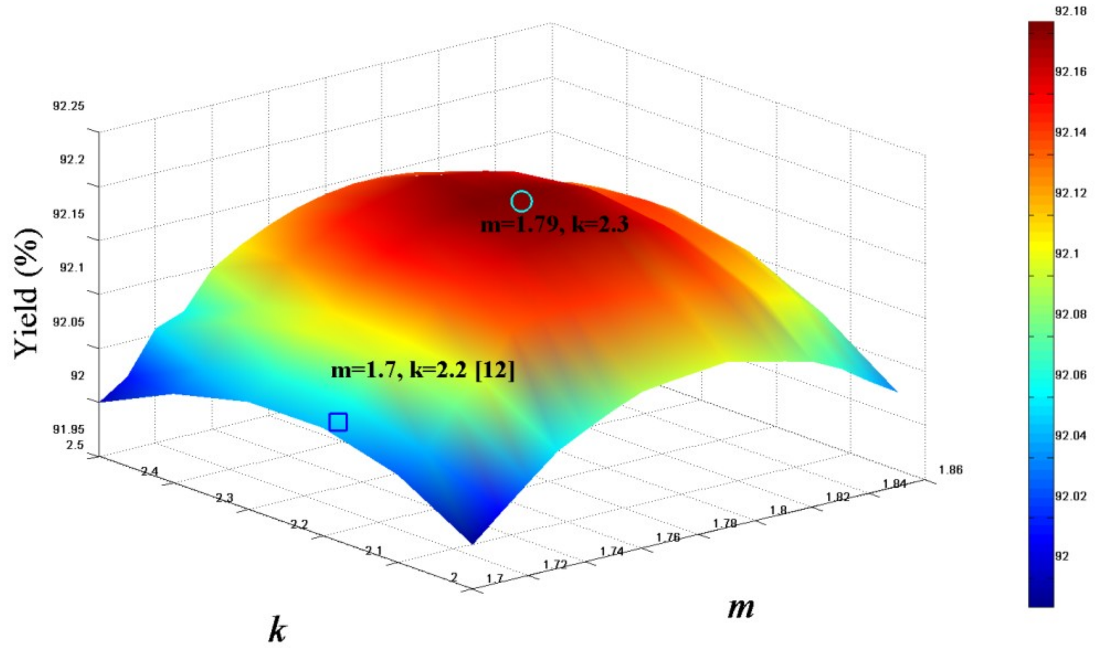

Fig. 9: Yield simulation for 8bit R-2R DAC

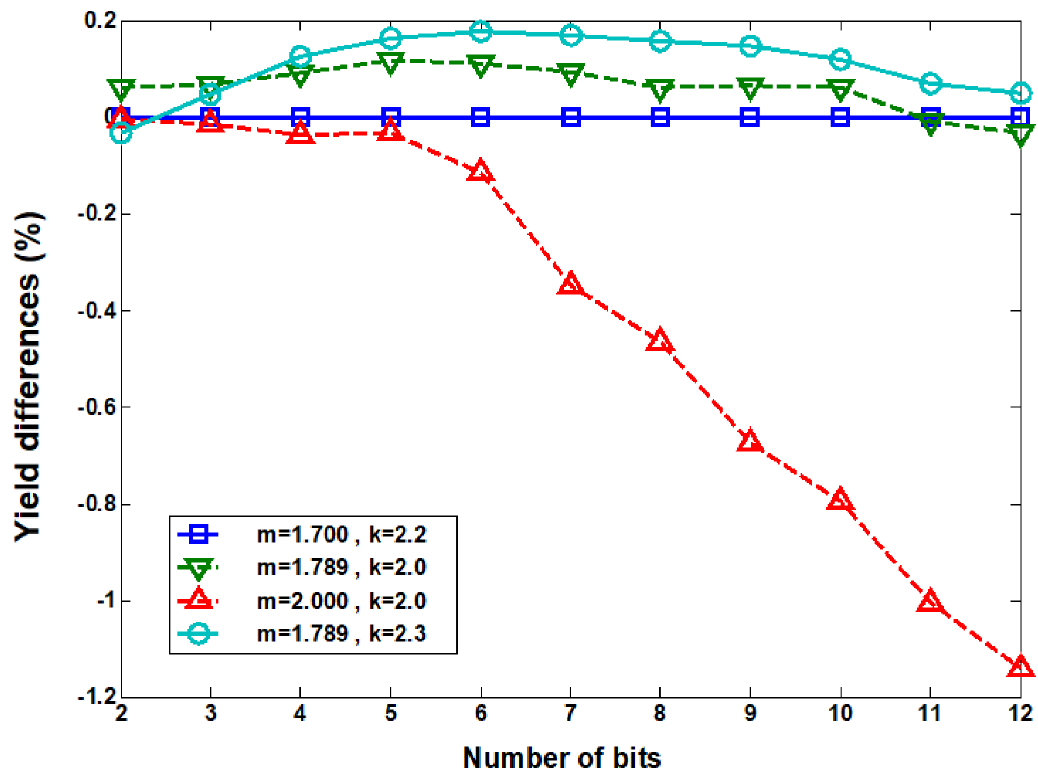

Fig. 10: Yield differences for multiple configurations of R-2R DAC [21]

3 Integer Programming

To get better understanding of the challenges of designing a R2R DAC with optimal layout strategy the optimization techniques are studied in this chapter. Mathematical optimization also known as mathematical programming is basically a method for selection of a best element from a set of alternatives with regard to some criteria.

Basic mathematical programming problem can be simplified to searching for minima of maxima of an objective function, such a solution of an objective function is called optimal solution. Finding the optimal solution under condition

$$f(x_{min}) \leq f(x) \tag{29}$$

or

$$f(x_{max}) \geq f(x) \tag{30}$$

can be done by first and second derivative of the functions

$$f'(x)=0 \wedge f''(x)>0 \tag{31}$$

$$f'(x)=0 \wedge f''(x)<0 \tag{32}$$

for obtaining a local minima and maxima respectively. This approach only works for continuous functions.

As the layout pattern has to be done as a matrix of finite number of devices, and the devices cannot be divided into partitions, it is not possible to find the optimal solution to the problem with derivative of a continuous function. The field studying optimization of integer problems is integer programming which is mostly missing in the curriculum of IC designers. Integer programming is usually covered in mathematics and computer science programs.

The integer problems can be divided into two groups: linear and non-linear. The linear integer programming problem is defined as:

$$\text{Maximize} \sum_{j=1}^{n} c_j x_j ,$$
$$\text{subject to} \begin{cases} \sum_{j=1}^{n} a_{ij} x_j = b_i , \quad (i=1,2,..,m), \\ x_j \geq 0, \quad (j=1,2,..,n), \\ x_j \in \mathbb{Z} \end{cases} \tag{33}$$

One of the ways to solve the ILP problem is graphical method. To illustrate the solution take the following example

$$\text{Maximize } f(x,y) = 6x + 5y,$$
$$\text{subject to} \begin{cases} x + 4y \leq 16 \\ 6x + 4y \leq 30 \\ 2x - 5y \leq 6 \\ y \geq 0 \\ x \geq 0 \\ x, y \in \mathbb{Z} \end{cases} \tag{34}$$

Plot the constraints in Fig. 11. Within the area enclosed by constraints is yellow marked area of feasible solutions. Black dots show feasible integer solutions. The point (2.8;3.3) is called relaxation point and is a boundary limit of integer solutions. If rounding to the closest integer feasible solution (2;3) the solution is close to optimum. To get optimal solution line of objective function is moved across the data set. The line of objective function displays the points with same functional value, thus in this case all points to the right side of the line give higher functional value.

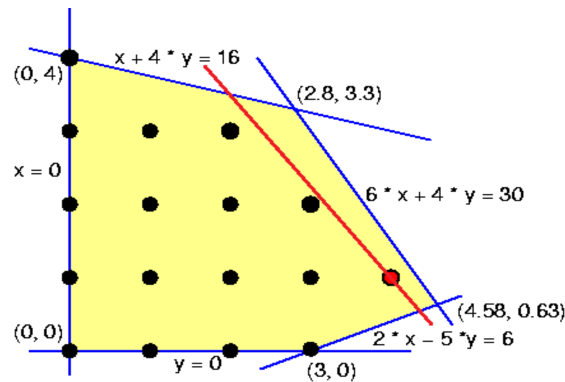

Fig. 11: Graphical solution to ILP problem [31]

These points are suspected to be the optimal solution. By shifting the line to right, the optimal integer solution is found, point (4;1) is identified as optimal solution to the problem (34). Another method that can be used for solving the problem is Simplex.[29]

Simplex method is well understood algorithm for solving linear programs with one significant drawback, which is that for integer linear programs an approximation by continuous variables is necessary and thus the obtained solution needs to be rounded to integer value, which may result in non-feasible or non-optimal solution as demonstrated in previous paragraph. The solution is only close to the relaxation point but is not guaranteed to be the optimal solution. This method is good for implementation in scripts. Details can be found in [30].

Non-linear integer programming problem is defined as:

$$\text{Maximize } f(x_1, x_2, \ldots, x_n),$$
$$\text{subject to} \begin{cases} g_1(x_1, x_2, \ldots, x_n) \leq b_1, \\ \vdots \\ g_n(x_1, x_2, \ldots, x_n) \leq b_n, \\ x_i \in \mathbb{Z}, b_i \in \mathbb{Z} \end{cases} \tag{35}$$

From which is clear that ILP is a special case of NLP. Non-linear integer programming is new research discipline and not well understood, thus problems and methods are still to be discovered and any review on the field would be out-dated rather

fast, although some methods providing with close to optimal solutions exists. Two mostly used methods for solving these problems are separation and linear approximation.

Separation basically means to split the objective function into several functions with only one variable and optimize them separately as linear problems. Than the solution is combined and considered close enough to optimum. Obviously the deviation from optimum solution can be significant, but there is no solid method available.

Linear approximation basically solves the problem as if it would be a linear integer programming problem as described above in this chapter.

Genetic algorithms are also used for solving NLP problems, but these still do not guarantee optimal solution.

4 Layout Strategies

In this chapter different layout approaches for large number of different ratio component matching will be discussed. It is very difficult to compare the layout strategies, because there is no clear metrics for their comparison. It is most dependent on the application, thus under certain application requirements certain layout strategy performs better. Some of the studied layouts proposed pseudo common centroid layout or no common centroid. Because the common centroid strategy proved itself as most reliable, only common centroid based strategies are studied. In order not to get biased idea of layout strategy very different layout strategies are presented. The aim of all presented strategies is to minimize impact of systematic mismatch.

4.1 Omran's Layout

Omran's layout strategy for matching the ratios of capacitors in the 9-bit programmable capacitor array (PCA) layout has been studied as first one. This work is particularly interesting for it's origin in Egypt and Saudi Arabia, which do not have strong research tradition. The authors are from Ain Shams University, Cairo and from King Abdullah University of Science and Technology, Thuwal which was established only in 2009. Although as shown later in chapter 6.2 the results of proposed layout pattern are not groundbreaking, it displays couple of interesting ideas to consider.

In [23], Omran's team shows a common centroid layout of capacitors with a routing channel for 9-bit PCA. To create the layout sub-devices are placed from the center starting from LSB to MSB devices. The sub-devices are placed in elliptical-like shape as shown in Fig. 12. However the exact algorithm for placing is not given in [23].

The design aims on ease of routing, so the sub-devices for each main device are located right next to each other. Because all the sub-devices are be connected in parallel, it is only necessary to connect the neighboring sub-devices. In order to minimize parasitic capacitance induced by routing to the LSB devices in the center, the layout is divided in half and a routing channel is inserted.

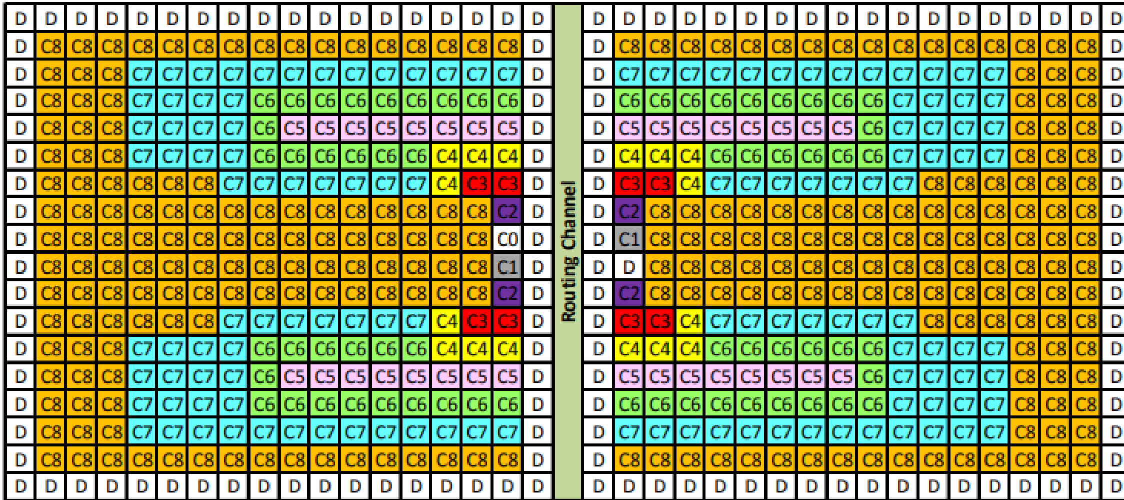

Fig. 12: Omran's 9-bit programmable capacitor array.[23] D – dummy, C0 – LSB capacitor sub-device, ..., C8 – MSB capacitor sub-devices

4.2 Borisov's Layout

This approach comes from Robert Bosch Center for Power Electronics, Reutlingen, Germany. Borisov's research group focuses on analog IC design automation. In the work [26] a common centroid pattern generating algorithm is provided. The algorithm builds on trial and error method with help of sophisticated shuffling. The shuffling is particularly interesting. As depicted in Fig. 13 the layout pattern is treated as a matrix. The shuffle algorithm first fills the matrix in rows. One row for one device as depicted in Fig. 13a. Next the created matrix is transposed as in Fig. 13b and odd columns are shifted to the left half and even columns are shifted to the right half. The odd rows on the left half are inverted so that the most left sub-device is swapped with the most right of that left half of the row, which is in

the middle of the whole row. This is repeated for the rest of the sub-devices of the half row. The even rows swap left and right half of the row and after that the newly located sub-devices in the left half are swapped the same way as for the odd rows. After swapping in Fig. 13c is completed, the matrix looks like in Fig. 13d. In case there is blank space, the full rows are moved to the center so that the blank space occurs on the boundaries.

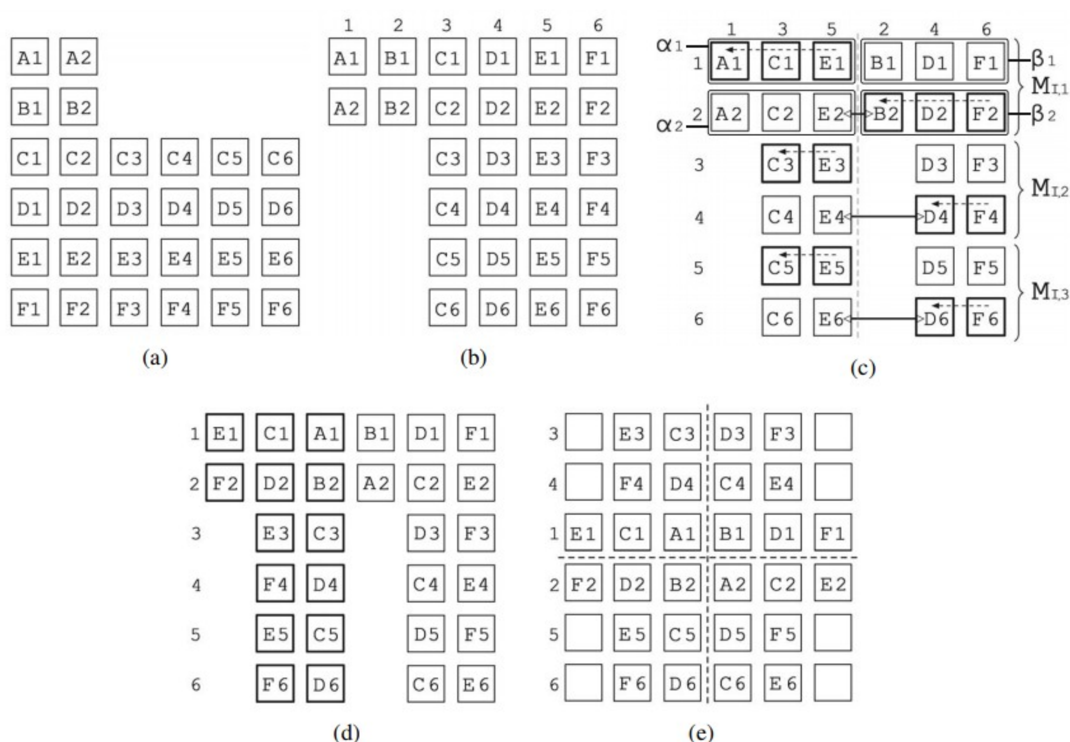

Fig. 13: Borisov's layout pattern generation [26]

Borisov's team than calculate a mismatch metric. Because solely with this approach the results are not optimal, iterative computation is suggested with randomly changing the input matrix Fig. 13a. To ease the computational burden they suggest to use a genetic algorithm to obtain a best possible result. From the presented layout variants it is obvious that this method is most difficult to compute, because of many iterations needed for the genetic algorithm to run. MATLAB® implementation is shown below:

```
l = length(res_list)
for i= 1:l
   layout(i,1:res_list(i)) = i;
end
```

```
layout_pom = transpose(layout);

%odd and even divide
layout = layout_pom(:,1);
for i=3:2:l
   layout = horzcat(layout, layout_pom(:,i) );
end
for i=2:2:l
   layout = horzcat(layout, layout_pom(:,i) );
end
%shuffle
w = length(layout);

for i=1:2:w
   layout(i,1:l/2) = fliplr(layout(i,1:l/2));
end
for i=2:2:w
```

4.3 Bastiaansen's Layout

This work is fairly old, from 1991. The research group comes from Philips Research Laboratories in Eindhoven, Netherlands. The paper [27] concerns 10-bit current steering DAC. The proposed layout strategy is shown for 6bit DAC example. First MSB sub-devices are placed in chessboard like pattern, because the number of MSB sub-devices is largest. Basically a sub-device is placed in every 2nd empty position in the matrix. For MSB+1 sub-devices also every 2nd empty position is filled. For MSB+2 every 2nd empty position in perpendicular direction is filled to achieve close to common centroid layout pattern. The rest of the bits is placed in similar way. Fig. 14a shows chessboard like placement of MSB sub-devices. Fig. 14b shows placement of MSB+1 sub-devices, Fig. 14c shows whole layout pattern of the DAC.

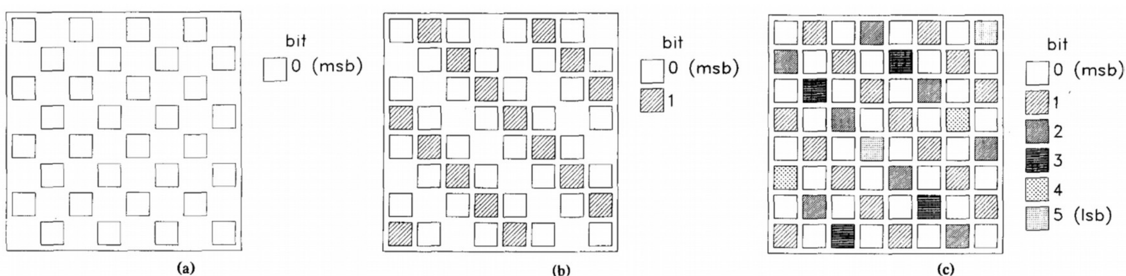

Fig. 14: Chessboard-like Bastiaansen's layout [27]

This layout strategy is easy to be implemented in a script for an automatic layout generation, however is complicated to implement for different ratio devices, which cannot fit the ratio of 2.

4.4 Interleaved Two Arm Spiral Layout

This layout strategy has been designed specially for the purpose of this work. From the previous layout strategies it was not possible to implement an efficient algorithm to generate a layout pattern for large number of matched devices with a ratio different from 1 or 2.

To conquer this problem a layout strategy, which is suitable for matching large number of devices with any matching ratio, has been devised. The algorithm aims to retain common centroid and low compute cost. First of all it is necessary to specify the number of sub-devices for each device. Than a list of devices is made and the devices are sorted from the smallest to the largest number of sub-devices. Placement algorithm places devices from this list. Placement starts from the center, so it is necessary to pick a center coordinate first. Sub-device of the smallest device is placed at the center. Than two sub-devices of the largest device are placed diagonally from the center as shown in Fig. 15a. Next two sub-devices of the smallest device are placed above and under the center position as in Fig. 15b. In a subsequent step two sub-devices of the largest device are placed in diagonal position again as shown in Fig. 15c.
Afterwards, two sub-devices of the smallest device are placed. In case that all sub-devices of the particular device are placed the role of the smallest or the largest device is passed to 2nd smallest or 2nd largest device and so on until all sub-devices are placed. If there is no free position in the square for placing the next sub-devices, the square is enlarged as shown in Fig. 15e. The algorithm interleaves large and small devices and places corresponding sub-devices in square two arm spiral, thus the algorithm is called interleaved two arm spiral. The spiral placement enables

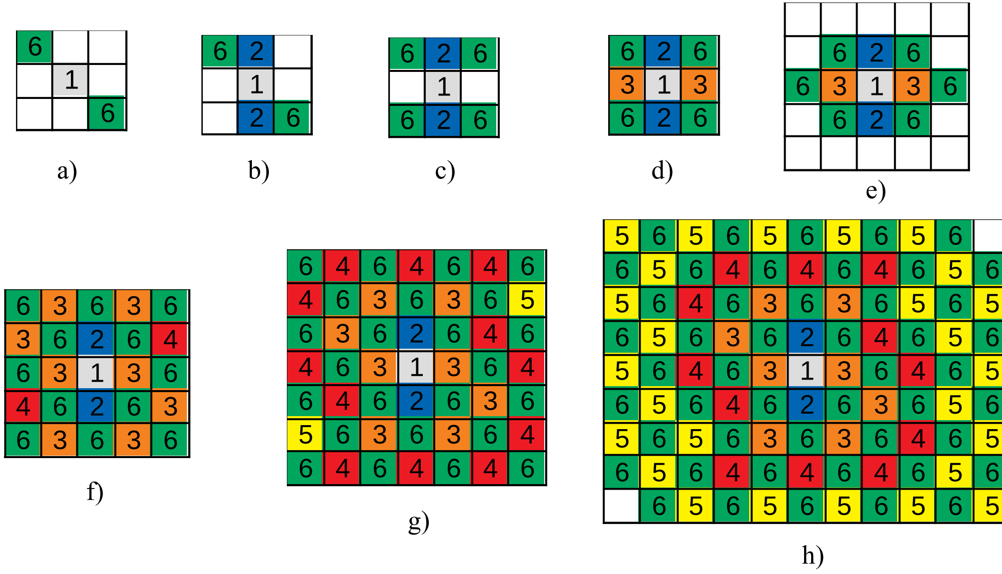

Fig. 15: Pattern generation; a to e step by step placing of the sub-devices, f to h illustrate more steps

the algorithm to easily scale up to large patterns while possessing good 1st and 2nd order gradient resistance. The performance of this algorithm could be increased by using more sub-devices per device and by enhancing the interleaving algorithm, so that the sub-devices are distributed more evenly, but this enhancement comes with a cost of high routing difficulty. The algorithm implementation in MATLAB® is listed in appendix section of this work. The original scheme is subject to difficult routing, but the sub-devices of one device are kept in circle-like formation, so the routing is restricted to ring like areas. The proper design of routing is left for future work and ILP could be used in order to find optimal routing. Fig. 16 shows possible routing around center of the layout pattern.

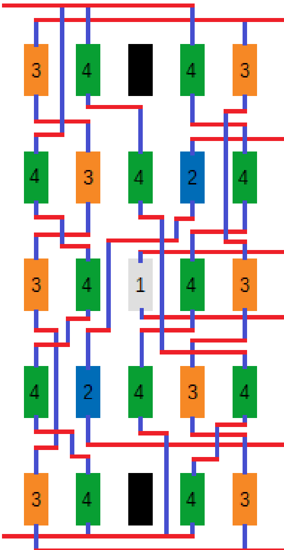

Fig. 16: Example of routing

5 Design of R2R DAC

In this chapter the implementation of R2R DAC is covered. The very basic architecture of binary weighted DAC with R-2R ladder network is used. An 8bit DAC is proposed in order to be suitable for comparison with the simulation conducted in [12] and [21]. Diagram of all components is shown in Fig. 17.

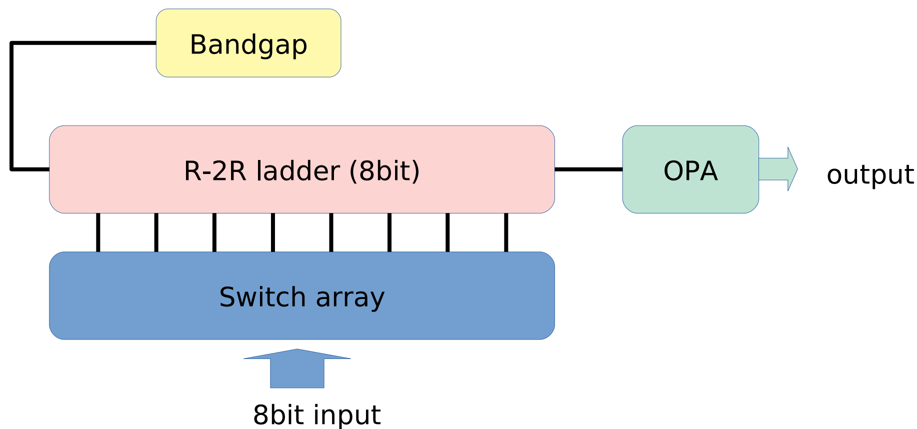

Fig. 17: DAC flow chart

5.1 Components

The design uses bandgap voltage reference, OPA, Switch Transfer Gate and R2R ladder. As the main focus of this work is on the R2R area allocation, attention is paid on the choice of resistors. More can be found in [25].

Resistors used are chosen to be high-poly, because of highest sheet resistance and lowest resistance variation with respect to total resistance of the device.

Circuits of the components can be found in appendix section.

5.2 Area allocation strategy

The area allocation strategy for critical resistors of the R-2R ladder is based on the simulated values. The values of the coefficients *m* and *k* are given in Tab. 3. The parameters of unit resistor sub-device are given in Tab. 4.

Tab. 4: Unit resistor parameters

sheet resistance (ohm/μm²)	1050
W (μm)	1
L (μm)	2
unitR (ohm)	2100

Based on the ratios *m* and *k* resistor networks for each R_n and $2R_n$, that would fulfill the following conditions, were tried to be found:

- *Area of each R_n and $2R_n$ has to follow the bit-to-bit area ratio m and inner bit ratio k.*

$$\frac{R_n+2R_n}{R_{n-1}+2R_{n-1}}=m, \qquad \frac{R_n}{2R_n}=k \tag{36}$$

- *Resistance of all R_n networks has to be R. Resistance of all $2R_n$ networks has to be 2R.*
- *Resistor network must be made of integer number of unit resistors.*

This is non-linear integer programming problem. Because solving it for 8bits is nearly impossible, it has been decided to find near optimum solution by linear approximation and rounding the relaxation solution to a feasible solution.

Considering simple resistor networks with single branching, the network resistance is given by

$$R_{network}=\frac{S}{P}\cdot R_{unit} \tag{37}$$

where *S* is number of resistors in series and *P* is number of parallel branches.

From (37) is found, that for all networks where *S* equals *P* the networks have equal total resistance the same as the unit resistor. Square resistor networks with number of parallel branches equal to number of series of resistors in the branch

are found as the trivial linear solution. Feasible solutions for areas of R_n and $2R_n$ are obtained from those networks.

The linear integer program to find close to optimal solution can be described as

$$\begin{aligned} &\text{Minimize} \sum_{i=1}^{n} (\Delta m_i + \Delta k_i) \\ &\text{where} \begin{array}{l} \Delta m_i = m_o - (a_i / a_{(i-1)}) \\ \Delta k_i = k_o - (b_{R(i)} / b_{2R(i)}) \end{array} \\ &\text{subject to} \left\{ \begin{array}{c} \sum_{i=1}^{n} (a_i) \leq a_{max} \\ a_i \in A_{bit}, b_{R(i)} \in B_{innerbit}, b_{2R(i)} \in B_{innerbit} \end{array} \right\} \end{aligned} \tag{38}$$

Where a_i is area of bit i. $b_{R(i)}$ is area of inner bit R_n and $b_{2R(i)}$ is area of inner bit $2R_n$, A_{bit} and $B_{innerbit}$ are sets of feasible solutions to R_n and $2R_n$ resistor networks. Because the objective function would not guarantee exceptional INL as required, it was adjusted by treating Δm and Δk as logic functions.

$$\begin{aligned} &\text{Minimize} \sum_{i=1}^{n} (\Delta M_i + \Delta K_i) \\ &\text{where} \begin{array}{l} \Delta M_i = \text{if} (|\Delta m_i| > 0.1) \text{ than } 1 \text{ else } 0 \\ \Delta K_i = \text{if} (|\Delta k_i| > 0.1) \text{ than } 1 \text{ else } 0 \end{array} \end{aligned} \tag{39}$$

Fig. 18 shows the objective function of 8bit R-2R ladder. The minima of the objective function is at MSB's *2R* area of 3136um^2, thus the bit areas are derived as shown in Tab. 5.

The derived set of resistor networks is than used as input to the interleaved two arm spiral algorithm, which creates the final layout pattern of the 8bit R-2R ladder.

The routing proved to be very challenging problem, which remains to be solved properly. The CADENCE® software tools provide some degree of auto-routing, which was used, but the resulting routing is not optimal.

Tab. 5: 8bit area allocation

R (ohm)	2100	2100	2100	2100	2100	2100	2100	2100
series	3	5	6	8	11	15	20	26
parallel	3	5	6	8	11	15	20	26
no. of unitR	9	25	36	64	121	225	400	676
area with unitR	18	50	72	128	242	450	800	1352
2R (ohm)	4200	4200	4200	4200	4200	4200	4200	4200
series	8	10	14	18	24	32	42	56
parallel	4	5	7	9	12	16	21	28
no. of unitR	32	50	98	162	288	512	882	1568
area with unitR	64	100	196	324	576	1024	1764	3136
k_i	**3.56**	**2.00**	**2.72**	**2.53**	**2.38**	**2.28**	**2.21**	**2.32**
Δk	-1.26	0.30	-0.42	-0.23	-0.08	0.02	0.09	-0.02
m_i	**1.83**	**1.79**	**1.69**	**1.81**	**1.80**	**1.74**	**1.75**	**0.00**
Δm	-0.04	0.00	0.10	-0.02	-0.01	0.05	0.04	

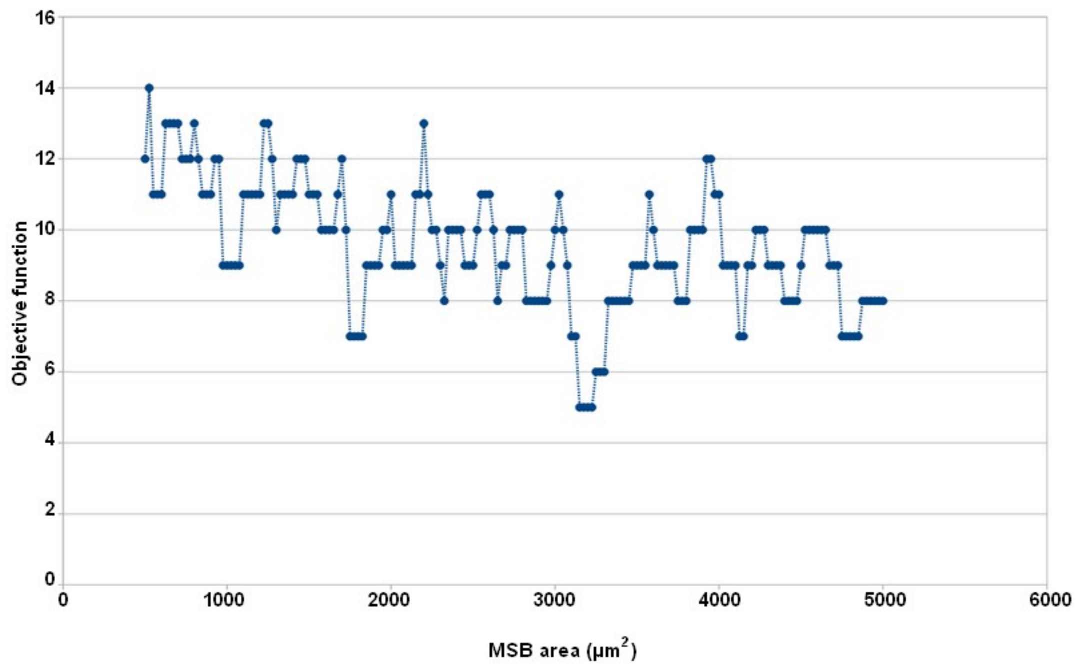

Fig. 18: Objective function of area allocation

Based on simulation results shown in Fig. 10, using coefficients k and m, 2.3 and 1.789, a 0.7% improvement in yield is estimated for 8bit R2R DAC in comparison to using value of 2 for both.

For comparison a second device is designed based on [12], resistor ratios are given in Tab. 6

Tab. 6: Resistor ratios of a simple R2R DAC [12]

R (ohm)								
series	3	2	1	1	1	1	1	1
parallel	3	2	1	1	1	1	1	1
no. of unitR	9	4	1	1	1	1	1	1
2R (ohm)								
series	6	4	2	2	2	2	2	2
parallel	3	2	1	1	1	1	1	1
no. of unitR	18	8	2	2	2	2	2	2

6 Layout Evaluation

This chapter concerns the evaluation of proposed layouts by simulation.

6.1 Evaluation Methodology

In order to evaluate the layout patterns, a pattern to match 6 different ratio devices has been made. Tab. 7 shows number of sub-devices for each device. The number of sub-devices is chosen to give different ratios between each matched device. In order to maintain the layout symmetrical the number of sub-devices is

Tab. 7: Count of different ration matched sub-devices

device	count
0	dummy
1	1
2	2
3	8
4	12
5	28
6	48

rounded to an even number.

To determinate the quality of each single pattern, gradient error up to 5th order in eight orthogonal directions has been calculated, the worst case direction was than taken as a result for the layout pattern.

The calculation is done by Vančura's Parameter Gradient Modeling method [25], which provides an excellent tool to compare multiple layout patterns between each other. It is important to remember, that the obtained results can only be used to compare the robustness of tested layout patterns between each other, it does not provide information on device mismatch in any particular technology.

The model describes the parameter value by a two-dimensional function:

$$p_n(x,y)=a\sum_{i=1}^{n}\sum_{j=0}^{i}x^j y^{(i-j)}+C \qquad (40)$$

where p_n is the parameter value for n-th order gradient, a is a gradient coefficient, C represents a nominal value of a device and n is the number of gradient. Using this method the gradients within the sub-device are neglected, thus this method might not be used for sub-devices with considerable gradient within themselves. In order to get the total device parameter value a simple sum can be of help:

$$P=\sum_{i=1}^{m} p_n(x_i, y_i) \tag{41}$$

For different ratio devices, more preferable is to normalize the parameter value to a single sub-device, thus the parameter value of the sub-device is

$$P_{sd}=\frac{1}{m}\sum_{i=1}^{m} p_n(x_i, y_i) \tag{42}$$

In order to compare parameter values of the devices, systematic mismatch is calculated as a variance of the normalized parameter value. The systematic mismatch is calculated in eight orthogonal directions and the worst case direction is taken as a result. For multiple device matching comparison of only single value instead of several mismatch values for each combination of devices is desired. Because of that the evaluation vector is introduced.[25]

The worst case systematic mismatch for n gradients is assembled into a vector $\vec{M}_i=[m_1,\ldots,m_5]$ for i-th device. Some devices might have different weight in the circuit, so mismatch vector is weighted by weight W_i

$$\vec{M}_{wi}=\frac{\vec{M}_i}{W_i} \tag{43}$$

$$\vec{EV}=\frac{\sum_{i=1}^{n}\vec{M}_{wi}}{dim(\vec{W})} \tag{44}$$

Finally the evaluation vector $\vec{EV}$ is obtained by sum of all systematic mismatch values for each order of gradient and divided by number of weights, more precisely number of matched devices. The evaluation vector is set of five numbers showing

the overall weighted systematic mismatch for particular layout pattern. With the evaluation vector is easy to compare layout patterns for matching devices. It also gives rough idea of how well a layout pattern cancels 1st to 5th order gradients.

6.2 Layout Pattern Comparison

This work introduced possible layout patterns in chapter 4, in order to decide, which one is best suitable for matching different ratio devices. A set of test devices has been made as shown in Tab. 7. Algorithms used for creating this layout pattern are those presented in chapter 3. Fig. 19 ÷ Fig. 22 show the graphical depiction of the evaluated patterns.

0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	6	6	6	6	6	0	0	6	6	6	6	6	0
0	6	5	5	5	5	0	0	5	5	5	5	6	0
0	6	5	4	4	4	0	0	4	4	4	5	6	0
0	6	5	5	3	3	0	0	3	3	5	5	6	0
0	6	6	6	6	1	0	0	2	6	6	6	6	0
0	6	6	6	6	2	0	0	0	6	6	6	6	0
0	6	5	5	3	3	0	0	3	3	5	5	6	0
0	6	5	4	4	4	0	0	4	4	4	5	6	0
0	6	5	5	5	5	0	0	5	5	5	5	6	0
0	6	6	6	6	6	0	0	6	6	6	6	6	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fig. 19: Omran's evaluation layout pattern

0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	5	6	6	5	0	0	0	0	0
0	6	6	6	6	6	6	6	6	6	6	6	6	0
0	6	6	6	6	6	5	5	6	6	6	6	6	0
0	5	5	5	5	5	3	4	5	5	5	5	5	0
0	3	4	3	4	3	1	2	4	0	4	0	4	0
0	4	3	4	3	4	2	0	3	4	0	4	0	0
0	5	5	5	5	5	4	3	5	5	5	5	5	0
0	6	6	6	6	6	5	5	6	6	6	6	6	0
0	6	6	6	6	6	6	6	6	6	6	6	6	0
0	0	0	0	0	5	6	6	5	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fig. 20: Borisov's evaluation layout pattern

0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	5	5	6	4	6	5	6	3	6	5	6	0	0
0	4	6	5	6	2	6	5	6	4	6	5	0	0
0	6	3	6	5	6	4	6	5	6	3	6	0	0
0	5	6	4	6	5	6	5	6	5	6	4	0	0
0	6	5	6	3	6	5	6	4	6	5	6	0	0
0	4	6	5	6	4	6	5	6	3	6	5	0	0
0	6	3	6	5	6	1	6	5	6	4	6	0	0
0	5	6	4	6	5	6	4	6	5	6	3	0	0
0	6	5	6	3	6	5	6	2	6	5	5	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fig. 21: Bastiaansen's evaluation layout pattern

0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	5	0	0	0	0	0	0	0	0	0	0	0	0
0	5	6	5	6	5	6	5	6	5	6	0	0	0
0	6	5	6	4	6	4	6	4	6	5	6	0	0
0	5	6	4	6	3	6	3	6	5	6	5	0	0
0	6	5	6	3	6	2	6	4	6	5	6	0	0
0	5	6	4	6	3	1	3	6	4	6	5	0	0
0	6	5	6	4	6	2	6	3	6	5	6	0	0
0	5	6	5	6	3	6	3	6	4	6	5	0	0
0	6	5	6	4	6	4	6	4	6	5	6	0	0
0	0	6	5	6	5	6	5	6	5	6	5	0	0
0	0	0	0	0	0	0	0	0	0	0	5	0	0

Fig. 22: Kostal's Interleaved Two Arm Spiral evaluation layout pattern

Tab. 8 shows evaluation vectors of test layout patterns

Tab. 8: Comparison of evaluation layout patterns

Layout pattern	Evaluation Vector (%)				
	1st	2nd	3rd	4th	5th
Omran	0.1649	3.7382	32.1355	81.2904	110.9751
Borisov	0.0988	2.5378	22.5967	58.5079	84.3872
Bastiaansen	0.1770	3.9750	33.4805	82.7735	112.5498
Kostal	0.0000	0.9099	11.5935	34.6801	54.4091

The proposed interleaved two arm spiral layout strategy exhibits the best gradient mismatch cancellation.

7 Results

The layout of the binary-weighted R2R DAC was realized as proposed in chapter 5. Also designs according to [12] were realized. TSMC 180 nm process was used although the designs were not manufactured. To evaluate the layouts, post layout Monte Carlo simulation for 500 samples was conducted. Fig. 23 shows obtained INL from the simulation, for convenience only first 20 traces are shown.

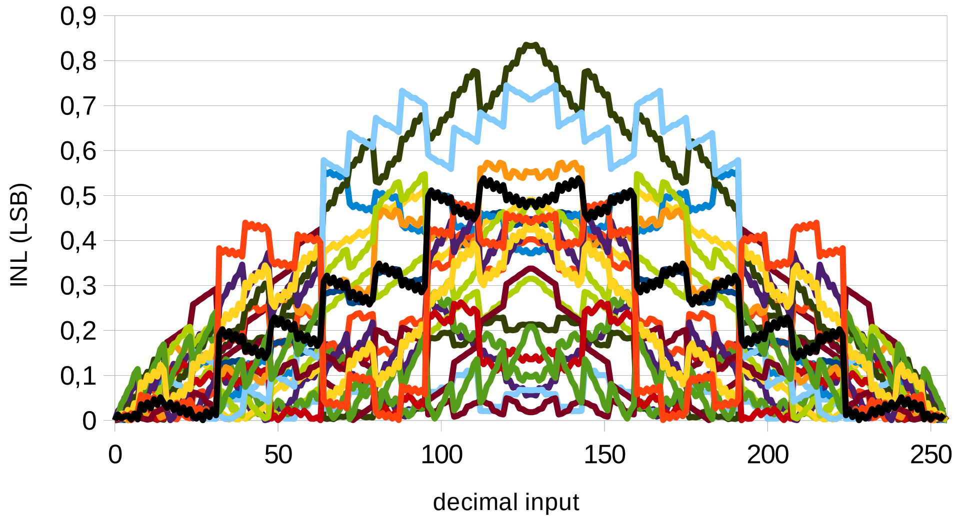

Fig. 23: Simulated INL, R2R DAC with applied interleaved two arm spiral and impact based area allocation strategies

Tab. 9 shows the obtained INL mean and standard deviation and estimated yield. The Optimal column shows the theoretically achievable result as found in [12] but due to integer nature of the problem is unreachable. The Geiger gives results for proposed area allocation strategy by Geiger [12] . The last one shows results of this work.

Tab. 9: INL and yield comparison

	Optimal	Geiger [12]	This work
INL_{μ} (LSB)	0.260	0.298	0.297
INL_{σ} (LSB)	0.124	0.145	0.143
Yield (%)	97.4	90.8	91.1

The results show strong correlation with simulation in chapter 2.1 with only 1.2 % and 0.9 % difference. In order to further increase yield, the area of MSB and thus

of the whole chip would need to be increased.

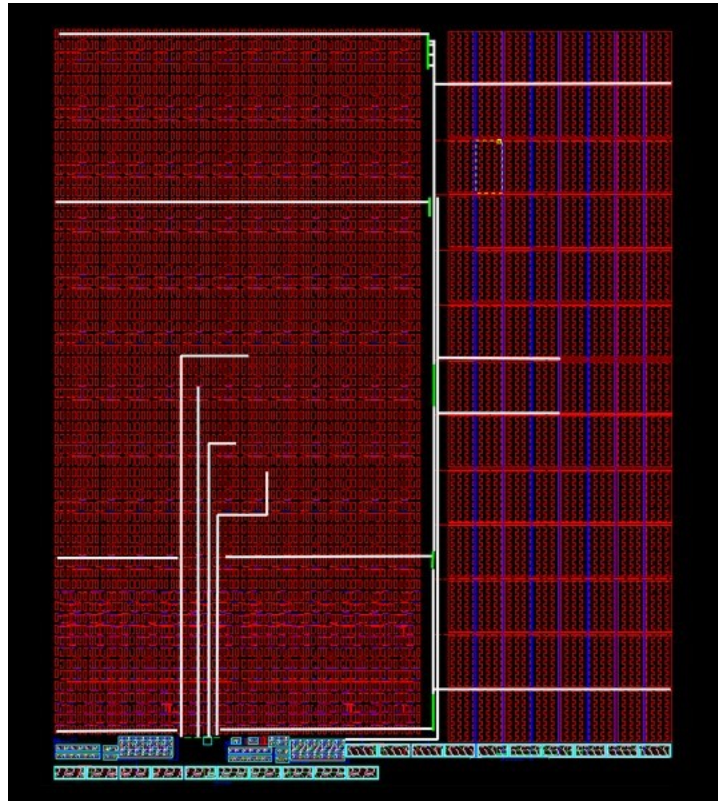

Fig. 24: Layout of the two R2R DAC designs

Fig. 24 shows the layout, on the left side R2R DAC with proposed area allocation strategy, on the right side R2R DAC with allocation suggested in [12].

8 Conclusion

At first this work shows a model of random mismatch cancellation based on log-normal PDF for R2R ladder circuit with estimated INL based yield improvements. Later, It suggested a new methodology to analog IC optimization based on mathematical programming. Today its application is limited only to comparatively simple problems, however it is expected that it will be adopted for more complex analog ICs once more breakthroughs are done in this relatively new field.

With help of this methodology a more complicated area allocation strategy for yield enhancement of R-2R DAC was developed, with 0.7 % improvement in yield compared to previous proposal made in [21] and 0.2 % improvement compared to [12].

New Interleaved Two Arm Spiral layout pattern generator algorithm was created to fulfill the need for good systematic mismatch cancellation in circuits with many critically matched devices of arbitrary matching ratio. The presented layout pattern reduces 1st order gradient mismatch to 0, 2nd order of gradient by order of magnitude and higher order gradient mismatch by tens of percent in comparison to known common centroid layout patterns for matched devices of arbitrary ratio. Further improvement in yield is expected from implementation of a proper routing instead of auto-routing.

Finally results and comparison of post-layout simulation is given in a form of INL mean and standard deviation together with yield estimates. The proposed layout pattern exhibits yield better by 0.3 %.

Further research efforts should be expended on routing the resistor networks with use of integer programming. Also application of these layout strategies to other analog circuits can be discovered.

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Appendix

Matlab code for generating interleaved two arm spiral layout pattern

```
%edit dev_list to your desired number of subdevices
dev_list = [9 25 36 64 121 225 400 676 32 50 98 162 288 512 882 1568];
ls = ceil(sqrt(sum(dev_list))); %size
lc = [floor(ls/2+1) floor(ls/2+1)]; %centre
x1 = lc(1)
y1 = lc(2)+1
x2 = lc(1)
y2 = lc(2)-1
l = length(dev_list);
s = 1;%start of the array, it changes once beggining gets placed and
array filled with zeros
```

```
e = 0;%which end of array is being placed 0 for start, 1 for end
direction = 1; %1 - vertical


%origin

layout(lc(1),lc(2)) = 1;
dev_list(1) = dev_list(1)-1;
i=1;
e=1;
if res_list(1)== 0
   s=2;
end

%loop
for a=1:1:sum(dev_list)

%place

if res_list(i)== 0 && e == 1
   i = i-1;
   l=i;
end
if res_list(i)== 0 && e == 0
   i = i+1;
   s=i;
end
layout(x1,y1) = i;
res_list(i) = res_list(i)-1;
if sum(dev_list)==0
    return
end

if res_list(i)== 0 && e == 1
   i = i-1;
   l=i;
end
if res_list(i)== 0 && e == 0
   i = i+1;
   s=i;
end
layout(x2,y2) = i;
res_list(i) = res_list(i)-1;
if sum(dev_list)==0
    return
end

if e == 1
    e=0;
    i=s;
else
    e=1;
    i=l;
end

%new cursor position
%decide change direction
%move in direction or move to new circle
```

```
if direction == 1
   if layout(x1,y1-1) == 0
       direction = 2
   end
elseif direction == 2
    if layout(x1-1,y1) == 0
       direction = 3
   end
elseif direction == 3
    if layout(x1,y1+1) == 0
       direction = 0
   end
elseif direction == 0
    if layout(x1+1,y1) == 0
       direction = 1
   end

end

if direction == 1
    x1 = x1+1
    x2 = x2-1
elseif direction == 2
    y1 = y1-1
    y2 = y2+1
elseif direction == 3
    x1 = x1-1
    x2 = x2+1
elseif direction == 0
    y1 = y1+1
    y2 = y2-1
end


end

numberOfNonZeros = nnz(layout==4);
```

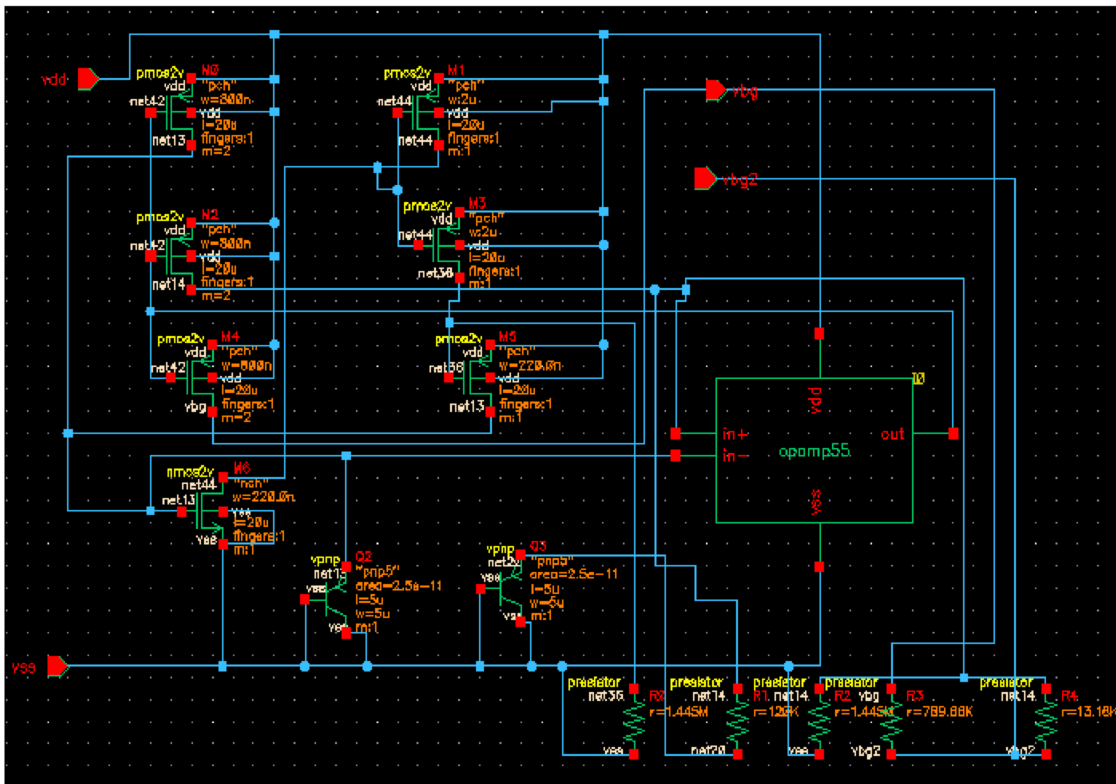

Fig. 25: Bandgap reference

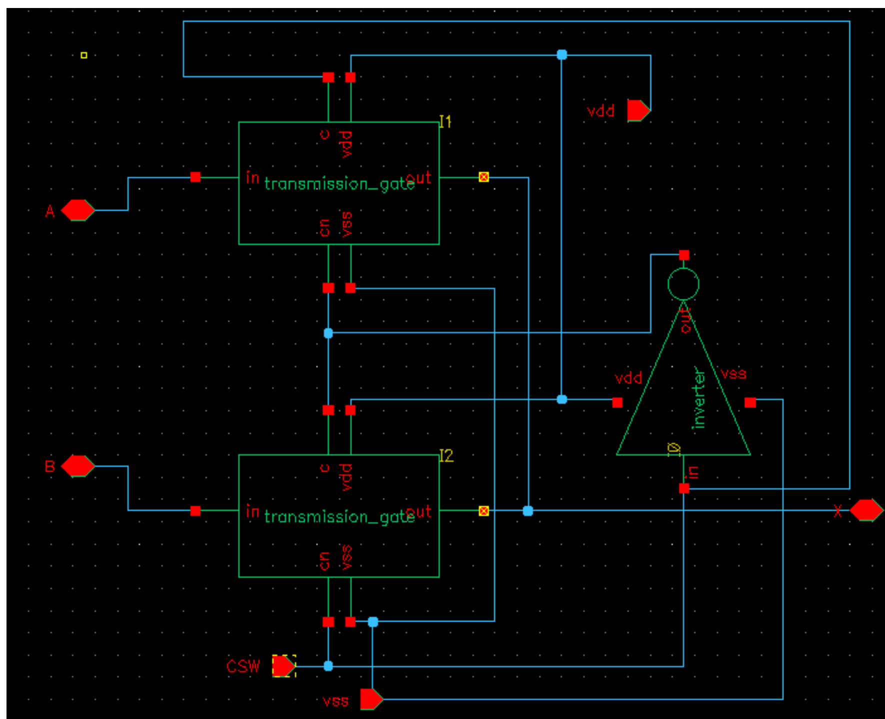

Fig. 26: Integrated switch

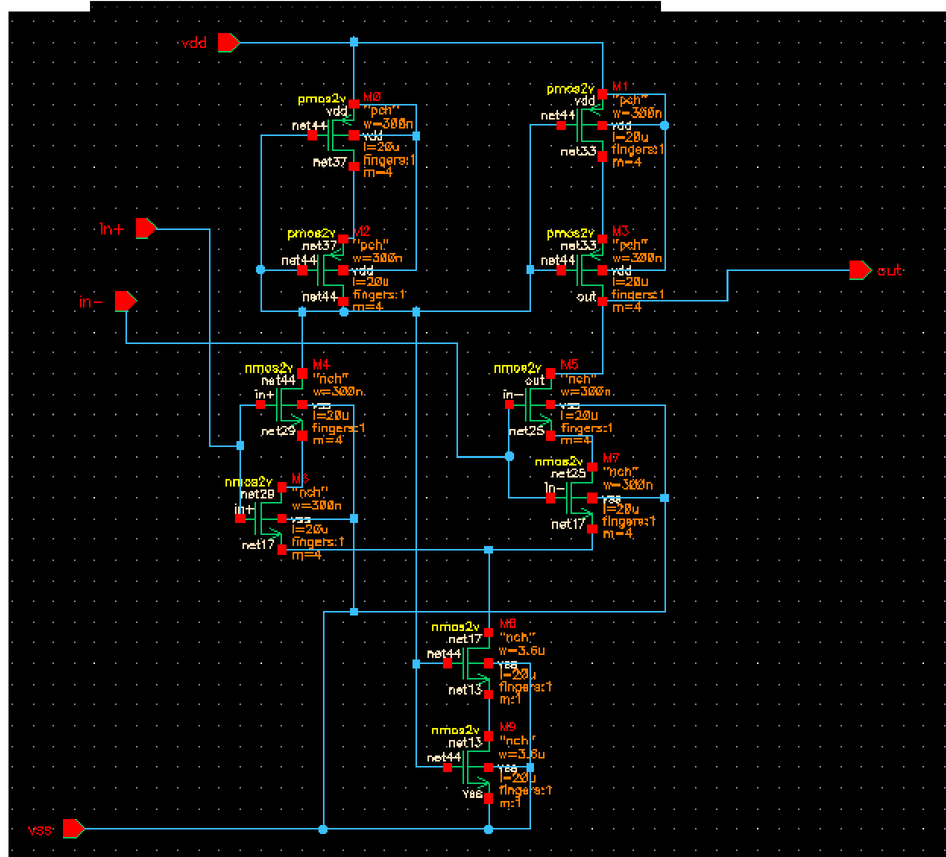

Fig. 27: OPA

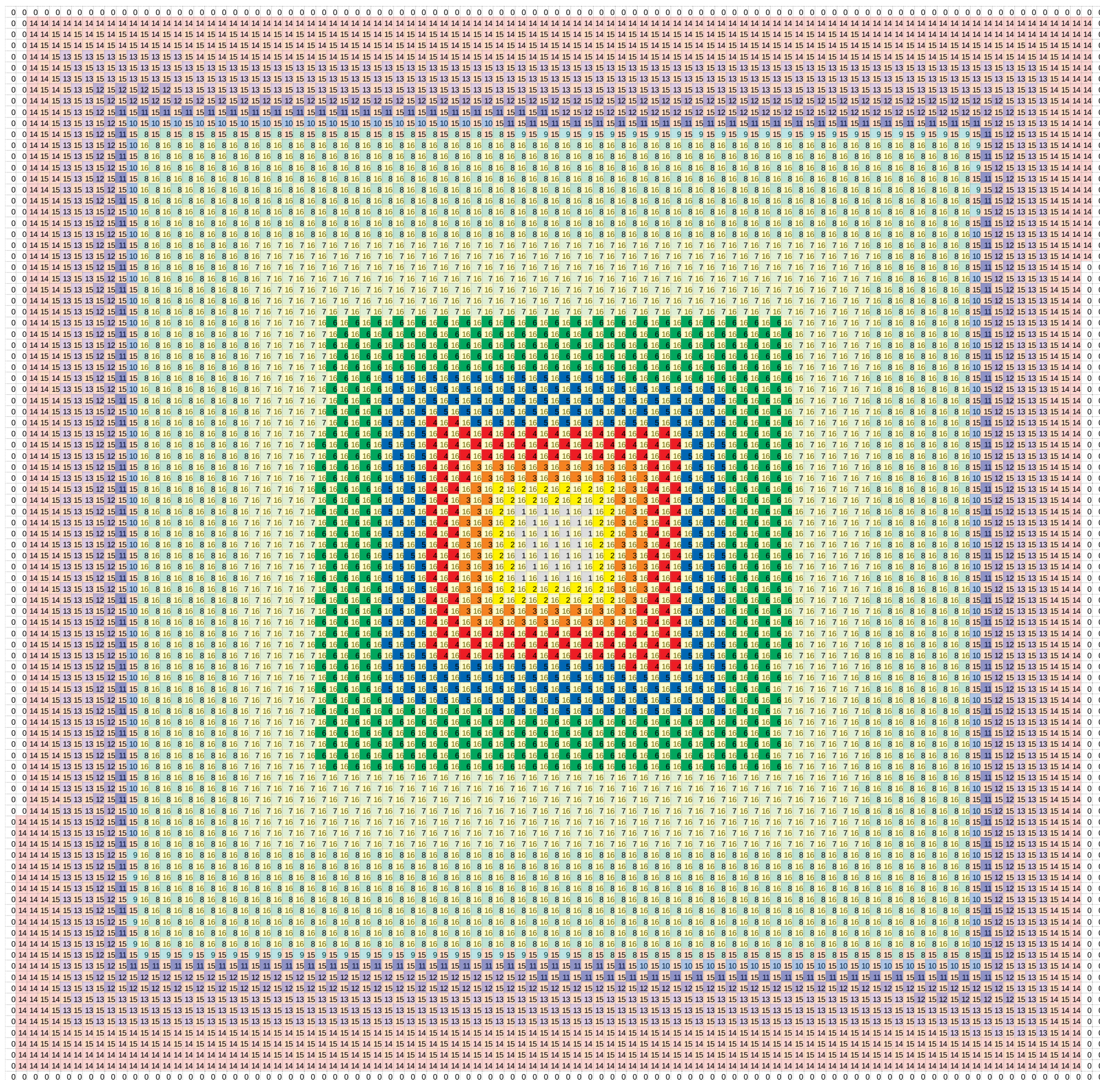

Fig. 28: Proposed layout pattern of 8bit R-2R DAC