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Design of a RF Communication Receiver Front-End for Ultra-Low Power and Voltage Applications in a FDSOI 28nm Technology

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Abstract

The advances in the semiconductor and wireless industry have enabled the expansion of new paradigms, which have given rise to concepts like Internet of Things (IoT). Apart from qualities like size, speed or cost, the ever-increasing demand for autonomy focuses all design efforts in the minimization of power consumption. Scaling technologies and the request to reduce power consumption have pushed designers towards lower supply voltages. Despite the fact that technology scalability allows for faster transistors, radio-frequency (RF) integrated circuit (IC) design accuses the reduction of the voltage supply through frequency response degradation, which significantly deteriorates the overall performance. Analog and RF circuits in high-end applications require substantial gate voltage overdrive to maintain device speed, which further complicates the design due to the reduction of voltage headroom. As a consequence, the necessity to develop circuit topologies capable to deal with low-power and low-voltage stringent constraints well suited to applications requiring long battery life and low cost emerges. This work aims to implement a low-noise amplifier and mixer stages of a radio-frequency receiver front-end working under an ultra-low power ($< 100\,\mu W$) and ultra-low voltage ($< 0.8\,V$) scenario while targeting decent overall performance. To cope with the stringent power requirements, 28nm FD-SOI technology will be used to take maximum profit of aggressive forward body bias and enhance transistor performance.

Preface

First, I would like to express my deepest gratitude to my thesis supervisors, Xavi and Diego, who have patiently guided the development of this work providing advice when needed. I would also like to thank all professors I have been given the opportunity to share class with, from whom I have learnt more things than I can remember.

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List of Abbreviations

Abbreviations

IoT	Internet of Things
WSN	Wireless Sensor Network
RF	Radio-Frequency
IC	Integrated Circuit
TEG	Thermoelectric Generator
MFC	Microbial Fuel Cells
PVC	Photo Voltaic Cells
PEH	Piezo-Electric Harvesters
ULP	Ultra-Low Power
ULV	Ultra-Low Voltage
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
NMOS	Negative-channel Metal-Oxide Semiconductor
PMOS	Positive-channel Metal-Oxide Semiconductor
DIBL	Drain-Induced Barrier Lowering
UTBB	Ultra-Thin Body and Buried
FD-SOI	Fully-Depleted Silicon-On-Insulator
FinFet	Fin Field-effect transistor
LNA	Low Noise Amplifier
LO	Local Oscillator
ADC	Analog-to-Digital Converter
IF	Intermediate Frequency
BER	Bit-Error Rate
NF	Noise Figure
IP3	Third-order Intercept Point
IIP3	Third-order Input Intercept Point
OIP3	Third-order Output Intercept Point

LVT	Low Threshold Voltage
RVT	Regular Threshold Voltage
FBB	Forward Body Bias
RBB	Reverse Body Bias
PDK	Process Design Kit
FoM	Figure of Merit
IO	Input-Output
DC	Direct Current
AC	Alternating Current
CAD	Computer Aided Design
PCB	Printed Circuit Board
TQFP	Thin Quad Flat Package
SPICE	Simulation Program with Integrated Circuits Emphasis
FFT	Fast Fourier Transform
IFFT	Inverse Fast Fourier Transform
PAC	Periodic AC Analysis
PXF	Periodic Transfer Function Analysis
PSS	Periodic Steady State Analysis
Pnoise	Periodic Noise Analysis
SNR	Signal-to-Noise Ratio

Chapter 1

Introduction

More than 50 years later, society is conceiving the impact of Moore's prediction in many different ways. The uninterrupted race towards a technological-based civilization has evoked the expansion of new paradigms, which have given rise to concepts like Internet of Things (IoT).

The term IoT addresses the idea of building novel type of interactions among network-connected objects and humans, enabling the realization of smart cities, infrastructures, and services to enhance the quality of life and utilization of resources. As its name suggests, the two pillars of IoT are "Internet" and Things". A "thing" is not limited to an object capable of connecting to the Internet, but it encloses a more generic set of entities with the ability to generate, exchange and consume data over a network, making it accessible without any time or place restrictions [1]. Each of these devices is allowed to work as an intelligent node.

Within the IoT context, devices do not need to be extremely complex systems such as smartphones or computers. In fact, most IoT nodes are small and inexpensive electronic circuits that implement some sensing functionality, perform a basic signal processing, and wirelessly transmit the information to some nearby gateway or concentrator. In this regard, Wireless Sensor Networks (WSN) are gaining demand in many applications ranging from remote sensing and monitoring to healthcare, bio-sensing, security system, and environmental applications [11][29]. These systems shall be sufficiently small to make the deployment non-intrusive and consume as little power as possible to minimize any maintenance action. Regardless of the power supply, consumption should be limited to tens of microwatts for a reasonable volume and lifetime [1]. Teardown of the power consumption of some commercial motes that target IoT applications shows that the radio-frequency (RF) circuitry of both the transmitter and receiver is the dominant part, responsible for more than 50% of the total power consumption. Therefore, design of RF circuitry consuming in the order of a few microwatts is a capital target for the IoT paradigm.

Conventional battery-based solutions exhaust easily and not only lead to their costly replacement especially when the device is located at inaccessible locations, but also places a limitation on the miniaturization of the system, not to mention the ecological impact due to the pollution caused to the environment. As a result, sensors

that harvest the energy from the environment has emerged in the past few years. The goal in energy harvesting is to enable self-powered electronic devices by scavenging ambient energy for various wireless electronic applications ranging from structural health monitoring to medical implants. Different energy sources existing in the environment around a system, such as sunlight, wind, and mechanical vibration, can be the options for energy harvesting. Among them, thermoelectric generators (TEG) and microbial fuel cells (MFC) are attractive candidates to supply power in the order of tens of microwatts with reduced size [1]. In contrast to discrete-time solutions in which energy and voltage are highly volatile, like photo voltaic cells (PVC) or piezo-electric harvesters (PEH), TEG and MFC provide a continuous-time energy source, although producing voltages in the order of a few hundreds of millivolts. Hence, besides low power consumption, the second major requirement for the RF circuitry is to be able to provide reasonable performance even if operated with supply voltages of a few hundred of mV. These requirements define the boundaries of a new design approach referred as Ultra-Low Power (ULP) and Ultra-Low Voltage (ULP) design.

1.1 Ultra-Low Power and Ultra-Low Voltage

Every ULP and ULV design is constrained by stringent consumption requirements. In order to cope with the previously stated IoT demands, power consumption shall be lower than 100 µW while operating under a voltage supply no larger than 800 mV. Power consumption does in fact benefit from this aggressive voltage scaling. Other than that, though, reducing the supply voltage of CMOS circuitry has dramatic impacts on the operation of transistors. Besides the intrinsic voltage gain reduction, the transition frequency becomes severely deteriorated when the available headroom decreases, limiting dynamic range, noise, and linearity of RF systems. In the end, designers are pushed towards power-saving near-threshold and sub-threshold transistor conditions, although at the cost of an overall performance degradation.

Furthermore, the ever-shrinking size of transistors gives rise to short channel effects. In short channel devices, the gate is not the only terminal that has control over the channel but also the drain through the size of the depletion region it creates. The impact of the drain on the channel potential rises as the drain voltage increases, and the result is a reduction in the threshold voltage V_{TH} of the device. This phenomenon is called drain-induced barrier lowering (DIBL), and is also responsible for drain conductance degradation, especially in short channel devices operating at low-inversion levels [1].

$$V_{TH} = V_{TH_0} - \lambda_{DIBL} V_{DS} - \lambda_{BB} V_{BB} \tag{1.1}$$

where V_{TH_0} is the threshold voltage when no bulk bias is applied, λ_{DIBL} is the DIBL effect coefficient, and λ_{BB} is the body effect coefficient. Thus, V_{TH} increases in an approximately linear fashion when the magnitude of the drain-source voltage is reduced, further enhancing sub-threshold operation. The DIBL coefficient is in

the order of 0.1 or larger, thus stating the pronounced dependence of the threshold voltage on the supply of the circuit.

The constraints imposed by ULP-ULV scenarios motivate the research on new technologies in order to supersede the limitations of the conventional bulk technology, like gate tunnelling leakage current due to thinner gate insulators. To help with the purpose, FD-SOI (fully depleted silicon-on-insulator) is a promising technology for low-power designs due to its low leakage and precise threshold voltage control. Moreover, it offers an easy manufacturing process and migration from conventional bulk technology compared to other advanced technologies like FinFet. Chapter 2 will cover in more detail FD-SOI capabilities and its potential application in low-power low-voltage designs.

1.2 Receiver Front-End Basics

The basic structure of a radio-frequency (RF) receiver is depicted in Figure 1.1. The first block just after the antenna is the low-noise amplifier (LNA), which amplifies the severely attenuated incoming RF signal for the subsequent stages. The next block is the mixer, having as inputs the amplified RF signal and the local oscillator (LO). The RF signals in a receiver need to be down-converted to a lower frequency before the waveform is transformed into a digital signal by an analog-digital converter (ADC). The process of digital conversion is not performed at RF due to the high power consumption of ADCs at high frequencies. The circuit that performs the frequency down-conversion process is the mixer, whose main functionality is to shift the RF signal in frequency as per the frequency magnitude of the LO. Once the signal has been down-converted, it may be further amplified by baseband circuitry before demodulation takes process and it is finally converted to digital data.

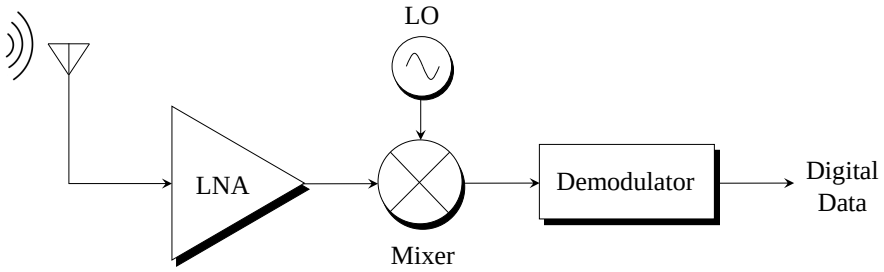


Figure 1.1: Front-end radio-frequency receiver block diagram.

Two different receiver architectures are differentiated depending on the down-conversion frequency employed. When the RF signal is directly translated to DC, the receiver is called to be homodyne. On the other hand, when the signal is shifted to a lower intermediate frequency (IF) the receiver is heterodyne. One inconvenient of the heterodyne architecture is the image frequency, which is the frequency situated

at the same distance form the LO but in the opposite side with respect to the desired band. Both the desired and the undesired image frequency will be down-converted into the intermediate frequency, so typically image-reject filters are employed to alleviate this issue. Homodyne structures, despite not having an image frequency, specially suffer form DC offsets (which require compensation) and low frequency flicker noise from devices.

Noise is a parameter of critical importance in any receiver as it corrupts the desired signal carrying the information resulting in an increase of the bit-error rate (BER) and limiting the sensitivity of the system. The addition of noise by a circuit is usually characterized by the noise factor (F) or alternatively by the noise figure (NF) when using logarithmic scale, which is defined as

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{1.2}$$

Each of the stages in the receiver chain has different noise contributions to the output. Assuming equal input and output impedances, the overall NF of a receiver with N cascaded stages is given by the Friis' formula as following.

$$NF_{receiver} = 10\log\left(F_1 + \sum_{i=2}^{N} \frac{F_i - 1}{\prod_{j=1}^{i-1} G_j}\right) \tag{1.3}$$

Where F_i is the noise factor and G_i is the available power gain (linear) of i-th stage in the receiver chain. It is thus evident that the system noise figure is dominated by the noise performance of the first stage, given that subsequent contributions are attenuated by the gain of the preceding stages. In other words, the low-noise amplifier should add as little noise as possible, while providing sufficient gain to minimize the impact of the following blocks.

Ideally, an amplifier device has a linear response from input voltage to output voltage. However, in a practical implementation, the devices have a non-linear response. The most common measure of linearity is the third-order input intercept point (IIP3), which provides the value of input power for which the output wanted signal and output unwanted third-order intermodulation product have the same power. Intermodulation distortion is mainly important when handling large values of input power, since for the small values the power of the harmonics is much smaller than that of the signal of interest. In this case, as opposed to noise, the total IIP3 point is mainly determined by the last stages of the chain.

$$IIP3_{receiver} = -10\log\left(\sum_{k=1}^{N} \frac{\prod_{j=1}^{k-1} A_j^2}{IIP3_k}\right) \tag{1.4}$$

Where A_i is voltage gain and $IIP3_i$ is the input-referred third order intercept point of i-th stage in the receiver chain.

1.3 Goal of this Work

The aim of this work is to implement a pre-layout design of a receiver front-end architecture capable to work under the restrictions imposed by ultra-low power ($< 100\,\mu W$) and ultra-low voltage ($< 0.8\,V$) scenarios while targeting decent overall performance. Although the power consumption of a transmitter structure is in general much larger than that of the receiver, the low transmission data rate expected in most IoT applications can allow power amplifier operation with aggressively reduced duty cycles, which would then result in average consumptions orders of magnitude below the peak ones. Therefore, consumption of the system is mostly determined by the receiver chain, the design of which becomes specially challenging with an ultra-low power budget.

The specific blocks that are being addressed in this thesis are the low-noise amplifier and the mixer. The receiver is targeted to operate in the unregistered ISM $2.4\,GHz - 2.5\,GHz$ band, using an intermediate frequency of $2\,MHz$. Furthermore, to cope with the stringent power requirements, 28nm FD-SOI technology PDK will be used to take maximum profit of aggressive forward body bias and enhance transistor performance under low supply voltages.

Besides the implementation of the front-end, this work aims at evaluating the interference on the system coming from the body bias generator. Concretely, large-signal periodic analyses are employed to compute the steady-state operating point of the circuitry. Under such conditions, frequency translation effects can be characterized and utilized to determine the impact on the performance.

Chapter 2

State of the Art

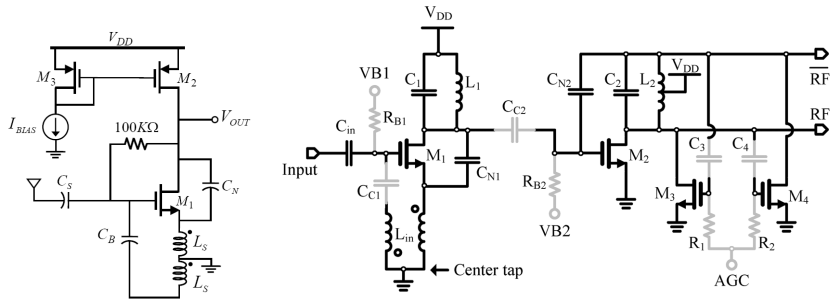
The IoT paradigm demanding inexpensive sensor nodes with wireless communication capabilities, compact size, and low cost demands the development of integrated receivers with a pronounced emphasis on low power consumption. IoT nodes have a severe constraint on power consumption in order to run for long periods of time using either small batteries or alternative energy sources like those obtained from harvesting. Scaling technologies and the request to reduce power consumption have pushed designers towards lower supply voltages, enhancing the investigation and development of new low-voltage techniques which help alleviating effects from voltage headroom reduction in analog and RF circuits. These new techniques enable the creation of integrated ultra-low-power wireless receivers well suited to applications requiring long battery life and low cost.

2.1 ULP-ULV Receiver Front-end Solutions

In the last years the research about ultra-low voltage and ultra-low power design has gained importance due to the growing number of portable devices and the power-related issues derived from CMOS technology scaling. Two common approaches exist to achieve low power consumption. The first of these approaches is utilizing stacked devices where DC current is shared by multiple circuit blocks. For example, typical stacked circuits in RF front-ends could be the LNA and the mixer, or the mixer and oscillator. Maximum current efficiency occurs when stacking the complete mixer, oscillator and LNA, achieving nearly 100% current reuse. However, this solution requires a high voltage headroom to keep transistors properly working in saturation, which does not fit the available voltages available in that scenario. The second technique is to specifically use ultra-low supply voltage to reduce as well the power consumption, which demands basically circuits based upon harshly shrinking internal voltage drops. The low supply voltage of these circuits reduces power consumption to a level that is comparable to current-reuse designs. This section covers some strategies employed in the design of ULV-ULP RF front-end receivers, focusing on the LNA and mixer blocks.

LNA design usually targets enough small-signal transconductance to overcome

the main challenge in ULV-ULP. A promising technique to raise the transconductance value even when the supply is very low is the so-called gm-boosting, which can be achieved with different solutions. The LNA presented in [24] uses gm-boosting by applying the concept of inductive feedback, which targets to double the transconductance of the input transistor by driving the signal to both the gate and source terminals with a 180° phase shift. With such approach, $v_{gs} = 2v_{in}$, and the behaviour of a transistor with twice gm is obtained. The LNA, shown in Figure 2.1a, is fabricated in a standard 0.18 µm CMOS technology and has a nominal operating frequency of 1 GHz. It presents a power consumption of 100 µW using a voltage supply of 1 V, so the ULV requirement would be satisfied. Instead, the inductive feedback LNA in [11] promises reliable operation under an extremely reduced supply of 250 mV, although the consumed power is 150 µW using a 2-stage gain architecture, arguably still large in terms of ULP. The circuit, which can be checked in Figure 2.1b, is fabricated in standard 130 nm process and its operation centre frequency is 1.575 GHz.

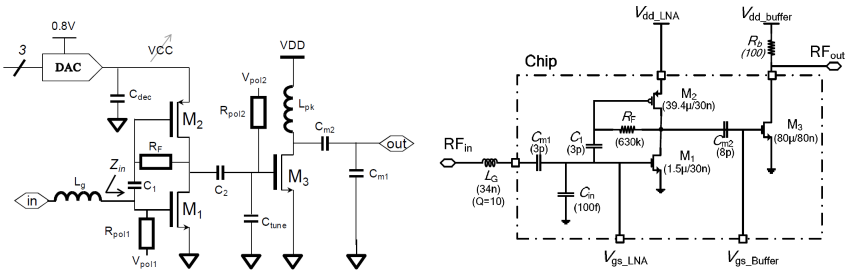


(a) *gm*-boosting LNA at 1 V and 100 µW.

(b) *gm*-boosting LNA at 250 mV and 150 µW.

Figure 2.1: Inductive feedback LNAs. Images taken from [24] and [11]

As it can be seen from Figure 2.1, inductive feedback requires a transformer to couple the gate signal to the source terminal. To save the costly footprint of the transformer, active gm-boosting approaches are an alternative solution. The LNA in [29] employs current-reuse technique, which consists on using two transconductors in common-source configuration such that the overall *gm* is contributed by both devices. This LNA implements standard 130 nm process and achieves a power consumption of 90 µW using a nominal supply of 0.5 V. Thus, it could fit the ULV-ULP requirement. The consumption reported does not include the contribution of the output buffer stage. The LNA, shown in Figure 2.2a, features a digital to analog converted to control the supply voltage by means of maximizing the figure of merit of the amplifier. A similar current-reuse architecture can be found in [10] implementing standard 28 nm technology (Figure 2.2b). The paper states a design algorithm to maximize a given figure of merit based on the inversion coefficient of the transistors. The reported performance is claimed to be validated under a supply of 0.5 V, presenting a power consumption of 15 µW (excluding the output buffer) and a somewhat unrealistically low noise figure.



(a) Current-reuse LNA at 0.5 V and 90 µW.

(b) Current-reuse LNA at 250 mV and 15 µW.

Figure 2.2: Inductive feedback LNAs. Images taken from [29] and [10]

Other typical LNA topologies have also been studied and designed to operate under ULV-ULP. In particular, Chapter 3 exposes the pros and cons of a classical Inductive Source Degeneration presented in [9], which suggests decent performance due to its single-transistor structure.

Low voltage mixers are very challenging because traditional structures rely on stacking multiple transistors. Thus, to avoid limiting the minimum supply voltage, alternative topologies are needed. A possible solution are folded mixers, which prevent stacking transistors but at the cost of adding additional current branches, which traduces in higher consumption. Some works enclosed in low-power low-voltage designs employ "power-less" passive mixers like [26] or [8]. However, derived losses shall be later compensated with larger amplification in baseband thus increasing power consumption.

Probably the most interesting structure in terms of low-voltage and low-power performance is the switched transconductance mixer. An example of this type of mixer can be observed in Figure 2.3 [11]. Instead of using transistors at the source or drain terminals of the transconductors, the LO is directly applied to the source. Therefore, the whole LO swing can be used by the transconductors, maximizing headroom.

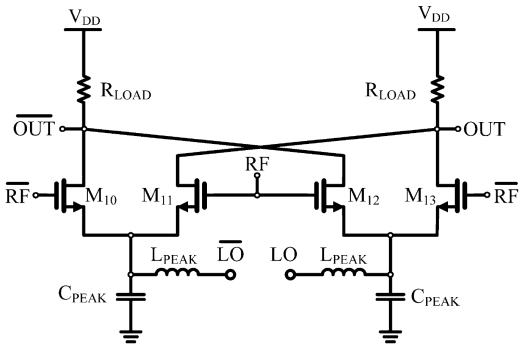


Figure 2.3: Switched transconductance mixer. Image taken from [11].

2.2 UTBB FD-SOI

The Process Design Kit (PDK) used in this work to design our circuits corresponds to a 28 nanometre ultra-thin body and buried oxide fully depleted silicon-on-insulator technology (UTBB FD-SOI). This is a planar process technology that implements an ultra-thin layer of insulator, or buried oxide, on top of the base silicon. The transistor channel is built upon a thin silicon film, thus making the transistor fully depleted. Figure 2.4 shows the structure of a typical bulk MOS transistor and an FD-SOI transistor.

Figure 2.4: MOSFETs implemented in bulk (left) and FD-SOI (right) technologies. Image taken from [18].

FD-SOI is a promising technology for low-power designs due to its low leakage and precise threshold voltage control. Moreover, it offers an easy manufacturing process and migration from conventional Bulk technology compared to other advanced technologies like FinFet [18]. In comparison with conventional CMOS Bulk technology, FD-SOI reduces the source/drain capacitances and the leakage current to the substrate by eliminating the source-bulk and drain-bulk parasitic diodes.

As a matter of design optimization and flexibility, multiple threshold voltage flavours of the transistors are available, including Regular Threshold Voltage (RVT) and Low Threshold Voltage (LVT), being the last one the model used in this work. As its name implies, LVT transistors feature a smaller threshold voltage value due to their flipped-well structure, which make them especially suitable for low-supply scenarios.

2.2.1 Body Bias

One of the most powerful features provided by FD-SOI is the additional control of the transistor through the substrate below the device, known as Body Bias. The Body Bias exploits the body effect, which describes the impact of the source to bulk voltage V_{SB} on the threshold voltage V_{TH}.

$$V_{TH} = V_{TH_0} + \gamma\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{|2\Phi_F|} \tag{2.1}$$

where V_{TH_0} is the threshold voltage with no source-body voltage, γ is the body effect coefficient and Φ_F is the substrate Fermi potential. Therefore, the designer is capable of creating an own V_{TH} by applying a voltage to a back-gate contact. Two different types of Body Bias can be applied: Forward Body Bias (FBB) and Reverse Body Bias (RBB). In Bulk technology, body biasing is limited to 300 mV due to the

need to preserve reverse-biased junction diodes and avoid excessive leakage through them. Thanks to the ultra-thin insulator layer, FD-SOI permits a very sensitive and large-range control of the threshold voltage. Qualified FD-SOI models permit FBB voltages up to 1.3 V for a decent improvement in the switching speed and RBB voltages as low as −300 mV to allow the reduction of the quiescent leakage currents.

Figure 2.5 shows the threshold voltage tuning capability offered by an NMOS LVT transistor. As it is observed, an FBB voltage application between 0 V and 1 V allows to linearly reduce V_{TH} from 310 mV to 220 mV, which corresponds to a 90 mV V^{-1} sensitivity in contrast to the 25 mV V^{-1} sensitivity provided by the typical bulk technology [18].

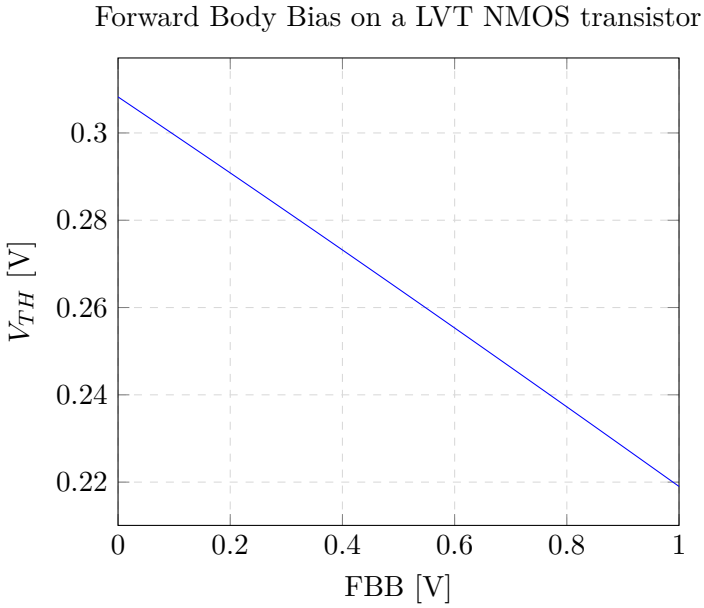


Figure 2.5: FBB effect in the threshold voltage of a LVT NMOS transistor.

One possible application of FBB is to counter the effects of DIBL, previously introduced in Chapter 1. Figure 2.6 shows how the threshold voltage evolves when the drain-source voltage diminishes for a 28 nm FD-SOI NMOS LVT.

2.2.2 Inductors

Real inductors do not behave as purely reactive elements but have losses. Due to the metal wire/track forming the coil, inductors present a series parasitic resistance which can be related to their quality factor according to 2.2, thus playing a critical role in the performance of RF circuits.

$$R_s = \frac{\omega_0 L_s}{Q} \tag{2.2}$$

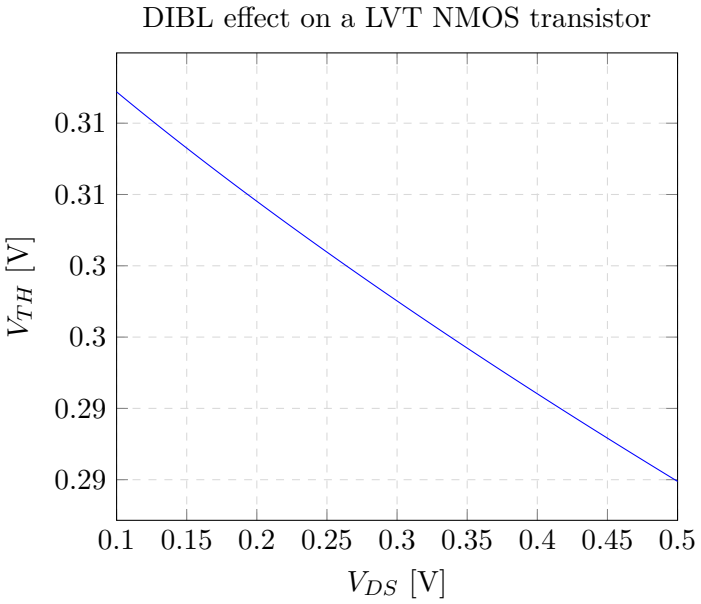


Figure 2.6: V_{TH} voltage of a LVT NMOS transistor with respect V_{DS} voltage.

where R_s is the series resistance element, L_s is the series inductance value, ω_0 is the working frequency, and Q is the quality factor.

Planar IC technologies difficult the integration of inductors, easily determining most of the RF chip area. To maximize the quality and reduce parasitic capacitances to the substrate (for a larger self-resonance frequency), thick metal layers far from the substrate shall be used. The PDK version used in this work offers a library of inductors based on parametrized cells (pcells) implemented in a limited 8-level metal stack. Due to the low number of metal layers available, the maximum inductance value that can be built at our operating frequency is only 7.8 nH. Even worse, the maximum quality factor that can be achieved is 12 using an inductance around 2 nH. The obtainable quality factor is discouragingly small attending that typical discrete commercial components easily achieve values greater than 50.

Chapter 3

Low Noise Amplifier

This chapter presents the design of the first stage of the receiver front-end, that is, the low noise amplifier (LNA). First, a brief introduction with the basic topologies and fundamental metrics of LNAs is provided. Then, a suitable topology that fits our requirements is chosen. Once the LNA topology has been determined, the basic metrics are analytically derived to gain some insight into the circuit's behaviour. The design implemented in FD-SOI 28nm technology is then presented, with a particular emphasis on transistor biasing and input matching after pad inclusion. The overall results are finally shown at the end of the chapter.

3.1 Introduction

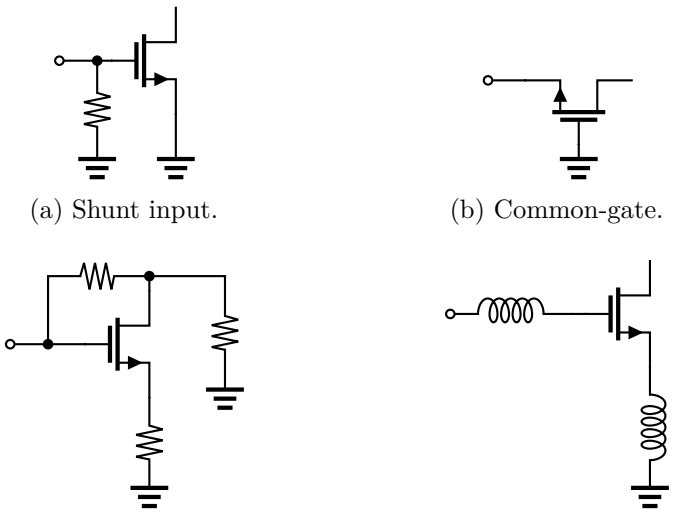
The Low Noise Amplifier or LNA is typically the first active stage in the receive path. As its name suggests, it has two main functionalities. First, it shall be able to amplify for the subsequent stages the incoming RF signal, which may be severely attenuated due to channel losses, while presenting a specific input impedance. Second, since it is the first gain stage, it should add as little noise as possible. Aside from providing enough gain while adding minimum noise, an LNA may also be required to present good linearity in order to cope with nearby strong interferences or operate with minimum power consumption. In particular, this work aims to design an LNA capable to operate under ULP ($< 100\,\mu W$) and ULV ($< 0.8\,V$) conditions.

3.1.1 Elemental Topologies

These key specifications set the targeted performance of an LNA, that depends on the circuit topology and most times unavoidable trades-offs exist between them. In the end, each topology has its own advantages and disadvantages. In some cases topologies are combined to overcome a given limitation arisen in standalone form [13]. However, the addition of extra stages usually translates into an increase of power consumption, preventing its implementation within ULP environments

Topologies may be classified in many different ways. The approach followed in this work is to present the core architecture of the basic topologies in terms of input

impedance matching solution [23]. This classification divides the architectures into four distinct approaches, which are illustrated in a simplified manner in Figure 3.1.



(a) Shunt input.

(b) Common-gate.

(c) Shunt-series feedback.

(d) Inductively degenerated common-source.

Figure 3.1: Typical LNA topologies.

Given that the aim is to provide a real input impedance to the signal source, one may think about directly adding a parallel resistance at the input of the amplifier. This configuration does actually exist and it is called shunt input termination or simply resistive termination, in which the value of the resistance is equal to the source resistance (see Figure 3.1a). While effective and easy, the use of resistors in this fashion harshly degrades the noise figure of the amplifier as the thermal noise voltage generated by the resistor directly appears at the input of the LNA, thus amplifying its contribution at the output. Besides the high noise figure, this topology may be especially suitable for wideband operation or high linearity circuits, since the effective voltage at the gate of the amplifying transistor is half the input, thus improving the linearity of the whole topology.

The shunt-series feedback topology shown in Figure 3.1c sets the input and output impedance of the LNA. It uses a feedback resistor between the gate and the drain of the amplifying device such that the input impedance presents a real part that may be used for impedance matching. When the frequency of operation is high enough, though, the parasitic capacitances of the transistor dominate the input impedance, which forces the designer to employ other matching mechanisms. Moreover, due to the direct path between the input and output ports created by the feedback resistor, this topology lacks reverse isolation and so stability shall be accurately ensured within the working frequency range.

So far, the presented topologies enter the RF input through the gate of the amplifying transistor. The common-gate topology in Figure 3.1b uses a different strategy by applying the input to the source of the transistor. By using this method,

the input signal sees an effective impedance equal to the inverse of the transistor transconductance (1/gm). Thus, matching the input impedance of the common-gate amplifier restricts the size and power consumption of the whole topology and prevents noise performance optimization as the transconductance of the input transistor is inherently fixed.

Probably the most extensively used LNA topology is the inductively degenerated common-source, graphically presented in Figure 3.1d. As in the case of shunt input termination and shunt-series feedback the input signal is applied to the gate and the output is taken from the drain. This topology uses however a completely different way of providing input impedance matching through inductive source degeneration. The source inductor is used to set the real part of the input impedance equal to the source resistance. The inductor at the gate of the input transistor adds an extra degree of freedom for the designer such that it resonates with the source inductor and the gate-source capacitance, providing narrow-band operation around a specific frequency (or resonance frequency). It is worth noting that this topology does not explicitly need a resistive element to provide a real input impedance and thus it generally exhibits the best noise performance of the previous architectures. In practice, a common-gate stage is added acting as a cascode in order to increase both the input-output isolation for improved stability and the output resistance such that a higher intrinsic gain is attained [12].

3.1.2 Previous Work on an LNA with Inductive Source Degeneration

Due to its low noise figure, ease of input matching, moderate-high gain and low-power consumption, the inductively degenerated common-source amplifier has been broadly employed in narrowband LNA designs. A recent work reports the design of an LNA using this topology while operating at a voltage supply as low as 0.25 V [9]. Moreover, the implemented technology is the same as the one being addressed in this work; 28nm FD-SOI. The circuit, which is shown in Figure 3.2, uses a single transistor stage in order to allow a deep reduction of the supply voltage while still keeping the transistor in saturation. A usual approach to increase the input-output isolation and intrinsic gain is to use a cascode transistor between the drain of the input transistor and the output node. However, the circuit in Figure 3.2 benefits from larger voltage headroom, which results critical when the voltage supply reduces

The gate and source inductors, L_G and L_S respectively, are used to resonate with the total gate capacitance to match the source impedance, while the drain capacitance L_D maximizes the gain by resonating with the load capacitance. The number of inductors that are required should not be underestimated due to the area occupied. It is thus evident that on-chip inductors impose a severe size restriction in RF integrated circuits and shall be considered early in the design stage, especially when the circuit inherently requires them.

The circuit studied in [9] serves as a starting point for this work, so it is instructive to give some hints about its operation in order to provide valuable insights into potential FD-SOI applications while stating arguments that lead to adopt a different

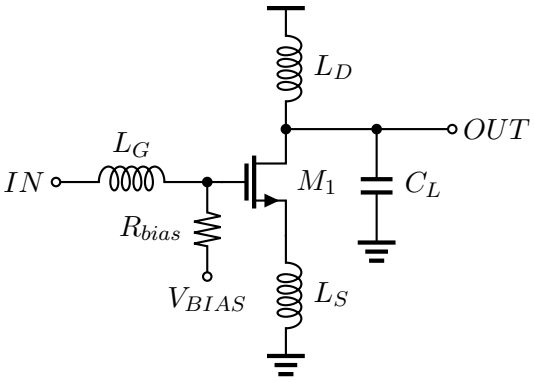


Figure 3.2: Common-source inductively degenerated LNA.

architecture for the current work. The inductively degenerated common-source is in fact a widely documented LNA topology and its analytical derivations have been thoroughly assessed before [16][32]. The basic circuit expressions will be therefore exposed without further detail and only the key design actions that deserve further argumentation will be contended.

The circuit in Figure 3.2 has an input impedance

$$Z_{in} = j\omega_0(L_S + L_G) + \frac{1}{j\omega_0 C_{GS}} + \frac{g_m L_S}{C_{GS}} \tag{3.1}$$

Once transistor dimensions and biasing are set, a value for L_S is chosen such that the real part of Z_{in} is equal to the source resistance, $50\,\Omega$. Then, the value of L_G is chosen such that L_G, L_S and C_{GS} resonate at the working frequency ω_0 thus revealing the narrowband behaviour of the amplifier.

$$\frac{1}{\omega_0 C_{GS}} = \omega_0(L_S + L_G) \tag{3.2}$$

The drain inductance L_D is used to resonate at the operating frequency with the output capacitance, maximizing the gain and improving frequency selectivity. Assuming the LNA is input matched to the source impedance R_s, the voltage gain of the circuit is expressed in equation 3.3.

$$A_v = \frac{1}{2R_s}\frac{\omega_T}{\omega_0}R_p \tag{3.3}$$

where ω_T is the transition frequency of the transistor defined as $\omega_T = g_m/(C_{GS} + C_{GD})$, ω_0 is the working frequency and R_p are the parallel losses due to the drain inductor L_D.

Accounting for the source resistance R_s, gate inductor losses R_{L_G}, gate resistance R_G and channel thermal noise, the noise factor of the LNA is as follows.

$$F = 1 + \frac{R_{L_G}}{R_s} + \frac{R_G}{R_s} + \frac{\gamma}{\alpha} g_m R_s \left(\frac{\omega_0}{\omega_T}\right)^2 \tag{3.4}$$

where γ is the thermal noise coefficient, which decreases as the transistor moves from strong inversion to weak inversion region, and $\alpha = g_m/g_{do}$.

The library of integrated inductors provided by the design kit presents a maximum inductance value of 7.8 nH. The former limitation directly opposes the inherently small parasitic capacitances of the technology. According to 3.2, when C_{GS} is small due to the reduced transistor's dimensions and the operating frequency lays on the lower RF band (few GHz), it becomes necessary the addition of a capacitor C_{added} between source and gate of the transistor so that the required values of L_S and L_G can be reduced to permit on-chip implementation.

$$\omega_T = \frac{g_m}{C_{GS} + C_{added} + C_{GD}} \approx \frac{g_m}{C_{added}} \tag{3.5}$$

It can be checked from 3.3 and 3.4 that high values of ω_T influence both gain and noise figure in a positive manner. One consequence of voltage supply reduction, though, is that the threshold voltage of the transistor increases (see Chapter 2), which diminishes g_m and the resulting ω_T. In order to verify the potential advantages provided by FD-SOI, [9] applies forward body bias (FBB) such that g_m (and so ω_T) is recovered. Alternatively, equation 3.5 reveals that ω_T is directly proportional to g_m when C_{added} is used, which implies that ω_T may also be restored by simply increasing the width of the transistor.

Table 3.1 provides the simulation results for three different designs using a C_{added} of 250 fF. The first column corresponds to the circuit operating at 1 V supply without FBB application. The second column reduces the voltage supply to 250 mV and applies FBB. Finally, the third column shows a design with the same low voltage conditions but increasing the width of the transistor instead of applying FBB.

The first design operating at 1 V offers a transconductance close to 4 mA V^{-1} with a current consumption of 173 µA. The resulting gain is almost 12 dB and the noise figure is above 6 dB. When the voltage supply is reduced down to 250 mV, g_m and ω_T lessen. In order to restore them, the second design applies FBB, providing very similar gain and noise figure values, with a much smaller power consumption. Instead, the third design shows that increasing the width of the transistor induce the same effective ω_T boost due to its desensitization to C_{GS} variations, which, again, derives in similar gain and noise figure values.

As a summary, the analysis allows to observe that the achieved performance does not depend upon the implementation of FD-SOI, even after an aggressive reduction of the supply. Having a big capacitance between gate and source permits increasing transistor's width to recover ω_T, instead of boosting g_m by applying FBB. If FBB is not able to provide an advantage for the design under ULP-ULV operation, then FD-SOI proves to be unnecessary. Furthermore, the circuit needs 3 inductors to operate, which occupy a large area in a particularly expensive technology. Even using an off-chip gate inductor, it definitely implies a decisive disadvantage compared to other topologies which do not have such area constraint. Finally, other structures which take benefit from FBB, thus justifying FD-SOI implementation, are yet required. The subsequent Chapter analyses the alternative presented in this work.

Table 3.1: Inductively degenerated common-source LNA results.

Circuit values			
V_{DD}	1 V	0.25 V	0.25 V
FBB	No	Yes	No
V_{BIAS}	250 mV	250 mV	250 mV
Total Width	45 µm	30 µm	135 µm
C_{added}	250 fF	250 fF	250 fF
L_S	6 nH	4.50 nH	6 nH
L_G	6 nH	6.50 nH	6 nH
L_D	2.50 nH	2.50 nH	2.50 nH
DC Performance			
IDC	173 µA	209 µA	165 µA
g_m	3.88 mA V^{-1}	4.25 mA V^{-1}	3.98 mA V^{-1}
Power	173 µW	54 µW	41.25 µW
RF Performance			
f_0	2.40 GHz	2.40 GHz	2.40 GHz
S_{11}	−12.77 dB	−11.54 dB	−18.70 dB
S_{21}	11.64 dB	13.16 dB	10.50 dB
NF	6.20 dB	5.47 dB	5.75 dB

3.2 Circuit Design

This chapter details the design of Low Noise Amplifier based on a circuit solution different to that presented above, targeting an overall better performance, with similar power and V_{DD} reduction. First, the chosen circuit is presented while arguing the rejection of other topologies. The basic analytical expressions are then derived such that the reader gains some insight into the circuit's behaviour. Finally, a specific impedance matching network is designed according to the parasitics introduced from the package.

3.2.1 Topology

Apart from desirable qualities like decent gain and constrained noise figure, the chosen topology shall be capable of consuming as low as possible and while operating under a harshly reduced voltage supply. Unfortunately, even though power consumption is probably the only parameter that takes benefit from the voltage supply reduction, it definitely trade-offs with any other specification in the circuit and notably challenges the whole design process.

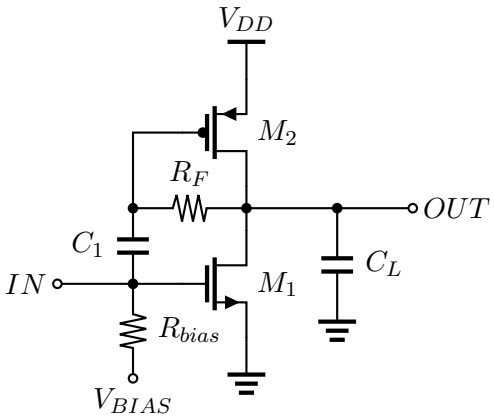


Figure 3.3: Current-reuse LNA.

It is thus required the implementation of alternative architectures that may have the potential to perform under the previous conditions. The topology selected in this work is a current-reuse active gm-boosting amplifier [29] [10]. Current-reuse is a key design technique in the implementation of ULP circuits [20]. Its operation principle relies on a complementary transistor structure where each transconductor device contributes to the overall gain of the amplifier while sharing the same DC current path, leading to a notable improvement in the current efficiency of the LNA.

The complete circuit is shown in Figure 3.3. The core of the LNA is formed by transistors M_1 and M_2 and the feedback resistor R_F. This transconductance stage converts the RF small signal input voltage into output current. A big R_F ensures proper biasing, helps reducing noise as shown in a subsequent analysis and makes the circuit less sensible to parasitics, temperature and process variations [33]. Certainly, the series connection of the PMOS and NMOS deteriorates voltage headroom compared to the source degenerated common-source of Figure 3.2. A measure to alleviate this effect, as will be later explained, consists in adding a decoupling capacitor C_1 between transistors gates. R_{BIAS} allows the proper biasing of the circuit while exhibiting a large RF impedance path. Finally, a load capacitance C_L emulates the loading of the subsequent active mixer stage.

3.2.2 Analytical Behaviour

The small-signal model of Figure 3.4 is employed to perform the gain and input impedance analysis derivation of the LNA core. For the sake of circuit understanding, the NMOS-related parameters (M_1 transistor) use an 'N' subscript and the PMOS-related parameters (M_2 transistor) use a 'P' subscript.

Due to the frequency of operation, gate-source and gate-drain parasitic capacitances are also accounted and shall not be disregarded unless otherwise demonstrated. On the other hand, the decoupling capacitor C_1 in the feedback path is shorted since it has a small impedance at the desired frequency. $g_{m_T} = g_{m_N} + g_{m_P}$ is the total

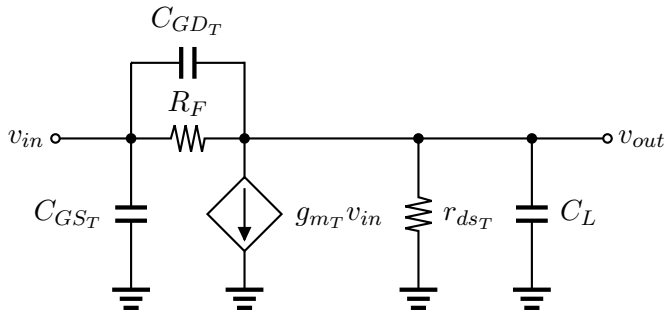


Figure 3.4: Small-signal model of the LNA core for gain and input impedance analysis.

transconductance of the amplifier and $r_{ds_T} = r_{ds_N} \parallel r_{ds_P}$ represents the total output resistance of the transistors. Moreover, both transistors contribute to the generated parasitics as well; namely, $C_{GS_T} = C_{GS_N} + C_{GS_P}$ and $C_{GD_T} = C_{GD_N} + C_{GD_P}$.

The following expressions will be frequently used throughout the different derivations as a matter of cleaning up and simplification of expressions. Z_F represents the feedback impedance due to gate-drain capacitances and the feedback resistor, while Y_F is the feedback admittance. It is worth clarifying that the actual output impedance of the amplifier should not be confused with the stated Z_{out} equation.

$$Z_F = R_F \parallel \frac{1}{sC_{GD_T}} \tag{3.6}$$

$$Y_F = \frac{1}{Z_F} = \frac{1}{R_F} + sC_{GD_T} \tag{3.7}$$

$$Z_{out} = r_{ds_T} \parallel \frac{1}{sC_L} \tag{3.8}$$

Gain

According to the small-signal model, both transconductors share the same input voltage dependence, which means that the individual contributions are summed up making the concept of current-reuse evident. A general expression of the amplifier's voltage gain is

$$A_v = \frac{(Y_F - g_{m_T})Z_{out}}{1 + Z_{out}Y_F} \tag{3.9}$$

The reduced dimensions allowed by the 28nm technology generate small parasitic capacitances that present relatively big impedances even at high frequencies. On the other hand, the value of the feedback resistance is required large according to bias and noise performance optimization. By using the approximations $g_{m_T} \gg |Y_F|$ and $| Z_{out}Y_F | \ll 1$ and considering absolute values, the resulting voltage gain is

$$A_v \approx \frac{g_{m_T}}{C_L \omega_0} \tag{3.10}$$

Where ω_0 is the working frequency.

The former expression for the gain neglects the contribution of the transistors' output resistance while still committing minor error, especially when circuit trends are analysed. Moreover, the ULP restriction implicitly confines current consumption, which in turn helps increasing transistor's output resistance.

As expected, the gain is directly proportional to the total transconductance, fed by both NMOS and PMOS transistors. Qualitatively, it can also be derived by realizing that M_1 and M_2 are common source stages driving the same output load. That is, $A_v = -g_m Z_L$, while assuming the output capacitance to dominate the load impedance. The effective transconductance is thus increased compared to a single common source stage and higher gain is achieved for a given current consumption.

Input Impedance

The Low Noise Amplifier will generally interface with an external antenna. Consequently, it shall precisely provide some specific impedance (50 Ω in this case) in order to maximize the power transfer and minimize undesired reflections back to the antenna. The input impedance of the small-signal circuit in Figure 3.5 can be obtained through the parallel computation of the gate-source impedance, namely Z_{GS}, and the equivalent impedance seen from the feedback resistance. At this stage, the effective gate-source impedance Z_{GS} is simply due to the total gate-source parasitic capacitance C_{GS_T} of the transistors.

$$Z_{in} = \frac{1}{\frac{1}{Z_{GS}} + \frac{1+g_{m_T} Z_{out}}{Z_F + Z_{out}}} = \frac{1}{sC_{GS_T} + \frac{1+g_{m_T} Z_{out}}{Z_F + Z_{out}}} \tag{3.11}$$

Equation 3.11 is not trivial to deal with, given that the approximations employed during the voltage gain derivation cannot be directly applied in this case. Also, even though gain performance is not fully determined by the transistors' output resistance, their contribution should not be neglected when the input impedance of the amplifier wants to be finely adjusted.

Tempting simplifications that the reader may be prompted to use are disregarding the influence of r_{ds_T} and C_{GD_T} over the load capacitance and the feedback resistor, respectively, but the committed error when realistic values are tested is not assumable. As a consequence, the analytical process of converting the general input impedance expression into an elegant an intuitive solution becomes a cumbersome process. Instead, a numerical-based approach where the analytical equations are characterized will be used during the input impedance matching process later on.

Noise Figure

The small-signal model of Figure 3.5 is employed to perform the noise analysis. The noise sources considered are the thermal noise form the antenna's equivalent source

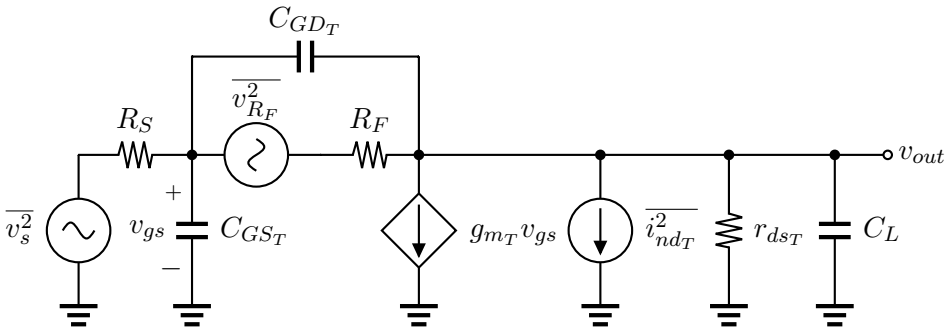


Figure 3.5: Small-signal model of the LNA core for noise analysis.

resistance (R_s), the thermal noise from the feedback resistor (R_F) and the channel thermal noise from both NMOS (M_1) and PMOS (M_2) transistors.

Given that all sources are uncorrelated we can apply superposition and analyse each of the individual contributions separately. The simplified minimum noise figure of the LNA is depicted in 3.12 [29].

$$F_{min} = 1 + \frac{R_s}{4R_F} + \frac{4\gamma}{\alpha} g_{m_T} R_s \left(\frac{\omega_0}{\omega_T}\right)^2 \tag{3.12}$$

Despite considering only the LNA core alone, the previous equation permits realizing that any additional noise source at the input of the amplifier will increase the resulting noise figure. In particular, losses from low-quality passive elements in the matching network have significant impact in the noise figure performance.

Usually, conditions for minimum noise figure and maximum power transfer are different and cannot be achieved simultaneously. Moreover, the former design is completely determined by the constraints imposed from ultra-low voltage and ultra-low power operation. The main mechanisms employed to reduce the noise figure of the amplifier are depicted below.

First, the transconductance will be maximized according to the biasing approach. On the other hand, it can be observed from 3.12 that the noise figure is minimized for high values of R_F, so the designer may be prompted to increase its value without apparent limit. However, noise figure cannot be further improved upon sufficiently high R_F, and an over dimensioned layout is not justifiable.

3.2.3 Biasing

Circuit biasing involves a deep knowledge of device characteristics and greatly determines overall performance. Furthermore, scaling technologies and low power requirements obsolete the well-known strong inversion long channel model promoting the development of new design methodologies. For the last decades, low-power analog IC design has been governed by the g_m/I_D figure of merit (FoM), which pursues maximizing the efficiency of the transistor's transconductance. Thus, the effective way of minimizing power consumption is biasing the transistor such that

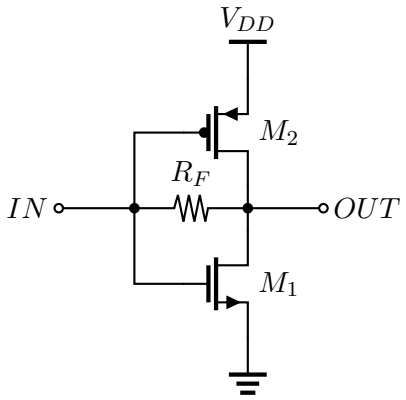


Figure 3.6: Basic structure of a current-reuse amplifier.

the g_m/I_D metric is maximized, which occurs in weak inversion. However, a weakly inverted transistor offers very poor frequency response as a result of cutoff frequency f_T degradation and it is not recommended for RF IC design. Instead, a good compromise between RF performance and DC power consumption can be achieved with the $g_m f_T/I_D$ figure of merit, permitting maximum gain-bandwidth product for a given bias current. In order to maximize $g_m f_T/I_D$, the transistor shall be biased in the moderate inversion region [25][10]. Moreover, technology scaling allows for high f_T values such that the strong inversion requirement can be relaxed making possible the migration of the design towards moderate inversion.

The traditional current reuse amplifier is shown in Figure 3.6. This type of amplifier is also called self-biased inverter, as no external biasing is required other than the supply voltage. The feedback resistor R_F permits a diode-connected structure that ensures saturation where 3.13 is hold.

$$V_{DD} = V_{SG_P} + V_{GS_N} \tag{3.13}$$

According to 3.13, the gate-source voltages of both transistors directly respond to V_{DD} variations, limiting its reduction. In order to alleviate this issue, capacitor C_1 in Figure 3.3 decouples both transistors' gates and allows lowering V_{G_P} below V_{G_N}. This new structure requires externally biasing M_1, which sets the DC current through the branch by means of V_{BIAS}. V_{SG_P} results from the generated current and sets the intermediate node voltage.

$$V_{GS_N} \rightarrow I_{D_N} \rightarrow I_{D_P} \rightarrow V_{SG_P} \rightarrow V_{DS_N} \tag{3.14}$$

Thus, supply voltage is now limited by

$$V_{DD} = V_{SG_P} + V_{DS_N} > V_{SG_P} + V_{DS_{sat_N}} \tag{3.15}$$

Given that the saturation voltage V_{DSsat_N} is well below V_{GS_N}, a more aggressive V_{DD} reduction is permitted compared to the basic self-biased inverter.

The main issue arises from the fact that, when V_{DD} reduces, V_{DS_N} reduces as well, which increases V_{TH_N} due to DIBL. As a consequence, current I_{D_N} (and so I_{D_P}) and the overall g_m lessen. Besides transconductance degradation, current reduction produces $|V_{TH_P}|$ to increase as well, thus leading to subthreshold operation region under ULV conditions.

$$V_{DD} \downarrow \rightarrow V_{DS_N} \downarrow \rightarrow V_{TH_N} \uparrow \tag{3.16}$$

$$V_{DD} \downarrow \rightarrow V_{DS_N} \downarrow \rightarrow I_{D_N} \downarrow \rightarrow I_{D_P} \downarrow V_{SD_P} \downarrow |V_{TH_P}| \uparrow \tag{3.17}$$

3.2.4 Design Methodology

This section describes the general methodology adopted for the design of the former LNA. The process is then briefly characterized attending the peculiarities of two different voltage supply scenarios.

As discussed in the biasing chapter, the low-power RF metric $g_m f_T / I_D$ has been used for biasing. In order to maximize f_T and take advantage of the technology's capability, minimum transistor length is being used. Given that $g_m f_T / I_D$ theoretically does not depend upon employed width, transistors' dimensions are not needed to be precisely defined at the very beginning of the process. Further, a high R_F value is required for proper biasing and noise figure minimization.

The proposed circuit requires an external bias voltage V_{BIAS} that polarizes transistor M_1. Thus, its inversion degree is primarily characterized by V_{BIAS}, which can be swept to search for the maximum $g_m f_T / I_D$ spot. Once the bias voltage has been defined, the desired DC current is adjusted with transistor's width W_N.

M_2 does not define the biasing conditions, although the overall results account for both transistors' performance. According to 3.10, the amplifier's voltage gain is directly proportional to the total transonductance g_{m_T} and output load. The expression assumes that the LNA is loaded with a mixer stage that dominates the output capacitance, represented by C_L. Given that V_{SG_P} is set by I_D and PMOS dimensions, the way to increase g_{m_P} is by adding width fingers M_P. However, as transistor size increases, the generated parasitics contribute loading the output as well as reduce f_T, which opposes the gain. Intuitively, thus, there shall be an optimum width size for M_2 such that voltage gain is maximized.

Nominal Supply Voltage Approach

An initial design featuring a voltage supply of 1V is first arranged to smooth the transition towards an ULV environment. At high V_{DD}, the resulting V_{DS_N} and gate-source voltages are large enough to keep the transistors within safe operating conditions. Accounting for the benign supply margin, the design is expected to provide more than 20 dB of gain and a noise figure below 3 dB with a maximum current consumption of 30 µA.

The optimum bias point on M_1 is found around $V_{BIAS} = 450\,\text{mV}$. Nonetheless, a somewhat smaller value of 350 mV is actually selected to approach lower supply

conditions early in the design process. With the aforementioned bias and assuming fingers with $W/L = 10$, the number of M_1 fingers required to provide a current of 30 µA is 4.

Ultra-low Supply Voltage Approach

In a low V_{DD} scenario V_{DS_N} is harshly reduced and derives in increased threshold voltages (see Biasing section). The main consequence is that transistors are easily brought to subthreshold due to DIBL effect degrading the frequency performance. Thus, the application of FBB to M_1 and M_2 becomes necessary. For the purpose, 1 V and −1 V bulk voltages are applied to M_1 (NMOS) and M_2 (PMOS), respectively.

Using a voltage supply of 350 mV, the maximum $g_m f_T / I_D$ is reached around $V_{BIAS} = 340\,\text{mV}$, as seen in Figure 3.7. The fact that the optimum bias point nearly coincides withV_{DD} suggests that a proper minimum supply has been selected, especially since it closely approaches the theoretical minimum $V_{TH} + V_{DS_{sat}}$. Using fingers with $W/L = 10$, the number of M_1 fingers needed to set a DC current of 30 µA is 3. In practice an equally optimal bias voltage of 350 mV has been selected to take advantage of the whole supply rail and relax the transistor sizes for a given current consumption. Regarding the dimensions of M_2, the optimum number of fingers that permit maximizing the transconductance while still generating assumable parasitics are 82. With such approach, thus, the gain is maximized.

According to 3.12, the noise figure is minimized when high values of feedback resistor R_F are employed. Figure 3.7 shows that an R_F value of 100 kΩ is sufficiently large to minimize its contribution.

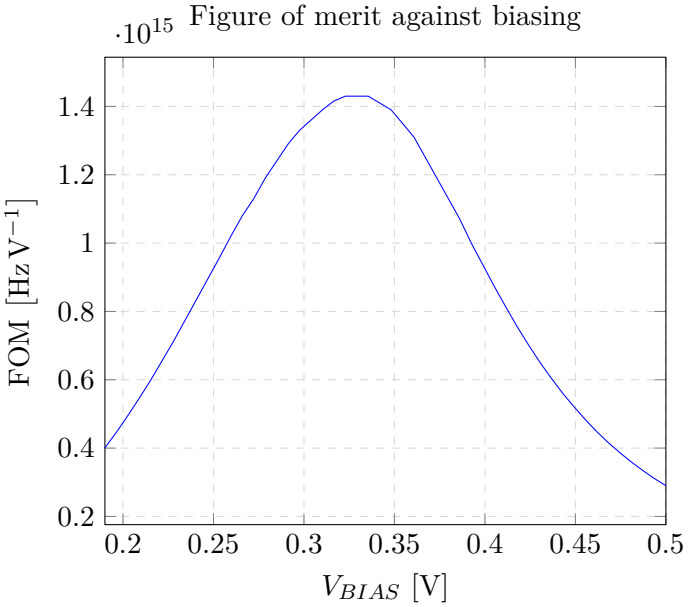


Figure 3.7: Optimum bias point at ultra-low voltage supply.

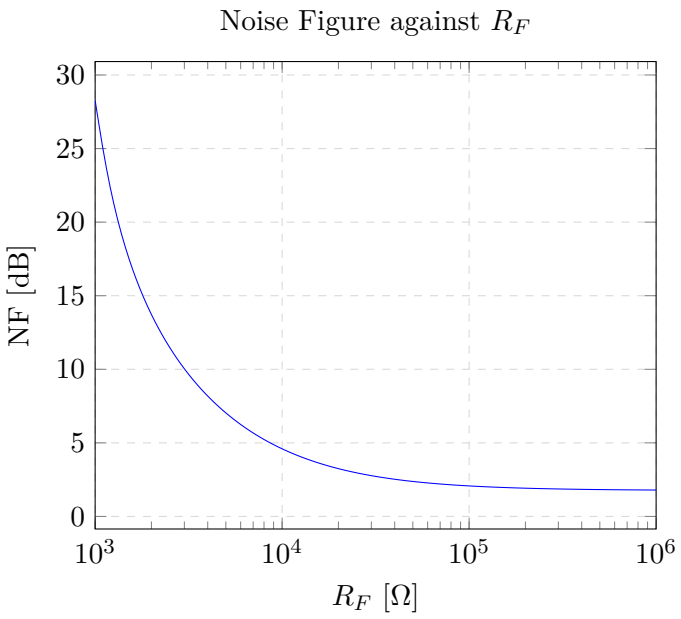


Figure 3.8: Noise figure optimization by the feedback resistor.

3.2.5 Stability Considerations

The stability of the LNA shall be checked in order to ensure that it will not oscillate under any combination of source and load impedances. The presented LNA lacks a cascode stage to maximize voltage headroom, so it becomes a major concern checking the stability due to the degraded input-output isolation caused by the feedback resistor RF and specially the gate-drain parasitic capacitances of the transconductors.

Stability is usually defined with the Rollet stability factor K_f and its intermediate terms.

$$K_f = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + D^2}{2|S_{21}||S_{12}|} \tag{3.18}$$

$$B_{1f} = 1 + |S_{11}|^2 - |S_{22}|^2 - D^2 \tag{3.19}$$

$$D = |S_{11}S_{22} - S_{21}S_{12}| \tag{3.20}$$

These expressions are characterized by the scattering parameters of the amplifier and so they are only valid under small-signal conditions. When $K_f > 1$ and $B_{1f} > 0$, the circuit becomes unconditionally stable. That is, the circuit will not oscillate under any combination of source and load impedances. Stability shall at least be evaluated over the whole frequency range of operation.

3.3 Impedance Matching

Impedance matching between the antenna and the LNA is necessary in order to guarantee proper performance of the front-end receiver and it shall be considered early in the design process. All design efforts and methodologies introduced in previous chapters are meaningless unless good matching is achieved. Due to historical reasons, a standardized impedance is typically $50\,\Omega$ [16], and this will be the target value to be achieved for the design.

The first section of this chapter analyses the resulting input impedance of the LNA-core scenario once design values have been set and some actions to restore its value. Then, the effect of the packaging on the input impedance is presented, stating the necessity to implement a specific matching network including its parasitics. The chapter concludes identifying a proper matching network through numerical and graphical approaches and its resulting implementation.

3.3.1 Input Matching Preface

When using the optimum parameter design values discussed in the previous section, the analytical derivation shows an input impedance value of $Z_{in} = 1697 - j2382\Omega$ at the centre 2.45 GHz frequency, very far from the desired $50\,\Omega$. Therefore, a mechanism able to lower the impedance values is required.

The impossibility to apply fair simplifications into the input impedance expression provided in 3.11 demands the adoption of a numerical-based approach where trends are evaluated on the analytical plots. Given a complex number y, we can find its inverse through the conjugate and modulus.

$$z = Re\{y\} + jIm\{y\} = a + jb \tag{3.21}$$

$$y^{-1} = \frac{\bar{y}}{|y|^2} = \frac{a - jb}{a^2 + b^2} = \frac{a}{a^2 + b^2} - j\frac{b}{a^2 + b^2} \tag{3.22}$$

Note that by quickly examining 3.11 the input impedance is directly stated as the inverse of a given complex expression, which we may simply identify as Z_{in}^{-1}.

$$Z_{in}^{-1} = sC_{GS_T} + \frac{1 + g_{m_T} Z_{out}}{Z_F + Z_{out}} \tag{3.23}$$

Let's consider Z_{in}^{-1} the generic complex number y in 3.21, and Z_{in} the inverse of that complex number. In other words, let's set

$$Z_{in}^{-1} = Re\{Z_{in}^{-1}\} + jIm\{Z_{in}^{-1}\} = y = a + jb \tag{3.24}$$

Quick simulation results of Z_{in}^{-1} show that its imaginary part is in the order of 10^{-3} and the real part is in the order of 10^{-3}. That is, $Im\{Z_{in}^{-1}\} \gg Re\{Z_{in}^{-1}\}$. In other words, $b^2 \gg a^2$, and Z_{in} may be simplified to

$$Z_{in} = y^{-1} = \frac{a}{a^2+b^2} - j\frac{b}{a^2+b^2} \approx \frac{a}{b^2} - j\frac{1}{b} = \frac{Re\{Z_{in}^{-1}\}}{Im\{Z_{in}^{-1}\}^2} - j\frac{1}{Im\{Z_{in}^{-1}\}} \tag{3.25}$$

The former equation reveals the strong dependence of the input impedance on $Im\{Z_{in}^{-1}\}$. The key point is to realize from equation 3.23 that $Im\{Z_{in}^{-1}\}$ is directly affected by the gate-source capacitance impedance $1/(sC_{GS_T})$. According to 3.25, thus, we can directly tune both the real and imaginary parts of Z_{in} through the addition of an input shunt capacitance, which we may provisionally identify as C_{added}.

$$Z_{in}^{-1} = s(C_{GS_T} + C_{added}) + \frac{1 + g_{m_T} Z_{out}}{Z_F + Z_{out}} \tag{3.26}$$

The result of adding an input shunt capacitance C_{added} is presented in Figures 3.9 and 3.10. As expected, both real and imaginary magnitudes of the input impedance decrease as the capacitance values increase. According to simulations, the particular gate-source capacitance value that would adjust $Re\{Z_{in}\}$ to 50 Ω is 41.15 fF. The remaining $Im\{Z_{in}\}$, which has a negative magnitude, could then be cancelled using a series inductor. However, it is worth noticing from 3.25 that the influence of C_{added} is more severe towards $Re\{Z_{in}\}$ than $Im\{Z_{in}\}$. In other words, even though the shunt capacitance can easily adjust $Re\{Z_{in}\}$, the resulting $Im\{Z_{in}\}$ may still require fairly large impedance values (that is, big inductances) to be neutralized.

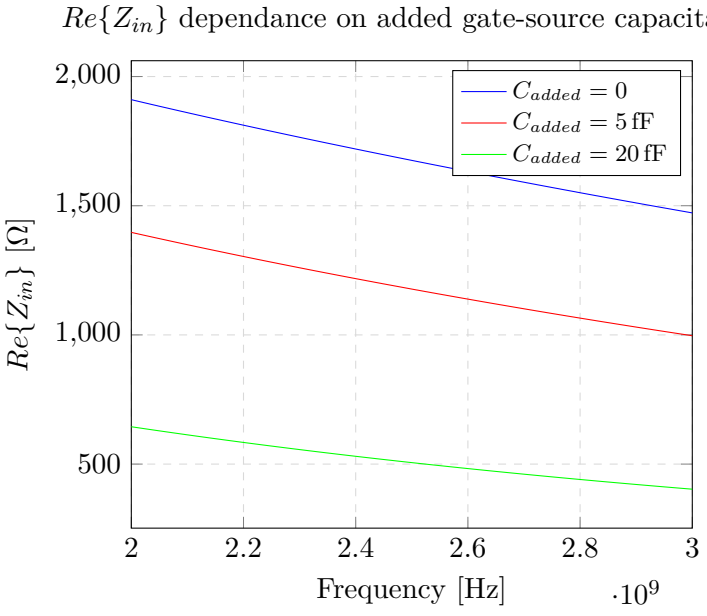


Figure 3.9: Real part of input impedance using different gate-source capacitance values. The curve for $C_{added} = 0$ corresponds to the kick-off input impedance.

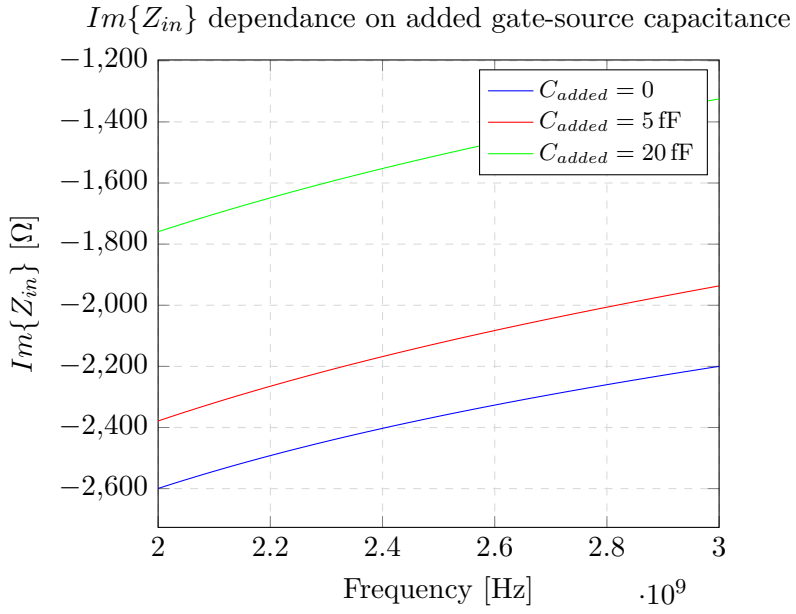


Figure 3.10: Imaginary part of input impedance using different gate-source capacitance values. The curve for $C_{added} = 0$ corresponds to the kick-off input impedance.

3.3.2 Input Matching with Pad

The semiconductor active part of a chip shall be encapsulated in a supporting case called package in order to prevent physical damage and corrosion while allowing interfacing with the outer world through pad connections. Depending on the package type, the silicon die may be connected to the pads using different bonding techniques. Two typical types of IC bonding are wire bonding and bump bonding.

Wire bonding is a conventional technique which provides electrical connection between the silicon die and the pads using very fine wires, typically made either of gold or aluminium. Due to its effectiveness in terms of cost and interconnection flexibility, wire bonding is still used in more than 90% of current semiconductor packages assembly [31]. This traditional bonding style uses a back-side down orientation of the silicon die where Input/Output cells on the chip are placed at the boundaries surrounding the core.

As silicon processes migrate to lower technology nodes, the demand for interconnection approaches that achieve more compact solutions emerges. Flip Chip is a growing technology that allows a higher Input/Output cell density by directly facing the active area towards a substrate base, which provides the pad interface. Instead of facing up and bonded to the package leads with wires from the outside edges of the chip, like wire bonding, any surface area of the flip chip can be used for interconnection, which is typically done through metal bumps of solder, copper or nickel/gold, hence the notation bump soldering [17].

In the end, all forms of packaging structures will introduce (usually undesired) parasitics to the circuit. Although typical low-frequency designs may be able to cope

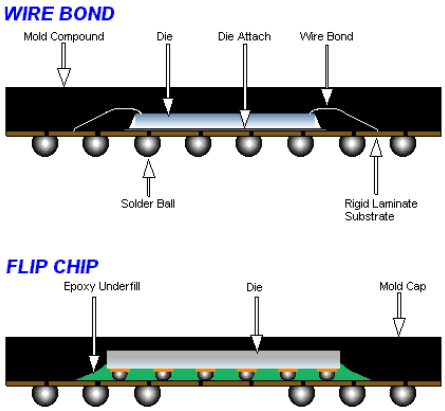


Figure 3.11: Wire bonding and bump bonding interconnection processes. Image taken from [17].

with those parasitics without further attention, the performance of radiofrequency circuits will vastly degrade unless proper countermeasures are evaluated from early design stages. These parasitics are more significant depending on the chosen package. For example, if the package requires wire bonding, the resulting series inductance due to the connection wire will be much more predominant than in a Flip Chip approach.

According to the technology library specification, the IO cells induce a parasitic capacitance around 220 fF and an additional worst-case 67 fF capacitance due to the pad itself. An intermediate approximate total capacitance value of 250 fF is assumed in the following, which directly appears at the input of the LNA acting as an additional gate-source capacitance. From now on, the term 'pad' may be used to refer to both the IO cell and pad itself.

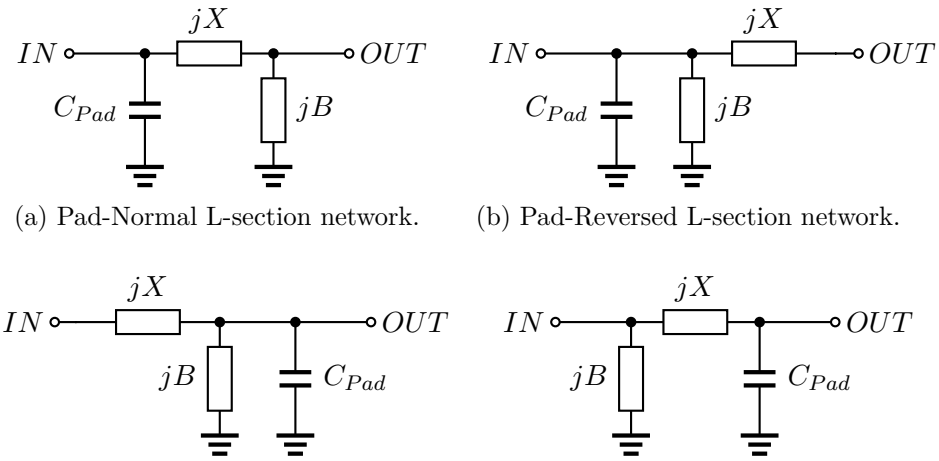
At this point the reader may already realize the impact of a 250 fF big capacitance at the input of the LNA by having a look to Figures 3.9 and 3.10 again. Effectively, the input impedance of the amplifier will become severely reduced, changing from the starting $Z_{in} = 1697 - j2382\Omega$ to $Z_{in} = 6.2 - j200\Omega$ according to simulation results. As a consequence, a specific matching network which accounts for these parasitic effects shall be designed.

There are multiple options as regards matching network topologies. Some of the features which characterize a network design include frequency bandwidth, quality factor, DC biasing, adjustability or size. In this case, the aim is to achieve a robust design by keeping it as simple as possible. Otherwise, as complexity increases, so does the number of factors which determine the performance of the network and consequently that of the overall receiver.

The analysis of lumped element components assumes that the wavelength at the frequency of operation is much higher than the dimensions of the components themselves. Current technologies allow for components dimensions of phew millimetres and lower, so the assumption of lumped elements will be valid even at our working frequency range.

One of the simplest types of impedance transformation network is the L-section, named due to the topology shape. It consists of two reactive elements to conjugately match the load impedance to the source [3]. The quality factor is determined by the ratio of impedances to be matched and cannot be used as a design variable, suggesting a limitation on bandwidth improvement. The main reason to use only inductors and capacitors is that reactive elements are ideally noise-less and, considering that their location is at the beginning of the receiver chain, they have a direct impact upon the LNA's noise figure. Moreover, reactive elements permit minimizing the power losses.

In order to palliate the effect of the pad, its parasitic capacitance will be included as part of the matching network. Analytically speaking, we have a total of four different network configurations as shown in Figure 3.12. It is worth noting that any shunt element at the boundary may be implemented inside or outside the chip, like networks 3.12c and 3.12d.



(a) Pad-Normal L-section network.

(b) Pad-Reversed L-section network.

(c) Normal-Pad L-section network.

(d) Reversed-Pad L-section network.

Figure 3.12: Overview of L-section matching networks including the parasitic capacitance of the pad.

Many approaches can be adopted in order to choose the appropriate network. In this case, both analytical and graphical solutions will be used. Even though in-situ lab measurements together with tuning work are often required to determine the proper final values, preliminary computation is needed to set up the type of structure and target the component values.

The difficulty to build high quality on-chip inductors with minimum inductance values requires good comprehension of commercial device characteristics. Due to the narrowband behaviour of the amplifier, it is highly important to consider component tolerances in order to evaluate the potential deviations produced on the input impedance. In this regard, selection of the best matching topology will be done after a sensitivity analysis in which the network response will be examined upon variation of the matching elements values due to their tolerances. This sensitivity analysis will allow to identify those networks which suffer the most from components tolerances

and will be thus discarded. A graphical representation using Smith charts will then provide a deeper understanding on the network's' behaviour and optimal solutions will be discussed.

Despite there being no transmission line as such, a system impedance must still be defined to enable normalization and de-normalization calculations, and $Z_0 = 50\,\Omega$ is a good choice as it is the stated source impedance.

Sensitivity Analysis

Real components present some deviation from the nominal specifications. For example, a $1\,\text{k}\Omega$ resistor with a specified 10% tolerance on its value has a potential range of values between $0.9\,\text{k}\Omega$ and $1.1\,\text{k}\Omega$. In a front-end receiver, it is highly important to present a fairly robust input impedance value such that matching conditions are guaranteed under different non-ideal conditions. The former analysis exposes the analytical expressions of the different networks and identifies those which are more sensitive to their components variations.

As a matter of mathematical derivation aid, the impedances shown in Figure 3.12 are expressed in terms of reactance X for the series elements and susceptance B for the shunt ones. Moreover, the analysis accounts only for plausible solutions. That is, for example, if a network requires the implementation of an on-chip inductor, its value shall be smaller than 7.8 nH in order to be in compliance with the library constraints.

The outcome of the sensitivity analysis is provided in a relative percentage error way. By circuit analysis, a system of equations for X and B can be obtained the solution of which provides the nominal values of the components such that matching is achieved at the frequency of interest. A details this analysis and the resulting expressions, where a quadratic solution takes places. That is, each network has two possible pairs of solutions, which we will simply name option 1 (X_1, B_1) and option 2 (X_2, B_2).

Then, each element is varied from its nominal value according to a $\pm 5\%$ tolerance basis and the resulting input impedance is compared against the desired one, both real and imaginary parts. The committed error is defined as

$$\delta = \left| \frac{Z_{in} - Z_0}{Z_0} \right| 100\% \tag{3.27}$$

Where Z_0 is the characteristic impedance of the system and Z_{in} is the input impedance, which differs from Z_0 when the network element is varied from its nominal value. It is worth noting that, despite there being no transmission line as such, a system impedance must still be defined to enable normalization and de-normalization calculations, and $Z_0 = 50\,\Omega$ is a good choice as it is the stated source impedance.

Figures 3.13, 3.14, 3.15, 3.16, 3.17, 3.18, 3.19 and 3.20 show the results of the sensitivity analysis for all networks, where both pairs of component values (recall, (X_1, B_1) and (X_2, B_2)) and the resulting error in the real and imaginary parts of the input impedance are plot. The x-axis is used to represent the tolerance variation (in a normalized way) applied on the network element with respect to the nominal

value. Therefore, the centre of the axis represents the nominal value of the network element where matching occurs and thus the error is 0. Finally, the y-axis specifies the committed error as defined in 3.27.

The obtained results let us retrieve some conclusions. The Pad-Normal L-section network presented in Figure 3.12a is extremely sensitive to tolerance in the shunt component regardless of the option used, easily exceeding 100% relative error with tolerances lower than 5% as seen in Figures 3.13 and 3.14. Given that the series reactance component does also induce relevant error, the performance of the network is too dependent upon the quality of both series and shunt elements. As a consequence, this network is being discarded as a plausible solution.

The reader may be prompted to assess the suitability of the Normal-Pad L-section network (Figure 3.12c) by inspecting the influence of the series reactance element in the real part of the input impedance. As it can be observed from Figures 3.17 and 3.18, the error committed is almost negligible. Nonetheless, the error in the imaginary part, which is higher than 50% at the tolerance margins, turns out to be excessive. The matching objective demands an input impedance similar to 50 Ω, which effectively induces an imposition on both real (50 Ω) and imaginary parts (0 Ω). In other words, the resulting error should be ideally constrained for both real and imaginary parts. In this regard, both Pad-Reversed L-section (Figure 3.12b) and Reversed-Pad L-section (Figure 3.12d) networks present an overall decent robustness towards the shunt component, since the resulting error on the real and imaginary

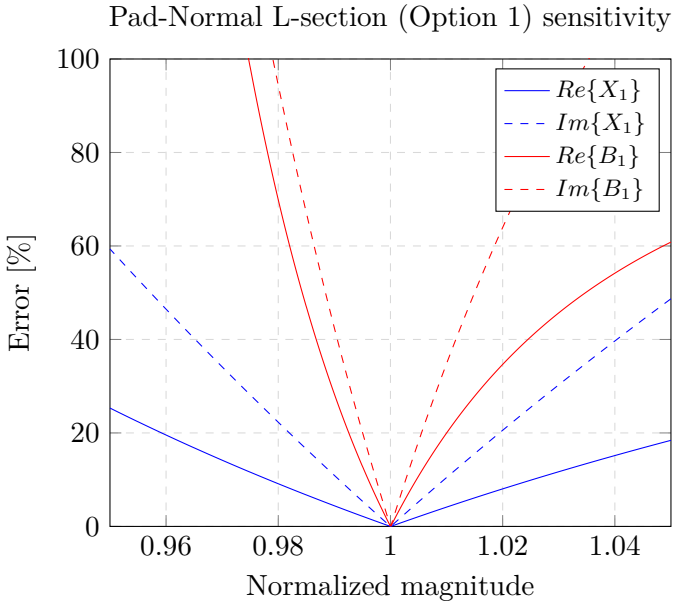


Figure 3.13: Input impedance relative error due to tolerance variations on real and imaginary parts of series (X) and shunt (B) elements using Option 1 of Pad-Normal L-section network.

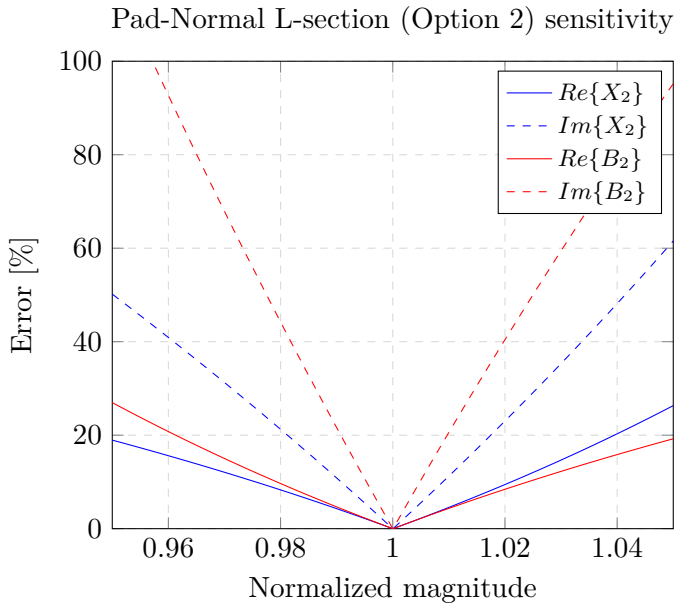


Figure 3.14: Input impedance relative error due to tolerance variations on real and imaginary parts of series (X) and shunt (B) elements using Option 2 of Pad-Normal L-section network.

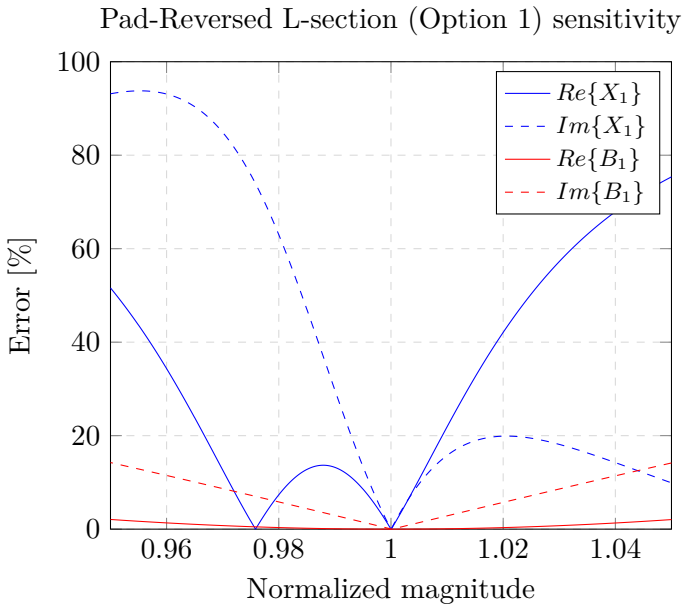


Figure 3.15: Input impedance relative error due to tolerance variations on real and imaginary parts of series (X) and shunt (B) elements using Option 1 of Pad-Reversed L-section network.

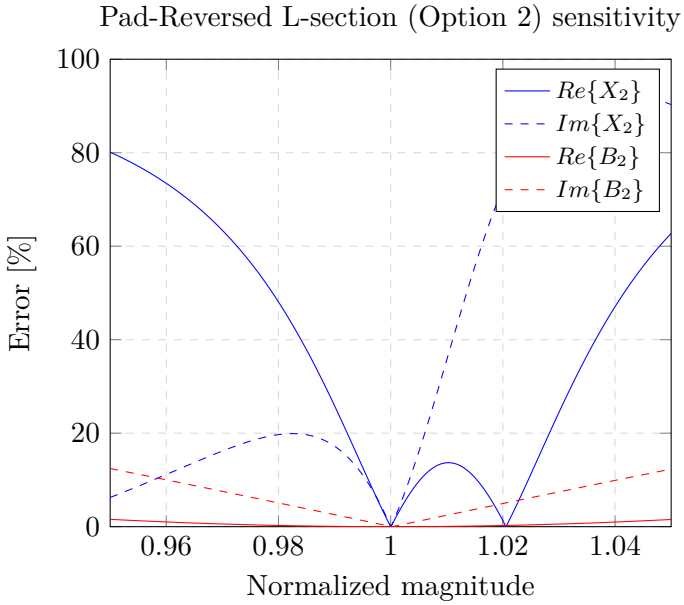


Figure 3.16: Input impedance relative error due to tolerance variations on real and imaginary parts of series (X) and shunt (B) elements using Option 2 of Pad-Reversed L-section network.

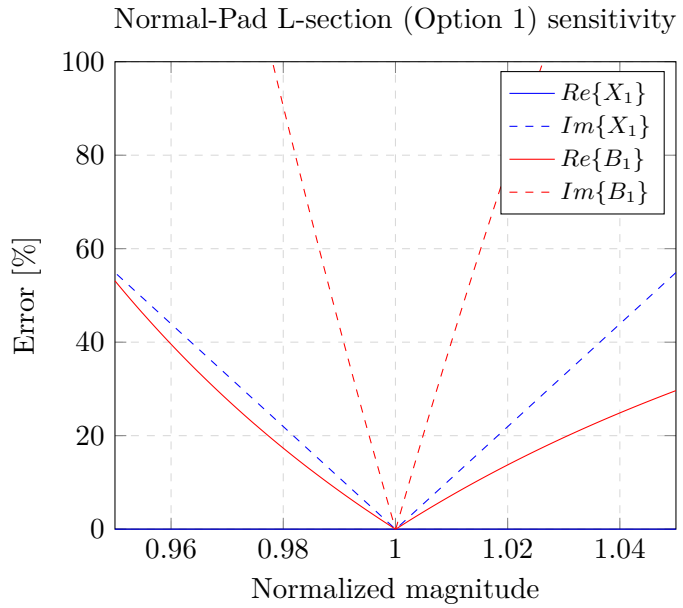


Figure 3.17: Input impedance relative error due to tolerance variations on real and imaginary parts of series (X) and shunt (B) elements using Option 1 of Normal-Pad L-section network.

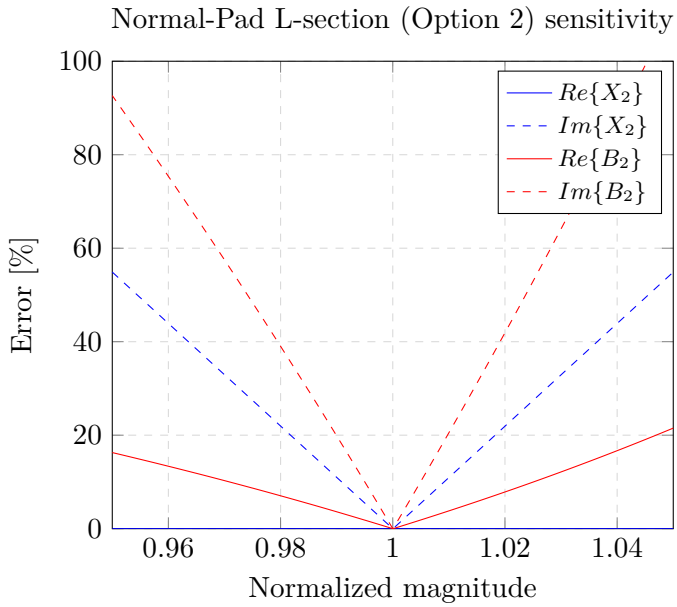


Figure 3.18: Input impedance relative error due to tolerance variations on real and imaginary parts of series (X) and shunt (B) elements using Option 2 of Normal-Pad L-section network.

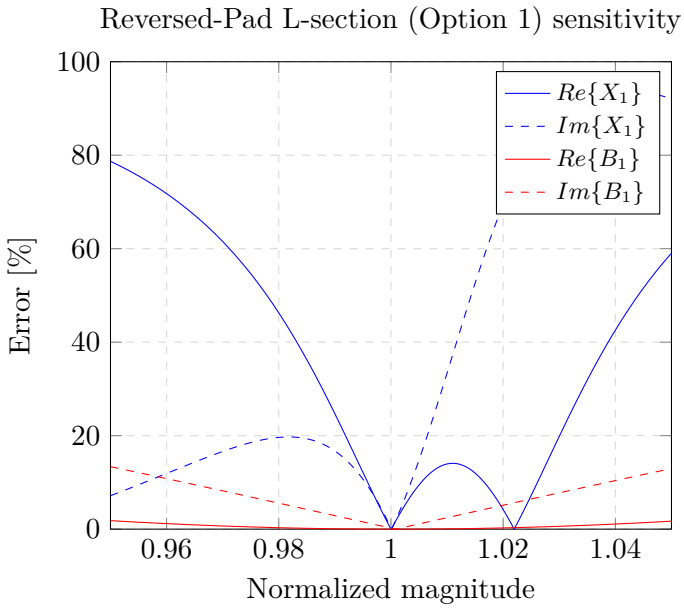


Figure 3.19: Input impedance relative error due to tolerance variations on real and imaginary parts of series (X) and shunt (B) elements using Option 1 of Reversed-Pad L-section network.

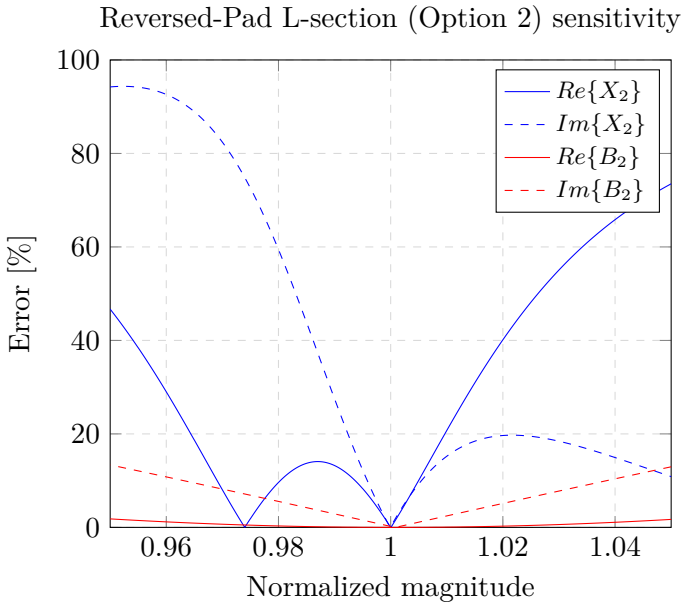


Figure 3.20: Input impedance relative error due to tolerance variations on real and imaginary parts of series (X) and shunt (B) elements using Option 2 of Reversed-Pad L-section network.

parts is less than 5% and 15%, respectively (see Figures 3.15, 3.16, 3.19 and 3.20). The value deviations of this component are thus not critical and those shall only be accurately restricted for the series element.

As a conclusion, Pad-Reversed L-section (Figure 3.12b) and Reversed-Pad L-section (Figure 3.12d) have proven relevant sensitivity towards only one of its constituent elements. Without further evaluation, only the Pad-Reversed L-section would be capable of providing a fully-integrated solution, so it would be definitely preferred in terms of cost and (presumably) size. As previously commented, though, there exist multiple aspects that determine the performance and viability of a matching network. For example, a network which requires on-chip passive elements may be severely restricted due to the limited values and quality factors provided by the library. Thus, an alternative methodology is required in order to help deciding the proper topology. The following chapter provides a graphical solution of the two networks.

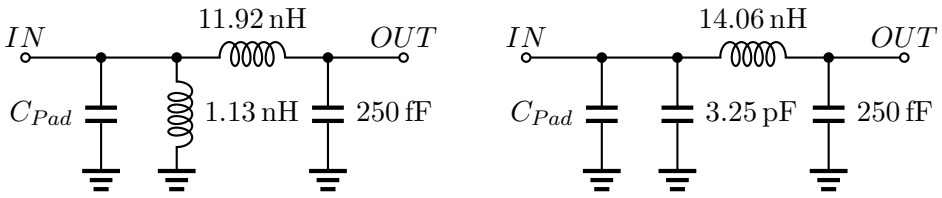
Graphical Analysis - Smith Chart

To determine which is the network solution that best suits our requirements, the Smith Chart will be used. Appendix B details basic aspects of this graphical tool, describing its shape, how it is used and the benefits provided to the designer.

So far, the reader may wonder the reason to use graphical approaches when computational CAD analysis may easily solve the problem. The fact is that, when

used correctly, the Smith Chart can provide matching impedances without any computation at all, providing the engineer with an extremely valuable insight into network trends.

According to the sensitivity analysis outcome, the selected networks that require further assessment are the Reversed-Pad L-section (Figure 3.12d) and the Pad-Reversed L-section (Figure 3.12b). Both of them are being graphically evaluated in Appendix B with the aid of the Smith Chart. Figures 3.21 and 3.22 show the result of the graphical analysis. As predicted by the sensitivity analysis, each network features two different combination of component values, named Option 1 and Option 2 for simplicity. By observing Figure 3.21, the reader may note two important facts. First, the Pad-Reversed L-section network explicitly requires a shunt capacitance just before the LNA to lower the kick-off load impedance. Otherwise, the given structure is not capable to provide matching as seen in Appendix B. Second, a main concern is the large value required for the series inductor, which, due to library restrictions, cannot be implemented on-chip. Even more, if maximum inductor quality is targeted, then the inductance value should be around 2 nH as explained in Chapter 2. Thus, this matching solution must be discarded in favour of the Reversed-Pad L-section network. As commented in Appendix B, the Smith Chart permits easily observing that a larger gate-source capacitance is capable to reduce the value of the inductor, which has a great impact in the circuit's performance as explained the following section. In other words, by implementing an added on-chip gate-source capacitance, the external inductor value may be adjusted as desired to fit the best commercial option.

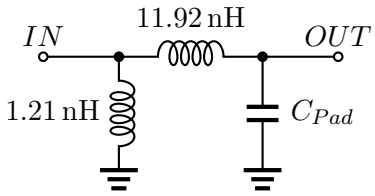


(a) Option 1. (b) Option 2.

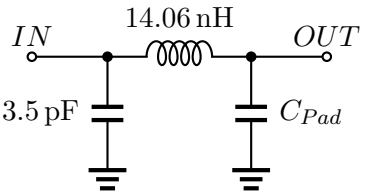
Figure 3.21: Pad-Reversed L-section network values with 250 fF pad capacitance and an additional 250 fF input capacitance.

The chosen solution shall feature high-quality inductors, which definitely cannot be implemented with the current library. Consequently, the Pad-Reversed L-section network is being discarded and the remaining option is the Reversed-Pad L-section network. In this case, both shunt and series elements are off-chip, which avoids the commented restrictions imposed by the library. Far from being an obstacle, though, catalogues from RF manufacturers offer a wide range of passive types and values which face the inherent adjustability of on-chip devices. Moreover, the topology of the network permits interfacing the series inductance with the pad, so the structure can easily handle the parasitic inductance from any potential bonding.

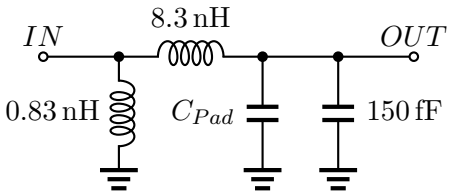
The first solution obtained from the Smith chart (Figure 3.22a) features a shunt inductor and a series inductor prior to the pad capacitance. The value needed for



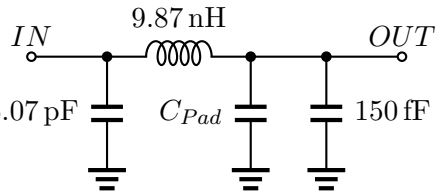
(a) Option 1 without additional shunt capacitance.



(b) Option 2 without additional shunt capacitance.



(c) Option 1 with additional shunt capacitance.



(d) Option 2 with additional shunt capacitance.

Figure 3.22: Reversed-Pad L-section network values with 250 fF pad capacitance without any additional component ((a) and (b)) and employing an additional 150 fF input capacitance ((c) and (d)).

the shunt inductor is quite low (below 2nH), which restricts its quality factor and tolerance availability. Also, the shunt inductor requires the addition of a series decoupling capacitor such that the biasing of the amplifier is maintained. As a matter of minimizing the interference on circuit operation, the decoupling capacitor shall be large enough to present a low impedance path at the operating frequency, which in turn asks for a larger chip area and additional parasitics to account for.

On the other hand, the second option in 3.22b consists of a shunt capacitor and a series inductor. This topology does not require the addition of a decoupling capacitor and its nominal value stands within typical manufacturers' portfolio specifications. Even though the resulting series inductor presents a larger value than the first option, the Smith chart study demonstrated the possibility to handle an additional input capacitance that would relax the required inductance value, as seen in Figures 3.22a and 3.22d. Moreover, given that this capacitance can be easily implemented on-chip, it may also be employed as a matter of final adjustment mechanism. All things considered, this solution is the most optimal among the different topologies presented so far.

3.3.3 Implementation

The Smith chart provides the first approach to the magnitude values that are required for the matching network. These values are used as the starting point in order to smooth the simulation process, which allows for the final adjustment according to components non-idealities. The chosen network uses two off-chip components; a capacitor and an inductor, the specifications of which will determine the accuracy

of the initial graphical approach. The fact of not being restricted by the utilization of on-chip library models allows for a greater availability in terms of components selection. Among the different specifications, the search shall prioritize quality and tolerance as a matter of performance maximization.

As commented in section 3.3.2, wire bonding is still used in more than 90% of the package assemblies, so the presented solution will incorporate its parasitic inductance. One of the advantages of the chosen matching network is precisely the integration easiness of the bonding inductance in the design. Assuming 1 nH per millimetre of wire, a total of 3 nH is assumed. According to the previous analysis and accounting for the additional bonding inductance, the value of the series off-chip inductor may be comprised within the 6nH-10nH range. Proper election of this component greatly determines the overall outcome, so the most appropriate inductor is first detected and the rest of the components are then accommodated to the chosen model.

The impact of the matching inductance L_{match} in the design is of major importance. Besides its inductance value, a low-quality inductor presents a high parasitic resistance $R_{L_{match}}$, as 3.28 shows. This resistance creates thermal noise, which appears directly at the amplifier's input. Therefore, the output noise contribution is the result of the input thermal noise amplified by the gain of the LNA.

$$R_{L_{match}} = \frac{\omega_0 L_{match}}{Q} \tag{3.28}$$

Attending the portfolio offered by electronic components manufacturers [7][19], the inductor can be selected according to its characteristics. First, the inductance value must roughly match the theoretical derivation. It is not critical if the exact value is not satisfied since all components present certain deviation from the ideal behaviour, while fine adjustment is more easily achieved by on-chip components due to their reduced dimensions. Also, it is worth noticing that, at high frequencies, the inductance may significantly differ from the nominal stated value.

Probably the most critical feature that determines the resulting performance is the quality factor of the inductor. As shown in 3.28, it is extremely important to have a high quality factor which permits decreasing the parasitic resistance and its derived thermal noise at the input of the LNA. Precisely, the main advantage of using an off-chip inductor against its integrated counterpart is the achievable quality factor.Chapter 2 mentioned the performance of the on-chip inductors offered by the library. Apart from reaching inductances below 8 nH, the maximum quality factors approached values between 11 and 12, whereas commercial off-chip inductors easily achieve values greater than 40.

Due to the frequency of operation, the chosen inductor must also feature a high self-resonance frequency, in our case at least near 5 GHz, or above. Also, a tight tolerance is desirable to avoid excessive dispersion. And last but not least, the size of the inductor should be as small as possible.

Coilcraft is a manufacturer of electronic components specialized in the design of all kinds of inductors, including radio-frequency magnetics. Among its broad portfolio the air core inductors provide exceptionally high quality factors by virtue of their air wound coil as well as tight tolerances, while still combining a surface

mount design which allows for automatic placement reducing the assembly costs. The model which fits the target inductance range and provides the highest quality factor together with minimum tolerance is the A03T from the Mini SpringTM air core inductors family [5]. The specified quality factor of this component at 2.45 GHz is 408.91, nearly 40 times higher than the maximum provided by the most optimal integrated inductor.Table 3.2 summarizes the specifications of the chosen inductor. It is worth noting the reduced dimensions of the component as well as the excellent tight tolerance which severely reduces the chances of circuit tuning. In case size was a key determining factor, the 0908SQ-8N1 model from the Small Square family [6] would be a solid proposal at the expense of having greater variability due to the increased tolerance.

The chosen family of capacitors in this case is the Accu-P from AVX manufacturer [2], which uses a thin-film technology in contrast to the typical fired-ceramic reducing component variability in order to exhibit nearer ideal characteristics. The main features of this family of capacitors include high quality factors, extremely small sizes and very tight tolerances, so they are ideal for this application. The exact component which better fits the simulation using the A03T inductor model is the 02013J3R2ABSTR, whose characteristics are summarized in Table 3.2. Finally, a second shunt capacitor is used at the input of the amplifier in order to finely adjust the matching to the selected components.

Table 3.2: Off-chip matching network components specifications.

	Inductor	**Capacitor**
Part Number	A03T	02013J3R2ABSTR
Value @ 2.45 GHz	8.77 nH	3.72 pF
Q @ 2.45 GHz	408.91	76
Tolerance	1%	50 pF
Length	3.95 mm	0.60 mm
Width	4.45 mm	0.33 mm
Height	3.15 mm	0.23 mm
Price @ 1000	0.49€	0.19€

Figure 3.23 shows the complete LNA design featuring the amplifier core together with the matching network and the pad parasitics. L_{match} and C_{match1} correspond to the off-chip matching network, L_{bond} represents the parasitic inductance of the wire bonding, C_{pad} models the parasitic capacitance due to the pad and C_{match2} is an on-chip capacitor which provides the final matching adjustment.

Probably the reader may not visualize the actual appearance of the proposed solution. For the purpose, Figure 3.24 presents a 3D PCB perspective of a 3 cm by 2 cm PCB including two TQFP packages of 32 and 64 pins together with the components which comprise the matching network. As a reference, a typical 1/4W through-hole resistor demonstrates the reduced dimensions of the system.

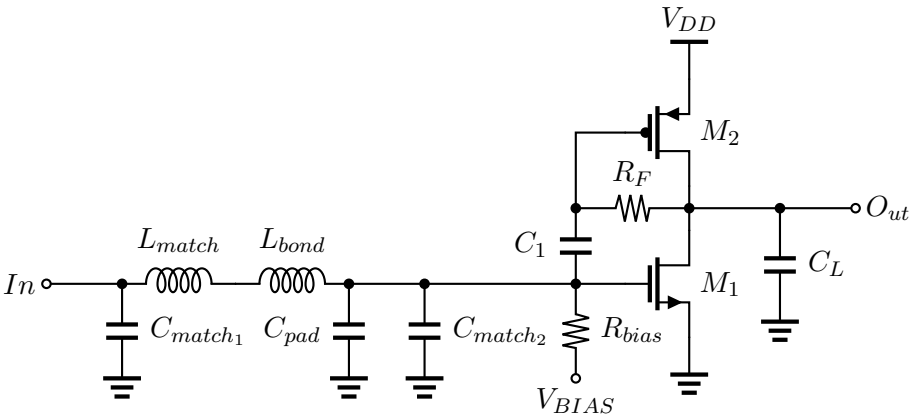


Figure 3.23: Complete current-reuse LNA with matching network.

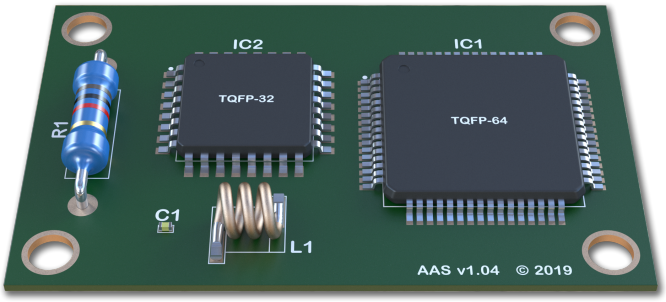


Figure 3.24: 3D exposition of a PCB including two TQFP integrated circuit packages of 32 pins (IC1) and 64 pins (IC2), the proposed matching network with the capacitor (C1) and inductor (L1) and a 1/4-Watt resistor (R1) included as a size reference. The dimensions of the PCB are 3 cm by 2 cm.

3.4 Results

Final results are provided in Table 3.3. The first two columns represent a pad-less scenario operating at nominal and ULV supply conditions, while the third one includes the effects of the pad and wire bonding. The pad-less scenarios are mainly exposed as a matter of comparison between the nominal and ULV environments. Thus, unless otherwise specified, any forthcoming result will correspond to the ULV scenario including the pad and bonding.

The reported Figure of Merit (FoM) combines the most important characteristics in any LNA design [10]: gain, noise factor and power consumption.

$$FoM = \frac{|S_{21}| f_{0_{GHz}}}{(F-1)P_{mW}} \tag{3.29}$$

The results obtained at $V_{DD} = 1\,\text{V}$ respond to the initial expectations. The design shows a gain near 30 dB and a noise figure below 3 dB, with acceptable input matching. More interestingly, the designs using $V_{DD} = 350\,\text{mV}$ provide excellent performance as well: both gains are near 24 dB, noise figures kept well below 3 dB and input matching is maintained while consuming only 10.5 µW. In contrast with the values presented in Table 3.1, the proposed circuit efficiently supersedes the source-degenerated topology, which shows gains below 14 dB, noise figures above 5 dB and greater power consumption. As a downside, the current-reuse LNA does not allow the same V_{DD} reduction, and requires an off-chip gate inductor.

Figures 3.25, 3.26, 3.27, 3.28 and 3.29 show the performance of the ULV-ULP design including the effects of the pad's parasitics. The power gain, represented by S_{21} parameter, reaches a maximum value of 24.4 dB at the working frequency 2.45 GHz. The designed matching network permits having an input matching value, represented by S_{11}, below −30 dB. Moreover, the LNA presents an excellent noise figure below 3 dB over the entire frequency range, with minimum at 2.04 dB. The fact that the minimum noise figure and the actual noise figure of the circuit are very similar at the operating frequency involves that the design has been properly optimized in terms of this parameter. The output to input isolation S_{12} is well below −40 dB, and the output matching represented by S_{22} is kept below −13 dB. Finally, the amplifier is unconditionally stable given that $K_f > 1$ and $B_{1f} > 0$ over the entire frequency range.

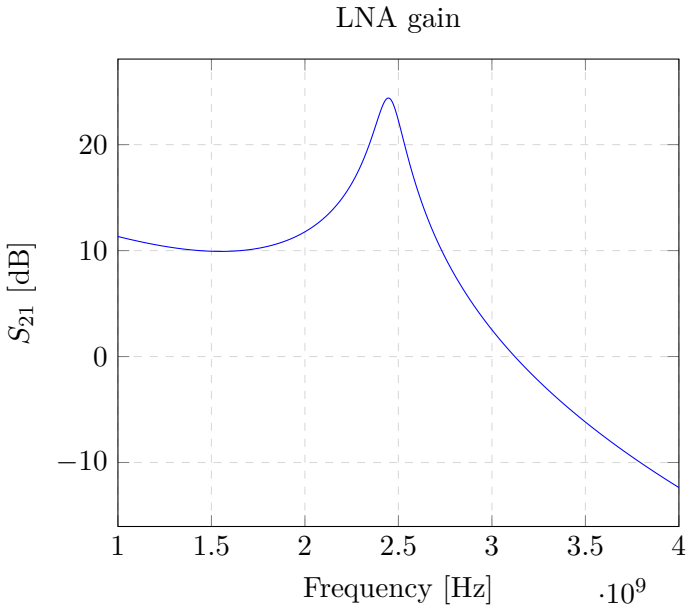


Figure 3.25: S_{21} parameter.

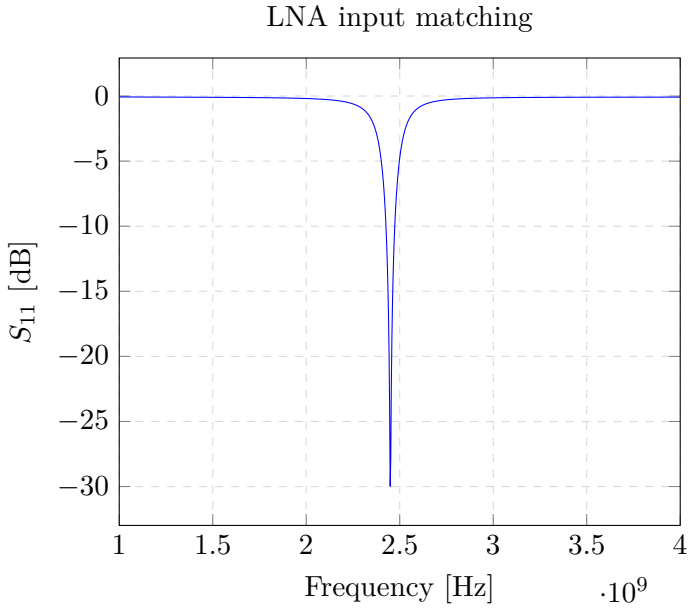


Figure 3.26: S_{11} parameter.

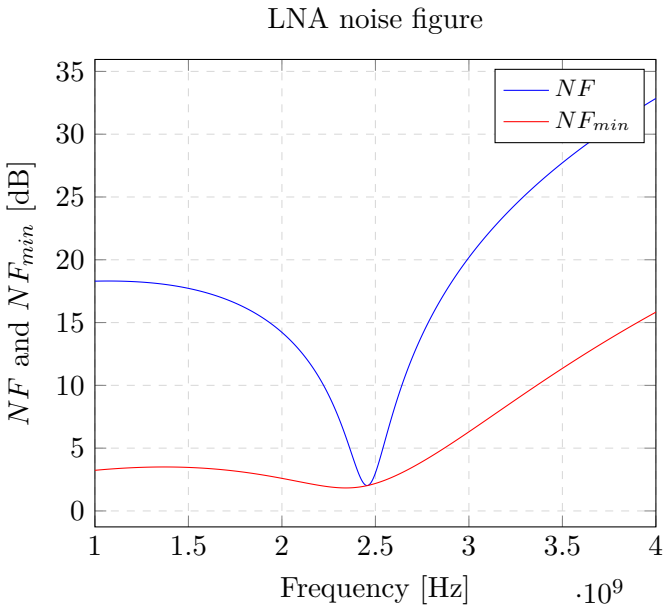


Figure 3.27: NF and minimum NF parameters.

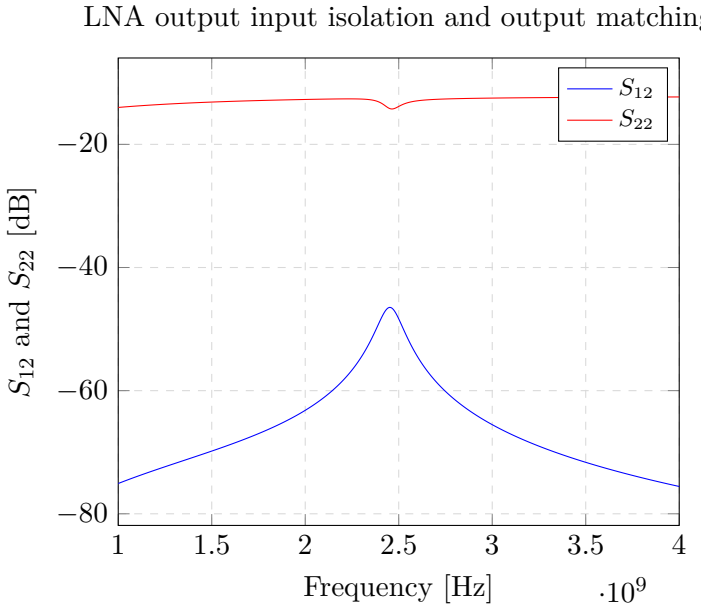


Figure 3.28: S_{12} and S_{22} parameters.

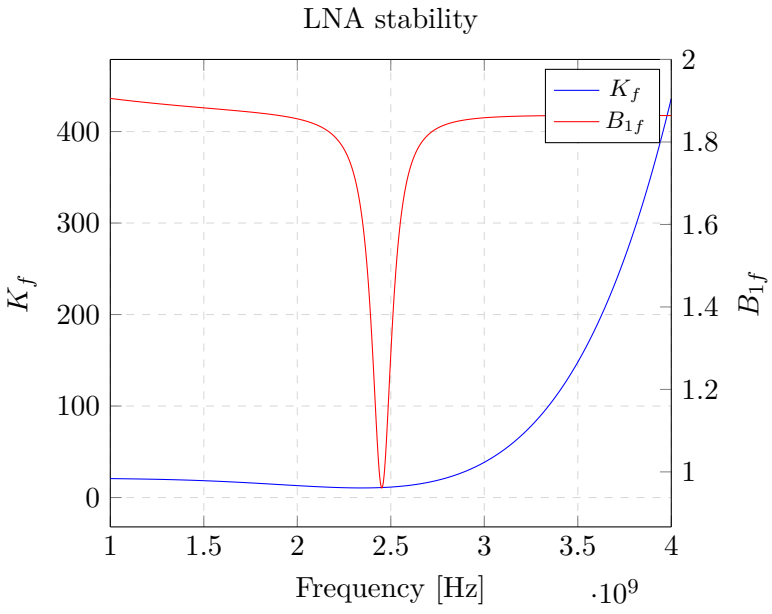


Figure 3.29: K_f and B_{1f} stability parameters.

Table 3.3: LNA design values and results at nominal and ULV supplies.

Circuit values			
V_{DD}	1 V	350 mV	350 mV
FBB	No	Yes	Yes
Pad + Bonding	No	No	Yes
V_{BIAS}	350 mV	350 mV	350 mV
NMOS Width	1.20 µm	0.90 µm	0.90 µm
PMOS Width	7.20 µm	24.60 µm	24.60 µm
R_F	100 kΩ	100 kΩ	100 kΩ
L_{match}	31.91 nH	32.91 nH	8.77 nH
C_{match1}	-	-	3.72 pF
C_{match2}	52.13 fF	41.15 fF	48.80 fF
DC Performance			
IDC	30 µA	30 µA	30 µA
g_{mN}	468 µA V^{-1}	434 µA V^{-1}	434 µA V^{-1}
Power	30 µW	10.50 µW	10.50 µW
RF Performance			
f_0	2.45 GHz	2.45 GHz	2.45 GHz
S_{11}	−10.20 dB	−24.60 dB	−31 dB
S_{21}	27.80 dB	23.60 dB	24.40 dB
NF	2.15 dB	2.15 dB	2.04 dB
FoM	3133	5582	6453
IIP3	-	−21.46 dBm	−16 dBm

3.5 Conclusions

The design of the low noise amplifier (LNA) has been explained in this chapter. First, a brief introduction to typical LNA topologies has been provided, addressing in more detail the well-known inductively degenerated common-source amplifier and its operation under ULV conditions. Then, the analytical behaviour of the chosen LNA topology has been derived. During the design methodology, the RF figure of merit has been employed as the biasing approach to optimize the performance-consumption trade-off. Two different design approaches have been commented under nominal and ULV supply conditions, deducing the necessity to apply FBB when low supply voltages are used. Then, the development of a matching network which accounts for the parasitics introduced by the package has been presented. Both analytical and graphical methods have been employed in order to choose the most optimal network while preserving simplicity as a matter of design robustness. Finally, simulation

results have been shown in Section 3.4. The typical LNA performance metrics such as gain, noise figure and matching have been reported for the chosen design.

According to the provided results, the designed LNA has been successfully migrated to a very low supply scenario while being able to maintain overall performance by virtue of the implementation of the FD-SOI technology. The final design features the highest figure of merit (3.29), which is defined in accordance to the main target to be achieved; that is, low power. Therefore, it is a solid alternative for the development of future ULV-ULP devices.

Chapter 4

Sensitivity to Body Bias and Supply Voltage

In a scenario of IoT mote supplied from energy scavenging sources, non-constant environmental conditions would result in variable voltages generated, thus needing some kind of converter to stabilize supply voltage to the targeted value. As a consequence, we can expect V_{DD} voltage in the circuit to be non-constant, but have low-frequency variations around the targeted value. Similarly, body-bias voltages of 1 V generated from lower supply voltages will require some switching up-converter, therefore we can expect also some low-frequency ripple added to the body bias. In this section we target to analyse the effects of these low-frequency ripples present in either body bias or supply voltages, on the high-frequency signal of the circuit.

4.1 Introduction

4.1.1 Periodically Time-Varying Circuits

Radio-frequency (RF) circuits exhibit very particular characteristics that make them difficult to simulate using traditional SPICE transient analysis. As an example, consider a down-conversion mixer with a local oscillator frequency of 2 GHz and an intermediate frequency of 1 MHz. A SPICE transient analysis is extremely expensive for such circuits since it needs to take very small time steps to follow the 2 GHz fundamental, and simulate for a long time to adequately resolve the intermediate frequency.

Baseband circuits can be linearized about their DC operating point and a small-signal analysis is used to efficiently determine the sinusoidal steady-state response of the circuit. The circuit is expected to respond in a near-linear fashion to an input signal while operating about a DC operating point, which implies that the solutions computed by the analysis contain only sinusoids at the same frequency as the input signal, that is, frequency translation does not occur. However, some circuits, such as mixers, are specifically designed to translate signals from one frequency to another. To do so, they are driven by a large periodic signal the magnitude of which determines

the amount of frequency translation [15].

Probably the easiest example to particularize a large signal-driven circuit is a mixer. The large signal is the local oscillator (LO) and it is independent of the information signal, so it may be considered as part of the receiver circuit rather than an input to it. This approach permits having a single input and a linear, though periodically time-varying, transfer function. Assuming that the mixer is an ideal multiplier, when an input signal $x(t) = \cos(\omega_c t)$ is applied to the system, the outcome becomes multiplied by the LO signal.

$$y(t) = x(t)\cos(\omega_{LO}t) = \cos(\omega_c t)\cos(\omega_{LO}t) = \frac{1}{2}[\cos(\omega_c - \omega_{LO})t + \cos(\omega_c + \omega_{LO})t] \tag{4.1}$$

which is easily demonstrated to be linear with respect to the input $x(t)$, but also time-variant. Assuming a low-pass filtered output and neglecting the amplitude modulation the output signal may be re-written as

$$y_{LPF}(t) = \cos(\omega_c - \omega_{LO})t \tag{4.2}$$

It has thus been demonstrated that a linear periodically varying transfer function implements frequency translation.

Apart from mixers, there is a wide variety of other circuits for which these assumptions apply, such as samplers, switched-capacitor filters, phase detectors, etc. Other circuits do not strictly require a large clocking signal to operate but may also be included as per the influence of high-amplitude noises, like the ripple effect in the body bias and supply voltage on the LNA presented in this work.

Conventional small-signal analyses like AC and noise linearize about a DC operating point to create a linear time-invariant representation of the circuit, which cannot exhibit frequency conversion effects. According to the previous argumentation, large-signal driven circuits do not fit this time-invariant representation and thus require the traditional small-signal analyses to be extended in a way that the circuit is linearized about a periodically varying operating point such that frequency conversion effects are exhibited.

Baseband circuit designers are provided with different types of SPICE analyses which include DC, AC, noise and transient. Similarly, RF designers need the same analyses but must be extended to address the issues described so far. The RF versions of those basic SPICE analyses are based on two different simulation engines: harmonic balance and shooting method. Both methods started by simply providing the periodic steady-state solution of a circuit but have already been generalized to support all functionality required by RF designers [15].

4.1.2 Periodic and Quasi-Periodic Analysis

Periodic and quasi-periodic analysis can be thought of as the RF extensions of SPICE DC analysis. In a DC analysis the steady-state solution is computed upon the application of constant voltages and currents to the circuit, which defines the

point about which subsequent small-signal analyses are performed. With periodic and quasi-periodic analyses, the circuit is driven with one or more periodic signals and the steady-state response is computed. The result is a period or quasi-periodic operating point used for the subsequent small-signal analysis.

When a single large periodic signal is applied, the steady-state response features a discrete spectrum with frequency components at the drive frequency and its harmonics. If two or more periodic signals are applied, then the spectrum shows components at the drive frequencies, at their harmonics, and at the sum and difference frequencies of the drive frequencies. These signals are called quasi-periodic and apply to circuits such as mixers with multiple LO frequencies or large RF inputs.

The following sections will briefly introduce harmonic balance and shooting simulation engines, which are used to obtain the periodically varying operating point of the circuit. In order to facilitate the reading, the mathematical fundamentals will be skipped but a simple yet intuitive qualitative approach will be provided.

Harmonic Balance

Harmonic balance method solves the circuit equations in frequency domain rather than solving in time domain. It calculates the harmonics and mixing products of one or more inputs to the circuit taking into account all the large-signal effects. The solution is provided after an iterative process where each successive iteration produces a more accurate outcome. Recent simulators run a short transient analysis prior to the harmonic balance algorithm with a small number of periods of the fundamental frequency as the stop time. As the transient runs, the waveform is analysed until steady-state is reached, which is used as the starting point of the harmonic balance iterations. Even though the engine is based on frequency-domain computations, nonlinearities need to be evaluated in the time-domain using the FFT and the IFFT to translate between the domains.

The accuracy of the harmonic balance is mainly determined by the number of harmonics required to cover the signal bandwidth of interest. When too few harmonics are used, the spectrum outside the maximum harmonic is folded back into harmonics inside the plotted solution producing aliasing effects. Due to the nature of the IFFT and FFT, non-sinusoidal waveforms usually require a large number of harmonics to correctly recover the time-domain waveform. If time-domain accuracy is not necessary, though, an oversampling factor greater than 1 may be specified to relax the number of harmonics computed. For example, let's consider the case where we are only interested in the first harmonic of a square wave signal. Since higher order harmonics are not important, we may simply specify to compute 2 harmonics using an oversample of 4 or 8. In such case, the IFFT would definitely show a far from perfect square wave, given that only 2 harmonics were specified, but the spectrum value at the first harmonic would be very precise.

Harmonic balance is very efficient for simulating weakly nonlinear circuits such as LNAs or Gilbert cell mixers since few harmonics are needed to accurately represent the time waveform. For highly nonlinear systems with sharply rising or falling signals like sample-and-hold or switched-capacitor filter many frequencies are needed to

accurately represent the signal, which increases the expense of harmonic balance. In these cases the time-domain shooting method is usually more appropriate. However, harmonic balance may still provide a significant advantage during early design explorations using few harmonics if high accuracy is not a major concern.

Shooting Method

The shooting method is a time domain method that operates by finding an initial condition that directly results in steady state as defined by $v_f - v_i = \Delta v = 0$, being v_f the final value and v_i the initial value. The nonperiodicity Δv and the sensitivities of the final state v_f with respect to the initial state v_i are used to compute a new initial condition. The new initial condition results in periodicity when the final state is a linear function of the initial state. Otherwise, additional iterations are needed.

If the computed final state after one period is a near-linear function of the initial state, then few iterations will be required. This is generally true even for circuits that behave in a strongly nonlinear fashion to large stimuli. The shooting method integrates over a whole number of periods of the stimulus, which minimizes the nonlinearity in the relationship between the initial and final state and minimizes the number of iterations needed for convergence.

The main advantage of the shooting method over harmonic balance is its ability to follow abruptly discontinuous waveforms by placing time points in a nonuniform manner during transient analysis. The fact that the error is controlled choosing nonuniform timesteps allows for greater convergence capabilities [15].

Shooting methods has fallen into disuse given that they are prone to become slow when used on larger problems. This is so because the engine forms an N-by-N sensitivity matrix, where N is the number of equations that are required to represent the circuit. The algorithm requires at some point to compute the inverse of that matrix, which involves N^3 operations. Thus, the algorithm is impractical for larger circuits due to the computational complexity.

4.1.3 Periodic Small Signal Analysis

The engines presented in the previous chapters provide a large-signal solution to the subsequent small-signal analysis. Thus, periodic small-signal analyses address periodically-driven circuits using a two-step process. First, the time-varying operating point is found with the periodic analysis where the signal that causes the most distortion in the circuit is applied (for example, the LO in a mixer). Then, the circuit is linearised but about the periodic operating point and the steady-state response of the periodically-varying linear circuit is computed assuming that it is driven with a small sinusoid.

Periodic AC Analysis

The periodic AC analysis (PAC) computes the responses of a periodically driven circuit to a small sinusoidal input. The concept is the same as a small-signal AC analysis, except that the circuit is first linearised around a periodically varying

operating point rather than a simple DC operating point, so frequency conversion effects can be observed. When applying a small sinusoid to a linear time-invariant circuit, the steady-state response is a sinusoid at the same frequency. However, when applying a small sinusoid to a linear periodically time-varying circuit, the circuit responds with harmonics.

The Periodic AC analysis computes the different transfer functions that result from mixing the input signal with the harmonics of the periodic steady-state solution due to the large-signal. The mixing products that are produced are called sidebands. The sideband number is the harmonic number that is being mixed with to provide the output. Like an AC analysis, the small-signal effects of the input can be measured at the desired output node. In other words, the transfer functions are calculated from the input node to any output node.

The output spectrum components that result after a periodic AC analysis can be evaluated by

$$f_{out,K_i} = f_{in} + K_i PSS_{fund} \tag{4.3}$$

where f_{in} is the input frequency (which may be a swept range), K_i are the PAC sidebands and PSS_{fund} is the periodic steady-state fundamental frequency specified in the large-signal analysis

Figure 4.1 shows the small-signal response of a theoretical down-conversion mixer, where the input signal is just above the fundamental LO frequency. As it can be observed, the input signal is replicated and translated by each harmonic of the LO, which contains information about how strongly the circuit translate frequencies. In this case, the -1 sideband corresponds to the IF output.

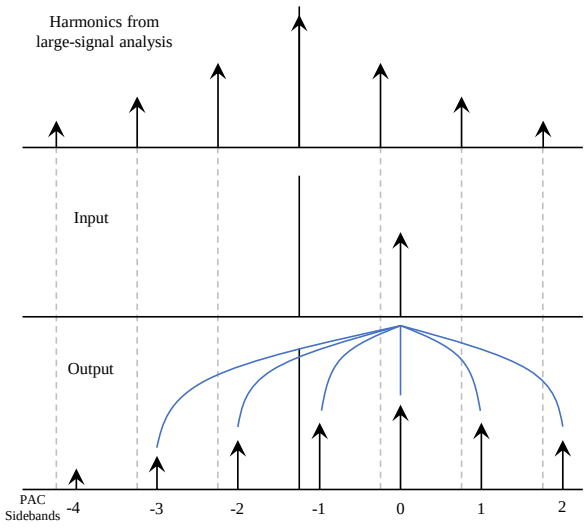


Figure 4.1: Small-signal periodic AC response.

Periodic Transfer Function Analysis

The periodic transfer function (PXF) analysis computes the transfer function from every source in the circuit and frequency to a single output and frequency. Whereas PAC analysis provides the response at all points in the circuit and all frequencies due to a small-signal input applied to a particular point at a particular frequency, PXF analysis does the reverse by computing the transfer function from any input to a single output at a given frequency. First, the large-signal analysis calculates the harmonics of the input that causes the frequency translation to occur and then the periodic transfer function runs to calculate the different conversion gains based on the nonlinearity in the large-signal analysis solution.

PXF differs from the typical procedure of driving an input and then measuring what comes out. In PXF, the output node and output frequency range in the circuit are first specified. Then the analysis determines the input frequencies that will contribute to that output, and finally measures the conversion gains from all the sources in the circuit to the output previously defined. In this way, a single output response is the combination of all possible frequency components in the design.

The input frequency components that are computed by the PXF analysis are

$$f_{in,K_i} = f_{out} + K_i PSS_{fund} \tag{4.4}$$

where f_{out} is the input frequency (which may be a swept range), K_i are the PXF sidebands and PSS_{fund} is the periodic steady-state fundamental frequency specified in the large-signal analysis

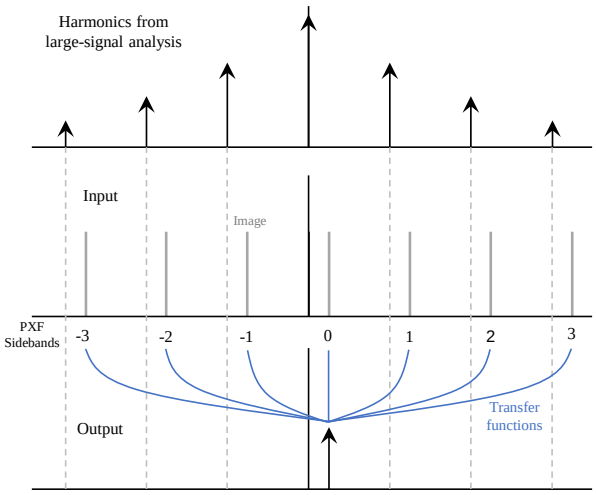


Figure 4.2: Small-signal periodic transfer function response.

Figure 4.2 shows the small-signal response of a theoretical down-conversion mixer as computed by PXF analysis, where the desired output is at low IF. As it can be observed, PXF computes all inputs that contribute to the specified output. A useful

advantage of PXF is the ability to compute both the passband (input sideband 1 in the example) and the image (input sideband -1 in the example) conversion gains at once.

Periodic Noise Analysis

The periodic noise analysis (Pnoise) characterizes the noise figure of circuits that are linearised around a periodically time-varying operating point. As the input power level increases, the circuit becomes nonlinear, harmonics are generated, and the noise spectrum is folded.

The procedure followed is the same as the PAC and PXF analyses. First, the circuit response to a large periodic signal is computed such that different harmonic levels can be calculated. In the second step, the Pnoise analysis runs in a similar way than linear noise except the frequency translations of the circuit are taken into account. Each noise source has now several contributions at the output from several different noise frequencies, so both the amplitude of the noise and the gain for the noise sources at the large-signal harmonics needs to be calculated. Pnoise uses the nonlinearity of the circuit and the amplitude of the harmonics that are present to mix with and calculates the transfer functions from all the frequencies for each noise source. Next, it calculates the total noise power at the output by adding up all the noise frequencies that contribute at the output from all the sources.

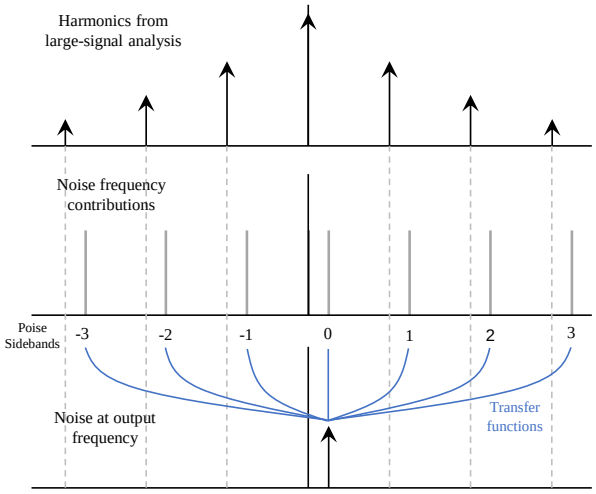


Figure 4.3: Small-signal periodic transfer function response.

The diagram in Figure 4.3 shows the noise output frequency and the various mixing paths due to the large signal harmonics. The first graph represents the harmonics that are calculated by the large-signal analysis. The middle represents all the frequency locations where noise sources can contribute to the total output

noise, which is shown at the bottom axis. In this case a single output frequency is represented, although usually a range of frequencies will be more interesting.

4.2 Body Bias Generator

FD-SOI is a suitable technology for near-threshold powered devices due to its high range of body bias voltages, as discussed in Chapter 2. The LNA presented in this work applies forward body bias of ±1 V in order to boost performance at low supply. Thus, a circuit able to generate voltages higher than the supply is needed. An attractive solution is the charge pump bias generator, which features a switched-capacitor architecture that makes it very suitable to be implemented in integrated circuits. [4] presents the design of a charge pump-based body-bias generator implemented in the current 28 nm FD-SOI technology with a power consumption below 10 µW. Besides the capability to boost the voltage, another benefit is the fine resolution through incremental step responses on the threshold voltage, which permits employing the body-bias generator as an active tuning variable. Due to load leakage, though, the generated voltage shall be maintained in a charge-discharge basis,as shown in Figure 4.4. The reported recharge time is 1 ms for the n-well and 0.2 ms for the p-well, which corresponds to a ripple effect of 1 kHz and 5 kHz with amplitudes below 90 mV and 40 mV, respectively. In order to have a safe margin between the specification and different load conditions, 100 mV ripple amplitude has been employed.

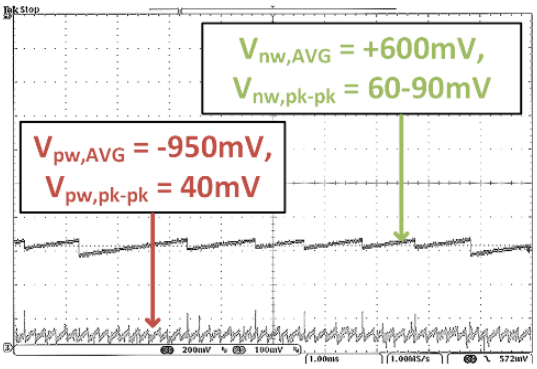


Figure 4.4: Body bias voltage ripple due to charge pump-based circuitry. Image taken from [4].

As a summary, the body bias voltage is not a pure DC signal but has a ripple superimposed. Taking into account that the useful signal received by the LNA is harshly attenuated, a noisy signal with several tens of millivolts may impose a non-negligible interference that needs being specifically evaluated using the tools provided in the previous chapters. Moreover, not only the body bias voltage but also the power supply would be presumably generated using the same charge pump circuitry. The specific charging-discharging times are not characterized in [4] for a theoretical power supply generation, so the same 1 kHz ripple will be assumed.

4.3 Evaluating the Effect of Ripple on Supply and Body Bias voltages

The evaluation of the body bias and power supply interference cannot be addressed using the typical small-signal approach. Due to the large ripple, circuit's nonlinearity emerges as a series of harmonics (see Section 4.1.1), which determine the amount of frequency translation.

The target of this analysis is to quantize the effects of the body bias and power supply ripple on the output of the LNA at the operating frequency 2.45 GHz. The following Section evaluates the analysis restrictions under such scenario and the necessity to choose an arbitrarily larger ripple frequency. Note that, since the magnitude of harmonics decreases as its order increases, the effects of a the low-frequency ripple are expected to be a tiny fraction of those observed for a ripple at larger frequencies. After that, a second analysis will quantize the ripple effects on the mixer input up to 1 MHz, which could easily represent an IF. In this case note that the real ripple frequency can be used as the number of harmonics required is more affordable than the previous analysis.

For both analyses, the time-varying operating point is first found with the periodic steady-state analysis where the signal that causes the most distortion in the circuit is applied. In this case, the large signal is the body bias or power supply voltage. The engine chosen to compute the periodically time-varying operating point is harmonic balance as it is very efficient for simulating weakly nonlinear circuits such as LNAs given that few harmonics are needed to accurately represent the time waveform.

Since the large signal that excites frequency conversion effects is not a pure tone but pulse-type, to correctly represent its spectrum we must use a reasonable number of harmonics and an oversample factor greater than 1. A proper methodology starts with a committed number of harmonics; for example, the minimum that are required for the application. Once the spectrum has been obtained, a second iteration would be performed specifying a larger number of harmonics. If the solution changed, probably the original estimate is not enough and a higher number of harmonics are needed to properly represent the desired spectrum. The process continues until the outcome does not differ in a great extent from the previous one, in which case the oversampling factor may be increased in order to relax the number of harmonics and speed-up the simulation.

4.3.1 Impact of Body Bias Ripple and Supply Voltage on LNA Output at 2.45GHz

The fundamental frequency of body bias and supply ripple is 1 kHz. Due to nonlinearities in the circuit, harmonics of the fundamental originate. If we want to evaluate the effects from the body bias or supply voltage at 1 kHz to the LNA output node at 2.45 GHz we need to at least calculate all necessary harmonics up to the specific one which performs the desired translation. That is, the required harmonic frequency is $-2.45\,\text{GHz} + 1\,\text{kHz}$, which corresponds to the harmonic number $|-2.45\,\text{GHz} + 1\,\text{kHz}|/1\,\text{kHz} = 2449999$, as the sketched scenario in Figure 4.5

shows. In other words, more than 2 million harmonics are required to be computed, which is too demanding in terms of CPU and memory resources. Therefore, a value 1 MHz is selected instead. In this case, the required harmonic frequency to push the fundamental up to the ISM band is $-2.45\,\text{GHz} + 1\,\text{MHz} = -2.449\,\text{GHz}$, for which a reasonable 2449 sidebands must be evaluated.

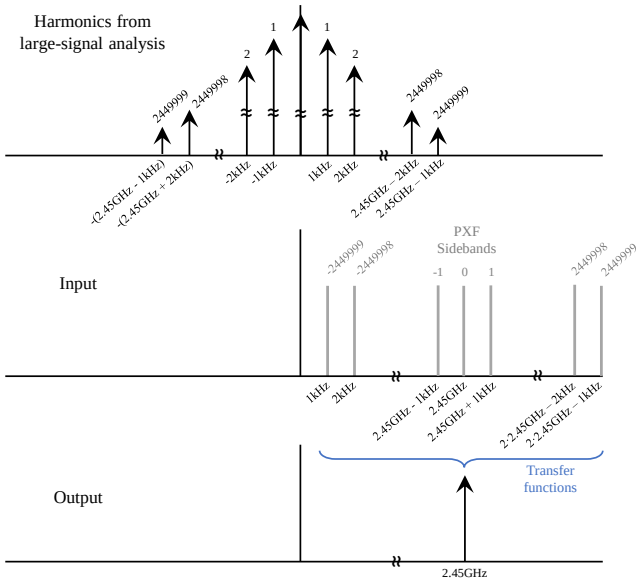


Figure 4.5: Small-signal periodic transfer function response of the low frequency ripple on the LNA output at 2.45 GHz.

Using a swept input ripple between 0 and 100 MHz, the sideband -2400 permits observing the transfer function at the 2.4 GHz – 2.5 GHz LNA output. Figure 4.6 show the transfer function from the NMOS body bias and the PMOS body bias to the LNA output. The gain in both cases is around −200 dB, which means that a 100 mV ripple would show as 10 pV at the 2.45 GHz output. In power units, 10 pV is around −210 dBm, well below the expected level of the signal at the LNA output.

Similarly, Figure 4.7 shows the transfer function form supply voltage to the LNA output. The gain from the fundamental harmonic is now around −130 dB, somewhat larger than the obtained in the body bias voltages. Even so, a 100 mV ripple would be translated into a 30 nV (approx.) output signal noise, still much lower than the output LNA signal. But note this is only the contribution of the main harmonic of the ripple.

One way to observe the total contribution of all input harmonics at the output node is to plot the power spectrum at this node. In Figures 4.8 and 4.9 we can see that the output harmonics between 2.4 GHz and 2.5 GHz barely exceed −160 dBm. As expected from the transfer function, the output harmonics due to supply voltage ripple are higher, although lower than −130 dBm as shown in Figure 4.10.

In order to assess the impact of the output harmonics, we can estimate the noise power expected at the LNA output.

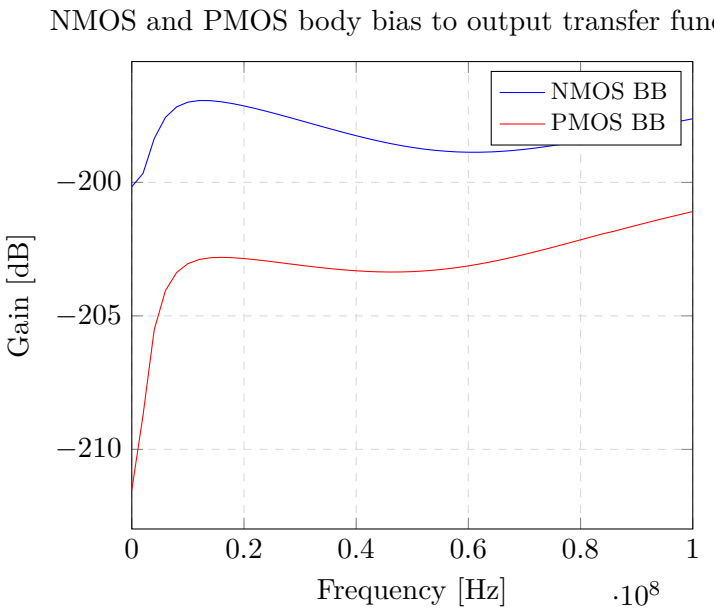


Figure 4.6: Periodic transfer function from 0 Hz to 100 MHz body bias input-swept to LNA output at 2.4 GHz to 2.5 GHz.

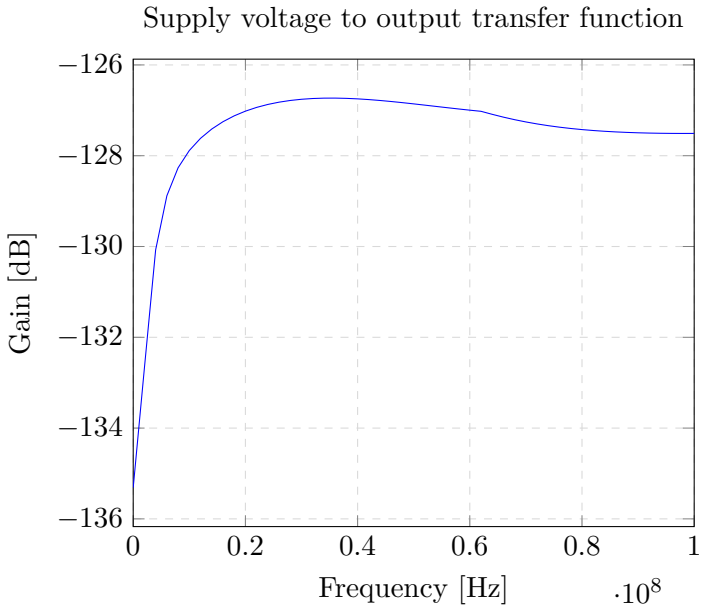


Figure 4.7: Periodic transfer function from 0 Hz to 100 MHz supply voltage input-swept to LNA output at 2.4 GHz to 2.5 GHz.

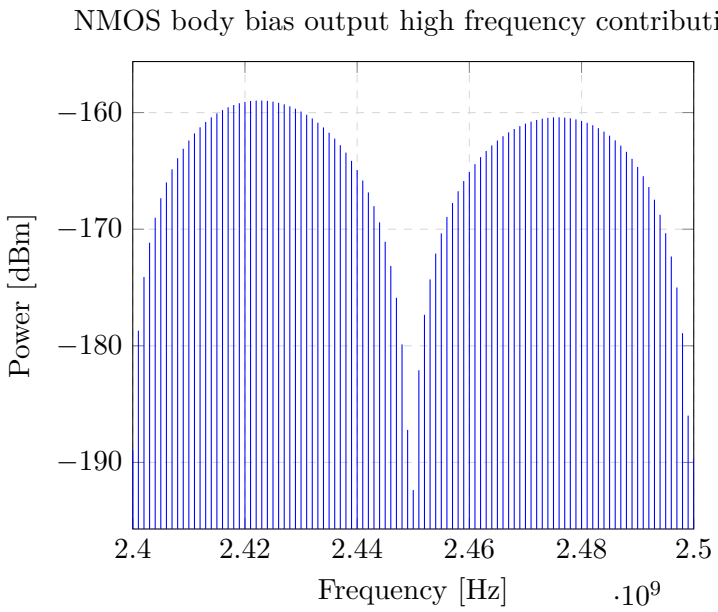


Figure 4.8: LNA output spectrum at the operating frequency range due to NMOS body bias ripple.

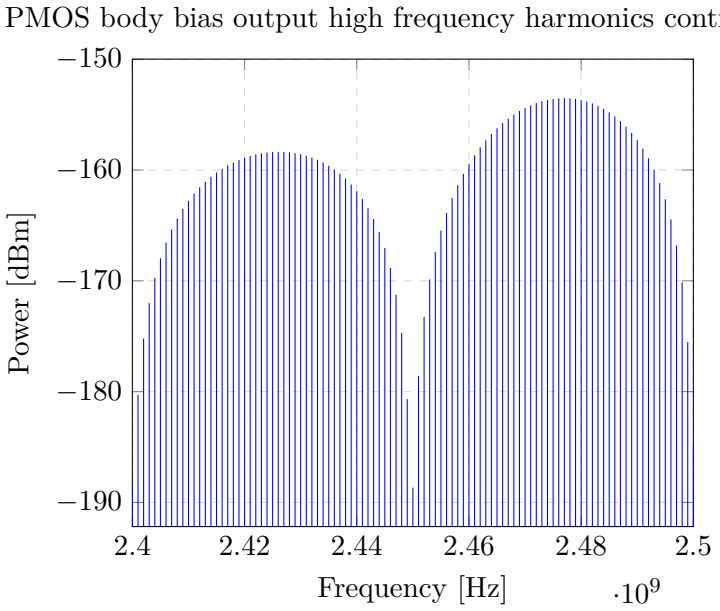


Figure 4.9: LNA output spectrum at the operating frequency range due to PMOS body bias ripple.

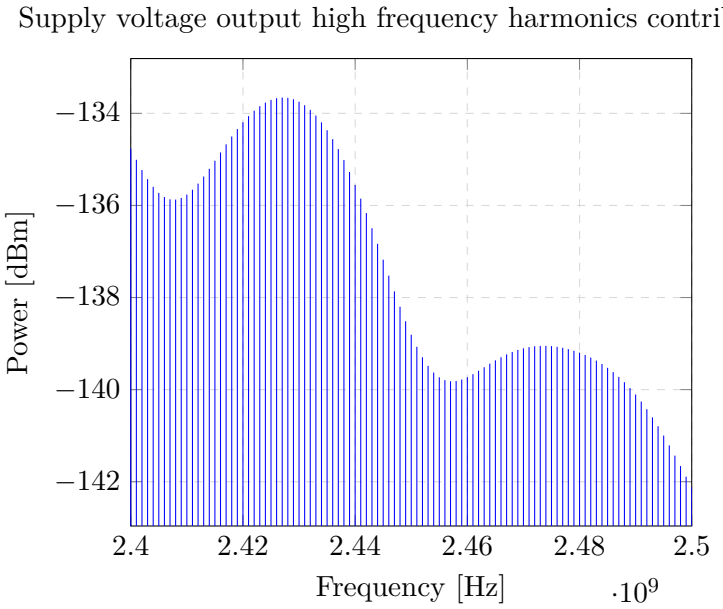


Figure 4.10: LNA output spectrum at the operating frequency range due to supply voltage ripple.

The noise factor of a circuit quantifies how much the signal-to-noise ratio (SNR) has worsened because of its internal noise. Besides the degradation in SNR, an alternative definition of the noise factor relates the total output noise and the noise at the output due only to the input.

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{S_{in}/N_{in}}{S_{in}A_v^2/N_{out}} = \frac{N_{out}}{N_{in}A_v^2} \tag{4.5}$$

where A_v stands for the voltage gain, S_{in} and S_{out} are the signal power at the input and output and N_{in} and N_{out} are the total noise powers at the input and output. The total output noise can be thus computed as

$$N_{out} = FN_{in}A_v^2 \tag{4.6}$$

Assuming equal source and load impedances, both voltage and power gains are the same. According to the LNA performance results, we can consider a voltage gain of 24 dB, or 15.8 in linear value.

At the receiver's input we will always have at least the thermal noise due to the antenna impedance. The noise generated by the antenna derives from its standardized resistance, 50 Ω in this case. It can be easily demonstrated that the thermal noise power of a resistor delivered to a matched load is

$$N_{match} = k_B T \Delta f \tag{4.7}$$

where k_B is Boltzmann's constant (about $1.38 \cdot 10^{-23}$ J/K), T is the absolute temperature in kelvins, and Δf is the noise bandwidth in hertz over which the measurement is made. Then, assuming a 1 MHz channel bandwidth and 290°K temperature, the noise power delivered by the antenna to the matched LNA is

$$N_{in}[dBm] = 10\log\left(\frac{k_B T}{1\,\text{mW}}\right) + 10\log(\Delta f) = -114\,\text{dBm} \rightarrow N_{in} = 3.98 \cdot 10^{-12}\text{mW} \tag{4.8}$$

The noise figure of the designed LNA is around 2 dB, which corresponds to a noise factor of 1.58. Finally, the total output noise can be computed.

$$N_{out} = F N_{in} A_v^2 = 1.57 \cdot 10^{-12}\text{mW} \rightarrow N_{out}[\text{dBm}] = -88\,\text{dBm} \tag{4.9}$$

As it can be seen, the contribution of the body bias and supply voltage ripple harmonics on LNA output at the working frequency range 2.4 GHz − 2.5 GHz is well below the noise level. We can thus expect that a further reduction on the ripple frequency (down to a realistic 1 kHz) would further minimize the effect since the magnitude of harmonics decreases as its order increases. The conclusion from the analysis is then that a 100 mV ripple in the body bias or supply voltage will show as an added noise to the output signal, but with negligible levels (well below the device noise levels), due to the extremely small conversion gains obtained from the low-frequency body and supply to the high-frequency output.

4.3.2 Impact of Body Bias Ripple and Supply Voltage on Mixer input

Having concluded that a low-frequency (around 1 kHz) body bias would show negligible up-conversion effects to the 2.45 GHz LNA output, we now check the contribution of this ripple to lower frequency components at the output node. Effectively, the LNA works at a much higher frequency and its usual operation will not become affected by those low-frequency components, yet possible near-IF components still appear at the input of the mixer and potentially couple directly to the output, thus overlapping the downconverted signal. For the purpose, we will evaluate the contribution up to 1 MHz, so a minimum of 1 MHz/1 kHz = 1000 harmonics shall be computed. It is worth noting that the number of harmonics is also enough for the PMOS ripple, which features a higher fundamental frequency (around 5 kHz).

The spectrums directly measured at the output due to the NMOS and PMOS body bias ripple are shown in Figures 4.11 and 4.12 up to 1 MHz. For the PMOS, the power at 100 kHz output is about −100 dBm, and decreases at an approximate rate of −40 dB per decade, thus resulting in negligible power at the frequency of 1 MHz and above. The noise contribution from the PMOS is larger, but still well below the expected signal at the LNA output.

The same exercise has been carried out for the supply voltage; whose result is shown in Figure 4.13. In this case, the power at 100 kHz output is about −100 dBm, and decreases at an approximate rate of −40 dB per decade, thus resulting (again) in negligible power at the frequency of 1 MHz and above.

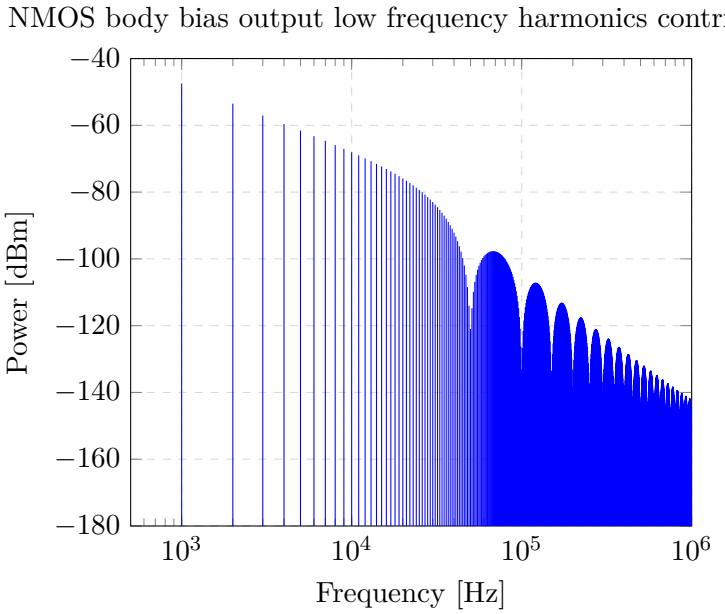


Figure 4.11: LNA output spectrum at low frequencies due to NMOS body bias ripple.

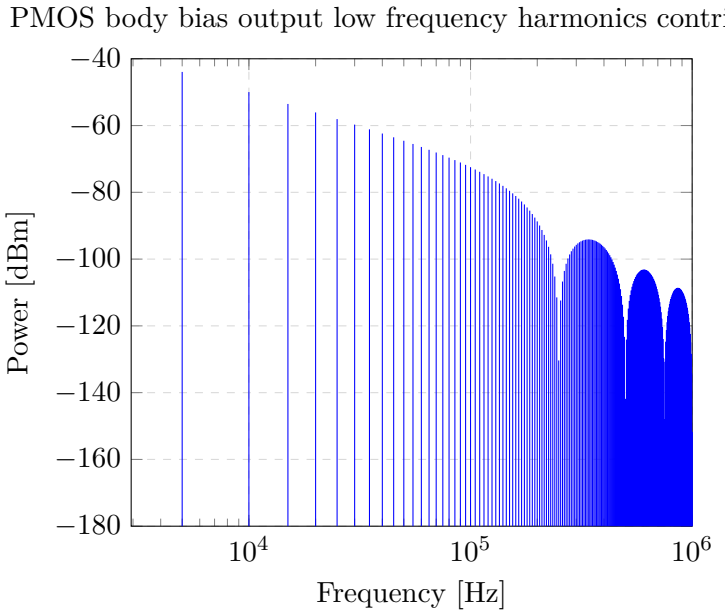


Figure 4.12: LNA output spectrum at low frequencies due to PMOS body bias ripple.

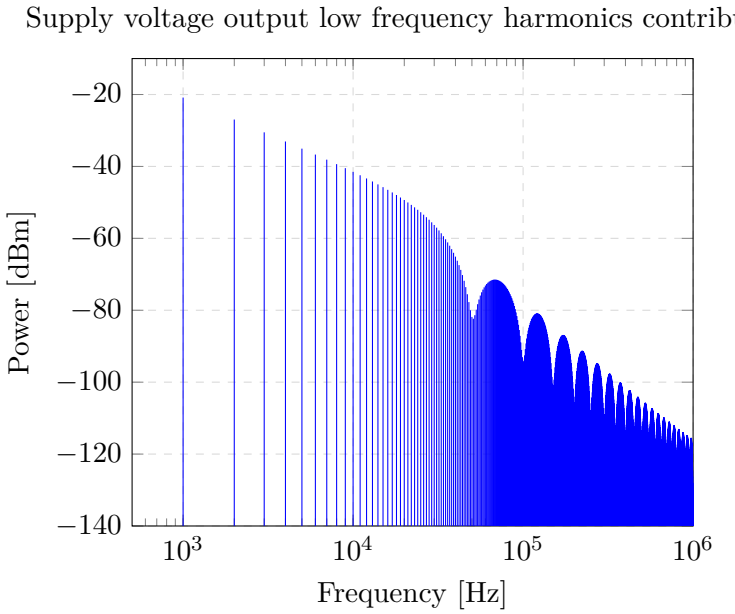


Figure 4.13: LNA output spectrum at low frequencies due to supply voltage ripple.

4.4 Sensitivity of DC Operating Point to Supply Voltage and Body Bias Variations

The above analysis has shown that, since conversion gain from a low-frequency input to the 2.4 GHz − 2.5 GHz output decreases as the frequency of the input decreases, and given the huge difference between input ripple frequency and the GHz output, negligible AC coupling is expected. But being a kilohertz-range ripple in the order (or significantly larger) than a symbol time, the effects of those low-frequency variations can effectively be perceived as low-frequency variations of the operating conditions during data reception. Thus, it will be more relevant to evaluate the sensitivity of the LNA to OP variations produced by Body Bias or supply voltage shifts respect to their nominal DC values.

Given that the supply voltage ripple has been assumed 100 mV peak-to-peak amplitude, we evaluate a $V_{DD} = 350\,\text{mV} \pm 50\,\text{mV}$ variation effect, as a consequence of the modification produced in the operating point. Also, in the designed LNA the bias voltage ($V_{BIAS} = V_{GN}$) would be directly taken from the V_{DD} value, thus can expect to suffer the same variations. As shown in Figure 4.14, the effects are relevant but not dramatic. LNA input matching is good enough in all cases, and worst-case values for S21 and NF are 20 dB and 2.8 dB, still producing outstanding FoM.

The effect of 100 mV peak-to-peak amplitude variations on body bias voltages have also been evaluated. Variations are assumed to be produced only in one transistor, i.e. $V_{BODY,N} = 1\,\text{V} \pm 50\,\text{mV}$ and $V_{BODY,P} = -1\,\text{V}$, or $V_{BODY,P} = -1\,\text{V} \pm 50\,\text{mV}$ and $V_{BODY,N} = 1\,\text{V}$. The effects of those variations on S_{11}, S_{21} and NF are very small.

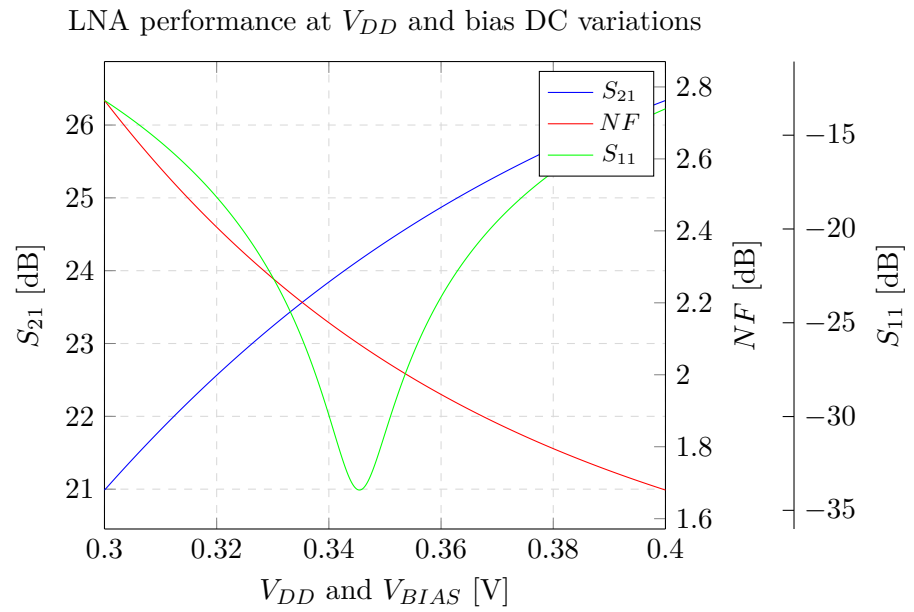


Figure 4.14: S_{21} and S_{11} and NF parameters upon supply voltage and bias DC variations.

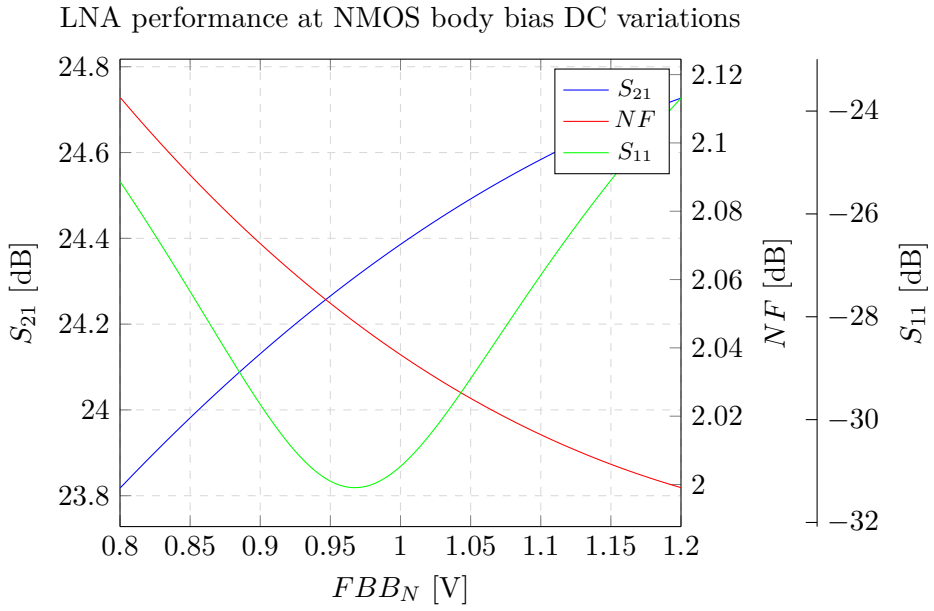


Figure 4.15: S_{21} and S_{11} and NF parameters upon NMOS body bias DC variations.

Simulations are repeated for an extended variability, i.e. $V_{BODY,N} = 1\,\text{V} \pm 200\,\text{mV}$ and $V_{BODY,P} = -1\,\text{V}$, or $V_{BODY,P} = -1\,\text{V} \pm 200\,\text{mV}$ and $V_{BODY,N} = 1\,\text{V}$. As shown

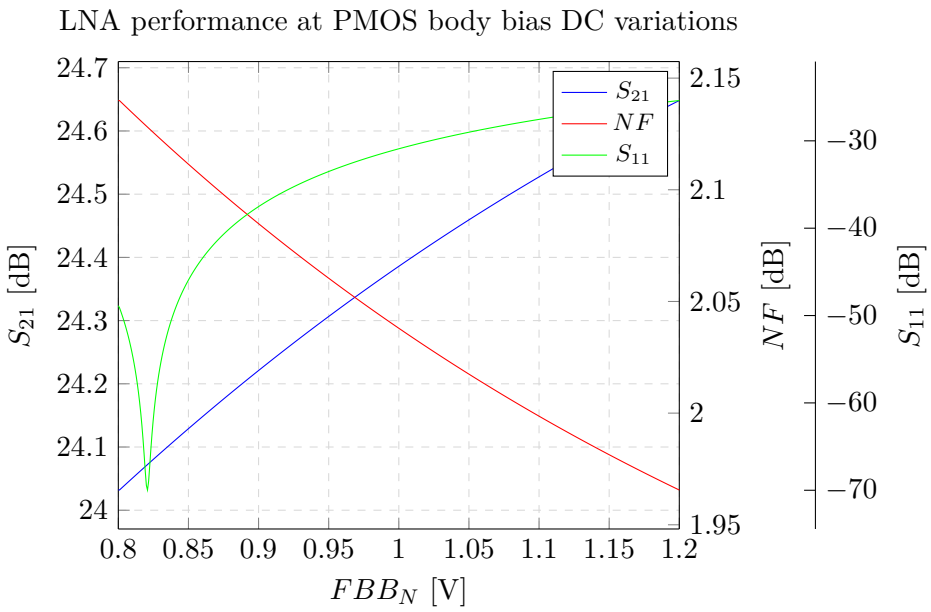


Figure 4.16: S_{21} and S_{11} and NF parameters upon PMOS body bias DC variations.

in Figures 4.15 and 4.16, even in this extreme scenario, the effect of this variability is well below than that produced when due to V_{DD} and V_{BIAS}.

A side consideration of these simulations results concerns the possibility to use FBB voltages different than nominal ones to compensate performance deviations due to PVT variability. The plots show that, given the low sensitivity of gain and NF to Body Bias, a large V_{BODY} tuning range would be required to compensate important deviations of LNA performance.

4.5 Conclusions

This chapter has addressed the evaluation of the potential interference in the LNA performance due to charge pump circuitry, which is used to boost the body-bias voltage beyond the supply of the circuit.

Throughout the simulations, different conservative approaches have been adopted. First, in order to cover different load conditions, the amplitude of the ripple interference has been set to 100 mV. Apart from the increased amplitude, the frequency of the ripple has also been significantly incremented due to the practical impossibility to perform simulations at a realistic frequency, which inherently means assuming a worst-case scenario. By shifting the ripple fundamental to higher frequencies, the influence of the harmonic components will be magnified in comparison to a more realistic low-frequency ripple. Finally, a large range of supply and body voltage variations has been assumed during the DC variability analysis.

Besides all the previous self-imposed restrictions, it has been fully demonstrated

the robustness of the design against the ripple interference at the transistors' body and power supply. A low-frequency ripple (order of several kHz), with amplitude in the order of 100 mV peak-to-peak, present in the body bias or in V_{DD}, will show as an added noise to the RF output signal, but with negligible levels (well below the device noise and sensitivity levels), due to the extremely small conversion gains obtained from the low-frequency input to the high-frequency output. The same input ripple will show at the output at lower frequencies (order of 1 MHz), but also with negligible levels (below sensitivity levels). Thus, a possible effect on the mixer output (IF) is discarded.

The largest impact of these low-frequency ripples is shown as a time-variability of OP conditions, which results in a time-variant RF performance (gain, NF and input matching). In particular, the largest impact is produced by variations in V_{DD} voltage ($= V_{BIAS}$). A ± 50 mV variation, however, is still tolerable (input matching preserved, still moderate degradation of S_{21} and NF), although variations beyond ± 50 mV should be avoided. Finally, RF performance shows a low sensitivity to Body Bias variations. Thus, a large V_{BODY} tuning range would be required to use FBB as a tuning knob to compensate important deviations of LNA performance produced by PVT.

Chapter 5

Mixer

The following chapter presents the design of the mixer stage of the receiver front-end, which is the next element after the LNA. First, a brief introduction with the basic topologies and their operation fundamentals is provided. Then, a suitable topology that fits our requirements is chosen. The design methodology is then presented, optimizing the gain performance under the adverse supply conditions. The overall results are finally shown at the end of the chapter.

5.1 Introduction

In a superheterodyne radio-frequency receiver architecture, the mixer translates the incoming RF signal, which is typically amplified by a preceding low noise amplifier, to a lower frequency known as the intermediate frequency (IF). It has two inputs and one output. One input is used for the information signal and the other is for the local oscillator (LO). Ideally, the output signal contains the same information as the received input signal, although down-shifted in frequency by an amount equal to the frequency of the LO.

The main reason to down-convert the incoming RF signal is that higher gain and sensitivity are easier to achieve at lower frequencies. Also, filtering channels at the carrier frequency is not feasible because it implies using extremely high quality filters. Again, when down-converting the received signal tuning is accomplished by varying the frequency of a local oscillator (LO), rather than varying the centre frequency of a multipole bandpass filter as it should be done without the down-conversion. Moreover, analog-to-digital conversion for further processing is performed at down-converted frequencies due to the high power consumption of ADCs at high frequencies.

Typically, many circuit analysis proceeds with the assumptions of linearity and time invariance. It is usually considered as undesirable whenever any of these assumptions is not fulfilled. However, as introduced in Chapter 4, some circuits heavily rely on the presence of at least one element that fails to satisfy linear time invariance [16]. Since linear time-invariant systems cannot generate frequencies that are not present in the original signal, mixers shall be either non-linear or time-variant in order to provide frequency translation.

The core of all mixers is a multiplication of two signals in the time domain. The usefulness of multiplication can be understood by considering the application of an input signal and the LO to the mixer.

$$(A_{RF}\cos\omega_{RF}t)(A_{LO}\cos\omega_{LO}t) = \frac{A_{RF}A_{LO}}{2}\left[\cos(\omega_{RF}-\omega_{LO})t + \cos(\omega_{RF}+\omega_{LO})t\right] \tag{5.1}$$

Therefore, multiplication results in output signals at the difference and sum frequencies of the input and the LO. Usually, only the down-converted term will be of interest, so the high frequency term is filtering out. The ideal relation just presented suggests an amplification factor equal to $A_{LO}/2$ and will be henceforth referred to as the conversion gain of the mixer.

5.1.1 Square Law Mixer

Some mixers implement the multiplication action in a direct manner while others provide it incidentally through a nonlinearity. The N-th order nonlinearity of a general two-port input-output relationship can be described as

$$v_{out} = \sum_{n=0}^{N} C_n v_{in}^2 \tag{5.2}$$

which produces three types of products: DC terms, harmonics of the inputs, and intermodulation products of those harmonics. The intermodulation products are the sum and difference frequency terms, being only the second-order intermodulation term normally desired. However, other intermodulation products have frequencies near the desired IF, making them difficult to remove. Generally, the higher the nonlinearity order the larger number of intermodulation products that may potentially corrupt the desired signal. Thus, mixers should approximate the lowest-order nonlinearity, which follows a square-law behaviour.

In a square law mixer the only nonzero coefficients in the previous series expansion are the C_1 and C_2 terms. In fact, the DC component represented by the C_0 term may also be present, but it is easily removed by filtering. If we assume that the input signal is the sum of two sinusoids representing the incoming RF signal and the LO,

$$v_{in} = A_{RF}\cos\omega_{RF}t + A_{LO}\cos\omega_{LO}t \tag{5.3}$$

then the output of the mixer consists of three different components.

$$\begin{aligned} v_{in} &= C_1(A_{RF}\cos\omega_{RF}t + A_{LO}\cos\omega_{LO}t) + C_2(A_{RF}\cos\omega_{RF} + A_{LO}\cos\omega_{LO}t)^2 \\ &= v_{fund} + v_{square} + v_{cross} \end{aligned} \tag{5.4}$$

Where

$$v_{fund} = C_1(A_{RF}\cos\omega_{RF} + A_{LO}\cos\omega_{LO}t) \tag{5.5}$$

$$v_{square} = C_2 \left[(A_{RF} \cos \omega_{RF} t)^2 + A_{LO} \cos \omega_{LO} t)^2 \right] \tag{5.6}$$

$$v_{cross} = 2C_2 A_{RF} A_{LO} (\cos \omega_{RF} t)(\cos \omega_{LO} t) \tag{5.7}$$

Not all these spectral components are desirable. The fundamental terms represent scaled versions of the input, and so represent no useful information. Similarly, the squared terms can also be filtered as they simply produce components at both DC and double the fundamental frequencies. The useful output thus comes from the cross product term, where the multiplication becomes in fact evident.

Square-law mixers may be realized with long-channel MOSFETs working in saturation, as the expression for the drain current inherently presents a quadratic behaviour. Figure 5.1 shows two simple square-law mixer topologies [16]. The first one uses the bias, RF signal and LO driving the gate in series, which makes the RF-LO isolation extremely poor. This lack of isolation is a potential source of problems like overloading IF amplifiers or radiation of the LO signal back out through the antenna. Alternatively, the second configuration applies the LO signal to the source of the transistor to reduce the effect of the LO on the RF port. The fundamental operation is based on the generation of the drain current, which actually employs both transistor's gate and source terminals.

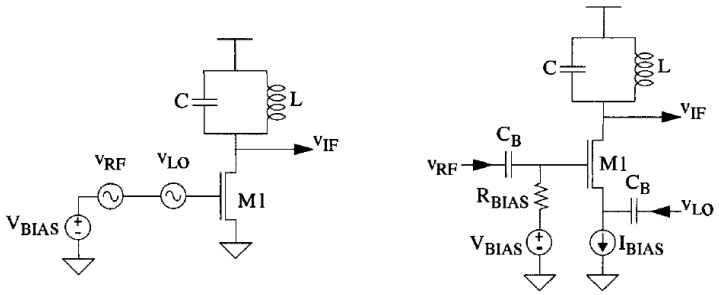


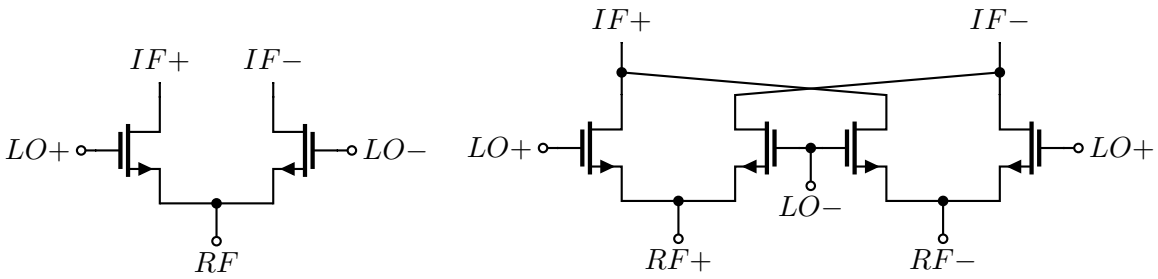
Figure 5.1: Square-law MOSFET mixers. Image taken from [16].

5.1.2 Multiplier-based Mixer

Despite the inherent quadratic behaviour of long channel MOSFETs, the most common way of implementing mixers in CMOS integrated circuits is by directly multiplying RF and LO signals through switching. Mixers that apply direct multiplication generally demonstrate superior performance since only the desired intermodulation product is ideally generated as well as they can provide a high degree of isolation between the signals, which are applied through separate ports. In contrast, square law mixers produce mixing incidentally through the multiplication provided by the nonlinearities they produce, which are prone to generate a lot more undesired spectral components.

The most common multiplier-based mixer topology in CMOS technology uses the structure shown in Figure 5.2. It features two configurations: single-ended and differential, usually referred as single-balanced and double-balanced, respectively. The differential topology combines two single-balanced circuits to produce a double-balanced mixer such that the coupling from RF and LO ports to the IF port is made structurally zero. Practical implementations, though, result in a finite isolation due to mismatch. In both structures the RF signal is applied at the source of the transistors and the LO at the gate. Two instances of the LO shifted 180º one from the other are employed, identified as LO+ and LO-. Ideally, the LO amplitude is chosen large enough so that the transistors switch in an alternate manner. As stated before, the resulting differential output contains two terms at the sum and difference frequencies of the LO and RF signals. The difference down-converted component represents the intermediate frequency (IF).

Actually, the structures shown in Figure 5.2 are two different topologies of active mixers, as they employ a bias current. On the contrary, passive mixers are a different type of multiplier-based mixers that do not require a supply voltage, although need large LO amplitudes to provide linearity. Moreover, derived losses shall be later compensated with amplification, which further increases power consumption. It cannot be stated, thus, that a passive mixer has no power consumption. Generally, passive mixers are employed where strict linearity requirements apply, like in base stations, in which case power consumption may not be the primary concern. On the other hand, active mixers provide gain and thus a better overall front-end noise figure.



(a) Single-balanced. (b) Double-balanced.

Figure 5.2: Common types of multiplier-based mixers.

5.2 Circuit Design

This chapter exposes the influence of all design elements and decisions taken on the receiver front-end's mixer. First, the topology employed is presented, with special emphasis on its viability under stringent low voltage scenarios. A qualitative approach is then used to characterize its operation principle and conversion gain. Just like the LNA design, the proper way to bias the circuit is deeply argued, as it majorly determines the overall performance of the mixer. Both the load element and

size of transistors are then introduced into the equation. Finally, the impact of the local oscillator's amplitude is addressed and a potential application of forward body bias is commented.

Due to the conditions imposed by ULP-ULV designs, targeting all mixer's specifications is not feasible. Rather, this chapter aims at analysing a topology which is capable to cope with those severe voltage and power limitations while still offering acceptable gain, which arguably represents the most valuable factor concerning subsequent receiver stages. That is, other parameters like noise figure and linearity are not specifically optimized. In case unacceptable results would be obtained regarding these specifications, specific design actions should then be taken.

5.2.1 Topology

As in the case of the LNA, low voltage and low power consumption are the key operation requirements defined for the mixer. Traditional active mixers rely on stacking multiple transistors as the typical double-balanced architecture shows in Figure 5.2, so low voltage active mixers are very challenging to design. In fact, passive mixers are often employed to avoid this problematic [26][8][30]. However, passive mixers suffer from low voltage swings yet are not able to provide gain. This work proposes an active mixer topology called switched transconductor [11][14], which resembles that of the typical implementation with a couple of key modifications to allow low voltage operation. The circuit, shown in Figure 5.3, presents single-transistor branches where both the LO and RF are being applied, which permits voltage headroom improvement. Thus, the topology lacks a specific transconductor where the RF signal is employed to generate an RF current to the switching device like Figure 5.2. Probably the main advantage of the proposed architecture relies upon the direct application of the LO signal to the source of the transistors instead of the gate. If the LO is centred around 0 volts, both the positive and negative swings of the signal can be handled by the transistors. Traditional implementations of switched transconductor mixers make use of a digital LO through buffers [14][28][27]. However, LO buffers require a significant amount of power running at high speed and, more importantly, the negative swing of the sinusoidal LO is lost.

The switched transconductor mixer addresses the concerns related to ULV-ULP operation since there is no transistor stacking and the whole LO swing is actually used to maximize headroom. Furthermore, the current draw is minimized because there are not multiple current paths like in folded topologies. From the schematic in Figure 5.3 it is evident that the mixer has a double-balanced implementation such that common mode noise is minimized at the output and a high degree of isolation is achieved between the IF output and both the RF and LO inputs. In this case, thus, it is necessary to utilize a balun at the output of the LNA to convert the single-ended output to differential. The mixer is resistively loaded, meaning that common mode output voltage and output impedance may be easily characterized [11].

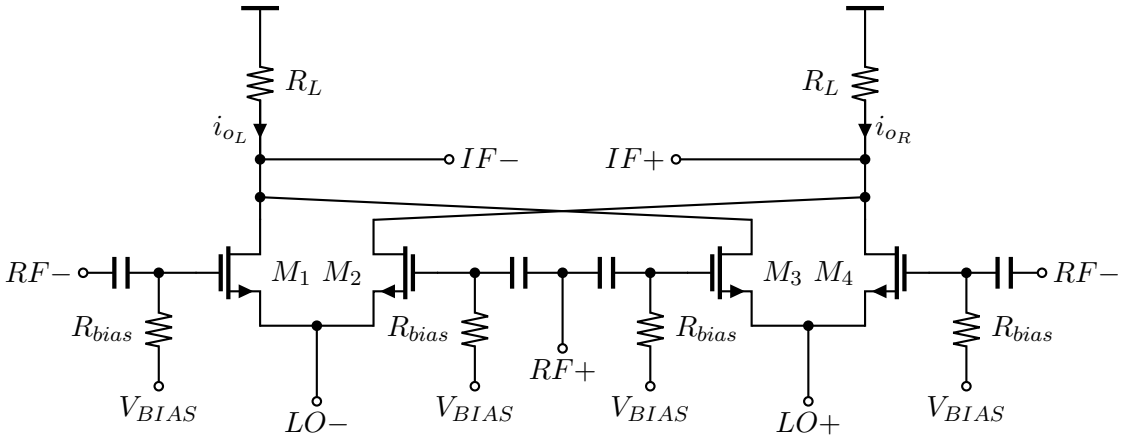


Figure 5.3: Switched transconductor mixer.

5.2.2 Qualitative Behaviour

The circuit in Figure 5.3 combines two NMOS differential pairs acting as transconductor $g_{m_{1-2}}$ and $g_{m_{3-4}}$, formed by $M1$-$M2$ and $M3$-$M4$ transistors, driven in antiphase. Two instances of the LO at 0° (LO+) and 180° (LO-) phase shift are employed such that, when LO- is minimum, $M1$-$M2$ are on and $M3$-$M4$ are off, and vice versa. Typical active double-balanced mixers (see Figure 5.2) drift the RF current through one branch or the other. Instead, the proposed architecture directly switches on and off the transconductor itself, hence the name switched transconductor.

Usually, analyses assume that the transistor is biased well in strong inversion and saturation. Assuming long channel behaviour, consider the expression of the drain current as follows

$$i_{D_{s.i.}} = \frac{1}{2}K\left(v_{GS} - V_{TH}\right)^2 \tag{5.8}$$

where $K$is the transocnductance coefficient given by $\mu_n C_{ox} W/L$, v_{GS} is the gate-source voltage of the transistor and V_{TH} is the threshold voltage. By simply observing 5.8 one may guess that, despite being an active double-balanced-based topology, the operation will in fact remind that of a square-law mixer.

As a matter of simplicity, the current through the left load resistance is called i_{OL} and the current through the right load resistance is called i_{OR}. Let's consider first the differential pair formed by transistors $M1$-$M2$, which are matched with respect $M3$-$M4$. When LO- is minimum, M1's transconductance generates a drain current $i_{OL,g_{m_{1-2}}}$. Similarly, $M2$ induces a current $i_{OR,g_{m_{1-2}}}$.

$$i_{OL,g_{m_{1-2}}} = \frac{1}{2}K\left(V_{BIAS} - V_{TH} - \frac{1}{2}v_{RF} - v_{LO}\right)^2 \tag{5.9}$$

$$i_{OR,g_{m_{1-2}}} = \frac{1}{2}K\left(V_{BIAS} - V_{TH} + \frac{1}{2}v_{RF} - v_{LO}\right)^2 \tag{5.10}$$

The differential output current due to transistor pair $M1$-$M2$ is thus

$$i_{O,g_{m_{1-2}}} = i_{OL,g_{m_{1-2}}} - i_{OR,g_{m_{1-2}}} = K\left[v_{RF}v_{LO} - (V_{BIAS} - V_{TH})v_{RF}\right] \tag{5.11}$$

Interestingly, the multiplication term $v_{RF}v_{LO}$ has appeared, revealing the mixing action. An equivalent procedure can be followed to derive the differential output current due to transistor pair $M3$-$M4$ when LO+ is maximum. The generated currents at the left and right branches are

$$i_{OL,g_{m_{3-4}}} = \frac{1}{2}K\left(V_{BIAS} - V_{TH} + \frac{1}{2}v_{RF} - v_{LO}\right)^2 \tag{5.12}$$

$$i_{OR,g_{m_{3-4}}} = \frac{1}{2}K\left(V_{BIAS} - V_{TH} - \frac{1}{2}v_{RF} - v_{LO}\right)^2 \tag{5.13}$$

It can be easily observed that the differential output current in this case is the same as 5.11 with opposite sign.

$$i_{O,g_{m_{3-4}}} = i_{OL,g_{m_{3-4}}} - i_{OR,g_{m_{3-4}}} = K\left[-v_{RF}v_{LO} + (V_{BIAS} - V_{TH})v_{RF}\right] \tag{5.14}$$

Finally, the overall differential output current is

$$i_O = i_{O,g_{m_{1-2}}} - i_{O,g_{m_{3-4}}} = 2K\left[v_{RF}v_{LO} - (V_{BIAS} - V_{TH})v_{RF}\right] \tag{5.15}$$

By considering RF and LO sinusoidal signals given by $v_{RF} = A_{RF}\cos\omega_{RF}t$ and $v_{LO} = A_{LO}\cos\omega_{LO}t$,

$$i_O = 2K\left[\frac{1}{2}A_{RF}A_{LO}(\cos(\omega_{RF} - \omega_{LO})t + \cos(\omega_{RF} + \omega_{LO})t) - (V_{BIAS} - V_{TH})v_{RF}\right] \tag{5.16}$$

Up to this point, it is worth noting that all current expressions may be easily converted to voltage by multiplying them by R_L. In the end, thus, the output voltage expression takes the same format as the output current with the load resistance value multiplying.

Assuming that only the down-converted term preserves and all other components are filtered out, the conversion gain of the mixer using strongly inverted saturation devices becomes

$$CG_{s.i.} = \frac{\frac{1}{2}KR_LA_{RF}A_{LO}}{A_{RF}} = \frac{1}{2}KR_LA_{LO} \tag{5.17}$$

Noticing that $g_m = K(V_{GS} - V_{TH})$ we can rewrite the conversion gain expression as follows

$$CG_{s.i.} = \frac{g_mR_LA_{LO}}{2(V_{GS} - V_{TH})} \tag{5.18}$$

The former equation assumes strong inversion for the transconductor devices. Due to the low voltage operation, though, it is also useful to address the expression when the transistors have entered weak inversion. In such case, the drain current presents an exponential behavior as follows.

$$i_{D_{w.i.}} = I_s e^{\frac{v_{GS}-V_{TH}}{\eta U_T}} \tag{5.19}$$

$$I_s = 2\eta\mu_n C_{ox}\frac{W}{L}U_T^2 \tag{5.20}$$

Due to the exponential term we can easily decompose the expression into its DC and AC terms.

$$i_{D_{w.i.}} = I_s e^{\frac{V_{GS}-V_{TH}}{\eta U_T}} e^{\frac{v_{GS}}{\eta U_T}} \tag{5.21}$$

Where η is the subthreshold slope factor with typical values between 1.2 and 1.5 and U_T is the thermal voltage which is approximately 25 mV at room temperature. Expansion of this relationship up to the second term yields

$$i_{D_{w.i.}} \approx I_D\left[1 + \frac{v_{gs}}{\eta U_T} + \frac{1}{2}\left(\frac{v_{gs}}{\eta U_T}\right)^2\right] \tag{5.22}$$

The result is again a structure presenting a quadratic term that will effectively originate the mixing products. By following the same procedure as before, we can obtain the expression for the conversion gain under weak inversion.

$$CG_{s.i.} = \frac{g_m R_L A_{LO}}{2\eta U_T} \tag{5.23}$$

The conversion gain expression when the transconductors are in strong inversion and weak inversion have been provided. In order to ensure strong inversion, the gate-source voltage shall significantly exceed the threshold voltage. Therefore, by observing 5.18 and 5.23 we may intuitively guess that, at similar transconductance values, the conversion gain under weak inversion is capable to present larger values than the strong inversion counterpart. The following chapter details the biasing approach of the mixer, confirming the previous expectations.

5.2.3 Biasing

As previously discussed, the switched transconductor mixer has an inherent advantage for low voltage, low power applications. Even so, it is important to consider optimizing transistors biasing in order to maximize performance.

Even though the performance of the circuit shall be evaluated with a periodic steady-state analysis, a DC characterization permits evaluating the proper biasing approach and helps visualizing circuit trends. AC signals are virtually grounded when a DC analysis is performed. Thus, all source terminals in Figure 5.3 would be effectively set to 0 volts, which actually does not represent the time instant when a given transistor is completely on. Consequently, all DC characterizations will be

carried out adjusting the source of the device under test at the minimum value of the local oscillator. To start, a reasonable LO amplitude of $A_{LO} = 210\,\text{mV}$ will be considered, which corresponds to 60% of the supply voltage V_{DD}. When the LO is minimum, a complete voltage headroom equal to $V_{DD} + A_{LO}$ is achieved, highlighting the powerfulness of the topology.

Let's recall the conversion gain equations under strong inversion 5.18 and weak inversion 5.23. Indeed, both expressions invite us to consider various approaches to increase the gain. First, as one may expect, the transconductance value may be boosted by increasing the number of width fingers or the bias voltage. This methodology has a direct effect on consumption, though, as the current does also increase. Alternatively, the reader may also be prompted to reduce the bias voltage such that the transistor still operates in strong inversion in order to reduce the gate-source voltage. However, the transconductance would decrease at the same rate and the overall gain would not become affected. In conclusion, focusing the efforts towards the transconductance is not a viable option since it opposes the low power requirement. A different approach could be increasing the amplitude of the local oscillator. However, oscillator designs are majorly impacted by the required swing amplitude, so the mixer design should not strongly impose severe amplitude restrictions for the LO. Finally, thus, the easiest way to achieve gain is by increasing the load resistance R_L. When R_L increases so does its voltage drop, which in turn reduces the drain voltage of the transistor. Ultimately, there would be a point where the transistor would finally enter ohmic region, misadjusting the operating point and degrading the performance. Intuitively, thus, there is an optimal R_L value which offers the best compromise throughout the whole LO cycle.

In order to permit larger R_L values we need to reduce the current such that the drain voltage drop is slowed down. Consequently, the mixer should provide the highest possible transconductance for a given amount of current. This quantity is in fact maximized in weak inversion, so using weakly inverted devices enables the desired transconductance to be realized in the most efficient way as it was already predicted in the previous Section.

In order to demonstrate the aforementioned behaviour, Figure 5.4 shows the drain-source voltage evolution with respect to the load resistance under different bias voltages, where all curves have been adjusted at similar transconductance values. The minimum saturation voltage has also been included such that the boundary between saturation and ohmic can be easily identified. As it can be observed, as we keep reducing the bias voltage, the transistor's inversion degree diminishes, which lowers the generated current and permits larger R_L values before entering ohmic condition. Weak inversion thus permits maximizing the load resistance value, which implies larger gain.

Strictly speaking, the saturation voltage depends on the bias level. In strong inversion it approaches the value $(V_{GS} - V_{TH})/\eta$ and saturates between 100 mV-150 mV as it moves towards weak inversion. Therefore, the saturation voltage shown in Figure 5.4 corresponds to weakly inverted devices and dictates a lower bound value. In fact, it becomes more difficult to keep saturation in strongly inverted devices due to their higher drain-source saturation voltage values.

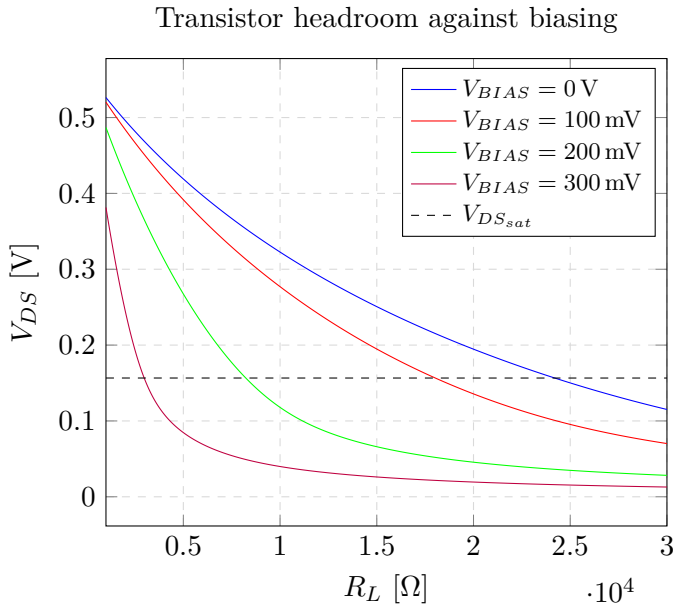


Figure 5.4: V_{DS} voltage against R_L using different bias voltages.

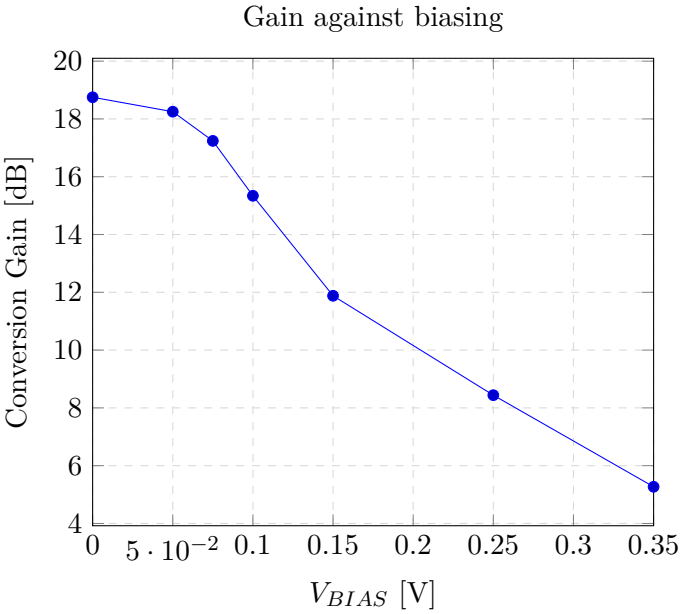


Figure 5.5: Conversion gain against biasing. All graph points have been adjusted at equal transconductance values.

By inspecting the simulation results in Figure 5.5 it becomes clear that properly biasing the transistors in weak inversion yields a significant gain improvement. There is another benefit form operating the transistors in weak inversion, since flicker

noise is inversely proportional to device size and a weakly inverted device will be considerably larger than strongly inverted one [11].

5.2.4 Load Resistance

As demonstrated in the previous chapter, high values of load resistance are required to improve gain performance. However, one may expect to have some upper bound for its value, and in fact there is. As R_L is increased, its voltage drop also increases and so the drain voltage of the transistors reduces. In case the value of R_L was kept increasing, the drain voltage would finally drop below the saturation voltage of the transistors, bringing them into ohmic region. The aforementioned trends manifest an optimal load resistance value which offers the best compromise throughout the whole LO cycle. Figure 5.6 depicts a conversion gain curve against R_L. At low resistance values the gain follows a linear approach as per 5.23. The gain increases up to the point where ohmic effects prevail during a significant time of the LO cycle.

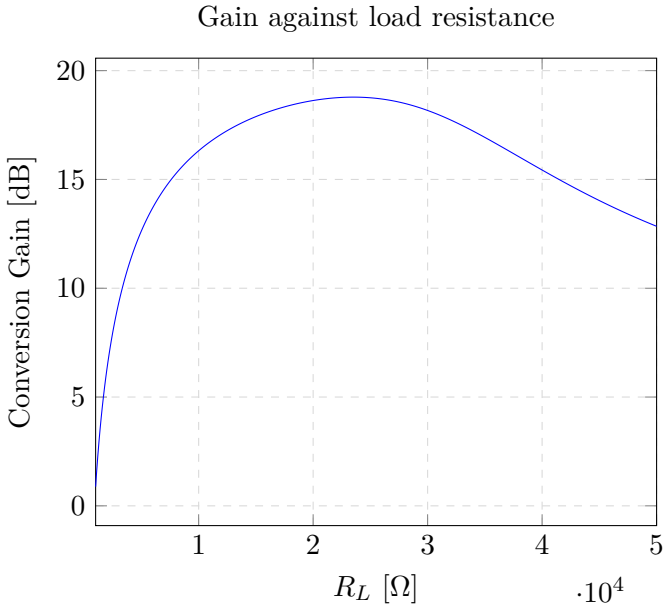


Figure 5.6: Conversion gain against R_L.

5.2.5 Transistors Size

Both weak inversion and strong inversion transconductances are directly proportional to the number of width fingers employed.

$$g_{m_{w.i.}} = \frac{I_D}{\eta U_T} \propto W \tag{5.24}$$

$$g_{m_{s.i.}} = K(V_{GS} - V_{TH}) \propto W \tag{5.25}$$

Therefore, conversion gain expressions in 5.23 and 5.18 imply that, in order to relax the size of transistors, one may increase the required load resistance value to maintain the optimum gain spot. The main drawback while operating in weak inversion are the significant dimensions of the transistors. Apart from the physical space being occupied, big transistors generate larger parasitics which may load the oscillator. It is thus convenient to reasonably manage the W-R_L pair of values.

Figure 5.7 shows the same dependence of the conversion gain upon R_L using three different transistor sizes. As it is observed, when the number of fingers is reduced, the required R_L value to achieve maximum gain is greater, and vice versa.

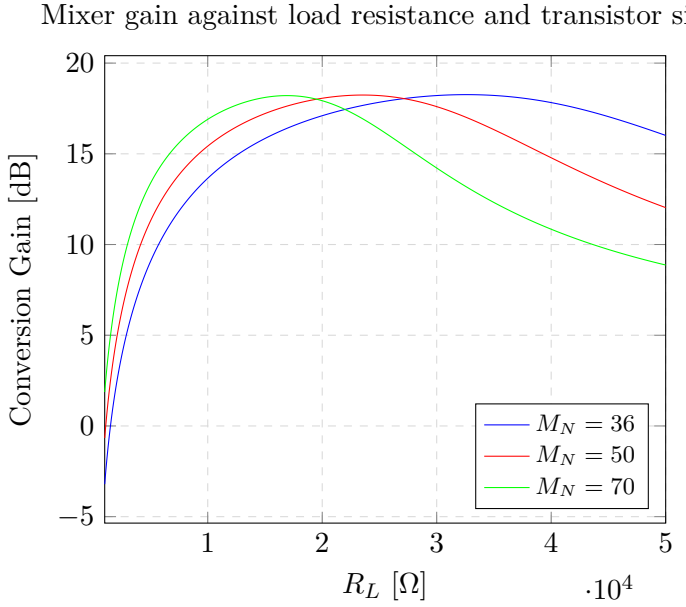


Figure 5.7: Conversion gain against R_L using three different number of transistor fingers (aspect ratio $W/L = 10$).

5.2.6 Local Oscillator Amplitude

The derived expressions for the conversion gain depict a direct dependence upon the amplitude of the local oscillator, which may be intuitively assessed by noting its implication on the available voltage headroom. The key feature of the chosen switched transconductance mixer topology is its ability to take full profit of the whole LO swing. Hence, it is evident that the performance of the mixer will be partly determined by the amplitude provided by the oscillator.

The reduction of the LO amplitude has two main effects. First, the effective gate-source voltage is lowered, so larger transistors are required to keep the transconductance value. Simulations have shown that reducing the amplitude a factor of 1.6 traduces in transistor 4 times larger. Second, the drain-source voltage of the transistors does also decrement, emulating a similar effect as the one observed with increasing R_L. In order to compensate the voltage headroom reduction, we need to

reduce the value of R_L such that the resulting drain voltage increases. This effect can be observed in Figure 5.8, where the drain-source voltage dependence upon the load resistance is shown using different oscillator amplitudes. According to the previously stated benefits, the curves have been characterized under weak inversion operation. As expected, the lower the amplitude of the local oscillator the lower the load resistance value before the transistor enters ohmic region, thus having a direct implication on the gain.

A different approach regarding the convenience of big LO swings is the fact that we want to minimize the period of time when the LO voltage stays near its centre value (0 volts in this case). Proper operation of the mixer requires switching transistors alternatively, so large LO amplitudes are capable to make them reach the on and off states faster, while minimizing the time in which transistors have similar gate-source voltages.

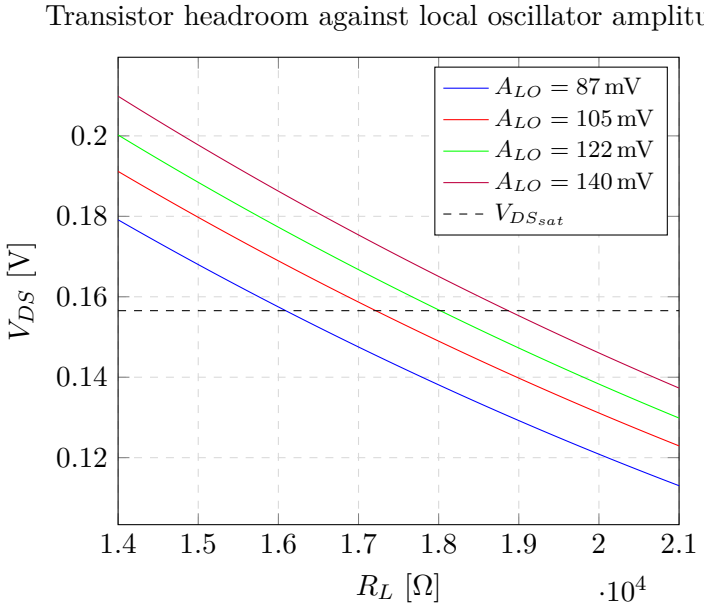


Figure 5.8: V_{DS} voltage against R_L using different local oscillator amplitudes.

The plot in Figure 5.9 illustrates the resulting conversion gain against the local oscillator amplitude, where each of the data points have been obtained biasing the transistors in weak inversion and adjusting similar transconductance values. As discussed, the gain increases for larger LO amplitudes, even though its impact does seem as determining as the analytical expression suggests. A possible reason is the fact that reducing the LO amplitude brings the transistors deeper into weak inversion, which has been proven to be the proper biasing methodology. Consequently, the inherent gain reduction predicted by the analytical expression is smoothed due to the second order biasing effects.

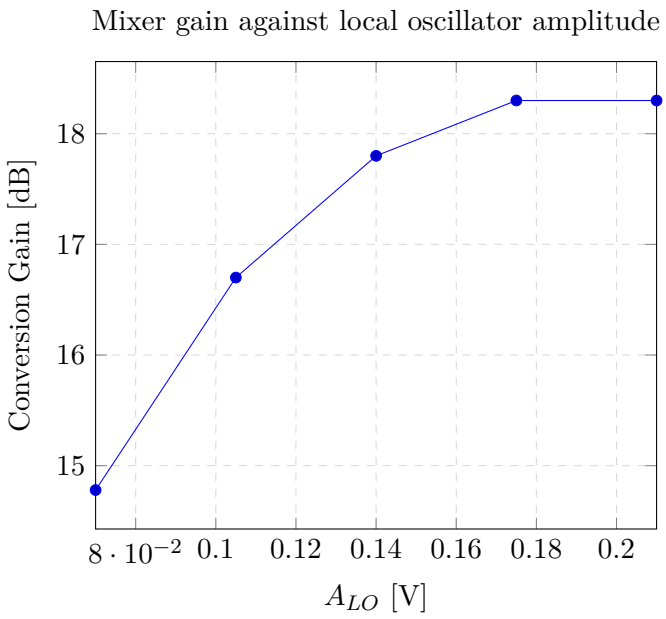


Figure 5.9: Conversion gain against local oscillator amplitude. All graph points have been adjusted at equal transconductance values.

5.2.7 Forward Body Bias

FD-SOI provides an additional design variable through the application of an aggressive forward body bias (FBB). This, combined with the high FBB-V_{TH} sensitivity, permits severe threshold voltage variations. Attending the qualitative behaviour of the mixer, more precise on-off states would be desirable by reducing the threshold voltage during the on-cycle and increasing the threshold voltage during the off-cycle. Actually, such behaviour can be emulated by using the same LO signal in counter-phase. That is, when the source voltage is at the minimum value, then the body bias would be at the maximum, thus reducing the threshold voltage and improving the on operation. Similarly, when the source voltage is at maximum, the body bias is at minimum, which increases the threshold voltage and the off condition is strengthened. Although correct, such reasoning does not take into consideration the biasing side effect. When the threshold voltage reduces during the on state, the overdrive voltage (and so the inversion coefficient) increases, which, as predicted in Section 5.2.3, asks for lower R_L values due to the current consumption boost.

$$FBB \uparrow \rightarrow V_{TH} \downarrow \rightarrow V_{OD} \uparrow \rightarrow I_D \uparrow V_D \downarrow \tag{5.26}$$

Consequently, there exists a self-compensating effect in which the improvement in transistors' switching performance is in turn neutralized by the necessity of reducing the load resistance value. Recalling Section 5.2.5, width fingers and load resistance share a similar dependence as far as gain is concerned. In the end, thus,

the application of forward body bias may be contemplated as a plausible action to reduce the size of the transistors. Simulations have proven that the size can be reduced by a 1.5 factor.

Figure 5.10 shows the conversion gain against the load resistance in both FBB and FBB-less scenarios, where the body signal (when present) is the same LO but reversely applied with respect to the source LO signal. As commented, the application of FBB demands the reduction of the load resistance value in order maintain the optimum gain spot. Although pretty similar, maximum gain values are a bit larger for FBB-less scenarios, which responds to the fact that the inversion degree of the transistors is being increased upon FBB application.

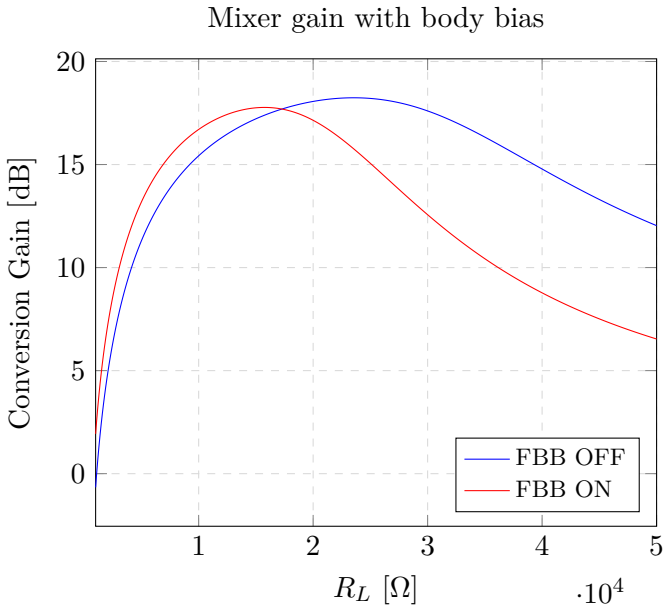


Figure 5.10: Conversion gain against R_L applying forward body bias.

5.2.8 Linearity

In the frequency domain, third-order products are the intermodulation distortion products between one of the fundamental signals and the second harmonic of the other signal. The presence of two or more tones in a nonlinear circuit generates intermodulation products. Many of the spurious tones are out-of-band and cause no problems. However, the third-order tones are nearest to the fundamental and are likely to fall in-band. They add distortion to the output signal. Together with the conversion gain, linearity is probably the most important specification of a mixer since it is amplified by the LNA gain.

IP3 is a metric or figure of merit for linearity that is used to describe the intermodulation performance of a mixer. The intercept point is obtained graphically by plotting the output power versus the input power both on logarithmic scales. Using the logarithmic scale, a function x^n translates into a straight line with slope

of n. Therefore, the linearly amplified signal will exhibit a slope of 1 while the third-order nonlinear product will present a slope of 3. The point where these extrapolated curves intersect is the intercept point, which can be referred from the input (IIP3) or the output (OIP3). Extrapolation is actually required due to compression effects at high power levels.

In order to evaluate this metric, the mixer has been fed using two RF tones; one at 2.45 GHz (we may simply call it RF1), and a second tone at 2.4501 GHz (referred as RF2). Since the mixer is down-converting to the baseband, the first harmonic is calculated as

$$f_{RF1} - f_{LO} = 2.45\,\text{GHz} - 2.448\,\text{GHz} = 2\,\text{MHz} \tag{5.27}$$

On the other hand, the third order harmonic can be computed as

$$2f_{RF1} - f_{RF2} - f_{LO} = 2 \cdot 2.45\,\text{GHz} - 2.4501\,\text{GHz} - 2.448\,\text{GHz} = 1.9\,\text{MHz} \tag{5.28}$$

5.2.9 Noise

Noise figure of mixers is difficult to compute because of the circlostationary nature of the noise sources. A qualitative analysis may be adopted as in [22], splitting the circuit in RF, time-variant and IF sections. Because of the time-variant part of the mixer it is difficult to obtain an accurate closed expression for the noise. Nonetheless, we can identify important noise sources and make general recommendations about how to minimize noise figure. One noise source is certainly the transconductor itself, so that its noise figure establishes a lower bound on the mixer noise figure.

Contrary to linearity, noise figure in mixers is not as determining because it becomes neutralized by the preceding LNA gain. Similarly, by ensuring good conversion gain, the same mixer can also help attenuating the noise figure of the subsequent receiver blocks.

5.3 Results

The proposed circuit parameters and specifications achieved for the low voltage/low power mixer are shown in Table 5.1. The design is based on a switched transconductance architecture using a supply of 350 mV and a local oscillator amplitude of 210 mV, even though it can be further reduced without loosing significant performance. The topology does not employ forward body bias, but it can be easily implemented in order to reduce transistors' size by a factor of 1.5. The bias voltage has been set to 50 mV to ensure weak inversion operation. Even lower voltages can be used, although the required transistor size does not justify the minor performance improvement. By adjusting the number of fingers to 50, the total width of each transistor becomes 15 µm and the optimum load resistance value to achieve the maximum gain spot is 23.5 kΩ. With the former parameters and circuit conditions, the resulting performance at an intermediate frequency of 2 MHz achieves a conversion gain of 18.24 dB, an IIP3 value of −10.7 dBm and a noise figure of 18 dB.

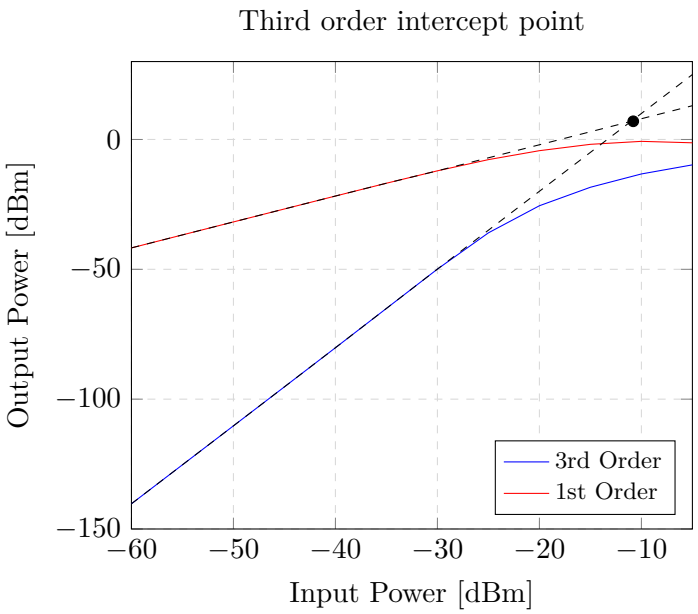


Figure 5.11: Third order intercept point with the extrapolated 1st order and 3rd order curves.

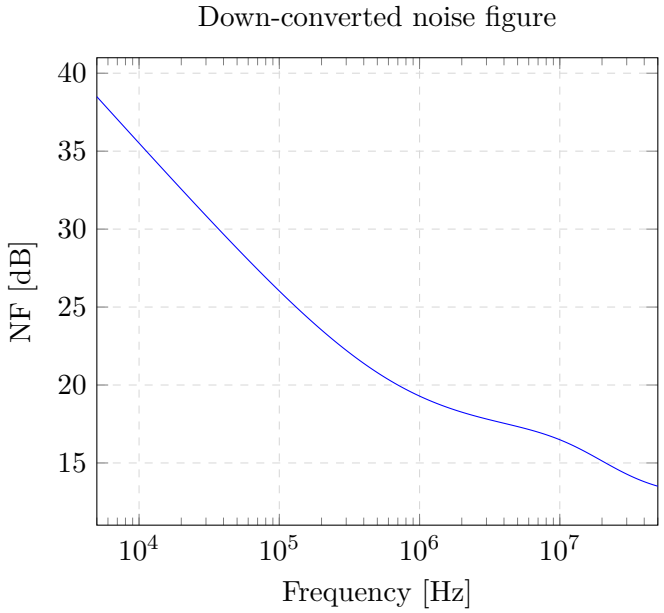


Figure 5.12: Noise figure at down-converted frequencies.

The reader may wonder about the significantly high noise figure result. The fact is that values of this order are typically assumed since noise figure of mixers

is neutralized by the preceding LNA gain. Finally, all this is accomplished using a limited peak current (that is, when the transistor is fully on) of only 11.5 µA per transistor, which corresponds to a maximum instantaneous power of 8.05 µW. Even better, consumption may be further reduced by employing a lower number of transistor fingers and increasing the load resistance by the same factor.

Figure 5.11 shows the linearity in terms of the third order intercept point. The extrapolated IIP3 point is located at −10.7 dBm. Although the result is fairly decent enough, one way to improve it could be by using larger currents, which, on the other hand, opposes the low power requirement. The overall noise figure between 5 kHz and 50 MHz is depicted in Figure 5.12. As expected, the low frequency behaviour follows the typical linear curve due to transistors' flicker noise when represented in logarithm scale. In case further improvement was desired, larger transconductance values should be used at the expense of, again, larger currents and overall power consumption.

Table 5.1: Mixer design values and performance.

Circuit values	
V_{DD}	350 mV
FBB	No
V_{BIAS}	50 mV
NMOS Width	15 µm
R_L	23.50 kΩ
DC Performance	
$I_{D,peak}$ Total	23.50 µA
P_{peak} Total	8.05 µW
RF Performance	
f_{IF}	2 MHz
CG	18.24 dB
NF	18 dB
IIP3	−10.70 dBm

5.4 Conclusions

The design of the ULV-ULP mixer has been addressed in this chapter. First, a proper active mixer topology capable to work under very low voltage supplies has been identified and argued. Then, the design methodology has been focused towards the obtention of acceptable conversion gain in order to relax the requirements of subsequent baseband circuitry. It has been demonstrated that the suitable biasing

approach for the transistors is to work in weak inversion, which allows larger load resistance values. The influence of other design parameters like oscillator amplitude and forward body bias has also been studied. Finally, simulation results showing the typical performance metrics have been provided.

According to the final results, the designed mixer has exceeded the initial expectations. Even at very low supply voltage, the circuit is capable of providing excellent gain as well as good linearity mostly by virtue of the employed topology, which takes profit of the full LO swing. The noise figure, although not being extremely elevated, is the worst of the obtained performance results. Nonetheless, as already commented, its influence is neutralized by the LNA gain. That is, the noise figure of the LNA has the highest impact in the design. Finally, the implementation of FD-SOI has not proven to be as necessary as in the case of the LNA, although it has been shown that FBB can potentially reduce the final size of the solution. Moreover, the design does not require the implementation of any on-chip inductor, which saves space and cost.

Chapter 6

Conclusions and Future Development

The pre-layout design of a low-noise amplifier and mixer working in a ULV-ULP scenario has been presented in this work. To enhance performance when low voltage supplies are used, 28nm FD-SOI technology has been implemented.

A current-reuse topology applying active *gm*-boosting has been chosen for the LNA. The biasing approach has verified an upper bound voltage supply of 350 mV, even though it has also been demonstrated in Chapter 4 that good performance is still accomplished with a supply of 300 mV. The amplifier presents a power gain of 24 dB, a very low noise figure of 2 dB and good input matching at 2.45 GHz, applying forward body bias of 1 V and only consuming 10.5 µW. Input matching has been achieved implementing an L-section matching network which contemplates the pad and wire bonding parasitic effects. Specific sensitivity and graphical analyses have been employed in order to discern the most suitable architecture. Due to library constraints and the necessity to employ high-quality components, a shunt capacitor and a series inductor have been built off-chip, which relaxes chip area utilization specially when integrated inductors are eluded. The small size of the chosen components permits considering the proposed solution even under strict area restrictions, minimizing its integration impact within the whole system.

Large signal effects from the charge pump-based circuitry generating the bias and supply voltages have been evaluated using periodic steady state analyses. It has been demonstrated that high order harmonics do not interfere with the normal operation of the amplifier, even after considering worst-case amplitude and frequency ripple approaches. Lower frequency response has also been addressed anticipating potential feedthrough form the LNA output to IF by observing near-IF harmonics, although their contribution has not required any specific attenuation neither. Moreover, the circuit has been proven to be robust enough against both supply and FBB DC variations. In fact, it has been observed that the body bias terminal can be employed as an additional design variable to finely adjust matching thus compensating non-ideal physical implementation effects.

Finally, a switched transconductance topology has been chosen as the ULV-ULP

mixer. The chosen architecture permits countering the low supply effects by offering the full LO swing, such that transistors headroom is increased. A proper methodology to maximize the gain has been presented, demonstrating the advantages to bias transistors in weak inversion region. Also, it has been shown that the mixer does not require very high LO amplitudes to keep decent performance. Using a low IF of 2 MHz, the mixer presents a voltage gain of 18 dB, an IIP3 point at -10.7 dBm and a noise figure of 18 dB, while consuming a very low power of 8.05 µW during the LO peaks. In this case, the design has not demanded the application of FBB, although it has been shown that it can be a valuable option to decrease the final size of the transistors while maintaining performance.

As future development, an LO structure should be implemented to accommodate the operation of the mixer. In this regard, it has been shown that the amplitude of the LO may still be significantly reduced if required. Also, even though the single-ended LNA output can be directly used at the input of the mixer, a specific custom balun should be designed if a fully-differential structure is pursued. Finally, mismatch simulation should be performed on the mixer transistor pairs to evaluate port isolation.

Appendices

Appendix A

Sensitivity Analysis Input Matching Expressions

The analytical derivation of the proposed matching networks used by the sensitivity analysis is presented in this annex.

A.1 Pad-Normal L-Section Network

The Pad-Normal L-section network shown in Figure A.1 consists of the pad followed by a series reactance X, a shunt susceptance B and the load Z_L, which represents the LNA.

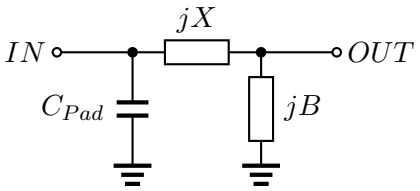


Figure A.1: Pad-Normal L-section network.

Given that the objective is to provide matching by equalling the input impedance to the characteristic impedance Z_0, we can express the input admittance Y_{in} as

$$Y_{in} = jB_{pad} + \frac{1}{jX + \frac{1}{G_L + j(B+B_L)}} = Y_0 \tag{A.1}$$

where $B_{pad} = \omega C_{pad}$ is the parasitic pad's susceptance, G_L is the load conductance, B_L is the load susceptance and Y_0 is the characteristic admittance. By developing A.1 and splitting real and imaginary parts, we can obtain the following system of equations.

$$\begin{cases} X(B_{pad}G_L - Y_0(B + B_L)) = G_L - Y_0 & \text{(A.2a)} \\ X(Y_0G_L + B_{pad}(B + B_L)) = B + B_L + B_{pad} & \text{(A.2b)} \end{cases}$$

The development of this system of equations results in a quadratic outcome. That is, the network has two possible pairs of solutions, which we will simply name Option 1 (X_1, B_1) and Option 2 (X_2, B_2).

A.2 Pad-Reversed L-Section Network

The Pad-Reversed L-section network shown in Figure A.2 consists of the pad followed by a shunt susceptance B, a series reactance X and the load Z_L, which represents the LNA. In this case the shunt component may be either implemented inside or outside the chip.

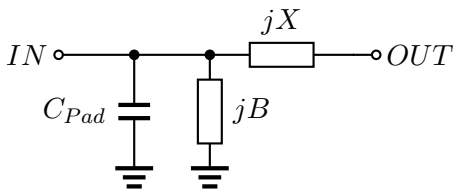


Figure A.2: Pad-Reversed L-section network.

The input admittance Y_{in} of the network can be derived as

$$Y_{in} = j(B_{pad} + B) + \frac{1}{R_L + j(X_L + X)} = Y_0 \tag{A.3}$$

where $B_{pad} = \omega C_{pad}$ is the parasitic pad's susceptance, R_L is the load resistance, X_L is the load reactance and Y_0 is the characteristic admittance. By developing A.3 and splitting real and imaginary parts, we can obtain the following system of equations.

$$\begin{cases} Y_0 R_L = 1 - (B_{pad} + B)(X_L + X) & \text{(A.4a)} \\ Y_0(X_L + X) = R_L(B_{pad} + B) & \text{(A.4b)} \end{cases}$$

Again, the network has two possible pairs of solutions, named Option 1 (X_1, B_1) and Option 2 (X_2, B_2).

A.3 Normal-Pad L-Section Network

The Normal-Pad L-section network shown in Figure A.3 consists of a series reactance X, followed by a shunt susceptance B, the pad and the load Z_L, which represents the LNA. Like with the Pad-Reversed L-section network, the shunt component may be either implemented inside or outside the chip

Due to the series reactance element at the antenna-network interface, it is easier to specify the input impedance Z_{in} rather than the admittance. Thus, the input impedance can be derived as

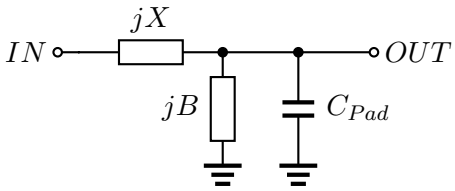


Figure A.3: Normal-Pad L-section network.

$$Z_{in} = jX + \frac{1}{G_L + j(B + B_{pad} + B_L)} = Z_0 \tag{A.5}$$

where $B_{pad} = \omega C_{pad}$ is the parasitic pad's susceptance, G_L is the load conductance, B_L is the load susceptance and Z_0 is the characteristic impedance. By developing A.5 and splitting real and imaginary parts, we can obtain the following system of equations.

$$\begin{cases} X(B + B_{pad} + B_L) = 1 - Z_0 G_L & \text{(A.6a)} \\ X(G_L/Z_0) = B + B_{pad} + B_L & \text{(A.6b)} \end{cases}$$

The system of equations provides again two pairs of solutions, named Option 1 (X_1, B_1) and Option 2 (X_2, B_2).

A.4 Reversed-Pad L-Section Network

The Reversed-Pad L-section network shown in Figure A.4 consists of a shunt susceptance B, followed by series reactance X, the pad and the load Z_L, which represents the LNA. The reader may easily notice that this structure is the same as the Pad-Normal L-section (see Figure A.1) where the pad capacitance and the shunt components are interchanged.

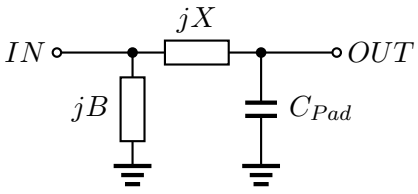


Figure A.4: Reversed-Pad L-section network.

The input admittance Y_{in} of the network can be derived as

$$Y_{in} = jB + \frac{1}{jX + \frac{1}{G_L + j(B_{pad} + B_L)}} = Y_0 \tag{A.7}$$

where $B_{pad} = \omega C_{pad}$ is the parasitic pad's susceptance, G_L is the load conductance, B_L is the load susceptance and Y_0 is the characteristic admittance. By developing

A.7 and splitting real and imaginary parts, we can obtain the following system of equations.

$$\begin{cases} X(BG_L - Y_0(B_{pad} + B_L)) = G_L - Y_0 & \text{(A.8a)} \\ X(Y_0 G_L + B(B_{pad} + B_L)) = B + B_L + B_{pad} & \text{(A.8b)} \end{cases}$$

Again, the network has two possible pairs of solutions, named Option 1 (X_1, B_1) and Option 2 (X_2, B_2).

Appendix B

Smith Chart Input Matching

The Smith chart is a polar plot of the voltage reflection coefficient. Instead of considering the impedance directly, its reflection coefficient Γ_L is expressed, which is used to characterize a load. Given a generic load Z_L and the characteristic impedance of the transmission line Z_0, the reflection coefficient is defined as

$$\Gamma = \frac{z_L - 1}{z_L + 1} = |\Gamma| e^{j\Theta} \tag{B.1}$$

where $z_L = Z_L/Z_0$ is the normalized load impedance and the coefficient is expressed in terms of its magnitude and phase, that is, in polar form. The magnitude is plotted as a radius from the centre of the chart ($|\Gamma| \leqslant 1$), and the angle is measured form the right-hand side of the horizontal diameter

The real utility of the Smith Chart resides in the fact that it can easily convert a given reflection coefficient into its normalized impedance (or admittance) equivalent. In order to graphically relate the two quantities it is necessary to stablish an analytical relationship between them. By writing Γ and z_L in terms of their real and imaginary parts it can be demonstrated that

$$\left(\Gamma_r - \frac{r_L}{1 + r_L}\right)^2 + \Gamma_i^2 = \left(\frac{1}{1 + r_L}\right)^2 \tag{B.2}$$

$$(\Gamma_r - 1)^2 + \left(\Gamma_i - \frac{1}{x_L}\right)^2 = \left(\frac{1}{x_L}\right)^2 \tag{B.3}$$

where $\Gamma = \Gamma_r + j\Gamma_i$ and $z_L = r_L + x_L$.

Equations B.2 and B.3 represent two families of circles in the Γ_r, Γ_i plane. The resistance circles are defined by B.2 and the reactance circles are defined by B.3. All of the resistance circles share the $\Gamma = 1$ point at the right hand side and have centres on the horizontal $\Gamma_i = 0$ axis. The reactance circles also pass through the $\Gamma = 1$ point and the centres lie on the vertical line $\Gamma_r = 1$. The Smith Chart is presented in Figure B.1.

One benefit of the Smith Chart is that it can be used either in normalized impedance or normalized admittance forms, allowing the user to easily switch between impedance and admittance domains without tedious calculations. Converting a

normalized impedance to a normalized admittance, and vice versa, is equivalent to rotating the chart by 180°, which is also equivalent to imaging a given impedance or admittance point across the centre of the chart [21].

Rotating in clockwise direction along an impedance circle results in a positive reactance, that is, an inductance. Moving counter-clockwise along an impedance circle results in a negative reactance, that is, a capacitance. On the contrary, a clockwise rotation along an admittance circle provides a capacitance while moving counter-clockwise results in an inductance.

The graphical procedure followed with the Smith Chart has the objective to match a given complex load. In order to have impedance matching we require $Z_L = Z_0$, which means that $\Gamma_L = 0$ according to B.1. Considering that the Smith Chart is a polar plot of the reflection coefficient, the point where $\Gamma_L = 0$ is in fact at the centre of the chart. Thus, the approach consists in a backwards operation, moving from the load towards the input, passing through all network elements until the centre of the chart is reached. Furthermore, given that only reactive elements are being employed, we can only move along constant resistance or conductance circles. The idea is to work in impedance or admittance domain when the next element in the chain is a reactance or a susceptance, respectively.

Next, both the Reversed-Pad L-section (Figure A.4) and the Pad-Reversed L-section (Figure A.2) will be graphically evaluated with the aid of the Smith Chart. In order to avoid repeating the same concepts throughout the different derivations, only the first matching procedure will be explicitly addressed in more detail detailed.

B.1 Reversed-Pad L-Section Network

The Reversed-Pad L-section network (Figure A.4) permits considering the effective input impedance as that comprised of the LNA together with the pad capacitance. As commented in Section 3.3.2, a pad capacitance $C_{pad} = 250\,\text{fF}$ modifies the input impedance value from $Z_{in} = 1697 - j2382\Omega$ to $Z_{in} = 6.2 - j200\Omega$. Therefore, we will start from an equivalent input impedance $Z_L = 6.2 - j200\Omega$. The Smith chart requires operating with normalized impedances (or admittances). In this case

$$z_L = \frac{Z_L}{Z_0} = 0.12 - j4 \tag{B.4}$$

This value can already be plotted on the Smith chart, although it is also useful to evaluate the corresponding reflection coefficient by applying B.1.

$$\Gamma = \frac{0.124 - j4 - 1}{0.124 - j4 + 1} = 0.87 - j0.46 = 0.985\angle - 28.05^{\text{o}} \tag{B.5}$$

Starting from the pad, the first element towards the antenna is the series reactance jX, so it is appropriate to maintain the impedance domain. The absence of a resistive component allows us to move along the $r = 0.12$ circle until the normalized conductance g of the resulting combination is equal to 1. In this case it is thus very useful to draw both the impedance and admittance circles with $g = 1$. It is worth

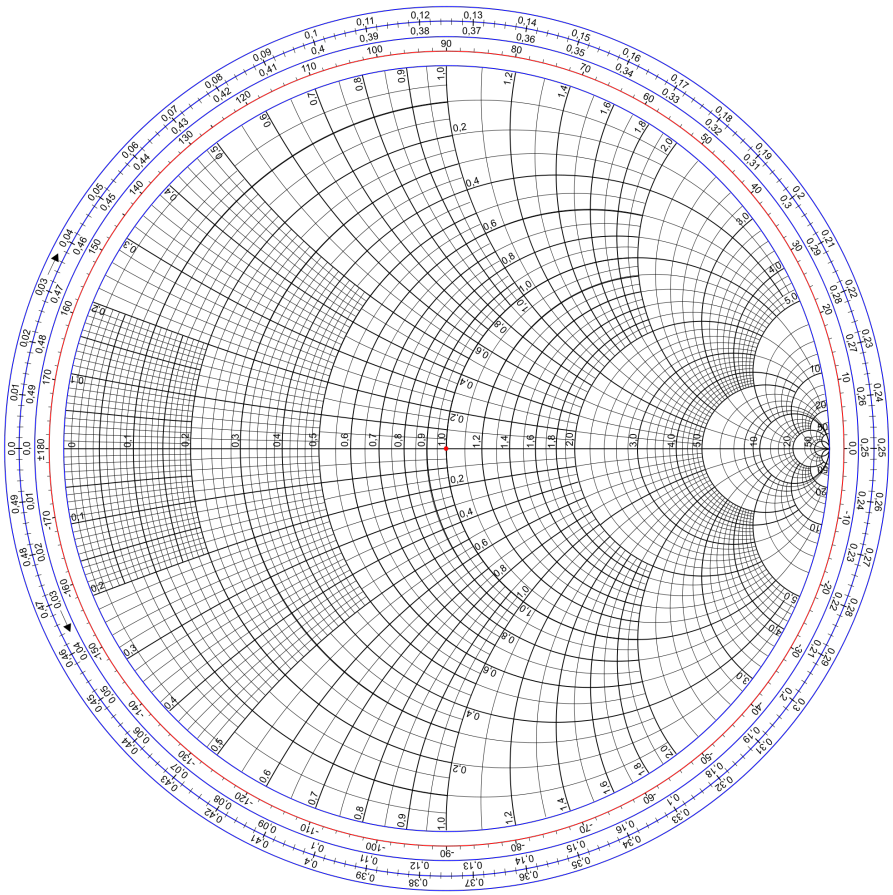


Figure B.1: The Smith Chart.

noting that the only possible movement is in clockwise direction; otherwise we would approach the open circuit point (right hand side of the chart) providing no solution at all. In other words, the series reactance can only be an inductance. Moreover, there exist two possible points which lead us to a normalized conductance $g = 1$, certifying the quadratic solution provided in the sensitivity analysis.

Then, we can cancel the reactive part of the resulting admittance by adding the parallel susceptance element jB. The goal of matching is to reach the centre of the chart, so in this case the rotation direction (and so the type of component) will be determined by the initial inductance selection.

The two solutions plotted in the Smith chart are shown in Figure B.2. The first option (or Option 1), represents the solution with the lowest trajectory from the load impedance z_L to the impedance circle with unity normalized conductance. The resulting impedance value is $z = 0.12 - j0.33$. This impedance transformation accounts for a normalized and absolute reactance values of

$$\Gamma = jx = z - z_L = 0.12 - j0.33 - (0.124 - j4) = j3.67 \tag{B.6}$$

$$X = xZ_0 = 3.67 \cdot 50 = 183.5 \tag{B.7}$$

As expected, the reactance is positive, which corresponds to an inductance. Knowing that the impedance of an inductor is specified as $2\pi f_0 L$, being f_0 the frequency of operation, the resulting inductance value L is

$$L_{series-Option1} = \frac{X}{2\pi f_0} = \frac{183.5}{2\pi 2.45 \cdot 10^9} = 11.92\,\text{nH} \tag{B.8}$$

The above inductance is required to provide an impedance with unity conductance. By simply rotating the chart by 180° we can observe that the resulting admittance has a value of $y = 1 + j2.69$. Working in the admittance domain permits easily introducing the next element in the network: the shunt susceptance. The value of the susceptance should be that which cancels the reactive part of the admittance in order to reach the centre of the Smith Chart $(1 + j0)$. That is,

$$jb = 1 + j0 - y = 1 + j0 - (1 + j2.69) = -j2.69 \tag{B.9}$$

$$B = \frac{b}{Z_0} = \frac{-2.69}{50} = -0.054 \tag{B.10}$$

Where b is the normalized susceptance of the shunt component. Interestingly, the required susceptance is negative. Therefore, the shunt component also corresponds to an inductance.

$$L_{shunt-Option1} = \frac{1}{2\pi f_0 B} = \frac{1}{2\pi 2.45 \cdot 10^9 \cdot (-0.054)} = 1.2\,\text{nH} \tag{B.11}$$

The second option (Option 2) plotted in Figure B.2, corresponds to the longest path between the load impedance and the impedance circle with unity normalized conductance. Given that we already know that the series reactance will be an inductor, we expect that its value will be larger than Option 1. In this case the resulting impedance value is $z = 0.12 + j0.33$. Intuitively, and since the rotation is still performed along the $r = 0.12$ circle, the resulting reactive part is the opposite as Option 1. Both normalized and absolute reactance values are thus

$$\Gamma = jx = z - z_L = 0.12 + j0.33 - (0.124 - j4) = j4.33 \tag{B.12}$$

$$X = xZ_0 = 4.33 \cdot 50 = 216.5 \tag{B.13}$$

Which corresponds to an inductance value of

$$L_{series-Option2} = \frac{X}{2\pi f_0} = \frac{216.5}{2\pi 2.45 \cdot 10^9} = 14.06\,\text{nH} \tag{B.14}$$

As expected, the obtained inductance value is larger than Option 1. The resulting admittance now has a value of $y = 1 - j2.69$. Thus, the required susceptance value to cancel the reactive part now becomes

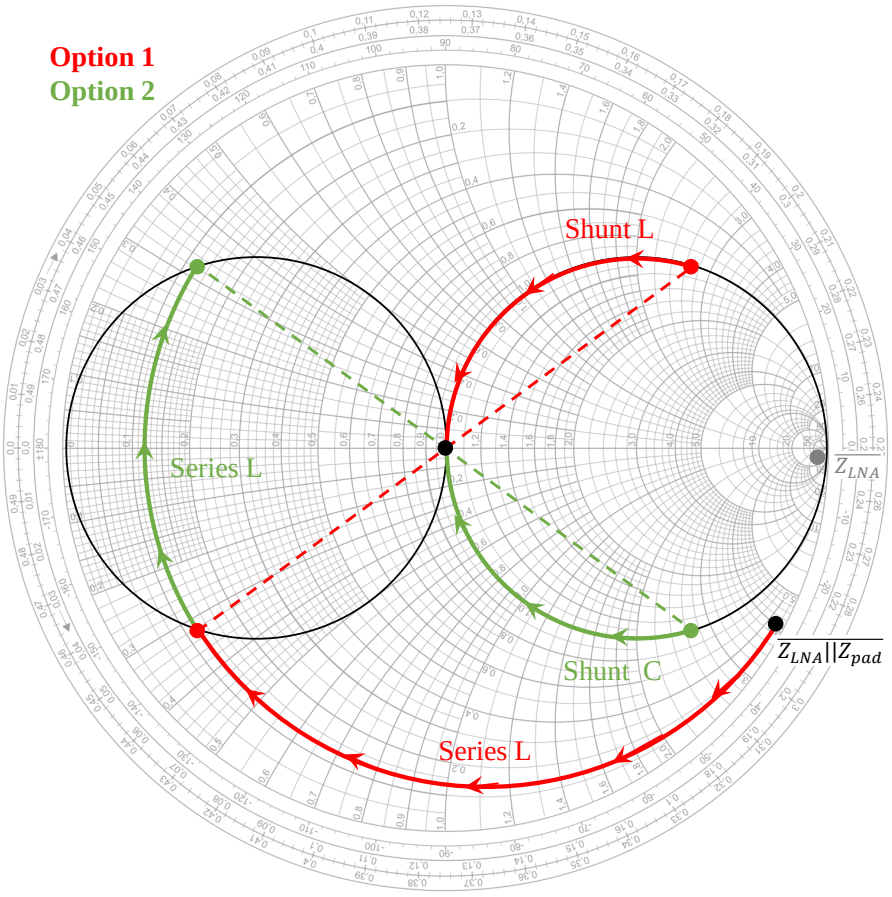


Figure B.2: Smith chart with solutions for Reversed-Pad L-section network.

$$jb = 1 + j0 - y = 1 + j0 - (1 - j2.69) = j2.69 \tag{B.15}$$

$$B = \frac{b}{Z_0} = \frac{2.69}{50} = 0.054 \tag{B.16}$$

Which means that the shunt component corresponds to a capacitor with a value

$$C_{shunt-Option2} = \frac{B}{2\pi f_0} = \frac{0.054}{2\pi 2.45 \cdot 10^9} = 3.5\,\text{pF} \tag{B.17}$$

So far it becomes quite evident that sketching matching schemes without almost any calculation at all is a valuable advantage. The real usefulness of this graphical representation resides in the insight and intuition gained by the user, as it easily permits evaluating potential actions to enhance the quality or viability of the current solution.

It is recommended to relax the value of the inductors such that the resulting parasitic resistance is minimized. By observing the Smith Chart, it will be shown

that additional capacitance at the input of the LNA reduces the input capacitance and the required inductance. When an additional 150 fF capacitance is used in parallel with the pad, the equivalent input impedance becomes $Z_L = 3 - j140$. The normalized impedance and the corresponding reflection coefficient are

$$z_L = \frac{Z_L}{Z_0} = 0.06 - j2.8 \tag{B.18}$$

$$\Gamma = \frac{0.06 - j2.8 - 1}{0.006 - j2.8 + 1} = 0.76 - j0.62 = 0.986\angle - 39.29^{\circ} \tag{B.19}$$

The current magnitude of the reflection coefficient is almost the same as the one obtained in B.5 while the phase has decreased around 11°. Graphically speaking, what this implies is that the load impedance still stands at the same distance from the centre of the Smith chart (due to having equal magnitudes), but now it is nearer and slightly left-sided to the impedance circle with unity normalized conductance. In turn, this is traduced into lower inductance values and higher capacitance for the Option 2, although it does not impose an obstacle due to the spread range of values offered by manufacturers. The main outcome derived from the analysis is that a new design variable may be used in the form of an additional shunt capacitance at the input of the amplifier such that the inductance values can be relaxed and tuned according to the solution which best suits our requirements. The whole solution with both options is plotted in the Smith chart of Figure B.3.

B.2 Pad-Reversed L-Section Network

The approach followed with this network (Figure A.2) differs from the previous one. Starting from the load towards the antenna, the last element in the chain is the pad capacitance. Given that $C_{pad} = 250\,\text{fF}$, the pad susceptance and its normalized values are

$$B_{pad} = 2\pi f_0 C_{pad} = 2\pi 2.45 \cdot 10^9 \cdot 250\,\text{fF} = 0.0038 \tag{B.20}$$

$$b_{pad} = B_{pad} Z_0 = 0.19 \tag{B.21}$$

Therefore, the resulting normalized admittance at the pad interface must be $y = 1 - j0.19$ such that b_{pad} is able to completely cancel the reactive part.

The first element of the network is directly interfacing the input of the LNA, so in this case the effective load impedance is $Z_L = 1697 - j2382\Omega$. Its normalized value is

$$z_L = \frac{Z_L}{Z_0} = 33.94 - j47.64 \tag{B.22}$$

The normalized resistive part of the load impedance exceeds 1. Therefore, the load will stand inside the unity resistance circle in the Smith chart. The next element is the series reactance jX, so the impedance domain is maintained. The absence

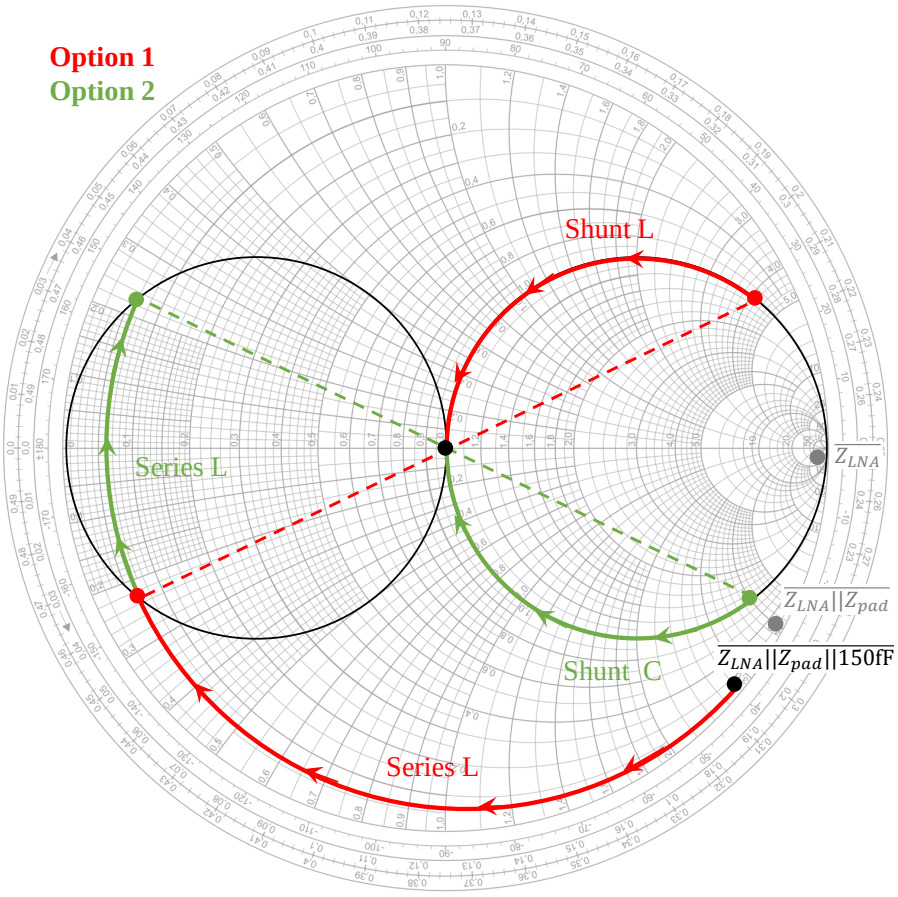


Figure B.3: Smith chart with solutions for Reversed-Pad L-section network including an additional 150 fF capacitance in parallel with the pad.

of a resistive component forces us to move along the $r = 33.94$ circle, which means that it is not possible to reach the $g = 1$ admittance circle like in the previous cases. This network thus explicitly requires the addition of a shunt component just before the LNA input such that the resulting impedance lies outside the $r = 1$ circle. According to the initial conditions of the Reversed-Pad L-section scenario, we may intuitively guess that adding a parallel capacitance will shift the starting load impedance as desired. A 250 fF capacitance permits emulating the previous pad-LNA configuration in order to establish a one-to-one comparison by modifying the original load impedance from $z_L = 33.94 - j47.64$ to $z_L = 0.12 - j4$, which clearly stays outside the $r = 1$ circle. The resulting series reactance is thus an inductance regardless of the option chosen, being the only difference the value of the shunt component as it shall account for the pad susceptance. The solution is graphically depicted in the Smith chart of Figure B.4.

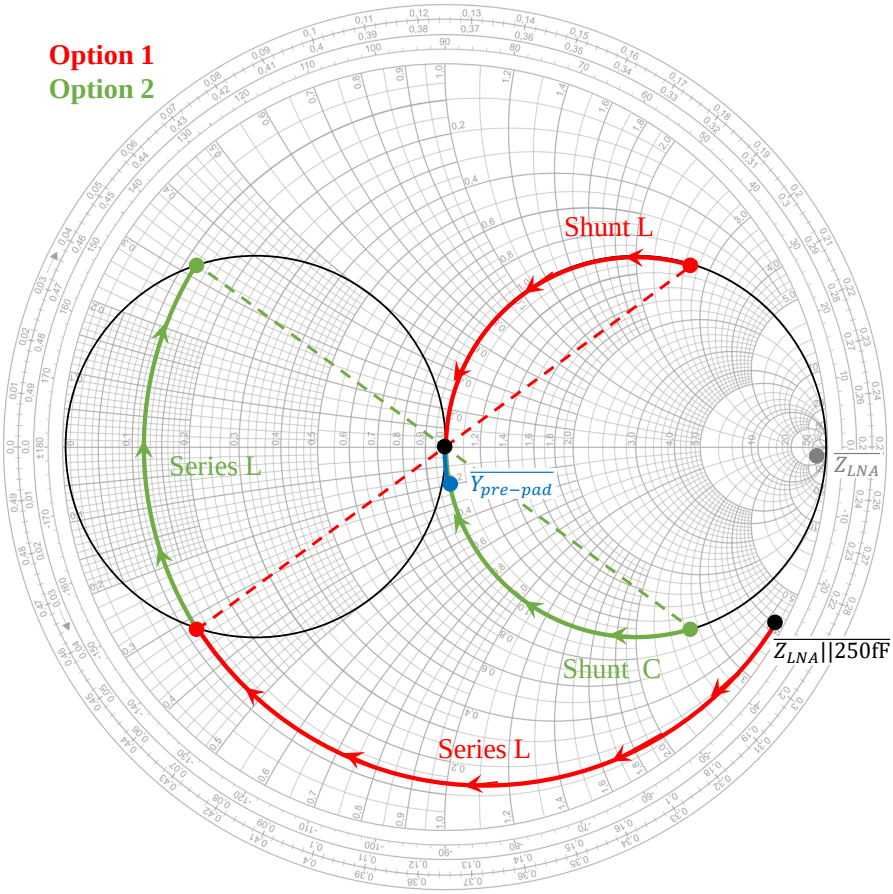


Figure B.4: Smith chart with solutions for Pad-Reversed L-section network including an additional 250 fF input capacitance.

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