Low-voltage organic thin-film transistors based on [n]phenacenes

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Abstract

Low-voltage p-channel organic thin-film transistors based on [n]phenacene (n = 5, 6 or 7) were fabricated on glass and on flexible poly(ethylene 2,6-naphthalate) (PEN) substrates. For the first time, these phenacenes were combined with two ultrathin gate dielectrics based on aluminium oxide and a monolayer of octadecyl-phosphonic acid in three different transistor structures. Regardless of the substrate and the transistor structure, the field-effect mobility is found to increase with increasing length of the conjugated [n]phenacene core, leading to the best performance for [7]phenacene. The largest average field-effect mobility we have obtained is 0.27 $cm^2/V{\cdot}s$ for transistors on glass and 0.092 $cm^2/V{\cdot}s$ for transistors on flexible PEN.

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1. Introduction

[n]Phenacenes are one-dimensional conjugated organic molecules that contain benzene rings fused in a zigzag pattern, where [n] represents the number of benzene rings. The zigzag pattern distinguishes the [n]phenacenes from the [n]acenes which consist of benzene rings fused linearly and include tetracene and pentacene. This difference in the arrangement of the benzene rings results in different electronic properties of [n]phenacenes compared with [n]acenes. [n]Phenacenes have a wider bandgap and a deeper highest occupied molecular orbital (HOMO), leading to lower reactivity and better environmental stability of devices based on them. Consequently, [n]phenacenes have attracted attention as promising organic semiconductors for p-channel organic thin-film transistors (TFTs) [1-7]. Previous reports showed excellent field-effect mobility in transistors based on single crystals of [n]phenacenes. These transistors were fabricated on oxidized silicon wafers and showed field-effect mobilities ranging from about 1 $cm^2/V{\cdot}s$ for [5]phenacene to about 11 $cm^2/V{\cdot}s$ for [9]phenacene [7]. One drawback of these transistors was the large threshold voltage, in excess of −30 V.

By reducing the thickness of the thermally grown SiO_2 gate dielectric and by taking advantage of high-permittivity gate dielectrics, a more desirable threshold voltage of about −6 V was achieved [4,8]. However, this reduction in the threshold voltage was accompanied by a substantial decrease in the field-effect mobility (often by a factor of 10 or more), since the semiconductor in these transistors was not a single-crystal, but a vacuum-deposited thin film. In these studies it was also observed that a more preferable molecular arrangement of the [n]phenacene molecules in the vacuum-deposited thin films was achieved when the semiconductor was deposited onto gate dielectrics with a small surface energy, e.g., SiO_2 coated with hexamethyldisilazane (HMDS) or parylene.

It is well-known that the operating voltage of a field-effect transistor is determined by the capacitance of the gate dielectric. Low-voltage operation can be achieved by employing a gate dielectric with a large capacitance, i.e. a dielectric having either a small thickness and/or a large permittivity. A well-established approach is the use of ultrathin bilayer gate dielectrics consisting of a thin layer of aluminum oxide prepared by the surface oxidation of the underlying aluminum gate electrode (providing large permittivity) and a self-assembled monolayer (SAM) of an alkylphosphonic acid (providing small surface energy) [9-14]. These bilayer dielectrics have a thickness of about 5 to 12 nm and provide a large capacitance (about 0.5 $\mu F/cm^2$), a small leakage-current density (below 5×10^{-8} A/cm^2 at 2 V) and a small surface energy (about 17.5 mJ/m^2) [14]. By employing such gate dielectrics in organic TFTs based on the small-molecule semiconductor dinaphtho[2,3-b:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT), the threshold voltage was reduced to about −0.5 V, providing operating voltages compatible with state-of-the-art silicon microelectronics [11,15].

In this report, we fabricated and investigated organic TFTs based on [n]phenacenes with n = 5, n = 6 and n = 7. In an attempt to reduce the threshold voltage of the TFTs to less than 1 V, we combined [n]phenacenes with ultrathin gate dielectrics based on aluminium oxide (AlO_x) and an octadecyl-phosphonic acid ($C_{18}PA$) SAM. In the first round, TFTs were fabricated on flexible poly(ethylene 2,6-naphthalate) (PEN) substrates, and two different multi-finger source/drain contact TFT architectures (leading to different channel width-to-length ratios) were investigated. In some transistors, the interface between the source/drain contacts and the organic semiconductor was modified. The interfacial layer consisted of [m]phenacene ($m \neq n$) with a different length than the [n]phenacene employed for the semiconductor layer. Since longer phenacenes have a smaller bandgap and/or deeper HOMO level than shorter phenacenes, the

insertion of a thin layer of a longer or shorter phenacene between the contact metal and the semiconductor could modify the injection of carriers at the metal-semiconductor interface. In the second fabrication round, TFTs with 'standard' source/drain contacts were fabricated on glass. The glass substrate and the standard TFT structure were selected to check if the choice of the substrate and/or the transistor channel geometry played a role. In addition, two different $AlO_x/C_{18}PA$ dielectrics were used [11,14] and the TFTs had no interfacial layer between the source/drain contacts and the organic semiconductor.

2. Experimental procedures

[5]phenacene, [6]phenacene and [7]phenacene were prepared according to the procedure published by H. Okamoto [16], in which the Mallory homologation protocol is employed [17]. Octadecyl-phosphonic acid was purchased with 97% purity (Strem Chemicals, USA) and purified by recrystallization from hot hexane solution using decolorizing charcoal.

In the first fabrication round low-voltage bottom-gate, top-contact p-channel TFTs [14,15] based on [n]phenacenes (n = 5, 6 or 7) were fabricated on PEN (Optfine PQA1, DuPont Teijin). Transistors with two different multi-finger source/drain contact geometries [15] were produced. The nominal dimensions of the 'wide-gate' multi-finger TFTs are L = 50 μm and W = 18.23 mm, while those of the 'narrow-gate' multi-finger TFTs are L = 20 μm and W = 4.03 mm. In the second fabrication round 'standard' TFTs with nominal channel length L = 30 μm and channel width W = 1 mm were fabricated on glass (Ossila, U.K.). Figure 1(a) shows a cross-section of the TFTs fabricated on PEN and Figure 1(b) depicts the phenacene molecules used in this study. Figures 1(c), 1(d) and 1(e) show the schematic top views of the standard, wide-gate and narrow-gate TFTs, respectively.

The TFTs fabricated on the flexible PEN substrates have aluminum gate electrodes deposited by thermal evaporation in vacuum and a bilayer gate dielectric consisting of aluminum oxide (AlO_x) prepared by UV/ozone oxidation of the surface of the gate electrodes [18] and an octadecyl-phosphonic acid ($C_{18}PA$) SAM prepared by thermal evaporation in vacuum [14]. The details of the SAM preparation are given in [12]. The [n]phenacene semiconductor layer has a thickness of 50 nm and was deposited in vacuum at room temperature. Gold source and drain contacts were evaporated onto the semiconductor layer. In some cases, an interfacial layer was deposited between the semiconductor layer and the source/drain contacts. The interfacial layer was made of a longer or shorter phenacene. Since [5], [6], and [7]phenacenes exhibit a slight variation in their HOMO level [1], one may expect a slight modification in the injection properties of such source/drain contacts.

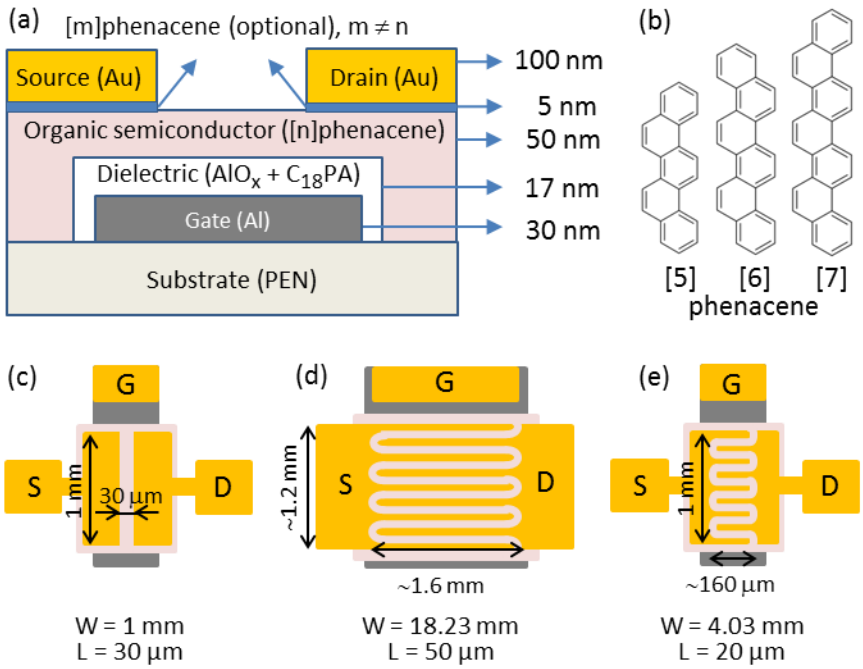

Figure 1. Cross-section of a phenacene transistor on a PEN substrate (a); [n]phenacenes (b); and top views of standard (c), wide-gate (d) and narrow-gate (e) transistors.

The TFTs fabricated on glass had the same layer structure, except that no interfacial layer between the semiconductor and the contacts was used and the thickness of the semiconductor layer was at least 100 nm. In addition, two different preparation methods for the $AlO_x/C_{18}PA$ gate dielectrics were used to provide a direct comparison between them: For some of the TFTs, the AlO_x layer was prepared by UV/ozone oxidation of the surface of the gate electrodes (having a thickness of about 15 nm) and the $C_{18}PA$ SAM was prepared by vacuum evaporation [14] (as shown in Figure 1(a) for TFTs on PEN), while for the other TFTs, the AlO_x layer was prepared by plasma oxidation of the surface of the gate electrodes (having a thickness of about 3.6 nm) and the $C_{18}PA$ SAM was prepared in solution [9]. To differentiate between these two $AlO_x/C_{18}PA$ bi-layer dielectrics, we will refer to them as 'vacuum-prepared' and 'solution-prepared', respectively.

The electrical measurements were performed using an Agilent B1500A Semiconductor Parameter Analyzer in a dark environment in ambient air.

3. Results

Figure 2(a) shows the measured transfer characteristics of a [7]phenacene narrow-gate TFT on PEN. The gate-source voltage V_{gs} was swept from 0 to −6 V and back, while the drain-source voltage V_{ds} was kept constant at −6 V. The TFT exhibits a threshold voltage of −3.28 V, a field-effect mobility of 0.027 cm^2/Vs and a subthreshold slope of 110 mV/decade. The capacitance of the gate dielectric is 0.24 $\mu F/cm^2$. The on-off current ratio is about 5×10^5. Figure 2(b) depicts a set of output characteristics of the same TFT. The drain-source voltage was swept from 0 to −6 V and back, while V_{gs} was gradually stepped up. The TFT exhibits good behavior for V_{gs} up to about −4.5 V. For higher V_{gs}, a slight deviation from linear behavior is observed at low V_{ds}.

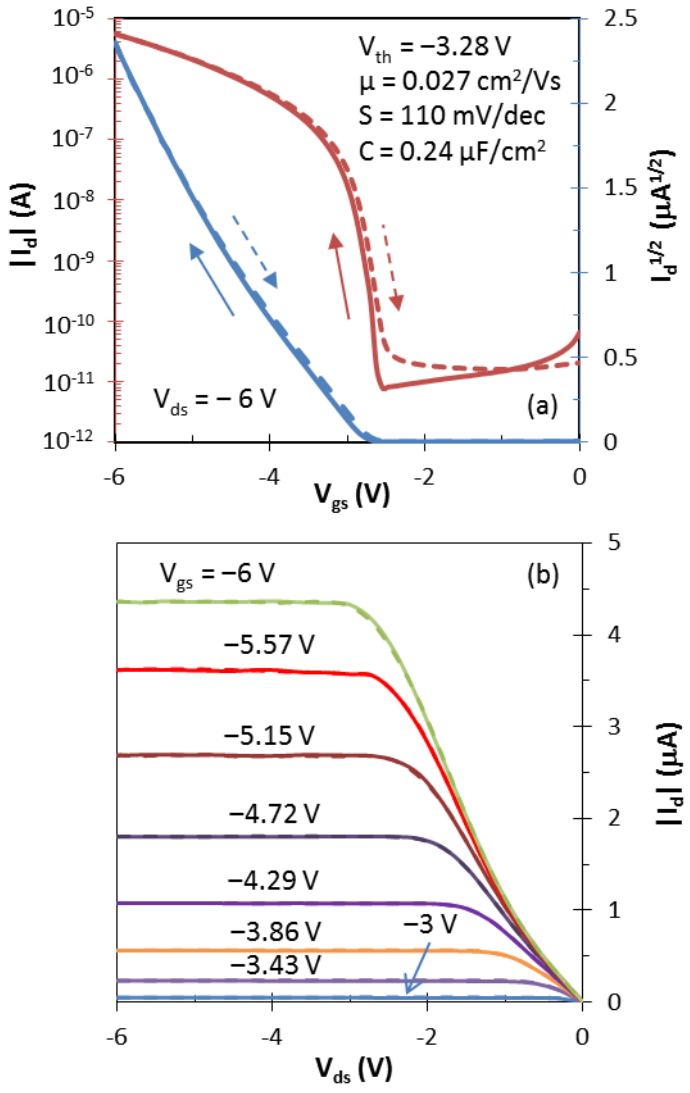

Figure 2. Transfer (a) and output (b) characteristic of a narrow-gate TFT based on [7]phenacene on a PEN substrate.

Figure 3 summarizes how the length of the [n]phenacene molecule affects the field-effect mobility, the threshold voltage, and the on-state drain current of the narrow-gate and the wide-gate TFTs fabricated on PEN. As can be seen, the mean value of the field-effect mobility increases with increasing phenacene length, both for the narrow-gate and the wide-gate TFTs. For all [n]phenacenes, the wide-gate TFTs show higher mean mobility when compared to the

narrow-gate TFTs. In addition, as the phenacene length increases, so does the difference between the mobility of the narrow-gate and the wide-gate TFTs. Consequently, the highest mean mobility of 0.092 $cm^2/V{\cdot}s$ was achieved for wide-gate TFTs based on [7]phenacene.

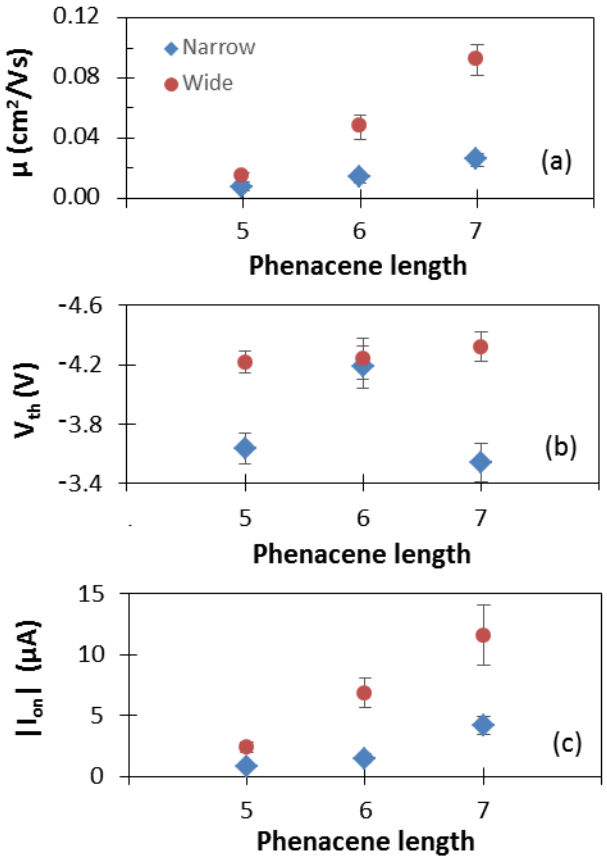

Figure 3. Field-effect mobility (a), threshold voltage (b), and on-state drain current (c) as functions of the length of the [n]phenacene molecule for narrow- and wide-gate TFTs on PEN substrates. The on-state drain current was extracted at $V_{ds} = V_{gs} = -6$ V.

The mean threshold voltage shows a different behavior with respect to the length of the [n]phenacene molecules for both the narrow-gate and the wide-gate TFTs. In fact, with the exception of the narrow-gate TFTs with [6]phenacene, the threshold voltage is unaffected by the choice of phenacene, even though the wide-gate TFTs exhibit a higher threshold voltage of about

−4.3 V when compared to the narrow-gate TFTs, which exhibit a threshold voltage of about −3.6 V.

Finally, the behavior of the on-state drain current is qualitatively similar to that of the field-effect mobility. For both the wide-gate and the narrow-gate TFTs, the on-state drain current increases as the phenacene length increases, leading to an on-state drain current of about 12 μA for the wide-gate [7]phenacene TFTs.

Figure 4 shows a summary of the field-effect mobility, threshold voltage, and on-state drain current (extracted at $V_{ds} = V_{gs} = -6$ V) when the [m]phenacene interfacial layer is inserted between the [n]phenacene semiconductor ($m \neq n$) and the source/drain contacts. The mean values for the narrow-gate TFTs are represented by diamonds while the parameters of the wide-gate TFTs are shown as circles. Empty symbols depict the values of the reference TFTs without interfacial layer.

For the [5]phenacene TFTs, the insertion of a [7]phenacene interfacial layer did not affect the field-effect mobility. The addition of a [5]phenacene or [7]phenacene interfacial layer to the [6]phenacene TFTs led to a slight reduction in the field-effect mobility. The addition of a [5]phenacene interfacial layer to the [7]phenacene TFTs made no difference, while the addition of a [6]phenacene interfacial layer to the [7]phenacene TFTs led to a slight increase in the field-effect mobility. Overall, one would conclude that the addition of the interfacial layer does not lead to a measurable improvement in the field-effect mobility of the TFTs.

The addition of the interfacial layer leads to a reduction of the threshold voltage for almost all combinations of semiconductor and interfacial material. The greatest threshold-voltage reduction is observed when combining [5]phenacene and [7]phenacene. Using [5]phenacene for

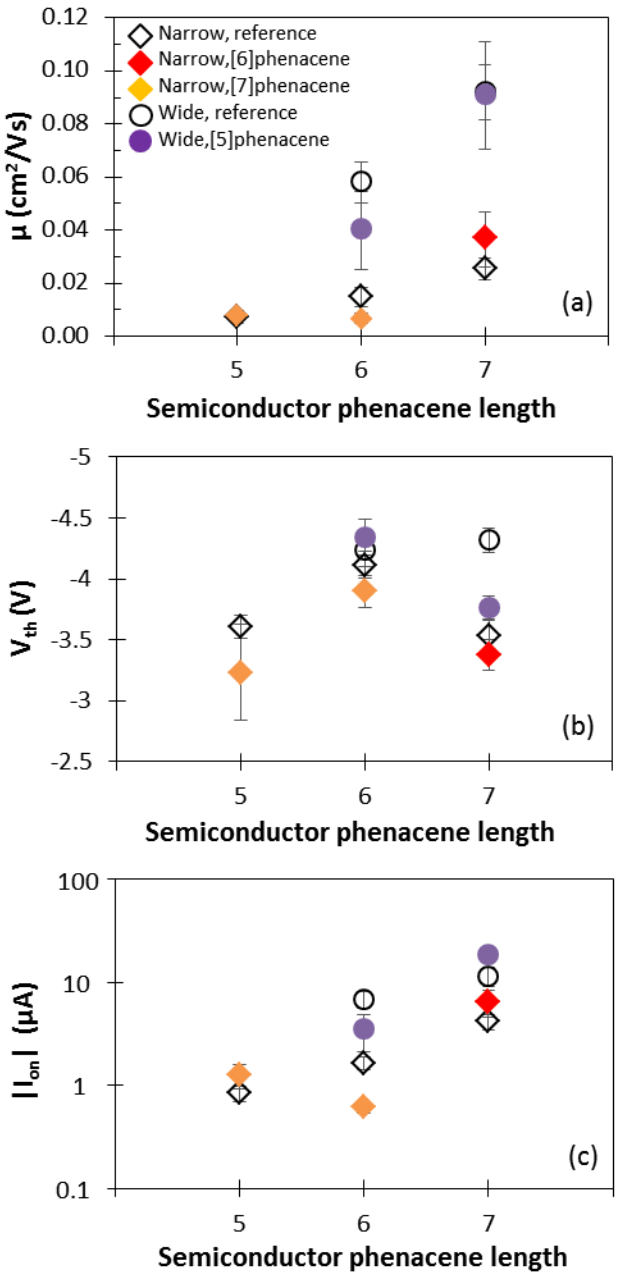

Figure 4. Field-effect mobility (a), threshold voltage (b), and on-state drain current (c) of wide-(•) and narrow-gate (♦)TFTs on PEN substrates as a function of the length of the [n]phenacene molecule employed for the semiconductor layer. The [m]phenacene molecule (m ≠ n) used for the interfacial layer is indicated in purple for [5]phenacene, red for [6]phenacene and yellow for [7]phenacene. The results from the reference TFTs without interfacial layer are shown with empty symbols.

the semiconductor layer and [7]phenacene for the interfacial layer, the threshold voltage decreased by about 0.4 V, while employing [7]phenacene as the semiconductor and [5]phenacene as the interface material resulted in a reduction of the threshold voltage by about 0.55 V.

The on-state drain current is decreased when [6]phenacene is used for the semiconductor layer in combination with [5]phenacene or [7]phenacene for the interfacial layer. Otherwise, a slight increase in the on-state drain current is observed when the interface between the source/drain contacts and the semiconductor in [5]phenacene or [7]phenacene TFTs is modified.

Next, the output characteristics of various phenacene transistors, with and without the source/drain interfacial layer, were measured and the results are summarized in Table 1. The source/drain contacts are listed as 'Ohmic' when the drain current increased linearly for small V_{ds}, for V_{gs} up to –6 V. Alternatively, the source/drain contacts are called 'Schottky' if the drain current rose non-linearly, as seen in Figure 2(b) for small V_{ds}. The rational for using these terms is explained later.

Table 1. Properties of the source/drain contacts for various OTFTs. DNTT transistors fabricated alongside the phenacene TFTs are added for comparison.

		Interfacial layer			
		None	[5]phenacene	[6]phenacene	[7]phenacene
Semiconductor	[5]phenacene	Ohmic		not available	Ohmic
	[6]phenacene	Schottky	Schottky		Schottky
	[7]phenacene	Schottky	Schottky	Schottky	
	DNTT	Ohmic	Ohmic	not available	Ohmic

As seen from Table 1, transistors based on DNTT and [5]phenacene display Ohmic source/drain contacts, regardless of whether the interfacial layer is used. On the other hand, TFTs based on [6]phenacene and [7]phenacene display Schottky-like behavior of the

source/drain contacts. The insertion of the thin interfacial layer (about 2 monolayers) does not fundamentally change this behavior in any transistor system.

Table 2 summarizes the results from the 'standard' TFTs fabricated on glass substrates. In this case, two types of gate dielectrics were used, namely the vacuum- and solution-prepared. In addition, the thickness of the semiconductor layer was larger than in the TFTs fabricated on PEN. With the exception of the gate dielectric, the TFTs were fabricated side by side. Table 1 lists the gate-dielectric capacitance C_{diel}, the field-effect mobility μ and the threshold voltage V_{th} in the saturation regime, the on-state drain current I_{on} (at $V_{gs} = V_{th} - 1V$ and $V_{ds} = -5$ V), and the off-state drain current I_{off} (the smallest drain current at $V_{ds} = -5$ V).

Table 2. Parameters of standard TFTs fabricated on glass with ultra-thin $AlO_x/C_{18}PA$ gate dielectrics prepared using two different procedures.

Gate dielectric	Semicon-ductor	C_{diel} ($\mu F/cm^2$)	μ (cm^2/Vs)	V_{th} (V)	$\lvert I_{on}\rvert$ (A) @ $V_{th} - 1V$	$\lvert I_{off}\rvert$ (A)
Solution-prepared [11]	[5]phenacene	0.70	0.0015	–3.96	2.36×10^{-8}	1.94×10^{-13}
	[6]phenacene	0.70	0.025	–3.89	4.34×10^{-7}	7.91×10^{-13}
	[7]phenacene	0.70	0.27	–3.40	4.17×10^{-6}	1.88×10^{-12}
Vacuum-prepared [14]	[5]phenacene	0.30	0.0093	–5.49	6.40×10^{-8}	5.76×10^{-14}
	[6]phenacene	0.30	0.010	–4.95	9.26×10^{-8}	1.09×10^{-13}
	[7]phenacene	0.30	0.031	–4.53	1.95×10^{-7}	3.36×10^{-13}

As seen with the TFTs fabricated on PEN, the transistors on glass with [7]phenacene as the semiconductor also showed the best electrical performance, namely the highest field-effect mobility and the smallest threshold voltage. For both gate dielectrics, as the length of the [n]phenacene molecules increases, the field-effect mobility increases, the threshold voltage decreases, the on-state drain current increases, and the off-state drain current also slightly increases. Furthermore, the solution-prepared gate dielectric displays a more dramatic effect on

the field-effect mobility (μ = 0.0015 $cm^2/V{\cdot}s$ for [5]phenacene, 0.27 $cm^2/V{\cdot}s$ for [7]phenacene) compared to the vacuum-prepared gate dielectric (μ = 0.0093 $cm^2/V{\cdot}s$ for [5]phenacene, 0.031 $cm^2/V{\cdot}s$ for [7]phenacene). In addition, the solution-prepared gate dielectric led to smaller threshold voltages for all [n]phenacenes. However, the vacuum-prepared gate dielectric led to lower off-state drain currents for all [n]phenacenes.

Comparing the standard TFTs on glass to those fabricated on PEN (all with the vacuum-prepared dielectric), one observes that the former exhibit field-effect mobilities similar to those of the narrow-gate TFTs on PEN. At the same time, the standard TFTs on glass have larger threshold voltages than the narrow-gate TFTs on PEN.

4. Discussion

For TFTs fabricated on flexible PEN substrates, the wide-gate Au/[7]phenacene/C_{18}PA/AlO_x/Al devices exhibited the best performance, with an average field-effect mobility of 0.092 $cm^2/V{\cdot}s$ and a threshold voltage of –4.32 V. On glass substrates, the standard transistors that combined [7]phenacene with solution-prepared gate dielectric exhibited the highest mobility of 0.27 $cm^2/V{\cdot}s$ and a threshold voltage of –3.40 V. These field-effect mobilities are similar to those realized in previous studies of low-voltage [n]phenacene TFTs [4,8]. However, the threshold voltages achieved here are smaller and the TFTs exhibit improved contact properties. Previously, [5]phenacene TFTs with a ZrO_2 gate dielectric showed a field-effect mobility of 0.036 $cm^2/V{\cdot}s$ and a threshold voltage of –6.7 V, [5]phenacene TFTs with a HfO_2 gate dielectric exhibited a mobility of 0.015 $cm^2/V{\cdot}s$ and a threshold voltage of –6.9 V, [5]phenacene TFTs with a $Ba_xSr_{1-x}TiO_3$ gate dielectric had a mobility of 0.0019 $cm^2/V{\cdot}s$ and a threshold voltage of –4.0 V, [5]phenacene TFTs with a parylene/Ta_2O_5 gate dielectric showed a

mobility of 0.54 $cm^2/V{\cdot}s$ and a threshold voltage of –6.2 V [8], and [6]phenacene TFTs with a parylene/Ta_2O_5 gate dielectric exhibited a mobility of 0.09 $cm^2/V{\cdot}s$ and a threshold voltage of –5.4 V [4]. However, in most of the previously reported low-voltage [n]phenacene TFTs, the output characteristics exhibited a strong diode-like behavior for drain-source voltages of up to a few volts.

Modifying the interface between the source/drain contacts and the semiconductor layer did not improve the transistor performance and only a slight reduction in threshold voltage was observed. The field-effect mobility is about the same, regardless of the presence of the interfacial layer, indicating that this property is controlled mainly by the molecular arrangement of the [n]phenacene molecules within the semiconductor layer. In fact, in all cases the mobility increases with increasing length of the [n]phenacene molecules, most likely as a result of stronger intermolecular interactions in the case of the longer [n]phenacenes. One can also observe that the preparation method of the phosphonic acid monolayer affects the field-effect mobility of the TFTs. Even though the solution- and vacuum-prepared C_{18}PA SAMs have similar water contact angles (macroscopic properties) [14,19], they are likely to differ on the microscopic scale. One would predict that the density of vacuum-prepared SAMs is lower than that of their solution-prepared counterparts as a result of the laws that govern physical vapor deposition. We have shown previously that the microscopic changes in the morphology of the vacuum-prepared SAMs have profound effects on the field-effect mobility of the TFTs based on dinaphtho[2,3-b:2',3'- f]thieno[3,2-b]thiophene (DNTT), even though these SAMs have similar water contact angles and surface energies. [14] Consequently, it is not surprising that the solution- and vacuum-prepared SAMs lead to [n]phenacene TFTs with different field-effect mobilities.

The non-linear response of the drain current for small source-drain voltages suggests the presence of carrier injection/extraction barriers. Schottky barrier may be formed at the interface between metal and semiconductor if their work functions are different and the interface is free of carrier traps (the presence of such traps will help the carriers to move/tunnel across the energy barrier, giving rise to Ohmic-like contact behavior). To avoid Schottky-like contacts in organic transistors the Fermi level of the source/drain metal and the HOMO (or LUMO) of the organic semiconductor should be aligned. If they are not, Schottky barriers may form. This has been recently studied for TFTs employing 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT) and Ag source/drain contacts [20]; the work function of Ag was modified from 4.2 to 5.2 eV, while the HOMO of C8-BTBT was 5.7 eV. The combination of Au (work function of ~5.1 eV [5]) and [n]phenacenes (HOMO increasing from 5.5 to 5.7 eV when [n] rises from 5 to 7 [1,5]) leads to a similar situation. Consequently, it is not surprising to observe Schottky-like behavior for TFTs with longer phenacene molecules, while such behavior is absent in DNTT transistors (HOMO of ~5.3 eV [21]).

Finally, we have demonstrated that the combination of [n]phenacenes with thin AlO_x/SAM bilayer gate dielectrics leads to low-voltage TFTs. Further optimization of the source/drain contacts and/or the use of [n]phenacenes with n > 7 hold promise for future low-voltage TFTs based on such organic semiconductors.

5. Conclusions

Low-voltage thin-film transistors based on [5], [6] and [7]phenacene were fabricated on glass and on flexible PEN substrates. Three different transistor structures were implemented, a ‘standard’ structure with a channel length of 30 μm and a channel width of 1 mm (on glass), a

'wide-gate' multi-finger structure with a channel length of 50 μm and a channel width of 18.23 mm (on PEN), and a 'narrow-gate' multi-finger structure with a channel length of 20 μm and a channel width of 4.03 mm (also on PEN). In some cases, two different methods for the preparation of the AlO_x/SAM gate dielectric were used, and the interface between the source/drain contacts and the semiconductor layer was modified by inserting a thin layer of [n]phenacene that had a different length than that used for the semiconductor layer.

For TFTs fabricated on PEN, the wide-gate Au/[7]phenacene/C_{18}PA/AlO_x/Al TFTs exhibited the best performance, with an average field-effect mobility of 0.092 $cm^2/V{\cdot}s$ and a threshold voltage of –4.32 V. On glass, the TFTs that combined [7]phenacene with a C_{18}PA SAM prepared from solution exhibited the highest mobility of 0.27 $cm^2/V{\cdot}s$ and a threshold voltage of –3.40 V. While the field-effect mobilities are similar to those reported previously for low-voltage [n]phenacene TFTs, a reduction in the threshold voltage, substantially improved source/drain carrier injection/extraction properties, and nearly hysteresis-free behavior were achieved. The insertion of the interfacial contact layer did not significantly improve the TFT performance, only a slight reduction in the threshold voltage was observed.

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