ELSEVIER

Journal of Neuroscience Methods 56 (1995) 195–202

JOURNAL OF NEUROSCIENCE METHODS

Design of the EPC-9, a computer-controlled patch-clamp amplifier. 1. Hardware

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Received 30 March 1994; revised 13 July 1994; accepted 21 July 1994

Abstract

The EPC-9 patch-clamp amplifier is a digitally controlled analog device for recording currents in membrane patches and in small cells. It has neither front-panel controls nor internal trim adjustments; instead all gain, range-changing, transient cancellation, calibration and other functions are computer controlled. Novel aspects of the circuit design of this instrument are discussed, with special reference to the issues of allowing computer control of all functions.

Keywords: Patch clamp; Ion channel; Computer; Electrophysiology; Data acquisition

1. Introduction

This and the following paper (Sigworth et al., 1995) describe the design of the EPC-9 patch-clamp amplifer. The goals in designing this instrument were to provide functionality similar to that of the conventional EPC-7 patch clamp: the head stage has switched resistors for recording single-channel, whole-cell and loose-patch currents; series resistance compensation is provided in conjunction with transient cancellation of cell membrane capacitance; and a variable, 4-pole filter is provided for filtering the current monitor signal. The difference from previous designs is that we wished to provide digital control of all functions of the amplifier, with two advantages in mind. First, if a computer controls all the functions of the amplifier, then a data-acquisition program can access and store variables that describe all of the settings during an experiment. Second, computer control allows a number of operations to be automated. These include automatic mode switching (e.g., switching between the settings for establishing a seal and those for single-channel recording) and also the automatic adjustment of capacitive transient cancellation and series-resistance compensation. We decided in fact to implement digital control of every adjustable parameter in the amplifier circuitry, including the calibration adjustments. The result is that the EPC-9 analog circuit board has no trimmer potentiometers. Precision components (such as laser-trimmed operational amplifiers) are used where possible. Where large component tolerances are unavoidable (e.g., the headstage resistors) appropriate digitally controlled adjustments are provided, and a set of calibration parameters for these adjustments is determined by an automatic calibration program. The parameters are stored in a file on the host computer.

The digital control of the analog circuitry is mainly performed through multiplying digital-to-analog converters (mDACs). These devices are used like variable resistors, the conductance of which can be changed in fixed increments according to the digital value written to them. The introduction of this sort of digital control to a patch-clamp amplifier presented two main problems. First, some signals in the instrument must have a very low noise level. The resistor networks in commercial mDAC devices have resistances that are high enough to introduce an excessive thermal voltage noise. We therefore had to build our own extended mDACs having lower impedance levels. Second, very good linearity is required of variable-gain elements in the current-injection and measurement circuitry so that large artifactual signals can be reliably subtracted to reveal

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SSDI 0165-0270(94)00128-6

the desired single-channel signals which are sometimes 3 orders of magnitude smaller. To maintain this linearity in critical places we used power MOS transistors as low-resistance switching elements instead of conventional analog-switch devices.

2. Overview of the circuitry

The general scheme of analog signal processing in the EPC-9 is identical to that in the EPC-7 patch clamp and is based on the principles outlined in Sigworth (1994). The circuitry is summarized in Fig. 1. The headstage uses current-measuring resistors of 50 GΩ, 500 MΩ and 5 MΩ; the lowest resistor value provides a new low-sensitivity range intended for use in 'loose patch clamp' recordings (Stühmer et al., 1983). The current-monitor signal passes through a stage of transient-response correction (correcting for distributed capacitances in the high-value resistors), a filter, a high-frequency boost stage (correcting the main pole introduced by stray capacitance with the 50 GΩ and 500 MΩ resistors) and an output amplifier and filter. A comparator checks for saturation of this chain of amplifiers to alert the user of non-linear amplification. In the normal voltage-clamp mode the stimulus is applied through a scaling amplifier, filter, summing amplifiers and a driver to the reference input of the headstage amplifer. In current-clamp mode the stimulus is diverted to form the reference input for the current-clamp feedback amplifier.

Compensation for capacitive transient currents on the input is provided by the C-Fast and C-Slow circuits. The C-Fast amplifier presents a scaled and filtered version of the stimulus signal to a 1 pF injection capacitor in the headstage. In the C-Slow generator a state-variable filter operates on the stimulus signal to produce a signal applied to both the 1 pF and 10 pF injection capacitors, and also modifies the stimulus to rapidly charge cell membrane capacitance ('prediction' as described in Sigworth (1994) or 'supercharging', Armstrong and Chow (1987)). A series resistance (R_s)

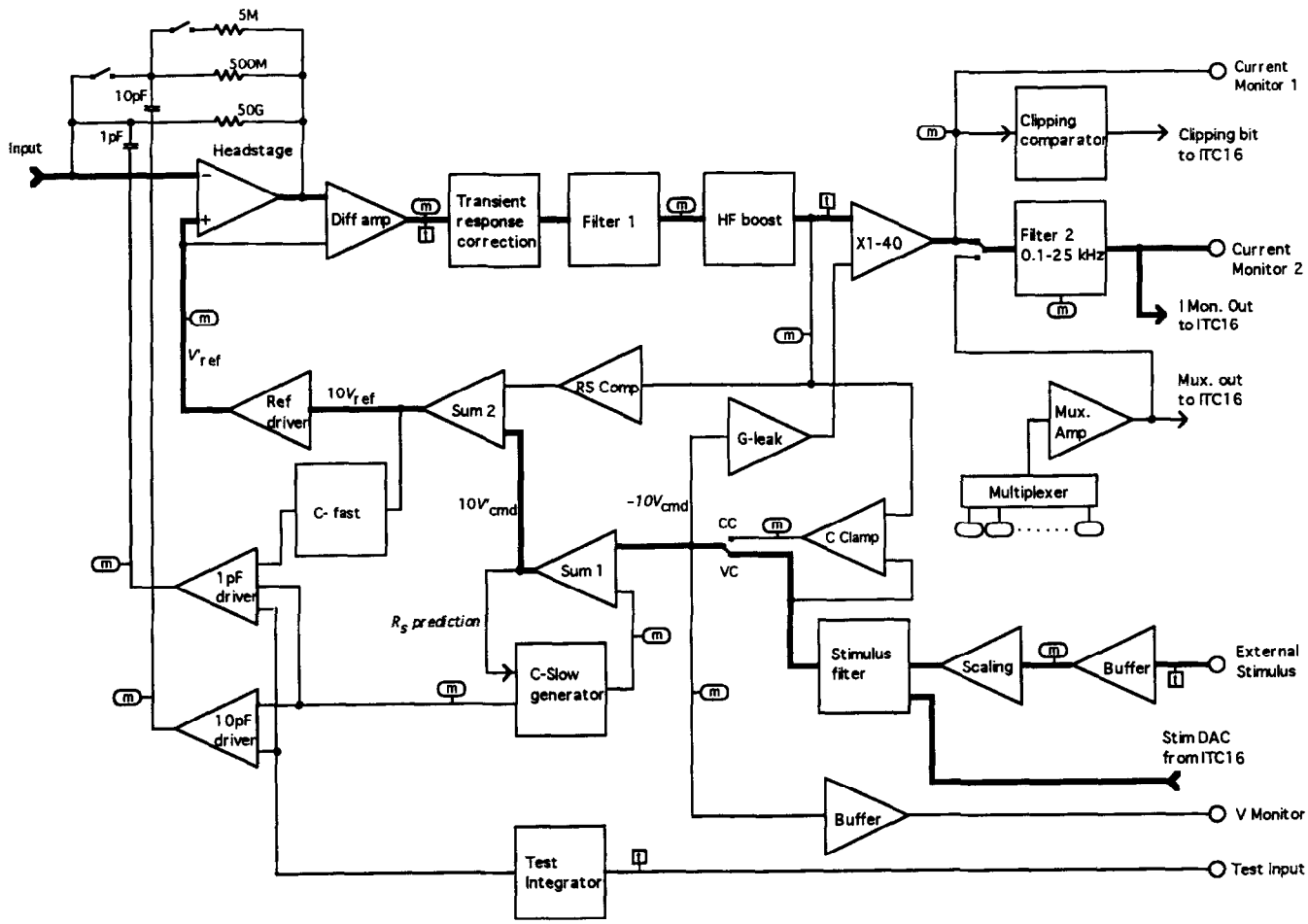

Fig. 1. Block diagram of the EPC-9 analog circuitry. Bold lines indicate the major signal pathways: in the upper part of the figure the current monitor pathway leads from the *Input* terminal to the *Current Monitor 2* output; in the lower part of the figure, the command voltage pathway starts at the right with the *External Stimulus* and *Stim DAC* signals and ends with the V'_{ref} signal applied to the headstage amplifier. Internal test points (*m*) are brought through the multiplexer to an ADC channel for self-test and calibration. Test signals can be injected into the circuitry from a dedicated DAC at 4 points in the circuitry (*t*).

compensation amplifier produces a scaled curent-monitor signal that is added to the headstage reference voltage V_{ref}. Finally, an auto-zeroing 'test integrator' (Sigworth, 1994) is provided to allow currents to be injected through capacitors into the headstage input to test the gain and freqency response of the amplifier.

To allow for automatic test and calibration of the analog circuitry, 14 test points in the circuitry are brought to a multiplexer for sampling by an analog-to-digital converter (ADC). Analog switches allow the injection of the signal from a dedicated DAC at 4 points in the circuit.

The implementation of this circuitry utilizes a total of 42 operational amplifiers. Digital control is performed by 22 mDACs, 13 quad analog switch chips, and 8 additional switch elements. These devices implement a total of 8 continuously variable parameters (e.g., C-Slow capacitance, Filter 2 bandwidth) that would be set by the user, and 10 discrete parameters that correspond to front-panel switches. They also implement various self-test and offset and gain trimming functions. Although the number of devices seems large, it should be kept in mind that some individual user controls require the action of several devices. For example, to set the 4-pole Filter 2 requires that four mDACs be loaded, while a change of the headstage resistor involves loading new values into 5 mDACs and operating four switch elements.

The mDACs and switches are supplied by a 15-line digital bus consisting of 8 data lines, 5 address lines and 1 strobe line. The devices used do not allow reading back their stored data. This is unfortunate since it precludes direct self-testing of the digital circuitry and it also means that the controlling software must maintain a shadow copy of the state of the digital devices. However it does allow a simple 'write-only' bus to be used. To minimize interference with the very sensitive analog circuitry, we chose to make this a 'quiet' digital bus on which there is no activity except when data are actually written to the devices on the bus. With conventional patch-clamp amplifiers the user rarely makes parameter changes during a sensitive recording; if changes are made, signal artifacts typically result. Similarly in the EPC-9, digital artifacts are expected only when parameters are changed.

The EPC-9 contains no processor in itself, but relies on software running on a host computer to provide initialization, control and calibration of its analog functions. The interface to the host computer is an Instrutech ITC-16 interface, which provides four 16-bit DACs, a 200 kHz 14-bit ADC, and 16 digital I/O lines. The inputs and outputs are optically isolated from the host computer ground, which is of great advantage since induced ground signals of ~ 1 μV can cause significant interference. Two DAC channels are dedicated to providing stimulus voltages and test signals, respectively, leaving the 2 remaining DACs free for other uses. Similarly 2 of the 8 ADC channels are dedicated to sampling the Filter 2 output (i.e., the current monitor signal) and the internal multiplexer output; the remaining 6 ADC channels are left free.

3. Head stage

The head stage consists of a low-noise operational amplifier, feedback resistors of 50 GΩ, 500 MΩ and 5 MΩ, and current-injection capacitors of 1 pF and 10 pF (Fig. 2). The operational amplifier is basically the same as that described previously (Sigworth, 1994). It consists of a preamplifier stage using a U430 dual junction field-effect transistor (JFET), followed by a conventional integrated-circuit op-amp (LF 356). The JFETs give low voltage noise and input capacitance (~ 2 nV/$\sqrt{\text{Hz}}$ and ~ 10 pF at 10 kHz) and have gate leakage currents below 1 pA. These characteristics are important for attaining input current spectral densities of approximately 10^{-30} and 10^{-29} A^2/Hz at 1 kHz and 10 kHz, respectively.

The input transistors, the current-injection capacitors, and the two high-value feedback resistors and their switching elements are enclosed in a hybrid integrated circuit. A package with borosilicate-glass feed-throughs for the leads was selected for this circuit because standard feed-throughs were found to intro-

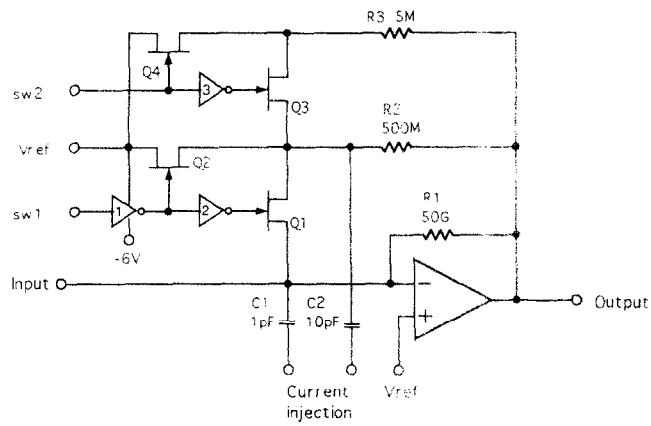

Fig. 2. Range switching in the headstage. Transistors Q1–Q4 (2N4118) switch the lower-value feedback resistors R2 and R3 to either the input or to V_{ref}. CMOS inverters 1 and 2 are powered from V_{ref} and a -6 V supply that tracks V_{ref}. All components shown here, with the exception of inverter 3, Q3, Q4, R3 and the output stage of the operational amplifier, are contained in a hybrid integrated circuit. The stray capacitance across R1 is approximately 20 fF. In the intermediate gain range, with sw1 high and sw2 low, resistor R2 is placed in parallel with R1 and the total capacitance across the resistors is about 160 fF. The operational amplifier circuit is essentially the same as in Fig. 1–11 of Sigworth (1994), employing a U430 dual JFET as the input device, except that 2 bypass capacitors are added to remove the contribution to input voltage noise due to the input transistor (Q2B in that figure) that is connected to V_{ref}.

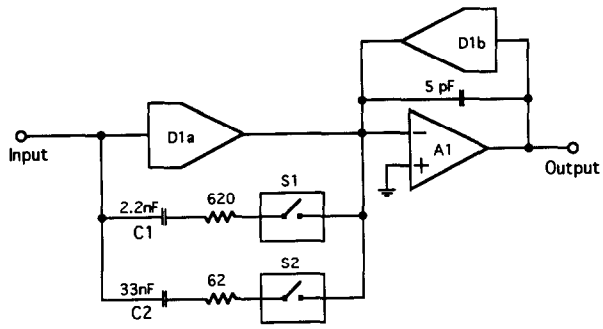

Fig. 3. Main frequency compensation (high-frequency boost) stage. A dual 12-bit mDAC (AD7549, Analog Devices) is used to set both gain and the time constant of a zero in the frequency response. The full-scale transconductance of the mDACs is nominally 100 μS. Analog switches S1a and S1b select ranges for compensating the 500 MΩ and 50 GΩ headstage resistors, respectively. The nominal DC gain of this stage is 1.3; the nominal time constant for the 50 GΩ resistor is 1 ms and for the 500 MΩ resistor, 80 μs. To obtain these gain and time constant values, D1a is typically set near 1360 (out of a maximum of 4095 counts) yielding an effective resistance of ~30 kΩ; D1b is typically set near 1024 counts. The operational amplifier is type OP-37 (Precision Monolithics).

duce substantial current noise, probably due to dielectric loss in the sealing glass. Also included in the hybrid is a CMOS quad-inverter chip, which drives the JFET switching transistors. The inverters, with their low-resistance outputs, provide a simple way to switch the JFET gate voltages between two values while introducing very little voltage noise. Such noise would otherwise be coupled through the gate capacitance into the head stage input. The positive power lead of the inverters is connected to the reference voltage V_{ref}; a -6 V negative supply for the inverters tracks V_{ref} to avoid the injection of current through the non-linear capacitance of the JFET gates when V_{ref} changes.

4. Frequency compensation stage

In parallel with the 50 GΩ head-stage resistor is a stray capacitance of about 0.02 pF, resulting in a low-pass filtering of the current-monitor signal with a time constant of about 1 ms. The main correction for this filtering is the frequency compensation stage shown in Fig. 3. It forms the sum of the input signal and its derivative, and since both the resistance of the 50 GΩ resistor and its stray capacitance can vary considerably, the gains are made variable with a dual 12-bit mDAC chip. One of the mDACs, D1a, acts as a variable conductance to set the strength of the 'direct' input, relative to the derivative input provided through the differentiating capacitor C1 (for compensating the 0.5 GΩ resistor) or C2. D1b sets the overall gain by acting as the feedback element. The 40 MHz gain-bandwidth product of the OP37 amplifier yields a typical bandwidth of 60 kHz for the differentiator function when C2 is switched in, or 120 kHz when C1 is switched in. The resistors in series with C1 and C2 provide zeros to stabilize the feedback around the amplifier.

5. Filter 2

A digitally controlled, 4-pole filter is provided for the current-monitor output. It was constructed of 2 cascaded low-pass state-variable sections, one of which is shown in Fig. 4. Two difficulties arise in simply using mDACs as variable conductance elements in such filters. First, the wide tolerance in the absolute resistance value of each mDAC means that the time constant of each integrator stage can vary. We used dual mDACs, which by their intrinsic matching preserve the Q value of each section of the filter; for the natural frequency a scale factor is calculated in the calibration program and is used for the conversion of frequency settings to mDAC settings in each section.

The second problem is the magnification of amplifier offset voltage that occurs when an mDAC serving as an input summing resistor is commanded to a low transconductance value. This problem arises because the internal R-2R ladder network of an mDAC has an output resistance that remains near 10 kΩ even when a low transconductance value is commanded from the

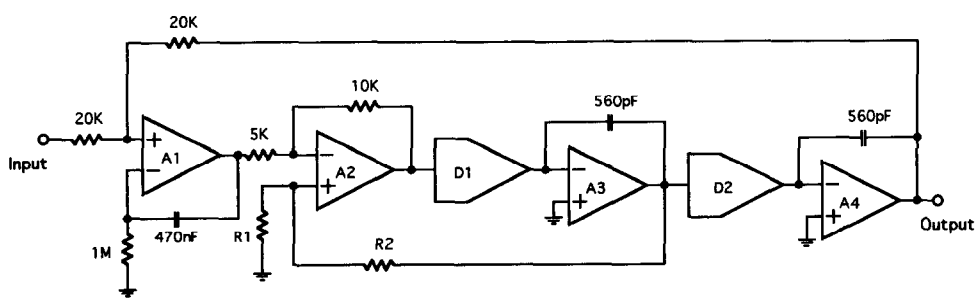

Fig. 4. One of the 2 cascaded 2-pole sections of Filter 2. A quad op-amp (LF347) and dual 8-bit mDAC (AD7528, Analog Devices) are used to implement an inverting, state-variable low-pass filter. A3 and A4 are the integrators, while A2 sums the quadrature signal to provide damping according to the values of R1 and R2. A1 serves as the auto-nulling integrator, which acts to force the sum of the input and the (inverting) output to zero with a time constant of 470 ms.

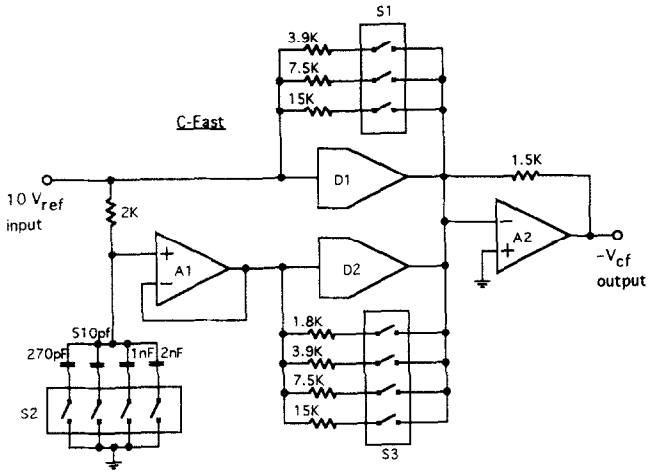

Fig. 5. Circuit of the C-Fast scaling amplifier with its 2 extended mDACs. The 8-bit mDAC D1 and associated resistors scale the unfiltered input signal, while D2 and its resistors scale the signal after filtering with a variable time constant up to 7.5 μs. The output signal from this stage is inverted and applied to the 1 pF current injection capacitor in the headstage.

digital input. For an 8-bit mDAC having only its least-significant bit turned on, the transconductance corresponds to 2.56 MΩ and the offset voltage, referred to the mDAC input, is some 256 times the offset voltage of the operational amplifier. Because the offset voltage of the filter needed to be below 1 mV, we enclosed each section of the filter inside an auto-nulling loop. In Fig. 4, amplifier A1 serves the auto-nulling function by forcing the sum of the input signal and the inverted output signal to integrate to zero, with a time constant of about 500 ms. Errors in the auto-nulling loop occur when the state-variable section is set to a low natural frequency, so that a substantial lag occurs between the input and output; the 500 ms time constant was chosen to keep the maximum transient offset error below 2 mV when a 1 V step is applied to the filter input at its 500 Hz setting. Errors in the auto-nulling can also occur when amplifiers in the filter go into saturation, making it impossible for the output to track the input voltage. To avoid this possibility, the filter sections run at a gain of 0.75 so that the amplifiers cannot be driven into saturation.

6. C-Fast scaling: use of extended mDACs

To keep the input current within the measuring range, the headstage has capacitors through which currents can be injected to cancel capacitive currents due to the charging of the pipette, patch membrane, and stray capacitances (together called 'C-Fast') and the currents due to the slower charging of cell membrane capacitance in the whole-cell configuration ('C-Slow'). For the C-Fast transient cancellation the stimulus voltage is scaled, filtered with a variable time constant of a few microseconds and applied through a 1 pF capacitor to the headstage input. The circuitry that perfoms this scaling and filtering function is shown in Fig. 5. The scaling amplifier's output voltage noise must be low ($\lesssim 10$ nV/$\sqrt{\text{Hz}}$) if it is not to add substantially to the input current noise of the headstage. A scaling amplifier using an mDAC will not have sufficiently low noise since the voltage noise in its 10 kΩ resistance alone is 13 nV/$\sqrt{\text{Hz}}$. To provide a lower impedance level along with variable gain up to unity we connected low-value resistors in parallel with each mDAC through switch elements. The resistors effectively extend the range of the mDACs by adding additional more-significant bits.

Because the resistors in the extended mDAC are not trimmed, the relationship between digital codes and the scaling of the amplifier stage is not linear. A linear relationship between digital values and gain of the amplifier is obtained through a software routine. During calibration the gain increment is measured from the full-scale mDAC and from the resistors as each combination is switched in. This information is

```
AddLinType = RECORD
     (* Calibration information *)
    MaxL         :  INTEGER;   (* Maximum step number *)
    Code         :  ARRAY[0..15] OF BITSET; (* Conversion from step
                                               number to switch code *)
    MaxD         :  REAL;       (* Full range DAC value, i.e. 255. or 4095. *)
    Threshold    :  REAL;       (* Thresh. value for trying to step down *)
    Add          :  ARRAY[0..15] OF REAL;   (* Effective DAC value
                                    corresponding to the ith switch level *)
      (* State information *)
    L            :  INTEGER;   (* Previous step number, kept for hysteriesis *)
    DacVal       :  INTEGER;   (* New computed DAC value *)
    SwVal        :  BITSET;     (* New computed switch setting *)
  END;
```

Fig. 6. Definition of a linearization record, the data structure which stores calibration and state information for an extended mDAC. During calibration the number of unique switch settings is assigned to MaxL, and the bit patterns corresponding to monotonically increasing conductance values are loaded into the Code array. The corresponding conductance values are placed into the Add array.

stored in a look-up table within a data structure, the 'linearization record' (Fig. 6). During operation this record is accessed by a procedure that computes appropriate mDAC and switch settings for the desired gain setting. Besides containing information for computing a new setting for the switches and mDAC, the record contains information about the previous setting, allowing hysteriesis to be implemented in order to avoid unnecessary switching of resistors.

7. C-Slow transient cancellation and series resistance compensation

In whole-cell recording the cell membrane current flows through a series resistance R_s that arises from the resistance of the patch pipette and the access resistance through the broken patch membrane to the cell interior. The series resistance gives rise to a slow time course of changes in membrane potential, and also introduces errors in the control of membrane potential when substantial ionic currents flow. In the EPC-9 the compensation for this series resistance performed by 2 pathways, as described by Sigworth (1994). First, a variable-gain R_s-compensation amplifier scales the current monitor signal, and its output is summed with the command signal V'_{cmd} to yield the input reference voltage V_{ref} (see the amplifiers 'RS Comp' and 'Sum2' in Fig. 1). This pathway provides the classical series resistance compensation (Hodgkin et al., 1952) that effectively synthesizes a negative resistance $-\alpha R_s$ at the amplifier input, compensating α fraction a of the series resistance.

The second pathway of series-resistance compensation involves the circuitry that cancels the transient charging current due to the cell membrane capacitance C_m. Assuming negligible membrane conductance, this 'slow capacitive' charging current I_{sc} is, in terms of the Laplace transform variable s,

$$I_{sc}(s) = V'_{cmd}(s)\tau s/R_s(\tau s + 1)$$

where V'_{cmd} is the command voltage applied to the pipette and the time constant is $\tau = R_s C_m$. To remove the capacitive transient from the current monitor signal, a current equal to this can be supplied through a current injection capacitor C_i in the headstage. The voltage V_{sc} that would need to be imposed on the capacitor is given by

$$V_{sc}(s) = C_m V'_{cmd}(s)/C_i(\tau s + 1) \quad (1)$$

i.e., a filtered and scaled copy of V'_{cmd}. The C-Slow circuitry generates this voltage, with parameters corresponding to C_m and R_s being determined by mDACs. By injecting this current into the headstage input, the capacitive transients are removed from the current monitor signal, aiding the observation of ionic membrane currents. However, a problem arises because the effect of this transient cancellation is to interfere with proper series-resistance compensation. Because of the transient cancellation no signal corresponding to I_{sc} is applied to the R_s-compensation amplifier (see Figs. 1–17 of Sigworth, 1994) and added to the command voltage V_{ref}.

The necessary correction to the command voltage involves adding a signal equal to the voltage drop across the compensated series resistance due to the

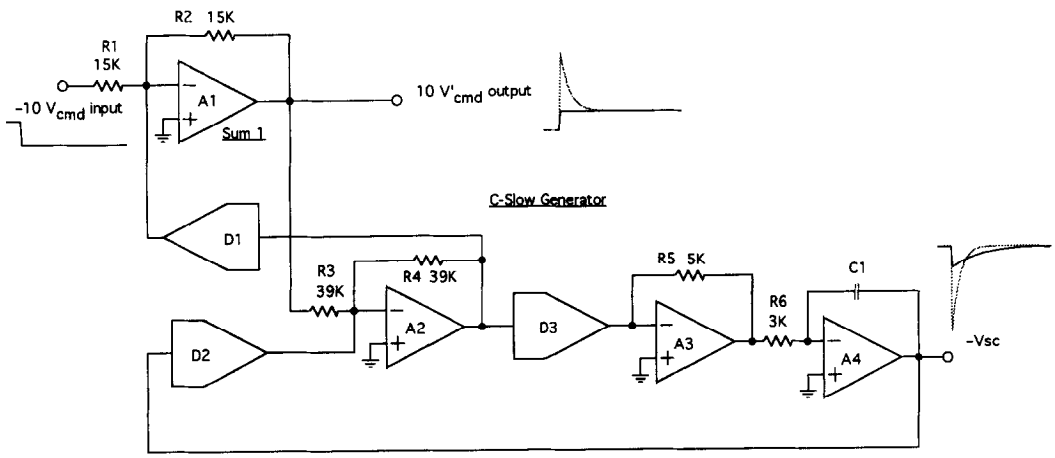

Fig. 7. C-Slow and R_s-prediction circuitry. A1 comprises the 'Sum 1' amplifier of Fig. 1. A2, A3 and A4 comprise a first-order state-variable filter with A4 being the integrator. D1 is an 8-bit mDAC (AD7528), while D2 and D3 are 12-bit mDACs (AD7549). D2 is extended by five additional analog switches and resistors to give a maximum conductance of 1.6 mS. R5 can be switched between values of 10 and 3 kΩ and C1 can take values of 3.3, 33 and 330 nF to give a wide range of time constants. Typical waveforms are shown at the V'_{cmd} and $-V_{sc}$ outputs. With D1 set to zero the responses to a step input are as shown by solid curves. The amplitude of the output V_{sc} (which is proportional to the capacitance C_m to be compensated) is determined by $1/G_2R_3$, where G_2 is the transconductance of D2. When D1 is set to a non-zero value, positive feedback through A1 and A2 results in an overshoot of the output voltage V'_{cmd} and a shorter time constant at the V_{sc}. The dotted curves show the responses to a step input with $G_1R_2 = 0.7$ (i.e., 70% series-resistance compensation).

injected current I_{sc}. As it turns out, the result of this correction is the introduction of overshooting transients into the command voltage V'_{cmd} which cause the membrane capacitance to be charged more quickly when step stimuli V_{cmd} are given. This correction has the same function as the 'supercharging' process described by Armstrong and Chow (1987). When a fraction α of the total series resistance is compensated, V'_{cmd} differs from V_{cmd} to include the voltage drop across the compensated resistance,

$$V'_{cmd} = V_{cmd} + \alpha R_s I_{sc} = V_{cmd} + [\alpha\tau s/(\tau s + 1)]V'_{cmd} \quad (2)$$

The generation of the voltages V_{sc} and V'_{cmd} is performed by the circuit shown in Fig. 7. The negative-feedback loop consisting of A2, A3 and A4 forms the 'C-Slow generator', creating an output voltage $-V_{sc}$ with a DC gain inversely proportional to the conductance of D2 and with a time constant determined by D2 and D3. A positive feedback loop that includes A2, D1 and the 'Sum 1' amplifier A1 produces the corrected command V'_{cmd} according to Eq. 2.

To understand the operation of the circuit, let us first consider the operation of the C-Slow generator alone. Letting G_2 and G_3 be the conductances of D2 and D3, V_{sc} is given by

$$V_{sc} = (10/G_2R_4)V'_{cmd}/[(R_6C_1/G_3R_5)s + 1], \quad (3)$$

which can be seen to be equivalent to Eq. 1 when

$$C_m = C_{max}/G_2R_4 \quad (4)$$

and

$$1/R_s \equiv G_s = (C_{max}/R_6C_1)G_3R_5 \quad (5)$$

where we have defined the nominal maximum C_m value

$$C_{max} = 10C_i.$$

Thus to inject a transient current that matches I_{sc}, in the circuit G_2 can be varied to match C_m, and G_3 can be varied to match G_s.

In order to allow transient subtraction as C_m and G_s values vary over a wide range, provisions are made for range-changing. Injection capacitors C_i of 1 and 10 pF are available, and the 1 pF driver amplifier can be set for a gain of either 0.3 or 1.0, yielding effective C_i values of 0.3, 1 and 10 pF. These correspond to the 3 C-Slow ranges with $C_{max} = 3$, 10 and 100 pF. Within each range, the C_m value is inversely proportional to the mDAC conductance G_2 which varies from zero to 1.6 mS, giving a range of $1/G_2R_4$ of about 0.016 to infinity. Thus in the 10 pF range C_m values from 0.16 pF to infinity are accessible. Although very large capacitance values can therefore be obtained in any range, there are two disadvantages in setting C_m values much larger than C_{max}. First, amplifier saturation can occur as the voltages V_{sc} exceed the amplifier output voltage limits (about ± 12 V). When C_m is equal to the range limit, V_{sc} has a magnitude of 10 V_{cmd}, and when 90% series resistance compensation is in use, V_{sc} can have peak values of 100 V_{cmd} (see Eq. 2). Thus if V_{cmd} excursions up to 200 mV are to be allowed, practical upper bounds for C_m are 6 C_{max} when no R_s compensation is used, or $6(1-\alpha)C_{max}$ when a fraction α of R_s compensation is used.

A more subtle issue concerns the resolution of the mDAC that sets C_m. D2 is an extended 12-bit mDAC with 5 external resistors and has an overall resolution of 16 bits. The value of G_2 thus has a resolution δG_2 of about 25 nS. The resolution of the C_m setting can be expressed as

$$\delta C_m/C_m = \delta G_2R_4C_m/C_{max} \sim 10^{-3}C_m/C_{max} \quad (6)$$

and is seen to become coarser as C_m/C_{max} increases. Thus for precise cancellation or determination of C_m, it is advantageous for the user to choose a range with high C_{max}.

Range changing is also provided for the G_s adjustment, in that the values of R5 and C1 can be changed by analog switches, yielding a 300:1 range of the scaling factor R_5/C_1 (see Fig. 7 legend). Low values of this factor reduce the noise applied to the headstage input via the injection capacitors; this noise is particularly important in cases where the intrinsic noise of the cell and pipette is low, i.e. when C_m and R_s are small. Like the look-up table used for the extended mDAC, a look-up table is maintained for the effects of the switches that control R5 and C1, and a software procedure performs automatic range-changing with these switches according to the G_s value being set by the user.

Finally, it can be seen that the circuit in Fig. 7 generates the corrected command signal V'_{cmd} according to

$$V'_{cmd} = V_{cmd} + [G_1R_2\tau s/(\tau s + 1)]V'_{cmd} \quad (7)$$

with

$$\tau = R_6C_1/G_1R_4G_2R_5$$

and G_1 being the transconductance of D1. Comparison of Eqs. 2 and 7 shows that the series-resistance correction α is determined by D1 according to

$$\alpha = G_1R_2.$$

8. Conclusion

The circuitry described here results in an instrument with the analog signal-processing capabilities of a conventional patch-clamp amplifier such as the EPC-7, but with computer control of all calibration and user ad-

justments. The circuitry contains almost twice as many operational amplifiers as the EPC-7. It should, however, be pointed out that whereas the EPC-7 has 33 trim potentiometers, the EPC-9 has none. Many of the additional amplifiers are used in conjunction with mDACs to make amplifiers with variable voltage gains; these fulfill the role of front-panel controls or of trim potentiometers in the earlier instrument.

Acknowledgements

The author is grateful to Drs. E. Neher and W. Stühmer for their support of this project, most of which was carried out in their laboratories at the Max Planck Institut für biophysikalische Chemie, Göttingen, Germany. The author also thanks F. Würriehausen and C. Koitz for their help with the design and debugging of the circuitry.

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