

The LHCb Silicon Tracker Project

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Two silicon strip detectors, the Trigger Tracker(TT) and the Inner Tracker(IT) will be constructed for the LHCb experiment. Transverse momentum information extracted from the TT will be used in the Level 1 trigger. The IT is part of the main tracking system behind the magnet. Both silicon detectors will be read out using a custom-developed chip by the ASIC lab in Heidelberg. The signal-over-noise behavior and performance of various geometrical designs of the silicon sensors, in conjunction with the Beetle read-out chip, have been extensively studied in test beam experiments. Results from those experiments are presented, and have been used in the final choice of sensor geometry.

1. Introduction

The LHCb experiment [1] aims at measuring CP-violation in the B-meson sector and rare decays. In $p\bar{p}$ collisions, B-meson pairs will emerge predominantly parallel to the incoming proton beams. Therefore, a single-arm forward spectrometer has been designed. Tracking information will be supplied by a vertex detector, the Trigger Tracker, an outer tracker and the corresponding Inner Tracker. Particle identification is given by ring imaging Čerenkov detectors in front of, and behind the 4 Tm dipole magnet, a hadronic and an electromagnetic calorimeter. Muon tracking chambers are used for the muon trigger, and track reconstruction.

2. Silicon Tracker Project

The Silicon Tracker project comprises the design and construction of two silicon strip detectors. The Trigger Tracker will be placed in the fringe field, in front of the dipole magnet to determine the transverse momentum of charged particles. In the off-line tracking, the TT will be employed to reconstruct particles, *e.g.* K_s^0 , which decay outside the vertex detector.

The Inner Tracker will be used to cover that part of the acceptance around the beam pipe behind the magnet where the particle flux density is around $10^5 \text{ cm}^{-2}\text{s}^{-1}$. The granularity of the IT is chosen such that an occupancy of less $\sim 2\%$ is expected, thus leading to efficient track reconstruction.

The design of the silicon sensors is a compromise between tracking efficiency on one hand, and maintaining a low material budget and a limited financial budget on the other hand. From the point of view of multiple scattering and track res-

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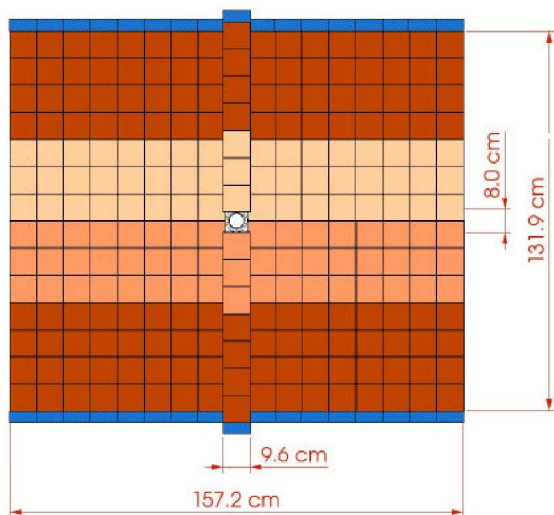


Figure 1. A sketch of the layout of a 0° plane for the second TT station. Here, respectively four and three sensors are combined in one read-out unit.

olution, one would minimize the thickness of the sensors, but from the point of view of signal-over-noise performance, *i.e.* detection efficiency, one would like to employ 'thicker' silicon sensors.

2.1. Trigger Tracker

The information provided by the Trigger Tracker will be used in the L1 trigger to reject background events. The detector will consist of two stations of two planes each in a 0° and a 5° stereo-angle configuration. The TT will cover the complete acceptance of 300 mrad in the vertical plane, and 250 mrad in the horizontal plane. As a consequence, multiple sensors will be joined in a single detector element. At the position ($z = 232$ cm and $z = 262$ cm, respectively) where the TT stations will be located, this constitutes an area of $\sim 1.44 \times 1.17$ m² for the first station, and $\sim 1.60 \times 1.32$ m² for the second station. A sketch of the layout of the 0° planes is shown in Figure 1.

Fourteen sensors will be mounted on two paral-

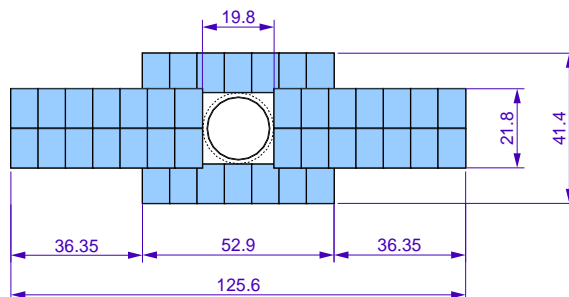


Figure 2. A sketch of the layout of a 0° plane for the Inner Tracker. The measures are in centimeters. Each of the three station will cover a similar acceptance.

lel rails, forming a single ladder. One ladder will consist of 2×2 read-out units, of four- and three sensors respectively. The three-sensor unit will be bonded to a $100 \mu\text{m}$ thick Kapton cable, in order to connect the inner units to the front-end read-out hybrids located outside the acceptance, at the bottom and on top of the TT planes.

The two planes of each station are mounted in an air-tight box. The frames of the box will be cooled by liquid C_6F_{14} , such that the ambient temperature remains at 5° Celsius. This way, the silicon sensors are expected to maintain their required performance for the duration of the experiment. The box will be flushed with dry nitrogen to prevent condensation on the cold surfaces.

2.2. Inner Tracker

A cross-shaped silicon strip detector, depicted in Fig. 2, has been designed and will be installed behind the magnet at the position of the corresponding Outer Tracker detector. Three stations of four planes each, two 0° -planes and two stereo-angle planes, at $\pm 5^\circ$, have been designed. Here, single- and two-sensor ladders are used.

Although the IT covers only a small fraction (1.5%) of the acceptance, more than 20% of the particles will traverse this part of the spectrometer. By using sensors with a $\sim 200 \mu\text{m}$ pitch,

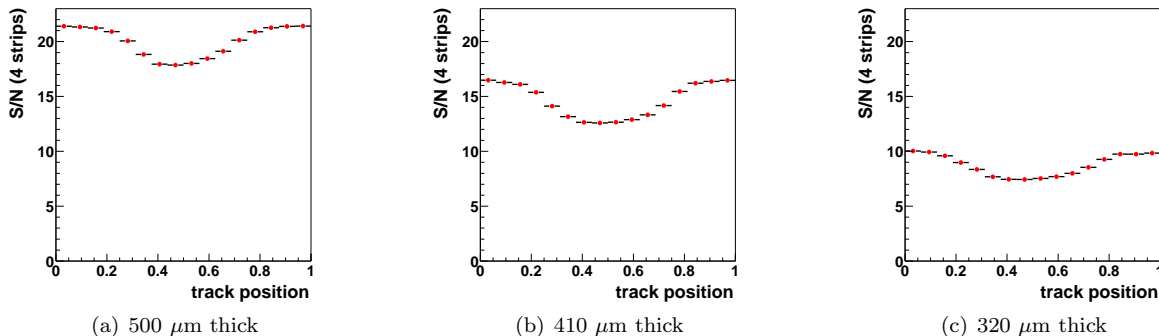


Figure 3. Signal-over-noise performance for the three sensors. The signal is shown as a function of the fractional position between two read-out strips.

a planar resolution of better than $60 \mu\text{m}$ is expected. Correspondingly, this will result in a momentum resolution of $\delta p/p \approx 0.4\%$. In case of an exclusive reconstruction of the $B_s \rightarrow D_s K$ decay channel, the contribution of the tracking resolution to the B_s mass resolution is about equal to the contribution from the angular resolution at the B_s vertex.

Each IT station consists of four boxes, arranged around the beam pipe. The diameter of the hole in the center of the respective IT stations follows the 10 mrad conical shape of the beam pipe. The front-end chip will be located in the acceptance of the spectrometer, consequently the amount of dead material needed for cooling has to be minimized.

2.3. Front-end

The front-end chip, called Beetle [2], has been designed at the ASIC laboratory in Heidelberg. This is a chip-design laboratory founded by the Max Planck Institute for Nuclear Physics and the Ruprecht-Karls-Universität.

The 128-channel read-out chip, which employs a 40 MHz sampling rate, has been developed for the LHCb experiment. It will be used in the in the TT, IT, the LHCb vertex detector and for the pile-up veto. The Beetle chip was designed using $0.25 \mu\text{m}$ CMOS technology, and has been extensively tested. In an irradiation test, the chip

has been proven to be fully operational, even after a dose of 45 Mrad. With a fast rise time of 14 ns, the signals can be uniquely associated to their respective bunch crossings.

3. Test Beam Results

In order to arrive at a judicious choice of sensor geometry and thickness, various geometrical configurations of strip design, number of sensors per ladder and sensor thicknesses have been investigated. These tests have been performed at

Table 1

Sensor properties used in the test beam. All ladders listed consisted of three sensors.

Ladder nr.	strip length (cm)	implant width (μm)	pitch (mm)	thickness (mm)
1	32.4	60	198	320
2	26.3	56	228	410
3	28.9	46	183	500

the X7 test beam facility at CERN, using versions 1.1 and 1.2 of the Beetle front-end chip. An extensive description of these tests and their results is given in Refs. [3,4].

In Table 1, a list is given of the various sensor

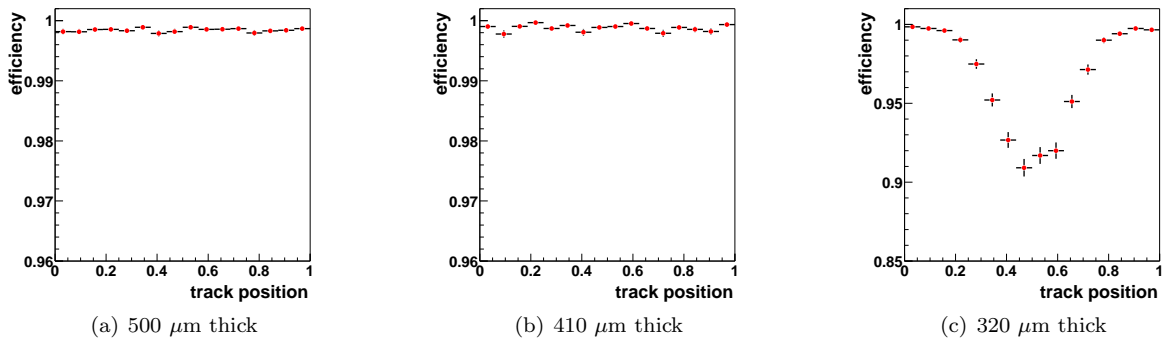


Figure 4. Efficiency performance plots for the three sensors. The signal threshold was chosen such that the noise rate was less than 6×10^{-4} .

thicknesses and designs of strip geometry. These ladders have been operated in a 120 GeV π^- beam. Triggering was provided by four scintillators positioned in front of and behind the ladders. The tracks were reconstructed using a beam telescope, consisting of four double-sided silicon strip sensors [5], provided by the HERA-B vertex group. With a track resolution of $\sim 14 \mu\text{m}$ at the position of the ladders, a precise study could be made of the performance of the various ladders.

In particular, the inter-strip dependence of the signal-over-noise ratio (S/N) has been extensively studied. With pitches as large as 228 μm and sensors as thin as 320 μm , it was unclear whether the resulting efficiency would be homogeneous across the inter-strip region.

In Figure 3, the results of such a study for the three cases mentioned in Table 1 are shown. A substantial drop in S/N can be observed, independent of the substrate thickness. It can be concluded that the 320 μm thick sensors exhibit a limited signal-over-noise performance. When these data are used to calculate tracking efficiencies, a drop of up to 9% is observed for the 320 μm sensors, as can be seen in Figure 4. For values of $S/N < 9$, the threshold selection criterion imposed on the data leads to a drop in efficiency, see Fig. 4(c). In addition, it can be observed that at higher values of signal-over-noise, the effect of the S/N drop in between two strips on the tracking

efficiency is negligible. The process of charge collection within the sensors has been simulated [6]. The observed charge loss could be reproduced, and is caused by charges trapped at the surface of the silicon ladders in the low field region between the strips.

4. Conclusions

Two silicon strip detectors have been designed for LHCb. The Beetle front-end, designed for operation in the harsh environment imposed by LHC will be used in the read-out electronics. The Beetle chip and various designs of the sensors and ladders have been tested. From these tests it was concluded that for the TT, sensors of at least 500 μm thickness are needed, while for the IT 320 μm thick sensors for the single-sensor ladders are sufficient, and 410 μm thick sensors will be used for the two-sensor ladders.

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