Factors Affecting EMCCD Technology for Use in Space

Thesis

Factors affecting EMCCD technology for use in space

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by

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Abstract

This thesis is an assessment of factors of the EMCCD that may prevent this technology from being used in the space environment. The factors of interest here are EMCCD ageing, radiation effects from gamma rays and protons, and finally, single event susceptibility to heavy ions.

The theory and architecture of the CCD and EMCCD are described with the aim of providing a technical basis in which to explore the results. The practical methods and novel experimental techniques carried out in this thesis are also described. However, EMCCD ageing is the primarily focus of this work concentrating on characterisation, understanding and then an experimental investigation into uncovering the cause of the phenomenon. Many EMCCDs (CCD97s) were tested with a cause of ageing being attributed to hot hole trapping in the oxide layer.

Radiation effects regarding the effects that gamma-rays and protons have on EMCCDs, specifically the ageing, is also investigated. This analysis has shown that gamma-ray radiation in particular, has a large effect on the ageing and gain of these devices. In addition to this work is an experimental campaign to investigate the susceptibility to heavy ions primarily focussing on Single event Gate Rupture; showing EMCCDs to be a resilient against this type of error.

Declaration

I hereby declare that no part of this thesis has been previously submitted to this or any other university as part of the requirement for a higher degree. The work described herein was conducted solely by the undersigned except for those colleagues and other workers acknowledged in the text.

Anthony Minas Evagora

25th October 2012

Dedication

To my parents, my brother, and my love.

Acknowledgements

I would like to acknowledge the following people as without them, the work detailed in this thesis could not have been accomplished.

I would like to thank my supervisors Andrew Holland and Neil Murray for their continued support and guidance.

Thanks to all members of the *centre for electronic imaging*, including; Andrew Clarke, Ben Dryer, Calum MacCormick, Dan Weatherill, David Hall, Edgar Allanwood, James Tutt, Jason Gow, Konstantin Stefanov, Matthew Soman, Philippa Smith, Richard Harriss, Ross Burgon, Simeon Barber and Tom Greig.

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Special thanks to David Burt whose knowledge and assistance over the last three years has been invaluable. Thank you.

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Contents

Chapter 1: Introduction

1.1 Electron Multiplying CCDs

The Electron Multiplying Charge Coupled Device (EMCCD) is an image sensor that utilises high electric fields in order to increase both the signal size and signal to noise ratio via the process of impact ionisation (Mackay(a) 2001). Such a process incorporated directly into a traditional Charge Coupled Device (CCD) image sensor has allowed for a more sensitive device. The high fields have however caused some difficulties. The gain achieved via the multiplication process tends to decay during operation and has been given the term 'ageing' (Evagora(a) 2012). In addition to this the high fields have created a possible vulnerability to radiation and single high energy particles which have not been a concern for traditional CCDs (Evagora(b) 2012).

1.2 Research goals

The general theme of this research is to establish the practicality of utilising the EMCCD for space applications. The Technology Readiness Level (TRL) assigned to a technology is a scale used to measure the maturity of technology when considering them for space use (ESA(a) 2012). An aim of this work is to increase this level in EMCCD technology, through research into three main topics: EMCCD ageing, proton/gamma irradiation and damage from heavy ions.

Firstly, EMCCD ageing has been a concern for a number of years. Although vitally important for the future of this technology, only a small amount of work has been done (Ingley 2009) (e2V-Technologies 2006). In order for these devices to be considered a viable and stable technology for space, the understanding of this effect and hence the TRL has to improve.

Secondly, proton irradiation of EMCCDs is well documented (Smith(b) 2006). However, little work has been done on the possible effects that proton irradiation has on the ageing effect of the devices. Similarly, work on the effect of gamma radiation directly on the ageing is currently not available. If a complete solution to the ageing is not found, then fully defining the ageing effect and identifying what to expect and when; is the next best thing to reduce the risk to space instrumentation. Additionally, identifying the cause of the possible effects these radiations have, may inadvertently lead to information on the ageing itself.

The third and final part of this research was to study how susceptible the EMCCD is to single event phenomena, in particular heavy ions. The gain mechanism as described before utilises relatively high fields and may therefore create a vulnerability to heavy ions. This vulnerability needs to be fully explored to allow the device to move forward where space flight is concerned. This study aims to give a definitive answer to whether or not EMCCD is a safe, reliable technology in a heavy ion environment, as may be found in space (Evagora(b) 2012).

All these studies have been of particular interest to our industrial partner, e2v Technologies, as results from this work allows them to move forward and promote their EMCCD programme for space applications. This is a good example of where industry and academia can collaborate for mutual benefit.

1.3 Thesis organisation

This work is laid out in 9 chapters. Chapters 2 and 3, respectively, introduce the CCD and the EMCCD. They provide an outline of device architecture, operation and enhancements. Chapter 4 outlines the practical methods used for this research, including mechanical, electronic, thermal and vacuum processes. Chapter 5 outlines the ageing phenomenon

and summarises the initial characterisation results of the EMCCD ageing investigation; showing the effect in detail alongside some of its dependencies. The second part of the EMCCD investigation is described in Chapter 6 where a novel experiment designed to probe deeper into the cause of the ageing phenomenon is described and the results analysed. Chapter 7 explains the effects of a proton/gamma irradiation on EMCCD ageing. Chapter 8 outlines the important work on Single Event Gate Rupture and outlines an experimental campaign to a heavy ion facility; this chapter describes an entire piece of work from hypothesis through simulation to the final results. The final chapter concludes the work in this thesis and possible progression to any future work.

1.4 Publications

First author peer reviewed publications:

1) Evagora, A.M, Murray, N.J, Holland, A.D, Burt, D, Endicott, J. "Novel method for identifying the cause of inherent ageing in Electron Multiplying Charge Coupled Devices." *Journal of Instrumentation, 7* , no 1 (2012)

2) Evagora, A.M , Murray, N.J, Holland, A.D, Burt, D "Single Event Gate Rupture in Electron Multiplying CCD technology." *Journal of Instrumentation*, (2012)

Contributing author peer reviewed publications:

1. Tutt, J.H, Holland, A.D, Murray, N.J, Hall, D.J, Harriss, R.D, Clarke, A, Evagora, A.M "The Noise Performance of Electron Multiplying Charge-Coupled Devices at soft X-ray energies" *IEEE Transactions on Electrons Devices*, 59 , no 8 (2012)

Chapter 2: CCD image sensor

An image sensor is a device which converts spatially distributed incident radiation into electrical signal. It resolves both the position and intensity of signal which may arise from photons or ionising particles.

The CCD is a semiconductor device that has long been used for the storing and transfer of charge. (Wood 1965) (Lutz 1999) The CCD stores charge in potential wells below the surface of the semiconductor and transfers it to neighbouring wells by the switching of potentials. Their high transfer efficiency has allowed the CCD to be used as an image sensor (Boyle and Smith 1971). For the remainder of this thesis the Charge Coupled Device image sensor will be referred to, as simply the CCD.

The CCD is currently the dominant technology for high performance/scientific imaging applications with stable high fill factors, small pixels and large formats (Mendis 1997). To function, the CCD sensor goes through various stages of operation which are; charge generation, collection, transfer and finally charge to voltage conversion.

2.1 The CCD

The modern CCD is a silicon integrated circuit of the Metal-Oxide-Semiconductor (MOS) transistor type. Unlike more conventional circuits which use a voltage or current amplitude, signal information is represented by a quantity of electric charge. With an image incident on the device, charge is photo-generated and stored within potential wells under an electrode structure. Then, with appropriate pulsing of the applied voltages to the electrodes, the charge signals are transferred to an output circuit for conversion to a more conventional output quantity for example a voltage or ADC digital number.

2.1.1 Basic device structure

Figure 2-1 shows a small section of a typical device. The CCD consists of an array of closely spaced electrodes or gates which have a typical applied bias of either 0V or +12V with respect to the substrate (SS). These electrodes are over an insulating layer of about 0.1 μm thickness, which is in-turn formed on p-type silicon substrate material typically 600 μm thick (Burt(a) 2012). The substrate has a connection which is typically at 0V.

Holes are attracted to SS and are not collected; signal charges are in the form of a quantity of stored electrons and are held beneath the electrodes with the applied biases. Alternatively, the charge can be located within an n-type buried channel of depth typically 1 μm below the insulator. The charge generation mechanism and the reason for the buried channel being present are described later.

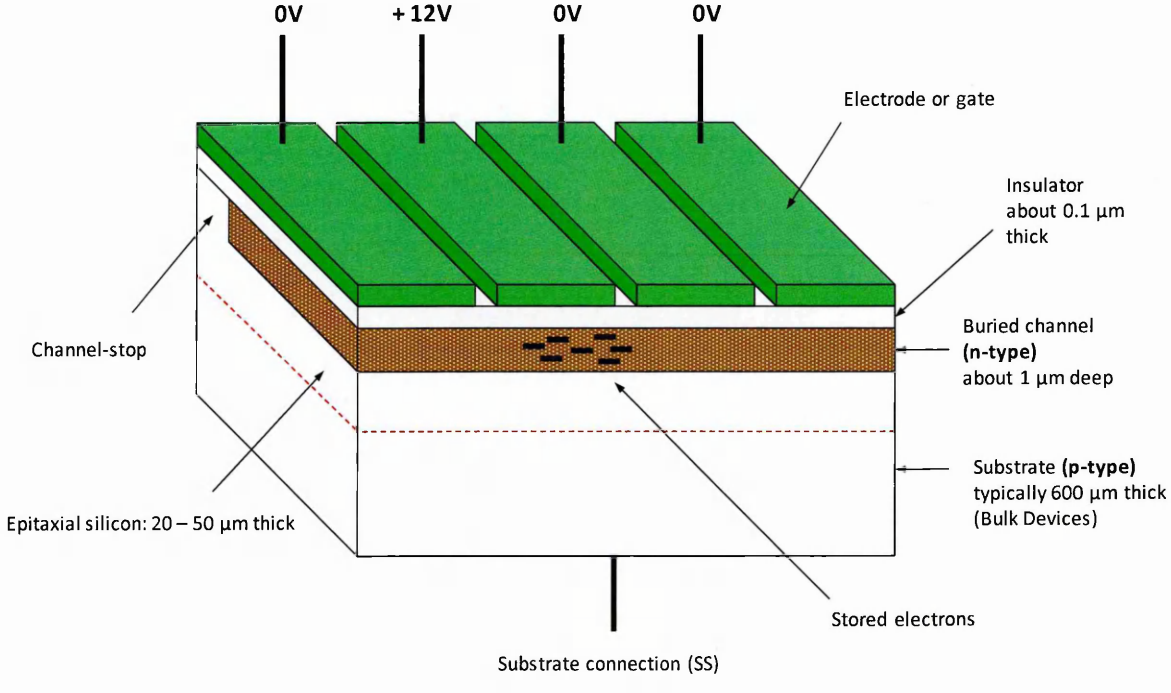


Figure 2-1. Typical CCD segment showing basic features (Burt(a) 2012).

2.1.2 Potential well model

Figure 2-2 (left) shows a cross section schematic of the device with the charge stored within the buried channel. Right of the diagram shows the potential distribution through the buried channel as a result of the electrode bias. The storage of charge is viewed as analogous to the storage of water in a well and with the positive voltages plotted downwards; the storage location is described as a potential well of a depth equal to the difference in electrode voltages.

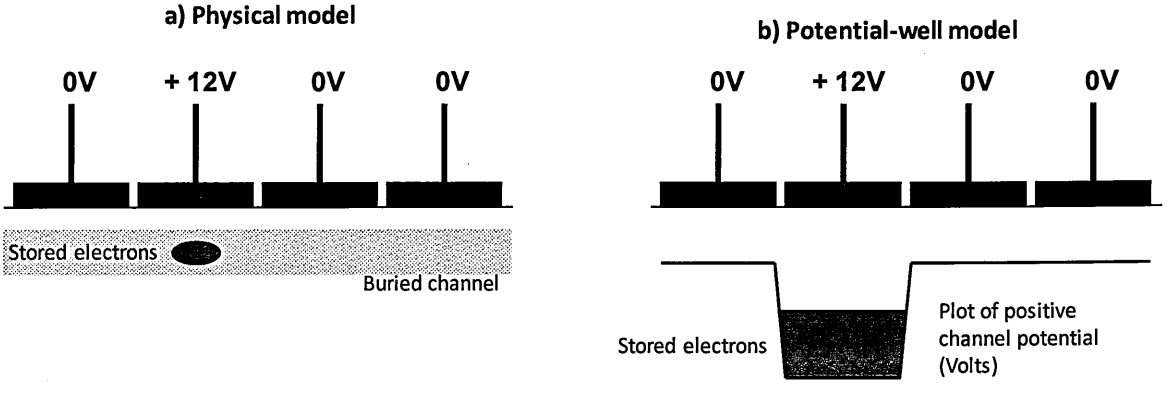


Figure 2-2. Physical model, a), alongside the potential-well model, b) of the internal processes of the CCD.

The essential nature of the CCD is the transference of charge from one electrode to the next, known as charge coupling.

2.2 Charge transfer

2.2.1 Drive waveforms

Figure 2-3 shows the arrangement for connecting an array of electrodes to the voltages used for charge transfer. What is shown is described as a 3-phase sequence described in further detail in a later section. There are three input connections shown as circles and designated Phase 1 ($\Phi 1$), $\Phi 2$ and $\Phi 3$. These connect to bus lines to which the electrodes connect in sequence. The applied voltages are in the form of timed pulses of amplitude

typically +12V. Progressing through the time sequence is as follows. Step 1, Φ2 is at 12V and the other phases at 0V. There are potential wells under every Φ2 electrode allowing them to store charge, as presented in the cross-section of Figure 2-3. At step 2 both Φ2 and Φ3 are now at 12V, as shown by the dotted line, and the signal charge is now stored under the combined Φ2 + Φ3 potential well. At step 3 the Φ2 phase has gone to 0V and the charges are now stored in the potential wells under the Φ3 electrodes. The sequence continues and the charges move together down the array of electrodes. The rate of movement simply depends on the timing of the drive pulses. For this reason the transfer operation of the device is often termed clocking and the pulses are called clock pulses.

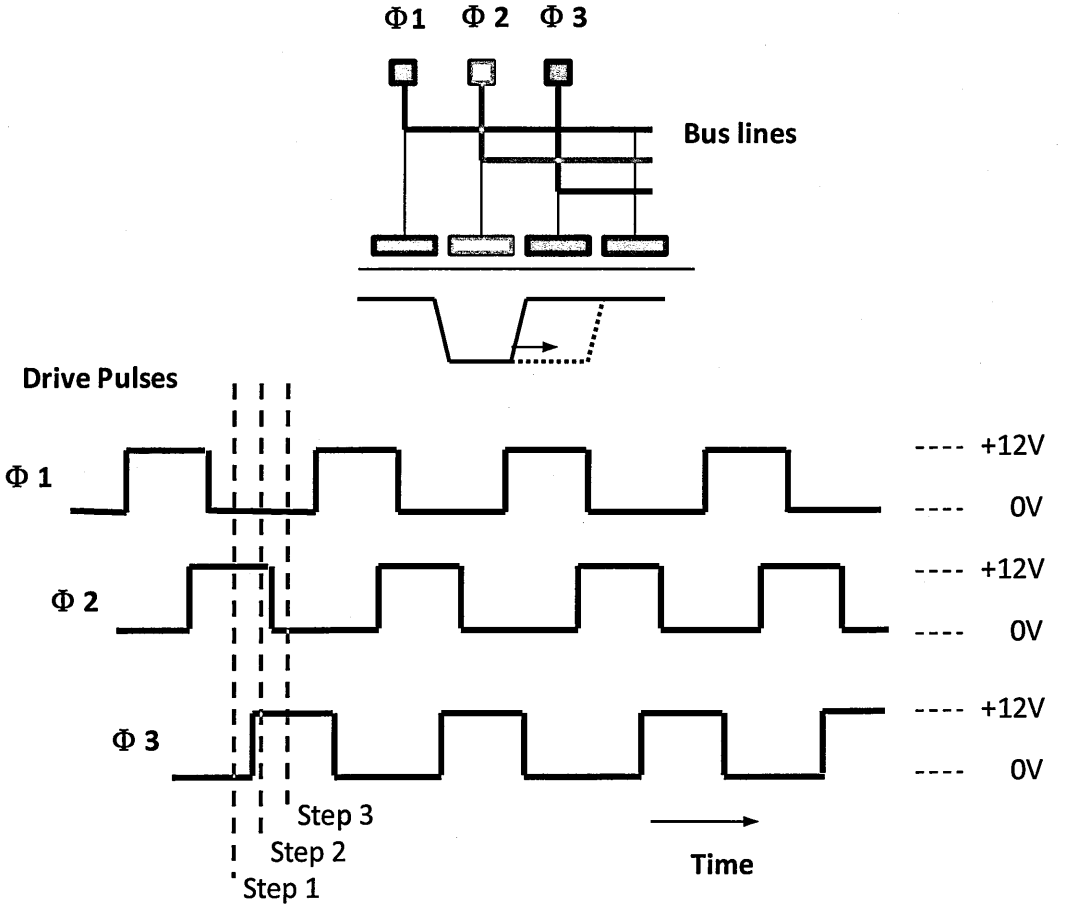


Figure 2-3. Drive waveforms for a 3-phase device.

The three electrodes that collect, store and transfer a single charge packet are described as one row element of the imaging array. Horizontal isolation is provided by channel stops and the combination of the two creates a picture element which is referred to as a pixel.

2.2.2 Polysilicon electrodes

Polysilicon electrodes are fabricated using thin films of silicon typically 0.5 µm thick. These layers are formed by a high temperature deposition process where a Silane (SiH_4) gas is used to form the silicon layer. The silicon is formed on the grown oxide and therefore does not form a perfect crystalline connection, instead disjointed separate silicon crystalline sections are formed hence the names polycrystalline and polysilicon. For a three-phase device three layers are typically used with inter-level insulation formed by the oxidisation, as shown in Figure 2-4.

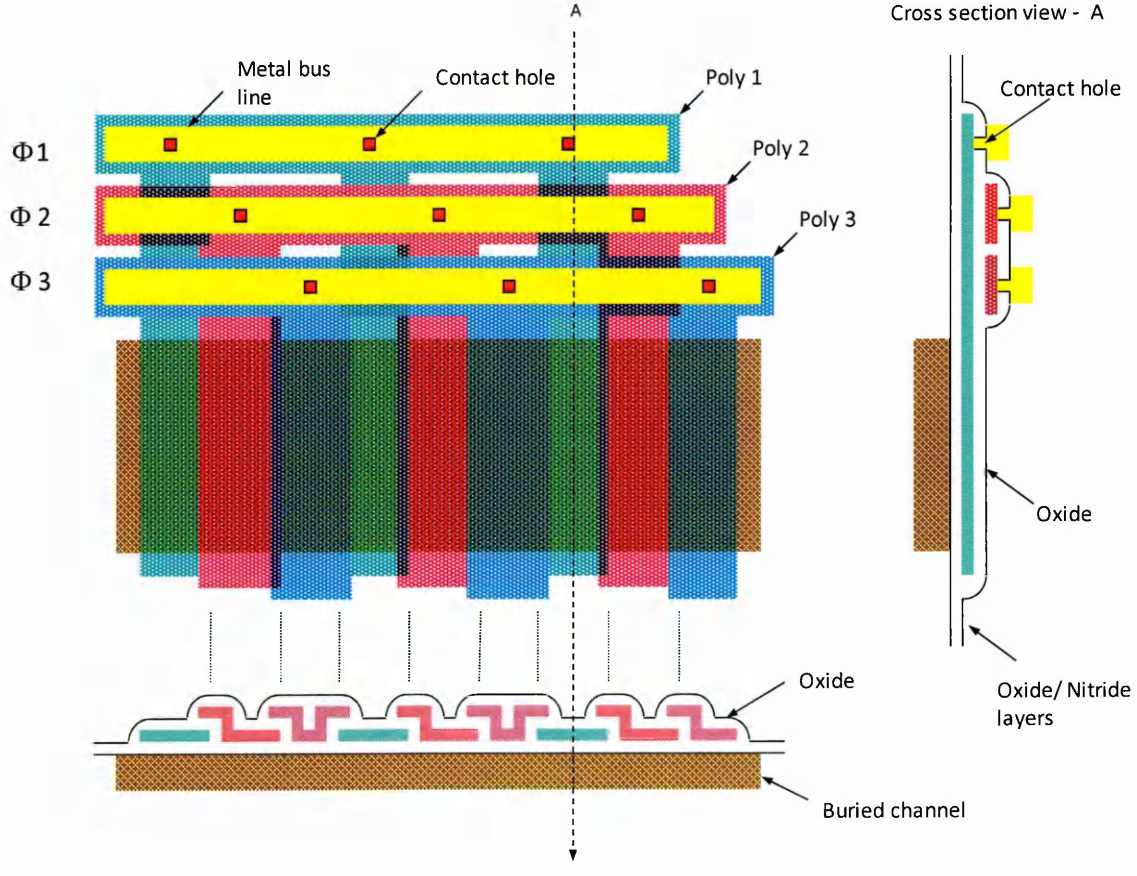


Figure 2-4. Polysilicon electrodes (Burt(a) 2012).

Advantages of this approach compared to metal electrodes are; 1) efficient transfer as the inter-electrode potentials are well-controlled, 2) good photo-response due to the semi-transparent nature of the material and 3) easy to electrically isolate.

2.2.3 The CCD channel

There are two types of charge transfer channels, surface and buried.

2.2.3.1 Surface Channel CCD

The earliest devices operated in the surface channel mode, where the device utilised either an n-type or a p-type substrate and the signal charge was stored at the Si/SiO_2 interface. The situation is illustrated in Figure 2-5 which shows the potential distribution through the structure for the case of a p-type substrate. This led to poor Charge Transfer Efficiency (CTE), which is the fractional loss of charge in each element transfer, as charge can come in contact with traps at the interface (Sze 1981).

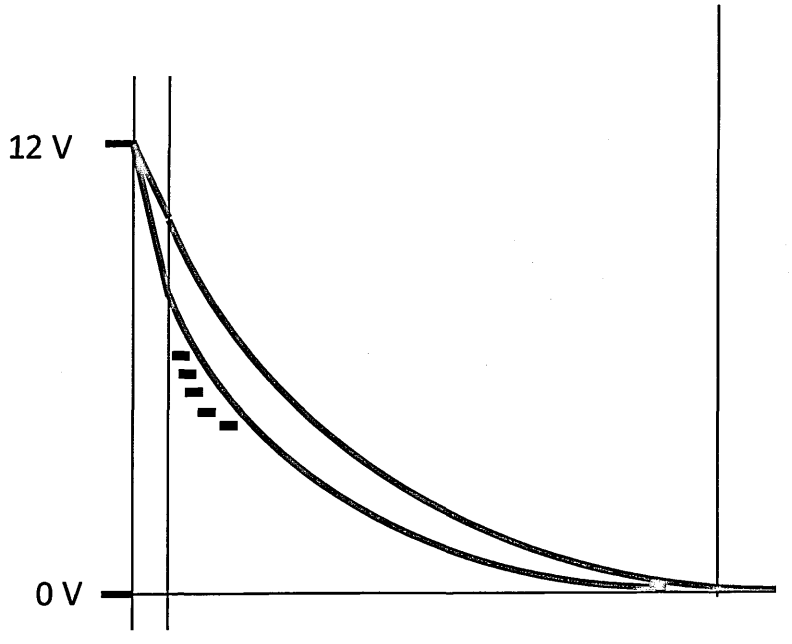


Figure 2-5. Surface channel storage

2.2.3.2 Buried Channel CCD

By incorporating a thin n- or p-type layer at the surface, as shown in Figure 2-6, the extra positive lattice charge causes the potential distribution to have a maximum value within the additional layer. Signal charge is stored and transferred at this maximum location and is therefore away from the influence of the interface traps. Much higher charge transfer efficiencies are typically achieved with the buried channel CCD (Janesick(a) 2001).

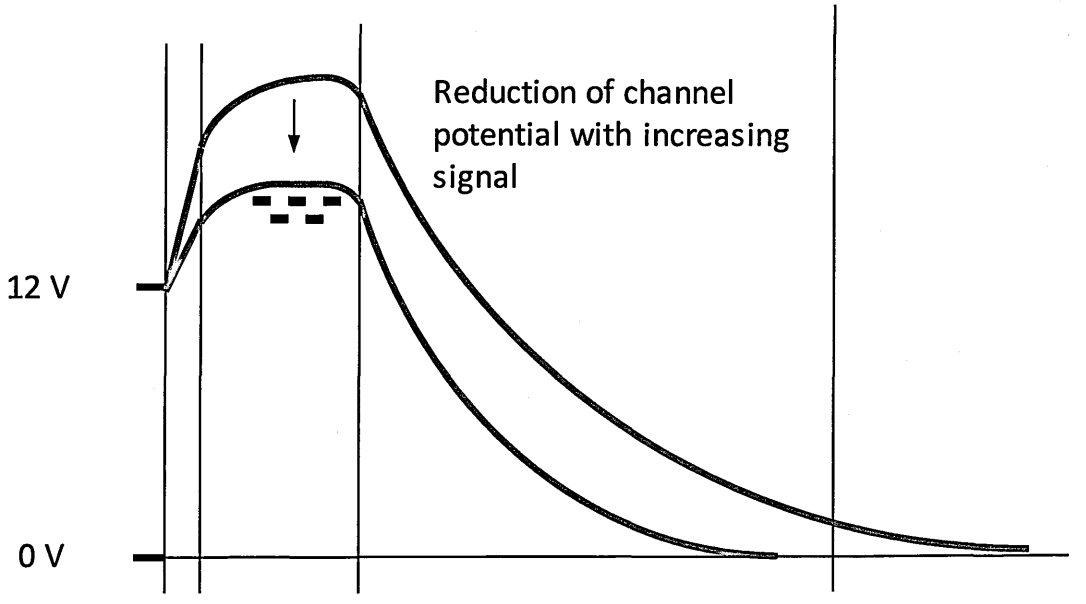


Figure 2-6. n-type buried channel storage, storing electrons, p-type buried channel would hold holes as signal charge.

2.3 Charge generation

The silicon substrate is in the form of a regular crystalline lattice. Each silicon atom is covalently bonded to four nearest-neighbour atoms in a tetrahedral type arrangement. An incident photon can 'knock out' a bonding electron which is then free to move through the silicon as signal, a process called the photo-electric effect.

2.3.1.1 Photoelectric effect

The photoelectric effect is a process whereby an incident photon of sufficient energy interacts with a binding electron causing it to be liberated from its bound state around

the atom. In silicon the electron becomes free to move through the lattice as signal. When liberated, the electron leaves behind an absence of an electron, termed a hole. Despite having lower mobility, the hole can also 'move' through the lattice by an adjustment of the other bonding electrons, shown by Figure 2-7 (Kane 1962).

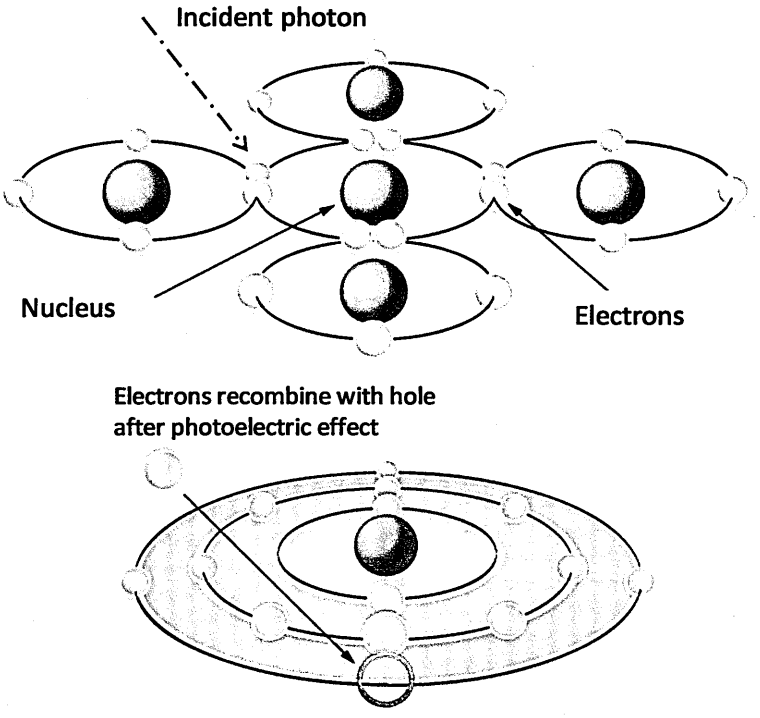


Figure 2-7. Photo-generation and the Silicon lattice (Commons 2012).

The energy of the incident photon, E_p, is given by equation 2.1 below; where h is Planck's constant, c the velocity and λ the wavelength of the incident radiation.

$$E_p = hc/\lambda \qquad (2.1)$$

The energy needed to create one e-h pair in silicon E_e is typically 3.65 eV. Electrons liberated with a photon energy $E_p > 3.65$ eV are said to be directly ionised (Bertolini 1968). Photons with lower energy can still free an electron by using energy contained within the lattice, known as indirect ionisation. This additional energy is in the form of thermal vibration or phonons and can make up the remaining energy. However, photons

must still have energy greater than 1.1 eV, the band gap energy, to utilise phonon energy to liberate electrons (Janesick(a) 2001).

Additionally photons with energies E_p greater than 3.65 eV can generate multiple e-h pairs. The initial liberated electron has the excess energy (E_p-E_e) in the form of kinetic energy and the energetic electron can collide with the other bound electrons generating more e-h pairs by impact ionisation (Geist(b) 1983). The mean number of electrons η liberated by a high energy photon is given by the equation (Geist(a) 1979):

$$\eta = E_p/E_e \tag{2.2}$$

Therefore X-ray photons of keV energies can generate hundreds of e-h pairs and for optical photons with 3.65 eV > E_p > 1.1 eV, each interaction generates a single e-h pair and η = 1, whist for an X-ray with photon energy ~6000 eV, 1600 e-h pairs will be generated.

2.3.1.2 Absorption depth

If a photon flux of F_p photons/cm^2/s is incident on silicon of thickness δx and the exit flux is (F_p - δF) photons/cm^2/s, then δF is related to δx by the equation:

$$\frac{\delta F_p}{F_p} = -\alpha\, \delta x \tag{2.3}$$

where α is termed the 'optical absorption coefficient'. Since every absorbed photon results in the generation of signal charge, by integration the rate of generation at depth x from the surface in electrons/cm^3/s is given by the equation:

$$G(x) = \eta\alpha \exp(-\alpha x) \tag{2.4}$$

The linear absorption coefficient for photons in silicon as a function of photon energy is illustrated in Figure 2-8.

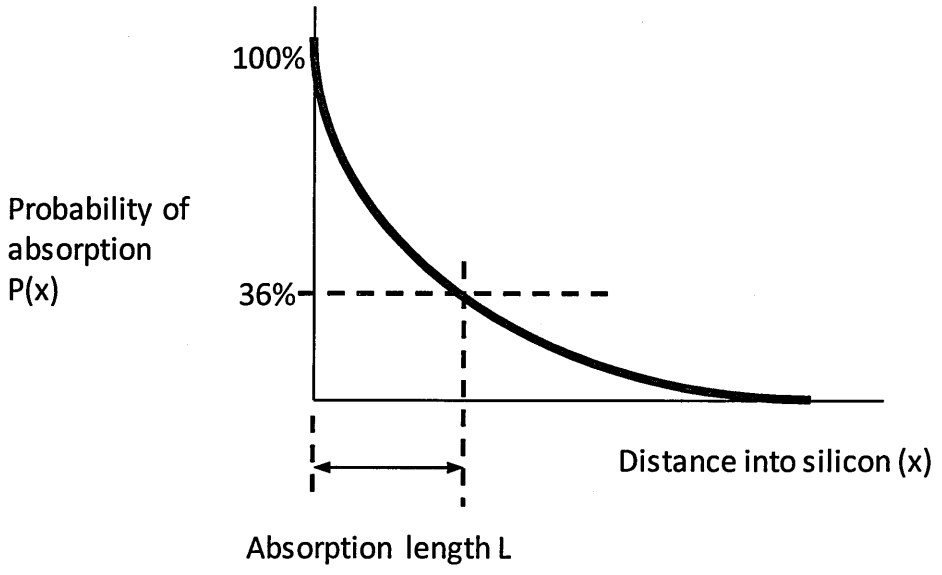


Figure 2-8. Probability of photon absorption.

The depth at which the absorption has fallen to 1/e times the maximum value at the surface is called the absorption length L_a, where:

$$L_a = 1/\alpha \tag{2.5}$$

Actual values for L_a are dependent on the photon energy, as shown in Figure 2-9. (Holland(b) 1990)

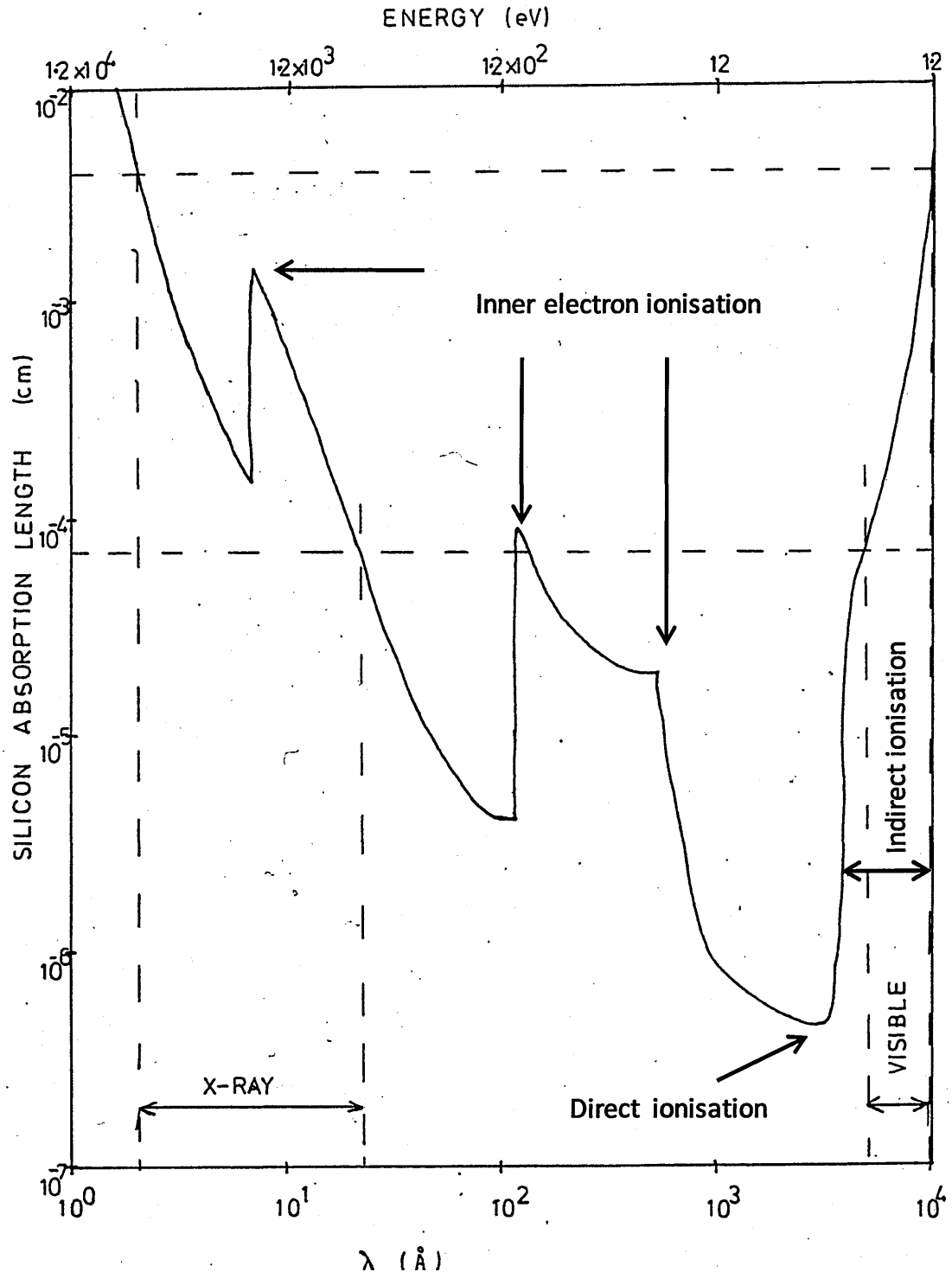


Figure 2-9. Photon absorption length for photons in silicon (Holland(b) 1990).

2.3.1.1 Quantum Efficiency

The quantum efficiency or QE is the fraction of incident photons that are sampled by the device. Actual values are dependent on the photon energy and the device structure. With reference to Figure 2-9, photons in the blue, UV and soft X-ray regions have a very short absorption length and are likely to be absorbed in the electrodes or other surface structures, causing signal loss and subsequently resulting in low QE. In the case of long-wavelength optical photons or high energy X-ray photons, the absorption length is so long that the photons are likely to pass right through a device without interacting and again resulting in low QE. It is only when the majority of the interactions are within the active thickness of a device that high useful QE values can be obtained (Murray 2008).

2.4 Charge storage

The photo-generated charge is attracted and stored within potential wells in the silicon. To maintain spatial precision, 0V barrier phases exist between each of the potential wells to separate the charge, Figure 2-10 shows the collection of charge underneath a biased charge collecting electrode.

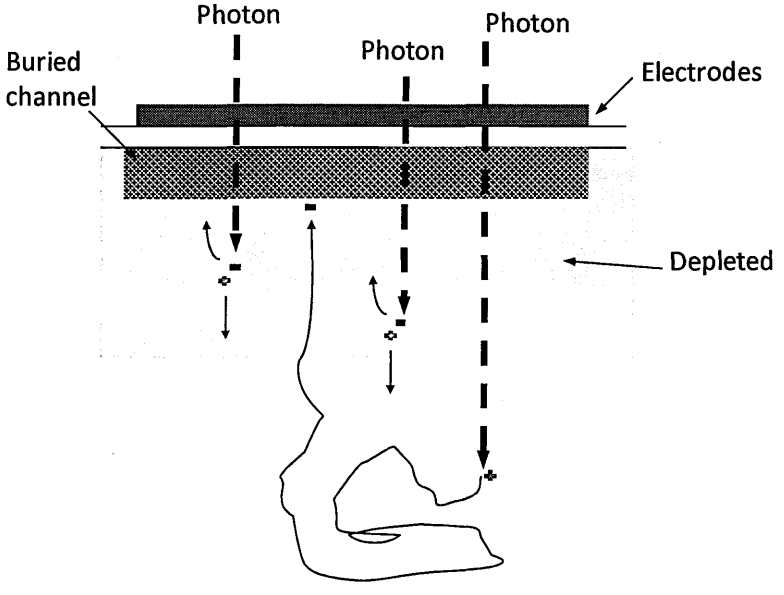


Figure 2-10. Electron generation in silicon.

During integration, which is the time allowed for any generated charge to be collected, one of the phases is held at around +12V forming a potential well to attract the electrons and allowing the charge to be stored. To prevent image smearing the barrier phases ($\Phi 1$ and $\Phi 3$) are held at 0V which stops charge from spilling over into neighbouring elements. However, electrons can also be generated in areas with two potential wells an equal distance away. In this case the electron has an equal probability to moving to either well; and with X-ray inputs where large numbers of electrons are concerned this introduces effects such as split events.

Described so far have been the basic means in which the CCD operates including; basic structures and the basic concepts of charge transfer, storage and generation. The following sections will describe some more advanced characteristics of the CCD including some alternative ways in which to operate them.

2.5 Practical image arrays

2.5.1 Pixel structure

A practical image sensor generally requires a two-dimensional array of charge collection elements called picture elements or pixels. Linear arrays have only a single line of elements.

Figure 2-11 shows how pixels are formed using a series of buried channels or 'columns' running perpendicular to the electrode structure. Along each column the electrodes at 12V form potential wells for charge storage which are isolated from the adjacent column by implants and adjacent row by barrier phases or electrodes.

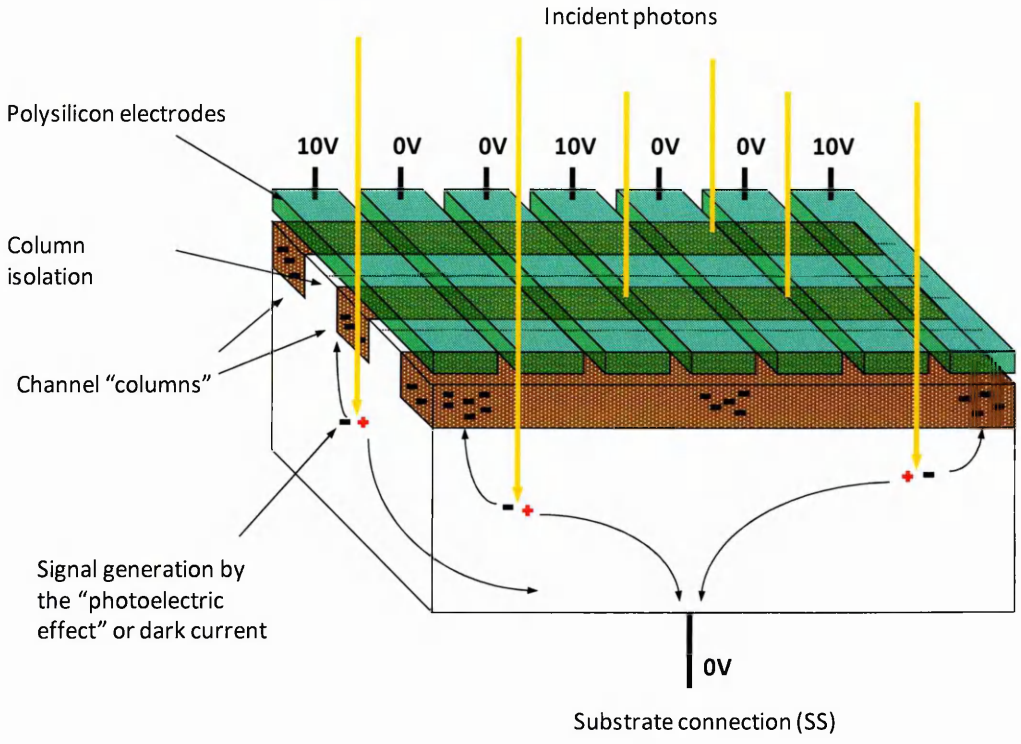


Figure 2-11. Pixel structure (Burt(a) 2012).

2.5.2 Full-frame array

The basic architecture of what is termed a full-frame array together with the associated drive pulse sequence is shown in Figure 2-12. The array has a total of 5 x 4 pixels and comprises an image section of the type shown in

Figure 2-11. Below the image section is a separately-clocked read-out register leading to a charge-to-voltage detection circuit of the type described later in Section 2.8. The drive pulses to the image area and read-out register have identifying prefix letters I and R, respectively.

In operation, a mechanical shutter is generally required to expose the sensor to the image illumination and to avoid image smear by limiting collection during the read-out operation. By way of an example the image is taken to be in the form of a capital F. With the shutter open the image section clocks are held with the IΦ2 phase at 12V and the

others at 0V thereby forming an array of potential wells. Photo-generated charge in the underlying silicon is collected as shown in Figure 2-11. The whole array of charge is known as a frame, originating from the term picture frame.

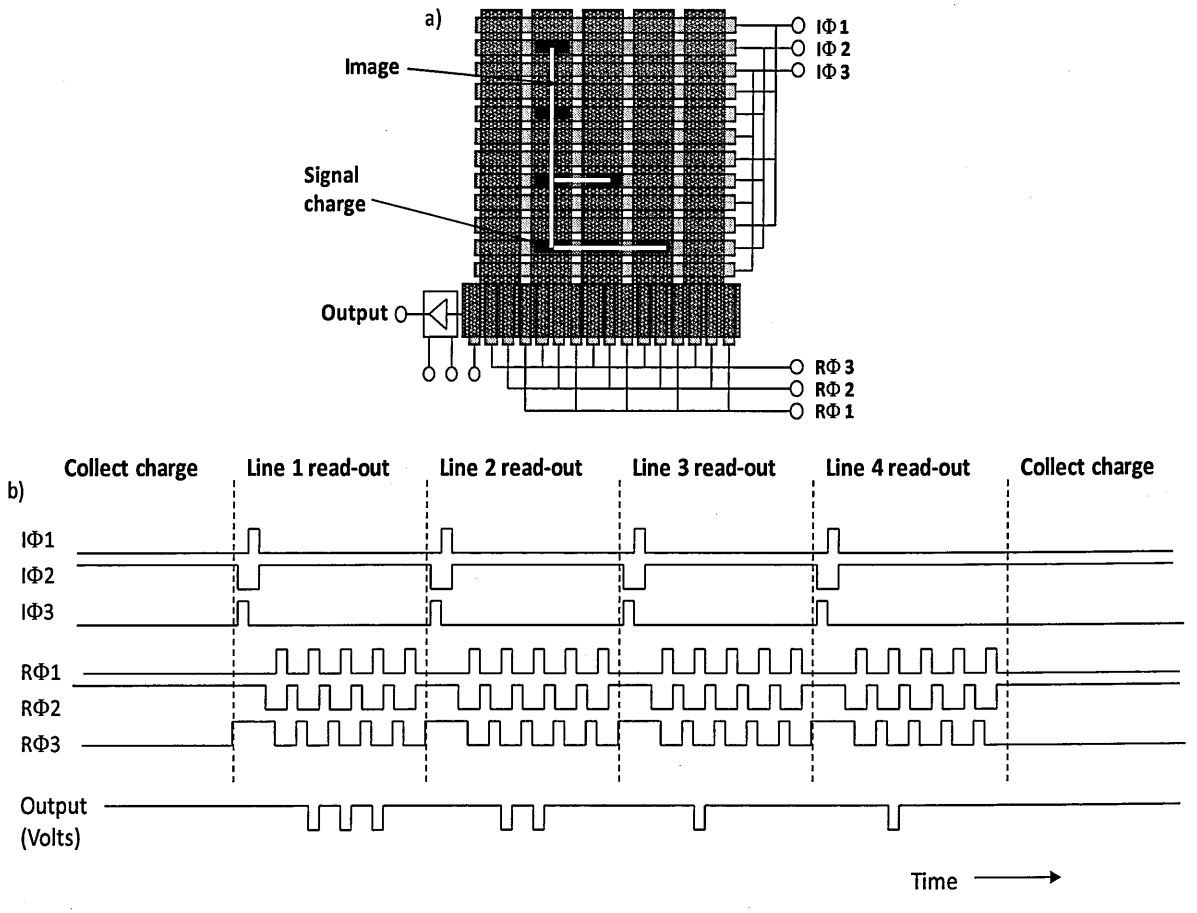


Figure 2-12. Full-frame array, a), and clocking sequence, b), (Burt(b) 2012).

At the end of the exposure period the shutter is closed and there is a single cycle of image section clocking. This transfers the frame of data down the image section by one pixel location, with the bottom line of charge signals transferred to the electrodes of the read-out register. The register is now clocked through 5 cycles to sequentially transfer the charge signals to the output circuit. Another single cycle of image section clocking follows to transfer the next line to the register for read-out, and so on, for all four lines. The shutter can then open for exposure of the next frame. Common practical image arrays can have image sizes from 256 x 256 up to 10000 x 10000 pixels.

Transfer down the image section is often known as parallel transfer and that along the read-out register as serial transfer.

2.5.3 Frame-transfer array

The shutter is necessary with the full-frame array to prevent spurious charge being picked up during transfer, but is impracticable for many applications. For these the frame-transfer approach can be used, as shown schematically below.

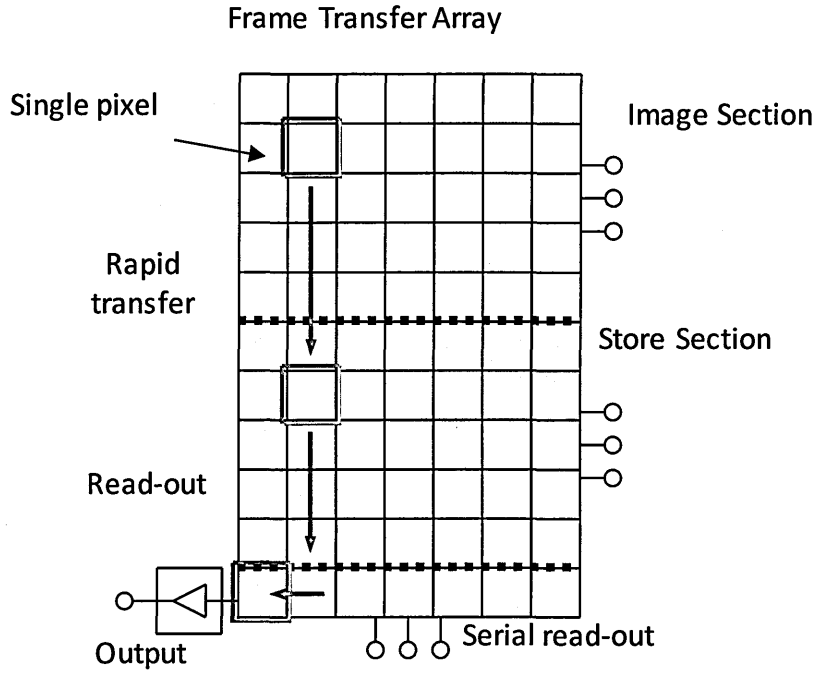


Figure 2-13. Frame-transfer array.

The device is essentially the same as the full-frame array but with an additional optically-shielded section between the image sections and register known as the store section (denoted by S). In operation, signal is collected in the image section as before but is then quickly transferred to the store section in typically less than 1ms (Burt(b) 2012). The frame in the store section is then read out as before, whilst the next frame is integrated in the image section, and so on through subsequent frames, removing the need for a shutter.

2.6 Alternative transfer modes

The main three transfer methods are 3-phase, 4-phase and 2-phase clocking. There are also some less well-known transfer methods such as the virtual phase.

2.6.1 Three-phase

The 3-phase CCD is the most common and the details of transfer have already been described. This type of clocking is useful as it allows total control of the direction of transfer. If two of the three phases are reversed in sequence, the charge will then move in the opposite direction. This is useful for clearing any unwanted charge to a drain or when using more than one output on a device.

2.6.2 Four-phase

A 4-phase CCD is similar to the previous type but with 4 electrodes per row element. The advantage is that charge can be stored under an adjacent pair of electrodes giving a higher full-well capacity versus 3-phase for a fixed pixel size, but the disadvantage is a more complex and slower clocking sequence.

2.6.3 Two-phase

A reduction in the number of phases per element gives simplicity of operation and can be achieved with a 2-phase structure. This device incorporates an additional positively doped region underneath one of the electrodes within the phase creating a sequence of steps of increasing potential. The principal advantages are that the clocking is; 1) simpler, 2) faster and 3) less critical than 3 and 4 phase alternatives as signal charge can never transfer backwards. Figure 2-14 shows a 2-phase device displaying the adjacent electrodes with identical timings. Stage t=0 shows the state of the device with no applied potentials to the electrodes to show how the implants affect the potential structure. Charge is generated at stage t=1 under a pair of adjacent electrodes, notice the level of one of the gates is

lower than the other creating a 'step' feature of increasing potential. Transfer is achieved at stage t =3 when the potential on Φ2 is increased and Φ1 lowered. Due to the implant the charge cannot travel backwards and is forced to travel forwards, stage t=4 completes the cycle.

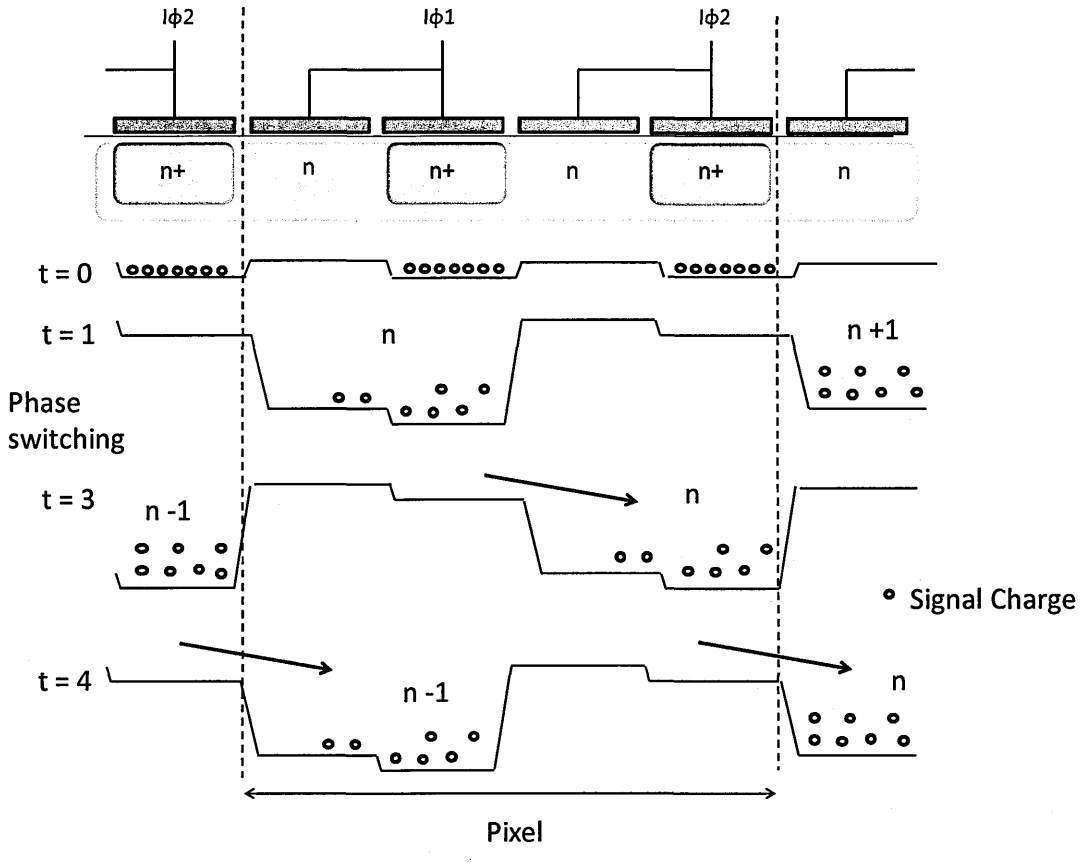


Figure 2-14. 2-phase clocking sequece.

Note that the device shown in Figure 2-14 is much like a 4-phase device but with the electrodes connected together in pairs. If this connection is made on-chip, then the direction of transfer is inbuilt and cannot be changed by the user. This would be done to reduce pin-count. Alternatively, if connections are made to the 4 phases, a change of direction is possible by using the opposite electrode pairing.

2.6.4 Virtual phase operation

This type of operation is less well-known than the methods described above and although not commonly used today, were adopted by large manufactures such as Texas Instruments (TI). It is of interest to show how these types of devices can be adapted to suit a purpose. This type of clocking is used with front illumined device where gate absorption of soft X-rays, UV and optical is a concern. The low QE at these wavelengths through absorption in the electrodes is partially resolved by leaving half the pixels 'open' and implementing a virtual phase (Janesick(a) 2001). This is similar to 2-phase clocking but instead of having another set of electrodes, to give an additional phase the semiconductor is implanted to create a static potential structure within the device. Figure 2-15 shows an illustration of the potentials within the device and how a charge packet moves through without merging.

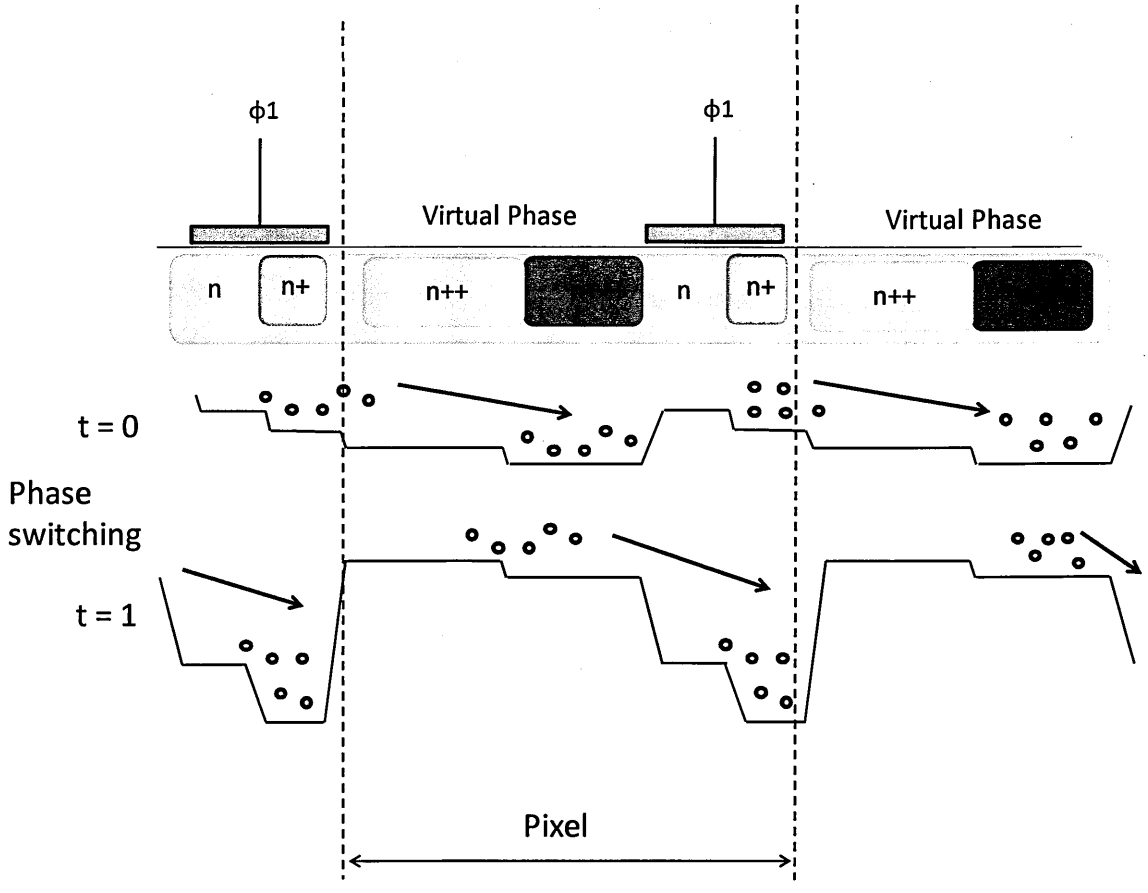


Figure 2-15. virtual phase clocking sequence.

In addition to the increased QE, another advantage is single-phase clocking leading to a faster, less complicated clocking sequence. However, a major disadvantage is that it is very difficult to control the internal doping profiles to achieve efficient transfer from the n+++ region to the adjacent gate and for this reason, the pixel structure has not been widely used. This clocking scheme also suffers from low full-well capacity and the inability to backward-clock.

2.7 Improving quantum efficiency

The QE of a CCD is highly dependent on the energy of the incident photons. High energy photons (> 10 keV) have a long absorption length passing beyond the depletion region of the device and low energy photons (< 0.5 keV) can interact in the electrode structure of the device hence not creating signal charge. Described below are some improvements made by CCD manufacturers to deal with the low QE at both extremes of the energy scale.

2.7.1 Open / thinned electrodes

Although back illumination can offer the best possible performance, as described later, front illuminated devices can also be improved. The first method is to remove parts of the electrode, as shown previously with the virtual phase structure, thereby creating an opening for the photons to enter the active silicon without being absorbed by the gate structure. A second method is to decrease their thickness, increasing the probability of lower X-ray energies to reach the active silicon area. Figure 2-16 and Figure 2-17 is an optical microscope image taken under this work of a FG100 test structure which is split into 4 quadrants, 2 of which have thinned electrodes and 2 an open electrode structure. Figure 2-18 is another microscope image of a CCD66 which uses a newer version of the thinned electrode structure which includes a high depletion region in the centre of each

pixel. A drawback of the thinned structure shown in the FG100 was a smaller depletion depth therefore this was introduced to increase the CCD's sensitivity to higher penetrating forms of radiation.

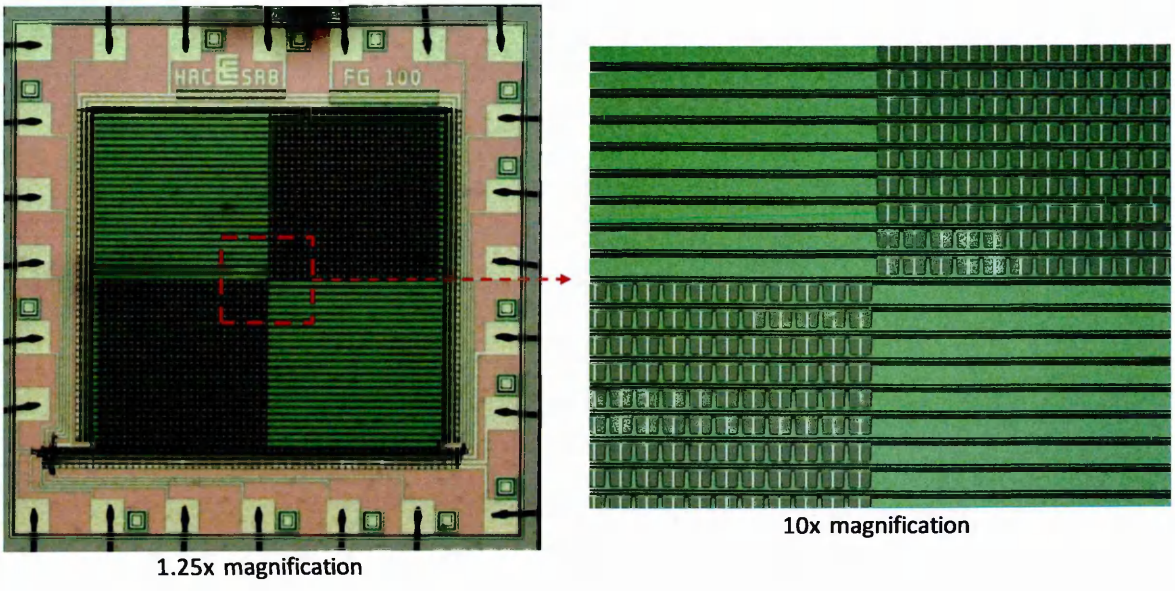


Figure 2-16. FG100 test structure with both a thinned and open electrode structure used for characterisation purposes.

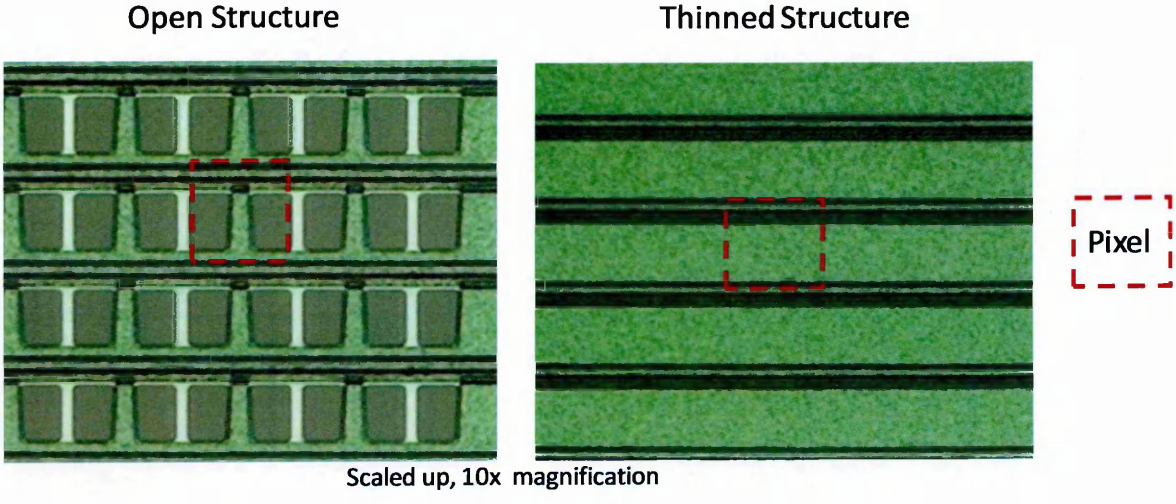


Figure 2-17. Open and thinned structures from the FG100 test structure, vertical column isolation no seen on the images keep the pixels from merging.

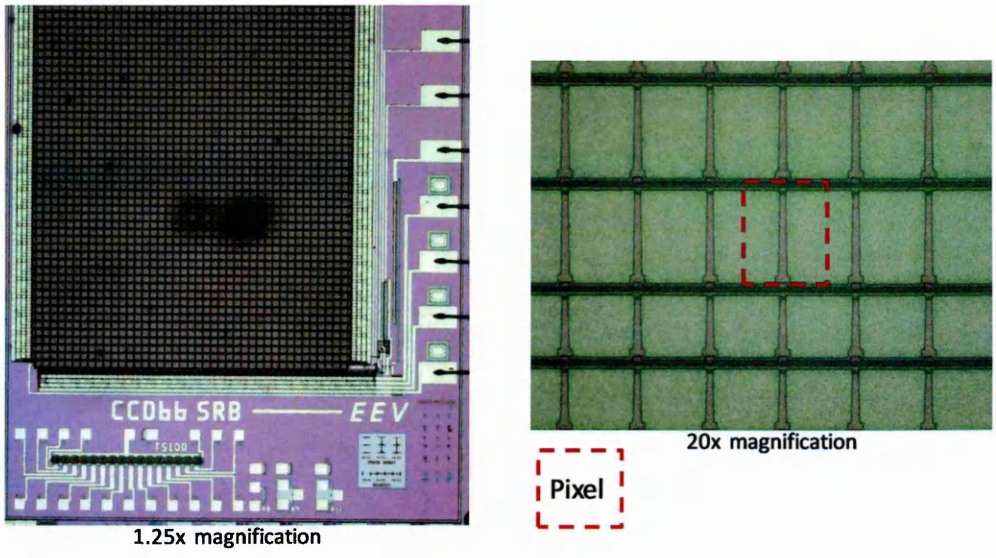


Figure 2-18. CCD66 with improved thinned electrode structure.

2.7.2 Back-illumination

The devices described so far are illuminated through the electrode structure. As described before, such front-illuminated devices suffered from poor QE at soft X-ray, UV and optical energies due to gate absorption. Back-illuminated devices have been produced to combat this by allowing the light to enter from the rear, through the back of the device rather than through the electrodes (Shortes 1974).

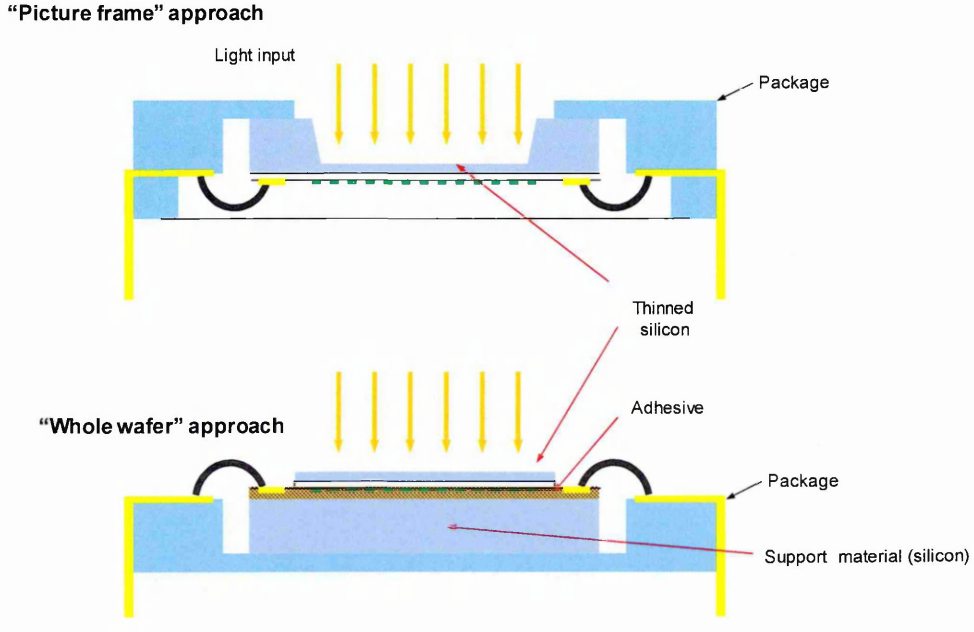


Figure 2-19. Two methods of back-thinning employed by CCD manufacturers (Burt(a) 2012).

Figure 2-19 shows two of the techniques used to create a back-illuminated device. The first involves only a part of the substrate being thinned leaving a thick edge for support. The other is to thin the whole substrate; this leaves the silicon vulnerable and, due to its thickness, unable to support itself. A supporting material, normally silicon, is used underneath.

The thinning process is vital to the efficient operation of these devices, details of which can be found in the literature (Janesick(a) 2001). The aim is to reduce the thickness to as near the depletion edge as possible. This minimises the possible loss of spatial resolution by charge diffusion in the undepleted field-free material.

After the thinning process is complete a native oxide layer of a few nm naturally grows on the back surface. The combination of oxygen and silicon gives rise to lattice defects, which create positive charge and recombination sites for electrons. Signal electrons produced by soft X-rays and UV radiation are generated near this interface and can interact with the surface leading to a decrease in QE. A short-term solution is to fill the sites prior to device operation; this process is called surface charging and is generally done with exposure to strong UV light. At cryogenic temperatures and under vacuum the QE value remains relatively stable for a long period of time. This is due to the emission time constant increasing as the temperature decreases causing the electrons to stay within the states for longer. A more permanent solution, and one widely adopted today, is to negatively dope the back surface of the device. This introduces a small potential step that repels signal electrons away from the surface. This method has the advantage of being stable but slightly decreases the QE at UV wavelengths.

2.7.3 High-resistivity silicon

High resistivity silicon is widely used in CCD fabrication for specialised applications (Holland(c) 2003). It is used to increase the depth of depletion (for a given operating voltage) such that the active thickness can be increased and still maintain good spatial resolution. A thicker device has higher QE for longer wavelength light and higher energy X-rays (Groom 2000).

2.8 Charge to voltage conversion

2.8.1 Output circuit

Figure 2-20 shows a typical CCD output circuit, which comprises of a detection node with associated capacitance C_n, a Reset Transistor and an output Source Follower transistor. The output is reset between successive pixel signals to avoid drift in the output node.

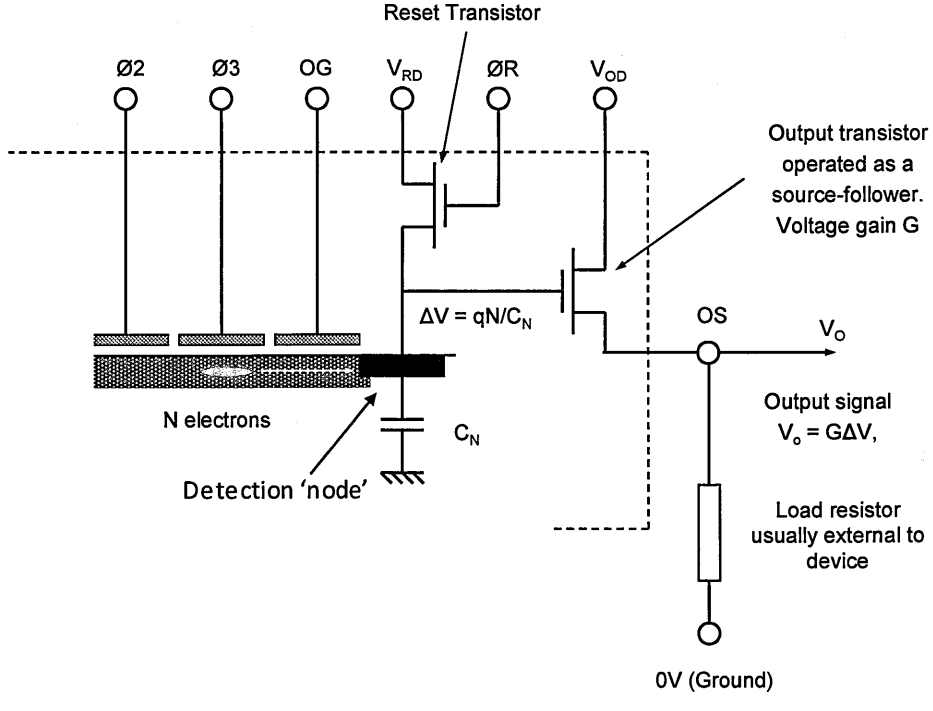


Figure 2-20. CCD output circuit (Burt(a) 2012).

Figure 2-21 shows the associated timing diagram.

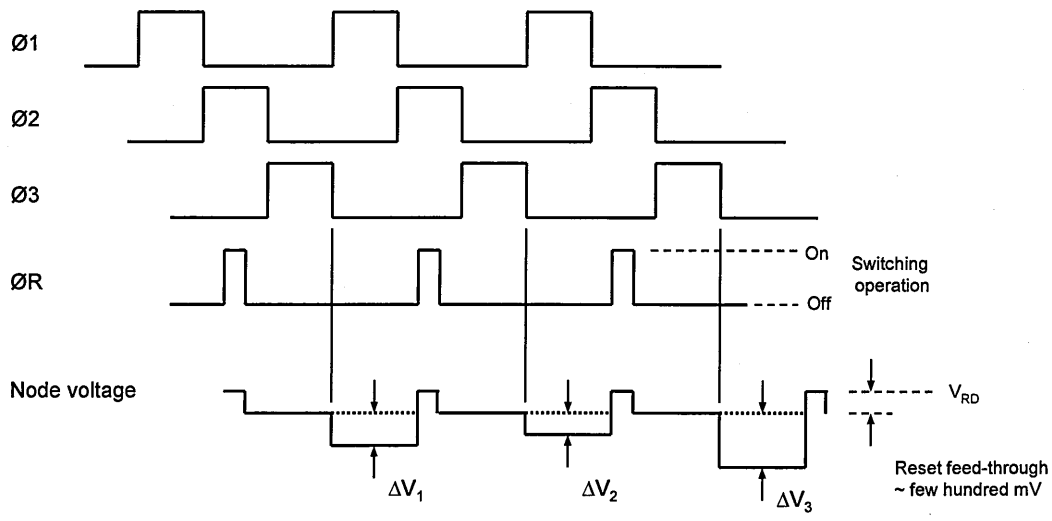


Figure 2-21. CCD output circuit timing diagram (Burt(a) 2012).

Between the last clocked electrode Φ3 and the output node is a DC biased electrode called the output gate, OG, with bias voltage V_{OG}. This is to minimise parasitic feed-through of Φ3 onto the output node by physically separating the two. Charge is transferred to the output node as Φ3 falls from 12V to 0V. Before this, a reset pulse is applied to the gate of the reset. This sets C_n, to the bias voltage on the reset transistor drain terminal, V_{RD}.

The source voltage V_S follows any change of voltage on the gate V_G caused by the new charge on the node, hence the term 'source follower'.

It may be noted in Figure 2-21 that there is parasitic feed-through of the reset pulse in the output waveform, typically of a few hundred mV amplitude. Typical bias values are V_{OG} = 2V, V_{RD} = 17V and V_{OD} = 28V.

2.9 Noise performance

Performance can depend on many different noise sources including; reset noise, transistor noise, shot noise, fixed pattern noise and dark signal as next described.

2.9.1 Output circuit noise

There are two sources of noise associated with the output circuit, reset and transistor.

2.9.1.1 Reset noise

During the reset operation (ΦR at 12V) the reset transistor is conducting and the channel presents a series resistance R. Johnson noise associated with this resistance is in series with V_{RD} and becomes sampled-and-held on C_n as ΦR goes to 0V. This gives an output-to-output fluctuation in the level to which C_n is reset. The Johnson noise voltage V_n is given by:

$$V_n = \sqrt{(4kTRB)} \qquad (2.6)$$

Where k is Boltzmann's constant and T is absolute temperature. B is the noise bandwidth.

From equation 2.4, since the transfer of a single electron to the node gives a voltage change equal to q/C_n, the fluctuations can be expressed as an equivalent number of electrons N_R:

Reset noise can be eliminated by double-sampling the output. This is performed in the post-CCD video processing circuitry. The output waveform is firstly sampled after resetting and then with signal present. Subtracting the first sample from the second eliminates the common reset voltage level. The operation is known as 'correlated double sampling' or CDS and will be described in greater detail in Chapter 4.

2.9.1.2 Transistor noise

Johnson noise (Johnson 1928) associated with the channel noise of the source follower transistor causes a temporal fluctuation in the voltage at the output source terminal. Normally this is small in comparison with the reset fluctuation, but it becomes the limiting factor when CDS is used. This fluctuation is also known as the 1/f noise. The noise voltage is usually measured in terms of the spectral density with results as shown schematically in Figure 2-22 (Tuite 2012). The frequency at which the 1/f and white noise components are of equal magnitude is termed the 'corner frequency' and shown as f_c.

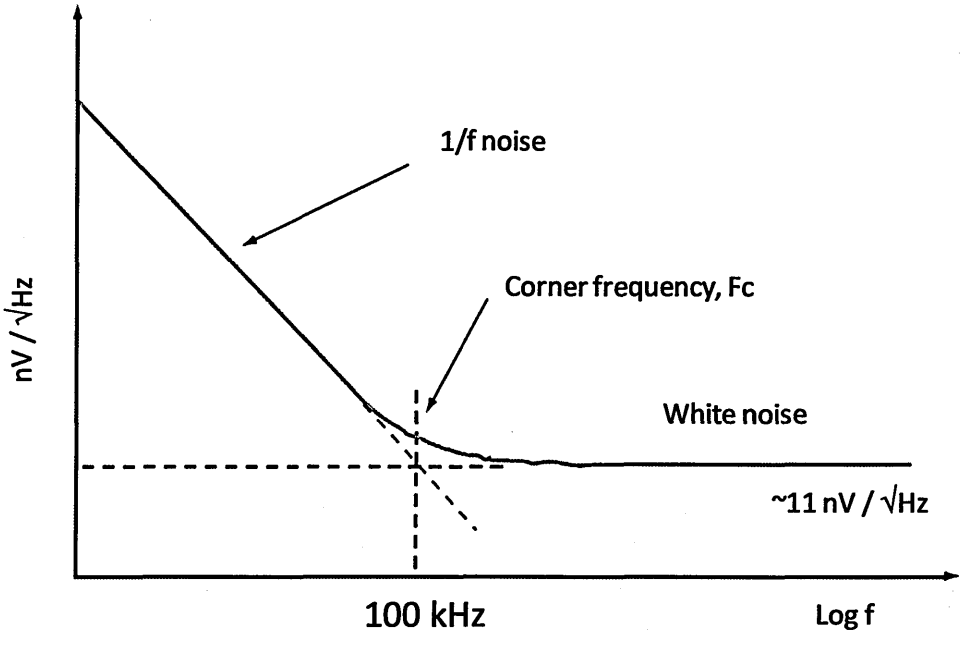


Figure 2-22. dependency of white and 1/f noise on frequency.

2.9.2 Shot noise and Fano factor

Shot noise is a temporal fluctuation in the number of photons being emitted from a source and this can lead to a spatial variation in the number of photons incident on each pixel of the CCD. Under conditions of uniform illumination, if the mean number of photons incident on each pixel during the collection period is N_P, shot noise causes a pixel-to-pixel fluctuation which can be characterised by a normal distribution having a standard deviation $\sigma = \sqrt{N_P}$. The fluctuations become more pronounced at low flux levels. This can be illustrated by a Monte Carlo simulation showing a 20 x 20 pixel region uniformly illuminated with 200 incident photons, as shown in Figure 2-23, where it may be noted that the pixels have a distribution from 0 to 4 photons.

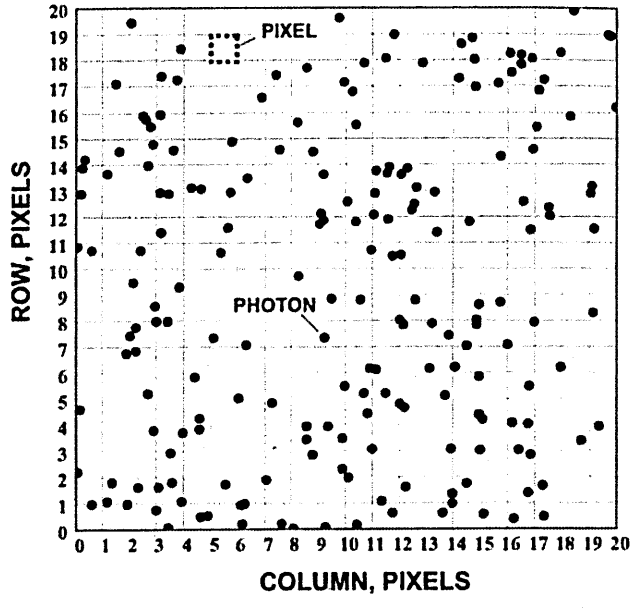


Figure 2-23. A Monte Carlo simulation showing incident photons on a 20 x 20 pixel array (Janesick(b) 2007).

The mean number of electrons generated in each pixel during the collection period is given by:

$$NS = QE\eta NP \tag{2.7}$$

where η is the quantum yield. The corresponding fluctuation due to shot noise is:

$$\sigma = \sqrt{N_s} \quad for \; n = 1 \tag{2.8}$$

However, for $\eta > 1$ the generation of secondary electrons by impact ionisation is somewhat dependent on the earlier generation and the interactions have a degree of correlation. This results in the fluctuations about the mean being less than would be expected for pure shot noise, i.e. if the electrons were all generated by individual photons, and this is characterised using the Fano factor, F, where $\sigma = \sqrt{FN_S}$. The value depends on the material but for silicon F is about 0.115.

2.9.3 Dark signal

Electrons can be thermally excited from the valence to the conduction band by way of trapping states and this leads to the generation of signal charge in the absence of illumination. This spurious charge is usually described as dark signal. If the dark signal collected in a time t within a pixel of area A is N_D electrons, then for purposes of comparison between device types it is conventional to calculate the dark current I_D per unit area using:

$$I_D = \frac{qN_D}{At} \tag{2.9}$$

The dark current is highly dependent on the temperature, as shown below, and values are often normalised to a standard reference temperature, typically 20°C. Typically:

$$\frac{I_D}{I_{DO}} = 122T^3 \exp\left(-\frac{6400}{T}\right) \tag{2.10}$$

where I_{DO} is the dark current at 20°C. Operation at cryogenic temperatures can usually reduce the dark signal to negligible levels. The dark signal has associated shot noise given by $\sigma = \sqrt{N_D}$ electrons rms. The sources of the dark current found in the CCD are shown in Figure 2-12.

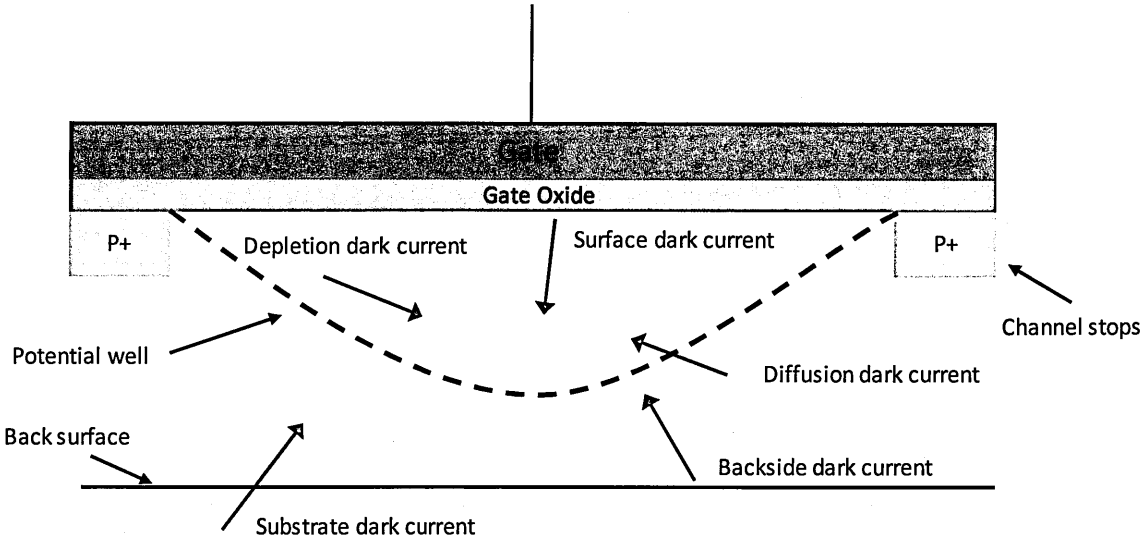


Figure 2-24. Regions on dark current in a CCD (Janesick(a) 2001).

2.9.4 Total temporal noise

The total system noise in electrons N_T is the rms combination of the various components, namely:

$$N_T = (N_A + FN_S + N_D) \tag{2.11}$$

where F = 1 for photon energies $E_P < 3.65$ eV and F = 0.115 for $E_P >> 3.65$ eV.

2.9.5 Fixed-pattern noise

The noise sources described so far are regarded as 'temporal' because they result in frame-to-frame fluctuations in the measured signal level from a given pixel under conditions of uniform illumination. Various imperfections can also give a fixed pixel-to-pixel variation and these variations are termed 'fixed-pattern noise'. These imperfections can normally be identified and removed from the data.

2.10 Conclusion

The concepts behind signal generation, collection, transport, measurement and noise have been described. This theory forms the basis of the next chapter which describes a more custom device namely the EMCCD. It also allows for further and more complex investigations into device properties and characteristics as will be become clear in later sections.

Chapter 3: The Electron Multiplying CCD

The Electron Multiplying CCD (EMCCD) is an image sensor whose architecture and design are similar to that of a traditional CCD but for an additional on-chip gain mechanism. This chapter will describe the processes involved in the gain mechanism followed by a description of an EMCCD device.

3.1 Avalanche multiplication

Impact ionisation occurs when an electron of sufficient kinetic energy collides with a bound electron, releasing it from orbit. If the kinetic energy of that initial electron is high enough or energy is provided by an external source then it may ionise a second electron. The secondary electron may also have enough kinetic energy to ionise a third electron, and the third electron a forth electron, and so on through more generation. The effect of cautiously adding energy into the system to cause impact ionisation is called avalanche multiplication. A way in which this effect can occur, represented in Figure 3-1, is through electrons passing through a high electric field; the electron gains kinetic energy and can therefore liberate electrons from orbit. This new unconstrained electron is accelerated by the same field and now too has enough energy to liberate another electron and so on; creating a runaway avalanche effect. Another common impact ionisation effect in semiconductor imaging is high energy photon absorption. This effect is not strictly avalanche multiplication, however, there is a cascade effect observed as the energy from the photon is absorbed into the material, also illustrated in Figure 3-1. This electron goes on to liberate other electrons which in turn have sufficient energy to ionise other atoms to create what is called an electron cloud.

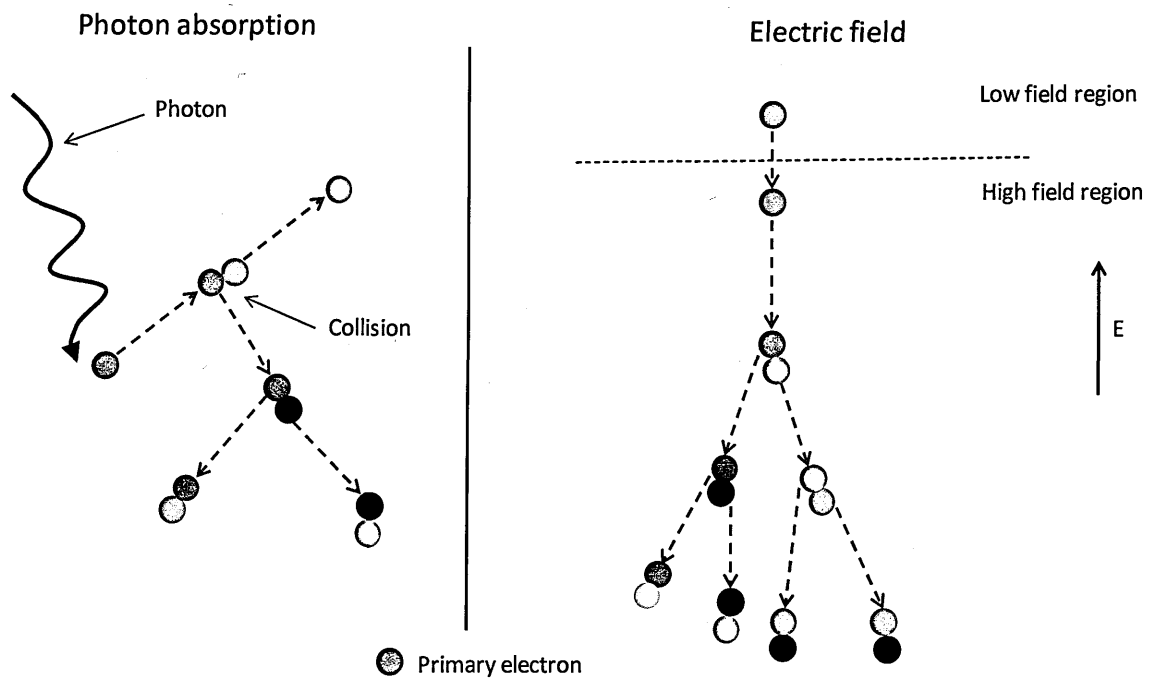


Figure 3-1. Impact ionisation due to high energy photon absorption (left) and impact ionisation due to a high electric field (right).

The average energy required for an electron to ionise another electron is dependent on the material and is 3.65eV for Silicon (Bertolini 1968). Described below is the avalanche process relevant to this work.

3.1.1 Avalanche mechanism

The basic behaviour of an electron in an applied field is described here, however due to the complex nature of this subject, more detail can be found in the literature (Jacoboni 1977) (Sze 1981). At zero field the electrons have an instantaneous thermal velocity u_T. This is obtained by equating their kinetic energy $\frac{1}{2}mu_T^2$ to their thermal energy 3kT/2, but with a random path caused by interactions with acoustic phonons (coherent vibrations of atoms in a single direction from equilibrium).

At low fields, E, an additional drift velocity component u_D is superimposed on the random motion as shown by Figure 3-2. The relationship is $u_D = \mu_o E$, where μ_o is the mobility. The electrons tend to gain energy from the field and, at sufficiently high fields, the scattering

becomes dominated by the higher energy optical phonons (out of phase vibrations of atoms going in opposite directions, due to differences in charge or mass) with the result that the drift velocity reaches a constant or saturated value given by $u_S \sim \sqrt{(8E_P/3m)} \sim 10^7$ cm/s, where E_P is the optical-phonon energy and m is the mass of the electron (Sze 1981).

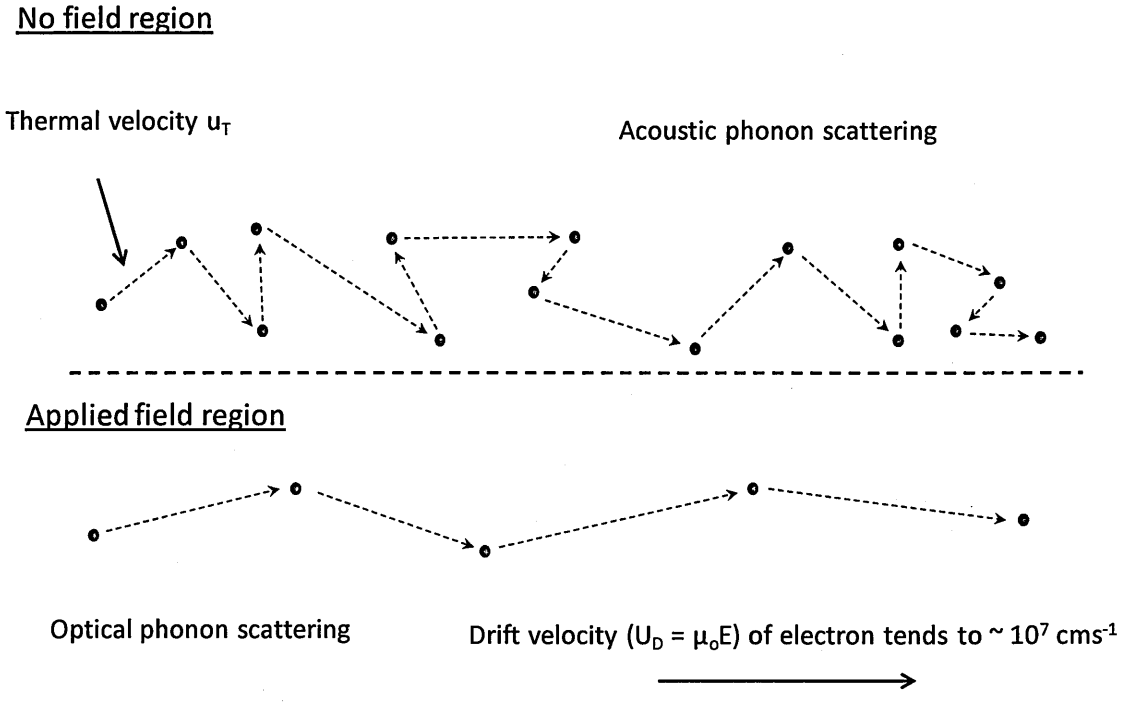


Figure 3-2. Electron path shown in different field conditions. When a field is applied the path of the electron is 'stretched' resulting in a higher drift velocity.

The resulting velocity-field characteristic is shown in Figure 3-3, where the low-field mobility is represented as μ_o.

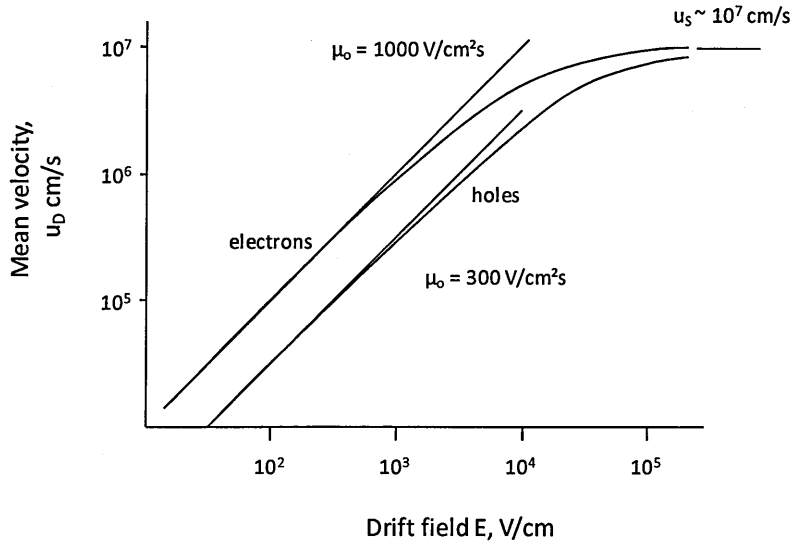


Figure 3-3. Mean velocity of electrons and holes at high fields showing saturation at 10^7 cm/s (Jacoboni 1977).

At fields higher than u_S/μ_o the velocity remains constant but the mean electron energy continues to rise, as shown in Figure 3-4 and the electrons are said to be 'hot'.

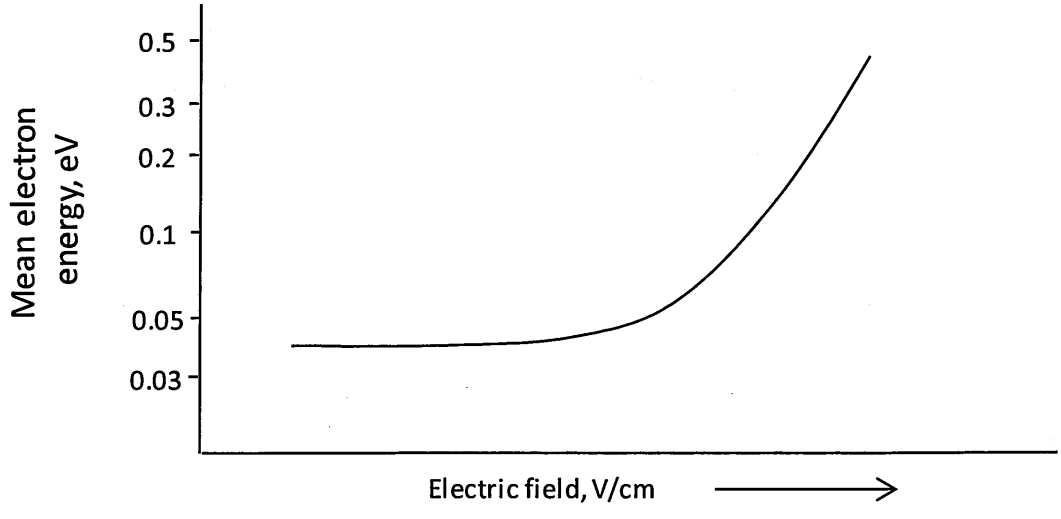


Figure 3-4. Mean energy of the electron shown to increase even after the saturation of velocity, resulting in an increase in temperature and a 'hot' electron (IPTI 2004).

The hot electrons will then inelastically collide with a bound electron, losing some of its kinetic energy to ionise it. The two electrons then restart the process of gaining kinetic energy from the applied field (Sze 1981).

3.2 The EMCCD

The EMCCD utilises the avalanche multiplication process described above to enhance the signal to noise and create a more sensitive device. The EMCCD includes an avalanche gain register which houses high voltage phases to accelerate the generated charge.

Some detectors such as Avalanche Photos Diodes (APDs) also use this effect in a single stage where gains of 10^3-10^5 may be observed. This however requires very high fields which are difficult to achieve in an MOS structure. The EMCCD uses a 'smaller' avalanche effect to replicate this by having multiple avalanching regions.

3.2.1 Avalanche gain register

The avalanche gain register is an additional register following an ordinary CCD serial register. This register has high voltage phases built into it which accelerate the generated charge causing impact ionisation and avalanche multiplication. Figure 3-5 shows the basic structure of an avalanche gain register element in the form of the potential well model.

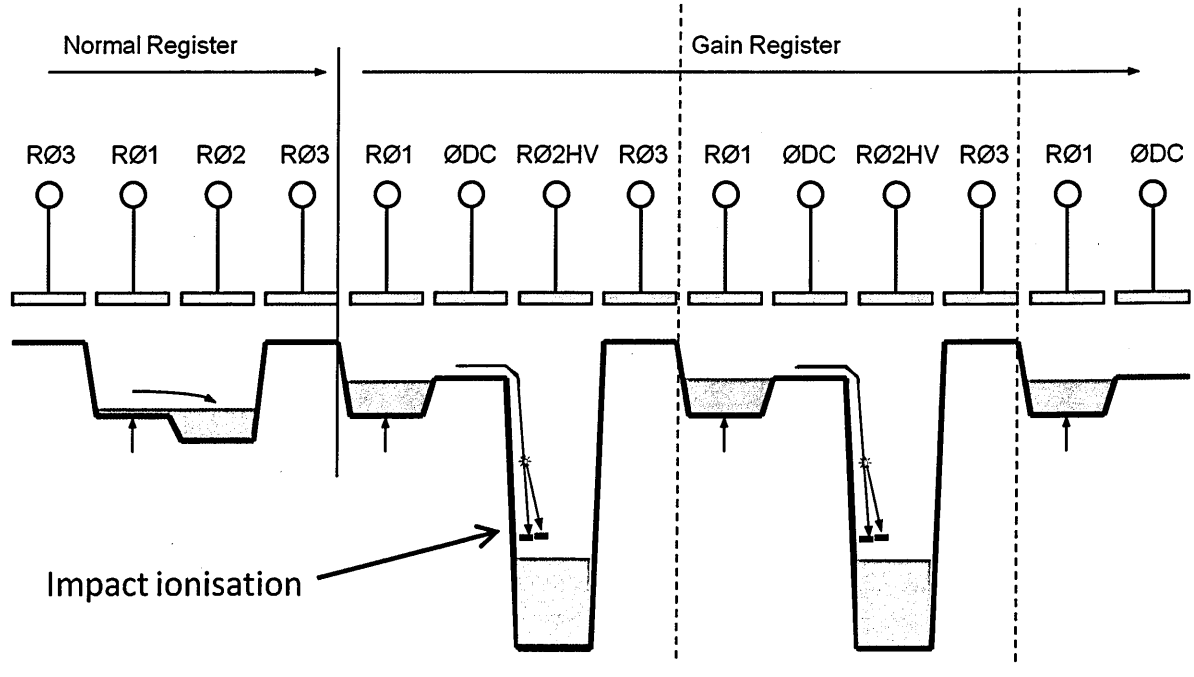


Figure 3-5. Basic architecture of an EMCCD avalanche gain register.

Unlike the normal register shown on the left of the figure the avalanche gain register has 4 phases, two of which are identical to the ordinary register (RΦ1 & RΦ3), a DC barrier phase (ΦDC) and lastly the avalanche phase (RΦ2HV). The avalanche process takes place between the ΦDC and RΦ2HV phases. The term 'avalanche potential' used in this thesis is the term used to describe the applied gate voltage to RΦ2HV rather than the potential difference between ΦDC and RΦ2HV. The EMCCD utilises relatively low voltages for this type of process with voltages in the region of 30V – 40V producing an avalanche effect. This is possible because there are over 500 avalanche elements in each register each producing a small gain, so the gain per element is compounded (Mackay(a) 2001).

The avalanche gain register is constructed in a similar way to an ordinary serial register with poly-silicon electrodes and grown oxides. However, due to the high voltage on the avalanche phase extra precautions are required. The first EMCCDs encountered difficulties as the high voltage would exceed the boundaries of the channel and pull in excess charge generated in the surrounding silicon leading to very high dark currents. The current EMCCD design is to house the avalanche phase within a low voltage DC phase to enable both efficient transfer and to isolate it from the surrounding area. Figure 3-6 shows a top down view of a single element, portraying how an avalanche phase is laid out.

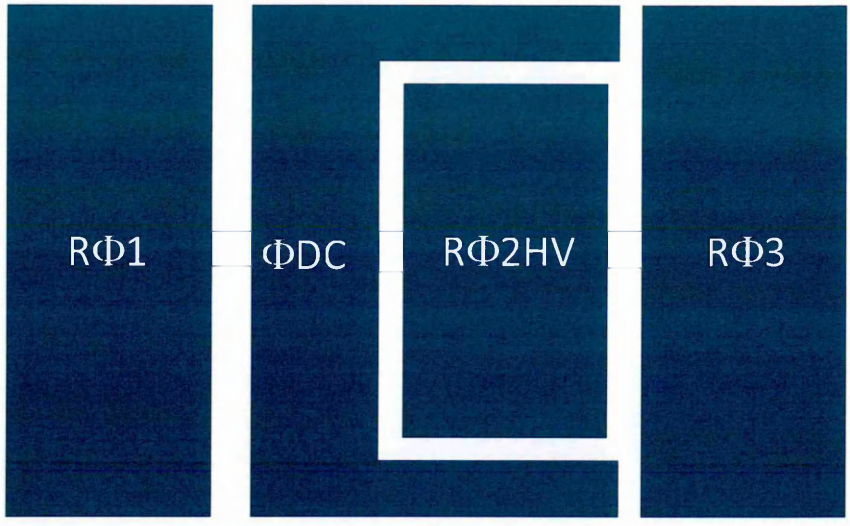


Figure 3-6. electrode layout of a single phase within the avalanche gain register.

As mentioned before, in addition to isolating the high voltage phase the DC phase also acts as a useful barrier between RΦ1 and RΦ2HV. Looking back to Figure 3-5, it allows for the avalanching bias to be established before RΦ1 is turned off ensuring that the signal charge experiences the full effect of the potential difference.

To make a compact design, the gain register is folded back alongside the standard register. The transition between the serial register and avalanche gain register is made via a corner section consisting of wedge shaped electrodes allowing for the signal charge to pass around in a semi-circle. Following the avalanche register are a dozen or so normal register elements leading to the output of the device. These are here to keep the high voltage clocking well separated from the output circuit. Figure 3-7 shows an optical microscope image of both the corner elements and the elements following the gain register.

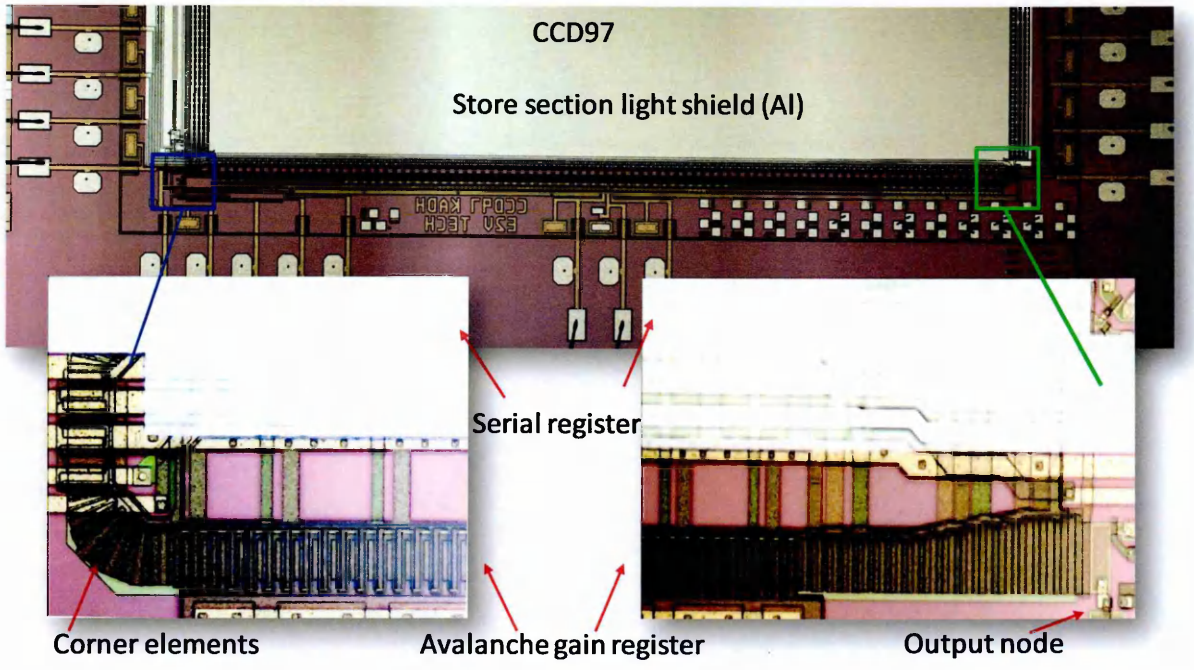


Figure 3-7. Microscope image of the entire bottom section of the device (top image, x20 mag stitched). Zoomed in regions (bottom images) of the corner elements and output regions (x50 mag) showing the transition between serial elements and gain elements.

These transition zones produce some interesting results when observing dark signal generation as the size, shape and location of the pixels all vary. These results are presented in Chapter 4.

3.2.2 Output Amplifiers

The majority of EMCCDs have two outputs, these can be seen in the bottom right of Figure 3-7. One of the outputs is after the ordinary serial register allowing the device to be used in a zero-gain mode and exactly the same as an ordinary CCD. The serial register operates in 3-phase allowing the direction of transfer to be changed, this allows for the avalanche register to be added as an extension. The second output is therefore after the avalanche register.

The responsivity of the two outputs is different due to the amount of signal each output is likely to receive. For a CCD97 the typical responsivity for the high responsivity (HR)

amplifier proceeding the serial register is 5.3 μV/e^- and for the large signal (LS) amplifier proceeding the avalanche gain register is 1.1 μV/e^-. For the HR output this means that for a full-well capacity of ~ 1x10^5 electrons, it will produce ~0.5V of signal where ADC saturation occurs at around 1V. However for the LS output it means that with 1.1 μV/e- and with a moderate EM-gain of 100G then only ~1x104 electrons can be sampled in image area.

3.2.3 Probability of impact ionisation

The average multiplication for each individual gain element within the avalanche register can vary from 0% to a maximum of approximately 1.5% depending on the voltage applied to the avalanche phase (Mackay(a) 2001). The maximum is a practical limit as set by the onset of image artefacts, e.g. flashes in the image, signal smearing and damage to the MOS structure past 50V. A typical value for normal operation is about 1%. The following worked example shows a method to calculate the overall gain for the entire gain register.

Consider a single element within the avalanche register having no multiplication. This can be represented as a gain, g = 1.

If there is now a 1% probability of multiplication within that single element, g now becomes:

$$g = (1 + 0.01) = 1.01 \qquad (3.1)$$

Now consider a second element with an equal chance of 1%, the chance of probability within the second element is independent of the last and is cumulative and therefore forms an 'AND' probability statement. The overall gain, G is therefore given by:

$$G = 1.01 \times 1.01 \qquad (3.2)$$

Where the first term is from the first element and the second from the second element.

This can now be generalised for any given probability, p, and for any number of gain elements, n:

$$G = (1 + p)^n \tag{3.3}$$

A voltage difference between ΦDC and RΦ2HV of approximately 40V will produce a probability per stage of ~ 1% and with 591 elements this yields a gain of 358 (1.01^{591}) while a voltage of approximately 44V, produces a 1.5% probability leading to a maximum approximate gain of 6628 (1.015^{591}) (Mackay(a) 2001).

3.2.4 EMCCD gain

The most important thing regarding EMCCD gain compared to other types of gain .i.e. amplifier gain, is that it occurs within the charge domain of the device. The avalanche gain is applied within a device transport register and before the charge to voltage conversion. Applying the gain this way around, in contrast to after, results in an increase in signal without an increase in read-out noise. This allows for very fast read-out speeds which would otherwise excessively increase amplifier noise. It has been reported that sub-electron equivalent read-noise can be obtained when operating at MHz pixels rates. This is particularly useful with photon counting imaging applications (Mackay(a) 2001) (Jerram 2001). It is important to note that any unwanted signal generated on-chip from cosmetic defects and dark signal will also have the same gain applied to them. It is essential therefore to sufficiently cool devices such as to reduce the unwanted signals. Figure 3-8 shows a schematic comparison between the different types of gain.

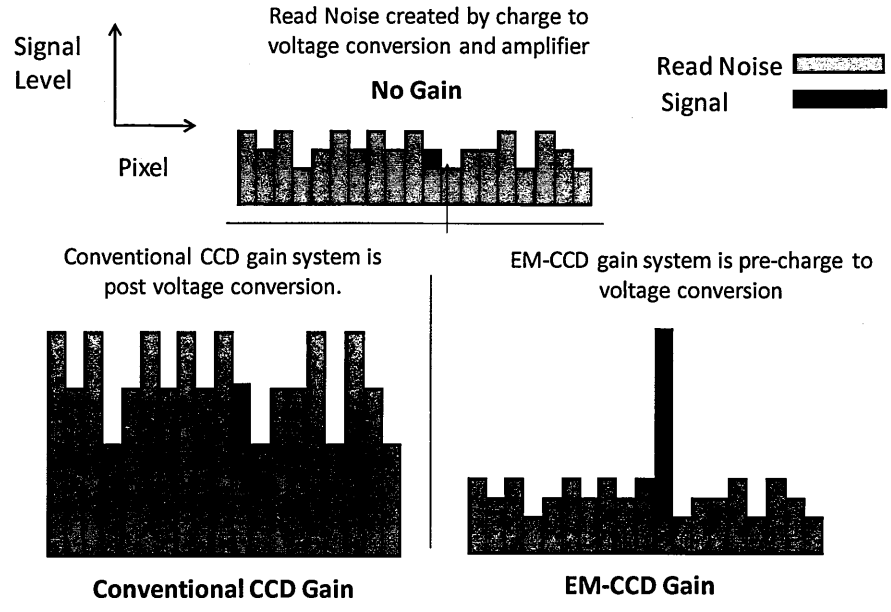


Figure 3-8. Comparison between convention CC gain and avalache multiplication gain.

Measurements of gain and its dependence of avalanche potential and temperature are presented in Chapter 4.

3.3 Noise

Described below are the key noise sources that are important when considering EMCCD technology.

3.3.1 Avalanche multiplication shot noise

The process of impact ionisation is a stochastic one producing a mean probability of multiplication across the whole register. This introduces shot noise on the gain process, a noise source not seen in conventional CCDs (Robbins(a) 2003).

Each electron during the gain process may be seen to act independently and due to the random nature of the multiplication process different electrons will create a dissimilar number of avalanche electrons. An additional noise factor is therefore required and acts to increase the noise on any signal which undergoes avalanche multiplication by a factor, known as the excess noise factor, E_N. The factor is given by equation 3.4 (Henecek 2001).

$$F^2 = \frac{\sigma_m^2}{G^2\sigma_i^2} \tag{3.4}$$

Where G is total gain, σ_m is the variance on the multiplied signal, n_m, and σ_i is the variance on the injected signal, n_i. The gain at each stage, g, can be treated as a Bernoulli process and the number of output electrons can be described by a Binomial distribution. The details of this expansion can be found in the literature (Robbins(a) 2003). Equation 3.5, is substituted into equation 3.4 to obtain 3.6:

$$\sigma_m^2 = n_i G\left(\frac{2G+g-1}{g+1}\right) \tag{3.5}$$

$$F^2 = \frac{2G+g-1}{G(1+g)} \tag{3.6}$$

The profile of the above equation is graphically shown in Figure 3-9, where at high gains F^2 tends to 2 giving a value of ~1.4 for E_N (Hall 2010).

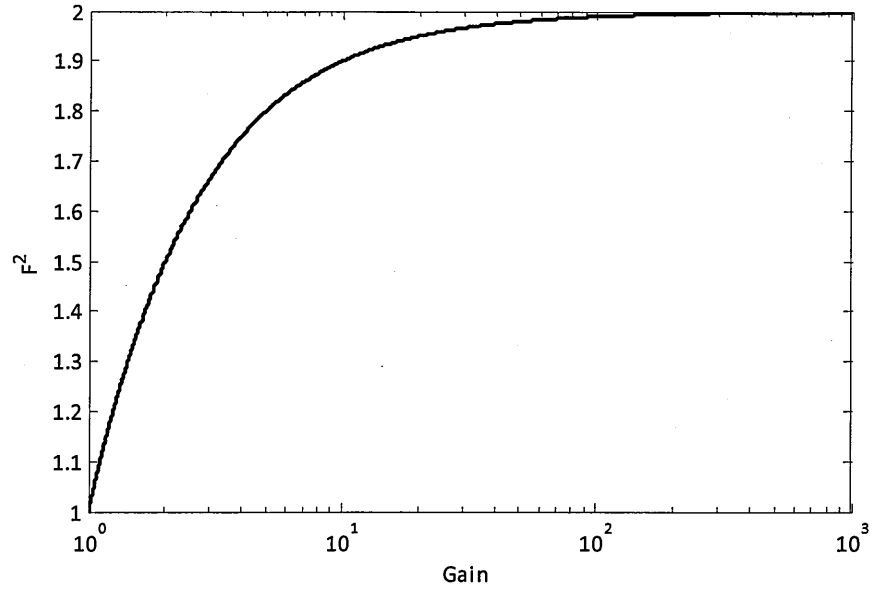


Figure 3-9. Excess noise factor as a function of gain (Hall 2010).

3.4 EMCCDs for space flight

EMCCDs have been widely used in terrestrial applications with uses in medicine (Teo 2006) (Takeda(c) 2008), military applications (Heim 2006), astronomy (Mackay(b) 2010) (Wei and Zhao-Wang 2006), cyclotrons applications and many others (Robbins(c) 2008). However, with the EMCCD being a relatively new technology they have yet to be used in space. Prior to being considered as a technology ready for space flight the concerns regarding device stability need to be addressed, these concerns include a gain 'ageing' effect, radiation hardness and their susceptibility to single event phenomena.

3.4.1 Technology Readiness Level

The Technology Readiness Level (TRL) is a measure of the maturity of technology in preparation for space flight. This measure of technology maturity as described by the European Space Agency (ESA(a) 2012) includes a scale of 9 specifications shown below:

1. Basic principles observed and reported.
2. Technology concept and/or application formulated.
3. Analytical and experimental critical function and/or characteristic proof-of-concept.
4. Component and/or breadboard validation in laboratory environment.
5. Component and/or breadboard validation in relevant environment.
6. System/subsystem model or prototype demonstration in a relevant environment.
7. System prototype demonstration in a space environment.
8. Actual system completed and "Flight qualified" through test and demonstration.
9. Actual system "Flight proven" through successful mission operations.

It is difficult to definitively say exactly where on this scale the EMCCD lies. It is likely to be between the levels of 5 and 6 as the basic principles have been shown and tested. However, due to the ageing and their unknown reaction to Single Event Phenomena it is

unlikely to be higher than 6, despite traditional CCD technology being used extensively on space missions.

3.4.2 Device ageing

EMCCD ageing manifests itself as a continuous un-recoverable decrease in gain for a given avalanche potential (Ingley 2009) (e2V-Technologies 2006). It is of particular concern for the technology's chances of space flight, due to the unknown nature of its cause. This unknown and the instability that it brings to the technology is a great hindrance where space flight is concerned. Additionally, having an imaging device in space where constant recalibration of the gain is required is not ideal. An Automated Test Equipment (ATE) was created under this work to more efficiently and accurately perform life testing experiments in order to fully define the effect. In addition to the characterisation some novel experiments to investigate the cause from the inner-workings of the device were performed (Evagora(a) 2012). The details of these experiments and the results are described in Chapters 5 & 6.

3.4.3 Radiation effects on EMCCD ageing

The effect of gamma ray and proton irradiations were also investigated. Previous work has been done on the radiation hardness of EMCCDs, showing results of increasing dark signal and changes in gain (Smith(b) 2006) however, if the ageing rate or extent is severely affected by radiation then this again could be of concern. Several EMCCDs were irradiated and the effect upon the ageing observed. The results of this are again described in Chapter 7.

3.4.4 EMCCDs and Single Event Phenomena

Another aspect of EMCCD technology which needs to be considered for use in space is their potential vulnerability to Single Event Phenomena. This is of particular concern

when considering the high voltage phase; even a small chance of catastrophic failure caused by an interaction between a heavy ion and the high voltage phase will cause potential space missions to continue to reject these devices. This work describes a complete investigation undertaken to model, simulate and finally test the EMCCD in a harsh heavy ion environment. Results of this work are described in Chapter 8.

3.5 Conclusion

Described here is the theory behind the well-established method of increasing the signal to noise ratio of an image device using signal multiplication in the charge domain. The method of increase is via impact ionisation, which is reasonably well documented, however, the literature does not give a clear and simple model. This chapter attempts to bring together and provide, to a certain degree, a clear explanation of impact ionisation. What is known, however, is that this method of multiplication used in conjunction with a CCD has yielded improvements in sensitivity, thereby opening up the possibility of a wider range of scientific imaging applications and potentially new discoveries. The aim of the research in this thesis is to improve the TRL of these devices in regards to space flight.

Chapter 4: Methods and equipment

The main aim of this research is to determine the reliability of EMCCD image sensors for space applications, and specifically raising the TRL by investigating of the risks of ageing, heavy ion damage and radiation degradation. This chapter reviews the practical methods and techniques that were used and developed for this work. The mechanical, electrical, thermal and vacuum aspects of the work performed will be discussed, followed by an overview of the overall camera system. Additionally, following on from Chapter 2 and 3 some analysis and noise reduction techniques alongside some measurements with EMCCDs will be discussed.

4.1 System setup

The mechanical and thermal design is one of the initial challenges faced when planning a specific experiment. Within the Centre for Electronic Imaging (CEI) there are standard experimental facilities that can accommodate a large number of experiments. However, some research objectives, like the EMCCD ageing investigation, require original designs.

4.1.1 Standard vacuum chamber

The design of the standard chamber consists of a 200 mm cylinder shaped chamber with two detachable flanges and two smaller 25mm and 16mm feed-throughs. Figure 4-1 shows one of these chambers, the two feed-throughs are used for any additions that may be required for that particular experiment, including vacuum systems, X-ray sources, electrical feed-throughs and pressure gauges. Each standard chamber flange also includes three vacuum electrical feed-throughs which carry temperature information, camera clocks, biases, inputs and outputs. Additionally, there is also a Conflat flange on the top of

each chamber which is ordinarily closed off, but can be used with a rotatable flange for the mounting of X-ray fluorescence targets or an Fe^{55} source.

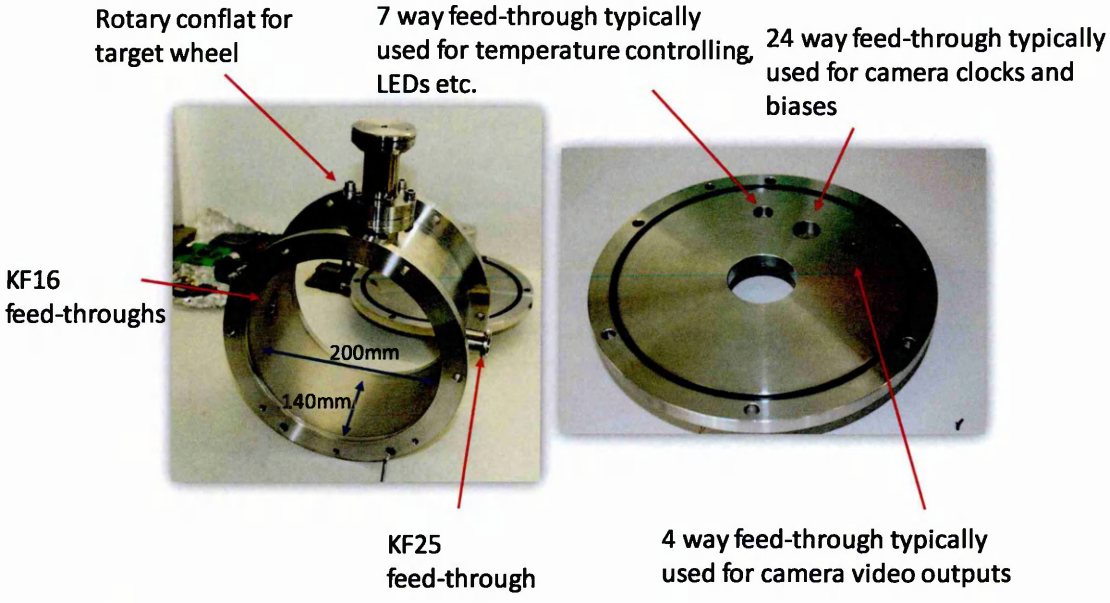


Figure 4-1. Standard vaccum chamber (left) and detachable flange with feed-through holes and o-ring (right).

4.1.2 EMCCD ageing test chamber

Although the standard vacuum chamber setup is designed to accommodate a wide range of experimental procedures, occasionally a custom piece of metal-work is required in order to run a particular experiment. The original aim of the EMCCD ageing investigation was to operate the devices for long periods of time and characterise both the short-term and long-term effects. Cooling is ordinarily provided by a Thermo Electric Cooler (TEC) or a CryoTiger, however the expense of the CryoTiger and the low cooling capacity of the TEC prompted the exploration of an alternative, the Free Piston Stirling Cooler (FPSC). This long-term experiment provided an excellent opportunity for preliminary reliability tests of the FPSC. The addition of the FPSC into the experiment meant however, that new metal-work was required, as this was the first time an FPSC was used with this vacuum chamber. A comparison of the different cooling methods is given in the next sub-section.

4.1.2.1 Cooling methods

The chosen method of cooling for any given experiment largely depends on the temperature requirement and the convenience of utilising that type of cooling. For example, if the experiment is executed overseas then transporting a CryoTiger unit of >30kg may be problematic therefore a compromise may be necessary; cooling capacity for convenience. Whist the TEC is cheaper and more portable low temperatures of approximately -50°C can only be achieved with additional water cooling.

As mentioned previously the types of cooling used within the CEI are; the CryoTiger, TECs and more recently the FPSC. The TEC is the most versatile of the three and easily implemented into the system (with no flange customisation required) and can cool down to approximately between 5°C - 0°C without any additional heat removal. If water or forced air cooling is used to remove heat from the back-side of the TEC, then temperatures in the order of -30°C to -40°C may be achieved. While the large cooling capacity of the CryoTiger makes it ideal for low temperature experiments, (approximately -130°C) the size and weight of the compressor does not allow easy manoeuvrability. Additionally the CryoTiger is the most expensive of the three and requires servicing and fluid top-ups. The FPSC offers a midway point between the TEC and CryoTiger as temperatures of -120°C may be reached, if the cooler is properly coupled and with minimal load; additionally it is easily transportable as weight and size are not a great concern (approximately 3kg). The difficulty with the FPSC is the mounting as it requires a custom flange and is not easily made compatible with other systems although the same applies to the CryoTiger. Table 4-1 gives a brief summary of the different coolers.

Technology	Base Temperature	Weight	Cost (£)
TEC* (2 stage)	-50^{0}C	<1kg	~1500
FPSC	-120^{0}C	~3kg	~1000
CryoTiger	-130^{0}C	>30kg	~10,000

*Requires water supply

Table 4-1. Main types of coolers utilised within the CEI.

4.1.2.2 Free Piston Stirling Cooler

The FPSC utilises the Stirling Cycle, an article written by Thombare provides a detailed description on its workings (Thombare 2008).

It was identified that only the end of the snout reached sub-zero temperatures, as seen by Figure 4-2; this became particularly important when the new flanges were designed as described later.

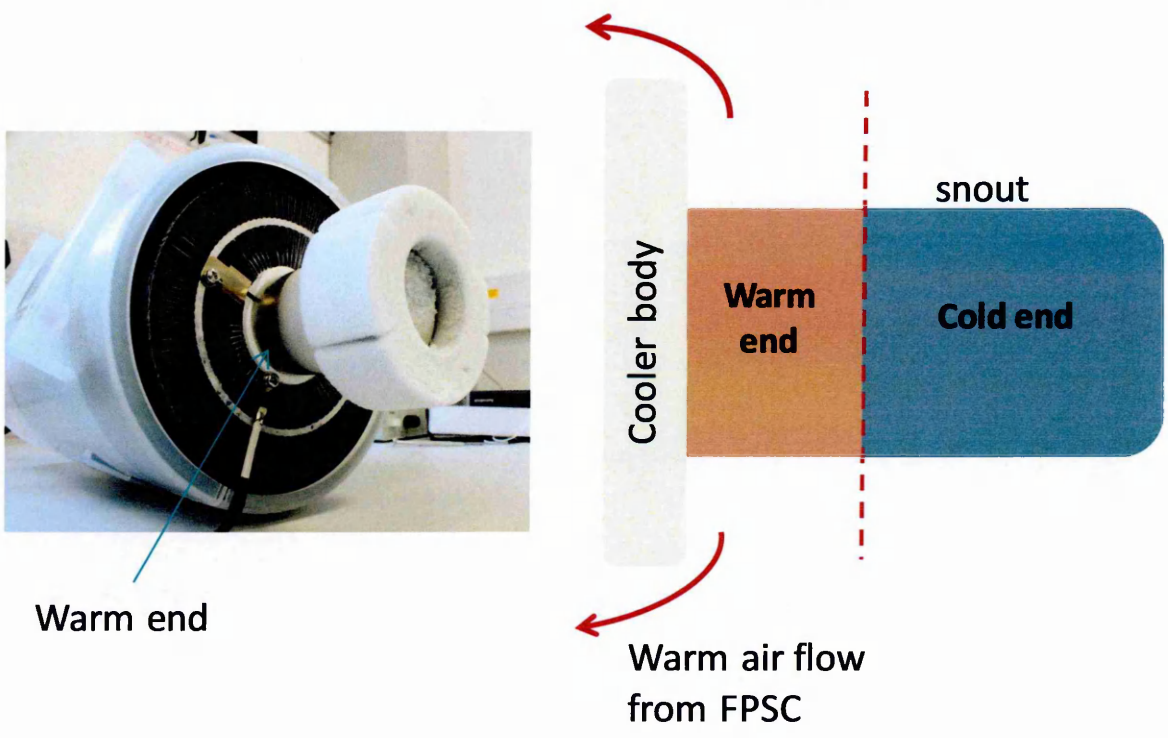


Figure 4-2. FPSC portraying that only the end of the snout reaches sub-zero temperatures as demontrated by ice formation.

This particular cooler consisted of the main cooler body and an external interface board. The reported maximum power rating was approximately 200W running at 8 amps with 25V applied. However in reality the current drawn by the cooler never exceeded 4 amps giving a power rating of 100W.

4.1.2.3 Mechanical designs

A re-designed front flange was needed to accommodate the FPSC, but still be compatible with the standard chamber. The initial design shown in Figure 4-3 consisted of an external copper housing for the snout, this copper then formed a vacuum seal with the outside of the new flange. It became clear after the initial tests however, that this design was impractical, as the cold regions although insulated, were effectively in contact with the external environment resulting in ice formation on the external parts of the chamber as shown in Figure 4-4.

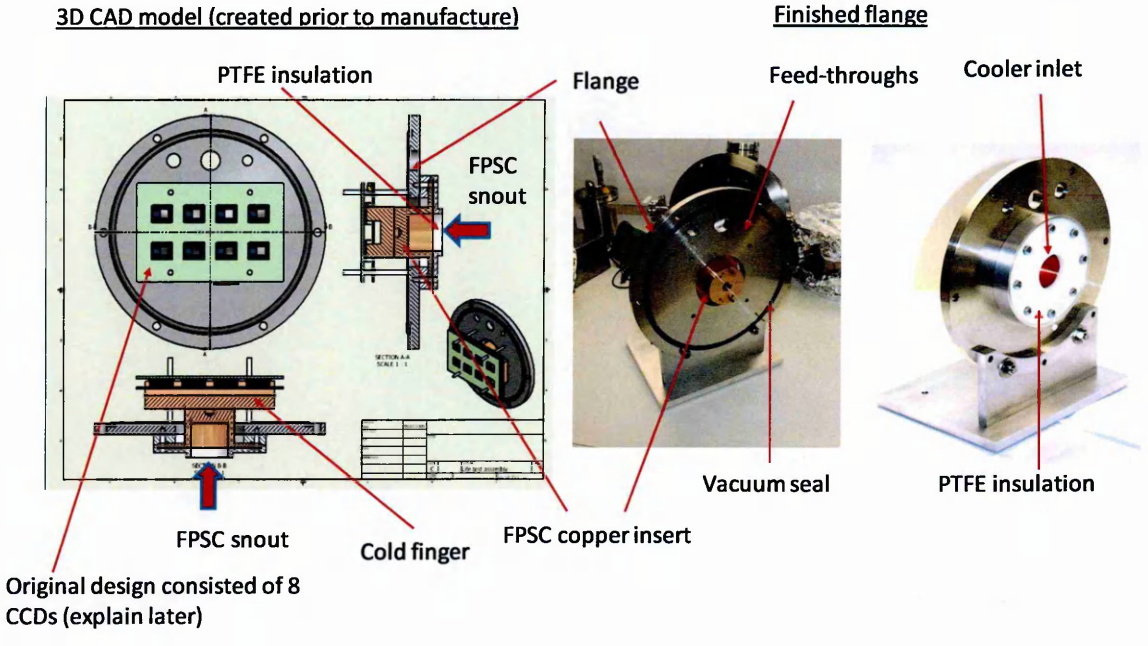


Figure 4-3. CAD designs (left) and finished manufactured product (right) for the initial flange.

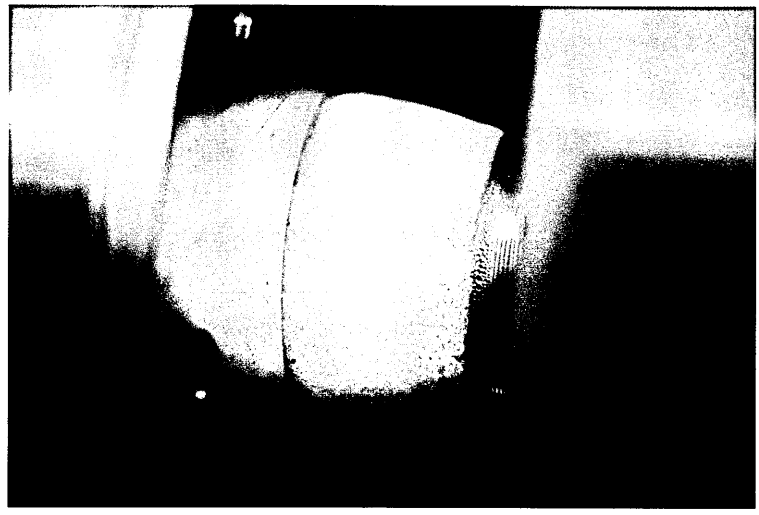


Figure 4-4. Initial flange showing poor thermal isolation and ice formation on the external regions of the vaccum chamber.

This first design was an oversight and it became clear that further thought was required in order to correctly use the FPSC. The mechanical design of a system ultimately affects its thermal characteristics. The cold regions of the first mechanical design were directly coupled to the outside environment; this meant that heat was transferred to the system through both conduction and radiation. This resulted in poor cooling efficiency with the full potential of the FPSC not utilised. Figure 4-5 shows a temperature curve for this initial design, a 5W input was added after 2 hours into the cooling time. Multiple sensors were used in order to see whether a temperature gradient existed across the copper cold finger.

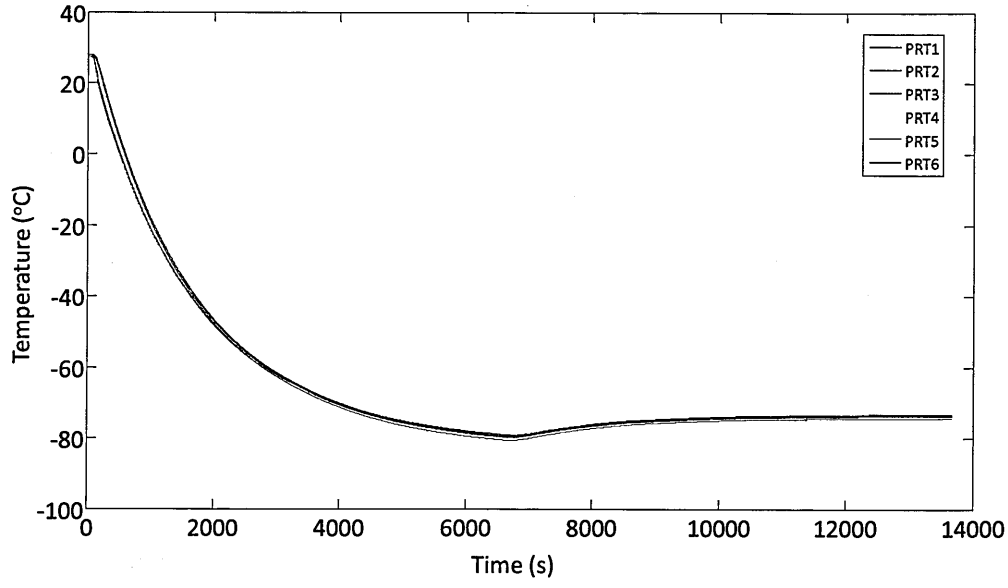


Figure 4-5. Cooling curve for the FPSC using the first flange design. Six PRT sensors were used in order to identify any significant thermal gradients across the copper cold end, none were found.

To progress the main experiment a second generation interface flange was designed. The challenge was to thermally isolate the cold end of the cooler but maintain all the electronics and the FPSC body outside the vacuum, whilst providing a good vacuum seal. The final design comprised of a precisely designed inlet on the main flange in which the snout was inserted, then a sealing O-ring clamping onto the cylinder of the snout itself. The vacuum seal was therefore obtained against the warm end of the snout, which meant that the cooler was now a part of the structure of the sealed chamber and could not be removed without warming and venting the chamber. The FPSC snout has a large temperature gradient across it, previously mentioned in Figure 4-2, allowing for the warmest region closest to the cooler body to make contact with the chamber and O-ring without concern. However, space is required to manage the airflow from the cooler so this required significant attention to detail on the exact design.

By having the cold end of the FPSC inside the vacuum chamber the cold section was successfully isolated. Mounting the copper cold-end to the external flange was still

necessary but, by using nylon studs for support it was possible to effectively eliminate heat exchange via conduction.

Figure 4-6 shows this design. Both this, and the first generation design were completed in the Autodesk Inventor CAD package (Autodesk 2012). Figure 4-7 is the final manufactured flange.

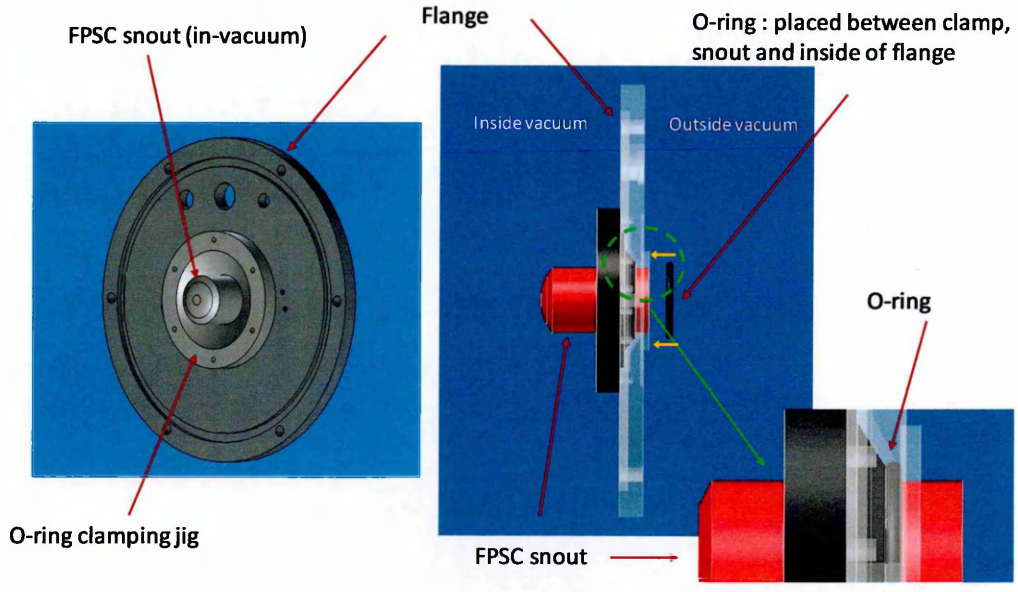


Figure 4-6. CAD designs of the second flange design showing the method of thermally isolating the FPSC.

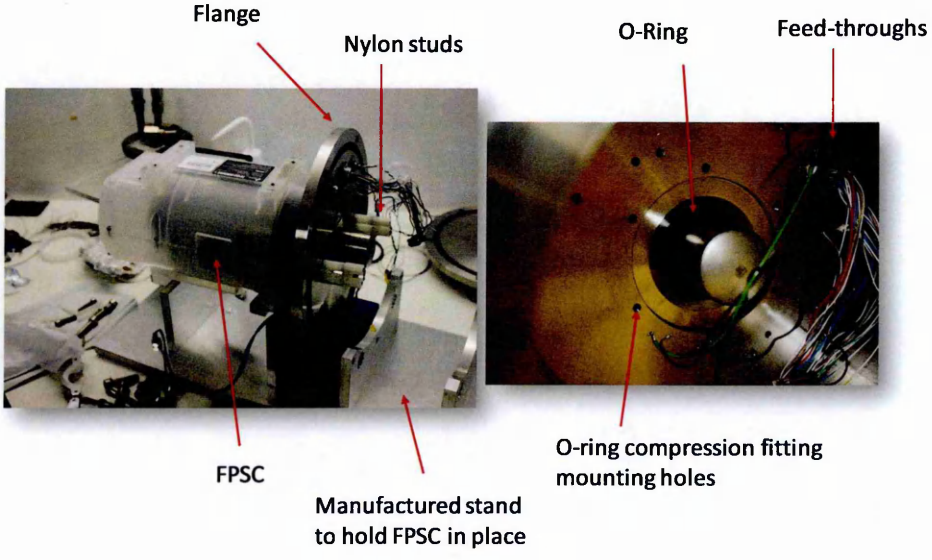


Figure 4-7. Manufactured flange showing how the FPSC is attached and becomes an integral part of the vaccum system.

Figure 4-8 shows the cooling curve for the new design; unlike the test procedure for the first design only a single PRT was used as the results from the first test showed that a gradient across the finger did not occur.

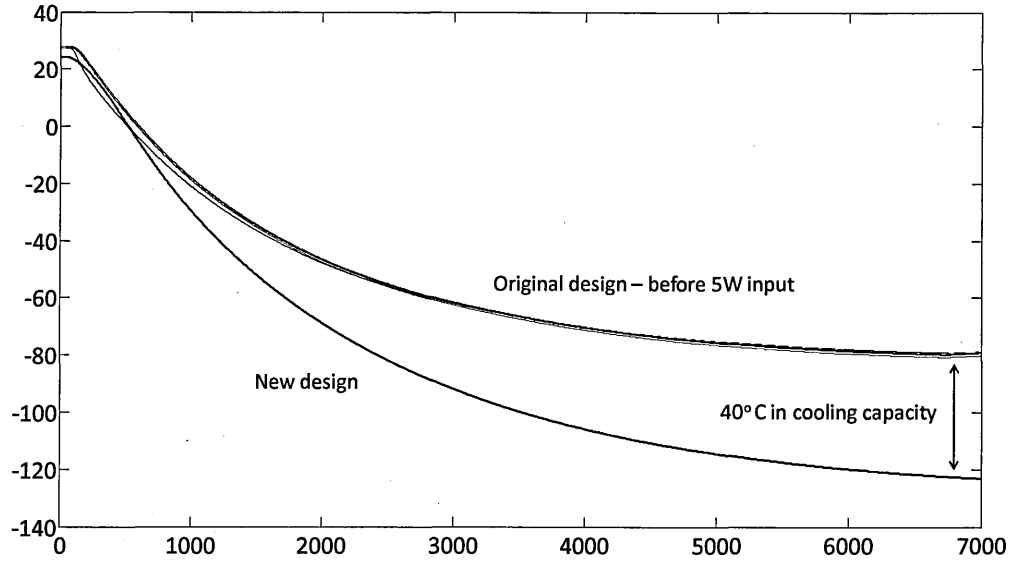


Figure 4-8. Cooling curve for the FPSC using the second flange. A single PRT sensor was used this time as no significant thermal gradients were observed in the previous setup.

A much lower temperature was obtained using the second generation design, -120°C, as compared with -80° C of the first design, a temperature difference of approximately 40° C. For this run however, instead of introducing a 5W load, which seemed excessive, a more appropriate input of a CCD97 was introduced from the start of the cooling, emitting approximately 250mW.

In addition to the experiment on EMCCD ageing this setup was also used with the pre and post characterisation of devices used in the irradiation and single-event study.

4.2 Vacuum

Vacuums are an essential part of any scientific imaging system wishing to image incoming radiation or cool devices. If the system is properly designed, vacuums allow for operation at cryogenic temperatures without the consequence of condensation which can lead to device failure. Therefore it is important to maintain good vacuum practice, such as cleaning and oil and grease contamination, when working at low temperatures and one must always warm the system before venting to atmosphere to avoid condensation. Figure 4-9 shows the phase diagram of water, ice and steam; this provides the minimum pressure required to operate a cryogenic camera system without the risk of condensation. The minimum pressure for any cooled (-70°C) CEI camera system is 10^{-3}mbar, however, to avoid condensation at temperatures of -100° C (173K), 10^{-5}mbar is required.

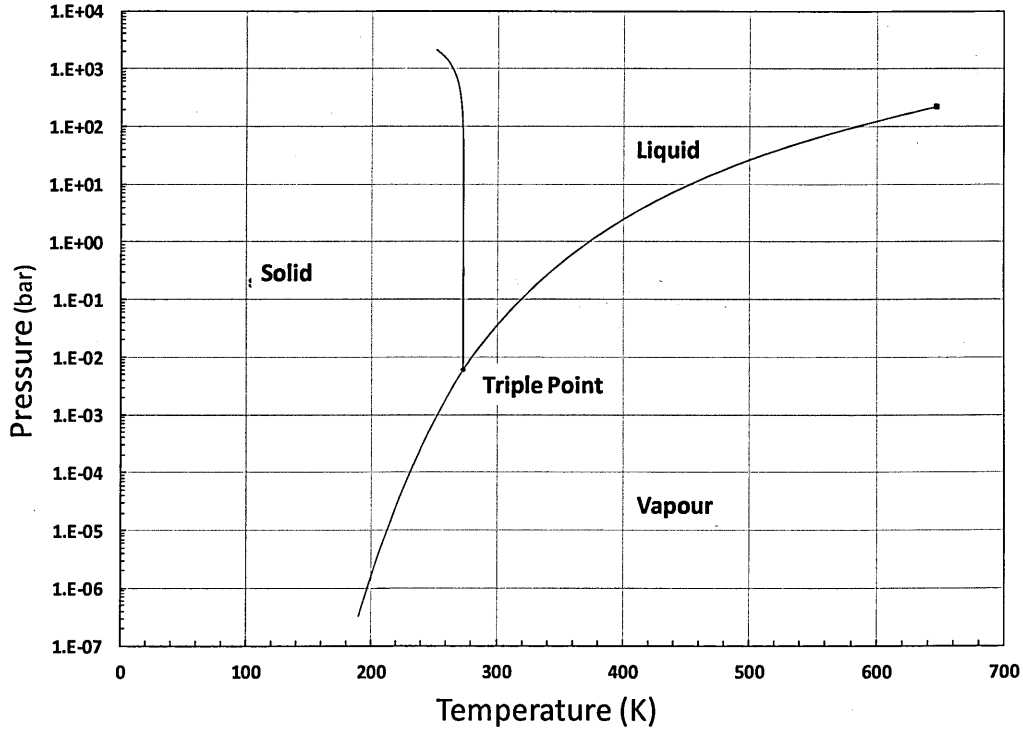


Figure 4-9. Tripple point of water showing the required pressures to ensure condensation does not occur (ChemicaLogic 2012).

4.2.1 Standard Vacuum System

The standard vacuum setup is comprised of a dry Pfeiffer unit including a diaphragm pump (roughing pump) and a turbo. The diaphragm pump initially pumps down to approximately $10^{-1} - 10^{-2}$ mbar, at this pressure the system transfers from the viscous flow regime to the molecular flow. The turbo is able to 'spin-up', due to a decrease in air resistance, which takes the pressure down further to 10^{-4}mbar – 10^{-7}mbar, depending on the quality of the seals, the cleanliness of the chamber and whether or not a cryogenic cooler is active. When a cooler is active within a vacuum chamber, the cold regions act as a cold-trap, which act to Cryo-pump the dominant water vapour components, decreasing the pressure of the system. It is therefore important that the CCD is not the coldest entity within the chamber as this can result in contamination. Either a designated cold-trap should be used or it should be arranged that any condensation takes place preferentially on the cold finger that the CCD is attached to.

4.3 Electronics

Unlike the mechanical aspects where a standard piece of equipment can be used for a number of experiments with different devices and objectives, each new detector requires a new set of electronics and head-board. A head-board is an electric board, whether a Printed Circuit Board (PCB) or otherwise, in which the detector is mounted. However, there are some standard features that each head-board requires in order to operate a CCD.

4.3.1 Standard circuitry

Each head-board designed to run a CCD must include the appropriate sockets for that particular device type, low pass Resistor-Capacitor (RC) filters for the bias lines and operational amplifiers connected to the output source of each device. The reasons for the

filters and amplifiers will be explored in a later section of this chapter. Each head-board is designed to suit an experiment and good planning is vital to ensure that everything required is present on the board. Figure 4-10 shows a simple EMCCD head-board, like most boards it includes filters and amplifiers, however, EMCCD head-boards must also include a high voltage circuit to control the voltages applied to the avalanche phase within the gain register. An external PSU is required to power the avalanche phase as the standard XCAM drive box (described later) is not designed to output the high potentials required.

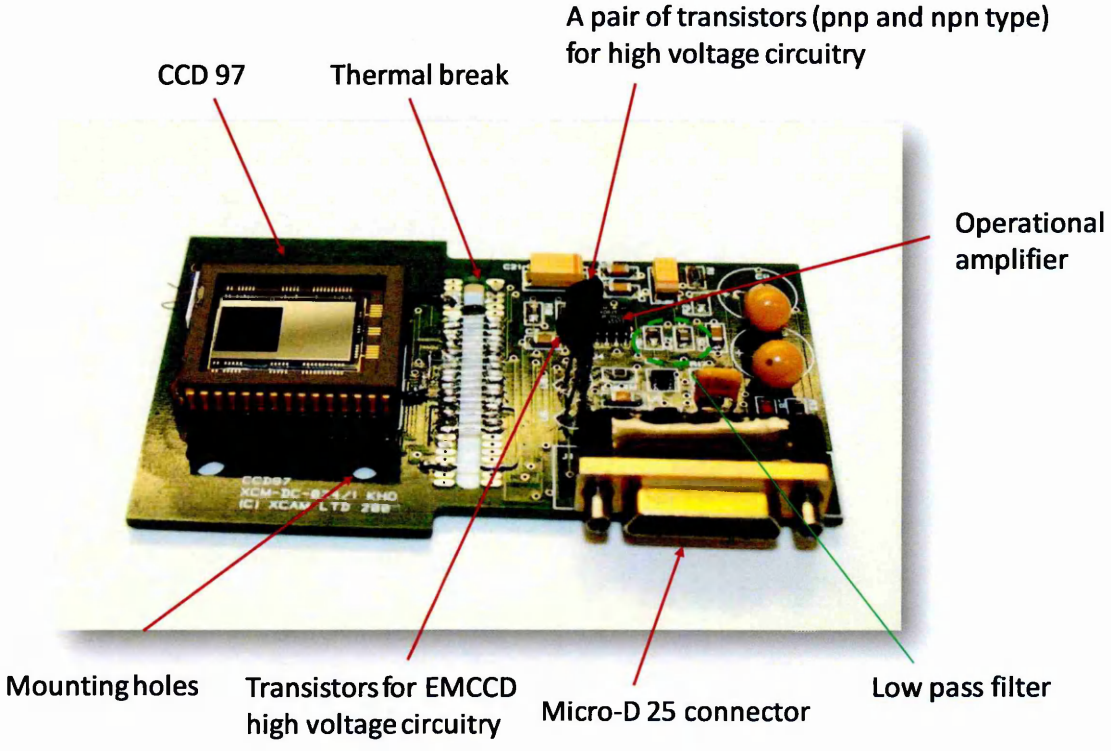


Figure 4-10. EMCCD head-board with a CCD97 attached.

4.3.2 EMCCD ageing study head-board design

The initial plan for the EMCCD ageing investigation was to design a head-board that can accommodate up to 8 EMCCDs running simultaneously with a variety of operating conditions. This was done in order to get a direct comparison between the operating conditions in order to identify ageing dependencies. A head-board was designed with all

the standards parts described above, including the filters, amplifiers and high voltage circuits. However, as there were 8 devices running on one head-board, it also required a switching mechanism in order to switch between outputs of the different CCDs. On-board temperature monitoring was also included. Figure 4-11 shows the designed circuit diagram alongside the finished PCB under this work.

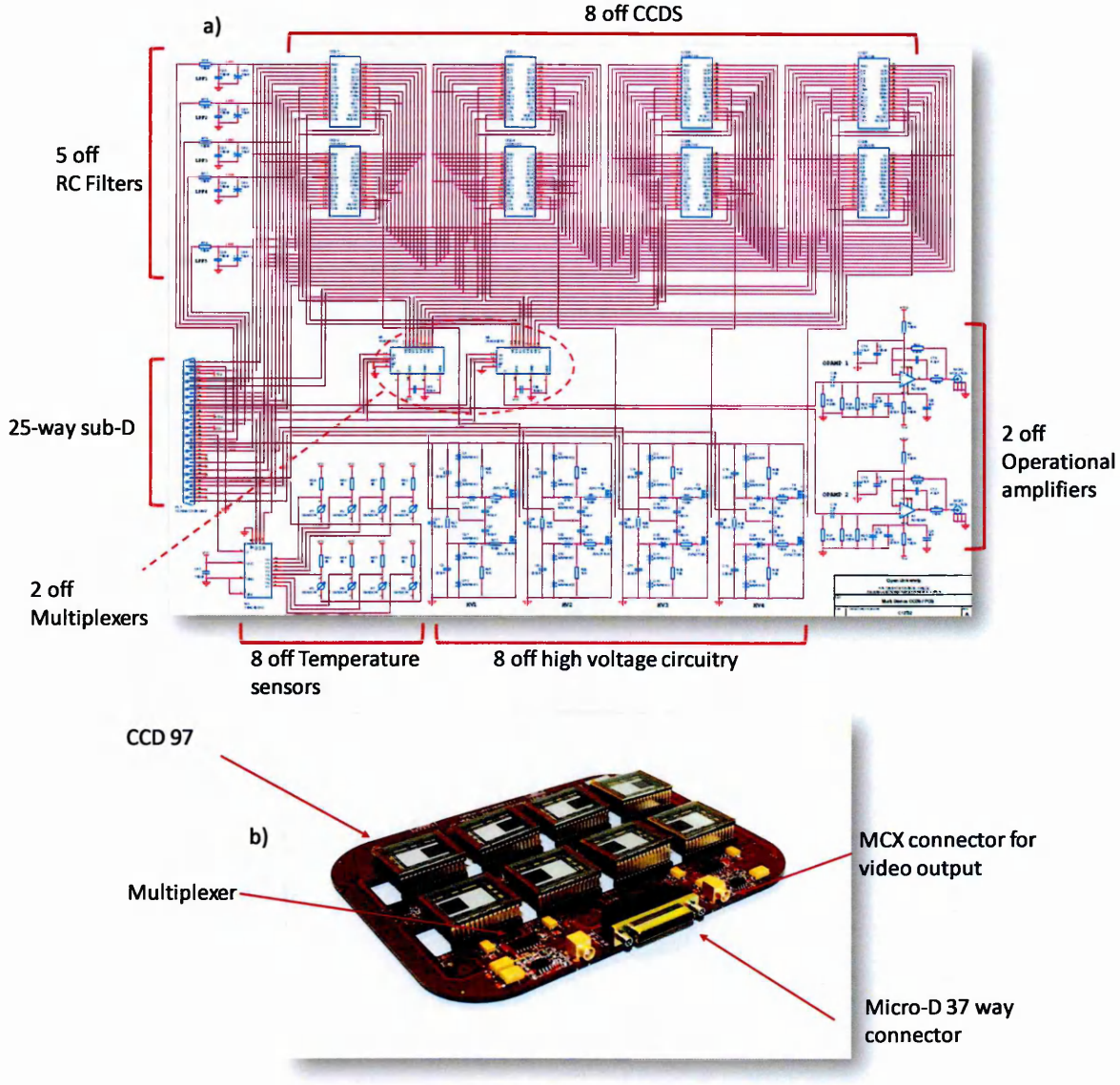


Figure 4-11. a),Schematic, and b), finished manufactured head-board, for the 8-device EMCCD head-board.

Despite the completion of this head-board, on-going work at the time suggested that it was more appropriate to undertake some smaller, more-focused tests on single devices

first in order to provide some experience in EMCCD life-testing and to gain a better understanding of the ageing effects before 8 devices were committed. As a result of this it was found that results sufficient for this research project could be obtained with a simpler single board arrangement. It was therefore decided to not continue with the more-complex 8 device experiment but to leave this for future work; building on the data gained from the more-focused results using the single device head-board shown in Figure 4-10. Although not directly used, the design and development of the head-board in Figure 4-11 provided a good learning experience. This, alongside the design of the chamber, provided an understanding of how all aspects of a camera system fit together and the experience of creating an entire experimental test system from the beginning.

4.4 Camera System

The mechanical, electrical, thermal and vacuum features described above all form a vital part of any cryogenic camera system. At the heart of the CEI system however, is the electronic drive system, manufactured by XCAM (XCAM 2012), which provides the clocks, biases, performs CDS and provides a Graphical User Interface (GUI) for easy running of the device.

4.4.1 XCAM drive system

The XCAM drive system provides a full set of control waveforms and the external video processing electronics. The drive system is readily accessible allowing for easy modifications of the output clocks and biases which are directed to the head-board via a 25-way D-type connector. The video output of the CCD is generally sent to the box via a coaxial cable, and once the CDS is complete the data is transferred via USB to a PC where the GUI displays the information. It is also possible to operate the box using other software packages that can replace the XCAM GUI; one regularly used is MatLab. For this

research an Automated Test Equipment (ATE) was developed, in MatLab, providing an efficient testing environment for EMCCD ageing. This environment proved to be very successful in running ageing and other experiments. More detail on the ATE will be described in Chapter 5. Despite what software is used, a series of files are required in order to run a device; a voltage file to specify the required voltages on the bias and clock lines, delay file to indicate any necessary pauses and most importantly, a sequence file to provide the clock timing information.

4.4.1.1 Clock sequence generation

The sequence file is created to generate the clocking events that enable the CCD to operate. It is written in assembler code and consists of a series of nested loops which are executed by a Digital Signal Processor (DSP). Once complied, a Dalvik Executable (DEX) file is created which is used by the sequencer to drive the CCD. Throughout this research a number of custom sequencer programs were created, allowing for custom experiments to be carried out. The exact modifications made to the sequence files will be described in greater detail in their respective results chapters.

4.5 Testing Techniques

The following sections will describe some general analysis techniques alongside methods to determine and increase the noise performance of a CCD. Additionally some results concerning EMCCDs will also be described.

4.5.1 Analysis Methods

4.5.1.1 Noise calibration

There are several methods available for determining device noise. The photon transfer curve (Janesick(b) 2007) is generally used with optical inputs but is somewhat complicated to set up and interpret. A simpler method is the X-ray spectrum technique,

where the device is placed near a radioactive source of known photon energy, E_p, usually an Fe^{55} source producing Mn-Kα (5.898 MeV). Knowing the peak signal from the photon interaction, it is then possible to calibrate the noise in either electrons or equivalent energy.

The output of the CCD can be represented as a histogram as shown in Figure 4-12. The background signal, a), and the known energy, b), from the Gaussian peaks are identified and their location and the standard deviation, σ determined. The background is set to 0 eV and the known energy is then divided by the number of analogue to digital units (ADUs) between the two giving an energy conversion, eV/ADU. The generated σ (in ADU) for the background peak is then multiplied by the conversion scale to give the noise value in eV. To present this as a noise signal in electrons the signal in eV is divided by the quantum yield for silicon; 3.68eV, per e-h pair (Geist(a) 1979). This calibration can then be used for other signals that may be present, but needs to be repeated each time the device, temperature or setup is changed. This simple measurement can be performed with only a single frame.

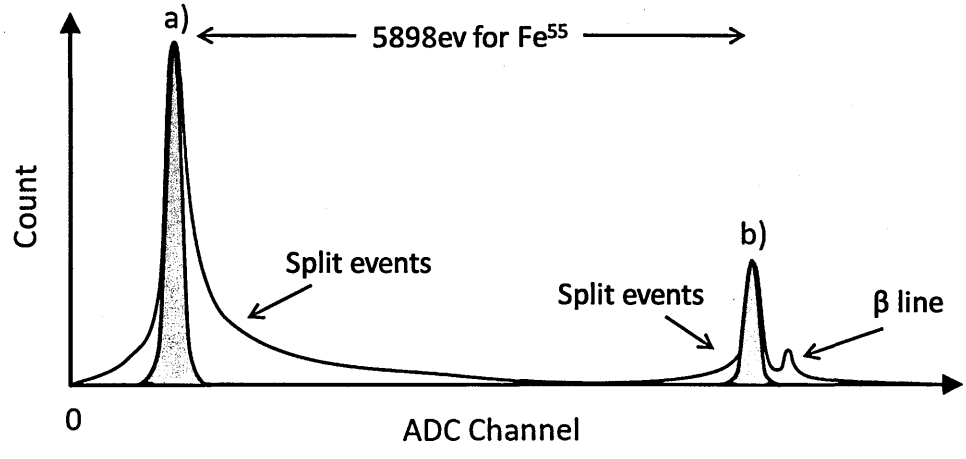


Figure 4-12. Histogram pf a typical CCD output when imgaging X-rays.

4.5.1.2 Under/Over-scan

A number of analysis techniques can be performed by using under-scan and/or over-scan elements. The number of rows and columns entered into the XCAM GUI are forwarded to the sequencer, alternatively these can also be hard coded into the sequence file. The rows and column parameter are then 'called' in the sequencer which performs a row-loop or column-loop the requested amount of times.

As illustrated in Figure 4-13, under-scan is produced by register elements on the device that do not have a corresponding image pixel from which to receive charge. The read-out register extends a few elements beyond the image area and can range from 5 – 50 elements towards the output node; they are present so the FET structure can be fabricated without impact to the image area. To obtain a full image including these elements the full number of columns (image area + under-scan elements) needs to be coded for, or entered into the GUI. Additionally, over-scan is created at the end of the read-out register by simply calling for additional column elements that do not physically exist. The device will still perform the transfer procedure but no charge integrated in the image will be detected, yielding 'serial over-scan'. Furthermore increasing the number of rows beyond the physical amount will yield 'parallel over-scan' which originates from the top of the image section.

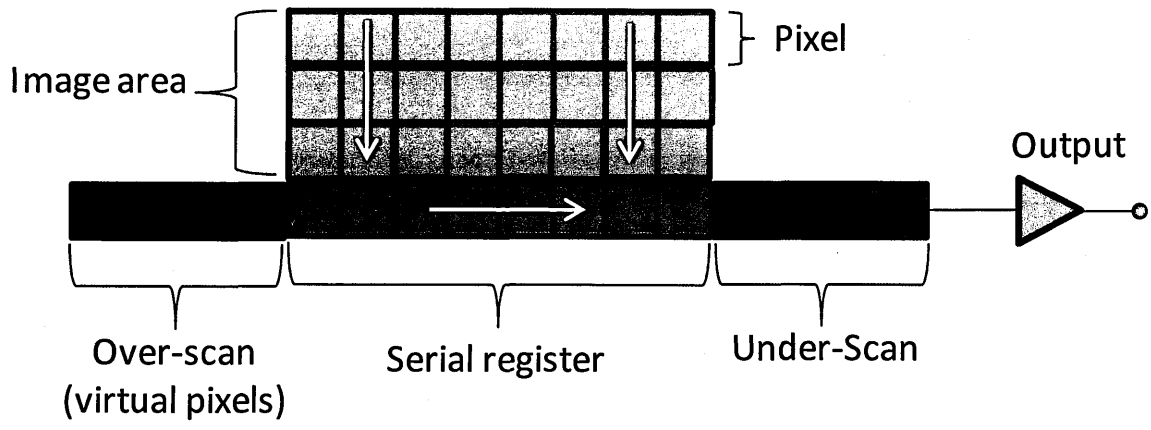


Figure 4-13. Origins of the different under/over-scan elements.

Since they capture no image signal, the over-scan regions can be used as a 'zero' level for calibration purposes as they only contain dark current accumulated during the read-out process. The speed at which the serial register transfers charge means that the dark signal generated during read-out is insignificant compared to the integrated signal and can therefore be used a 'zero' signal reference level. Parallel over-scan however from the image area spends more time within the device resulting in higher dark signals, and therefore cannot be used in this manner. Serial over-scan can be used to calculate EMCCD gain (described in a later chapter). Additionally, it can be used to calculate CTE as deferred charge will be swept up by these trailing elements, it is therefore important to not include the first few over-scan pixels in a zero-reference measurement.

4.5.2 Noise reduction techniques

Described below are some of the many techniques used to decrease the characteristic noise on a CCD leading to improvements in performance.

4.5.2.1 Correlated double sampling

Correlated Double Sampling or CDS is used to eliminate the kTC reset noise; described in Chapter 2, with an ultimate goal of improving the signal to noise ratio of the system (White 1974). This is performed in the post-CCD video processing circuitry. The output waveform is firstly sampled after resetting and then again with signal present. Subtracting the first sample from the second eliminates the common reset voltage level. Figure 4-14 shows the output of a single pixel and the timing of the sampling regions. The region can be integrated for a long period of time in order to obtain a good average of values. The time taken for the sampling is known as CDS integration time.

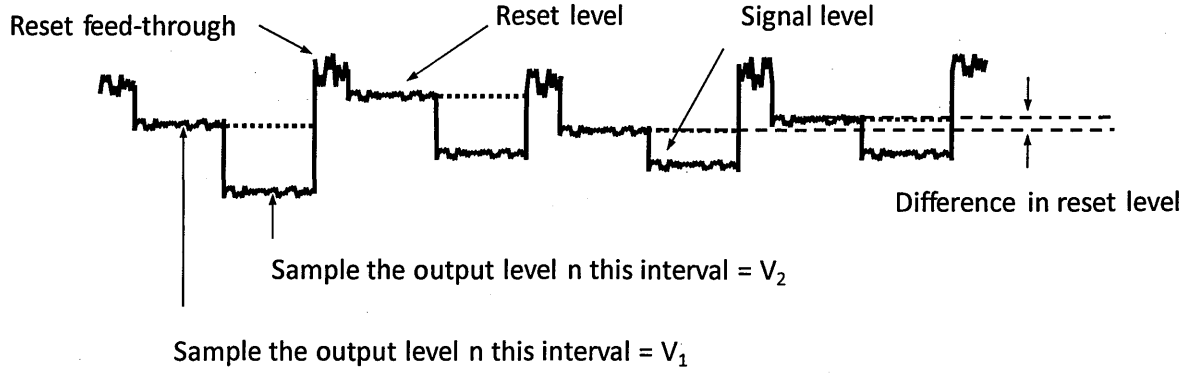


Figure 4-14. The samples taken before, V_1, and after, V_2 the charge is transferred to the output node are subtracted to isolate any noise created from resetting the node.

A common practical arrangement to perform the above is the 'clamp-and-sample' circuit, as shown schematically in Figure 4-15. The CCD is followed by a voltage amplifier, then a coupling capacitor and sampling switch, and finally an Analogue to Digital Converter (ADC). In operation, the capacitor is clamped to ground during the reset operation such

that the signal level is now referenced to ground and independent of the reset level. The ACD conversion now gives the signal value in 'Digital Units' (DU).

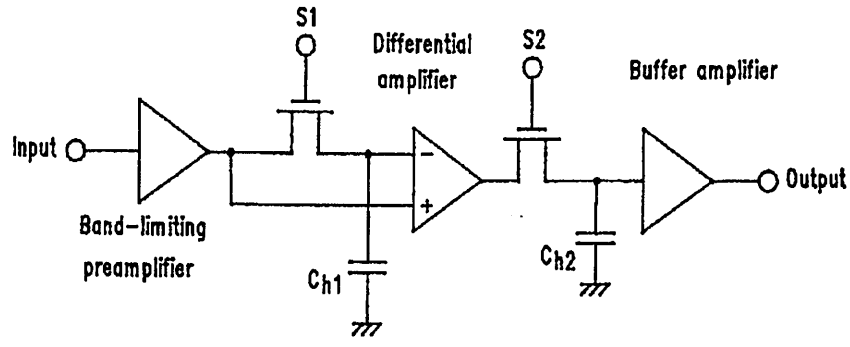


Figure 4-15. Clamp and sample circuitry (Holland(b) 1990).

The capacitor clamping operation introduces additional kTC noise which is not subtracted. In order that this noise is not larger than that from the CCD, it is necessary to include a gain stage between the CCD output and the CDS electronics; this ensures the noise on the CCD dominates the rest of the circuit. This effectively reduces the sampling noise by the magnitude of the gain, as it is applied before you add the kTC noise. An additional method of applying gain which produces similar results is via electron-multiplication in an avalanche gain register; this amplifies the signal without adding read-noise as it is applied earlier in the chain. The equivalent read-noise after this type of gain is the original noise divided by the amount of avalanche gain.

4.5.2.2 Filtering of DC bias lines

A low pass RC filter is an electronic circuit which attenuates signals with frequencies higher than a particular threshold. They are implemented for otherwise noise on bias lines such as Vod would translate directly to the CCD output. They are generally located in the bias lines between the device and PSU and are normally set to a threshold frequency of approximately 70 Hz to cut out any high frequency noise that may originate from the

PSU. This threshold frequency, f_c, is defined by the filter's RC time constant which is equal to the product of the circuit resistance, R, and capacitance, C. (Horowitz and Hill 1989) The frequency can be calculated by:

$$f_c = \frac{1}{2\pi RC} \tag{4.1}$$

A typical RC filter used on a CCD head-board is shown in Figure 4-16 where typical values for the resistance and capacitance are 100 Ω and 22 μF respectively, giving a frequency of 72Hz.

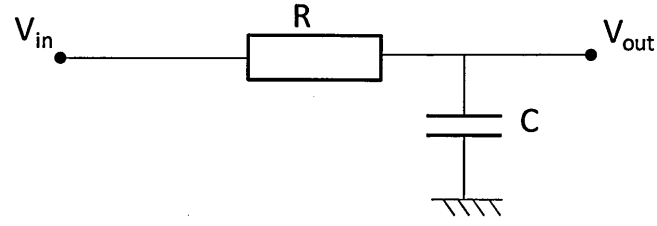


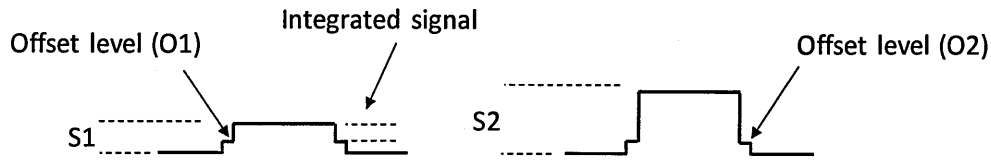
Figure 4-16. Low-pass filter used to reduce high frequency noise on the bias lines of the CCD.

4.5.3 EMCCD testing techniques

There are some testing procedures that are specific to the EMCCD. Detailed below are some results obtained for a) the dependency of temperature and avalanche potential on avalanche gain and b) an overlay of integrated dark signal with register position, following on from Section 1.12 in Chapter 3.

4.5.3.1 EMCCD gain

EMCCD gain is calculated by taking the ratio between the signal with avalanche gain applied and the signal without avalanche gain applied. The offset level created by the read-out process is also subtracted in order to give the true integrated signal, shown schematically by Figure 4-17.



$$G = \frac{(S2 - O2)}{(S1 - O1)}$$

Figure 4-17. Calculation of EMCCD gain.

Practical examples of how EMCCD gain is measured will be described in the respective results chapters.

4.5.4 EMCCD gain temperature dependence

As the temperature of the semiconductor increases the ionisation coefficient which is responsible for impact ionisation decreases. This decrease is due to an increase in lattice scattering via the emission and absorption of phonons. This effect in turn hinders the carriers to gain sufficient energy to ionise bound electrons. Figure 4-18 is a plot to show data gathered on the temperature dependence of avalanche multiplication gain using a CCD97. The same plot also shows how the gain scales with applied voltage, the data here has been fitted with the equations y = Aexp(bx). The data for this plot was taken using the methods what will be described in detail in the following chapter; the errors were calculated from the standard deviation of the mean of 10 measurements for each point.

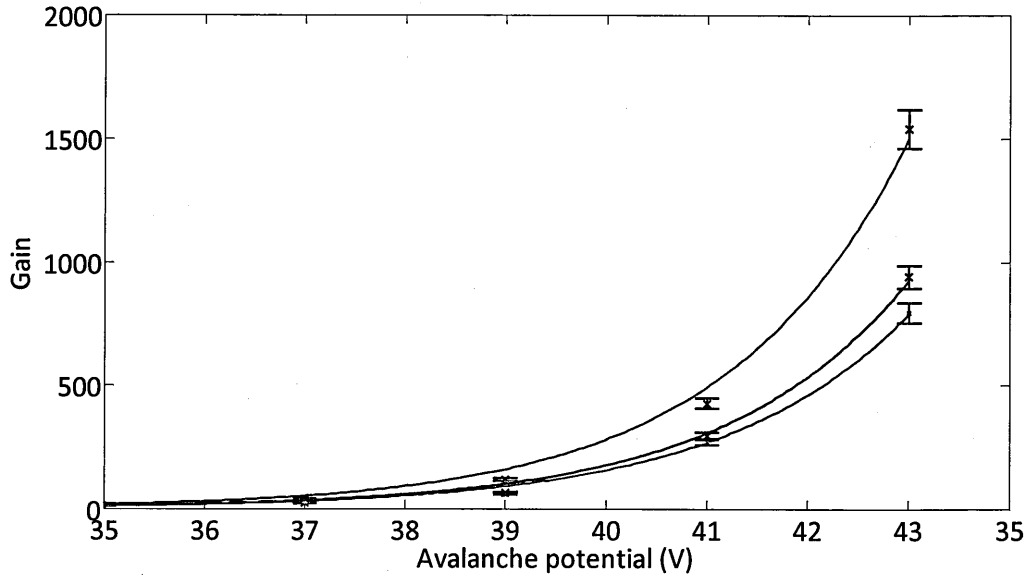


Figure 4-18. Gain measruement taken with CCD97.

4.5.4.1 Register dark signal

During the investigation into EMCCDs an interesting result revealed itself concerning the differences in dark signal generation within the different sections of the serial and avalanche gain registers. The investigation started with a microscope image shown in Chapter 3. Further interest was then generated from the result of actual dark signal generation within the register which seems to nicely match-up the different parts of the register shown in the microscope image and the manufacturer's schematic. However, some anomalies revealed themselves as explained below.

Figure 4-19 shows 1 second of integrated dark current in the serial register and avalanche gain register when run at unity gain (13V). The figure shows how the amounts of generated dark signal match up with a microscope image and the manufacturer's schematic of the device.

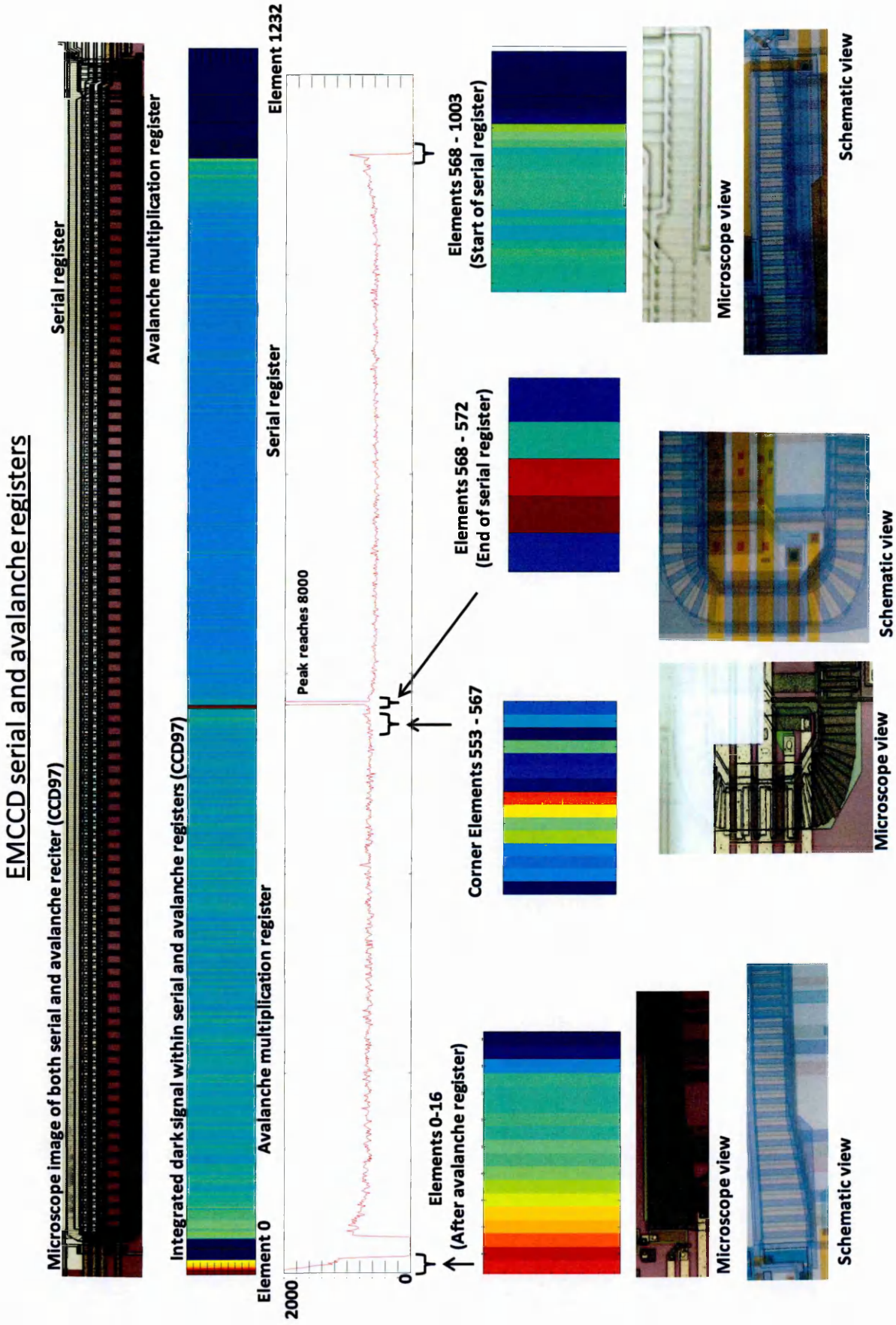


Figure 4-19. Dark signal integrated within the avalanche and serial registers of a CCD97 device.

On the whole, the amount of dark signal generated in the different parts of both registers is consistent with the design areas under the microscope and on the schematic. The larger register elements within the avalanche gain register accumulate more dark signal compared to the smaller serial elements, and the increasing size of the final elements after the avalanche register match up with the locations of increasing signal. However, there are a few anomalies. One of these regions is the last 16 elements of the avalanche gain register where the level of signal drops to that of the offset. This result is consistent throughout the data in this thesis despite using multiple CCD97 devices. It has also been observed by engineers at e2v technologies on their own setups and devices with no real explanation yet to be discovered. Some investigation into the schematics was undertaken in an attempt to see if any physical structure on the device could cause this. Figure 4-20 shows the schematic of this region.

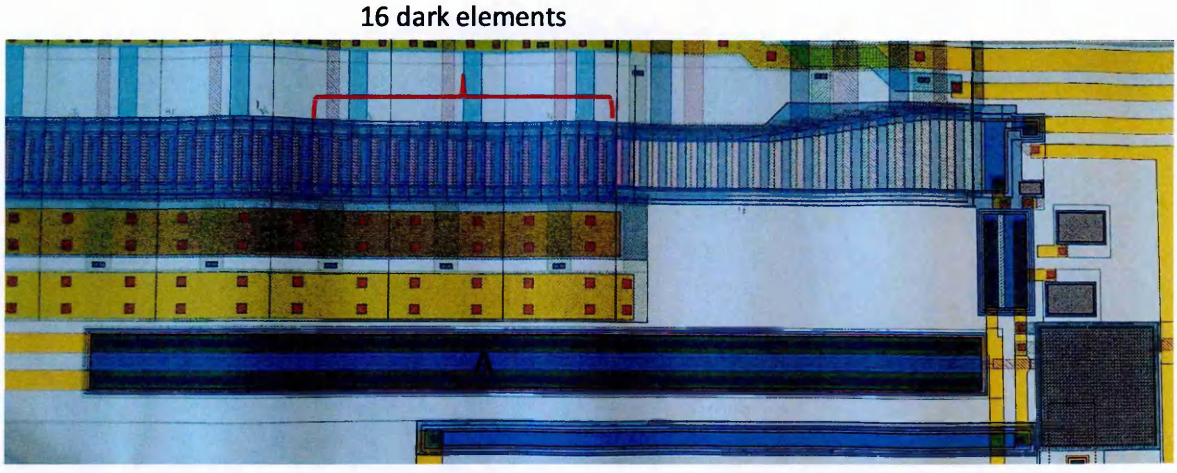


Figure 4-20. Schematic view of the end of the avalanche gain register showing the dark section alongside the 2 stage output.

The closest physical element that may be causing a problem is the 2nd stage FET, labelled A, as it terminates around 12 elements away from where the dark elements end. However, there is no evidence to support this and the fact that it does not affect any other element along its path makes this possibility unlikely. No real solution was found.

Another anomaly that may be seen is the slight increase in signal towards the end of both registers. As you approach the output of the serial register the elements get smaller but the integrated dark signal is seen to increase. Similarly, towards the output of the avalanche register the signal also increases, as mentioned before these elements do get larger, see Figure 4-20, however, the factor by which they increase in size does not match the factor by which they increase in dark signal. This extra charge at the outputs of both registers may be due to a glowing amplifier where photons are given off by the output circuit. The predecessor to the CCD97 was the CCD87 which was discontinued for this reason; perhaps slight glowing is still present newly revealed by the relatively long integration time. Figure 4-21 shows the glowing observed at the end of the gain register. If a closer look is taken at the trace to the right of the diagram, the sections before and after the dark section, mentioned above, look as though they would be continuous If not for the dark section.

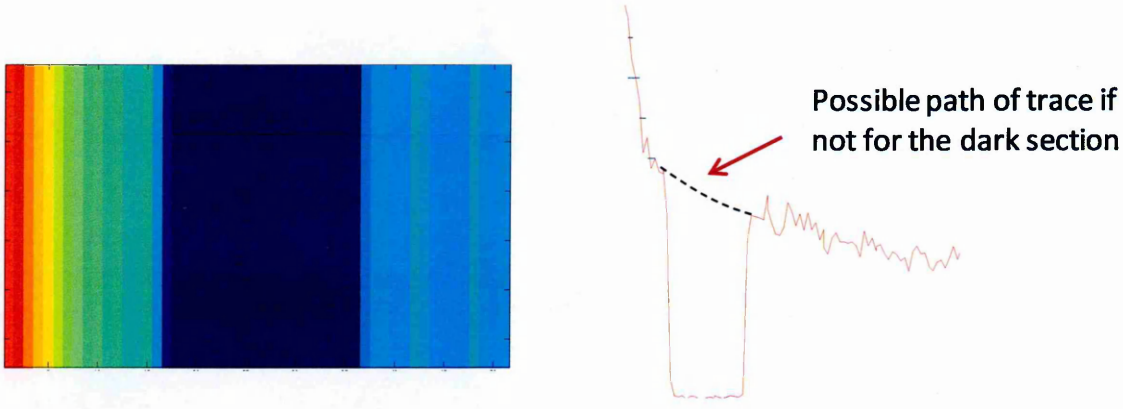


Figure 4-21. Dark signal integrated at the end of the avalanche gain register showing glowing output and dark section.

Finally, the spike in signal observed approximately in the middle of the register is 3 elements wide, believed to be a single bright element with a CTE tail. The original hypothesis was that this was due to the larger, wedge shaped elements found in the corner electrodes, however this result has shown that these 3 elements are in fact the

first three elements of the serial register, before entering the corner section. The origin of this charge is believed to originate from the barrier electrode structure found just above these elements. Figure 4-22 shows the schematic of this region. In the preceding electrode structure there are 4 columns on the side of the image/store sections which act as a shield or barrier from incoming charge from beyond the desired sampling region. This charge is intended to be harmlessly clocked into the drain, labelled 'A'. The fourth column extends a little further beyond the drain and there is a peculiar electrode structure which allows the charge to be transferred diagonally into the drain. An error in transfer from this structure is believed to be the source of the signal found in the three elements shown in the figure.

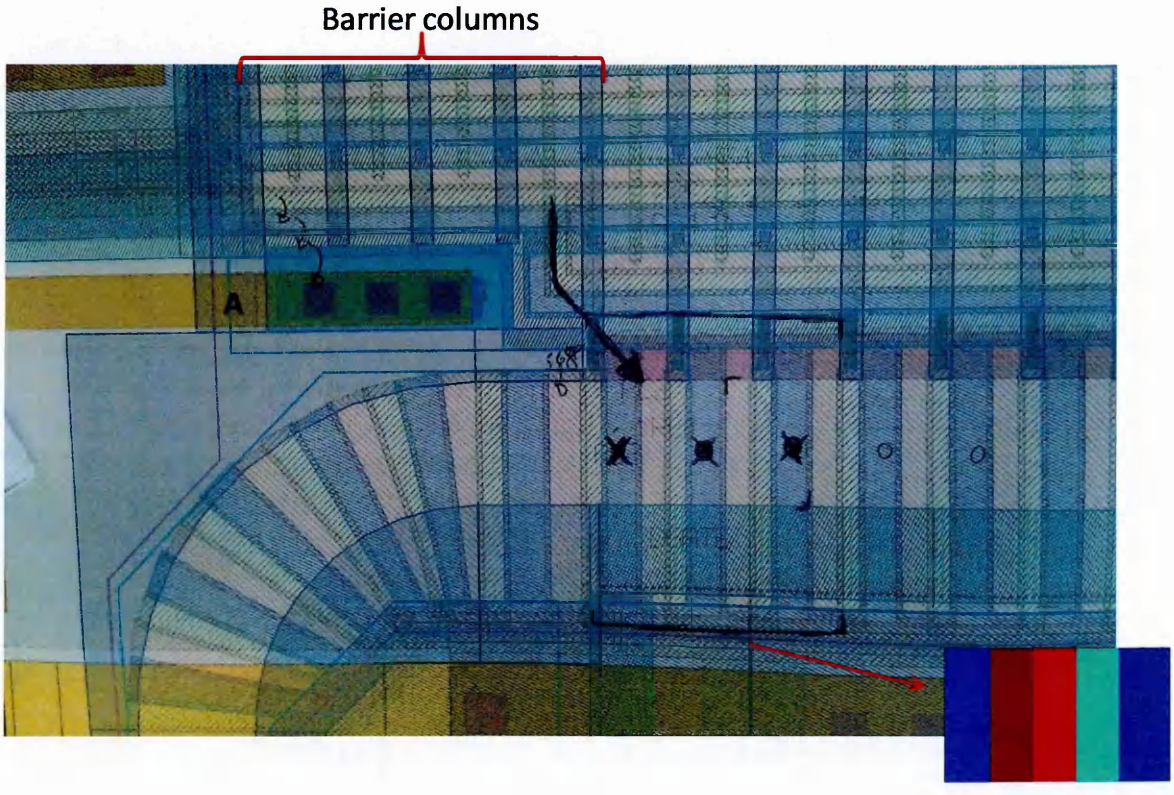


Figure 4-22. Schematic view of the serial register and preceding corner elements, showing the believed source of charge measured in the last three elements.

This type of investigation was found to be of particular interest to the device manufacturer as important, never before seen, device artefacts emerged.

4.6 Conclusion

This chapter reviewed the experimental equipment, setup and methods used in this research project. The mechanical, electrical, thermal and vacuum aspects all hold equal importance within the system; this work has proved a worthwhile experience. The understanding gained while working with all these aspects has provided an insight into what is necessary to create a camera system from the start and for a specific application. In addition to this, the work performed with the EMCCD provided a good platform in developing an understanding for the inner workings of a CCD-type device, and how their physical properties can affect an end result.

Chapter 5: Characterisation of EMCCD ageing

The EMCCD is a CCD image device adopting an on-board avalanche multiplication gain mechanism as described in Chapter 3. For a given avalanche potential EMCCD ageing manifests itself as an unrecoverable decrease in multiplication gain with time. The cause of this phenomenon is currently unknown. This chapter will explain the characteristics of the effect showing various results including some important dependencies. Chapter 6 will then describe research carried out into identifying the cause of the ageing.

5.1 EMCCD ageing

EMCCD ageing is a two stage process. Over the first 24 hours of operation the gain loss is relatively high, thereafter, a slower gain loss is observed extending over the life-time of the device. It is common for EMCCD manufacturers to condition their devices past the initial phase in order to present a more stable device to the customer (Evagora(a) 2012). All devices used in this research on EMCCD ageing are 'unconditioned' devices, which are devices that have not undergone this initial conditioning.

In addition to conditioning, it is common to compensate for the ageing by increasing the voltage applied to the avalanche phase. Figure 5-1 shows the potential increase required to maintain an avalanche gain of ~1000 with an e2v CCD65, which also illustrates the 2 stage process described above. This figure is a model published by e2v technologies in order to demonstrate the ageing effect in their EMCCD ageing program. The figure does not specifically relate to any operating conditions which will affect the end result, however is nicely demonstrates the effect.

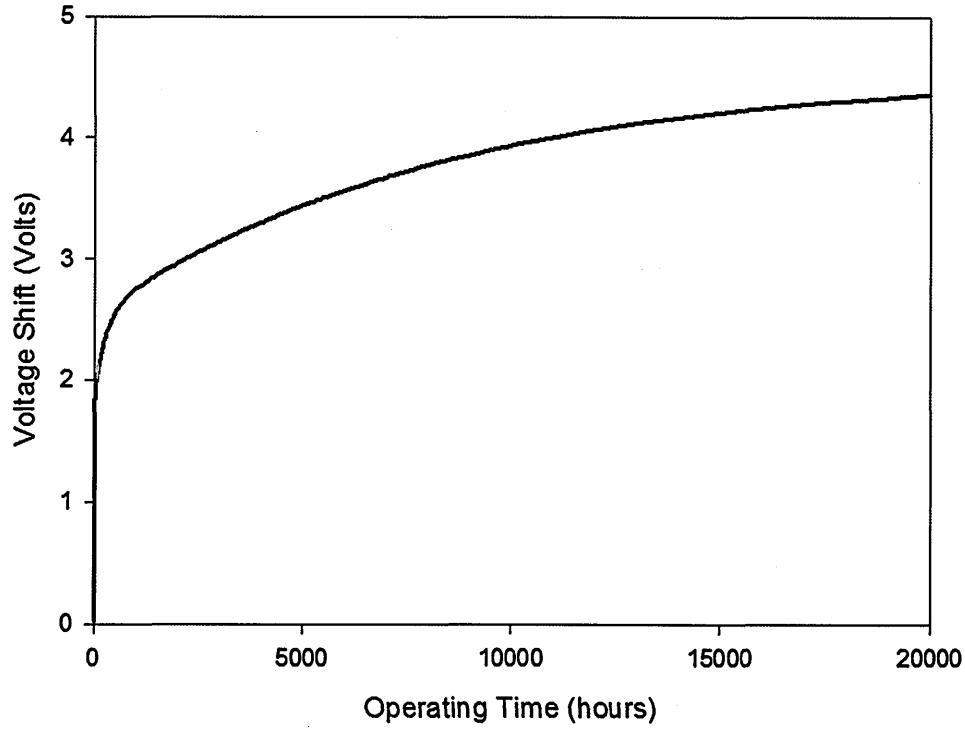


Figure 5-1. Voltage shift required to maintain a contant gain of x1000 (e2V-Technologies 2006).

By limiting exposures to both high potentials and high signals levels the ageing effect can be slowed, but not stopped. These methods can be used to work around the problem (Andor 2008). Although for particular terrestrial applications this may be acceptable, the uncertainties involved are not ideal for space applications, and therefore a more robust solution is necessary.

5.2 Automated test equipment

Life testing experiments on EMCCD ageing are long-term and time consuming; it is not sustainable to manually obtain data for the many hours it takes to obtain a single result. Therefore, an Automated Test Equipment (ATE) was setup prior to any results being obtained.

The newly developed ATE, see Figure 5-2, enabled complete autonomous life testing of the EMCCDs. With this, an EMCCD device, unconditioned or otherwise, could be taken, aged with whichever potentials or timings the user requires, while producing large amounts of data. The large amounts of characterisation data produced, with a point every few seconds in a 2 – 3 hundred hour experiment, allowed the use of a rolling average to plot the data and the standard deviation from the mean for the errors.

As will be described in Chapter 6, the ATE allowed for more advanced, novel experiments to be performed providing a deeper understanding of the inner workings of devices undergoing the ageing process. The different aspects of the setup are shown in Figure 5-3.

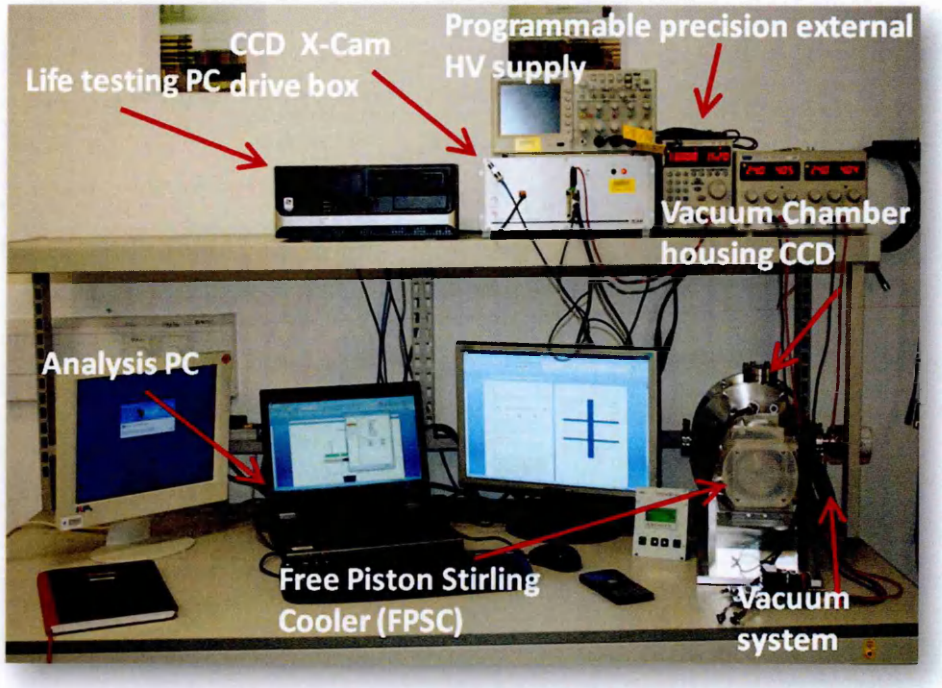


Figure 5-2. Experimental setup for ageing investigation.

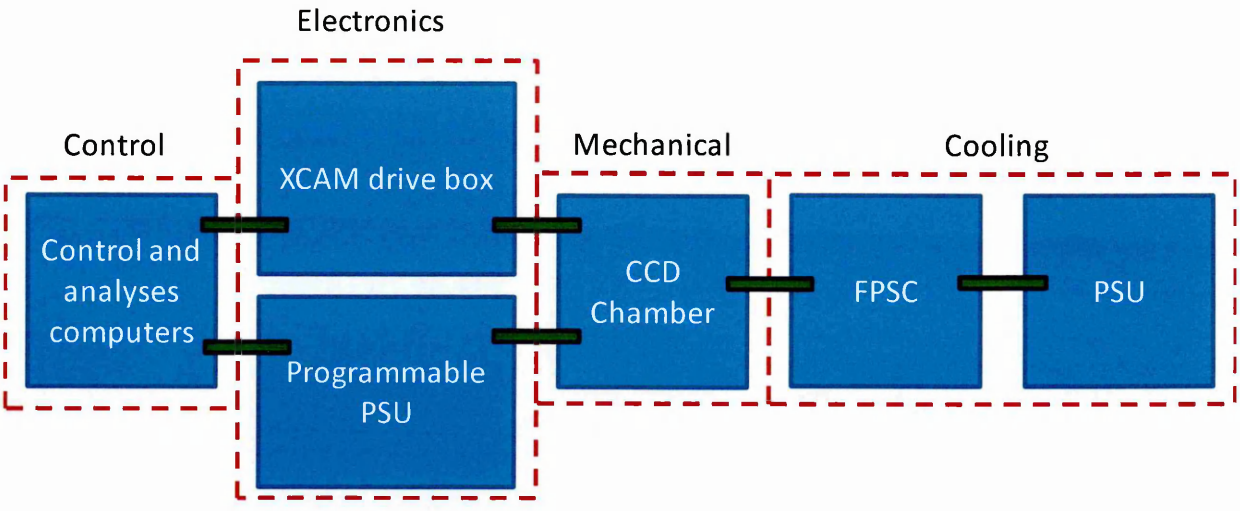


Figure 5-3. ATE block diagram.

The ATE took a sizeable amount of time to develop and get fully functional, however, once produced it allowed easy testing of these devices.

5.3 EMCCD ageing characterisation

5.3.1 Initial characterisation

The system used to take the initial characterisation results was temperature stabilised to approximately 28°C using a heating resistor and a temperature controller. Dark signal was integrated for 1ms in each frame and used to calculate the gain. The temperature stabilisation had a slight lag due to the fluctuating high voltage in the devices producing a relatively high power spike. Therefore, a pair of frames were taken in quick succession for each gain measurement, one at unity and on at the chosen avalanche potential. This method ensured that any changes in dark signal created by the temperature fluctuations would be cancelled out. The fluctuations were only +/- 0.5°C and were therefore deemed not to have a great effect on the gain itself. The offset provided by the readout system was subtracted and then the ratio of the two frames taken. The initial results are shown in Figure 5-4. These two devices were unconditioned and were used as an initial demonstration of the effect and the working of the ATE. The sampling rate was very high

with a frame every few seconds; the plot is a rolling average of 11 points. The errors were found by the standard deviation from the mean of the raw data.

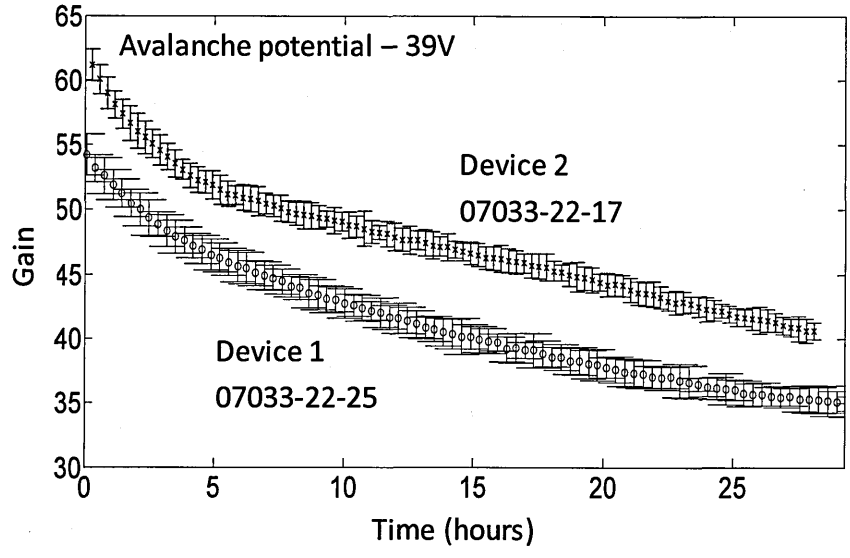


Figure 5-4. Ageing characterisation of devices 07033-22-25 and 07033-22-25

Reasons behind the different starting points of each device are; a) manufacturing inconsistencies and/or b) the devices were run for a different amount of time during the DC tests in manufacture, these are performed to see whether or not the devices are functional. The gain of each device was observed to decrease with operation starting more abruptly and levelling off. This intimal result was used to confirm the test procedure and the ATE.

Further devices were provided by e2v technologies to explore how the ageing phenomenon is affected by certain operating conditions, specifically signal levels and whether or not the speed at which the signal is passed through the register affects it in any way. All these results provide an understanding of the ageing effect in the hope that an answer to the cause and a solution can be found.

5.3.2 Dependency on avalanche potential

A third unconditioned device was taken further; the same method of calculating the gain was used as previous, however, a long-term automated process was implemented. The device was initially aged at 39V for approximately 4.5 hours; the HV was then automatically increased to 39.5V for another 4.5 hours. This process was repeated up to 42V at half volt intervals. Once complete and the 42V data was taken, a second run automatically started with the avalanche potential dropping back down to 39V and the process restarting. Like the data shown in Figure 5-4,

Figure **5-5** is a rolling average of 11 points and the errors calculated in the same way.

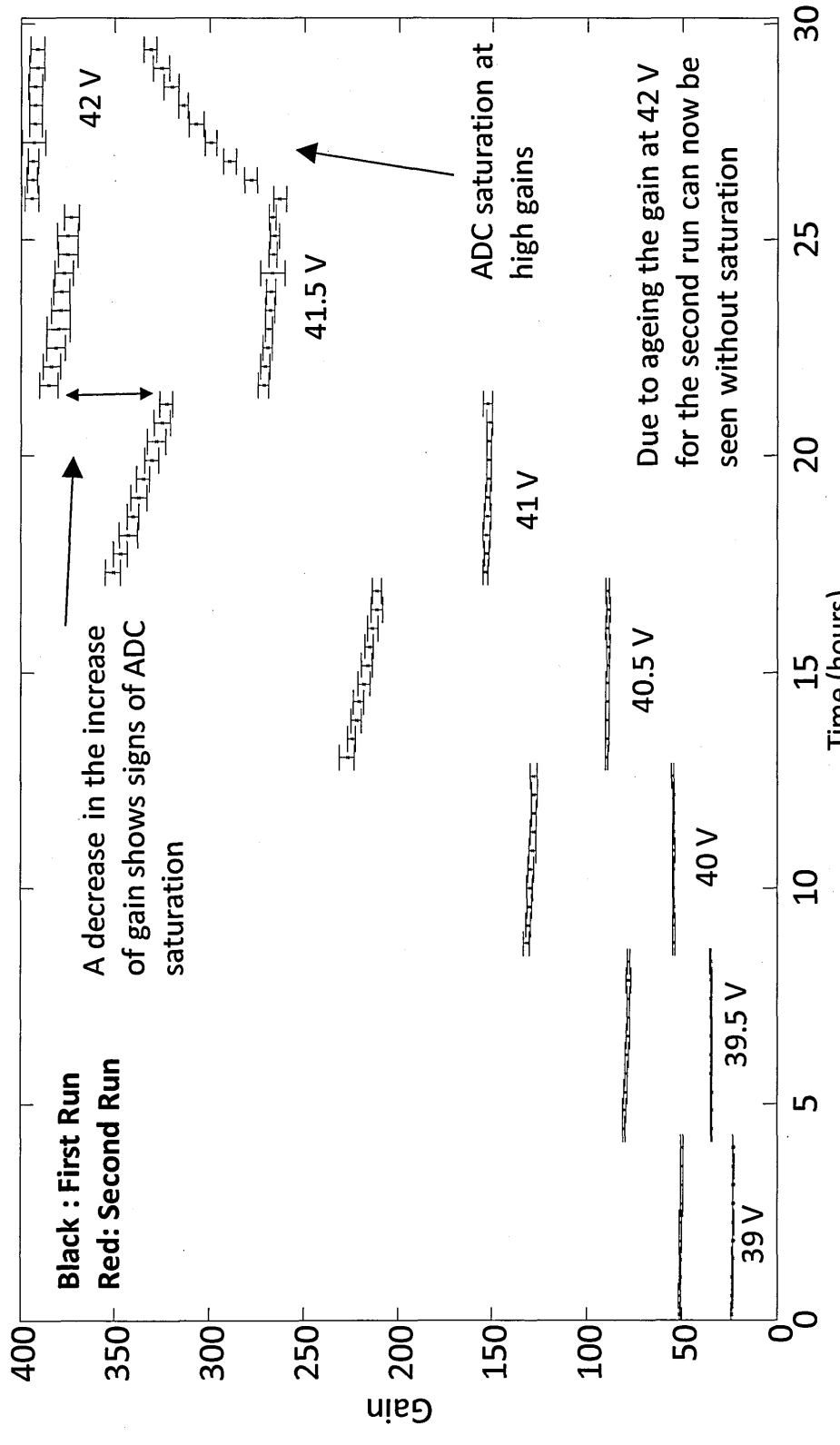
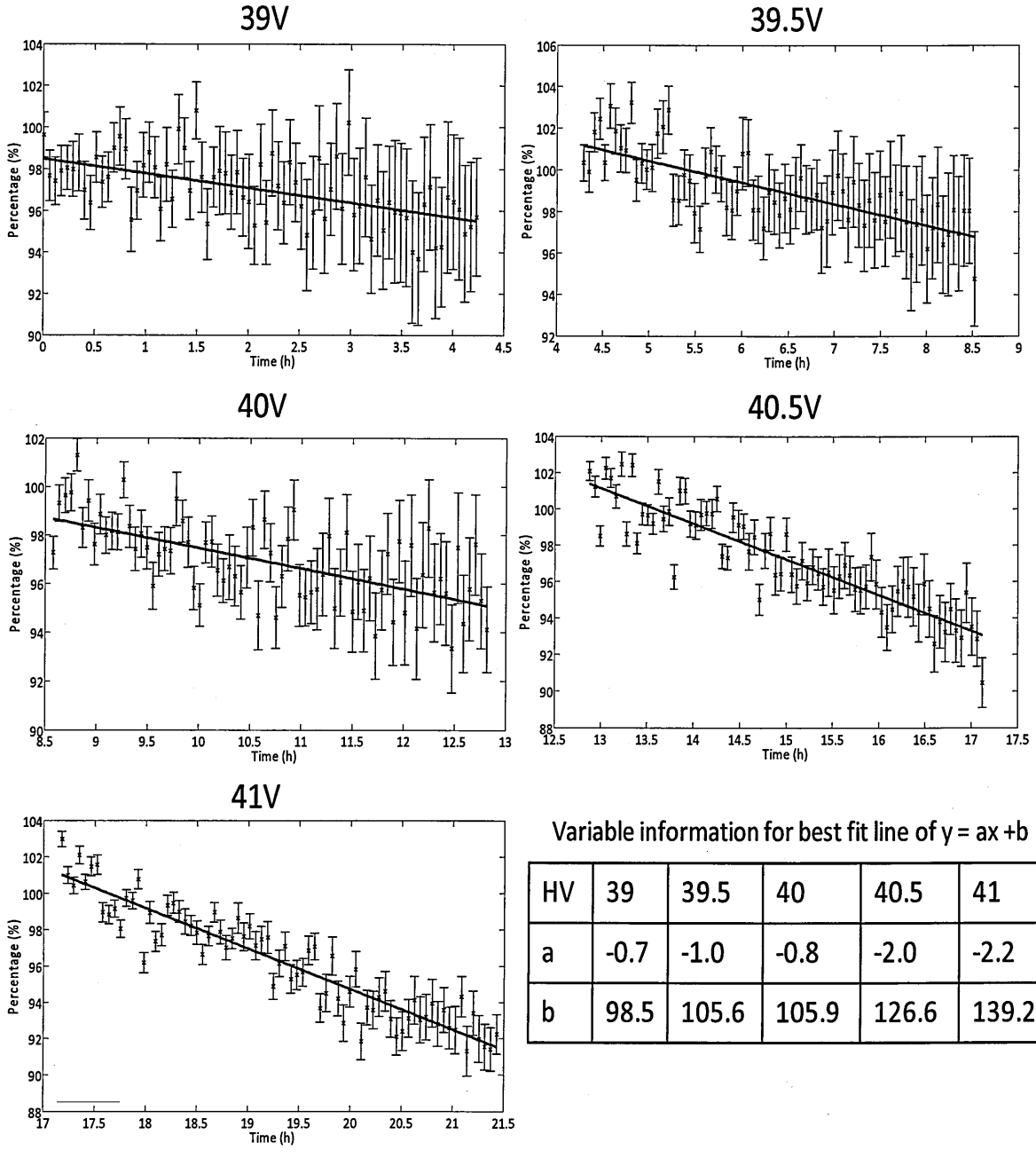


Figure 5-5. CCD97 aged at various avalanche potentials. Data taken and plotted autonomously using the ATE.

The initial run is indicated in black and shows an increase in both the gain value and in the rate of gain loss with increasing avalanche potential. Device saturation at the higher potentials can also be seen. The gap between the gains at 41V and 41.5V was not as large as expected due to the onset of ADC saturation. Once 42V was reached the ADC of the system was fully saturated and the data deemed not usable. After this 42V reading, the second run began with the results shown in red. It is clear that the gain at each avalanche potential is lower than the first run and more importantly, that the system no longer saturates at the higher potentials, which is indicative of a large decrease in output signal.

There is also a difference in the percentage drop in gain for each avalanche potential and between the two runs, showing both a slowing of the ageing phenomenon as time progresses and a dependence on the avalanche potential. For the initial run this is shown in Figure 5-6. A clear loss of gain within each potential and a distinct increase in the rate of gain loss is observed as the avalanche potential is increased. The second run shown in Figure 5-7 is somewhat less clear with only a clear gain loss seen at 39v and 41V. This is possibly due to the device, after 39V on the second run, now entering the second phase of the ageing phenomenon and therefore the effect is slowed. It is only once the avalanche potential reaches 41V that the device re-enters a steady decrease in gain loss and the ageing continues. The best fit lines plotted and the tabulated information in each figure best show this information with a steady negative increase in the gradient variable, 'a' for the first run and not so steady for the second. The errors of these plots were propagated through from the errors in Figure 5-5.

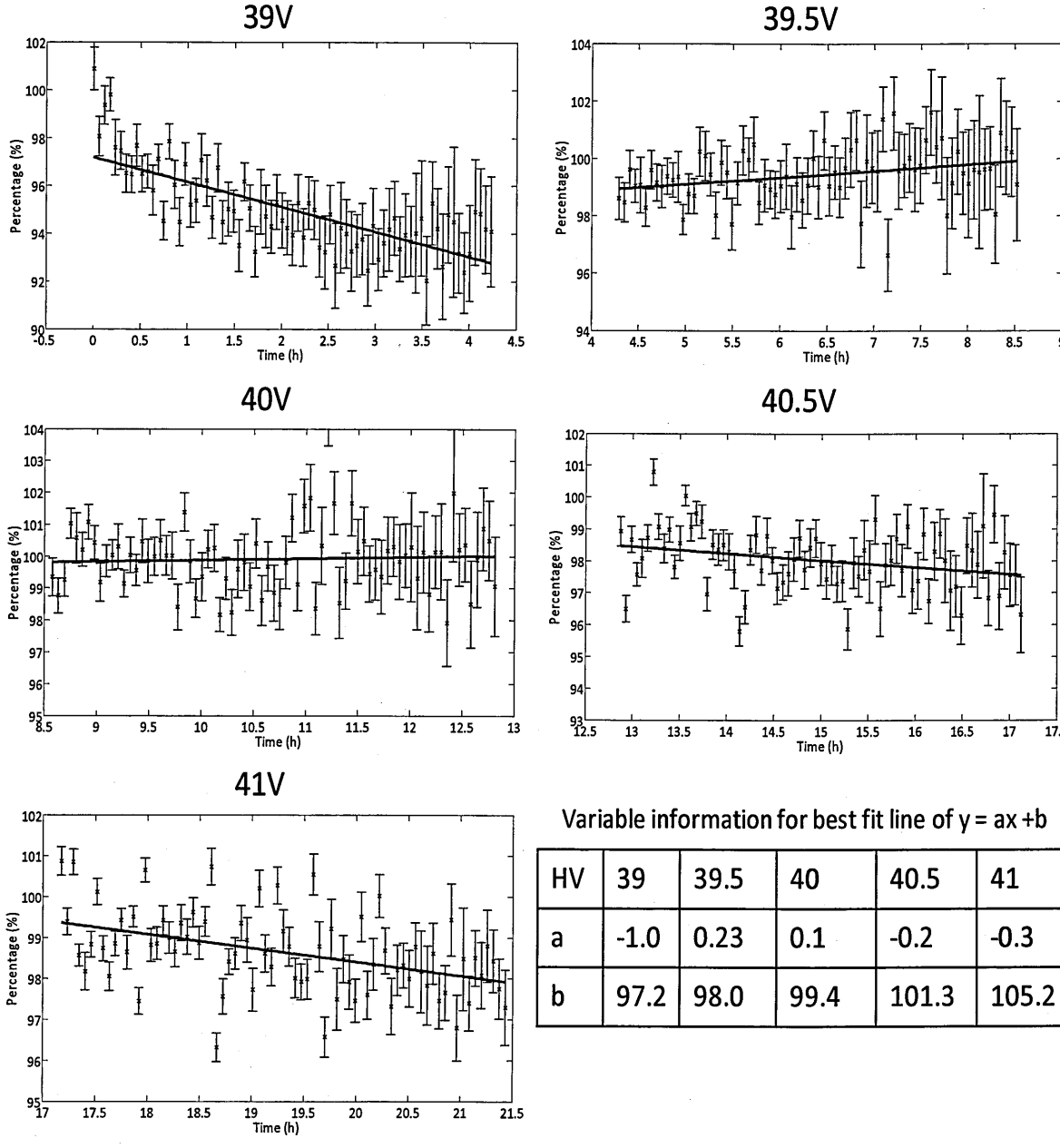
The dependence on avalanche potential shown here is found to be linked to the amount of signal that is generated under the higher potential electrodes.



Variable information for best fit line of y = ax +b

HV	39	39.5	40	40.5	41
a	-0.7	-1.0	-0.8	-2.0	-2.2
b	98.5	105.6	105.9	126.6	139.2

Figure 5-6. Change in gain loss for each avalanche potential.



Variable information for best fit line of y = ax +b

HV	39	39.5	40	40.5	41
a	-1.0	0.23	0.1	-0.2	-0.3
b	97.2	98.0	99.4	101.3	105.2

Figure 5-7. Change in gain loss for each avalanche potential.

5.3.3 Dependency on read-out rate

he same device was then used to show a dependence of gain loss on the read-out rate of the device. This time however, a different method of calculating the gain was used. The device was cooled to -100°C using an FPSC as described in Chapter 4. At this temperature the dark signal generated is negligible and therefore a different source of signal was needed, in this instance an LED. The sequence file was amended to flash the LED for 1ms at the time of integration. Aluminium foil was used to disperse the light as much as possible in an attempt to obtain a flat field, and for the purposes of this experiment; this method was found to be sufficiently effective. The gain calculation itself was then the same as for the dark signal, but a pair of frames was no longer needed for each measurement as there were no longer variations in dark signal. Due to there being no dark signal and very low light intensities from the LED, higher avalanche potentials and hence higher gains were achievable without saturating the ADC. For this experiment an avalanche potential of 44V was used and due to the low temperature, gains of approximately x8600 were observed. The first curve in Figure 5-8 shows the initial ageing at this potential with the device running at 190 kHz, the device was then switched to 410 kHz. There is a clear acceleration in the ageing once the device was switched to the faster pixel rate. This is consistent with the idea that larger signals passing through the register accelerate the process; this idea is further enforced in the following chapter where it is shown that the later elements of the gain register age to a greater extent than the former. The slight increase in gain at the point of switching is thought to be due to the timing differences of the clocking, but the fundamental reason for this is still unknown.

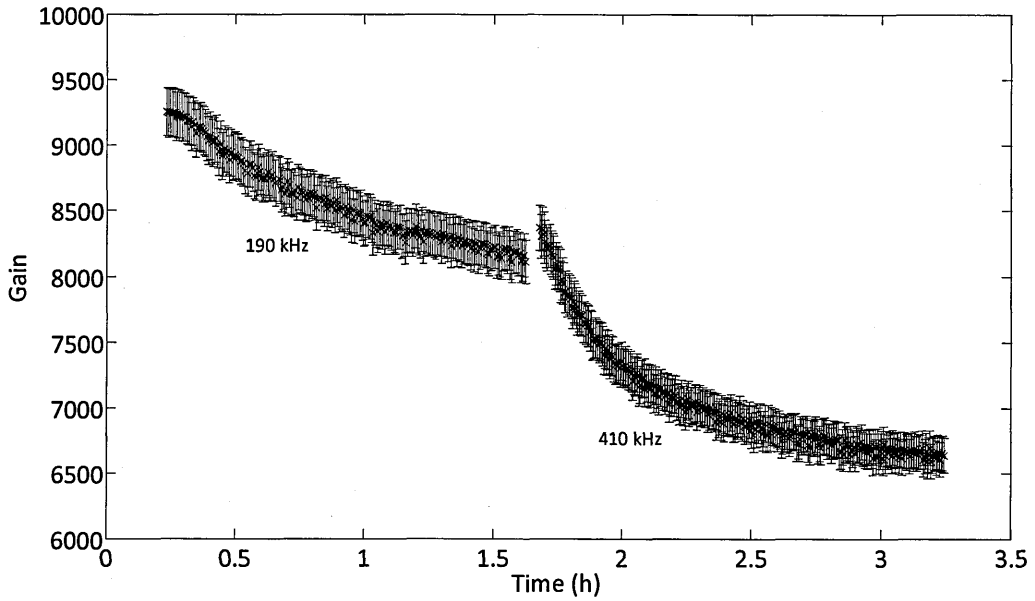


Figure 5-8. Ageing dependency on read-out rate.

The average rate of change of gain per hour (g/h), in the 190 kHz case was approximately 1278 g/h. For the faster, 410 kHz case this was 2467 g/h. This is a factor of a 1.9 difference, which is consistent with the 2.1 factor difference between the read-out rates themselves. This indicates that as the amount of signal passing through the avalanche register doubles, so does the rate of ageing. To appropriately compare this, exponentials were fitted to each curve and the rate of change parameter, b, was compared. Figure 5-9 and Figure 5-10 show the fits for 190 kHz and 410 KHz respectively. The errors for the data was calculated in the same way as the all the previous ageing results.

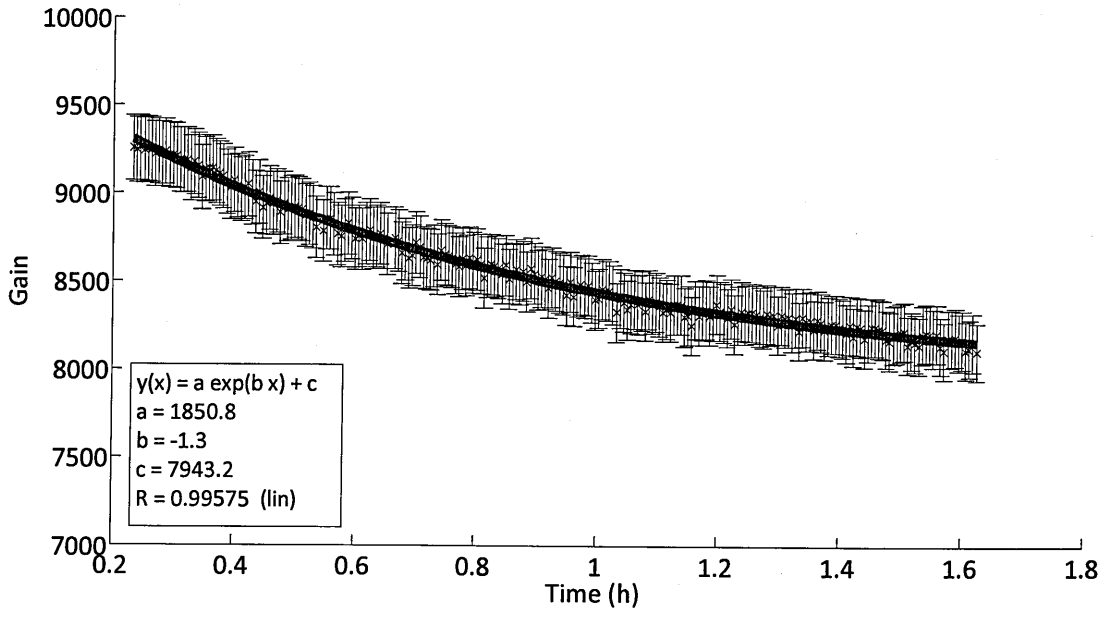


Figure 5-9. Ageing observed at 190 kHz.

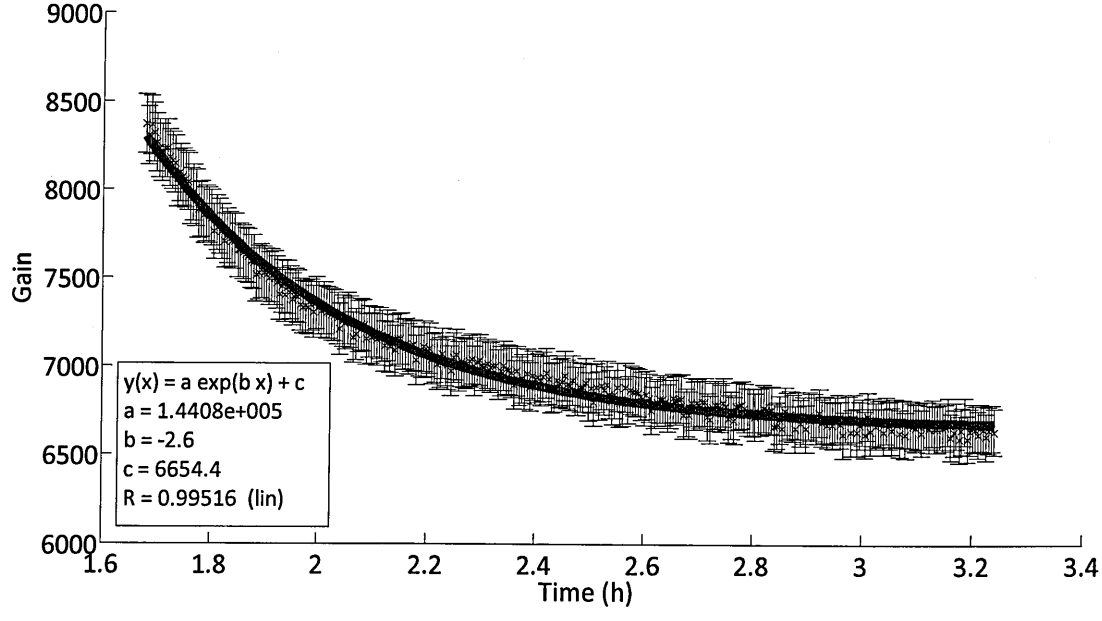


Figure 5-10. Ageing observed at 410 KHz.

Figure 5-11 shows a comparison between the rate of change parameter, b, for each fit. The line was then extrapolated and pinned to zero with the reasonable assumption that no ageing takes place when nothing is being read out.

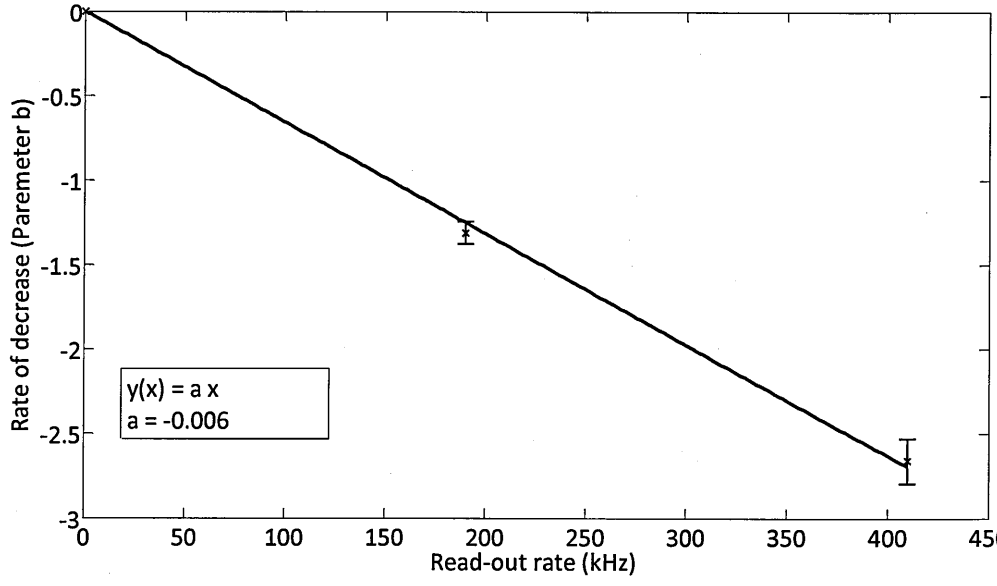


Figure 5-11. Comparison between parameter b for each different read-out rate.

This plot graphically shows that the rate of ageing is proportional to the read-out rate and can be used to determine the approximate rate of ageing at any given speed. It is important to note however that this plot is only valid for a CCD97 at the same stage of the ageing process, at the same temperatures and with similar sequence timings. It is also unwise to extrapolate this plot to MHz rates as the fast speed may have an unknown effect upon the ageing.

5.3.4 Dependency on signal

The results above show how, over the ranges investigated, the ageing is dependent on the avalanche potential and the read-out rate. However, although indirectly dependant on these factors, it is the increase in signal that these factors cause that directly changes the rate of ageing. This is reinforced again by a model completed by e2v technologies, by

having two input light sources of different intensities and observing the voltage shift required to maintain a constant gain, shown by Figure 5-12. Input signal 2 is the higher of the two signals introduced into the system at time t_1. The black curve is the profile of the curve if signal 2 was used from the start showing that the end result is the same.

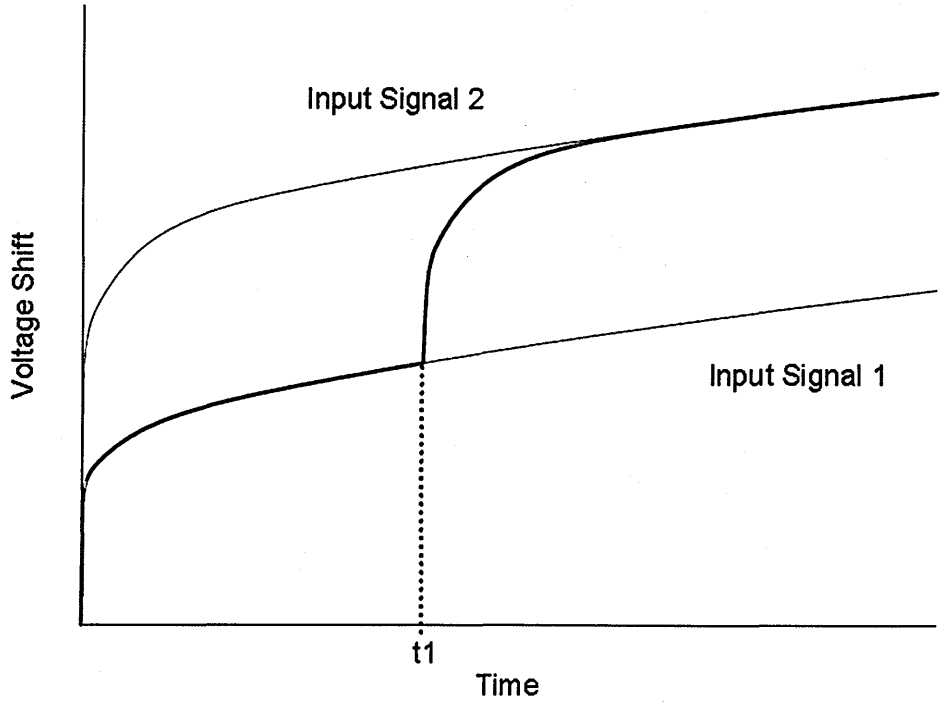


Figure 5-12. Moddelled change of ageing rate with different signal levels (e2V-Technologies 2006).

In these relatively simple experiments it is difficult to show how different parts of the gain register age due to the differences in signal along the length, and to definitively say which parts are ageing at which rates. However, as mentioned before results in the following chapter show that the latter elements of the avalanche gain register age at a higher rate than the leading elements. This is due to cumulative multiplication through the register; the signal starts off small and slowly grows as it travels through becoming much larger at the end.

5.4 The cause of EMCCD ageing

A large part of this research is into the cause of the ageing phenomenon. Characterisation work is essential to help determine the nature of the problem; however, the ultimate goal is to create/operate an EMCCD that exhibits stable gain. The trigger for the research described here and in the following chapter stems from simulation work performed by e2v technologies.

5.4.1 Simulations

The basic assumption prior to simulation was that electrons were gaining sufficient energy within the avalanche phase for injection into the oxide to become possible, resulting in a negative charge build-up and leading to a decrease in the potential underneath the avalanche phase and a reduction in the accelerating field and hence a loss in gain.

The work performed by Frederic Mayer and later repeated by Haydn Gregory however revealed an interesting result. SILVACO (Silvaco 2012), a physics based 3D semiconductor modelling packaged widely used in this field, was used to simulate an avalanche gain register element and the transfer of charge from RΦ1 over ΦDC and into the avalanche phase RΦ2HV. Figure 5-13 shows the complete transfer route of charge from RΦ1 to RΦ2HV. (This work has not been published therefore no reference is available)

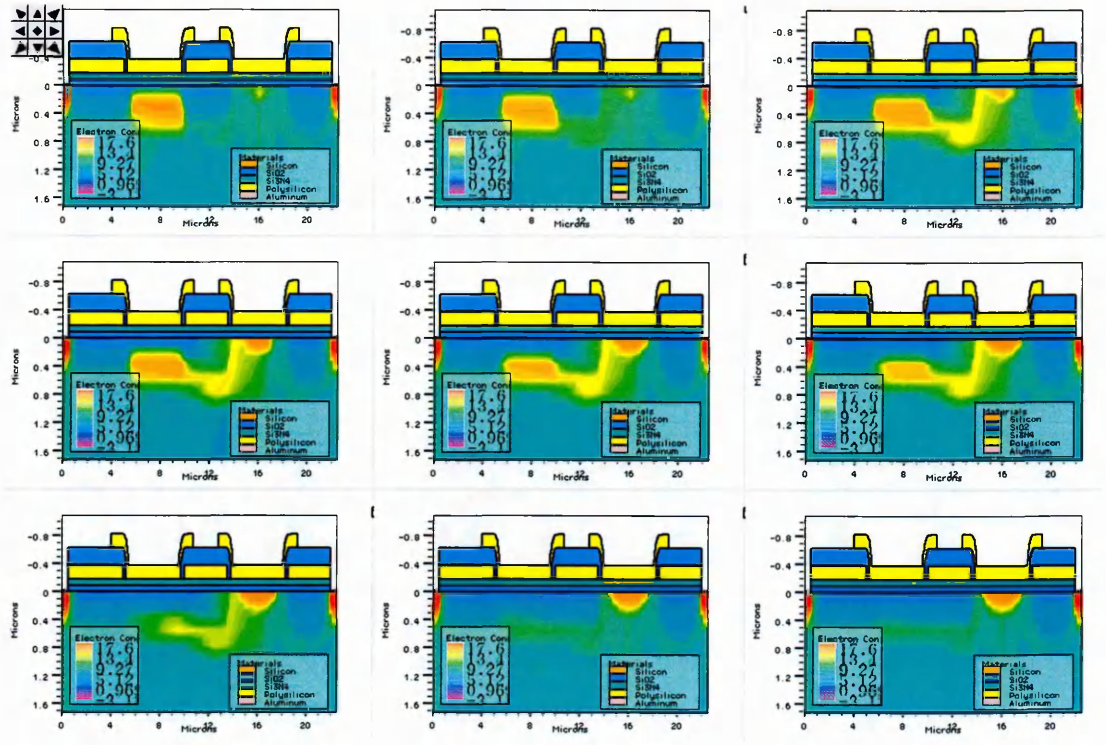


Figure 5-13. Charge transfer simulation of an avalanche register elements.

As the charge enters the high voltage phase, it moves towards the surface as the location of the buried channel potential maximum shifts towards the surface with increasing gate potential. At first glance it seems that from Figure 5-13 the charge is in contact with the surface, this however, due the scale on the y-axis being very different to the x-axis this is not the case. Although other plots were not available for this thesis the simulation was re-run by Haydn Gregory, also of e2v, which definitely shows the charge not in contact with the surface. This result shows that electron injection into the oxide is unlikely.

Another result produced by this simulation was a build-up of positive charge, holes, underneath the preceding barrier phase, ΦDC. Figure 5-14 shows the plot from this result with magnified sections below the main plot.

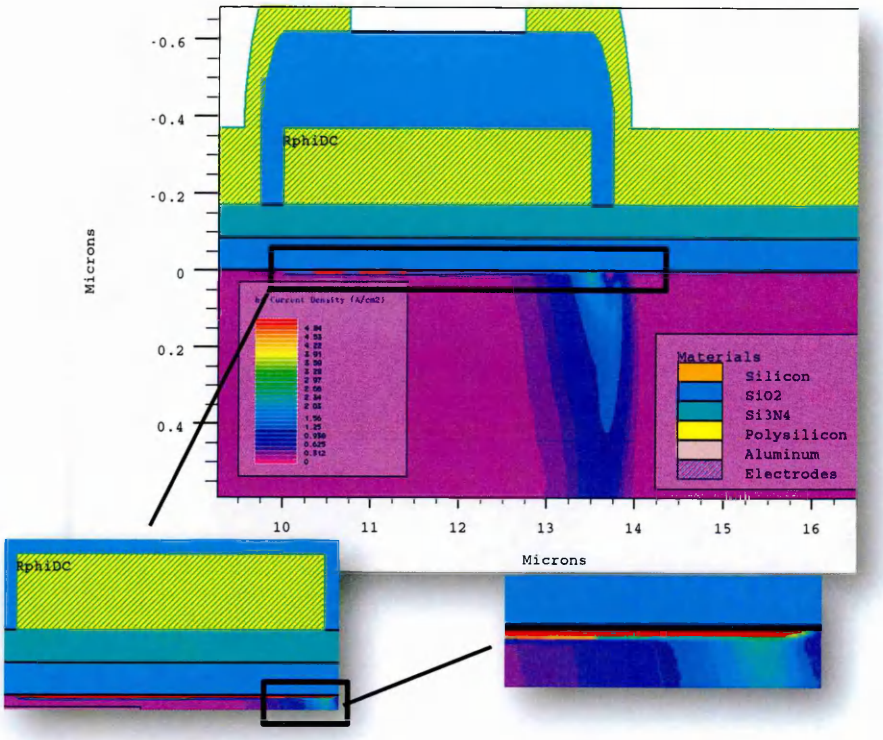


Figure 5-14. Simulation of hole accumilation under ΦDC.

These trapped holes could now in fact be the cause of the observed gain loss as described below.

As illustrated in Figure 5-15, as the trapped holes underneath ΦDC increase, this would cause a potential shift in ΦDC. This shift in ΦDC results in a decrease in the potential difference between ΦDC and the avalanche phase resulting in a reduction of the avalanching field and a loss in gain.

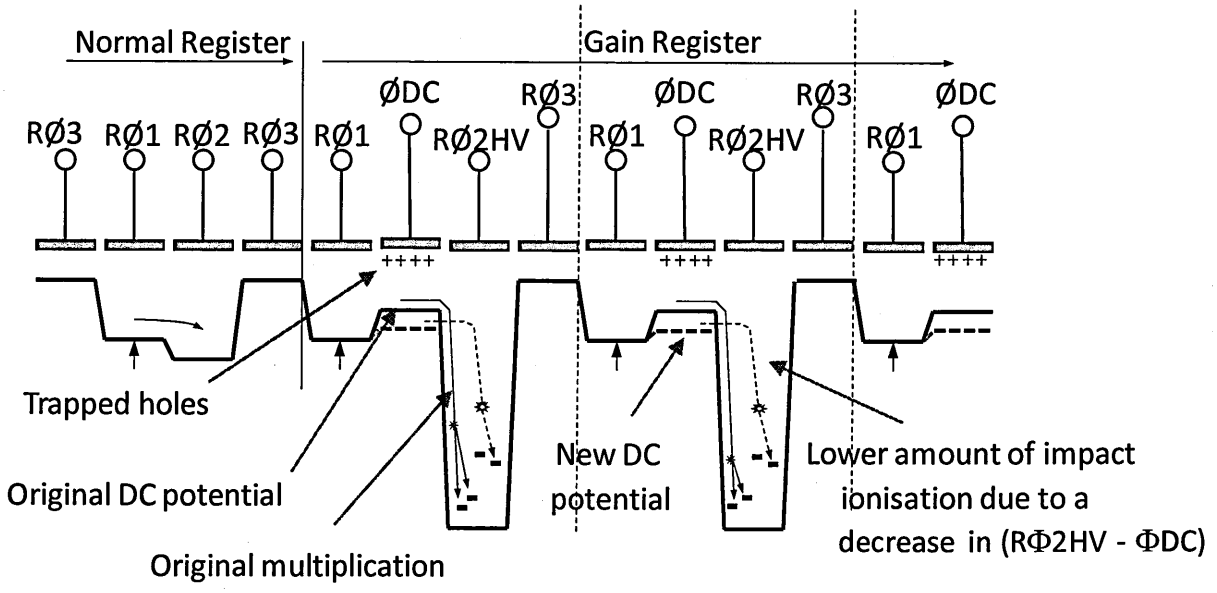


Figure 5-15. Schematic view of the effect of hole accumulation.

As mentioned before the new hypothesis generated from the simulation work formed the basis of the work described here and in the next chapter. Subsequently a theory base on the subject was created and experiments were then designed to test whether or not ΦDC was indeed shifting. Due to the lack of literature on the causes of EMCCD ageing and possibilities around this subject, it was necessary to look at other aspects of solid-state devices that seem to exhibit similar characteristics, namely MOS transistors. This theory is described in the next chapter.

5.5 Conclusion

Characterisation of an unknown phenomenon is vitally important when attempting to pinpoint its cause. At the start of this work only the presence of the effect was known. In this chapters the ageing and its dependence on avalanche potential, clocking frequency and signal have been demonstrated. Through 3D modelling undertaken at e2v and testing performed in this work it is becoming apparent that hole trapping under ΦDC may be a cause of the ageing. Exploration into the theory and the experimental methods followed by the results will be discussed in the following chapter.

Chapter 6: The cause of EMCCD ageing

As demonstrated in Chapter 5, EMCCD ageing manifests itself as an unrecoverable decay in multiplication gain with time. The fundamental cause of the effect is currently unknown, and in order for these devices to be used for space applications, a solution or a stable 'work-around' is required. The aim of this chapter is to present the first experimental data directly on the cause of the effect in the hope of finding such a solution and subsequently raising the TRL of EMCCD technology.

To further the investigation once the simulation work, introduced in Chapter 5, was complete in was necessary to build a theoretical base from similar semiconductor structures that may be exhibiting similar effects, as little has been done in regards to the cause of EMCCD ageing. The next section outlines an introduction into the theory gathered on hole/electron trapping and injection. The breadth of this subject is extremely large. Time constraints and the practical nature of this work has not allowed for an in-depth rigorous investigation to the extent required. The purpose of this work is to experimentally show the result; further work is required for the subject area to be fully explored.

6.1 Electron/Hole trapping and injection

6.1.1 Electron injection

The original hypothesis for the cause of the ageing phenomenon was that electrons were being injected into the oxide once accelerated by the high voltage phase. A good paper on the subject which also contains many references of other work was written by Hsu (Hsu 1984), mentioning channel hot electron injection and substrate hot electron injection. These are injection mechanisms that originate from the channel or substrate

respectively in a MOSFET device. Another paper of interest on this subject regarding the lucky electron model is written by Hu, also mentioning channel hot electron injection. The lucky electron model is one that describes the probability for an electron to be scattered perpendicular to the direction of travel with sufficient energy to become trapped at the Si/SiO_2 interface (Hu.C 1979).

There is also work on other types of electron injection building on 'Channel hot electron' and 'Substrate hot electron' including: 'Drain avalanche hot electron', which is when avalanche multiplication occurs at the drain of the MOSFET and 'Secondary generated hot electron' which is caused by impact ionisation of holes in the substrate. Details on these can be found in two papers written by Takeda (Takeda(b) 1983) (Takeda(a) 1984).

6.1.2 Hole injection

Following the simulation work carried out by e2v in 2010, the focus was on the interaction of holes with various parts of MOS type devices under high field conditions. Described below are possible methods of how the holes come to be trapped under ΦDC. In a following section (1.13) some of the transport mechanism of the holes, once injected, will also be described.

6.1.2.1 Avalanche injection

The process of avalanche injection is one of the possible sources of the proposed trapped holes. As described in detail in Chapter 3, below a certain critical field the drift velocity of the electron increases proportionally with the applied field. Within this region the temperature of the electrons also remains in equilibrium with the lattice. Above this region the mean electron velocity saturates, but individual electrons can have sufficient kinetic energy, i.e. a higher temperature than the lattice, to ionise valence band electrons causing impact ionisation. A cumulative effect of this process is known as avalanche

multiplication. Due to the saturation of the drift velocity at high electric fields and the continued increase of electron number due to the avalanche process the current density increases. Past a particular limit electrons can be considered as a gas or 'space-charge' rather than a single point. This space-charge distorts the electric field as described in detail by Gunn (Gunn 1956). The distortion leads to the field near the positive electrode becoming large compared to the mean field and the field at the negative terminal becomes very small. As the charge density increases further the effect is enhanced and the avalanche region now becomes very thin and a prolific source of holes. These holes are injected backwards into the low field region as depicted by Figure 6-1. Further details on avalanche injection can be found in the literature (Moens 2001) (Gunn 1956).

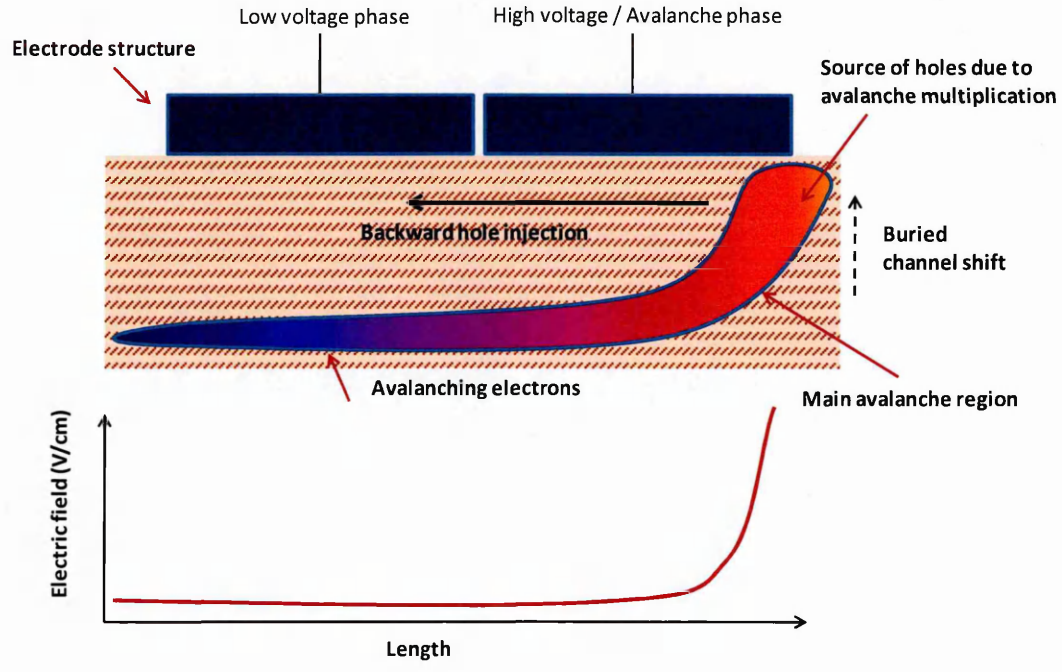


Figure 6-1. Avalanche hole injection within an MOS type device under high field conditions.

It is difficult to say for certain whether these holes are injected horizontally, vertically or some combination of the two. However, it is possible that the holes created in the avalanche process are injected back into the phase preceding RΦ2HV. As a result of their low mobility the holes are trapping at the Si-SiO_2 and/or SiO_2-Si_3N_4 interfaces.

6.1.3 Transport and trapping mechanisms

The subject of hole trapping and the creation of interface states due to hot hole injection is MOS type devices is very large. A good introduction into different hole traps including 'As-grown' traps and 'Generated' traps can be found in the first part of a paper series (Zhang(a) 2004). The second part of this paper then focuses on the generation mechanisms of these traps including the 'electron combination model', 'electric field energy model', ' hole injection model' and the 'hydrogen model' (Zhao 2004). These modes can be summarised as follows; the electron combination model describes trap generation caused by energy released during recombination of trapped holes and electrons. The electric field energy model describes trap generation by directly introducing energy into the oxide thereby creating trapping sites, the Hydrogen model is via both channel and substrate injection mechanism and lastly the hole injection model, which describes injected electrons and holes directly interacting with the oxide. Both papers also offer many references on the subject. There is also work that describes a two stage process in which holes in the oxide drift and trap at the interface, and then recombine with electrons to form interface states (Ogawa 1992) (Winokur 1979) (Zhang(b) 2001). This subject requires more time than available for this work, in order to be fully explored and draw definitive links to EMCCD ageing. As mentioned previously this can form a part of a future work project for a student studying in this area. This chapter is primarily focused on the experimental demonstration of the effect; it is important that the underlying theory be properly and thoroughly investigated in the future.

6.2 Testing for hole trapping

An experiment to measure the build-up of holes under ΦDC was conceived, designed, built and performed. The general theme of the experiment was to measure the full-well capacity under ΦDC, then age the device and then to re-measure. If there is indeed hole accumulation under this phase, then its potential well should increase without the need to increase the gate bias.

6.2.1 Test method

To achieve a full-well capacity measurement of ΦDC the device had to be run in a non-standard way. Custom sequence programs were created in order to operate the CCD in a different way to the manufactured intentions. Ordinarily, an image is acquired by firstly clearing out any excess unwanted charge, setting an image integration time (exposure) and finally reading-out the image data through the output electronics. For the purposes of this experiment the charge collected in the image area was of no use, except for making sure the device was imaging correctly. Therefore, for this experiment, an image was taken in the ordinary manner and then, whilst holding the image phases static, both the serial and avalanche registers were clocked in a custom sequence. This sequence involved integrating charge in the registers with all the clocks at 0V except for ΦDC, which created a small potential well in each element to store charge. The resets phases were held high to ensure that charge would only be stored within ΦDC and that any excess charge, once the phase was full, would drain along the register out through the reset transistor. Once the required integration time was complete, the charge was clocked backwards by one phase in order to return the device to its intended operating conditions (RΦ1 high), and then read-out normally as shown schematically by Figure 6-2.

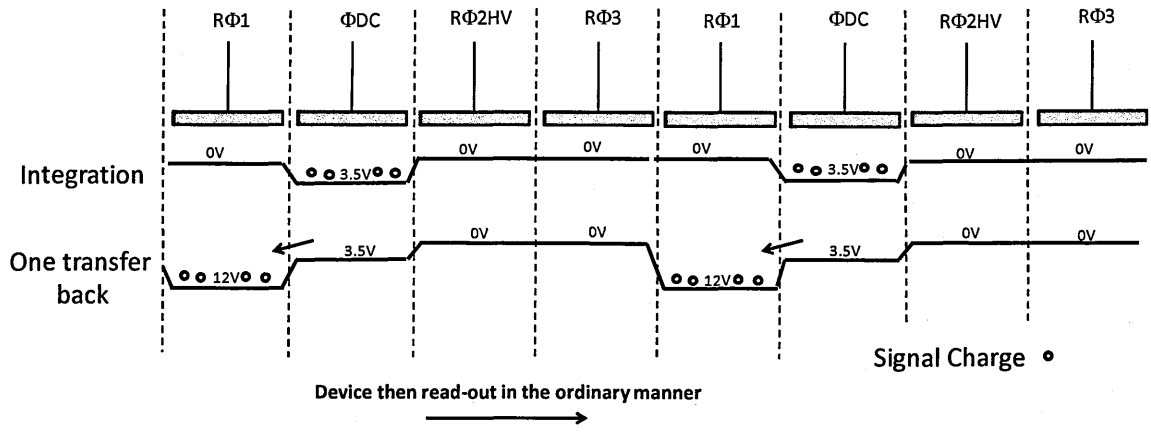


Figure 6-2. Schematic of clocking scheme for obtaining the full-well capacity of ΦDC.

Each frame consisted of one ordinary image and then 10 rows of signal integrated solely under ΦDC, between each of these rows, the signal that had built-up in the image area was cleared, using a clear-loop, and the image section then held static once again ready for the next register integration. Figure 6-3 shows the bottom section of a standard image produced in this experiment. The number of rows was chosen to be 10 as this was deemed enough for a single measurement. This number can be increased if desired, however, more time for each frame is then also necessary.

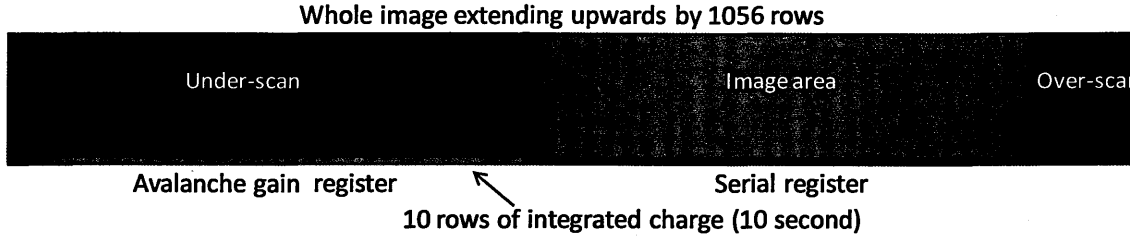


Figure 6-3. Bottom section of the image depicting the 10 rows of dark signal integrated within the serial and avalanche registers.

The integration time within the image area was always set at 1ms. However, for each ageing measurement 4 different register integration times were measured, 1s, 2s, 5s and 10s per row. A single frame, with 10s integration time on each row, with 10 rows took over 100 seconds; therefore the time of each frame was highly dependent on the number

of rows. To investigate the full-well capacity of ΦDC it was necessary to use 10 seconds integration to ensure that the well is saturated before read-out. Figure 6-4 shows a line trace of a single row of dark signal integrated under ΦDC for different ΦDC potentials. From this plot it may be observed no signal is measured from within the serial register, this is because only ΦDC is biased during integration and this phase does not exist in the serial register. Figure 6-5 shows the difference in signal between 10 seconds of dark signal measured over a range of ΦDC values. The linear decrease indicates that in each case full-well has been reached. It is important to note that the difference in signal between 2V and 3.5V is closer to 1.7V rather than 1.5V; this has been attributed to an error in voltage calibration in the voltage .VTG file used by the XCAM software. The same is observed in all the data where all the voltages are found to be offset by ~ 0.2V. This consistency allows the offset not to affect the end result. The errors for this data and all similar plots in the chapter were calculated using the standard deviation from the mean of the 10 rows in each frame.

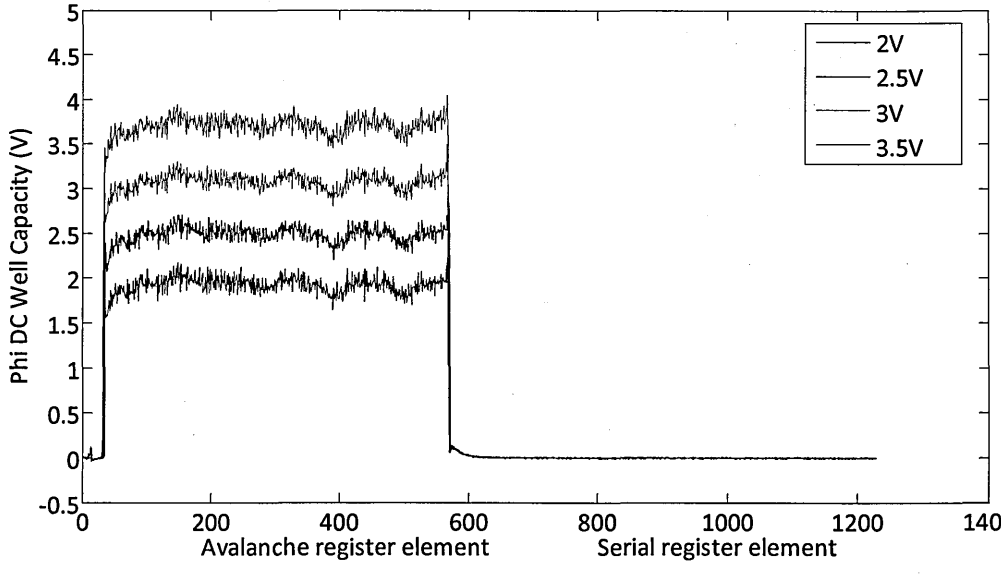


Figure 6-4. Line trace of integrated dark signal within the serial and avalanche registers.

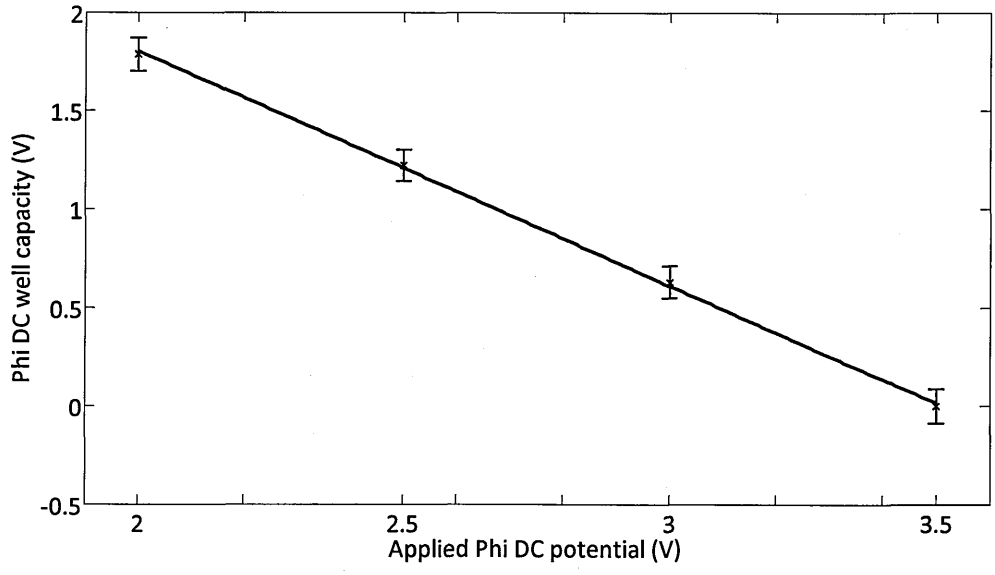


Figure 6-5. Difference of full-well capacity between 2V - 3.5V.

The setup and design of this experiment required careful consideration as the results are entirely new, subsequently there is nothing to compare them against. The non-standard method of operation used, emphasised the need to properly plan all aspects of the experiment.

6.3 Results

6.3.1 Forward avalanche

An unconditioned device was taken and aged using the ATE. Each full dataset required over 200 hours of continuous operation, which made it a perfect task for an automated setup. During the ageing process full-well capacity of ΦDC was assumed to increase. The initial results support the simulation work described in Chapter 5 where positive charge is seen to build-up beneath the phase. Figure 6-6 shows the increase in full-well capacity of ΦDC during the ageing process. This published result is the first to show a possible cause to EMCCD ageing. A repeat of the experiment shown in Figure 6-11 was essential as the result needed comparing for consistency against a similar finding.

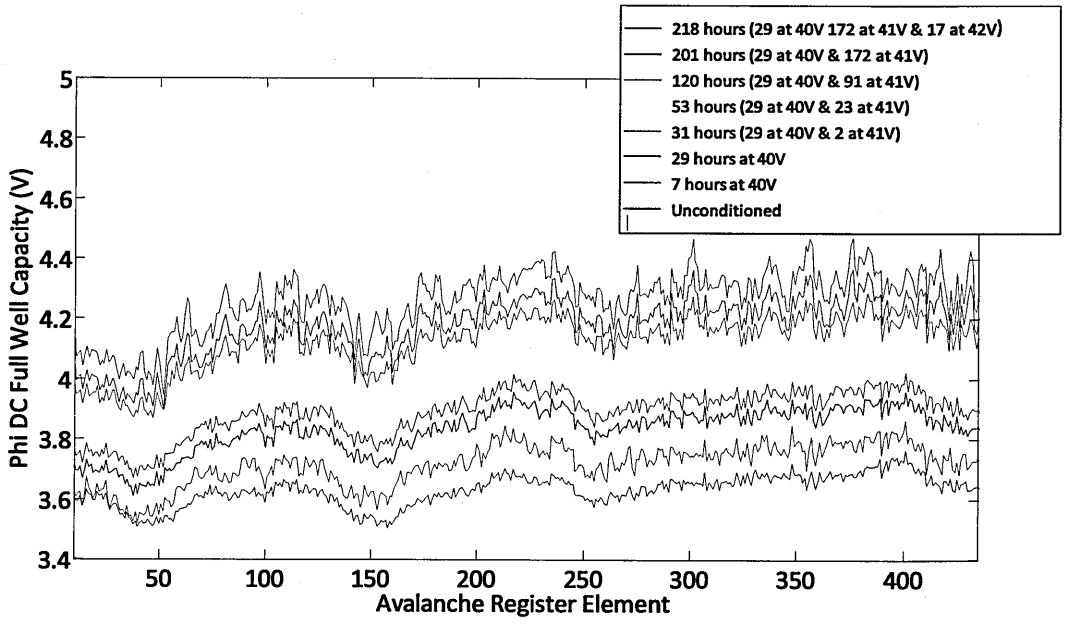


Figure 6-6. Initial result showing the increase of full-well capcity of ΦDC through the ageing process.

The rate of ageing also seems consistent with previous ideas of the rate of this effect starting high and then slowing down as shown by Figure 6-7.

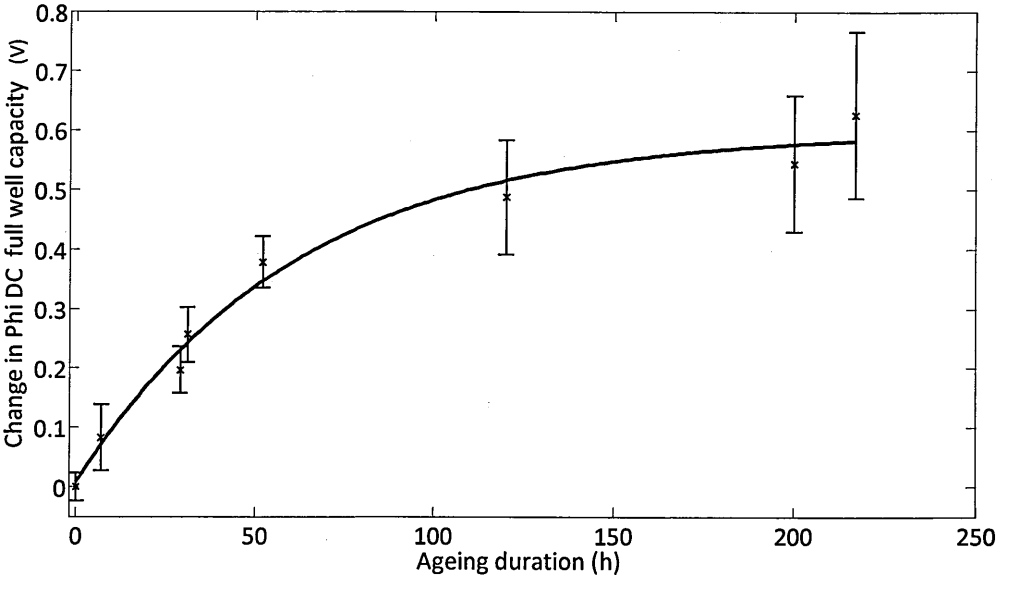


Figure 6-7. Change in full-well capacity device against ageing duration.

As shown by these plots the shift in full-well capacity of ΦDC is not enough to account for all the ageing observed by these devices. In Chapter 3, the ΔV experienced is around 3V -

4V, whereas, the shift observed here is only ~0.6V. It may be said that hole accumulation in this way is not the full effect and that there are possibly multiple causes. However, two possible reasons for the large discrepancy are as follows. Firstly it could be down to how the average signals were calculated. The calculated change was achieved by taking the mean of each ΦDC potential, at the various stages of the ageing process, then subtracting from the mean for the unconditioned device. This value does not take into account that the latter stages of the avalanche gain register have a larger shift compared to the start, as shown by Figure 6-8, and that these last elements have a greater effect on the gain than the first. The ΔV of 3V - 4V shown in Chapter 3 is again an average increase, and does not take into account the larger effect the latter stages of the gain register have. It may not be possible to directly compare the two results.

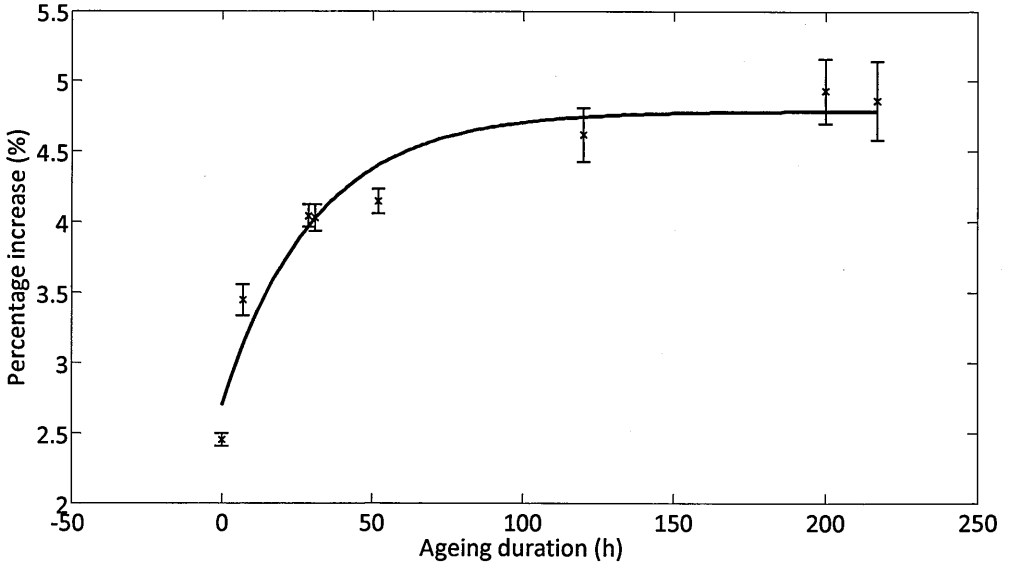


Figure 6-8. Percentage difference of the shift in ΦDC between the first 100 and last 100 elements of the avalanche gain register.

The above figure shows the percentage difference between the first 100 and last 100 elements of the avalanche gain register. The reason for the full-well capacity of ΦDC to change more at the end of the register compared to the start is linked to the work

performed in Chapter 5. The rate of ageing is dependent on the amount of signal passing through the register and due to the method of multiplication, the latter parts of the register experience more signal than the beginning, hence a greater shift.

The second possible reason for the difference between the measured ΦDC full-well shift and the ΔV observed in Chapter 5 can be down to the where exactly under ΦDC the holes are trapping. Figure 6-9 is the layout of an avalanche element, as the electrons flow 'over' ΦDC the main avalanche region will be the section labelled A. If, therefore the injected holes build up predominately in this area and not equally under the entirety of the gate then the measured change in ΦDC shown in Figure 6-6 will be some factor of the total shift observed as it is over a smaller area, the altered potential well diagram can be shown in Figure 6-10. The measured ΔV in this work is over a much smaller area than the value stated in Chapter 5, which is the ΔV applied to the entire gate. If the 'pocket' is for example, ¼ of the total area then the measured value will also be, ¼ of the measured ΔV for the entire gate.

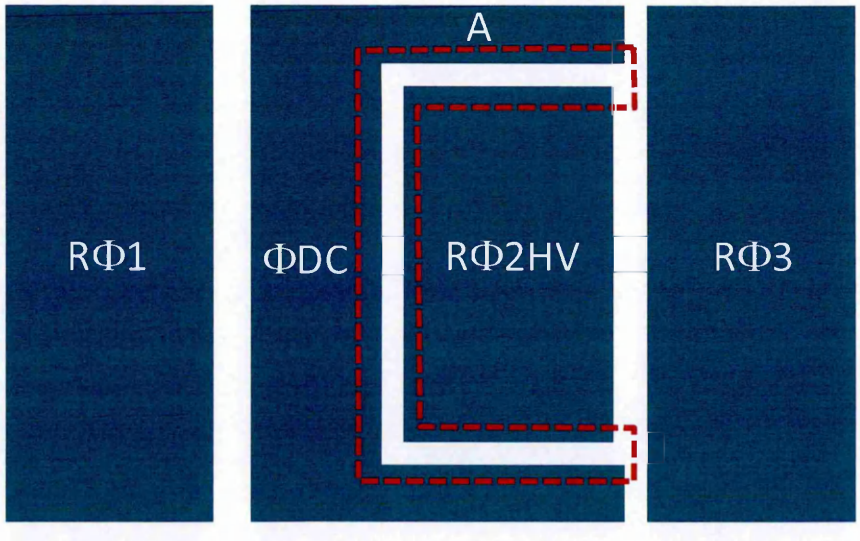


Figure 6-9. Avalanche register layout with avalanche region marked as section A.

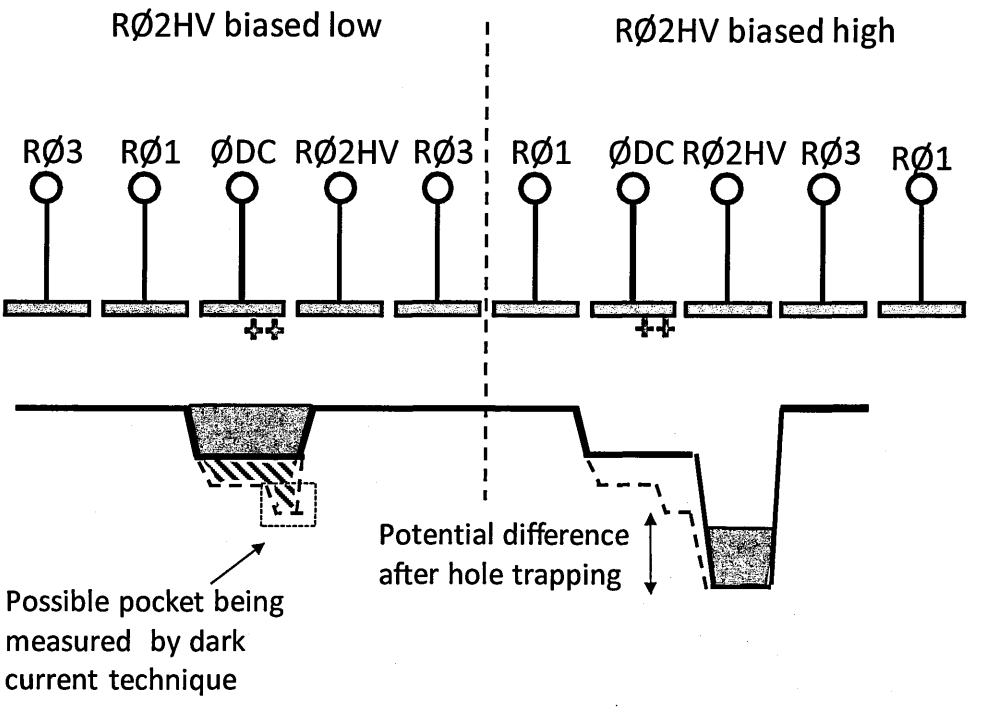


Figure 6-10. Potential well model of the possible accumulation of the trapped holes.

Using a device schematic the surface area of the avalanche region between ΦDC and RΦ2HV was estimated to be 43μm^2. The surface area of the entire ΦDC electrode is approximately 270μm^2. This results in a factor of 6.3 between the two. The approximate value of the ΔV produced by e2v to maintain a constant gain is ~4 V and the measured shift in this work is approximately 0.6 V. Taking the area difference into consideration:

$$0.6 \times 6.28 = 3.8\,V$$

As a working hypothesis this seems to be consistent.

The above results were all repeated using another unconditioned device; the results were very similar and summarised in Figure 6-11.

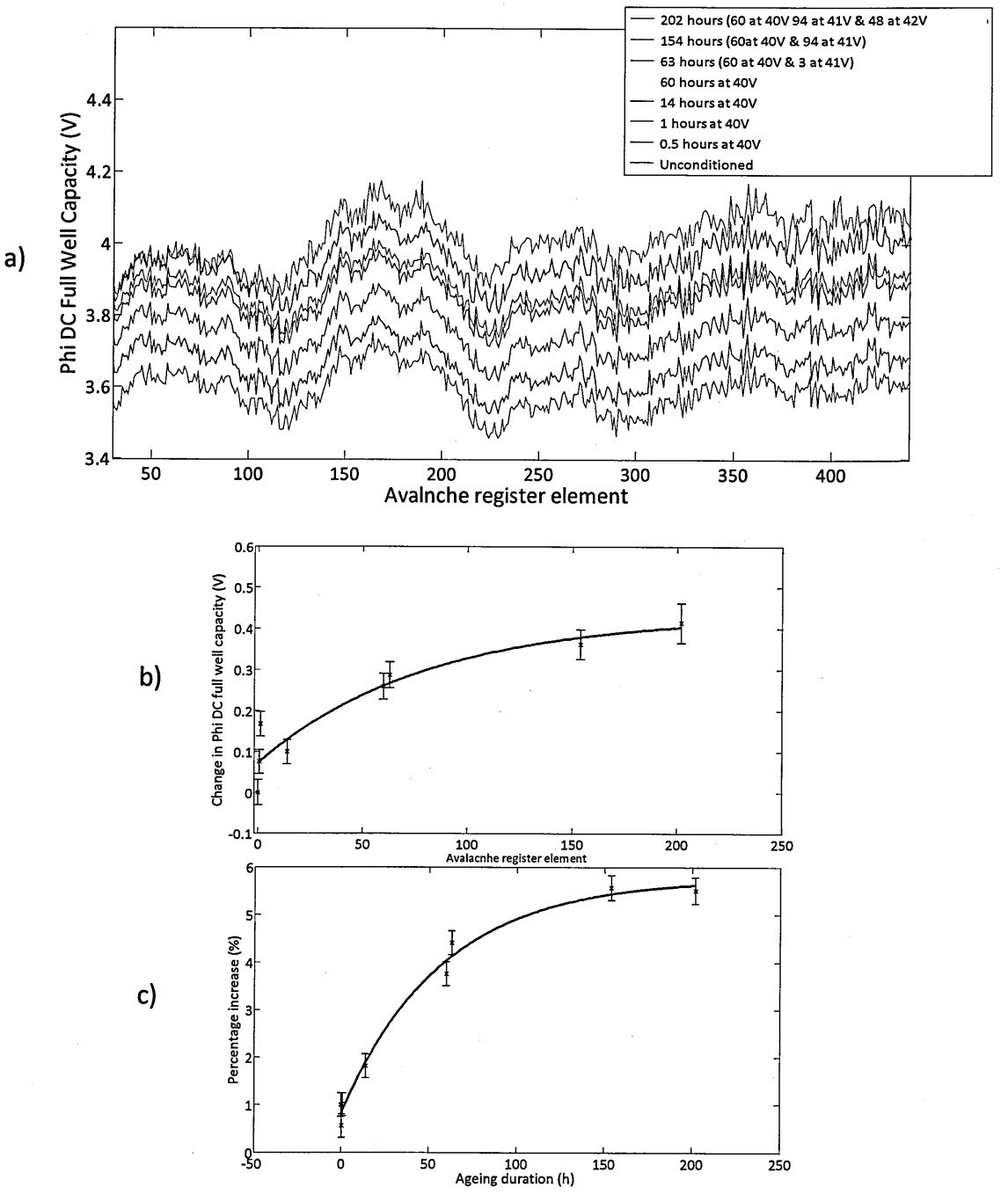


Figure 6-11. Experimental repeat of the full-well capacity shift observed in ΦDC, a) measured full-well shift under ΦDC, b) change in full-well capacity againts ageng duration, c) percentage difference of the shift in ΦDC between the first 100 and last 100 elements of the avalanche gain register.

The second device test supported the result that an actual ΦDC full-well increase is occurring within the devices during avalanche multiplication, equivalent to an increased positive bias. As mentioned previously the fundamental cause of this effect may be linked to hole injection and trapping under the phase.

To further investigate and characterise this phenomenon, an experiment to backwards clock the avalanche gain register was designed in the hope of seeing the reverse effect.

6.3.2 Backwards avalanche

Backwards avalanching was a difficult but interesting experiment to perform. This type of operation is far from the intended operating condition for the devices. The avalanche gain register was not designed to be clocked backwards. The aspect that made this especially difficult was the static barrier, ΦDC, which needed to be overcome in order to successfully move the signal in the opposite direction.

6.3.2.1 Method

Completely new sequences and head-board modifications were required in order to correctly perform this experiment. Figure 6-12 schematically describes how the devices were clocked with the use of the potential well model. A step by step explanation is described below the figure.

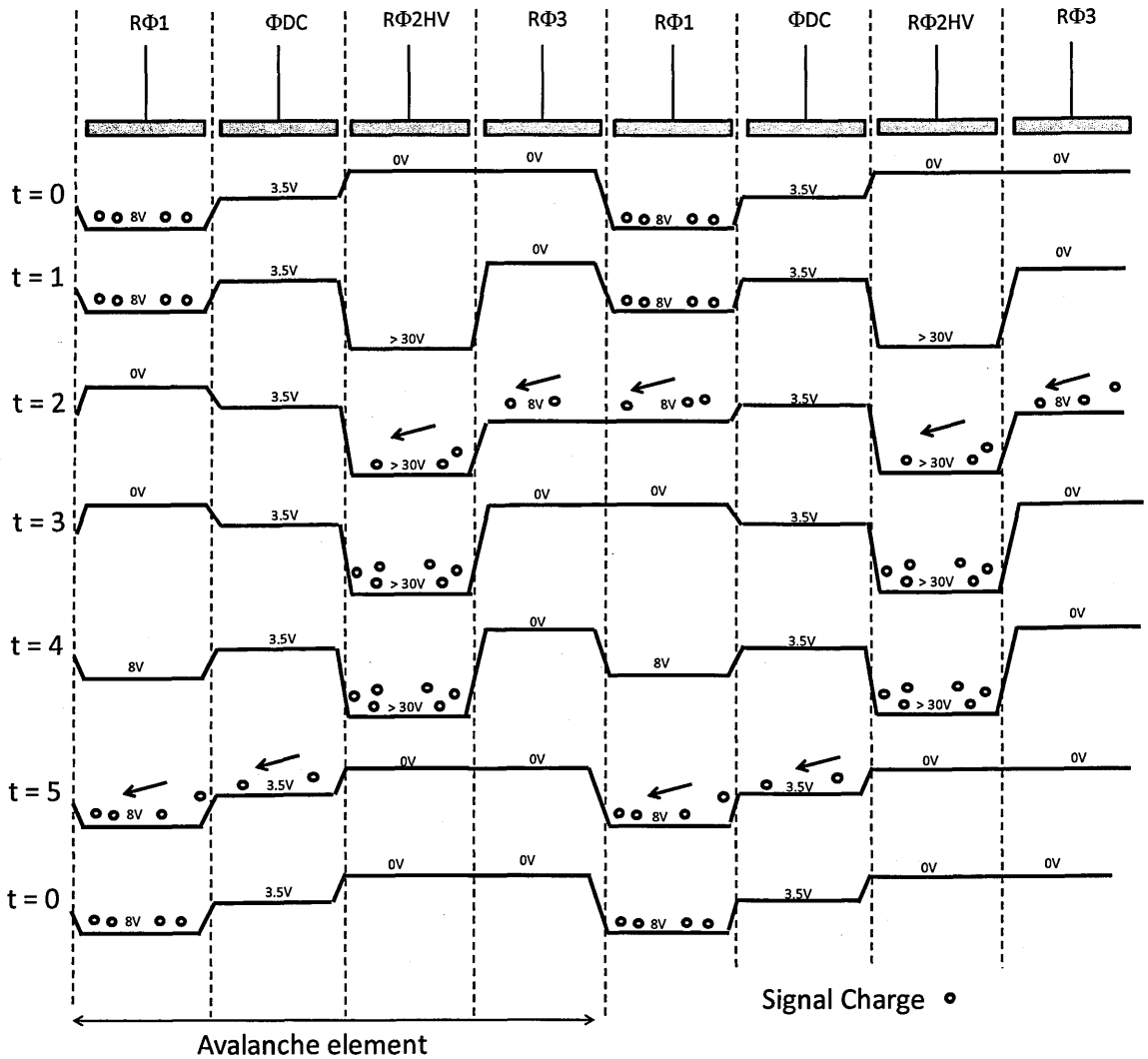


Figure 6-12. Charge transfer in backward avalanche experiment.

t=0: Signal is integrated within RΦ1, under a lower than normal potential of 8V.

t=1: RΦ2HV is biased ready to receive the signal from RΦ3. This well is created first whilst keeping the barrier phase in place in order for the signal to experience the whole potential difference.

t=2: RΦ3 is lowered and the charge signal accelerates through the avalanche phase. ΦDC now acts as the barrier phase

t=3: RΦ1 and RΦ3 and off, the signal is now stored under RΦ2HV.

t=4: RΦ1 is now turned on ready to receive the signal from the avalanche phase

t=5: Signal is transferred to RΦ1 and device returns to the, t=0 condition

In hindsight, this process can be made more efficient with steps 3 and 4 not necessarily needing to be separated; however the aim here was to achieve efficient transfer and not speed.

The devices were therefore clocked backwards under high potential for the desired ageing duration and then read-out under unity gain in the ordinary manner. This would allow the device to be sampled correctly while exposing it to backward avalanche conditions.

6.3.2.2 Results

The first device that was tested in this manner was successful, however; due to an oversight in the method in which the data was taken, the result was not as expected. As with the forward avalanche experiments the capacity of ΦDC was measured at each stage of the ageing process. However, after the result of no-change as shown in Figure 6-13 and, after more considered thought it became apparent that the capacity of ΦDC should in fact not change and it is RΦ3 that should now be assumed to change. The signal is now avalanching in the opposite direction (between RΦ3 and RΦ2HV rather than between ΦDC and RΦ2HV) and any hole injection will also be in the opposite direction, changing the trapping location to under RΦ3.

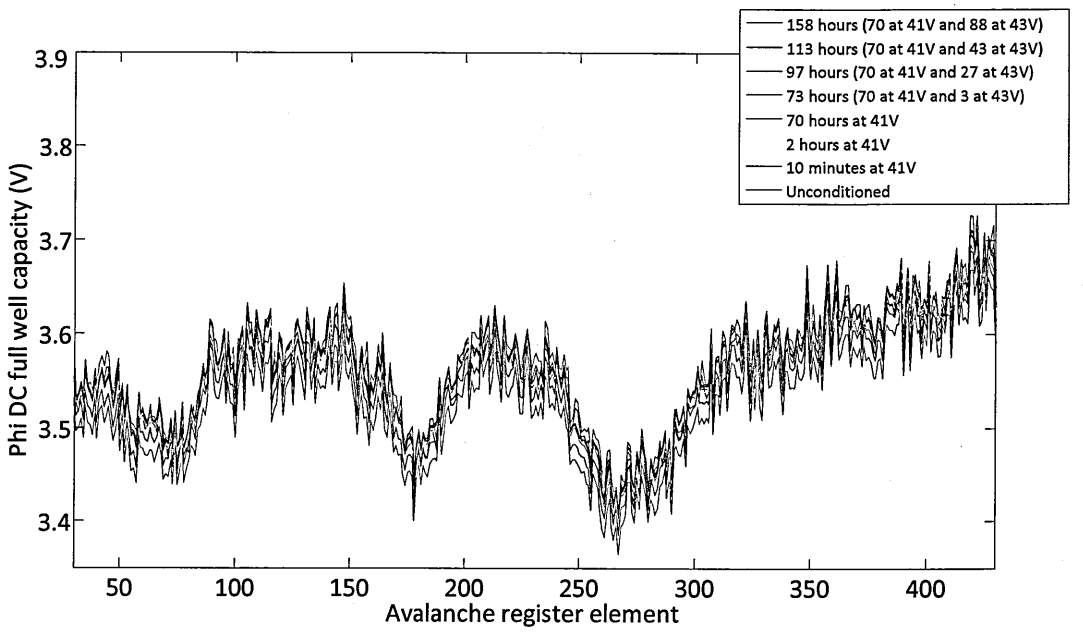


Figure 6-13. Full-well change observed for ΦDC during first backward avalanche experiment.

Once the data was taken and the device aged, the data cannot be retaken therefore a new unconditioned device had to be used to measure any shifts in the capacity of RΦ3. Figure 6-14 and Figure 6-15 now show the change in capacity of RΦ3 and ΦDC respectively. As shown by Figure 6-12, during the ageing process the register clocks were biased at 8V, this was done to obtain a good potential difference between them and RΦ2HV without needing to increase the avalanche phase too high. However, during the actual read-out of the data the register clocks were biased at 5V, this was in order to strike a balance between efficient transfer and a suitable full-well that needed to be filled. After each measurement of RΦ3, ΦDC was also measured to ensure the consistency with the result shown in Figure 6-13.

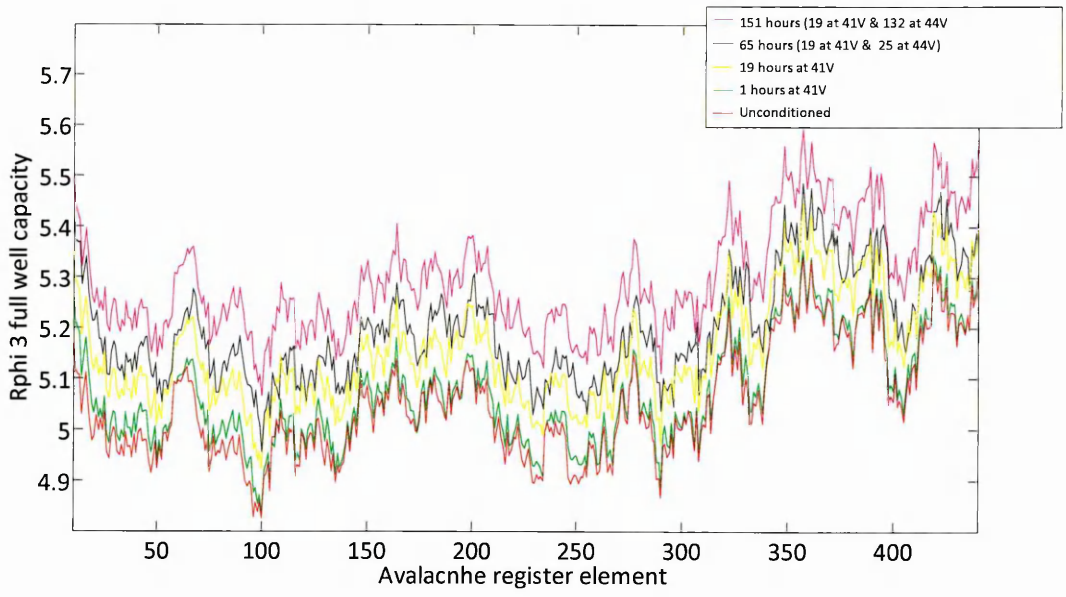


Figure 6-14. Full-well capacity change observed in RΦ3 during second backward avalanche experiment.

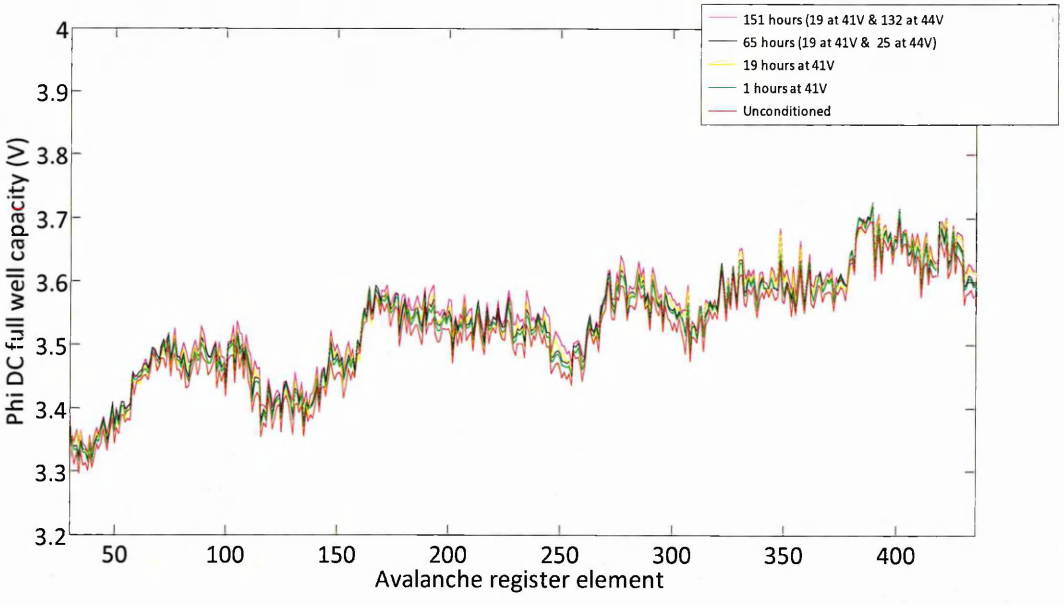


Figure 6-15. Full-well capacity change observed in ΦDC during second backward avalanche experiment.

It appears that now the hole injection is in the opposite direction, hole accumulation is now seen under RΦ3 causing the shift in full-well capacity. It may be noted however the change in capacity observed here is not as high as those in the forward case, although the

same characteristic in terms of the amount of change in relation to the location in the register is the same, shown by Figure 6-16.

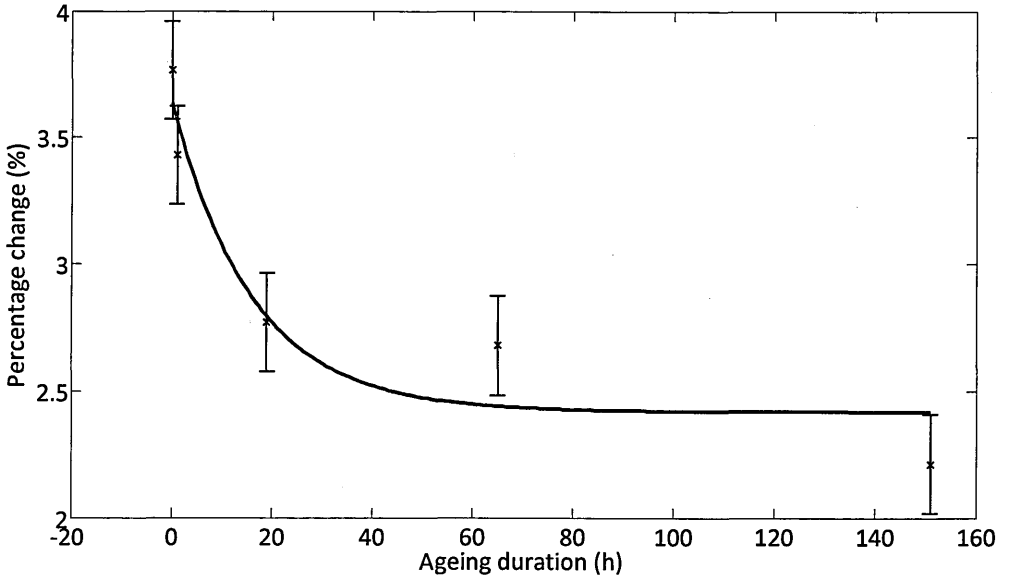


Figure 6-16. Percentage difference between the first 100 and last 100 elements of the avalanche gain register, showing the change to be in the opposite direction for the backward avalanche case.

Two possible reasons for the difference in shift between the forward and backward cases are described below. Firstly the higher voltage on RΦ3 may be having some repulsion effect on the injected holes which may result in fewer being able to trap. The threshold energy for hole injection to occur may have increased. Therefore, an experiment identical to the very first run can be undertaken, however this time, with a higher voltage on ΦDC during avalanche multiplication. Note, that higher avalanche potentials will need to be used to compensate for the decrease in the potential different between ΦDC and RΦ2HV.

The second possibility is linked to a previous section regarding the difference observed in the ΦDC shift between the forward measurement in this study and that of the quoted measurement in Chapter 5. Figure 6-17 again shows the layout of the avalanche element however this time the avalanche region is labelled B, as it is now in the opposite direction.

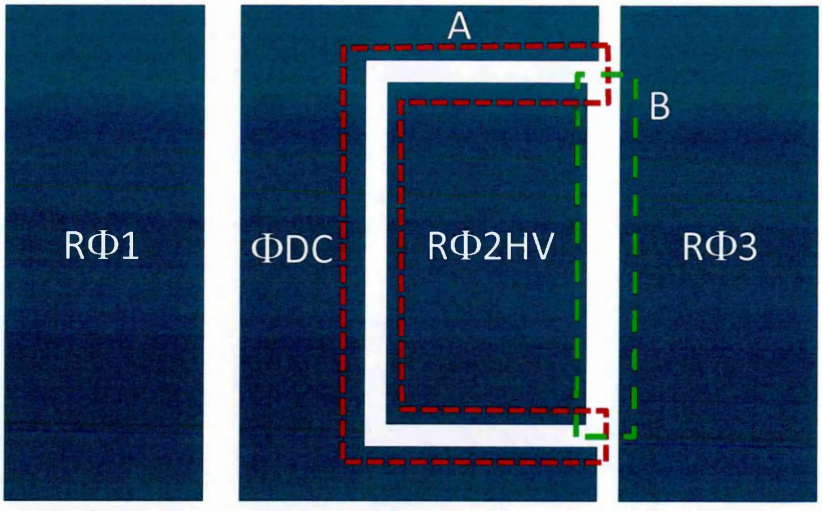


Figure 6-17. Avalanche register layout with forward (A) and backward (b) avalanche regions.

The possible reason for the lower measured shift in the backward case is that the surface area of the avalanching region is less, compared to the forward case, labelled A. Therefore the value of the shift observed is again some factor of, a) the original ΔV and, b) the shift measured under the forward avalanche conditions.

Similar to Section 1.3.1, the surface area of the two avalanche regions were estimated from the schematic. The estimated avalanche region between RΦ3 and RΦ2HV is 35μm^2, as mentioned previously the avalanche region between ΦDC and RΦ2HV was estimated to be 43μm^2. This gives a factor of 1.2 between the two. The measured shifts in ΦDC and RΦ3 are approximately 0.6 V and 0.4 V respectively. Taking the surface area into account:

$$0.4 \times 1.2 = 0.48\,V$$

This value does not seem as consistent as the last, however it appears that the final solution will be similar in nature.

6.4 Device designs

Results presented here can contribute to future of EMCCD designs in order to create a more stable device. Obviously, these results on their own will not be sufficient in persuading manufacturers to change their processes, however, they are the first steps.

Detailed below are some suggested alternatives/recommendations that have come through investigation of the ageing phenomenon throughout this research project:

- Low voltage alternatives: these devices have the aim of provided comparable avalanche gains with a much lower accelerating potential. This can be accomplished by adding additional elements onto the avalanche register, resulting in more avalanche steps hence a lower potential required for a set gain. Additionally, thinner oxides may be used however; this may open up other vulnerabilities such as those from single event particles. Lower avalanche potentials can have significant internal effects, the most obvious being that the ionised electrons and subsequent holes will possess less energy for injection.
- Nitride layer: Another modification that may lessen the ageing as well as allowing for lower potential is the removal of the nitride layer above the avalanche phase. This was originally performed by TI however, their devices suffered from excessive dark current due to the absence of the ΦDC 'horse-shoe' as described previously. Removing this layer can, a) reduce the amount of potential required and, b) removing a potential trapping site between the SiO_2 and SiN_3 layers. A device without this layer, has been developed by e2v technologies however the device was not available to testing for this work.
- ΦDC implant: Finally, the ΦDC barrier is currently created using an electrode much like the rest. However, due to the static nature of this phase it can be proposed to remove this electrode and implant the device in order to create a positive barrier potential. This modification may result in the removal of potential trapping sites within the devices and stop the trapped holes from contributing to the ΦDC potential.

6.5 Conclusion

The intention here was to produce some new results to support the theory revealed In Chapter 5 that energetic holes produced by avalanche multiplication are in some way affecting the bias level of the barrier phase, ΦDC. A novel method for probing the bias under ΦDC has been created by measuring the full-well capacity using dark current saturation. This techniques has been used to show that the full-well capacity of ΦDC does increase during ageing supporting the hole trapping theory. Furthermore it has also been shown that when the device is operated in reverse the bias change is now observed in RΦ3, which now becomes the preceding phase. These results give good support to the theory that hole accumulation in the oxide under the preceding phase of the avalanche gain register is a cause of the ageing phenomenon. The difference in the full-well capacity change to the voltage shifts required to maintain a constant gain is potentially caused by the location of the hole traps. If the holes are under a small section of the phase then the two values for the ΔV cannot be compared. Additionally the differences between the forward and backward cases is most likely down to a surface area effect as the avalanching region between ΦDC and RΦ2HV is larger than between RΦ3 and RΦ2HV.

Chapter 7: Radiation effects on EMCCDs

7.1 Introduction

Energetic particles or photons propagate through a medium; when incident onto an MOS type device, such as a CCD, can have significant effects. In order to safely use these types of devices in radiation environments such as those found in space, an understanding of the subject is necessary.

7.2 Radiation

There are many types of radiation consisting of both particles and photons. It is also common to discuss the electromagnetic spectrum as radiation, however in this chapter radiation will be primarily targeted to aspects that are potentially damaging to CCDs, such as gamma-rays and protons.

7.2.1 Types of radiation

The two types of radiation that this work will be focussing on are protons and gamma-rays. Protons are the nuclei of hydrogen atoms and have a positive charge association. Due to their mass they are less easy to deflect compared to electrons causing them to have a lower penetrating range, typically, a few centimetres in air. Gamma-rays and X-rays on the other hand are energetic, short wavelength electrometric waves or photons. They are identical in nature but have different names due to their origins. Gamma-rays originate from nuclear interactions whereas X-rays originate from charged particle interactions. They are both lightly ionising and highly penetrating. Unlike protons they do not leave any radioactivity within the material after they have interacted (Holmes-Siedle 2002).

7.2.2 Radiation environments

There are many radiation environments in existence on earth both man-made and natural. However, the environment of interest here is the radiation environment found in space.

7.2.2.1 Space environment

In general there are three main sources of radiation in the space environment. First is trapped radiation, this is energetic particles trapped within the earth's magnetic field creating the 'radiation belts'. Secondly, low flux energetic heavy ions extending to TeV in energy in the form of cosmic rays. Lastly, solar flares; these originate from solar eruptions and consist of energetic protons with a small contribution of alpha particle, heavy ions and electrons (Holmes-Siedle 2002).

Detailed accounts of the different radiation types can be found in (Smith(a) 2003), where more specific citations of works can be found. Additionally, more general information on this subject can be found in (Holmes-Siedle 2002) and (Srour(a) 1982).

7.2.2.2 Radiation belts

The radiation belts, discovered by Van Allen in 1958 (Van Allen 1959), are regions of trapped particles formed along the Earth's magnetic field lines. They consist of trapped electrons and protons which spiral in opposite directions around the magnetic field, shown in Figure 7-1. Characterisation of this type of radiation is essential for devices in orbit in these regions (Smith(a) 2003).

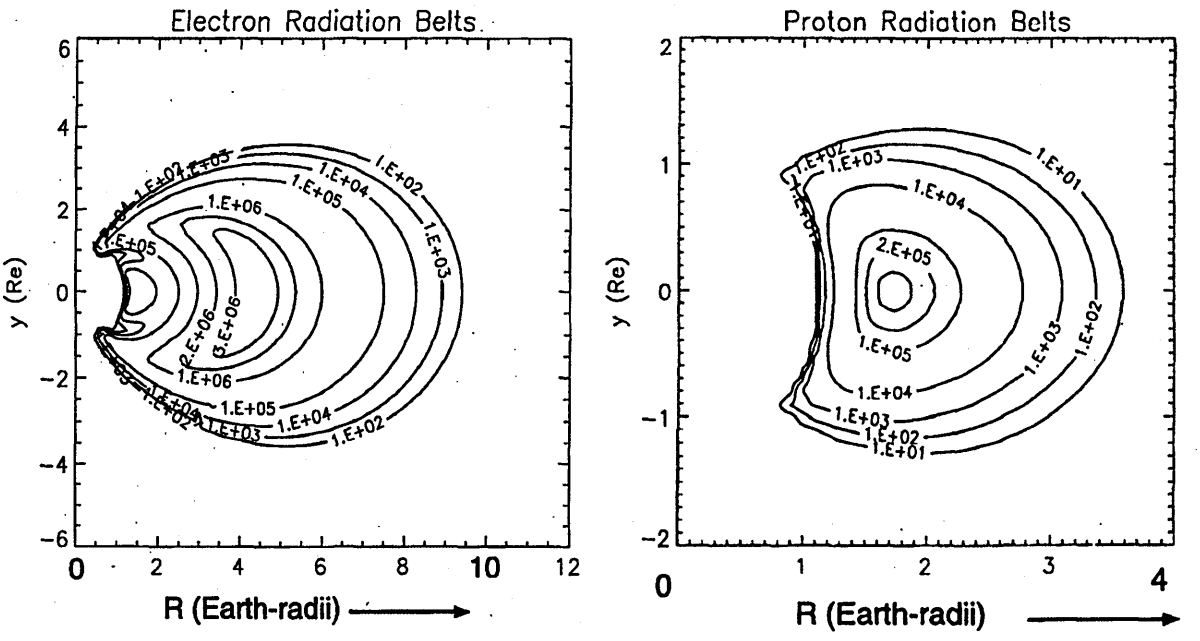


Figure 7-1. Radiation belts around the Earth's magnetic field, showing the number of particles per sqaure centimeter at different earth radii (Daly 1996).

7.2.2.3 Cosmic rays

The predominant type of cosmic ray experienced within the solar system is Galactic cosmic rays (GCRs), these cosmic rays originate from with the Milky Way and are comprised of 85% protons, 14% alpha particles and 1% heavier nuclei (Holmes-Siedle 2002). The source of these particles is still not definitive; however the current theory is that the particles are accelerated by supernova remnants until a point where their energy increases enough to free them (Koyama 1995). In addition to GCRs there are also Solar Cosmic Rays (SCRs) and Terrestrial Cosmic Rays (TCRs). SCRs are produced during a solar flare event where solar material is accelerated to high velocities. The principal cosmic ray observed on the Earth's surface is the TRC, these are cosmic rays that have been transformed from GCRs or SCRs within the atmosphere.

7.2.2.4 Solar flares

Solar wind is the continuous stream of particles from the Sun's chromosphere. During a solar storm, solar flares are emitted and consist of protons, electrons, alpha particles and heavy ions. These particles can be of very high energy and there have been many cases in history which suggest that these events, although not frequent, can create problems where, spacecraft solar cells, single event upsets in electronics and electronic failures on Earth are concerned. A model of the increase in single event upsets during a flare event can be found here in a paper by Adams (Adams 1984). These energetic particles are linked to work carried out in the next chapter, regarding heavy ions.

7.2.3 Effects of radiation

Understandably the range of effects that radiation has on different types of organic and inorganic material is very large. The effects of radiation on MOS-type devises, specifically CCDs, will now be described. To further make this relevant, only effects from gamma-rays and protons will be described as these are the radiation types used for this investigation.

It is important to understand the changes in performance that incident radiation has on a CCD for the entirety of the space mission. The results described in the later sections of this chapter, concentrate on the effects radiation has on EMCCD ageing and dark signal. This understanding can then lead to preventative measures, such as shielding, to ensure no undesirable affects occur.

In addition, the following Chapter describes high LET heavy ion work performed to investigate the effect these particles have with the avalanche phase. Both Chapters 7 and 8 explore the reaction of the EMCCD in a radiation environment as those found in space.

7.2.3.1 Damage mechanisms

There are three main mechanisms that contribute to the effects on CCD devices. The first is ionisation of the lattice electrons of the device, this type of radiation is called ionising radiation. When an electron is liberated from its orbit, a hole is also created; if a field is present the two will move in opposite directions. Secondly and thirdly are elastic and inelastic collisions of particles with the atomic nuclei. The different defects created by the different types are highlighted in Table 7-1. Figure 7-2 shows the path of a charge particle through a CCD with the areas of effect highlighted.

Damage Mechanism	Location	Resulting Defects
Ionisation	SiO_2 below the polysilicon gates (gate dielectric)	Generation of flat-band voltage shift, shifting clock and output amplifier bias signals
Ionisation	Si-SiO_2 interface	Generation of traps at the surface, further increasing flat-band voltage shift and surface generated dark current
Ionisation	Region of charge generation and collection	Transient effects e.g. leading to 'false stars'
Displacement through collisions	Silicon where charge is generated, collected, transferred and measured	Decrease of CTE, Increase in dark current. Increased numbers of bright pixels, dark current non-uniformity and random telegraph signals.

Table 7-1. Different types of damage and their resulting defects (Holmes-Siedle 2002) (Gow 2009).

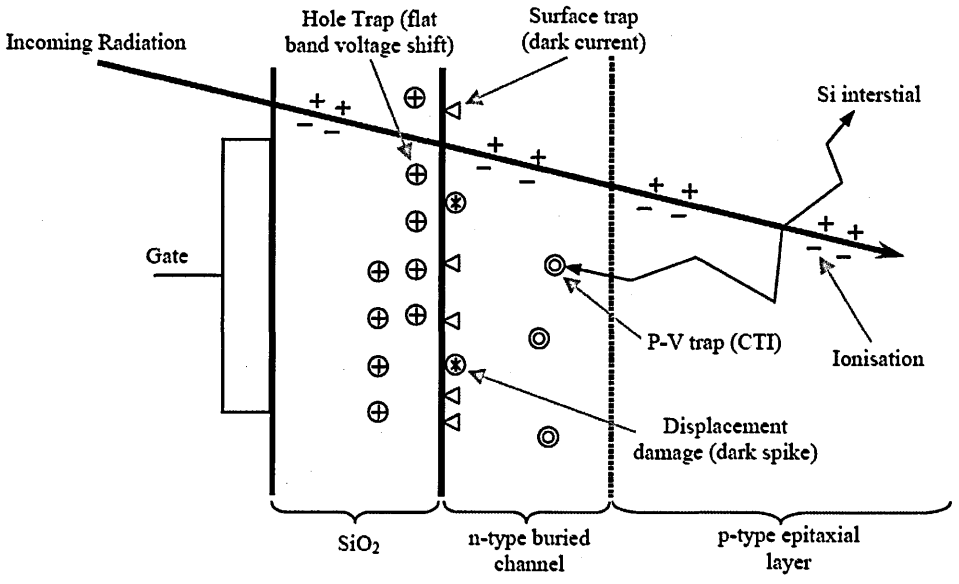


Figure 7-2. The path of a charged particle through a CCD, showing its effect as it travels (Janesick(a) 2001).

Much more detailed descriptions of the types of radiation damage and the effect on MOS type devices and other electronics can be found in (Srour(a) 1982) and (Srour(b) 1988). These reports provide an extremely detailed account on the subject, for the purposes of this chapter it is not necessary to provide such a full explanation. Brief descriptions on ionisation and displacement damage will now be given.

7.2.3.2 Ionisation damage in CCDs

In MOS type devices damage occurs when electron-hole pairs are generated in the dielectric by the ionising radiation; from this two problems arise. Firstly, due to their low mobility, holes will become trapped within the dielectric causing a flat-band / threshold voltage shift, ΔV_{FB}. This causes potentials on the clocks and output amplifier gate to shift in the positive direction (Janesick(a) 2001) (Hopkinson(b) 1992). This can become particularly problematic if the shift goes beyond a critical value, causing the device to no longer efficiently transfer to the output node. The potential well at the output node is created by Vrd which does not experience a flat-band shift therefore once the other clocks fall below this; transfer will stop as shown by Figure 7-3.

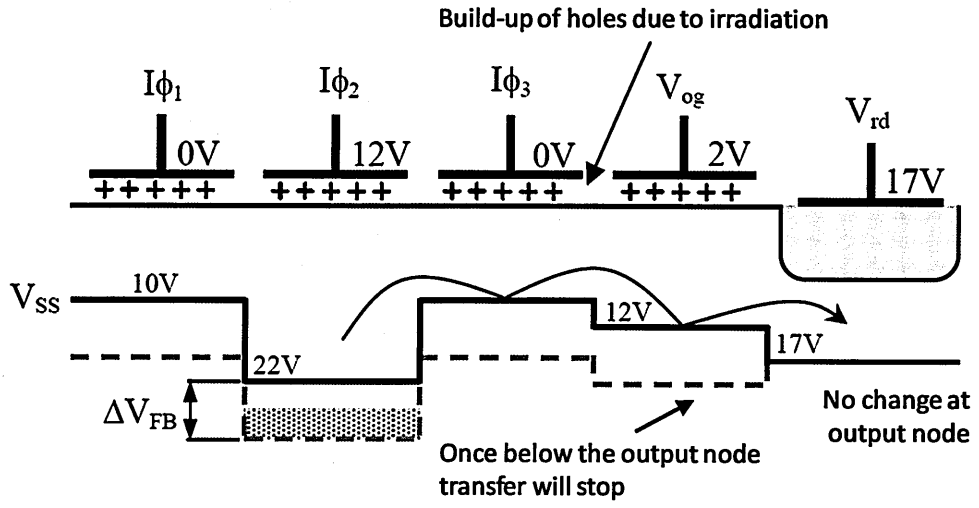


Figure 7-3. Schematic of the clock levels after a flat-band shift (Gow 2009).

Secondly, ionising radiation can break down weak bonds at the Si-SiO_2 interface, creating interface states. This can generate additional flat-band shift and surface dark current. As shown later in this chapter ionising radiation can have a big effect on the amount of generated dark signal (Hopkinson(a) 1991).

7.2.3.3 Displacement damage in CCDs

Displacement damage occurs during collisions between energetic protons, neutron or heavy ions and the silicon nuclei. Known as the 'primary knock-on' this is when the energetic particle displaces the silicon nucleus. If this nucleus has sufficient energy it can then go onto displace other nuclei creating a cluster defect. The result of a displacement is a vacancy and an interstitial atom, known as a vacancy-intestinal pair and depicted by Figure 7-4.

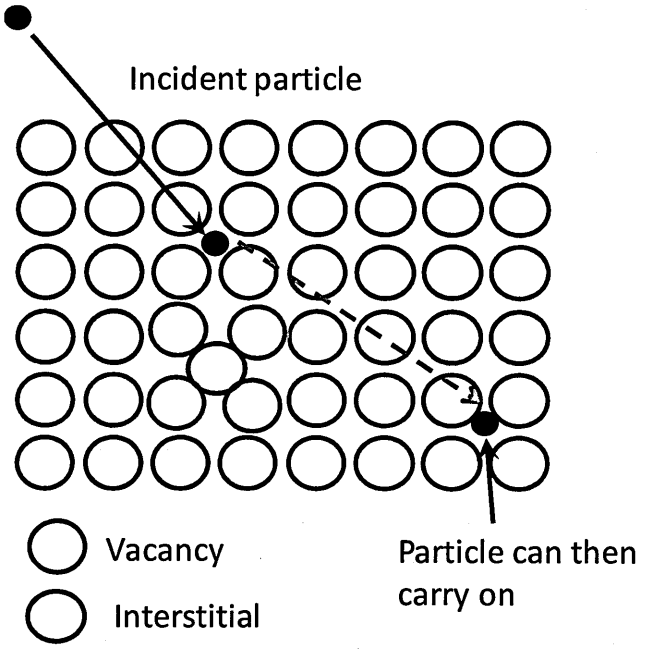


Figure 7-4. Schematic of the process of displacement damage.

This damage can result in an increase in CTI, dark current generation and CCD noise performance (Murowinski 1993).

7.3 Radiation effects in EMCCD technology

The focus of this investigation is to experimentally show performance changes of the EMCCD with regards to gamma-ray and proton irradiation. The primary performance trait that will be looked at is how the radiation affects EMCCD ageing. Secondary traits such as increasing dark signal will also be explored.

7.3.1 EMCCD gamma-ray study

Several CCD97s were taken and passively irradiated with gamma-rays (Cobalt-60) at the European Space Research and Technology Centre (ESTEC).

7.3.1.1 Setup

The devices were passively irradiated, with all pins shorted, therefore no complicated setup, in terms of electronics, was required. Six devices were taken in total, 2 unconditioned and 4 that had already undergone various amounts of ageing. The devices

were simply mounted at varying distances away from the source (depending on the required dose) and withdrawn when their allotted time was up. Figure 7-5 shows a picture of the mounted devices.

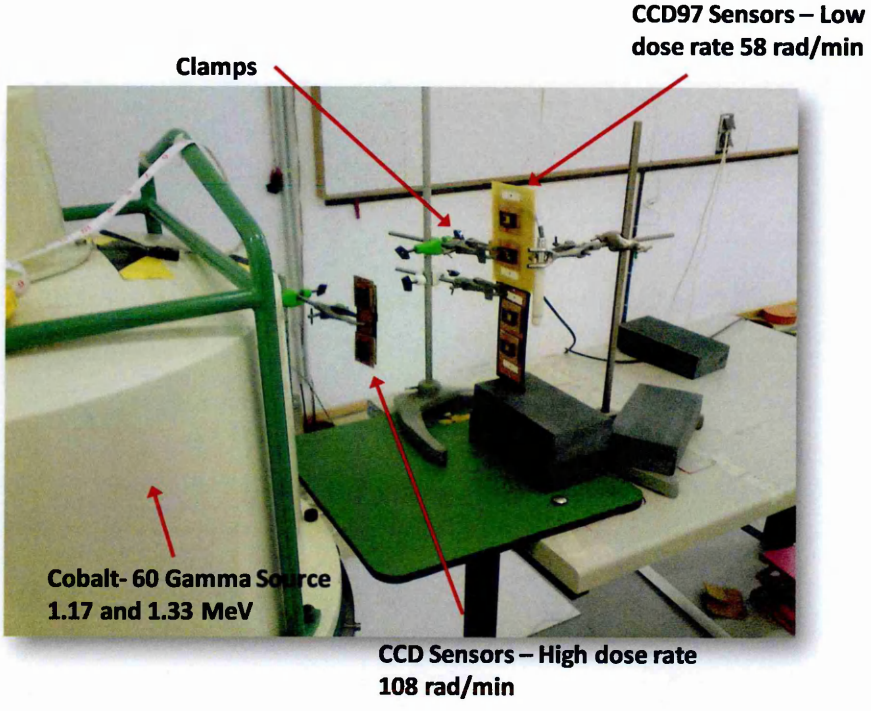


Figure 7-5. Experimental setup of gamma irradiation at ESTEC.

7.3.1.2 Results

The ageing of two unconditioned devices were pre-characterised before being irradiated at the facility. The number of available unconditioned devices is limited therefore it was decided that in order not to risk damage to the devices they would only be irradiated at the lower dose rate of 52 rad/min. Other, already-aged devices were also being testing, for dark signal purposes; at both 52 rad/min (07033-22-25 & 07033-22-17) and 108 rad/min (07033-22-24 & 07033-22-12). Unfortunately, the two devices irradiated at the higher 108 rad/min did not operate once they were installed for post-irradiation testing. Although it may appear that the high dose rate may have been the cause, it appears unlikely that this dose rate would cause this failure. Another possibility is that these two devices were transported in a different case to the other 4 and therefore may have

received a disturbance during transit. Fortunately however, these devices were not vital to the study and the 2 unconditioned devices operated well. Figure 7-6 and Figure 7-7 show the ageing observed before and after irradiation, device 07033-22-06 experience a total dose of 10 krad and device 07033-22-10, 20 krad. It was hypothesised that the amount of dark signal produced by a post-irradiated device would create difficulties when trying to measure gain; therefore, cooling eliminating the dark signal solved this. The data was taken at -45°C, at an avalanche potential of 43V, using an LED and the method described in Chapter 5.

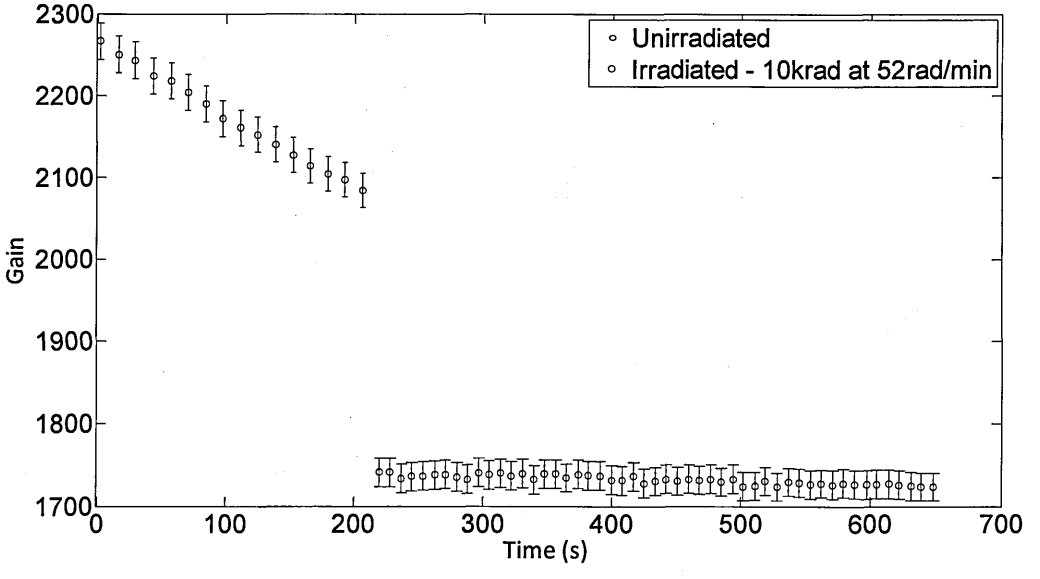


Figure 7-6. Ageing observed before and after gamma irradiation of 10 krad, RΦ2HV = 43V.

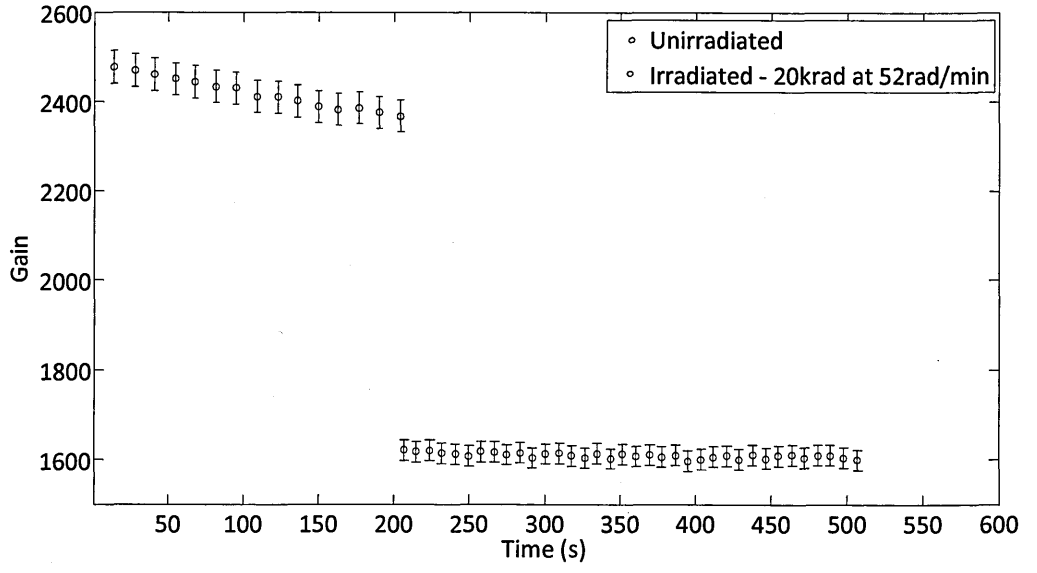


Figure 7-7. Ageing observed before and after gamma irradiation of 20 krad, RΦ2HV = 43V.

Since these devices showed a large change in gain a control device was also measured, however this particular control did not make the same trip to the Netherlands as the irradiated devices. Figure 7-8 shows this control device, it had been left for 6 months between pre and post testing.

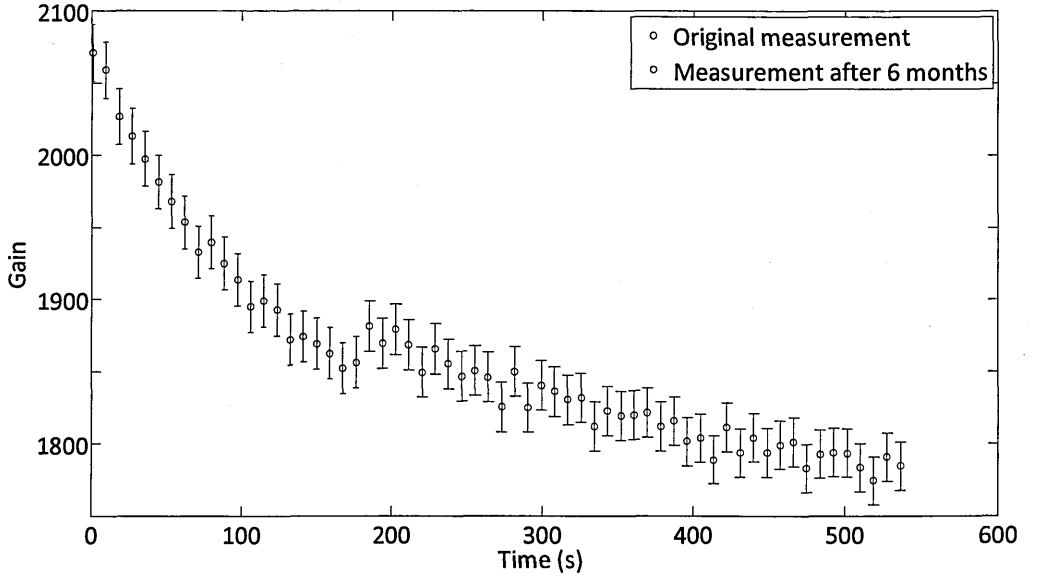


Figure 7-8. Control device comparing the ageing trends with a gap of 6 months, RΦ2HV = 43V.

These results indicated that the gain produced by the avalanche multiplication process decreases after a gamma irradiation, it is also suggesting that the rate of ageing decreases. The time between pre and post testing was approximately 4 – 6 months therefore the control was also left for this amount of time to ensure a fair result, however the control didn't go to ESTEC. The possible reason behind this gain loss will be discussed later however the result was unexpected. The use of a control which had not followed the exact same procedure (apart from the irradiation itself) as the irradiated devices called the result into question.

Therefore the result prompted another experimental run in order to repeat the peculiar results. An additional three unconditioned devices were taken to Brunel University for a gamma irradiation. The proposal was to irradiate one device at a dose of 10krad, to act as a direct comparison to Figure 7-6 above, the second device was to acquire a dose of 1krad, this was to see whether or not even with a small dose the rate of ageing would decrease, this was to see whether a small dose might be used in production in order to stabilise the ageing without overly damaging the device. Finally, the third device was a control that underwent everything the other devices did except for the irradiation.

Unfortunately, the 1krad device failed before it could be post tested. The reason for the failure is unknown; the device did not output an image when tested. This was particularly problematic as there was no longer enough time to re-take the data as this irradiation run was performed in September 2012. Unlike the irradiation at ESTEC the device was transported in the same case and experienced the same conditions as the other devices. Figure 7-9 and Figure 7-10 show the new irradiation results, the operating conditions were similar to the previous results with the devices operating at -35°C and at an avalanche potential of 43V.

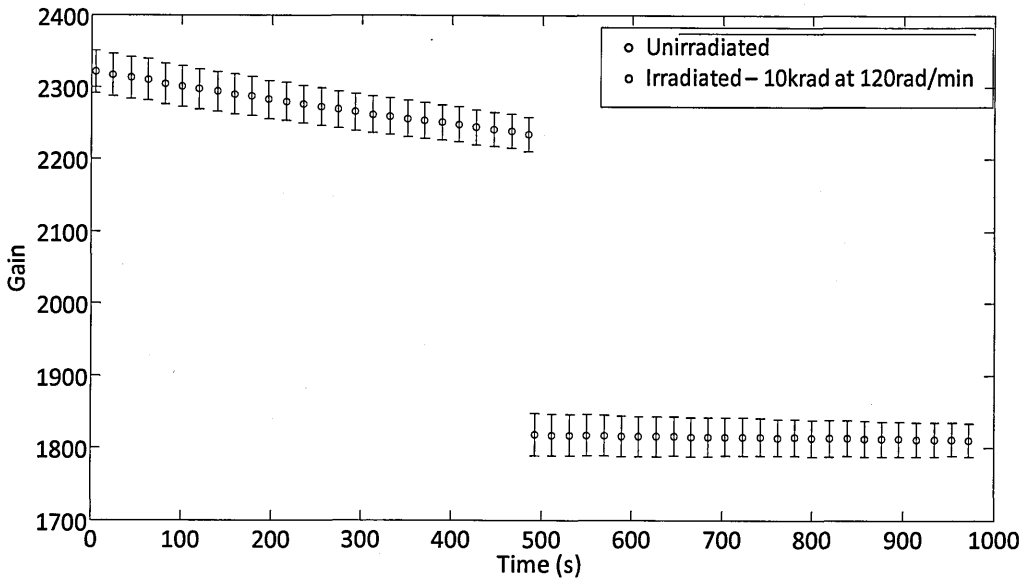


Figure 7-9. Second run of a 10 krad gamma irradiation showing the ageing before and after, RΦ2HV = 43V.

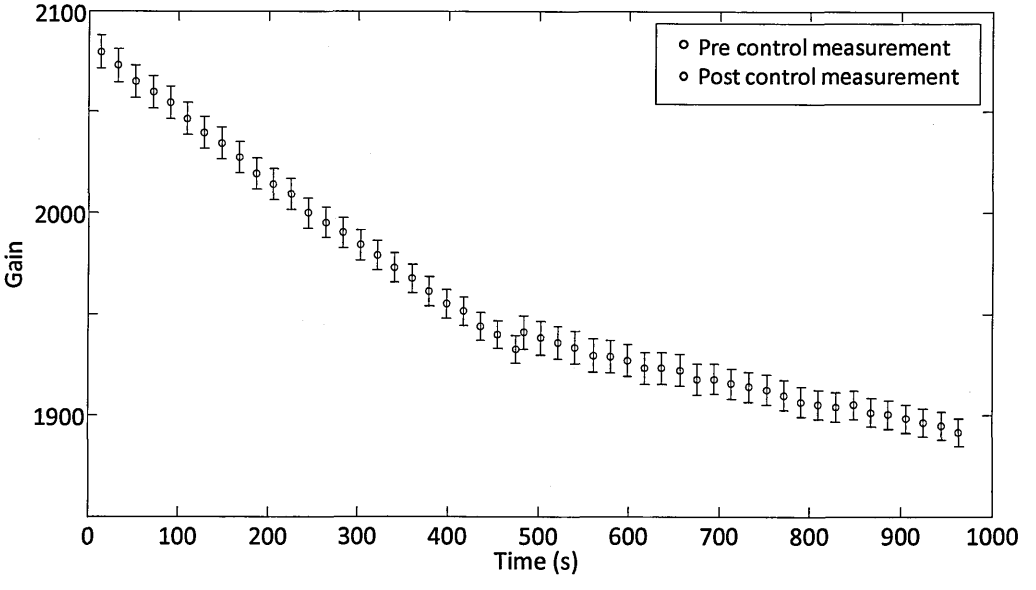


Figure 7-10. Second control device, time between pre and post is aproximately 4 days, RΦ2HV = 43V.

This repeat shows that the result of decreasing gain following a gamma-ray irradiation is repeatable and something within the device is occurring during irradiation that is causing a reduction in avalanche gain. Possible reasons for this are as follows, however a concrete reason is yet to be uncovered. The flat-band shift observed in unbiased devices during

irradiation is approximately 20 – 40 mV/krad and > 50mv/krad for biased (Hopkinson(b) 1992). This would indicate that the shift observed for these devices is approximately 400 – 800 mV for the 20krad case and 200 – 400 mV for the 10krad case. This flat-band shift observed is lower for unbiased devices because the lack of field permits the generated electron hole pairs a greater chance to recombine before the creation of a positive state. The value in flat-band shift and the amount of gain lost for each case seems consistent with the amount of gain that would be lost, Figure 4-17, if one were to decrease the avalanche potential by manually reducing RΦ2HV. An explanation of why this is the case is a reason yet to be discovered. However there seems to be some localised flat-band shift where a greater shift is occurring under ΦDC compared to RΦ2HV causing the potential difference between the two to change; perhaps through there being a local potential minimum established by the ageing and hole accumulation.

In addition to these results some secondary dark signal measures were taken, this was done to show the predicted increase and to and justify why room temperature gain measurements were not feasible. Figure 7-11 and Figure 7-12 show plots of integrated dark signal within the avalanche and serial registers. Unlike Chapter 6 where only ΦDC was biased, here integration took place under RΦ1. Due to the great contrast seen in the signal levels, and in order to suitably display them on a single plot the measurements taken pre-irradiation have an integration time of 1s, and the post-irradiation measurements have an integration time of 50ms and 100ms. The operating temperature of the devices was approximately 28°C.

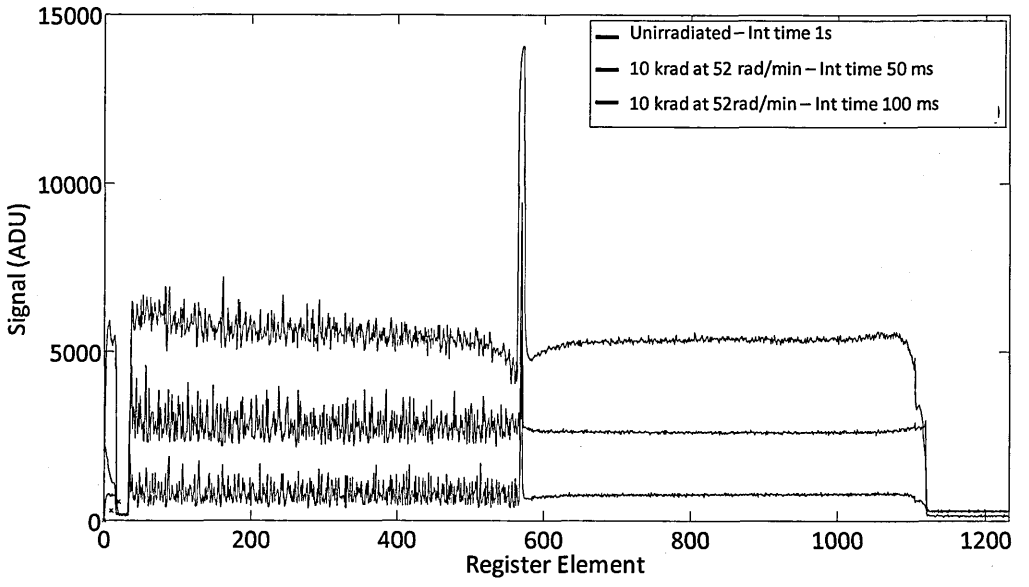


Figure 7-11. Dark signal integrated within the avalanche and serial registers for a 10 krad dose.

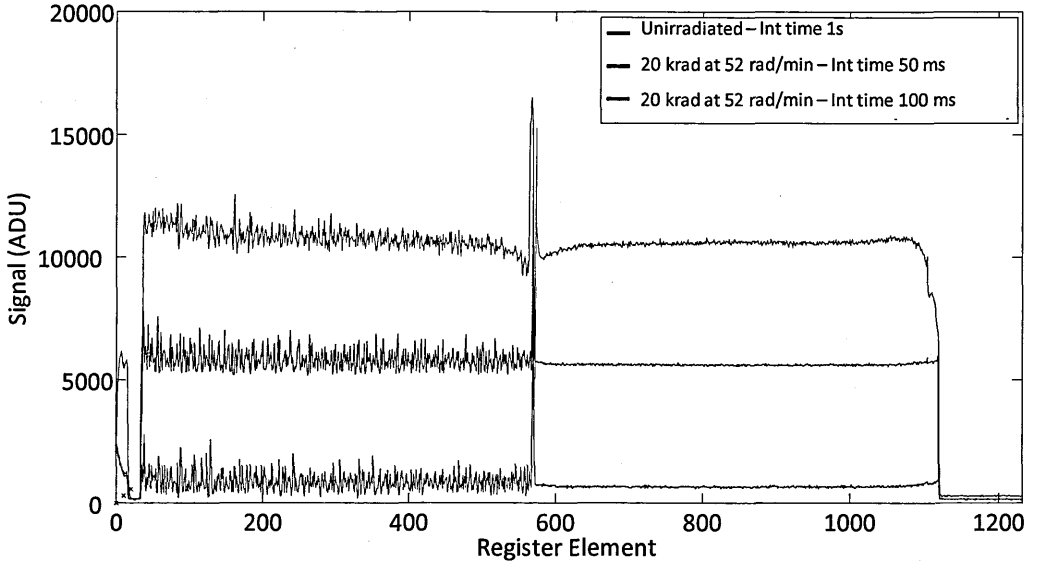


Figure 7-12. Dark signal integrated within the avalanche and serial registers for a 20 krad dose.

The anomalies found at the centre and on the edges of the registers are explained in Chapter 4 and are seen to be present in all results.

The reason for the large increase in dark signal is due to ionising radiation destroying the weak bonds at the Si-SiO_2 interface causing surface dark signal to increase as described previously.

Dark current rate of change is shown to increase linearly with both integration time and dose as shown by Figure 7-13 and Figure 7-14 respectively. Figure 7-13 was calculated by measuring the average across the mid-sections of the serial and avalanche registers register elements as to exclude the anomalous results observed. The errors were calculated from the standard deviation of mean.

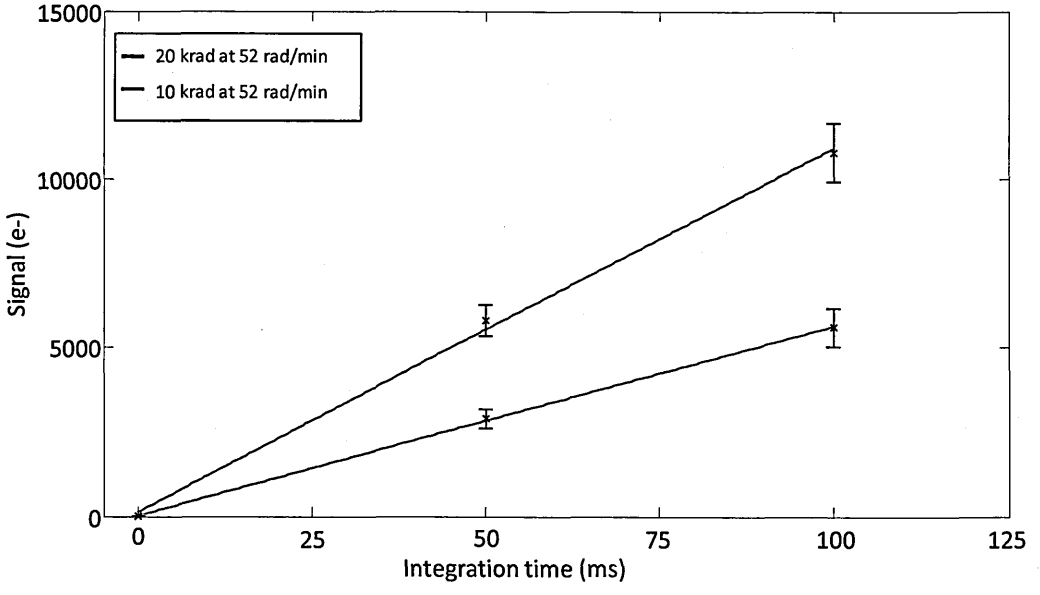


Figure 7-13. Signal dependence on integration time and dose.

The origin of Figure 7-14 was pinned to zero with the assumption that there is no dark current increase with zero irradiation.

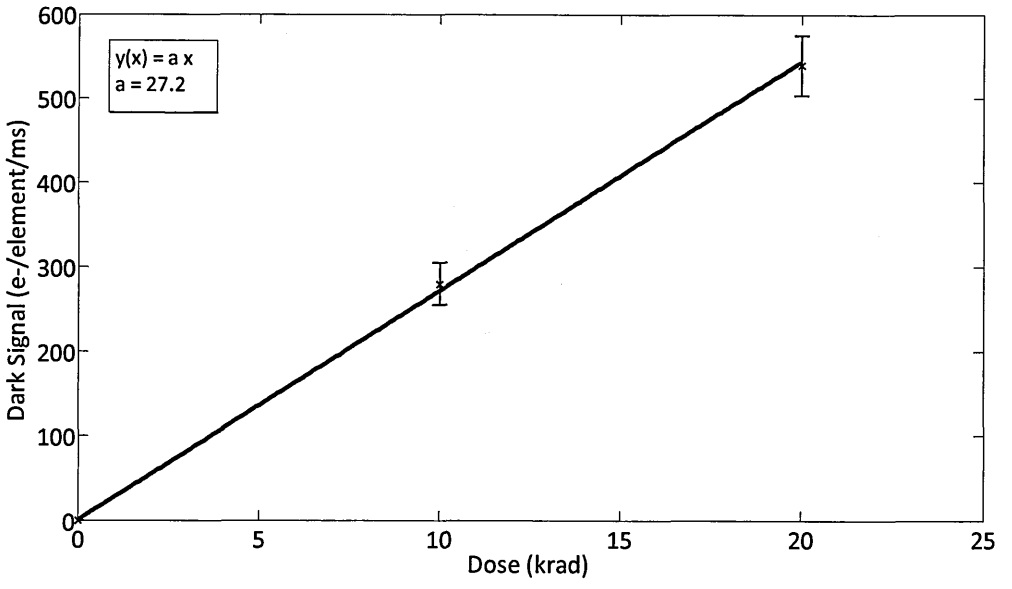


Figure 7-14. Dark signal as a function of dose.

From this plot the rate at which the dark signal increases in the device with integration time and dose is approximately 27 e^- /ms per krad.

7.3.2 EMCCD proton irradiation study

In addition to the gamma study, some devices that had undergone a proton irradiation were also investigated. In this case however, the irradiation itself was undertaken at Brunel University with the results already published (Smith(b) 2006). Two CCD97 devices were loaned to The Open University for this experiment in order to give an initial, simple, before and after proton irradiation comparison of EMCCD ageing. The devices loaned are labelled as device 04073-14-13 and 04073-14-14 and were in batch 11 from the above study. The devices were irradiated for 91 seconds and received a proton fluence of, 1.95×10^{10} protons/cm^2 and a 10MeV equivalent fluence of, 2.03×10^{10} protons/cm^2.

7.3.2.1 Results

Prior to irradiation the devices had undergone a gain characterisation; the measurements were then repeated post-irradiation. Due to the increase in dark signal directly after

irradiation the avalanche potential could not be increased past 38V due to image saturation (Smith(b) 2006). Figure 7-15 and Figure 7-16 show the gains achieved with devices 04073-14-13 and 04073-14-14 respectively. The original testing did not explore the ageing however in addition to the original data further data was taken once the devices were received at The Open University. An initial gain run was measured using the ATE, the devices were then left to age and subsequent gain curves taken.

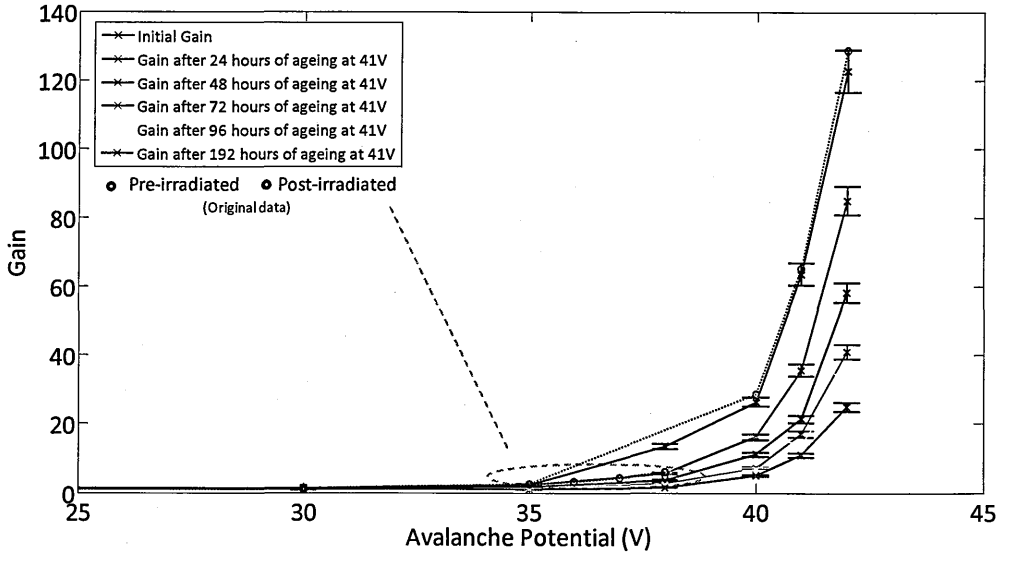


Figure 7-15. Gain curves for device 04073-14-13, before and after proton irradiation.

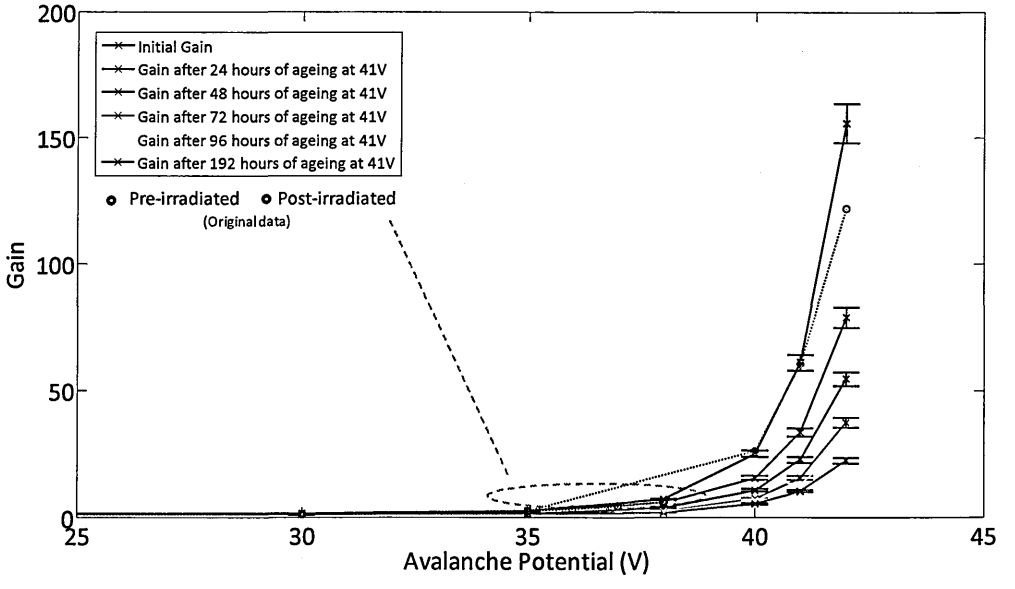


Figure 7-16. Gain curves for device 04073-14-14, before and after proton irradiation.

The original pre-irradiated data and the initial gain measurements taken once the devices were received were similar. As the post-irradiation measurements only have data up to 38V it was difficult to say what the difference was between the two runs. However, it can be said that because it is now possible to take data at higher potentials, compared to directly after irradiation, that some room temperature annealing of the dark current has taken place over the 6 years they have been in storage. Additionally the similarities between the original pre-irradiated measurements and the new initial gains measured at The Open University suggest that the devices suffered little or no damage to their gain mechanism and it was the increase in dark signal that resulted in the inability to properly perform a post test at Brunel.

The gains achieved at 41V were transferred into a plot of gain vs. time. An un-irradiated device was then selected and compared to the two irradiated devices. A third device was selected as a control and so that all devices were approximately at the same stage of the ageing process. This was done by selecting a device that produced similar gains for the same avalanche potential, operating under the same conditions. Figure 7-17 shows the ageing data for the two irradiated devices alongside the un-irradiated control device.

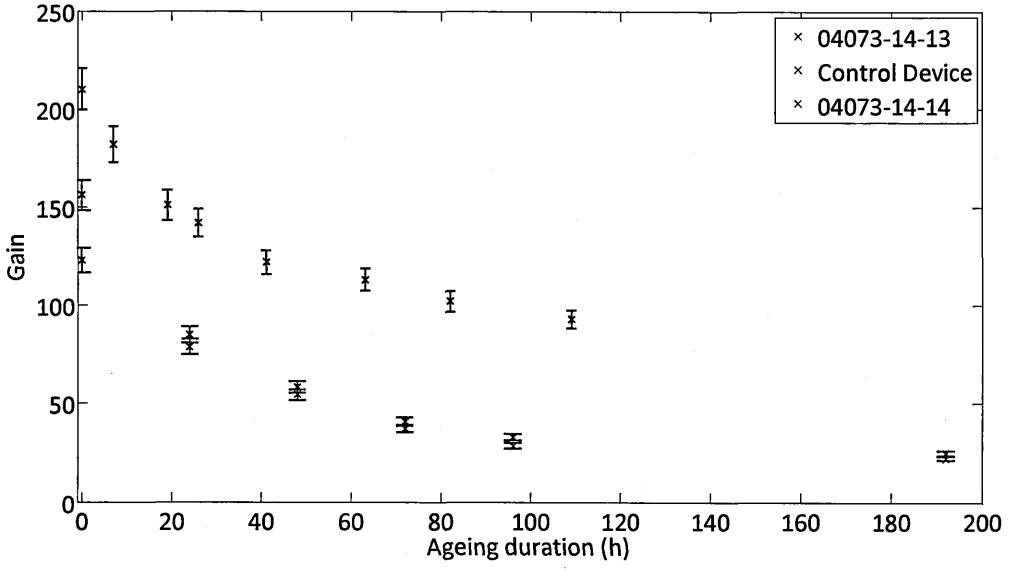


Figure 7-17. Ageing comparison between proton irradiated and un-irradiated control device.

The rate of ageing for the three devices shown in Figure 7-17 up to 109 hours is summarised in Table 7-2.

Device	ΔGain	Time (h)	Gain loss / hour
04073-14-13	122	96	1.27
04073-14-14	89	96	0.93
Control	117	109	1.1

Table 7-2. Summary of results.

The result from device 04073-14-13 shows an increased rate of ageing, by approximately 15% and 04073-14-14 shows a decrease, also by approximately 15%. However I think the gain loss per hour of all devices are approximately the same and fall within the experimental error, proton irradiation seems to have no effect of the gain mechanism and ageing of these particular EMCCDs.

7.4 Conclusion

The gamma irradiation study has shown an effect that has currently an unknown cause. The gain of the EMCCD is observed to decrease between pre and post-irradiation. In addition to this the rate of the ageing is perceived to stabilise. A possibility to the cause of the step change has been attributed to uneven, localised hole build-up during the irradiation caused primary by a potential structure within the device created by the hole accumulation during the ageing.

On the other hand the proton irradiation study has shown that the rate of ageing and gain mechanism itself is not affected by incident protons. The achievable avalanche gain by the devices was limited by the amount of dark signal, however after a lengthy room temperature anneal the subsidence in dark current has allowed for larger gains to be measured. This has been attributed to a dark current annealing process rather than a gain mechanism one. Room temperature annealing is a similar process to conventional annealing where energy is introduced into the system however the process is much slower

Both the gamma and proton irradiation studies have served as a suitable introduction for the work of the following chapter which is the interaction heavy ions have with the high potentials employed by the EMCCD. As a whole, the two chapters will have covered the three main radiation types of concern in the space environment.

Chapter 8: Single Event Gate Rupture in EMCCDs

Single Event Phenomena (SEP) are ionising effects involving microelectronic devices. This work will be using the terminology developed by NASA-JPL, meaning, that the term SEP covers; Single Event Upsets (SEUs), Single Event Latchups (SELs), and Single Event Gate Rupture (SEGR). Other publications may use other terminology where an SEU is used as the general term to describe 'soft' (non-fatal) errors as well as 'hard' (fatal) errors (Holmes-Siedle 2002). This work will explore SEGR for space applications in which they are becoming ever more significant when considering micro-electronic devices with higher density and complexity. The galactic cosmic background and other solar particle events create a prolific source of highly ionising energetic particles which, can cause failures where spaceflight in concerned. SEP can include soft SEU events and hard errors such as, SEGR and SEL (Messenger 1997). The primary focus here is on SEGR with EMCCDs and whether the high fields created by the avalanche regions can cause a fatal error through dielectric breakdown. Currently, the TRL of EMCCD technology is low due to both the ageing effect explained in Chapters 5 and the unknown reaction when the avalanche phase is exposed to a space-like environment. This chapter explores whether the EMCCD can withstand incident heavy ions with high energies and Linear Energy Transfers (LET) whilst operating with high avalanche potentials. No testing of this effect has been done previously and the aim is to contribute to the existing knowledge on EMCCD technology and to increase TRL towards its acceptance in space instrumentation.

The key point when considering hard error SEP is heavy ions, as soft, error-causing protons may not have sufficient energy to irreversibly damage the device. With both of these it is important to consider the Linear Energy Transfer, described in the next section, which is vital for understanding the events. This, together with an overview of the

different types of SEP and new experimental results and conclusion for space-use will be given.

8.1 Heavy ions, protons and Linear Energy Transfer (LET)

A heavy ion is generally considered to be an ionised atom with a mass equal to or greater than that of helium-4; below this it is ionised hydrogen or protons. When one of these energetic ions passes through a semiconductor it leaves behind a column of electron hole pairs from intense ionisation, which can create a highly conductive ion track or plasma channel. The conductivity and charge density of the initial plasma track is proportional to the ionising energy deposited by the incident ion. This energy is the Linear Energy Transfer (LET), measured in $MeV.cm^2/mg$. The further an ion travels through a material the more it loses energy and slows down resulting in greater interaction with the material, leading to an increase in LET. Therefore, generally surface LET (LET observed at the surface of the material) is lower than sub-surface LET. Simulations were performed using 'The Stopping and Range of Ions in Matter' (SRIM) software using the powerful 'Transport and Range of Ions in Matter' (TRIM) tool (SRIM 2012). Figure 8-1 shows the pictorial output of the TRIM tool, it provides a Monte-Carlo simulation of multiple ions illustrated here are Nitrogen (N) at 60 MeV and Xenon (Xe) at 420 MeV. Heavier ions interact more with the material and therefore are more likely to have larger deflection angles and lower ranges.

Nitrogen: 60 MeV

Xenon: 420 MeV

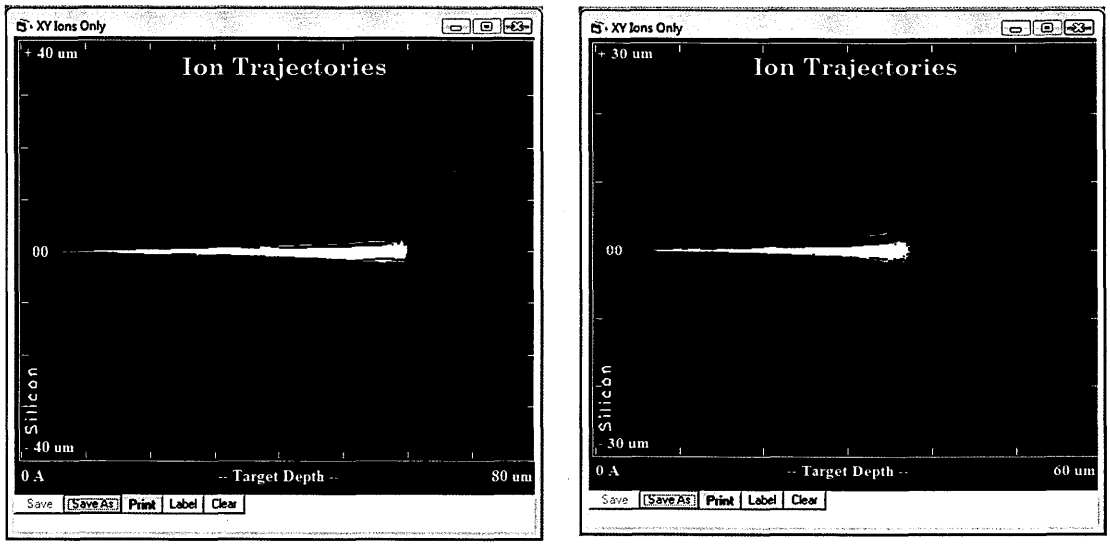


Figure 8-1. Graphical output of TRIM showing the ion paths of N and Xe in Silicon.

Figure 8-2 shows 60 MeV and 30 MeV Nitrogen (N) ions incident normal to the surface of Silicon. This simulation shows that as the ion travels through the different layers of material, 0.1μm of SiO_2 and 60μm of Si, the amount of energy deposited per unit length increases until the ion comes to a stop. Ions of lower energy deposit more energy into the material per unit length compared to more energetic ions of the same species due to rate of interaction with the material. The overall energy deposited however, is less, due to the integrated area under each curve being equal to the particles initial energy.

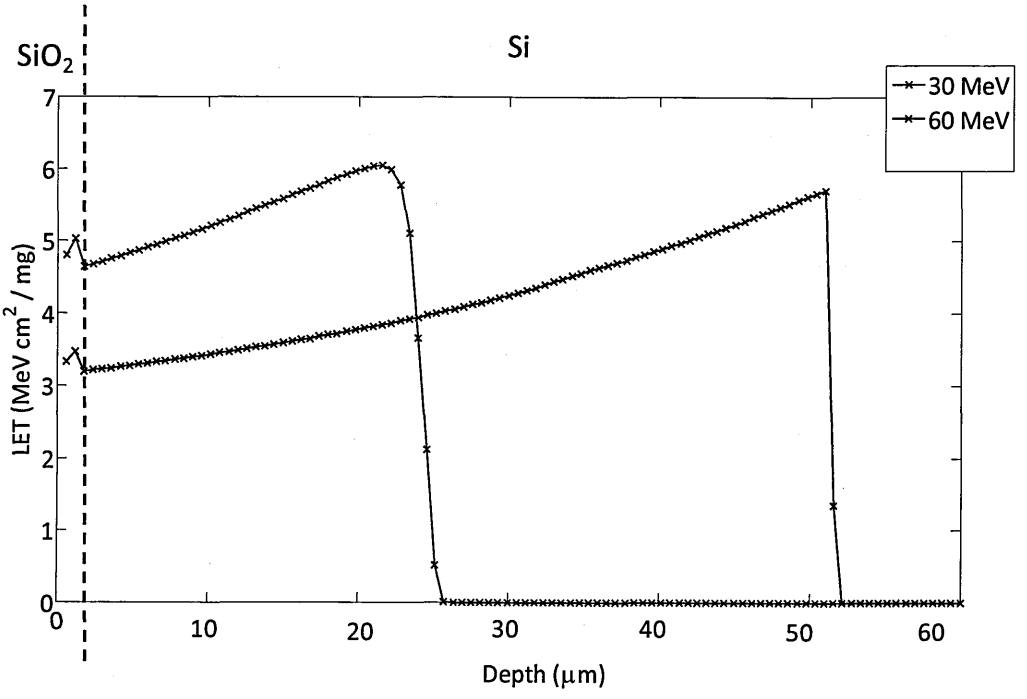


Figure 8-2. Simulated LET dependence on depth in Silicon for Nitrogen.

In this experiment back-illumination CCDs will be used, where the ionising particles have to travel 16μm through Si before reaching the sensitive area. Therefore simulation is vital when planning an experimental investigation of this type. The SRIM software becomes a vital tool enabling an estimate of LET delivered to the oxide layer from the incident particles.

8.2 Overview of single event phenomena

8.2.1 Single Event Upset (SEU)

An SEU or 'soft error' is one that changes the internal logical state of a digital circuit device without causing any permanent physical damage (Johansson 1994). This change can be caused by a heavy ion or incident proton. The ionisation path or plasma channel created by the ion creates a current path across a p-n junction. If the incident ion exceeds a threshold LET or the injected charge exceeds a critical charge, Q_c the sensitive

node can flip from the 'off' to 'on' position or vice versa. This change of state is known as a 'bit-flip' (Holmes-Siedle 2002).

This subject becomes particularly important when dealing with ever decreasing sizes of components as encountered in modern microelectronics. The critical charge needed to initiate the change of logic state decreases with decreasing size. Figure 8-3 (Burke 1985) gives an illustration of how the critical charge Q_C changes with feature size and indicating proportionality.

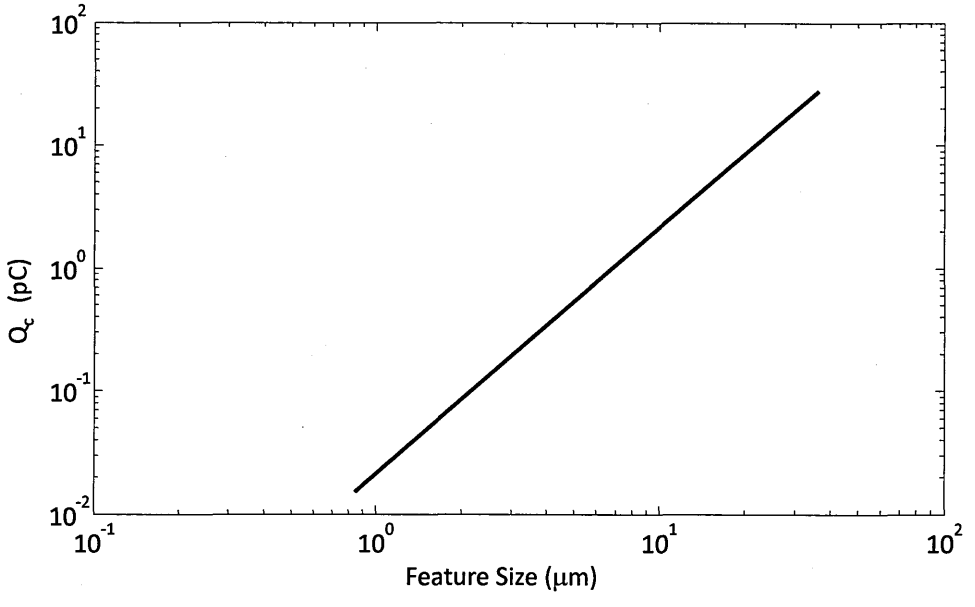


Figure 8-3. Critical charge required for a change of state as a function of components size. Line is a best fit from different types of technology including: nMOS, CMOS-Bulk and CMOS-SOS (Burke 1985).

8.2.2 Single Event Latchup (SEL)

A SEL event is more severe than the previously described SEU and is known as a 'hard' error. Parasitic structures, which are complex semiconductor structures made of up simpler standalone structures, can enter an unwanted mode of operation caused by an SEP event. A Silicon-Controlled Rectifier (SCR) or a thyristor for example under normal operation has high impedance between the cathode and anodes, however with an

incident particle creating a conduction path between the two the SRC can be held in an 'on' position and will conduct as long as there is current (Holmes-Siedle 2002) (The Aerospace Corporation 2011). The device will only return to its original operation conditions once it is reset or the current supply is interrupted which is an inconvenient procedure to undertake for an instrument already in space.

8.3 Single Event Gate Rupture (SEGR)

SEGR is the main focus of this work and may occur when a heavy ion is incident on the gate electrode of an MOS-type semiconductor device. The ion may cause a conduction path in the oxide underneath the gate which can then carry current possibly leading to rupture or damage. Whether the incident ion has this effect depends on the ionisation energy of the particle, the design and state of the semiconductor device and the voltage stresses within the local region (Microsemi 2007).

8.3.1 SEGR mechanism

Once the plasma channel is created by the ion passage, assuming positive gate bias, electrons will flow through the channel towards the gate and build up on the dielectric interface. The e-h pairs initially generated will also radially diffuse from the plasma channel to the surrounding material. Diffusion which occurs within the oxide causes the field to increase. If the field present in the semiconductor during the SEP is greater than a critical field, (dependent upon the breakdown field of the oxide and LET) and if enough charge forms on the oxide interface, the oxide ruptures. Once ruptured a large current flows through the oxide to the polysilicon gate creating a warming effect, resulting in the melting of the polysilicon, dielectric and silicon leading to device failure (Wheatley 1994) (Sexton(a) 1997). Wheatley (Wheatley 1994), Sexton (Sexton(b) 1998), Buruta (Buruta

2001) and Wrobel (Wrobel 1987) showed the dependence of the critical field, E_{crt}, for a power MOSFET with V_{DS} = 0 V with the empirical equation:

$$\mathbf{E_{crt}} = \frac{\mathbf{E_0}}{\mathbf{1+\frac{L}{B}}} \tag{8.1}$$

Where E_0 is the breakdown field of the oxide in MeV/cm, L is the LET in MeV·cm^2/mg and B a fitting parameter. Figure 8-4 is a model created in MatLab (MatLab 2012) of the above equation using a fitting parameter of 53 and E_o = 10 MeV/cm.

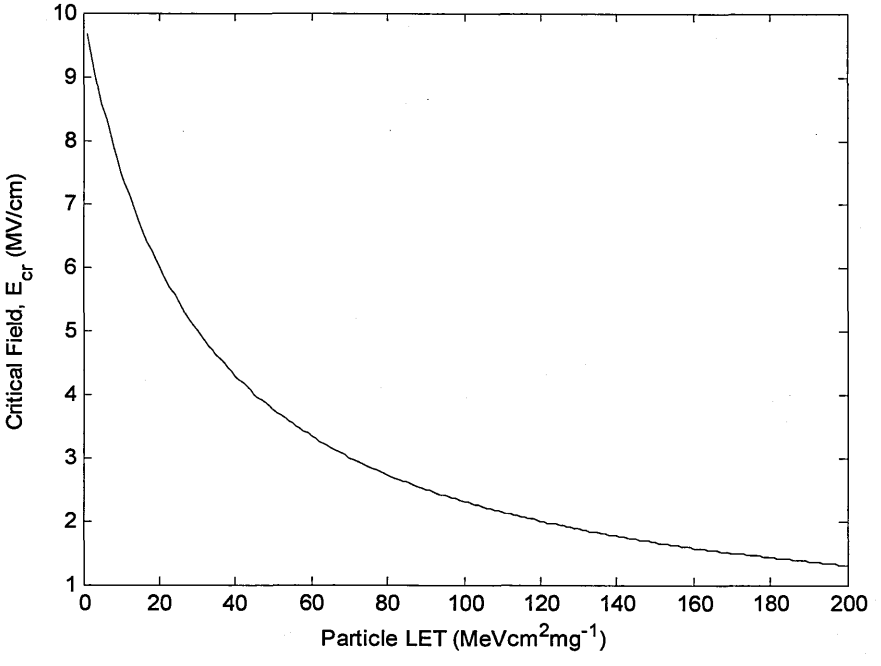


Figure 8-4. Critical field dependence on LET using a constant value of 53 for B and an oxide breakdown of 10 MeV/cm.

It can be seen that as the LET of the incident particle increases, the critical field or the external field required to cause gate rupture decreases. The above model was constructed with a constant value for the fitting parameter B. Table 8-1 shows the values of B obtained by varying authors with different gate oxide thicknesses and different breakdown fields. The CCD97 has an oxide thickness of 85nm therefore should have a breakdown field of 10 MV/cm, this brings it closer to the data obtained by Titus compared

to any other author. Therefore, the value for B obtained by him was used to create the above model. However, for the models in the following sections that will show how susceptible the EMCCD is to SEGR worst/best case scenarios will be demonstrated using maximum and minimum values for B (30-80).

Author	Oxide Thickness (nm)	E_o (MV / cm)	B (MeV cm^2 / mg)
Sexton 1998	6	15	68
Sexton 1998	6.5	15	72
Sexton 1998	12	14.3	53
Sexton 1998	18	13.4	48
Wrobel 1987	45	10.9	62
Wheatley 1994	50	11.1	50
Titus 1995	30 - 150	10	53

Table 8-1. Values of B used in various experiments.

8.3.1.1 Fitting parameter

Attempts by Sexton and Buruta were made at giving a clear physical representation of the fitting parameter B. The two methods differ in technique; Sexton derived B from first principles and Buruta with the use of a model he created. Buruta's method begins by quoting from Wheatley and then showing that for gate rupture to occur the sum of the internal and external fields, E_{int} and E_{ext} respectively have to be greater than the breakdown potential of the oxide E_0. The internal field is generated by the electron-hole pairs created in the oxide that have survived recombination, these charges now increase the field within the oxide. The external field is produced externally by the bias on the gate of the device. The explanation provided by Sexton, gives more detail into the exact

nature and origins of B and derives the equation for E_{crt} in the process. This derivation of the dependence of E_{crt} on the LET is based upon the plasma channel acting like a conducting pipe. It was discussed in Wrobel (Wrobel 1987) that gate rupture occurs in two stages, the first is the formation of the conducting pipe through the dielectric, in the form of a high density plasma channel created by the incident ion. The second step is the discharge of energy stored on either side of the pipe.

8.4 SEGR in EMCCD technology

Due to the high fields present in EMCCD technology it was proposed that an incident heavy ion of sufficient energy could create a conductive path either in the inter-poly oxide (between gates of the CCD) or through the gate dielectric (underneath the gates of the CCD). The motivation of this chapter is to explore SEGR in EMCCD technology and to either confirm or dispel this potential risk.

8.4.1 Gate dielectric SEGR

There are two types of dielectric used by e2v technologies, 'thin' dielectrics which consist of a 40nm silicon dioxide layer and a 40nm silicon nitride layer (40/40) and 'standard' dielectrics which consist of 85nm of silicon dioxide and 85nm silicon nitride (85/85). The electric field perpendicular to the surface for a non-inverted device is independent of the clock high level, and is approximately 500 kV/cm for both the standard and thin dielectrics (Robbins(b) 2010). If run in inverted mode, however, at low clock bias the field increases to 700 kV/cm for the standard dielectrics and 1MV/cm for the thin. Additionally, if an anti-blooming drain is present (biased at 16V), the field in this region is 1.2 MV/cm for the standard and 2.6 MV/cm for the thin (Robbins(b) 2010).

Figure 8-5 is a model created for this investigation similar to Figure 8-4 and shows the predicted field required at certain LET values to cause SEGR for specific CCD design. The

typical breakdown field of the gate dielectric, E_o is 10 MeV / cm. As mentioned before maximum and minimum values for B are used to give an idea of the 'danger area' in which SEGR could occur.

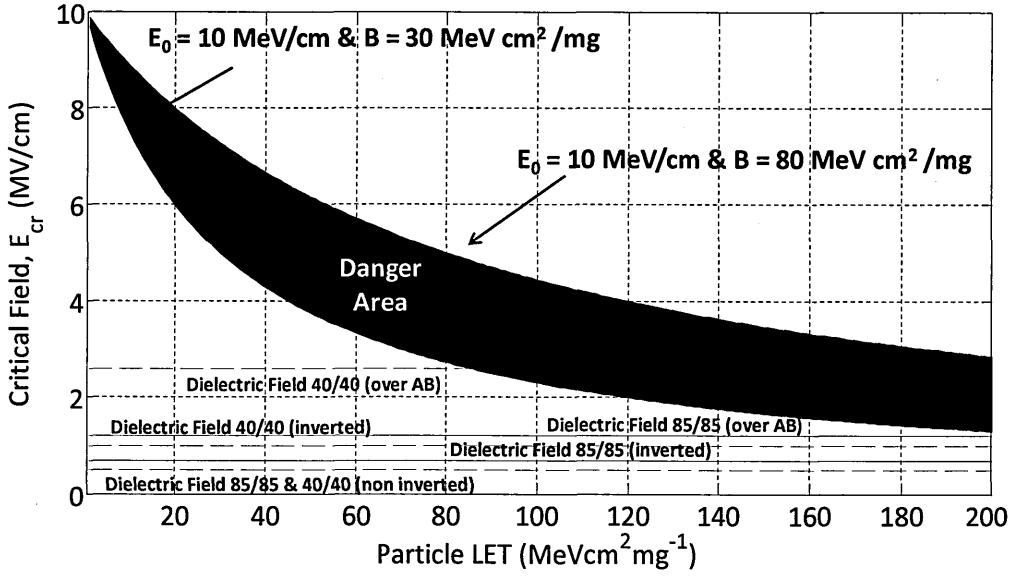


Figure 8-5. Model of gate dielectric SEGR for a standard CCD in various formats, including; inverted/non-inverted mode devices over the anti-blooming (AB) for both standard and thin devices.

From the devices described above only the anti-blooming region on the 40/40 dielectric may cause a problem. The probability of events occurring at or above certain LET values is well known and described later.

In addition to the risk to the oxide beneath the gate, there is a greater risk to the oxide between the gates. This is particularly true for the EMCCD where a relatively high field exists between two adjacent gates where only a thin 150 nm – 300 nm dielectric exists.

8.4.2 Inter-poly oxide SEGR

Inter-poly oxide is the dielectric that exists between the polysilicon electrodes in both the electrode-electrode overlap and bus-line regions to avoid inter-phase shorts. This dielectric, although thicker, has a lower breakdown field compared to gate dielectrics, this is because the crystalline structure formed with the polysilicon creates a 'spiky' structure

resulting in 'field crowding', additionally the inter-poly oxide is low temperature grown compared to the gate dielectric to prevent damage to the polysilicon. The typical breakdown field for the inter-poly oxides is approximately 3 MV/cm^2 and has a mean thickness of 225 nm. For e2v devices, the thickness can vary from 150 nm to 300 nm, this is due to the earlier layers of polysilicon being further oxidised when the later layers are grown, causing them to become thicker. From the basic structure of the device, the effective area for rupture to occur between gates is much lower than between the gate and the underlying silicon. For an ordinary CCD adjacent phases may have a potential difference of approximately 12 V, and an uncertainty in the oxide thickness can give rise to a large different in the field present. A 300 nm oxide with a potential difference of 12 V across it for example, would yield a field of 0.4 MV/cm^2 and for a 150 nm device 0.8 MV/cm^2. Figure 8-6 is a model to show the LET values needed for rupture to occur, the maximum and minimum values of B (30 – 80 MeV cm^2 / mg) were again used.

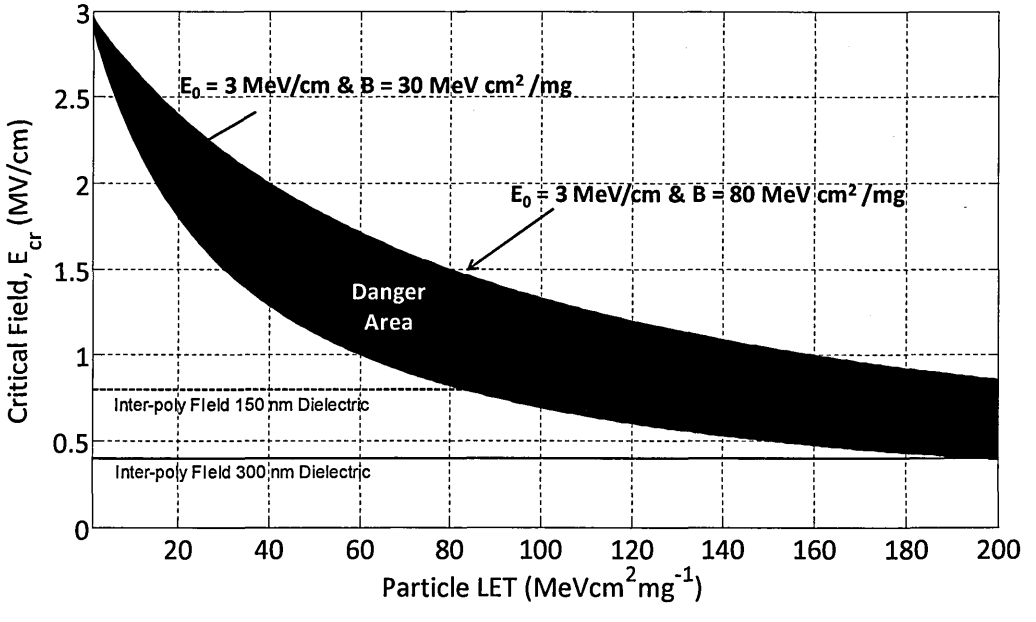


Figure 8-6. Model for inter-poly SEGR for a standard CCD in various formats.

The probability of rupture occurring for a 300 nm oxide is very small as LETs of over 180 $MVcm^2mg^{-1}$ should be required, the exact probabilities of such an event occurring will be shown later. However, the LET needed for a 150 nm oxide failure is above 80 $MVcm^2mg^{-1}$, which is a more probable event. This makes the thinner 150 nm inter-poly dielectric rupture as likely as the thin, 40/40, gate dielectric rupture above AB as shown in Figure 8-5. This model is however quite pessimistic, as in reality inter-poly oxides are likely to be thicker and the range of 150nm – 300 nm is quite large, also the cross section of interaction is very small.

Nevertheless when using EMCCDs there is further cause for concern when regarding inter-poly oxide rupture. An EMCCD has a high voltage phase within the avalanche multiplication register leading to higher inter-poly fields in the region where a gate bias of 40V – 50V may be applied adjacent to a 0V barrier phase. Assuming the same oxide breakdown, values for B and a potential difference of 45V, the fields present for a 300 nm and 150nm oxide are 1.5 MV/cm^2 and 3 MV/cm^2 respectively. These values are again quite pessimistic as 45V on the avalanche phase is the maximum needed to run the device. Nevertheless, Figure 8-7 is a model to show the LET values required for rupture to occur.

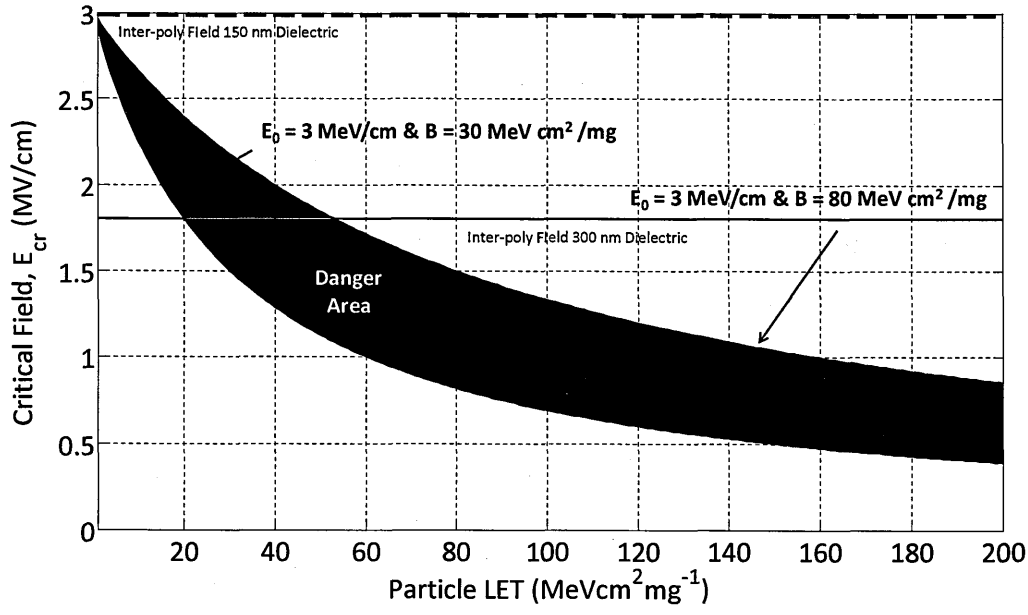


Figure 8-7. Model for inter-poly SEGR for a the EMCCD with an avalanche potential of 45V.

This result shows that for the thinnest of dielectric the inter-poly oxide should already be rupturing with a potential difference of 45 V. However this is of course not the case and the device can be operated beyond this potential without issue. In reality the dielectric is thicker than 150 nm as mentioned before. Despite any uncertainties in these models it was clear that the high voltage phase within a heavy ion environment was cause for some concern and some further investigation was required. To further the investigation, simulation of the possible space environments were created to obtain probabilities of a certain LET occurring.

8.5 Heavy ions in the space environment

In order to calculate the probability of a particle interacting within the device it was necessary to obtain flux values in the space environment for given LETs. The readily available Space Environment Information System from ESA allows quick and easy modelling of space environments at varying orbits (ESA(b) 2011). Figure 8-7 is a model created for a silicon device at an L2 orbit with varying thicknesses of aluminium shielding.

It shows the total fluence for a 5 year mission and the number of particle incident over a square meter for various LETs.

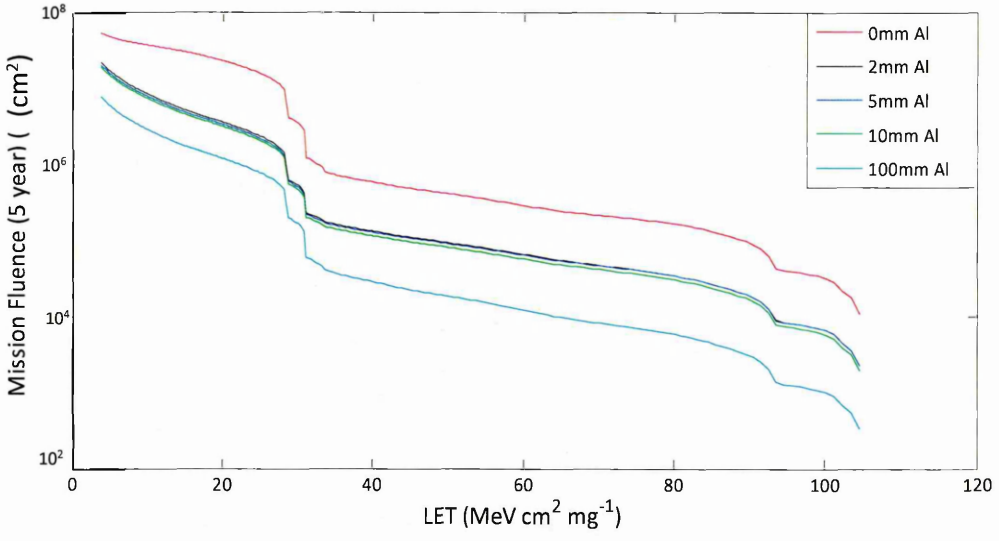


Figure 8-8. Total fluence over a 5 year period of incident heavy ions at L2 through various thicknesses of Al shielding.

8.6 Testing for SEGR in EMCCD technology

To fully test the models and space worthiness of the EMCCD regarding heavy ions, several CCD97s were taken to the Heavy Ion Facility (HIF) at the CYClotron of LOuvain la NEuve (CYCLONE) in Belgium. A total of 14 devices were taken for testing.

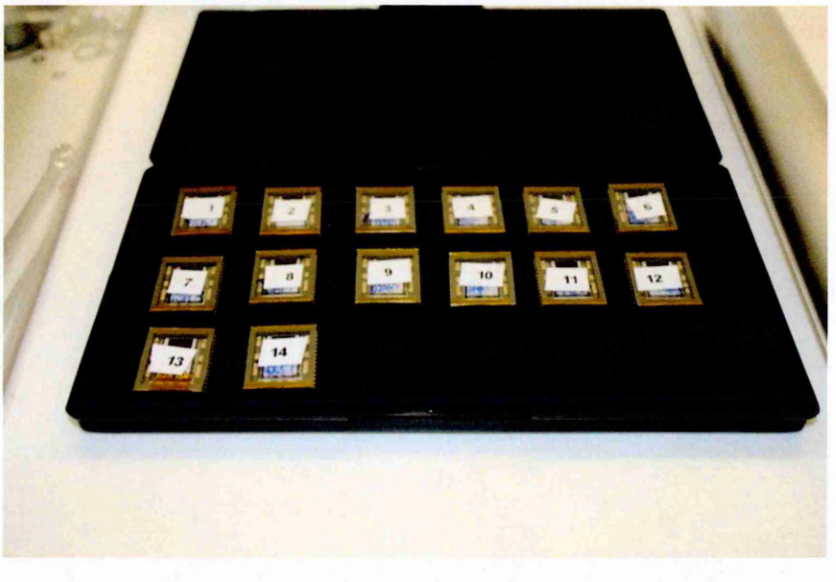


Figure 8-9. Fourteen CCD97s ready for testing at the HIF in Louvain.

8.6.1 Method and Setup

The principal aim of the experiments was to expose the devices to conditions that would represent the worst case scenario; this would determine whether SEGR was an issue. The experimental method was relatively simple; an initial device was exposed to the highest LET that was available from the HIF, if SEGR was observed than a critical LET (the LET were the devices would fail) would be found using the other 13 devices by varying the LET of subsequent runs. Figure 8-10 shows a single device mounted in the setup. An aluminium shield was used to cover the headboard and parts of the CCD that did not have a high voltage component, the avalanche multiplication register was the only part of the EMCCD that was exposed to the ions.

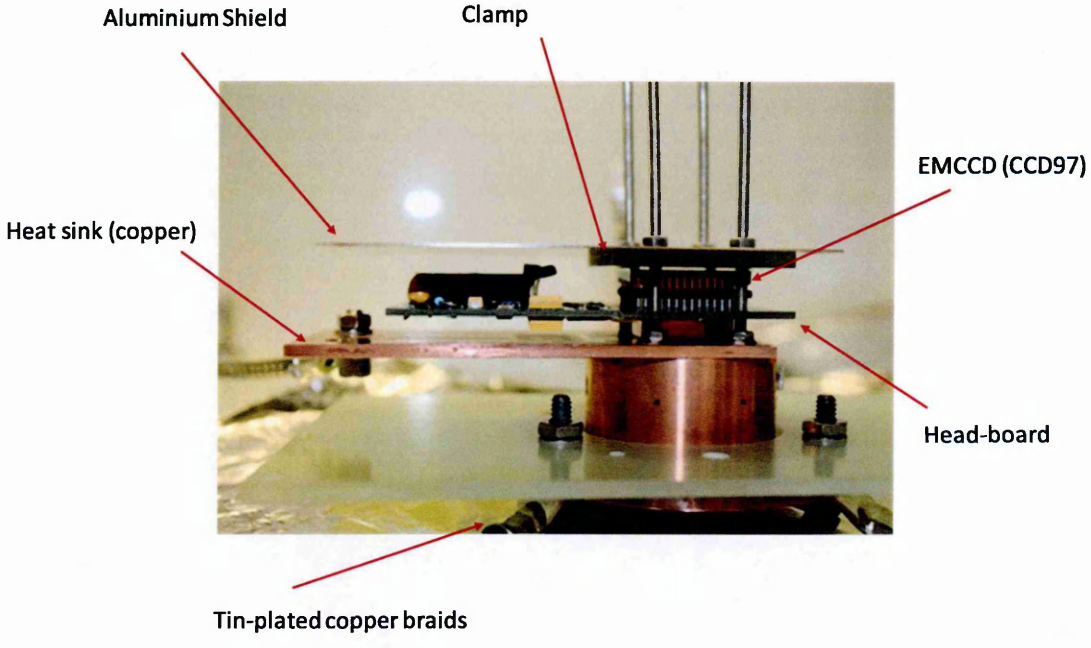


Figure 8-10. CCD97 mounted onto testing setup.

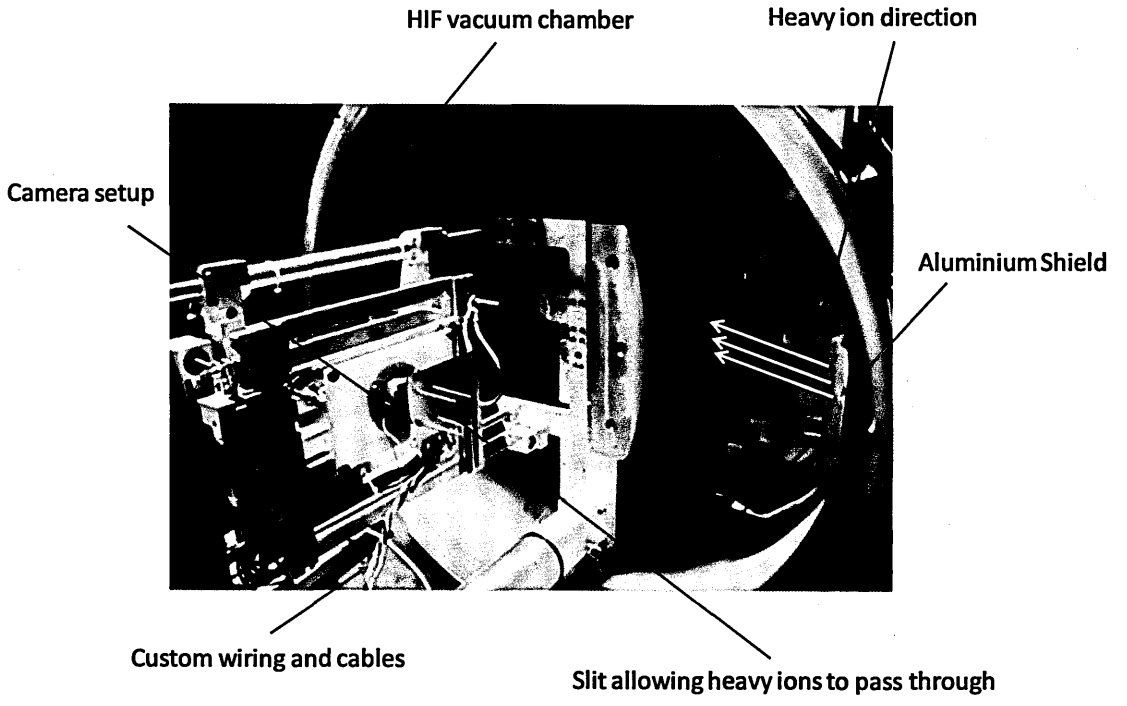


Figure 8-11. Camera head mounted onto the HIF vacuum system ready for testing.

It was anticipated that the signal produced by the heavy ions would be much larger than the generated dark signal; therefore, it was deemed not necessary to actively cool the device. It also proved difficult with the setup at the HIF, therefore tin-plated copper braid was used to couple the device to the chamber to act as a heat dump and move excess heat away from the CCD. The CCD temperature was monitored using a PT1000 attached to the ceramic of the device; the temperature of the CCD did not exceed 28°C during testing.

8.6.2 Frame acquirement

A new device clocking sequence was developed for this experiment; the image area and serial register were both 'dumped' using the dump gate present on the device. The avalanche multiplication register was continuously read out with no integration time, Figure 8-12 shows the schematic of the image and serial dumping and gain register read-out processes.

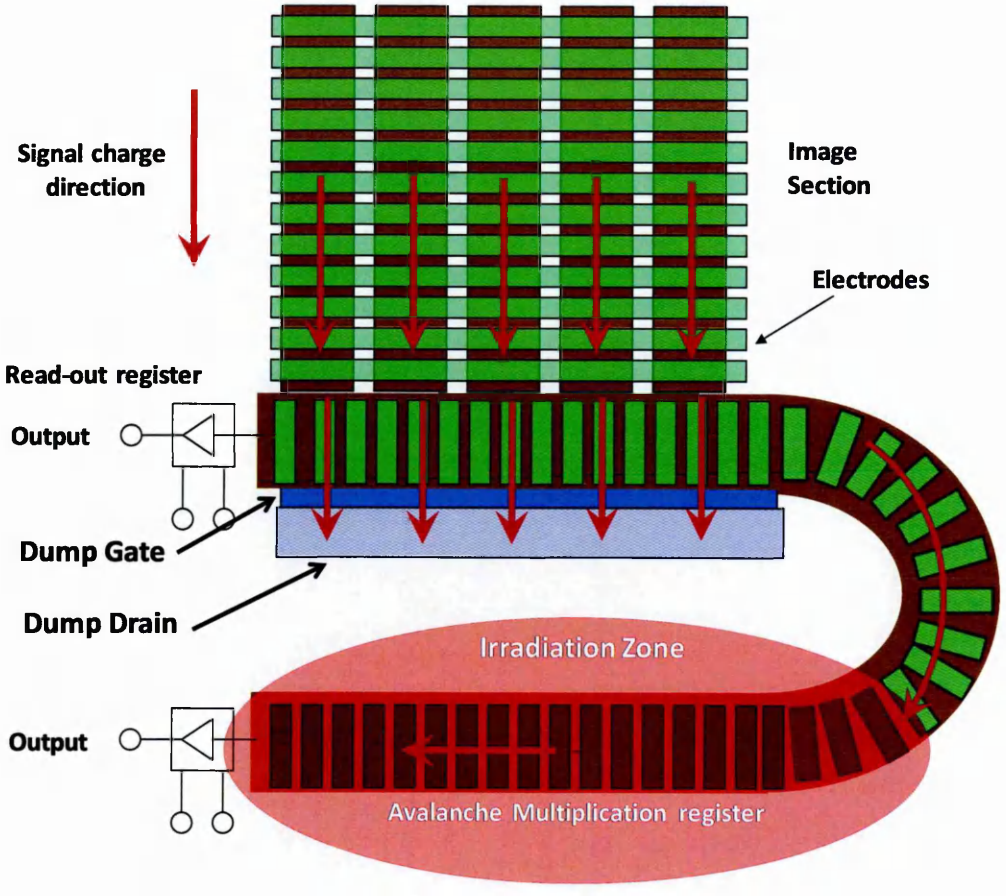


Figure 8-12. Schematic of read-out method used in reading out the SEGR setup, where the image charge was dumped; leaving only signal from the gain register.

The Dump Gate (DG) shown above was held at a high bias throughout the testing to allow any charge that was integrated within the image area or serial register to clear out into the drain. Both the avalanche register and the ordinary register were continuously clocked to allow real-time observation of events.

The device was exposed to heavy ions for 50s for each frame of data; the CCD was continuously read-out to capture live events and possible SEGR. Each frame consisted of approximately 18×10^6 pixels (1232x15000) and was read out at 350 kHz. The high speeds and method of transfer allowed the camera to operate with minimal dark signal at room temperature. This read-out method was chosen because it allowed real time measurements of changes and the count of particles or photons incident onto the device. This was perfect for the SEGR experiment as it would allow for any SEGR events and the

status of the device before and after to be observed. As an addition, the continuous read-out of the avalanche register allowed for an unusual test of the system. The frequency of the lighting at the HIF was used as the initial test to determine whether the device was working correctly. By calculating the rate of the intensity change and the taking into account read-out rate, the frequency of the lighting was found to be 48.3Hz which is consistent with the mains frequency. Figure 8-13 shows a sample from the test image taken at the HIF.

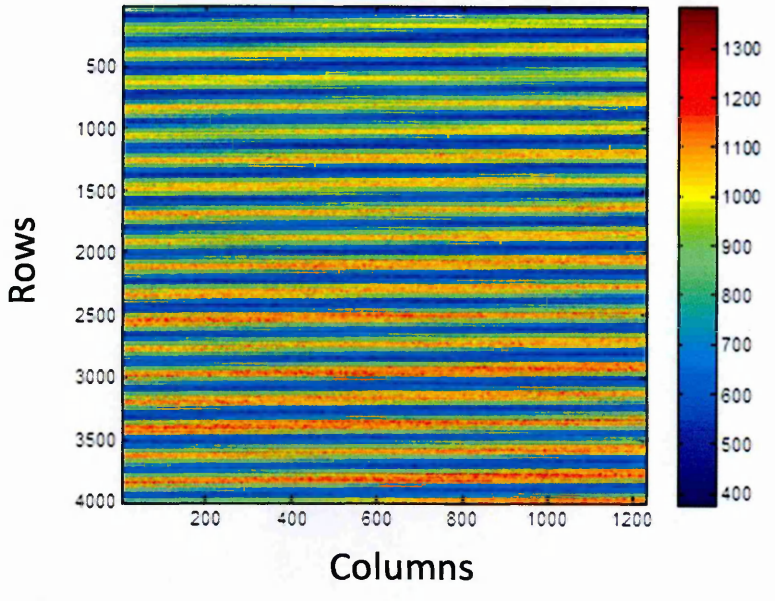


Figure 8-13. Image taken with laboratory light incident onto the device showing the frequency of lighting being imaged using a continuous readout method.

8.6.3 Ions and LET

Table 8-2 shows the different ions available at the HIF with the simulated LET using the SRIM software at both the surface of the device and 16 μm. Back-illumination devices were used, therefore to reach the electrode structure the particles have to penetrate approximately 16μm of silicon. As described in 8.1, the LET changes as the ion travels thought the material and the predicted LET at the gate structure had to be estimated from modelling using the SRIM tool.

The available ions at the HIF formed two 'cocktails' one being a high penetration option and the other a high LET option; the latter type being the most obvious choice for our aim. Extensive simulation using the SRIM software was undertaken to identify the LET and ranges of the ions; Nitrogen (N), Neon (Ne), Argon (Ar), Krypton (Kr) and Xenon (Xe).

Ion Species	Energy (MeV)	LET at Surface (MeV cm^2 /mg)	LET at 16 μm (MeV cm^2 /mg)	Range (μm)
Nitrogen	60	3.3	3.6	52
Neon	76	6.5	7.2	46
Argon	150	16.0	17.6	41
Krypton	305	42	40.2	41
Xenon	420	72.2	58.8	39

Table 8-2. Ions used for SEGR testing on the CCD97s.

8.6.4 Results

With heavy ions incident normal to the surface and penetrating a depth 16 μm in Silicon the highest available LET at the HIF was 58.8 MeV cm^2 /mg. The first CCD 97 was exposed to this LET at different flux levels and avalanche multiplication potentials. Table 8-3 shows a summary of the initial results obtained from this high LET, as a function of increasing EM avalanche phase voltage.

Type: Xenon $^{17+}$, Energy: 420 MeV , LET: 58.8 MeV cm^2 /mg, normal to the surface, SS at 0V and 4.5V					
Test Run	**Flux (particles/s/cm^2)**	**Related avalanche gain register flux (particles/s)**	**Exposure Time (s)**	**Avalanche potential (V)**	**SEGR**
1	500	1.7	30	40	No
2	1000	3.4	30	40	No
3	10000	34	30	40	No
4	10000	34	30	41	No
5	10000	34	30	42	No
6	20000	68	30	41	No
7	20000	68	30	43	No
8	20000	68	30	44	No
9	20000	68	30	45	No
5	20000	68	30	47	No

Table 8-3. Initial testing run for SEGR.

Figure 8-14 shows the image taken with the device on run 6. The frames above this avalanche potential were saturated due to the higher gains. The heavy ion events in the image 'streak' across many pixels as the signal exceeds the limits at which the gain register delivers good CTE.

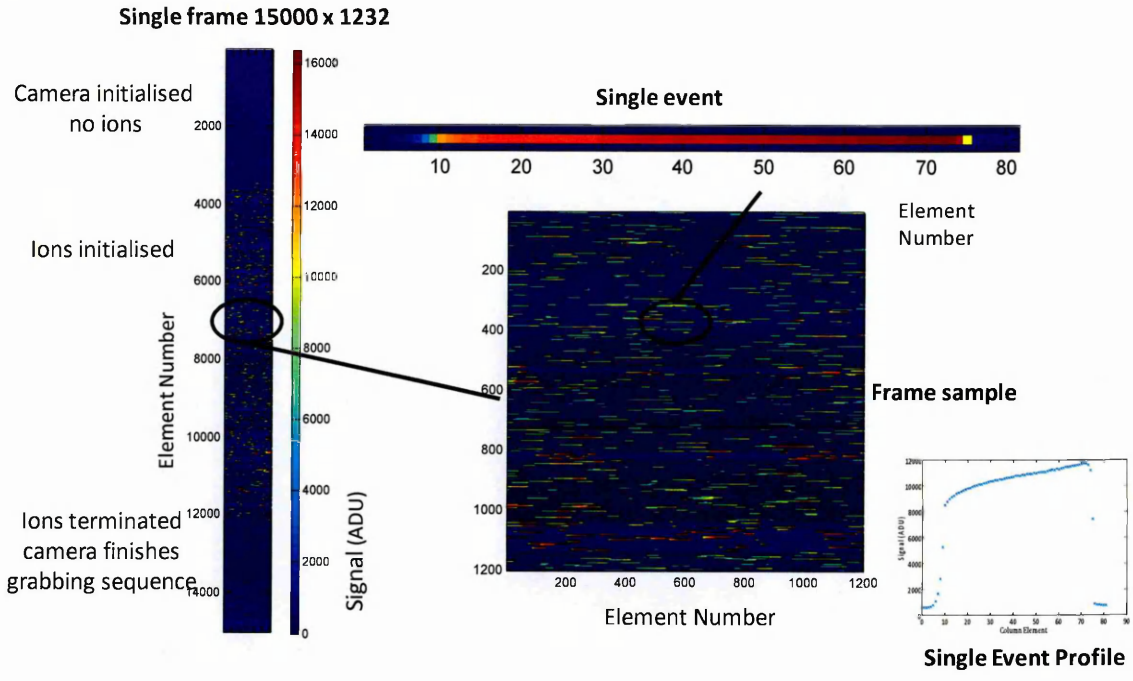


Figure 8-14. Image taken of Xenon at an avalanche potential of 41V.

It became clear after this initial test that the CCD97 was not incurring catastrophic gate rupture and was continuing to function. In an attempt to induce SEGR the avalanche potential of the gain register was further increased beyond the manufacturing specified safe level up to 53V. At this level the dark signal was saturating the ADC and therefore no information could be gained from the frame. The avalanche potential was therefore switched during readout from 41 V to the desired potential and then back to see if the device was functioning after exposure with the high avalanche potentials. Figure 8-15 shows an image taken using this method and Table 8-4 shows a summary of these results.

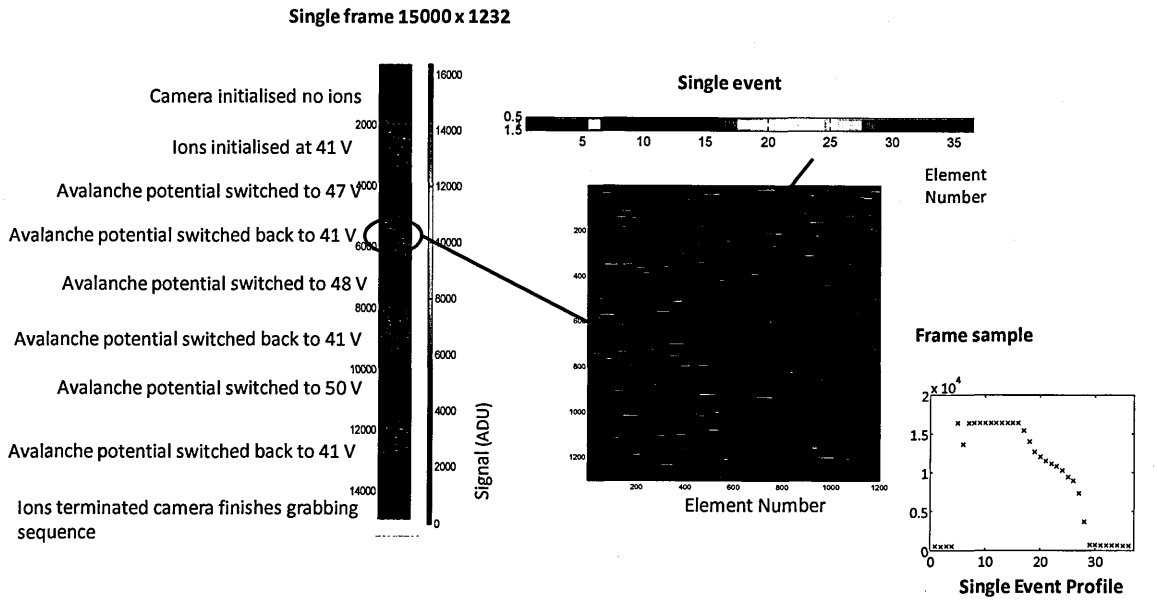


Figure 8-15. SEGR testing with extreme potentials, switching to a lower voltage of 41V to enable any changes to be seen as at high potentials ADC saturation was observed.

Table 8-4 shows the results obtained from this latter method developed whilst at the beam-line at Louvain.

Type: Xenon $^{17+}$, Energy: 420 MeV , LET: 58.8 MeV cm^2 /mg, normal to the surface, SS at 0V and 4.5V					
Run	**Flux (particles/s/cm^2)**	**Related avalanche gain register Flux (particles/s)**	**Exposure Time (s)**	**Avalanche potential (V)**	**SEGR**
1	10000	34	30	41, 47, 41, 48, 41, 50	No
2	20000	68	30	41, 50, 41, 51, 41	No
3	20000	68	30	41, 52, 41, 53, 41	No

Table 8-4. Results observed from SEGR testing using the switching method.

Initially the experimental plan was to only expose the device to ions normal to the surface giving us a maximum LET of 58.8 MeV cm^2 /mg at 16 μm (depth of the gates). However, if exposed at various angles to the surface the LET can vary. This was not originally planned due to the uncertainty in the fact that our sensitive region is extremely thin compared to

the rest of the device and varying the angle can introduce many uncertainties. Nevertheless as the CCD97 was not failing it became a final option to try and cause SEGR. The maximum angle produced by the HIF was 60° providing an apparent LET of 135 MeV cm^2 /mg. Also due to the angle the maximum flux produced by the HIF was reduced from 20,000 particles/s/cm^2 to 10,000 particles/s/cm^2. Table 8-5 summarises these results.

Type: Xenon $^{17+}$, Energy: 420 MeV , LET: 135 MeV cm^2 /mg, 60° to the surface, SS at 0V and 4.5V					
Run	**Flux (particles/s/cm^2)**	**Related avalanche gain register Flux (particles/s)**	**Exposure Time (s)**	**Avalanche potential (V)**	**SEGR**
1	10000	34	30	41, 52, 41, 53, 41	No
2	10000	34	30	41, 54, 41	No

Table 8-5. SEGR results observed at 60 degrees.

8.6.5 Discussion

The main aim of this investigation was to see whether the EMCCD is susceptible to SEGR when exposed to high LETs. It was successfully shown that no signs of permanent failure were present. Higher avalanche potentials were considered; however 54 V was reaching the limits of the electronics on the headboard and, in reality, devices will never be run at this kind of potential. A possible reason for the device not failing could be down to the size of the sensitive region. At maximum flux the avalanche multiplication register received 68 particles per second; approximately a quarter of this register is the high voltage phase (approximately 17 particles incident on high voltage phase per second) and even smaller still is the overlap area between electrodes. If left for a longer period of time, longer than our time restraints at the HIF, and with a higher flux, then rupture may still be possible. However, when compared to an L2 orbit that generates approximately

10^6 heavy ions per cm^2 over 5 years with an LET of 60 MeV cm^2 /mg, it seems that the fluxes tested of 20,000 particles/s/cm^2 at 58 MeV cm^2 /mg and 10,000 particles/s/cm^2 at an apparent LET of 135 MeV cm^2 /mg at 60°, were sufficiently high. The absence of SEGR, although unexpected was a positive one, a reason for this tolerance to heavy ions was then investigated. The gate overlap regions within the avalanche gain register were explored; this was originally performed to get an estimate of the size of the sensitive region however a more interesting result emerged.

8.7 Gate overlaps

For efficient transfer the gap between electrodes should be as small as possible. To get ever decreasing distances between electrodes is difficult therefore CCD manufacturers use an overlapping electrode structure as shown schematically by Figure 8-16.

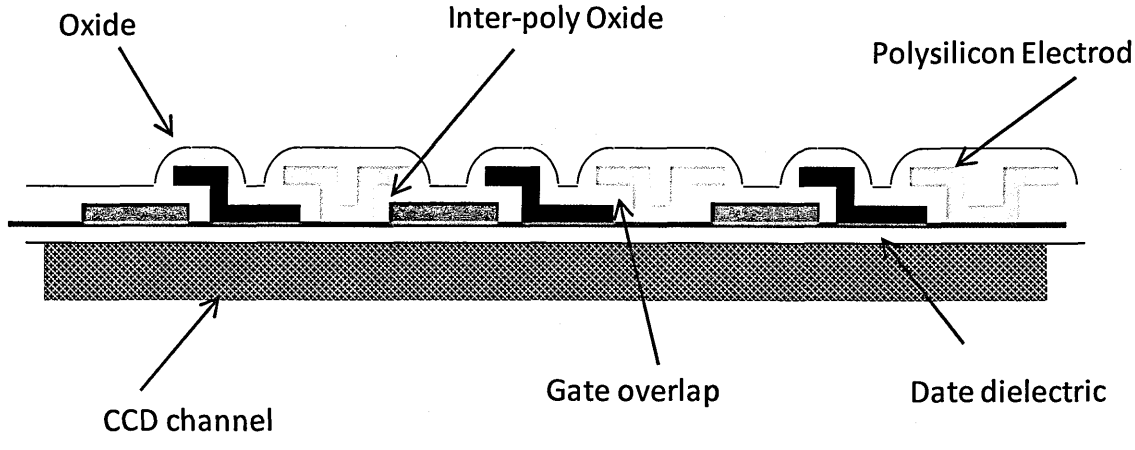


Figure 8-16. Gate overlaps, constructed with different layers of polysilicon sandwiched in oxide.

In order to explore the gate overlaps on the CCD97 a device was imaged in a Scanning Electron Microscope (SEM), the testing chamber is shown in Figure 8-17. Initially a Focussed Ion Beam (FIB) cut a trench in the silicon, more specifically across the avalanche gain register. The SEM was then used to image the cross section in order to view the gate overlaps. Figure 8-18, Figure 8-19 and Figure 8-20 show a small sample of

the images produced. It is difficult to point out which electrode is which from these images however the important aspect here is that the overlaps themselves are not as expected.

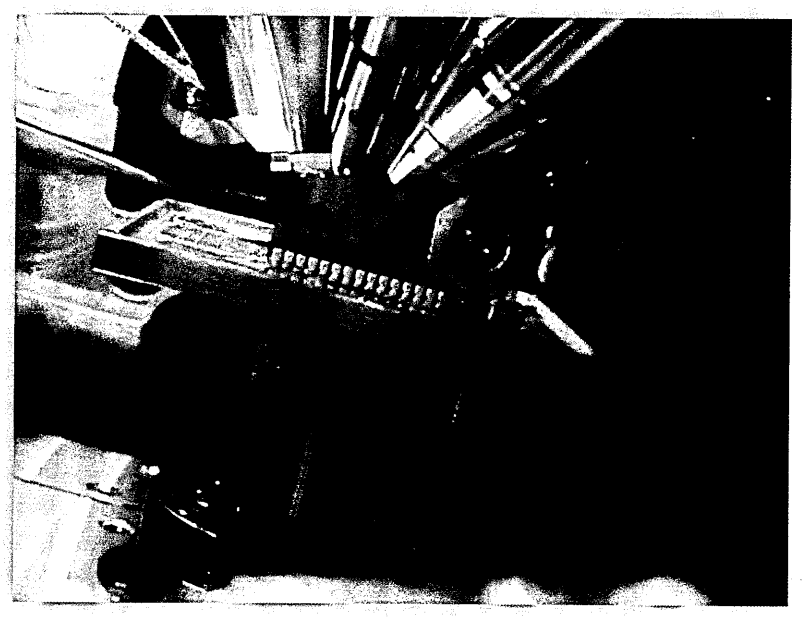


Figure 8-17. FIBSEM sample chamber.

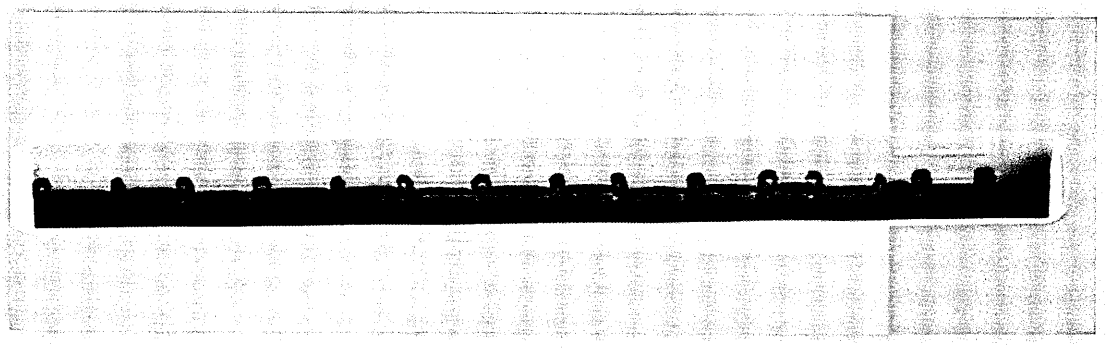


Figure 8-18. Trench along avalanche gain register showing electrodes and overlaps.

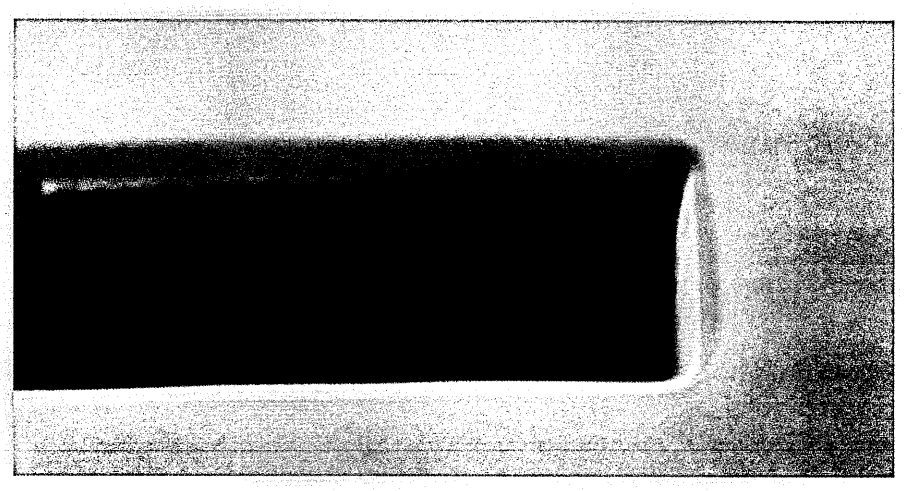


Figure 8-19. CCD97 electrode structure at the end of the trench.

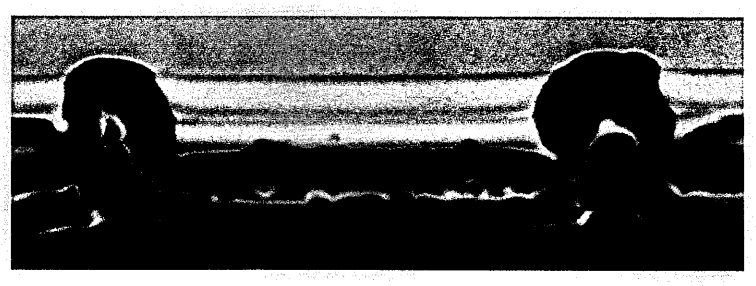


Figure 8-20. Magnified electrode of the CCD97 showing little overlap between adjacent phases.

In order to ensure that this result was true and not an artefact of the imaging techniques, an older device, a CCD02, was used to undergo the same procedure. Figure 8-21 and Figure 8-22 show these new images with overlaps that look more a classical CCD electrode structure.

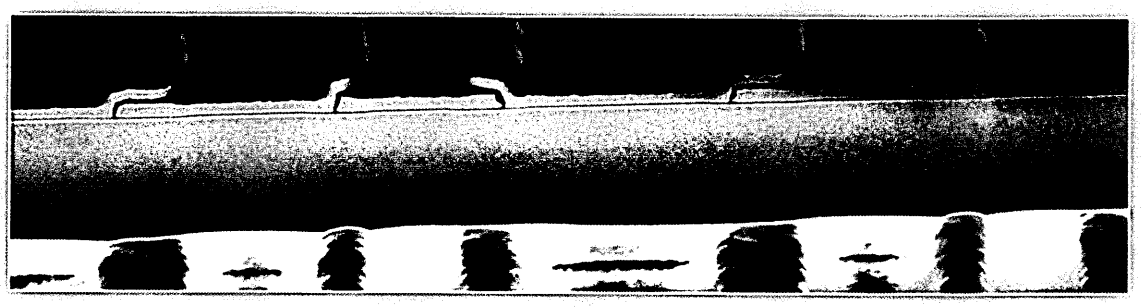


Figure 8-21. Trench of CCD02 serial register.

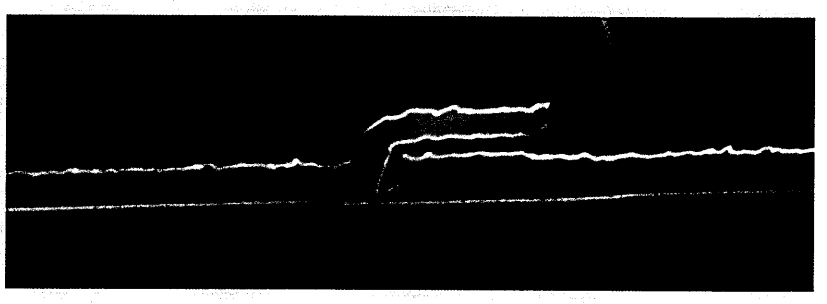


Figure 8-22. Magnified electrode structure of the CCD02 showing clear overlaps.

With the loss of any real overlaps in the avalanche gain register on the EMCCD a conclusion may be draw that SEGR did not occur because there was no overlap vulnerability to begin with. If however the manufacturing process is changed and the overlaps are brought back, then this subject will again need exploring.

8.8 Conclusion

SEGR was tested via an experimental campaigned to a heavy ion facility. Although not completely discarded, the idea that the EMCCD may be susceptible to a rupture event is an unlikely one. The likelihood that an ion will be incident on the sensitive region is very small, even at the excessive fluxes used at the HIF. In addition to this, the result produced by the FIBSEM has introduced uncertainties to whether or not the interpoly oxide or the gate overlaps themselves even exist. Therefore, it is difficult to make a judgement to

whether the devices will be vulnerable if the gate overlap situation is resolved. However, in their current state, this study has shown that the EMCCD should be a stable technology for space use where heavy ions are concerned.

Chapter 9: Conclusions and future work

Prior to this work, ageing had just been discussed and only the presence of the effect was known. This work set about establishing an experimental setup to enable a more thorough investigation of the phenomenon through creation of an ATE under software control. During this programme work has been performed exclusively on the CCD97, the findings can be broken down into:

- EMCCD register artefacts and anomalies
- Understanding and cause of EMCCD ageing
- Radiation effects on EMCCD technology, including important new work into SEGR

These are now described.

9.1 EMCCD register artefacts and anomalies

Physical properties of the CCD97 registers were investigated to ascertain the reasons behind particular measurements. Results and future work recommendations are detailed below:

- Various anomalous results were measured during a dark current integration within the serial and avalanche gain registers of an EMCCD device. Many were attributed to the physical properties of the device such as; the increasing surface area of register elements creating more dark signal, the glowing of amplifiers and the ineffective transfer of charge in certain areas. However, the source of one particular measurement, the dark section observed in the last 16 elements of the gain register, has yet to be solved although a re-consideration of design practice is recommended for this area.

- Gate overlaps have been used in the manufacturing of CCDs for some time however, it seems recently, something has changed where the overlaps are not as precise as the older devices. A comparison between a CCD02 and a relatively modern CCD97 was made, which showed a decrease in overlap quality. Once more some re-consideration of design practices is required.

9.2 Understanding and identifying the cause of EMCCD ageing

Characterisation and the pursuit of a cause to the EMCCD ageing phenomenon was undertaken with particular emphasis on hot-hole build-up under the phase preceding RΦ2HV. Results and future work recommendations are detailed below:

- Detailed characterisation of EMCCD ageing was undertaken using a newly developed ATE. The phenomenon was demonstrated alongside some dependencies, including read-out rate and avalanche potential. These factors directly affect the amount of signal passing through the avalanche register which is believed to be the main dependency of the ageing effect.
- A possible cause of EMCCD ageing has been experimentally shown to manifest itself as a voltage shift in the preceding phase to RΦ2HV, despite which way the register is clocked. This has been linked to simulation work that has shown hole accumulation under this phase. Further work is required in expanding the theory provided briefly in Chapter 6.
- This investigation has provided the first results to show a cause of EMCCD ageing in support of the simulations showing hole trapping under ΦDC. This has been demonstrated through a novel measurement technique to identify changes in full-well capacity under the specific phase.

- Possible changes to the manufacturing processes of the EMCCD have been suggested. These have included low voltage alternatives with the use of thin oxides and the removal of nitride layers. Additionally a suggestion to implant the device rather than have a static electrode ΦDC was suggested removing possible trapping sites.

9.3 Radiation effects on EMCCD technology

Radiation effects including both gamma and proton radiation were investigated, paying particular attention to the effects on the ageing and gain of the CCD97 devices. Results and future work recommendations are detailed below:

- The gamma irradiation study has shown that the gain produced by the EMCCD experiences a large decrease between pre and post irradiation testing. The reason for the step change has been attributed to an uneven, localised build-up of holes during the irradiation, caused by a potential structure in the EMCCD created by hole trapping during the ageing.
- The proton irradiation has shown that the gain and associated ageing of the EMCCD is not affected by incident protons. The avalanche gain observed in the original data was limited by the amount of dark signal, however after a lengthy room temperature anneal the lower dark current has allowed for larger gains to be measured. This has been attributed to a dark current annealing process rather than a gain mechanism one.

9.4 Single event gate rupture on EMCCD technology

The EMCCD's susceptibility to heavy ions was investigated, focussing on Single Event Gate Rupture. Results and future work recommendations are detailed below:

- The work performed on Single Event Gate Rupture has experimentally shown that the EMCCD, more specifically the CCD97, has out-performed the initial models which show it to fail at relatively low LETs. The final result showed that no rupture event occurred, even at fluxes 3 orders of magnitude higher than seen in orbit and with energies rarely seen in the space environment. However, the lack of gate-overlap seen in this device may be inadvertently causing a lack of sensitive region between the gates. This becomes particularly important if the overlap problem is solved, this may then re-introduce this sensitive region. A re-test will therefore be required.

9.5 Closing statement

The aim of this thesis was to raise the TRL of EMCCD technology so that it may be adopted for space use. Particular attention was given to creating an understanding of the ageing however the results on the radiation effects and SEGR have both provided answers to questions that contribute to understanding.

The work has uncovered new discoveries which could benefit from further investigation, most notably; the regions of the register that give anomalous dark current values during integration and the step change in gain following an exposure to gamma-rays.

The results produced from the ageing investigation have provided suggestions to new device designs which in the future may form the basis of a solution to the ageing phenomenon.

The important new work on SEGR resulted in no failure at the highest LET available at the HIF. Part of the reason uncovered for this is most likely the current polysilicon overlap practise at e2v technologies. Caution should be exercised if design or manufacturing techniques re-establish more profound overlaps, in which case, the SEGR testing should be re-visited.

After some attention on some issues outlined in this thesis there remains no significant reason to preclude adoption of EMCCD technology in space instrumentation.

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