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Journal Item

A Route Towards the Fabrication of 2D Heterostructures Using Atomic Layer Etching Combined with Selective Conversion

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Abstract

Heterostructures of low-dimensional semiconducting materials, such as transition metal dichalcogenides (MX_2), are promising building blocks for future electronic and optoelectronic devices. The patterning of one MX_2 material on top of another one is challenging due to their structural similarity. This prevents an intrinsic etch stop when conventional anisotropic dry etching processes are used. An alternative approach consist in a two-step process, where a sacrificial silicon layer is pre-patterned with a low damage plasma process, stopping on the underlying MoS_2 film. The pre-patterned layer is used as sacrificial template for the formation of the top WS_2 film. This study describes the optimization of a cyclic Ar/Cl_2 atomic layer etch process applied to etch silicon on top of MoS_2, with minimal damage, followed by a selective conversion of the patterned Si into WS_2. The impact of the Si atomic layer etch towards the MoS_2 is evaluated: in the ion energy range used for this study, MoS_2 removal occurs in the over-etch step over 1-2 layers, leading to the appearance of MoO_x but without significant lattice distortions to the remaining layers. The combination of Si atomic layer etch, on top of MoS_2, and subsequent Si-to-WS_2 selective conversion, allows to create a WS_2/MoS_2 heterostructure, with clear Raman signals and horizontal lattice alignment. These results demonstrate a scalable, transfer free method to achieve horizontally individually patterned heterostacks and open the

route towards wafer-level processing of 2D materials.

Introduction

Two-dimensional materials are attractive due to their specific properties such as a direct bandgap in single-layer, absence of dangling bonds, smaller permittivity, and therewith related smaller short-channel effects.[1] Therefore, 2D materials are promising as channel material in 2D field effect transistors (FET), tunnel-field effect transistors (TFET), and valleytronic devices, which are based on heterostructures.[2–4] Tremendous efforts were spent in the device fabrication on films made by mechanical exfoliation or by chemical vapor deposition (CVD). Novel heterostructure device concepts were tested by stacking flakes with the pick-and-place method or by growing nanosheets on top of each.[5] Despite those innovative device demonstrations, many of the used approaches lack manufacturability on wafer-level. The integration of a simple back-gated 2D transistor was achieved recently, but there is no vision on the wafer-level fabrication of heterostacks for new device concepts.[6,7] Water-based transfer techniques are widely used to transfer 2D films from a growth substrate to a target device wafer.[8–12] However, a mechanical transfer process remains a source of defects like cracks and wrinkles, especially for larger substrates. It leaves often organic residues behind and induces a undesired variability in the device performance. Therefore a transfer-free, direct patterning process is highly desirable. Heterostructures of different 2D materials were prepared by drop-casting of MoO_3 nanobelt solution, followed by sulfurization, drop-casting of WO_3 nanobelts, and final sulfurization to achieve a heterostack.[13] Also sequential chemical vapor deposition (CVD) was used to deposit one first layer and the second one on top.[14,15] These techniques lack the possibility for a controlled deposition in a desired location on the substrate. A selective deposition was achieved by pre-deposition of two different metals with shadow masks and subsequent thermal sulfurization.[16] However, a shadow mask does not fulfill the requirements for nanopatterning and alignment accuracy. Selective growth techniques are necessary to achieve regular patterns. Two-dimensional materials can be selectively grown by providing a metal seed like Pt, Ti, or Au or by providing other nucleation sites like a prepatterned SiO_2 surface.[17–19] Growth selectivity was also achieved by O_2 plasma pretreatment of SiO_2 surface to make areas superhydrophilic and promote preferential precursor adsorption.[20,21] Furthermore, polymer functional layers (PFL) were used to inhibit the growth of transition-metal dichalcogenide (TMD) in the areas with the PFL.[22] All those techniques enable the deposition of one 2D layer in specific locations. However, functional

devices based on 2D materials consist of stacked ultrathin layers and thus, they require at least a second layer on top of the first layer to achieve a band alignment being appropriate for band-to-band tunneling (BTBT) as it is used in TFETs.[23] Stacking only two 2D layers on top of each other is not sufficient, because each need separate contacts to the interconnect level. It is therefore necessary to create two 2D layers, with different geometries, overlapping only in the tunneling region. 2D building blocks are MX_2 materials with the metal M = Mo, W, Sn and the chalcogen X = S, Se. They consist of a metal atom which is sandwiched in between the chalcogenide layers and this structure results in a covalent in-plane bonding of a nanosheet and weak van-der-Waals bond in between the layers. This similarity in the atomistic structure complicates selective etching processes, since each TMD materials' properties are comparable. Conventional continuous wave (CW) plasma etching processes with high bias of a few hundreds of Volts are not applicable here to stop on such sensitive few-layer materials, due to the high damage caused by ion bombardment and poor control of stopping at a defined thickness or at the interface between two nanosheets. CF_4-based CW plasmas were used to thin MoS_2 and the etching rate was minimized by grounding the sample.[24] Nevertheless, even this soft etching introduced damage requiring a restoration by annealing in sulfur-rich plasma or gas treatment afterwards.[25] Such soft etching procedure leads also to the dilemma that extreme low ion energies limit the range of other etchable materials like high-k dielectrics. Another group reported the soft plasma etching of MoS_2 or $MoSe_2$ by SF_6 / N_2 with very low input power and etch rates of 4 – 5 layers per minute.[26,27] Even pure Ar plasma thinning was reported for MX_2 thinning, though no additional information about the chemical changes in the top surface layers was provided.[28]

Ultimately, cyclic material removal using atomic layer etching concepts (ALEt) offers the possibility to better control the material removal. In ALEt, the etching process is separated into a surface reaction step and a removal step.[29] This enables the self-limited removal of material, in defined amounts, with high uniformity and is therefore often referred to as "digital etching". This layer-by-layer etch technique removes material, in principle, with atomic precision and can therefore prevent deep removal or damage of the underlying material, which is essential when patterning a film placed on top of a sensitive TMD layer.

On MX_2 materials, Cl_2-based ALEt has been used to thin down a trilayer MoS_2 in a controlled way, by using a Cl_2 inductively-coupled plasma (ICP) for chlorination, where the plasma is

separated by a metal mesh grid to reduce ion bombardment on the sample surface. [30,31] The removal step is done separately, in a second chamber, with a dual grid and Ar plasma enabling the control of the ion energy of impinging Ar ions. Another ALEt method was demonstrated by plasma oxidation of a MX_2 nanosheet with the subsequent evaporation of the oxidized layer, which is possible due to the difference in the evaporation temperature of MoO_3 and the higher decomposition temperature of MoS_2.[32] In another approach, a top MoS_2 layer is etched by an O_2 plasma and the underlying damaged surface was recovered by sulfur-rich annealing.[25]
In this work, we explore an alternative approach and show that close-to-conventional ALEt tools can be used to pre-pattern a sacrificial Si layer on top of MoS_2 multilayers, which is afterwards converted into a stack of two transition-metal dichalcogenides (TMD), using an Si-to-WS_2 conversion process.[33,34] This process flow demonstrates a scalable, selective growth of MX_2 heterostructures in defined locations, which can be used for the fabrication of band-to-band tunneling devices based on TMDs.

Experimental

Si wafers were first coated with 20 nm SiO_2, then with 10 nm Al_2O_3 using atomic layer deposition (ALD), and annealed at 1000 °C for 60 s in O_2 to stabilize the substrate. MoS_2 multilayers were deposited by the sulfurization of MoO_3 prepared with physical vapor deposition (PVD) on top of the Al_2O_3 layers.[35,36] Then, 35 – 45 Å Si was deposited on top of the MoS_2 by PVD. Samples foreseen for patterning were coated with an additional 11 nm thick SiO_2 hardmask, deposited by PECVD at 150 °C. Patterns were created by optical lithography using IX845 resist and the hardmask was opened either with a CF_4/H_2 plasma or by HF wet etching, before the resist was removed in an acetone bath and eventually dipped in isopropanol.
The samples with amorphous silicon on top of MoS_2 and SiO_2 hardmask were exposed to different conditions in an Oxford Instruments PlasmaPro100 ALE system with Cobra300 ICP source.[37,38] To this end, approx. 4 cm^2 large samples were attached with Fomblin to a SiO_2-coated carrier wafer. In the preparation phase of the ALEt, either a CW Ar plasma with an equivalent of 100 V bias for 14 s or in situ ALEt cycles were applied to remove the native SiO_2 from the top Si surface. In the second phase, the actual ALEt of remaining amorphous silicon was a cyclic process consisting of 40 ms Cl_2 dosing steps, a purge step with Ar of 2 s, and an activation step of 3 s with a plasma pulse biased towards the sample substrate.[37] The ICP

discharge was kept on during the entire process to dissociate the chlorine species during the dosing step and to provide Ar ions during the activation step (the substrate biasing was applied only during the pre-sputter step or the activation step of the ALEt). Bias voltages of 33 V, 45 V, and 97 V were investigated. Figure 1 illustrates the steps of the ALEt cycle. For each condition, several samples were processed to ensure reproducibility.

To avoid inhibition of the Si etch rate or enhancement of the MoS_2 etch rate by unwanted species such as O_2, the chamber was conditioned first with 100 ALEt cycles with a SiO_2-coated wafer placed on the chuck. This ensures that the alumina chamber walls as well as the carrier wafer surface are sufficiently chlorinated and that other weakly-bound adsorbates are removed from the chamber walls.

To estimate the bias power impact in the most critical Ar plasma activation step, the ion velocity distribution functions were determined by a retarding field analyzer (RFEA), which was placed into the chamber. This system provided by Impedans as Semion RFEA sensor, consists of an orifice and an additional grounded grid confining the ion influx. A second grid behind this orifice is used to discriminate the ion energies (retarding voltage) and eventually a collector measures the incoming ion flux (collector current). The ion velocity distribution function (IVDF) is proportional to the derivative of the collector current with respect to the retarding voltage.[39]

The remaining thickness of Si and MoS_2 was measured by spectroscopic ellipsometry. The blankets films were analyzed by a confocal microscope-based Raman spectrometer Horiba Jobin-Yvon HR800 using a laser of 532 nm (100x 0.9 NA Olympus objective, 1800 grooves/mm grating) and Rutherford backscattering spectrometry (RBS) using a 1.523 MeV He^+ beam.[40] The chemical state of the surface was determined by X-ray photoelectron spectroscopy (XPS) with a Theta300 system from ThermoInstruments (Al K_α X-ray source of 1486.6 eV). Transmission-electron microscopy (TEM) images were obtained by a FEI Titan3 G2 60-300 system and the elemental distribution was characterized by energy-dispersive X-ray analysis (EDS).

The whole fabrication flow of the heterostructure is shown in Figure 2. The samples with the patterned Si on top of MoS_2 were converted by a cyclic process using WF_6 and H_2S to convert Si to WS_2 .[34,41] To this end, the samples with the ALEt-patterned Si on top were dipped into 0.5 % HF solution to remove the native SiO_2 from the surface. Then this sample was placed in a CVD reactor and exposed to a pulse sequence of WF_6 at 450 °C, which is forming volatile SiF_4

and selectively converted tungsten. This is followed by a N_2 pulse for purging and an H_2S pulse to convert the metallic W in situ to WS_2. Eventually, the samples were recrystallized using rapid thermal annealing (RTA) in H_2S-containing atmosphere above 800 °C.

Results and discussion

Atomic layer etching is the reverse process to atomic layer deposition (ALD). In the present study, a plasma-enhanced ALEt process was applied to remove Si selectively from MoS_2. At first, the ALEt was characterized on thick amorphous silicon to determine its etch rate. Then, the impact on the interface towards the MoS_2 layer was determined and eventually the conversion of the ALEt-patterned Si into 2D heterostacks was investigated.

Amorphous silicon etching by ALEt

Silicon oxidizes quickly in air, which can hinder the ALEt process due to the strong Si-O binding energy (~ 8.27 eV). Typically native oxide on Si grows 10 - 15 Å thick under ambient conditions. This oxide could be removed wet chemically by a HF dip. However, the used hardmask is also SiO_2 and would be quickly etched by the HF treatment as well, hence this particular native oxide removal method is not an option. A dry in situ removal during the ALEt process was used. Two native oxide removal techniques were studied: an Ar-plasma pre-sputter clean and the *in situ* removal by the application of the ALEt process. The pre-sputter clean consists of an Ar plasma, in which inert ions are accelerated towards the sample surface and remove the top layer by sputtering. At first, the sputtering rate for 100 V bias was determined to be 1 Å/s. To remove the native oxide layer prior to ALEt, a pre sputter clean of 14 s was applied before the Ar/Cl_2 ALEt cycles. The etch depth on 20 nm thick Si layer is shown in Figure 3. The remaining Si thickness upon ALEt is a linear function with a slope of 6.6 Å/cycle. A linear fit of those points would intersect at 194 Å, whereas the pristine sample had a aSi thickness of 208 Å. The 14 Å thickness difference correspond to the etch depth of the pre-sputter Ar plasma.

The bombardment of surfaces with high energetic noble ions is known to cause some amorphization and lattice defects of the remaining layer, over up to few nanometers. In order to determine the impact of the high voltage Ar pre-sputter step, two MoS_2 samples with 35 Å and 45 Å Si cap were exposed to 15 s Ar plasma. As it can be seen in the Raman spectra in Figure 4,

the MoS_2 related E^1_{2g} peak below a 35 Å Si layer lost already intensity, indicating damage, in contrast to the MoS_2 under the thicker 45 Å Si. Although this process is expected to only remove 14 Å of the cap layer, a degradation in the E^1_{2g} peak is seen for the thinner Si cap, whereas the observed increase in the E^1_{2g} peak for the thick cap can be related to effective thinning of the Si cap relative to MoS_2 (and thus less absorption). Although the ALEt on Si can be well controlled, the use of a pre-sputtering causes damage to the MoS_2 through the very thin remaining Si layers, which must be avoided.

Therefore, the *in situ* oxide removal by the ALEt process with the chlorine pulses itself was studied. The etch depth for different bias power settings and cycles are depicted in Figure 5a. The Si thickness changes show a horizontal shift - we call it the ALEt delay - and a linear part with a Si removal rate of 6 - 7 Å per cycle. This shows that the native oxide can be removed by the ALEt process itself, and that the oxide removal rate varies with the applied bias power, opposite to the Si removal rate which is independent of bias in this range. It requires one extra cycle for the 97 V process, seven extra cycles for the 45 V process, and ten cycles for the 33 V process until the native SiO_2 is removed and the ALEt continues in the linear regime. These results confirm that there is a low ion energy ALEt process, which can remove native SiO_2 and Si within the ALEt window.

The Figure 5a indicates that, in the investigated range of DC bias voltages applied during the ALEt cycles (33, 45, and 97V) , the Si etch rate does not vary. This is a typical fingerprint of the ALEt process, where a ion energy plateau shows a constant etch- per-cycle saturation behavior.[37] For too low bias (in our case, below 33V), the energy transfer by the inert ions to the chlorinated silicon surface is not high enough to enable the formation of volatile $SiCl_x$ species; on the contrary, for too high bias (in our case, higher than 97V), the system is above the sputtering threshold of silicon, and material removal becomes a two-component process, relying on the formation of $SiCl_x$ but also on pure sputtering.

ALEt on Si/MoS_2 heterostacks

In the next step, the chlorine-based ALEt process was applied to the heterostack of Si/MoS_2 on blanket samples to remove the Si selectively from the MoS_2 and to study the impact of the etch process on the MoS_2 surface.

The ALEt process without pre-sputtering was applied to the Si/MoS_2 with different bias (33 V and 45 V) until the complete Si layer was removed (monitored by residual Si measurement by ellipsometry). The remaining MoS_2 thickness is shown in Figure 5b. With a 45 V bias in the removal step, MoS_2 is recessed with a rate of 4.4 Å/cycle, whereas with 33 V, only 2.9 Å/cycle were removed. This shows that the MoS_2 removal rate is more dependent on the variation in power than the Si removal rate, i.e. for the specific plasma conditions used here, when applied to MoS_2, the system is out of the ALEt energy window.

This can be explained by the mechanisms of the ALEt cycles. The ALEt is based on the removal of a chlorinated surface layer, ideally selective to the non-chlorinated 'pristine' atomic layer underneath.

In case of layered MX_2 materials, there are strong in-plane bonds and weak bonds in between the layers. The sulfur termination passivates the metal atoms and is expected to be stable in dry conditions at room temperature. To replace the sulfur by chlorine, the sulfur needs to be removed first. Voronina et. al calculated that chlorine adsorbs preferably on MoS_2 with defects in comparison to defect-free MoS_2.[42] The energy for the creation of one sulfur vacancy is around 2.4 eV.[43,44] This is lower than the applied bias in the range of 30 – 50 eV for the present work (see Figure 8). This defect formation can occur in the Si removal step, in which the biased Ar plasma can desulfurize the top layer, resulting in a deteriorated 2D film. In the next ALEt cycle, fragmented chlorine chemisorbs on the surface during the dosing step to the metal. This modified surface layer is removed during the next Ar plasma biased pulse, which simultaneously does deteriorate the adjacent layer's sulfur termination. In summary, atomic layer etching rely on the existence of self-limited adsorption and activation steps, which are existing for Silicon in the ALEt parameter ranges investigated here. When applied to MoS_2, the activation step overlap with the adsorption step by creating Sulfur vacancies on the surface, which favor the chlorination. This vacancy creation process, during activation, is time- and energy -dependent, leading to variable level of subsequent chlorine adsorption on the surface. This determines the final amount of MoS_2 removed per cycle and the absence of a constant etch- per-cycle saturation behavior.

The above assumed mechanism is supported by the observed MoS_2 etch rate, in the range of a sub-monolayer per cycle. The monolayer thickness of MoS_2 is 7 Å and hence, it takes 2 to 3 ALE cycles to etch one monolayer of MoS_2 with the 33 V bias.

To understand the impact of this ALEt etch step onto the MoS_2 surface, the Si capped MoS_2 films were etched with a different number of cycles to identify the breakthrough at the interface from Si to MoS_2. The Raman spectra after different cycle number (without the additional SiO_2 removal cycles) are shown in Figure 6a. For 33 V, the MoS_2 is stable up to a few cycles and then the intensity decreases for increasing ALEt cycles. During the first few cycles, the ALEt process etches the Si cap and MoS_2 is not in contact with the plasma yet. Once the cap is removed, the MoS_2 is recessed as well. The faster decay for the 45 V bias ALEt process in comparison to the 33 V bias confirms the higher removal rate of MoS_2, opposite to the Si etch rate which remains constant for various bias (see Figure 5a).

The region of the breakthrough from Si to MoS_2 was studied by RBS. The results in Figure 6b and 6c indicate that this breakthrough occurred after approximately 6 cycles on the 45 Å thick Si. At 45 V, the sulfur amount is reduced after the transition, but the metal remains at its initial level. For additional ALEt steps, the metal amount reduces and the sulfur/metal ratio remains below pristine value. This confirms the proposed mechanism: the removal of MoS_2 occurs through desulfurization and depends on the bias power.

The surface damage was evidenced by XPS in Figure 7, which shows the surface chemical analysis after Si ALEt, stopping at the interface Si/MoS_2. The peak at high binding energy, characteristic for the MoO_3, increases in its relative intensity. MoO_3 forms after air exposure, once the MoS_2 surface is desulfurized (the XPS is done *ex situ*). Both the spectra, for 33 V and 45 V bias, are overlapping, indicating that the surface oxidation results in a similar damage for both bias settings.

Hence, this ALEt process can remove Si as well as MoS_2 layer-by-layer, but it leaves always a modified top surface layer behind. Since this damage is in the sub-monolayer range, it cannot be detected in the disorder-induced LA(M) mode in multilayers as this method is not sensitive enough to this top-layer damage.[38] This suggests the use of a multilayer system, in which the interface layer can be sacrificed, since it loses its function through the damage.

To determine the characteristic of the ions impinging on the surface, the collector current was measured. Its derivation is proportional to the ion velocity distribution and is shown in Figure 8. For zero applied bias voltage, the peak in ion distribution is at 10 eV, which represents the average ion impact energy during the dosing and in the purge step, and corresponds to the plasma self-bias for the specific geometry of this etch chamber. This 10 eV peak shows the highest

intensity in comparison to the distributions measured at higher bias, indicating that most ions hit the MoS_2 surface with the same, low kinetic energy. This energy is only one order higher than the Mo-S bond dissociation energy of 2.59 eV. With increasing bias up to 19 V, the distribution function broadens and the maximum peak intensity for the different modes reduces: less ions of a given energy are hitting the surface, but with a wider range of kinetic energy, between 20 eV and 40 eV for the 19 V bias case. At applied bias above 20 V, the IVDF splits into a bimodal distribution and shifts to higher energies. Above 40 V bias, the high energetic peak is located above 70 eV. Compared to the low molybdenum-sulfur bond energy of 2.59 eV, this explains the preferential sulfur removal during this step.[45,46] For even higher bias, this trend continues and a high energetic peak with only small intensity is present. However, these are the most damaging ions. For a bias of 82 V, the ion distribution ranges already from 60 eV to 130 eV. The high energetic ions in this distribution are already two orders of magnitude higher than the Mo-S bond energy and thus, during the activation step, sulfur vacancies are created at high rate, leaving metallic Mo behind, which is etched by Cl in the next pulse.

As a consequence, using a plasma process within the ALE windows of Si (hence between 30 V and 80 V bias) will always lead to damage of the top TMD layer. Hence, the method described here can only be applied for multilayer MX_2 systems. In order to reduce the damage, the wafer temperature might be increased to enable the removal of surface $SiCl_x$ at lower Ar activation energy and shift the ALEt window towards lower energies. In addition, one could think of the introduction of a sulfur-containing gas in an additional step after the Ar removal step and the next chlorination step in order to replenish broken bonds immediately with sulfur. The ALEt demonstrated that Si could be etched from MoS_2 without damaging its bulk composition, which is interesting for bilayers and few-layer structures.

Conversion of the Si into W and sulfurization to WS_2 – Demonstration of selectivity and resulting morphology

The ALEt process described above was used to remove silicon from a MoS_2 patterned sample with a small surface modification of the 2D material. Samples with ALEt-patterned Si/MoS_2 were then treated by HF to remove the SiO_2 hardmask including the native oxide from the Si and to dissolve MoO_3. The MoS_2 itself is inert against HF, since the hypothetic reaction

$$MoS_2 + 4\,HF_{(g)} \rightleftharpoons Mo + 2\,H_2S_{(g)} + F_{2(g)} \qquad \text{(I)}$$

is endergonic with a Gibbs free energy of 1300 kJ/mol and hence thermodynamically not favorable.[47–49] Degradation can only occur due to extensive exposure to moisture.[50]

This means that Si was removed in the regions which were not protected by the hardmask. Elemental Si was still present in the regions covered by the mask and it was converted to W by the gas phase precursor WF_6 (reaction II), then sulfurized by H_2S at 450 °C (reaction III):[33,34,41]

$$3\,Si + 2\,WF_{6(g)} \rightleftharpoons 2\,W + 3\,SiF_{4(g)} \quad \text{(II)}$$

$$W + 2H_2S \rightleftharpoons WS_2 + 2H_{2(g)} \quad \text{(III)}.$$

A linear scan with Raman spectroscopy was conducted over such a pattern and is depicted in Figure 9. In the ALEt patterned region, only the characteristic modes for MoS_2 are visible. Outside those regions, additional peaks indicate the presence of WS_2 resulting from the converted Si, forming a WS_2/MoS_2 heterostack. There, the signal of the MoS_2 is reduced due to the additional light absorption in the top WS_2 layer.

The selectivity of the conversion of the Si-containing region was demonstrated. MoS_2 is not reacting with WF_6, as it can be seen from the thermodynamics of reaction IV with a Gibbs free energy of 172 kJ/mol:

$$MoS_2 + WF_{6(g)} \rightleftharpoons MoF_{6(g)} + WS_2 \quad \text{(IV)}.$$

Figure 10a shows the as-deposited sample without patterning. The MoS_2 is covered by a thin elemental Si cap, which will be the reducing agent for the WS_2 deposition. The SiO_2 hardmask above covers the areas, which will not be patterned by ALEt. The TEM image in Figure 10b and c show the structures resulting from the combination of the ALEt and the selective conversion. In the ALEt-recessed regions the elemental Si is absent, since it was etched by the Ar/Cl_2 ALEt sequence. Consequently, there was no W-related compound deposited in those regions during the WF_6/H_2S conversion.

The selective growth of WS_2 is visible on the previously masked area. The elemental EDS maps confirm the presence of the WS_2 on top of the previously masked MoS_2 and the layered structure of the MoS_2 is still visible. Nevertheless, the images and the elemental maps reveal a low interface quality. The TEM images show a thin SiO_2 interlayer between the MoS_2 and the WS_2. This oxide interfacial layer is not visible in the images taken before the conversion of the Si to

WS_2. It appears only afterwards. As shown in earlier work, the conversion reaction of Si to WS_2 is non-stoichiometric in the case that the SiO_2 is not completely removed before the conversion.[33] This is the case for a too short HF-dip during the removal of the hardmask and the native oxide. Residual SiO_2 is then not reacting with the WF_6 and remains as a sediment at the interface between the MoS_2 and the WS_2 from the gas phase reaction. This could be eliminated by improving the HF wet etch step to remove the native SiO_2 fully and to passivate the Si again re-oxidation. Despite the fact that the interface it not sharp due to these SiO_2 interlayer, there are no signs of intermixing due to the clear Raman spectra and the absence of additional shifted peaks.[51,52]

In the ALEt-treated region, the number of layers decreased from nine layers (under the Si-cap) to seven layers (after Si etch), and the remaining layers keep their original crystalline quality (no amorphization). The loss of 1-2 layers confirms the surface damage induced in the top layer through the biased removal step during the cycles. This damaged layer, in the form of MoO_3, was removed during the HF-dip prior to the conversion.

These images demonstrate the proof-of-concept of a process flow allowing to create multilayer structures using a sacrificial Si patterning/conversion approach, in which one Si layer is patterned on top of a bottom MoS_2, then converted into WS_2. This is an important step towards the implementation of 2D materials with VLSI-compatible techniques, scalable to full wafer-level.

Conclusion

Atomic layer etching is a powerful tool to remove materials with a rate of only a few atomic layers per cycle, with the power to limit the damage towards sensitive substrate materials. In this study, the chlorine-based atomic layer etching of Si on MoS_2, using a close-to-conventional reactor was characterized. Repeatable, linear Si etch rates around 6-7 Å per cycle were achieved. It was found that the applied bias in the removal step can remove the native SiO_2 from the Si, in situ, without the need for a detrimental high bias Ar pre-sputter step. The native oxide resulted in an inhibited Si removal at start of the ALEt process, which is called the ALEt delay. After the

ALEt delay, the Si etch rate was constant for different bias power, indicating that this process is within the ALEt window for Si. The developed ALEt process was applied to Si/MoS_2 heterostructures to grow a WS_2/MoS_2 stack using a subsequent WF_6/H_2S conversion. Si etching using ALEt was studied and the selectivity and the damage towards underlying MoS_2 was characterized. Contrary to the Si removal, the ALEt impact onto the MoS_2 depends on the bias power applied during the removal step, with more MoS_2 removed at higher bias. Based on RBS observations, the layered structure of MoS_2, and the low energy required to create a sulfur vacancy, we conclude that the biased Ar plasma pulse removes previously chlorinated Mo and simultaneously desulfurizes the next layer. The plasma's ion velocity distributions indicated that the applied bias regime contains high energetic ions which cause the desulfurization of the top surface MoS_2 layer. Further research should focus on the study of bias regimes with low, sharp ion velocity distributions located around 10 eV, and their propensity to remove chlorinated layers. In the present case, despite using a low-bias process with high ALEt synergy, it is necessary to design the Si/MoS_2 stack with multilayers, considering the topmost layer as sacrificial, since it is damaged during the etch stop. Further work will focus on lowering the applicable Si ALE window, the optimization of the residual-free hardmask removal, and the in situ restoration of sulfur bonds to provide an optimal interface quality.

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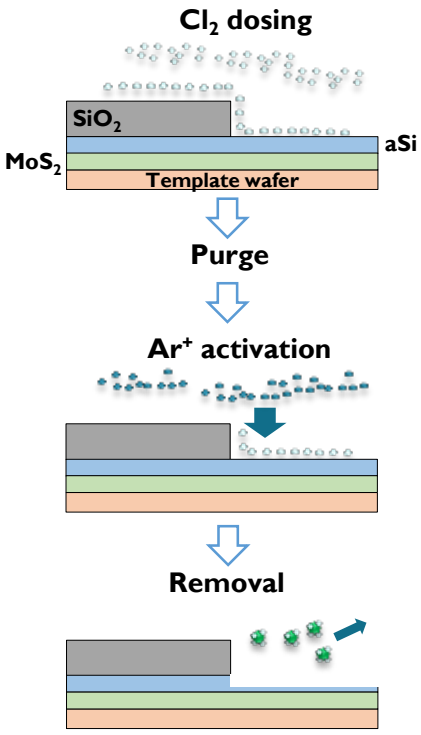

Figure 1: Schematic of the used ALEt process consisting of the steps of fragmentation of chlorine during the dosing, a purge with non-bias Ar plasma, and a biased Ar plasma step to remove the formed surface species and remove material in the sub-nm range

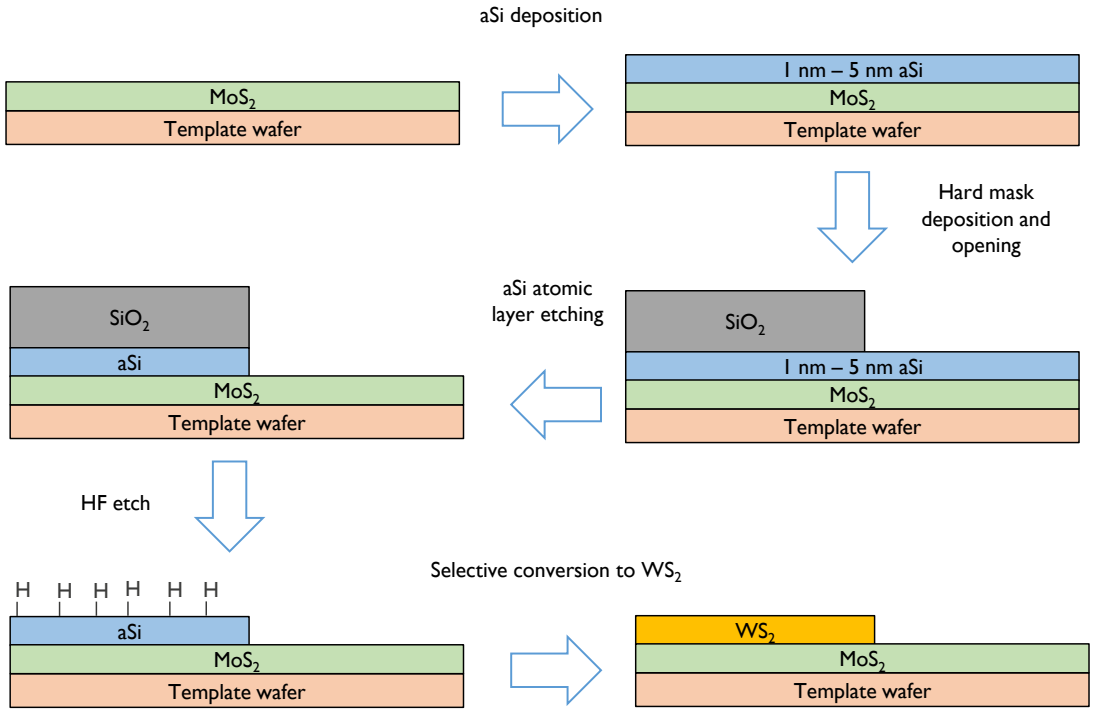

Figure 2: Schematic of the process flow for creating heterostack with a patterned top layer

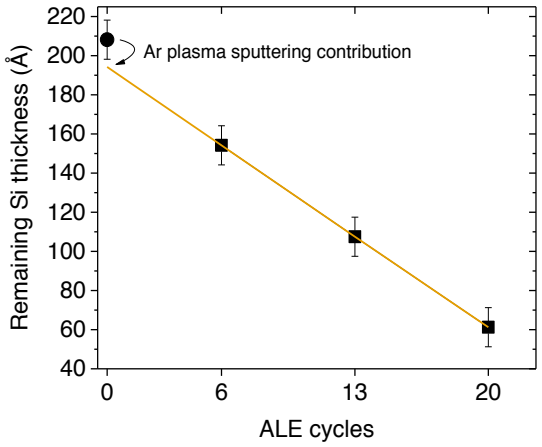

Figure 3: total thickness measured by spectroscopic ellipsometry on the Si samples before 45 V biased ALEt (dot) and after pre-sputtering and different numbers of ALEt cycles (squares). The

first point (pristine sample) correspond to Si covered by native oxide (SiO_2/Si), while subsequent points, measured directly after etch, correspond to Si only. Before applying the ALEt cycles, a 14s Ar-only (97V bias) pre-sputter step is applied to remove the native oxide.

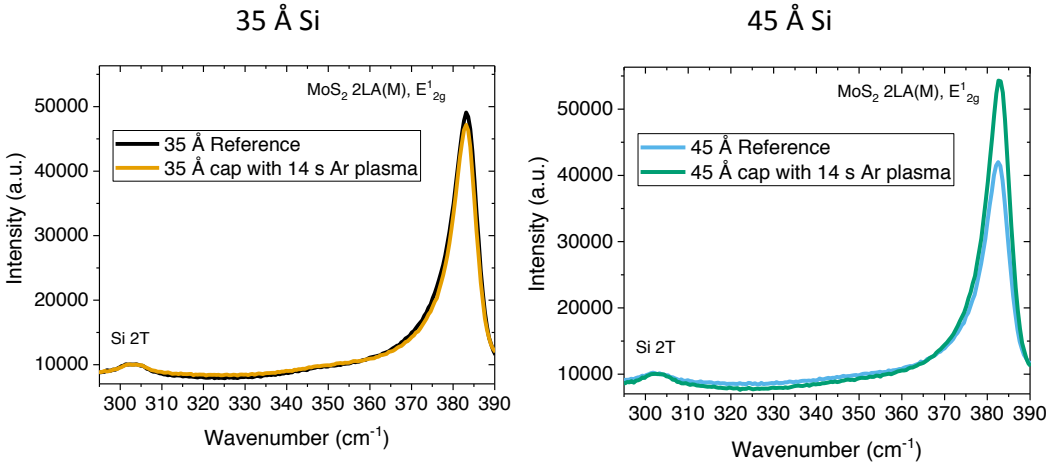

Figure 4: Raman spectra of the E^1_{2g} MoS_2 peak normalized to Si 2(TA). The spectra intensity decreases for the thin Si cap after plasma treatment and increase for the thicker Si cap.

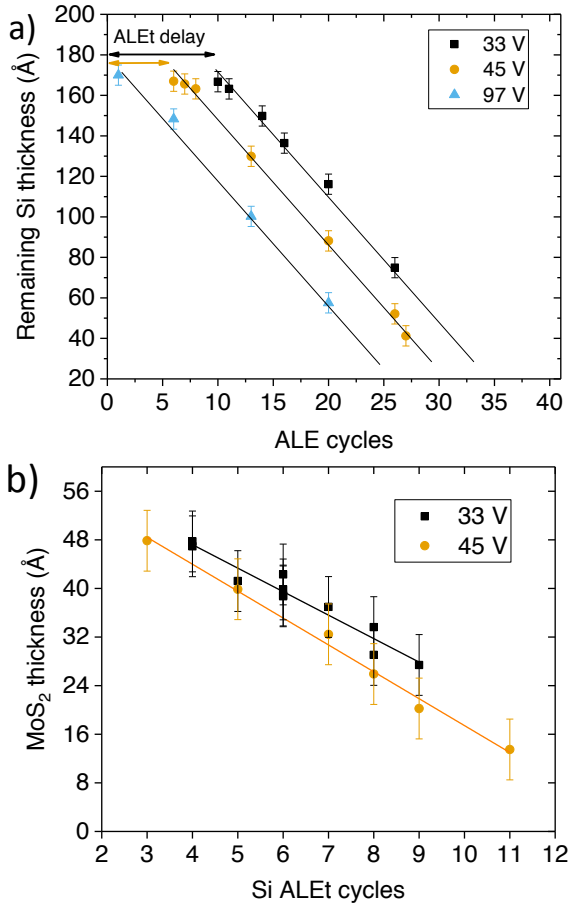

Figure 5: a) shows the remaining Si thickness as a function of the ALEt cycles for different bias power, measured by ellipsometry. No pre-sputtering for native oxide removal was applied. b) shows the remaining MoS_2 thickness determined by SE as a function of normalized overetch ALEt cycles; the cycles for breaking through native oxide and to remove the elemental Si are already subtracted

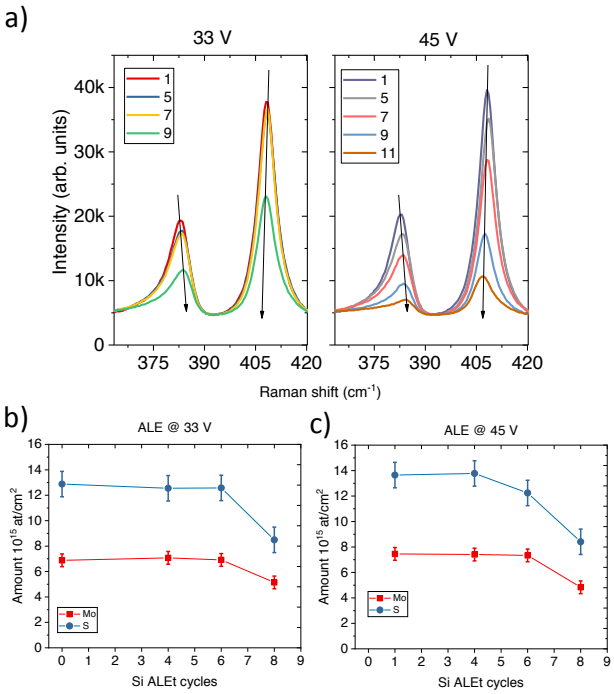

Figure 6: a) Raman spectra obtained after ALEt on Si/MoS_2 heterostack for a different number of cycles and different power; b) and c) are showing the atomic area density from RBS after different number of ALEt cycles and different power; line added for guiding the eyes.

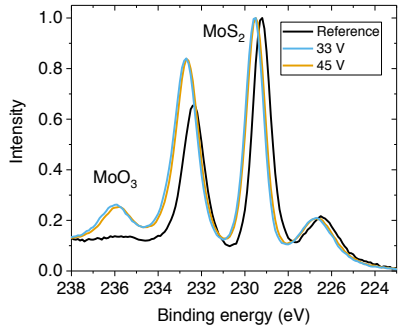

Figure 7: XPS spectra of reference samples and ALEt recessed samples stopping at the interface Si/MoS_2

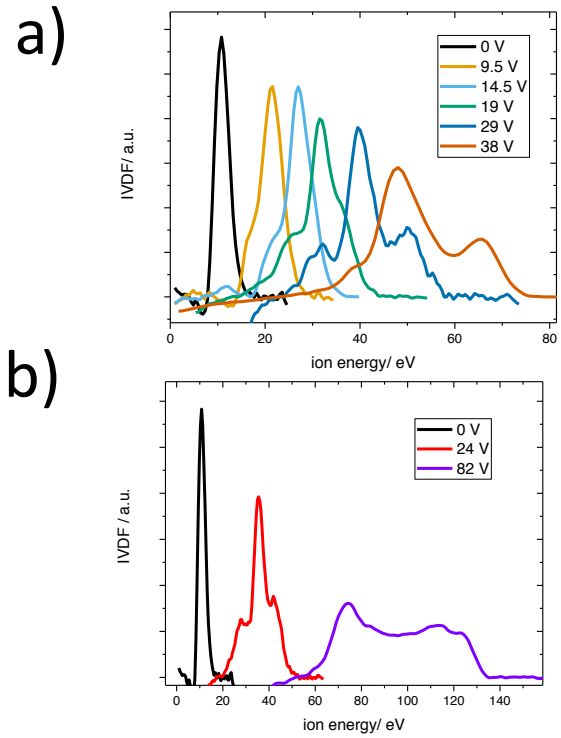

Figure 8: Ion velocity distribution functions for different setpoints of bias voltage for a) low bias range and b) high bias range. Above 20 V bias voltage, the ion velocity distributions becomes broad, ranging to high energies.

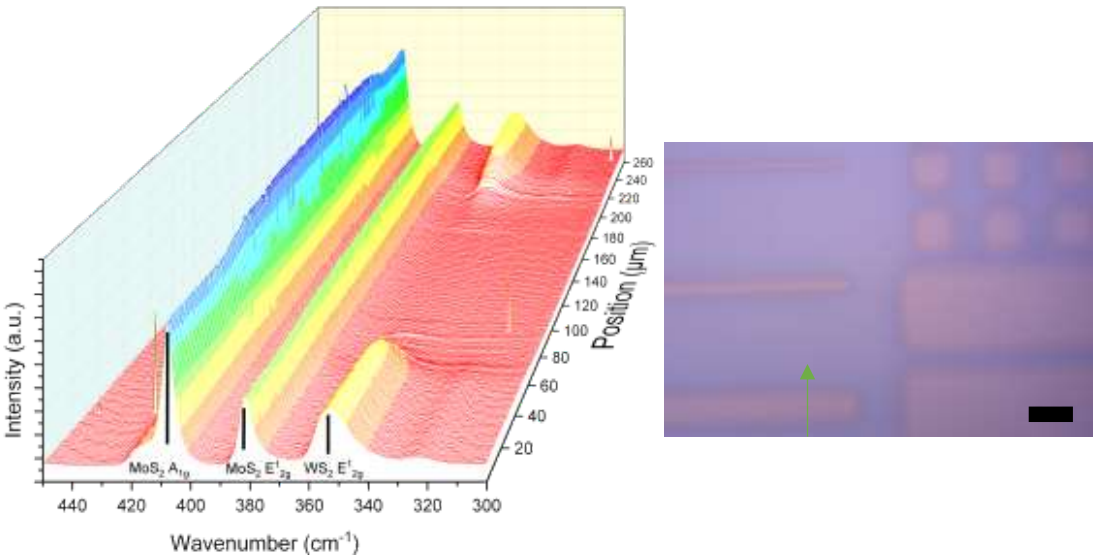

Figure 9: Raman linescan over the ALEt-recessed region after the conversion process. The ALEt-recessed regions show only the peaks from MoS_2. The area which was masked show in addition the top WS_2's characteristic peaks. The microscopy image with the arrow shows the scanning direction of the area with the heterostack and the single-material area. The scale bar is 200 µm.

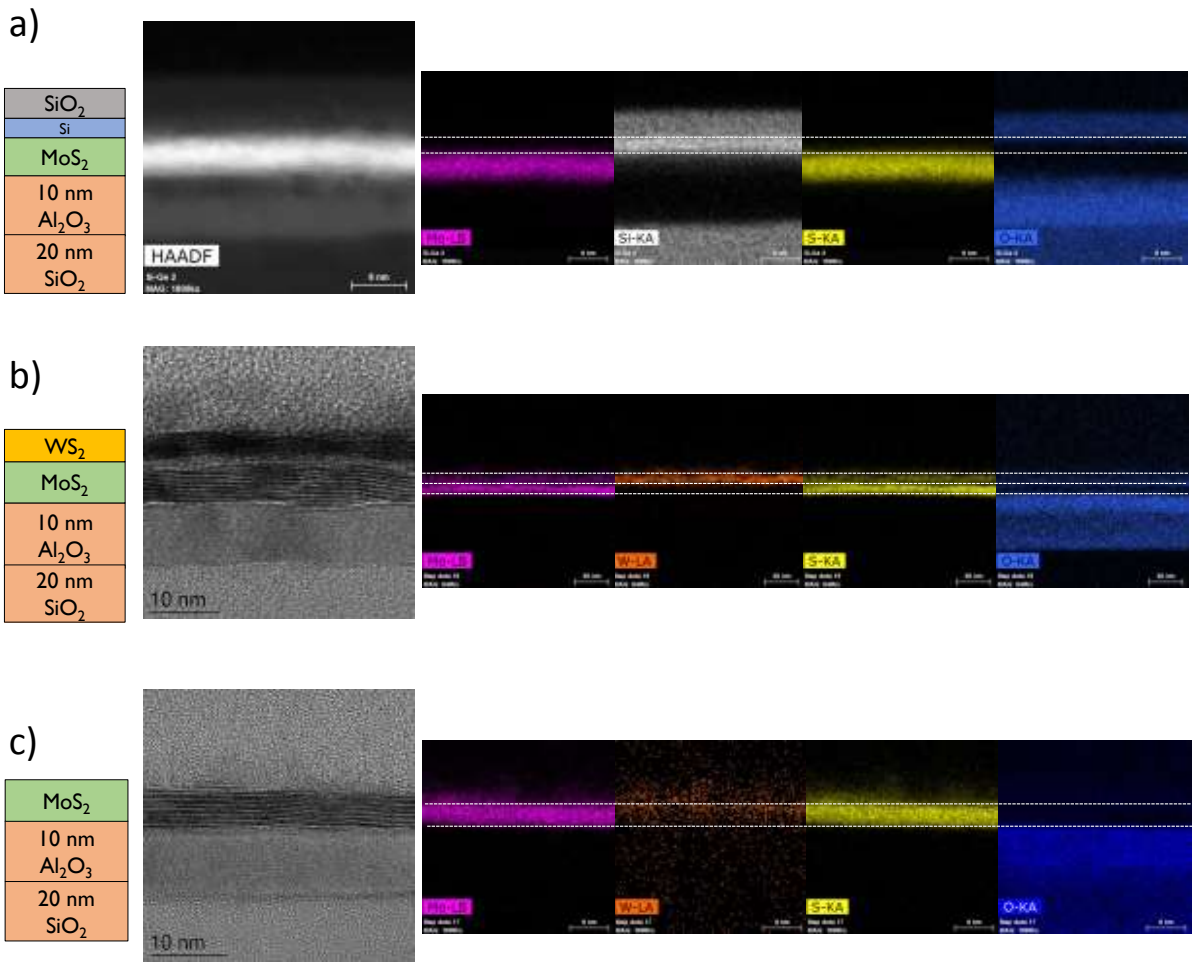

Figure 10: TEM cross-section images showing a) the heterostack with the elemental Si and the SiO_2 hardmask; b) the region which was covered during ALEt by the hardmask and then converted to W and sulfurized, and c) the MoS_2 from which the Si was etched by ALEt.