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Through-substrate coupling elements for silicon-photonics based short-reach optical interconnects

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ABSTRACT

Laser integration and photonics chip packaging are the two key challenges that require attention to drive down the cost/bit metric for silicon photonics based optical interconnects. We try to address the latter by demonstrating optical interfaces that fit well in an overall scheme of 2.5D/3D electro-optic integration needed for a high performance computing environment.
A through-substrate coupling interface provides the benefit of bonding a silicon photonic chip face-up on a package substrate such that the device-side of the chip remains accessible for die-stacking and fiber-array packaging, thereby offering a promising alternative to flip-chip based packaging. In this paper, we demonstrate three through-substrate coupling elements to enable alignment tolerant and energy-efficient integration of silicon photonics with board-level or package-level optical interconnects : (i) a downward directionality O-band grating coupler with a peak -2.3 dB fiber-to-silicon waveguide coupling efficiency; (ii) polymer microlenses hybrid integrated onto the substrate of a silicon photonic chip to produce an expanded collimated beam at λ=1310 nm for a distance of more than 600 μm; (iii) a ball lens placed in a through-package via to result in a 14 μm chip-to-package 1-dB lateral alignment tolerance for coupling into a 20×24 μm squared cross-section board-level polymer waveguide.

Keywords: Ball Lens, Chip-to-Board Coupling, Grating Couplers, Microlenses, Optical Interconnects, Photonics Interposer, Polymer Waveguides, Silicon Photonics Packaging

1. INTRODUCTION

Energy efficiency and high channel bandwidth is a significant requirement for interconnect applications between high-performance servers in modern datacenters.[1,2] For distances within a few hundreds of meters, optical interconnects offer a promising solution to achieve a larger bandwidth-distance product, interconnect density and power efficiency compared to their electrical counterparts. As of today, most of the servers across datacenters employ VCSELs operating at wavelengths in the near-infrared range between 780 nm and 980 nm, due to their low cost of deployment and reliability.[3] Most of these components have been used to enable bandwidth-limited multimode-optics based solutions for short-reach interconnect distances of upto 100 m (using OM4 fibers). Although there has been a tremendous effort to develop VCSELs for wavelengths of 1 μm and above, cost and bandwidth have been a challenging factor and that's where silicon photonics based technology has the potential to penetrate the landscape of electro-optic integration, bringing single-mode transmission, dense integration and wavelength division multiplexing capabilities along with it. In reference to Fig. 1, we try to show one of the possibilities of integration of a silicon photonics interposer chip where the laser and CMOS driver component are packaged onto the photonics interposer chip, with distance between the ASIC logic kept as close as possible to achieve mid-board co-packaged, low-latency and high-bandwidth optical solution. While embedding TSVs in photonics interposer enable the package/board-level electrical connections in this scheme, an efficient and alignment-tolerant through-substrate coupling mechanism between the photonics interposer and package/board-level optical interconnect can help push the cost-level benefit further towards silicon photonics.

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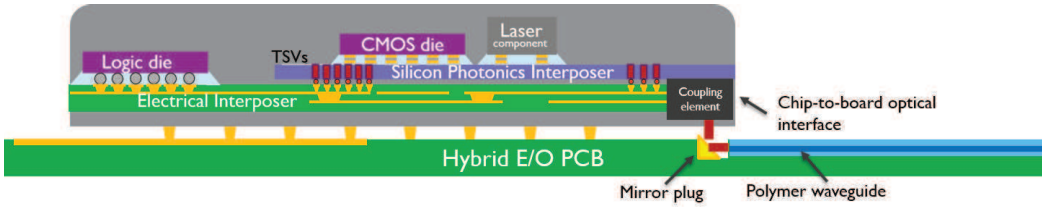


Figure 1: Overview of 2.5D/3D integration of Silicon Photonics for chip-to-board coupling.

In this paper, we highlight our progress in developing through-substrate coupling elements to enable photonics chip-to-board coupling. A through-substrate coupling interface provides the benefit of bonding a silicon photonics chip face-up on a package substrate such that the device-side of the chip remains accessible for die-stacking and fiber-array packaging, thereby offering a promising alternative to flip-chip based packaging. In addition, such interfaces can find utility in applications such as on-chip sensing and spectroscopy as they provide an alternate route to guide the resultant optical output other than in the conventional direction, with no need of additional back-end-of-the-line(BEOL) processing.

Here, we will discuss three such optical elements described as follows:
i) A grating coupler with a metal reflector that has been optimized to couple light from a waveguide to a beam slightly off-normal in the downward direction through the bulk silicon substrate of an SOI chip. The device then acts as a building block to interface with two other coupling elements described further (Section 2).
ii) Integration of microlenses on the backside of the photonics chip SOI substrate such that the expanded downward directed beam from the grating coupler is subsequently collimated. An expanded mode-field diameter helps in providing lateral alignment tolerance and collimation of the beam helps to achieve longitudinal alignment tolerance (Section 3).
iii) Integration of a ball lens inside a through-package via to refocus the downward directed optical beam from the photonic chip interposer to a board-level polymer multimode waveguide with good alignment tolerance (Section 4).

2. THROUGH-SUBSTRATE GRATING COUPLERS FOR DOWNWARD DIRECTIONALITY

2.1 Design concept

Grating couplers are a key passive optical component to perform wafer-scale testing of integrated photonic circuits.[4] Although they are bandwidth-limited and more polarization-sensitive compared to edge-couplers, they are more alignment tolerant, which is beneficial for both wafer-scale testing and packaging purposes. As of today, circuit-level prototyping has been simplified by the use of on-chip grating couplers. While gratings for upward directionality have been studied extensively, only a few instances have been reported of couplers diffracting in the direction of the substrate.[5,6] One of the ways to increase the grating coupler directionality toward the substrate is to deposit a metal reflector on top of the grating. By depositing a Ti/Al reflector on the oxide cladding above the diffraction grating, a coupler with a mixed directionality can be modified to realize a dominant downward directionality by exploiting constructive interference between the downward diffracted optical field from the grating and the upward diffracted field reflected downwards from the metal reflector. For the O-band wavelength of 1310 nm and a grating with a 10° diffraction angle, a 2 μm oxide thickness is derived by performing a parameter sweep of the top oxide thickness in 2D FDTD simulations, as shown in Figure 2. The grating couplers for downward directionality were designed for parameters corresponding to a standard SOI wafer with a 220 nm thick silicon waveguide layer and a 2 μm thick buried oxide layer (BOX). The gratings were designed with a period and etch depth of 490 nm and 70 nm respectively for TE polarization.

2.2 Results

The photonic chips used to perform grating coupler measurement and subsequent packaging experiments were obtained from wafers fabricated in imec's 200 mm Si Photonics pilot line. A further post-processing was per-

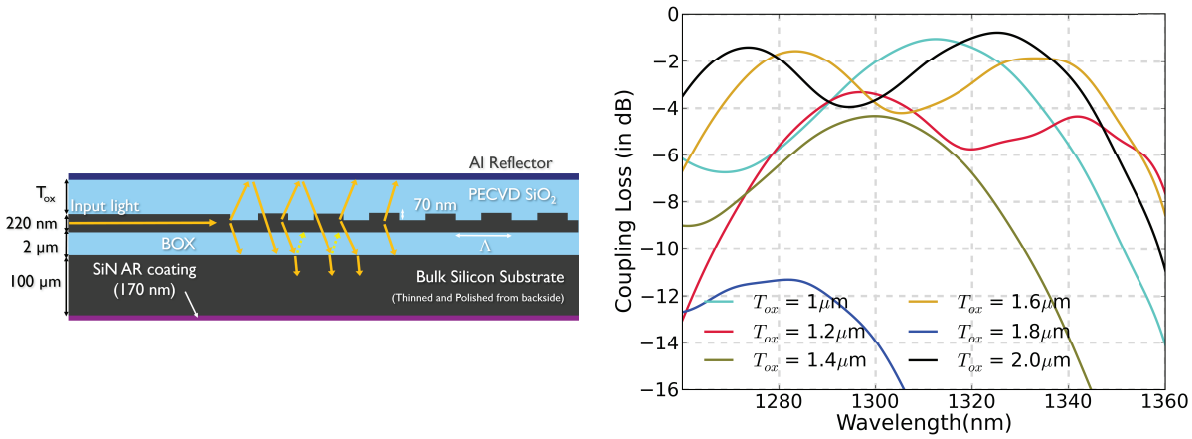
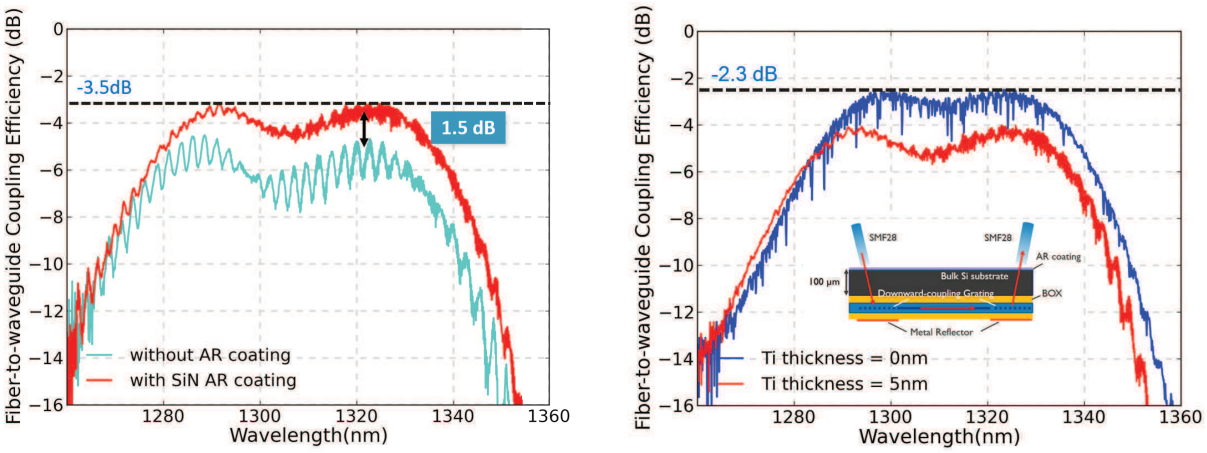


Figure 2: (a) Schematic of an SOI grating coupler for through-substrate coupling. Grating parameters: $\Lambda = 490$ nm, Fill-Factor = 0.5, Etch depth = 70 nm, Top silicon thickness = 220 nm, Bulk silicon substrate thickness = 100 μm, T_{ox} = oxide thickness that is optimized for downward directionality. (b) Effect of oxide thickness on fiber-to-grating coupling efficiency spectrum as calculated by 2D-FDTD simulations.

formed on the dies to deposit a 5nm Ti + 200 nm Al metal reflector on top of the gratings. These chips were then temporarily bonded onto a glass carrier to perform substrate-side lapping and polishing of the dies[7] starting with a silicon thickness of 650 μm to a final value of 100 μm. After releasing the dies from the glass carrier with the help of a solvent, a 170 nm SiN anti-reflective(AR) coating was deposited on the polished substrate-side of these chips. The RMS surface roughness after polishing was measured to be within 15-20 nm over an area of 1.5×1.5 cm^2 using an optical profilometer. The dies were then flip-mounted onto a vacuum chuck so that perpendicularly-cleaved fibers oriented at a 10° angle could be used to couple through the silicon substrate in and out of the gratings from the backside of the chip. When no AR coating was applied at the chip backside, a peak fiber-to-waveguide coupling efficiency of -5 dB was obtained for an optimal thickness of top oxide (Fig. 3a). The free spectral range (FSR) of the ripples in the spectrum caused by Fresnel reflections from the silicon-air interface



(a) (b)

Figure 3: (a) A 1.5 dB improvement in the coupling efficiency of the grating occurs after the application of SiN anti-phase coating at the substrate side of the chip. (b) Reduction in the thickness of the adhesion layer between the grating and metal reflector results in a net reduction of absorption and an improvement in the overall fiber-to-grating coupling efficiency.

correspond approximately to a 100μm thickness of silicon. After the deposition of AR coating,[8] a reduction in the ripple amplitude and an improvement in the coupling efficiency by a 1.5 dB margin was obtained as shown in Fig.3a. It was also found that the thickness of the adhesion layer (Ti) between the Al reflector and planarized oxide impacts the overall reflectivity and hence, the coupling efficiency. From Fig. (3b), it can be seen that when compared to 5 nm Ti adhesion layer, a 1.7 dB improvement in the coupling efficiency occurs after the removal of the adhesion layer between the metal reflector and the oxide cladding.

2.3 Chip-to-Package Coupling

For coupling between photonics chip to package-level optical interconnects, the distance between the chip and the package substrate is roughly determined by the dimensions of the solder balls and metallic pads needed for a particular application. Keeping that in mind, some preliminary coupling tests were performed in integrating a thinned photonics chip directly with polymer waveguides on a package substrate.[9] In this experiment, a downward directed beam from a grating coupler was directly coupled into a polymer multimode waveguide on the package substrate via a 40° metallized mirror plug placed in an optically transparent underfill. The polymer multimode waveguides had a cross-section of 50×50 μm^2. The fabrication and packaging of board-level optical components are explained in Section 4. At the time of performing this experiment, the grating couplers were not fully optimized and hence, the fiber-to-through-substrate grating coupler efficiency was measured to be -6.5 dB. Also, the input grating coupler had a metal reflector on the topside and was packaged from the backside of the chip using an angle-polished fiber.[9] This incurred additional losses caused by the beam expansion in bulk 100 μm silicon and the bottom fiber cladding of 60 μm. The loss contribution from the input packaged grating coupler was measured to be 11 dB. A minimum optical loss of 7.6 dB was measured at the die-to-package interface in O-band and a lateral 1-dB alignment tolerance of 25 μm was measured between chip-to-package-level polymer waveguide (Fig. 4). The losses could easily be reduced by packaging the die from the topside, use of AR coating on the chip backside as shown already in other demonstrations here. For single-mode operation, a backside lensing scheme can be used to perform chip-to-package/board coupling with good alignment tolerance.

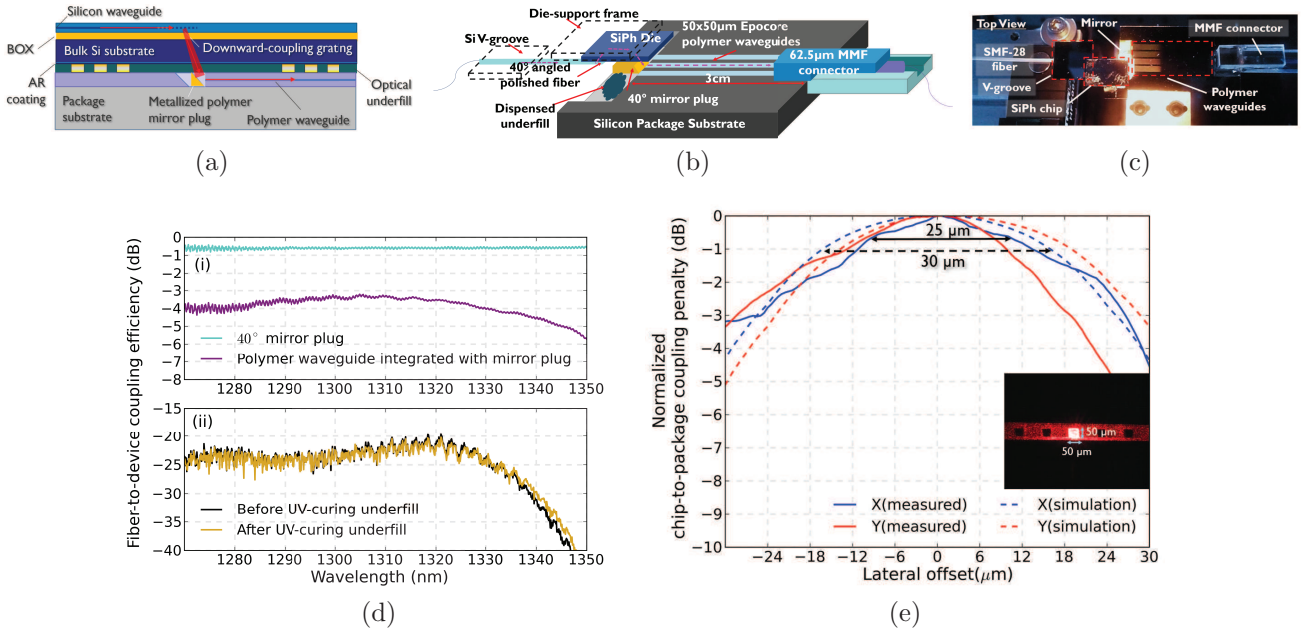


Figure 4: (a) Cross-section schematic of chip-to-package interface. (b) Schematic of photonic chip-to-package substrate assembly procedure. (c) Chip-to-polymer multimode waveguide packaged demonstrator. (d) (i) Loss of package substrate components (ii) Total angle-polished SMF-28-to-multimode fiber loss of packaged demonstrator. (e) Measured vs. simulated normalized lateral alignment tolerance between photonic die and polymer waveguide.

3. INTEGRATION OF SILICON PHOTONICS WITH BACKSIDE MICROLENSES

It is well-known that the on-chip grating couplers enable a 1-dB lateral alignment tolerance of $\pm 2.5\mu$m to a standard single-mode fiber. Despite offering a relaxed alignment tolerance compared to edge-coupling solutions, an active alignment step is still required through a "shunt" or "dummy" grating coupler during a multi-channel fiber-array packaging. A passive alignment based strategy not only renders the PIC packaging arena into the pluggable-optics domain but also helps reduce the cost of a PIC based product finding its applications in health-care, automotive and datacom market. This can be achieved by expanding the beam diffracted by a through-substrate grating coupler and collimating it from the chip backside by fabricating a microlens array on the substrate-side of a photonics chip (Fig. 5). Although a monolithic solution for integrating the microlenses is the ultimate goal,[10] we discuss here an intermediate step of hybrid-integrating a photonics chip with polymer microlens fabricated on a separate dual-side polished Si substrate.[11] Although the concept of an expanded beam collimation itself can be realized from the topside of the chip as has been described comprehensively already,[12] yet a through-substrate coupling allows for an alternative approach of doing face-up integration of the photonics chip and helps provide easy access to the device-side for advanced packaging technologies. In addition, it provides the designer with various degrees of freedom to choose between chip substrate thickness, starting mode-field diameter of the designed grating to allow a desired expansion and phase transformation of the beam propagation through the bulk silicon substrate.

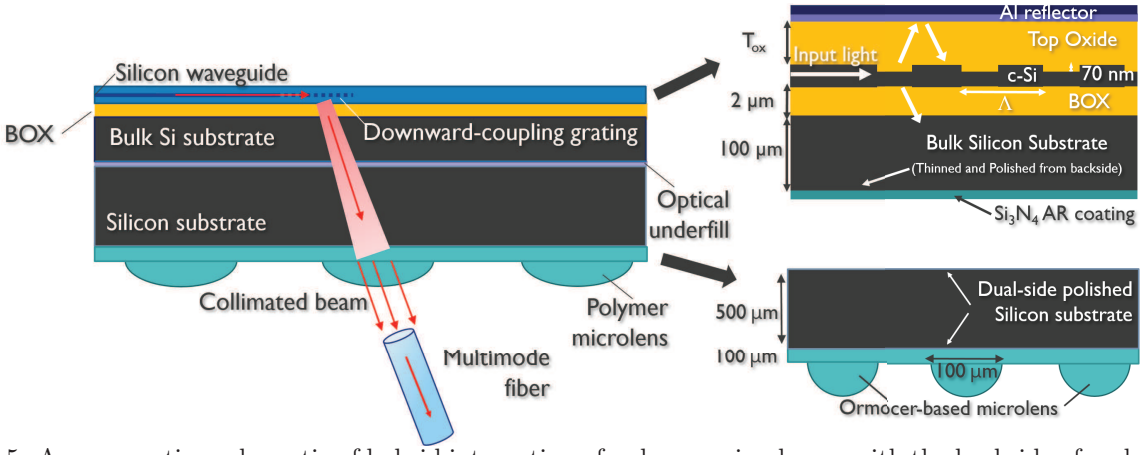


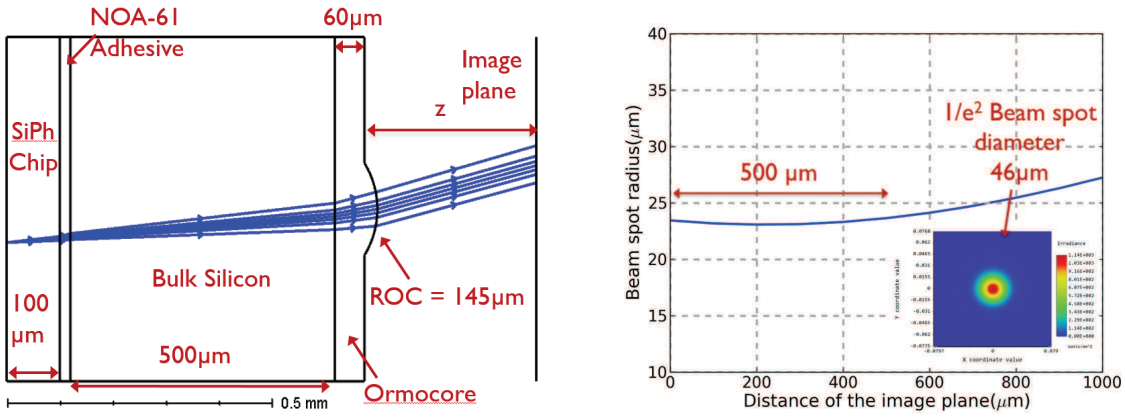
Figure 5: A cross-section schematic of hybrid integration of polymer microlenses with the backside of a photonics chip comprising of through-substrate grating couplers.

3.1 Microlens Design

In order to derive the parameters of the microlens for expanded beam collimation, firstly, a ray-trace based model is developed (Fig. 6a). The thickness of the Si substrate on which the polymer lenses were fabricated, was taken to be 500μm, which allows for sufficient expansion of the incoming diffracted beam from the output grating coupler. The thickness of the chip substrate was taken to be 100μm, keeping synergy with the through-substrate coupling interface analysis provided in Section 2. The far-field divergence of the output grating coupler, as determined from the 2D-FDTD simulations, was incorporated in the ray source of the model. Using Gaussian beam-propagation analysis within Zemax model, a parameter sweep for the radius of curvature (ROC) of the lens was performed to yield an optimal value of 145 μm radius of curvature for a lens diameter of 100 μm, achieving a collimation range of 500μm with a beam diameter of 46 μm (Figure 6b).

3.2 Fabrication and Assembly

For the fabrication of microlenses, UV-based imprinting of Ormocer material was used to form polymer microlenses on a silicon substrate.[13] In order to make the master stamp, a UV-sensitive AZ4562 photoresist was patterned onto a glass substrate and the microlenses were obtained by reflow of the cylindrical structures obtained post-patterning at 120° C. Assuming a perfect spherical shape of the microlens, the thickness T_{sph} of



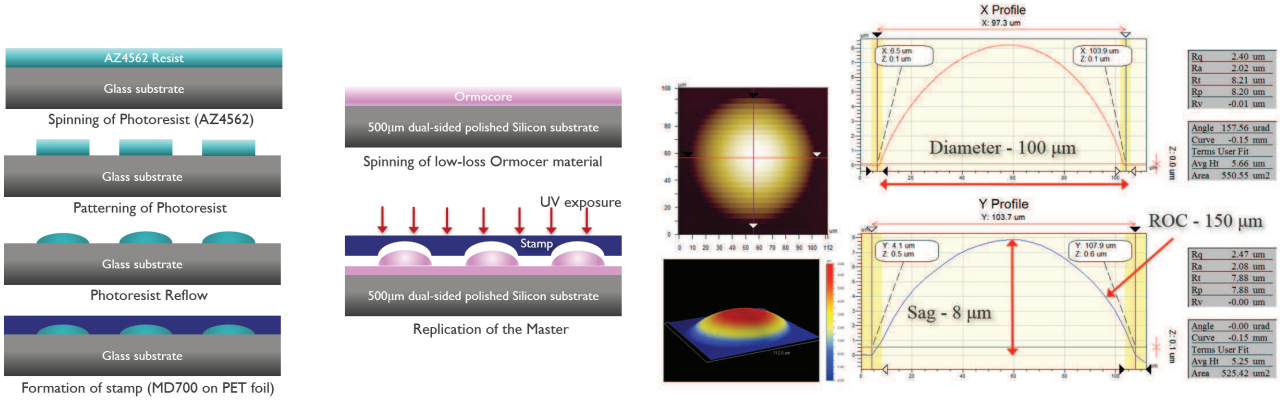
(a) (b)

Figure 6: (a) Ray-trace model of the chip-lens hybrid integrated system and (b) Evolution of the spot radius of a Gaussian beam as it propagates from the apex of the lens (z=0).

photoresist needed to obtain a microlens of a given radius, r and sag, h is given by Equation 1, while the lens sag, diameter and radius of curvature are related by Equation 2,:[14]

$$T_{sph} = \frac{h}{6}\left[3 + \frac{h^2}{r^2}\right] \quad (1) \qquad h = R - (R^2 - r^2)^{(1/2)} \quad (2)$$

These equations provide a good starting point for the resist thickness needed for a given diameter and curvature of the lens. After further optimization to arrive at a desired physical parameters of the microlens post reflow, a negative of microlenses was made to perform UV imprinting. For this, a soft stamp was made by dispensing Solvay MD700 material on top of a PET foil and bringing it in contact with the reflowed microlens structures on the glass substrate. After this, micro resist technology GmbH Ormocore material was spun onto one side of the 2-sided polished silicon substrate, over which the master foil was rolled over and UV cured to replicate the designed microlenses. A 3D-surface profile measurement over the microlenses resulted in a diameter and radius of curvature of 100 μm and 150 μm respectively, that matches closely with the intended design specs obtained from the ray-trace model(Fig. 7b). In order to perform the hybrid integration, the input grating coupler



(a) (b)

Figure 7: (a) Process flow for UV imprinting of microlenses and (b) A diameter = 100 μm and radius of curvature = 150 μm was obtained through 3D surface profile measurement performed with stylus-based profilometer.

on the photonic chip was packaged from the topside using a 40° angled-polished fiber.[15] The packaged photonic module was flipped in order to see the output grating coupler's beam profile from the backside of the chip via an IR camera. With the substrate consisting of microlens array held on a vacuum chuck, the flipped photonic module was brought underneath it and an active alignment of the output grating to microlens was performed with the aid of an IR camera (coarse alignment) and by coupling into a fiber from the side of the microlens (fine alignment). The bonding between the silicon substrate and the photonic chip was then performed using NOA-61.

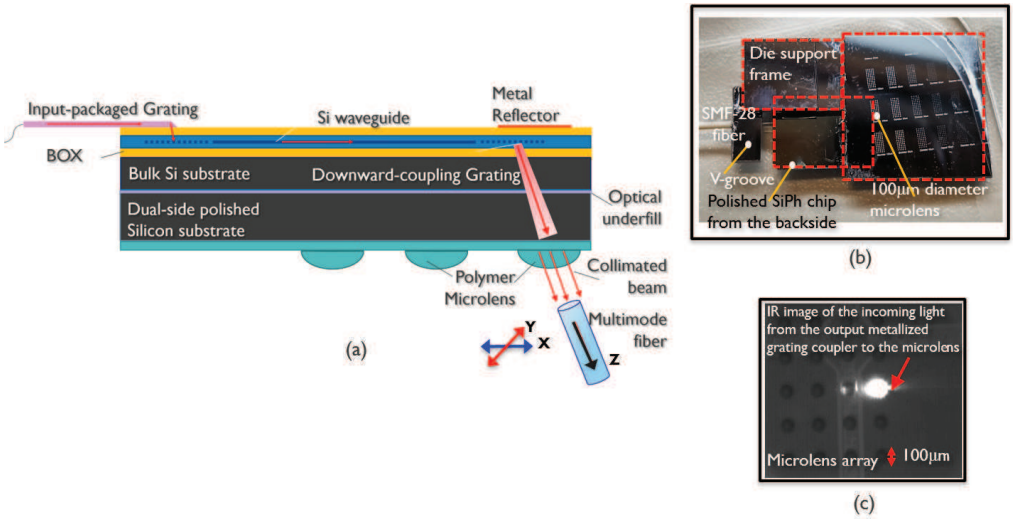
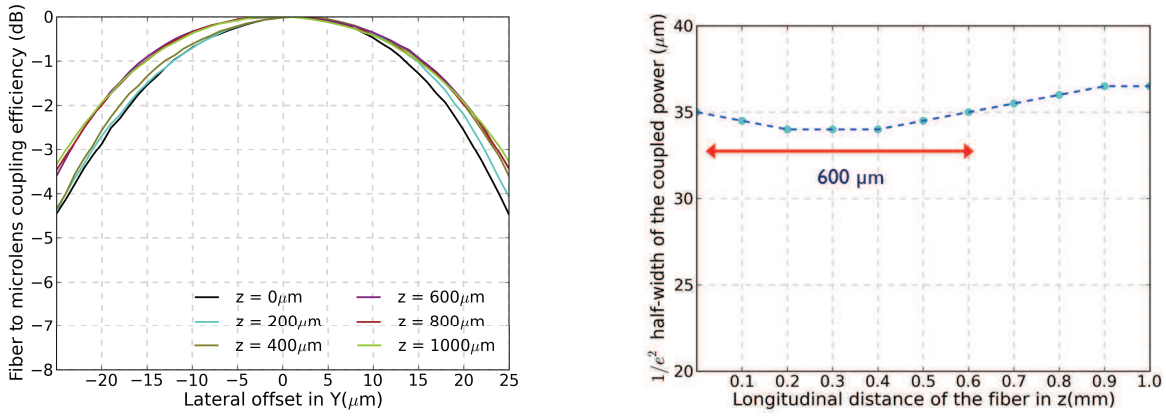


Figure 8: (a) Schematic of the packaged photonics chip integrated with polymer microlens. (b) An image of the packaged PIC-microlens module. (c) IR image of the incoming light from the output metallized grating coupler to the microlens.

3.3 Results



(a) (b)

Figure 9: (a) Normalized fiber-to-microlens coupling efficiency vs. lateral offset of a 0.2 NA multimode fiber and (b) Plot of $1/e^2$-width of the fiber-coupled power as a function of distance from the vertex of the microlens.

After the hybrid integration of polymer lenses with the packaged photonics chip was done, the optical output from the microlens assembly was coupled into a 50 μm core diameter 0.2 NA multimode fiber. The objective of using a multimode fiber was to establish the concept of collimation while still being able to couple an expanded

beam into the larger core diameter of the fiber. The fiber was first actively aligned at the intended angle of coupling with respect to the vertex of the microlens. A lateral scan of the fiber was performed in both the longitudinal and lateral directions with respect to the hybrid integrated grating-microlens system. The fiber was then retracted from the apex of the lens a fixed distance along the optical axis and then the same alignment process was performed. This was repeated for several points along the z-distance at fixed increments of 100 μm. The normalized power profile of the fiber to microlens along the y-direction has been shown in Fig. 9a. It can be seen that a 1-dB lateral alignment tolerance of 12 μm was measured as has been confirmed by another demonstration for similar mode-field diameters (between 40-45 μm).[10] The $1/e^2$-width of the aligned power profile was then compared with the longitudinal distance to determine the degree of collimation of the expanded beam (Fig. 9b). The minimal variation between the scans performed at successive distances from the hybrid integrated photonics chip-microlens system indicate that the output beam remains collimated over a distance of approximately 600 μm.

4. LENSED VIA FOR CHIP-TO-BOARD COUPLING

For chip-to-board coupling, while the expanded beam collimation with through-substrate coupling yields an improvement of lateral and longitudinal alignment tolerance, it comes at the expense of stringent angular alignment tolerance. Also, an inverse lensed collimation system is required to really benefit in coupling two beams with expanded mode field diameters at both the input and output interfaces. If the number of backside processing steps needs to be reduced, an off-chip lensing solution can be sought that is compatible with existing high-throughput assembly-level manufacturing facilities. In that respect, a lensed package substrate can be integrated with the photonics chip to perform chip-to-board coupling.[16] Here, a ball lens is placed into a laser-drilled via inside the package substrate (Fig.10). The incoming divergent optical beam from the bulk silicon substrate of the photonic interposer chip is refocused with the help of the ball lens. By controlling the laser-induced taper inside the package substrate, a ball lens can be made to sit at a desired location inside the via of the package substrate. The focused optical beam is then coupled into a board-level polymer waveguide, after reflecting off a 40° metallized mirror plug integrated in a laser-ablated cavity. The guided optical power in the polymer waveguide is detected with the help of a packaged multimode fiber connector. This approach allows for a natural beam expansion from the photonics chip in the free space between the chip and the ball lens. Also, the approach benefits from the via-processing technology available in PCB manufacturing facilities, which can be leveraged to perform a coarsely-aligned pick-and-drop approach of embedding ball-lenses inside the via of a package substrate on a larger volume.

4.1 Design

In order to understand the optical propagation physics of the overall system, a non-sequential Zemax ray-trace model was designed (Fig. 11a). Here, the distance between the chip and the polymer waveguide was limited by

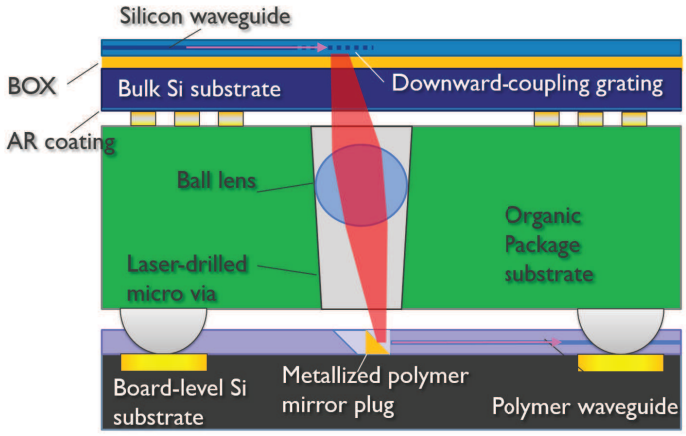
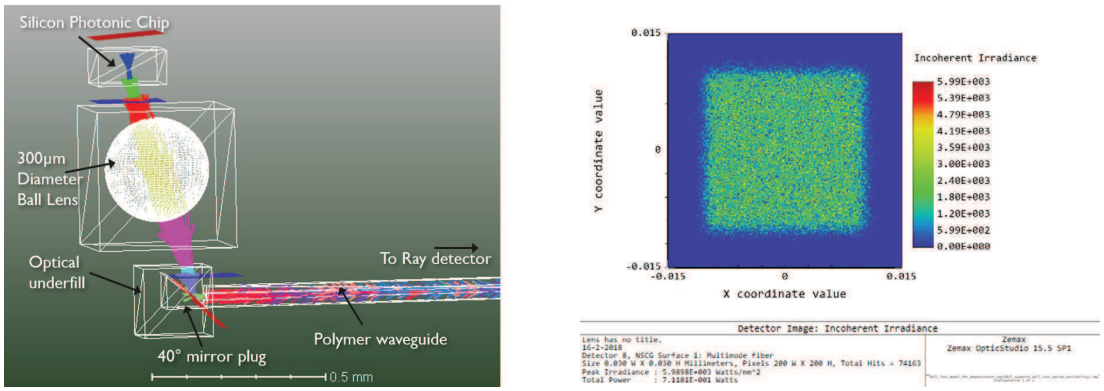


Figure 10: Schematic of Chip-to-board coupling interface

the thickness of the package substrate which was taken to be 500 μm in the model. A detector was placed at the opposite end of the polymer waveguide to detect the percentage of rays that were coupled through the ball lens and the 40° mirror plug into the waveguide core. The ray-trace calculations at a wavelength of 1310 nm indicated that for a given chip-to-board distance, the optimal coupling efficiency that is possible using active alignment of the chip is 71% (Fig. 11b).

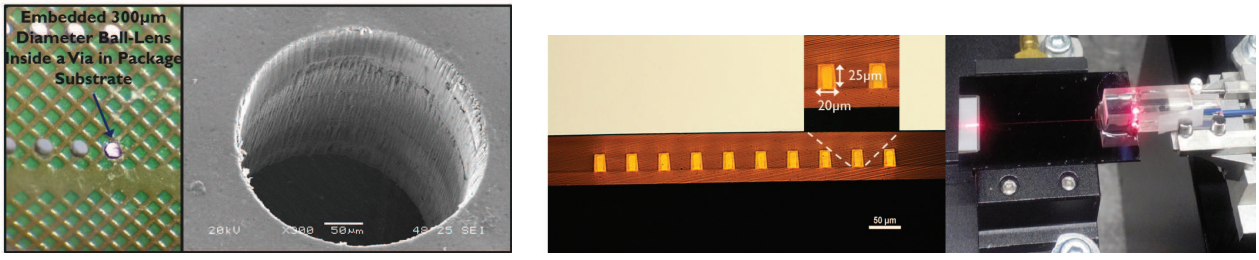


(a) (b)

Figure 11: 71% coupling efficiency was detected by the ray-detector placed at the opposite end of the polymer waveguide in the Zemax ray-trace model for photonic chip-to-board coupling.

4.2 Fabrication and Assembly

The packaging of the input grating on the photonics chip was performed as explained in previous sections. For the lensed substrate, a thru-hole via was created inside a 400 μm thick organic package substrate with the help of a pulsed Nd-YAG laser. The surface roughness of the via was qualitatively inspected using SEM imaging and optical microscope to determine the opening and the exit diameter of the ablated via. A 300 μm diameter ruby-doped sapphire ball lens was placed inside the laser-drilled via of the package substrate (Fig.12a). To demonstrate coupling to a board-level optical interconnect, polymer waveguides were fabricated on a silicon substrate with the help of laser-direct write method,[17] which is compatible with panel-level manufacturing. The Epocore/Epoclad material system (micro resist technology GmbH) was used to form the polymer waveguide stack. The waveguide propagation loss was determined with the help of the cutback method and it was found to be 0.8 dB/cm in the O-band for $\lambda = 1310$ nm. A 3 mm-wide cavity was made at one end of the polymer waveguide with the help of UV-excimer laser ablation to insert a gold coated 40° mirror plug that was fabricated out of a polyimide substrate.[18] The measured rms surface roughness of the mirror plug was found to be between 15-20 nm. The

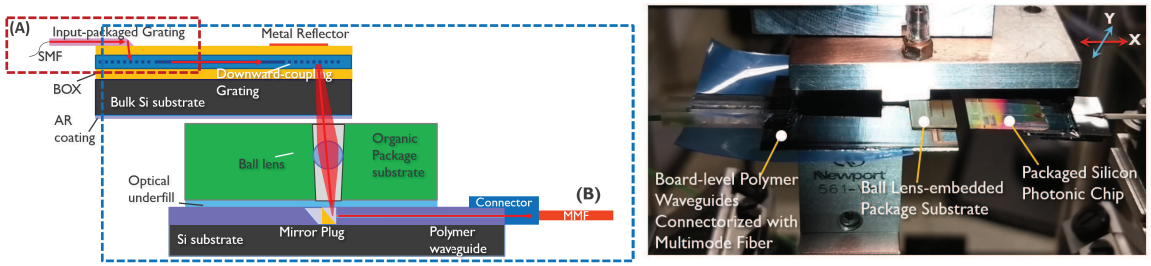


(a) (b)

Figure 12: (a) A microscope image of a ruby-doped sapphire ball lens embedded inside the via of a package substrate. Sidewall-surface quality of the via with SEM inspection. (b) A microscope image of the cross-section of the fabricated polymer waveguides and laser-ablated cavity for inserting the mirror plug into polymer waveguides connectorized at the opposite end.

opposite end of the polymer waveguide was packaged with a 0.2 NA 50 μm core diameter multimode fiber via a custom-made connector (Fig.12b).

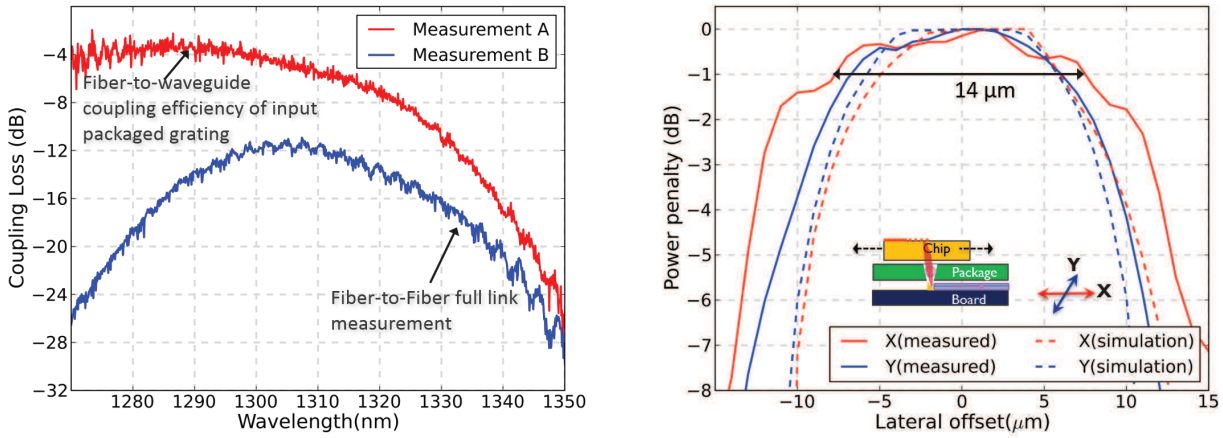
4.3 Results



(a) (b)

Figure 13: (a) The schematic of the experiment carried out in two stages: (A) Measurement of Fiber-to-waveguide coupling efficiency of the packaged input grating and (B) Measurement of SMF-to-MMF full link spectrum of the demonstrator after the assembly of the individual components using active alignment; (b) With the board-level substrate held on a vacuum chuck and ball-lens embedded package substrate aligned with respect to the polymer waveguide, the packaged photonic chip was aligned actively with the ball lens to facilitate chip-to-board level polymer waveguide coupling.

While the peak coupling efficiency of the packaged input grating was measured to be -3.5 dB (Measurement A), the coupling efficiency at a wavelength of 1310 nm was measured to be -5 dB (Figs. 13a and 14a). Measurement B in Fig.14a shows the spectrum measured across the full link, i.e., from the single mode fiber packaged to the input grating on the photonic chip to the multimode fiber connected at the end of the polymer waveguide. With the help of these two measurements, the true coupling loss across the chip-to-polymer waveguide optical interface comprising the output grating, ball-lens and mirror plug was determined to be 3.4 dB at a wavelength of 1310 nm as tabulated in Fig.15. Also, a 14 μm chip-to-package lateral alignment tolerance was measured compared to an estimated 12 μm alignment tolerance obtained from the Zemax ray-tracing simulations (Fig. 12). It can also be seen that a better overall alignment tolerance in the X-direction than that in the Y-direction is representative of the coupling into a polymer waveguide cross-section of 20×24 μm^2. Thus, a multimode-optics



(a) (b)

Figure 14: (a) Measurement A: Single-mode fiber-to-waveguide coupling efficiency spectrum of input packaged grating on the photonic chip; Measurement B: Input Fiber-to-Output Fiber full link spectrum. (b) A 1-dB chip-to-package substrate lateral alignment tolerance of 14 μm was measured.

based photonics chip-to-board coupling interface can be realized with the help of a ball-lens in the package substrate, where a photodetector chip can be expected to be interfaced at the receiver side in a similar way, thereby avoiding the need to adopt a a two-lensed collimator system. Moreover, the loss figure measured from the chip-to-board coupling interface can be further improved from a figure of 3.4 dB to less than 2 dB by using improved directionality gratings as described in section 2.

Various Components & Interfaces	Loss (dB) at λ=1310 nm
Silicon Photonic Chip	
Input Packaged Grating	5
4mm SOI Waveguide Propagation Loss (3dB/cm)	1.2
Output Grating with a Metal Reflector	
Organic Package Substrate	
Ruby-doped Sapphire Ball Lens	**3.4**
Board-level Optical Interconnect	
40° Au-coated Mirror plug	
3cm Polymer waveguide propagation loss(0.8 dB/cm)	2.4
Fiber-to-Fiber Loss Across The Complete Link	12

Figure 15: A 3.4 dB loss across the chip-to-polymer waveguide optical interface at $\lambda = 1310$ nm was deduced from the measurements.

5. CONCLUSION

We have demonstrated three through-substrate coupling elements to enable alignment tolerant and energy efficient face-up integration of silicon photonics with on-package/board optical interconnects :
(i) A downward directionality O-band grating coupler with a peak -2.3 dB fiber-to-grating coupling efficiency;
(ii) Backside microlenses hybrid integrated onto the substrate of a silicon photonic chip to produce an expanded collimated beam with a lateral and longitudinal alignment tolerance of 12 μm and 600 μm respectively;
(iii) A ball lens placed in a through-package via resulting in a 14 μm chip-to-package 1-dB lateral alignment tolerance for coupling into a 20×24 μm^2 cross-section board-level polymer waveguide.
Integrating backside microlenses with a silicon photonics chip benefits from the wafer-scale manufacturing capability and allow for several orders of magnitude lateral alignment tolerance for a coupling interface with single-mode operation on both chip-to-package and chip-to-board optical interconnects. On the other hand, a ball-lens enabled through-package via allows for a simplified chip-backside processing, compatibility with existing PCB manufacturing and assembly flows and relaxed chip-to-package lateral alignment tolerance for coupling to board-level multimode(or few-mode) optical interconnects, interfaced with a photodetector at the receiver side. Overall, we expect that these elements for through-substrate coupling have the potential to allow for an alignment-tolerant integration of TSV-enabled Si-photonics interposers with solder-reflowable packages.

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