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Research Article

Reversible Logic-Based Fault-Tolerant Nanocircuits in QCA

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Parity-preserving reversible circuits are gaining importance for the development of fault-tolerant systems in nanotechnology. On the other hand, Quantum-dot Cellular Automata (QCA), a potential alternative to CMOS, promises efficient digital design at nanoscale. This work targets design of reversible ALU (arithmetic logic unit) in QCA (Quantum-dot Cellular Automata) framework. The design is based on the fault tolerant reversible adders (FTRA) introduced in this paper. The proposed fault tolerant adder is a parity-preserving gate, and QCA implementation of FTRA achieved 47.38% fault-free output in the presence of all possible single missing/additional cell defects. The proposed designs are verified and evaluated over the existing ALU designs and found to be more efficient in terms of design complexity and quantum cost.

1. Introduction

Reversible logic has attractive perspective of constructing digital devices that can realize computing unit with almost zero power dissipation. Landauer [1] proved that for irreversible computations, each bit of information loss generates k_BTln2 joules of heat energy. The energy E_{bit} required for a binary transition is given by SNL (Shannon-Von Neumann-Landauer) expression in [1] as follows:

$$E_{\text{bit}} \geq E_{\text{SNL}} = k_BTln2 = 0.017\,\text{eV}, \quad (1)$$

where k_B is Boltzmann constant and $T = 300\,\text{K}$. This is the minimum energy to process a bit. Bennett [2] showed that a zero power dissipation in logic circuit is possible only if the circuit is composed of reversible logic gates. Since QCA circuits are clocked information preserving systems, the energy dissipation of QCA circuits can be significantly lower than k_BTln2. This feature favours the introduction of QCA technology in reversible logic design.

Though, reversibility recovers bit loss, but it is not able to detect bit error in circuit. Fault-tolerant reversible circuits are capable of preventing errors at outputs. If the system itself made of fault-tolerant components, then the detection and correction of faults become easier and simple. In communication and many other systems, fault tolerance is achieved by parity. Therefore, parity-preserving reversible circuits will be the future design trends to the development of fault-tolerant reversible systems in nanotechnology.

On the other hand, QCA (Quantum-dot Cellular Automata) is considered to be promising in the field of nanotechnology due to their extremely small sizes and ultralow-power consumption [3]. The QCA is based on encoding binary information in the charge configuration of quantum-dot cells. The interaction between cells is coulombic and provides the necessary computing power. The fundamental unit of QCA-based design is the 3-input majority gate [3]. Majority gate with inverter, called MI, is used to realize the QCA designs because of its functional incompleteness.

Significant contributions have been made in the literature towards the design of arithmetic units in [4–6]. Also, fault-tolerant full adder circuits are explored in [7–10]. However, there have only been a few efforts towards designing reversible fault-tolerant ALUs.

This motivates us to design a fault-tolerant reversible ALU architecture considering QCA technology. A cost-effective realization of a fault-tolerant reversible adder (FTRA) is first introduced. It is then utilized to synthesize the desired fault-tolerant reversible arithmetic logic unit which outperforms the efficiency of existing designs in terms of design complexity and quantum cost. The major contributions of this work

around reversible QCA architecture can be summarized as follows:

(i) realization of generic fault-tolerant reversible adder having parity-preserving logic with cost effective quantum cost;

(ii) the presented fault-tolerant reversible adder block is used to realize different arithmetic circuit such as full adder, subtractor, ripple carry adder, and carry-skip logic;

(iii) synthesis of a fault-tolerant reversible arithmetic logic unit (ALU) using proposed adder;

(iv) application of the proposed adder in QCA nanotechnology with effective fault tolerance of 47.38% in the presence of all possible single missing/additional cell defects.

Simulations using QCADesigner [11] supports all the results presented.

2. Preliminaries

Reversible Logic. A logic gate is reversible if the mapping of its inputs to outputs is bijective; that is, every distinct input yields a distinct output, and the number of inputs is equal to the number of outputs [12]. An important cost metrics in reversible logic circuits is the quantum cost. The cost of every 2×2 gate is the same; that is, unity and the cost of 1×1 gate are zero [13]. Any reversible logic can be realized using primitive quantum gates, like 1×1 *NOT* gates and 2×2 reversible gates, such as Controlled-V, Controlled-V^+, and CNOT gate (Figure 1). The quantum cost of a reversible gate can be calculated by counting the numbers of primitive quantum gates used in implementing it. The fan-outs and feedback paths are not permitted in reversible logic.

QCA Basics. A QCA cell consists of four quantum dots positioned at the corners of a square (Figure 2(a)) and contains two free electrons [3]. The electrons can quantum mechanically tunnel among the dots and settle either in polarization P = −1 (logic 0) or in P = +1 (logic 1) as shown in Figure 2(b). Timing in QCA is accomplished by the cascaded clocking of four distinct and periodic phases [3]. The basic structure realized with QCA is the 3-input majority gate, MV (A, B, C) = Maj (A, B, C) = AB + BC + CA (Figure 2(c)). It can also function as a 2-input AND (2-input OR) logic by fixing one of the three input cells to P = −1 (P = +1). Inverter is realized in two different orientations as shown in Figure 2(d). In QCA-based logic implementations, two kinds of wire crossover, termed coplanar crossover and multilayer crossover, are possible. Figure 2(e) describes the coplaner wire crossing considering a 90° (×-cell) and a 45° (+-cell) structures.

Fault-Tolerant Logic. Fault tolerance enables a system to operate properly in the event of the failure of some its components. If the system itself is made up of fault-tolerant components, then the detection and correction of faults become easier and simple. A fault-tolerant (FT) reversible gate is also called conservative gate [7]. The hamming weight of its inputs and outputs is equal. Let the input and output vectors of any fault-tolerant gate be $I_v = I_0, I_1, \ldots, I_{n-1}$ and $O_v = O_0, O_1, \ldots, O_{n-1}$, where

(i) $I_v \langle \text{Bijective} \rangle O_v$,

(ii) $I_0 \oplus I_1 \oplus \cdots \oplus I_{n-1} = O_0 \oplus O_1 \oplus \cdots \oplus O_{n-1}$.

Few fault-tolerant reversible 3×3 gate-like Feynman double gate (F2G), Fredkin (FRG), NFT, and so forth and 4×4 gate like MIG are already investigated.

Table 1: Truth table of proposed fault-tolerant adder.

A	B	C	D	E	P	Q	R	S	T
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	1	1	1
0	0	0	1	1	0	0	1	1	0
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	0	1	1
0	0	1	1	1	0	0	0	1	0
0	1	0	0	0	0	1	1	0	1
0	1	0	0	1	0	1	1	0	0
0	1	0	1	0	0	1	0	0	1
0	1	0	1	1	0	1	0	0	0
0	1	1	0	0	0	1	0	1	0
0	1	1	0	1	0	1	0	1	1
0	1	1	1	0	0	1	1	1	0
0	1	1	1	1	0	1	1	1	1
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1	1	0	0	1	1	1	0	1	1
1	1	0	1	0	1	1	1	0	1
1	1	0	1	1	1	1	1	0	0
1	1	1	0	0	1	1	1	1	0
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	0	0	1
1	1	1	1	1	1	1	0	0	0

3. Related Work

In [14], the feasibility of the parity-preserving approach to design of reversible logic circuits was explored. Few new fault-tolerant reversible logic gates were proposed in [8]. Fault-tolerant full adder circuits are explored in [7–10]. In all these researches, no such single logic unit was identified to implement fault-tolerant full adder. Also, the fault tolerance

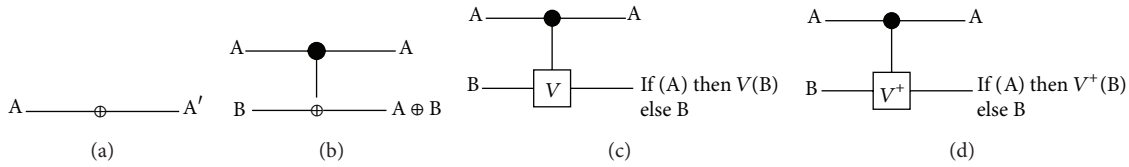


Figure 1: Elementary quantum logic gates: (a) NOT, (b) exclusive OR, (c) square root of NOT (SRN), and (d) Hermitian matrix of SRN.

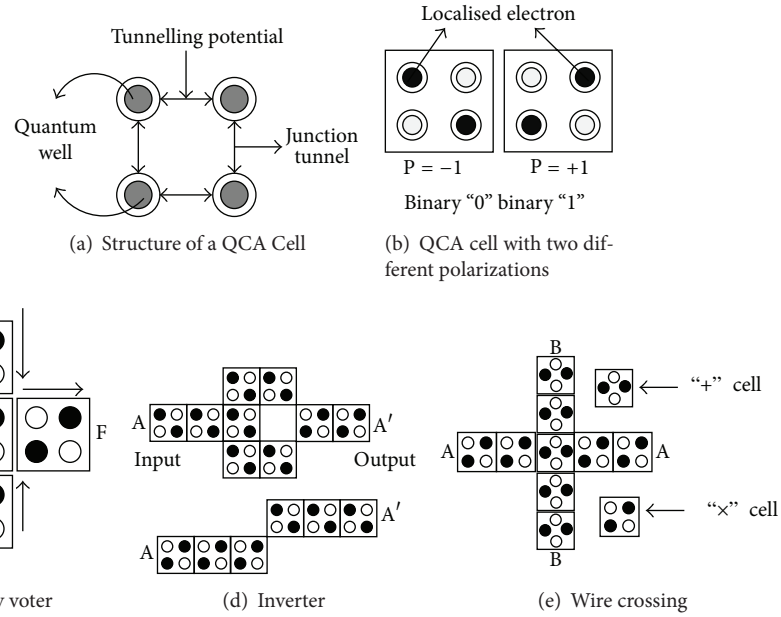


Figure 2: QCA basics.

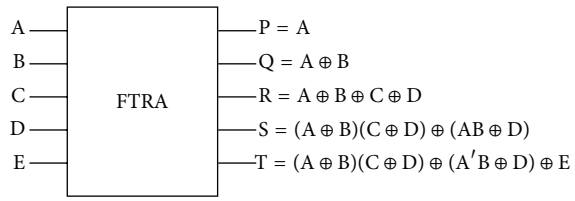
capability of those logic gates was not explored quantitatively. Significant contributions have been made in the literature towards the design of arithmetic units in [4–6]. However, there have only been a few efforts towards designing reversible fault-tolerant ALUs. A new fault-tolerant method based on majority multiplexing (Maj-MUX) is proposed for QCA in [15]. But the application of reversible logic in QCA to achieve fault tolerance was not identified (which is of primary interest to us in this work).

4. Proposed Fault-Tolerant Adder

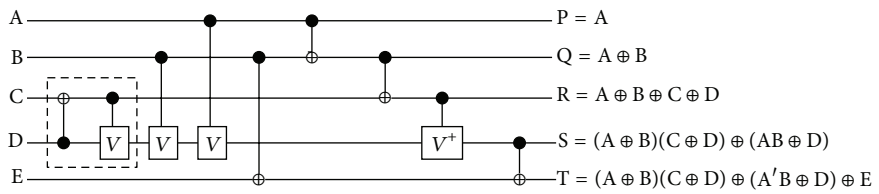
In communication and many other systems, fault tolerance is achieved by parity. A parity-preserving reversible gate, when used with an arbitrary synthesis strategy for reversible logic circuits, allows any fault that affects no more than a single logic signal to be detectable at the circuit's primary outputs [14]. In [10], a minimum number of garbage outputs and constant inputs for a fault-tolerant reversible full adder circuit are specified as 3 and 2. Keeping in mind to have minimum number of garbage outputs and constant inputs, a new fault-tolerant reversible adder (FTRA) is proposed here (Figure 3(a)) followed by design of different adder-based circuits. The input to output mapping of FTRA structure is P = A, Q = A⊕B, R = A⊕B⊕C⊕D, S = (A⊕B)(C⊕D)(AB⊕D), and T = (A ⊕ B)(C ⊕ D)($\overline{A}$B ⊕ D) ⊕ E, where A, B, C, D, and E are inputs and P, Q, R, S, and T are outputs. It is a 5 × 5 reversible gate with a quantum cost of 8 (Figure 3(b)). The proposed reversible FTRA gate is parity preserving. The reversibility and parity preserve nature of the proposed FTRA gate can be verified from Table 1.

A fault-tolerant reversible full adder and subtractor circuit using the newly proposed FTRA gate is shown in Figure 4(a). *The design uses only one FTRA gate, has a quantum cost of 8, produces 3 garbage outputs, and uses 2 constant inputs only*. No such single logic gate is found which can implement a fault-tolerant reversible full adder with such quantum cost and less complexity. Design capability of the proposed adder is further analyzed by implementing a 4-bit fault-tolerant ripple carry adder (Figure 4(b)) and carry skip adder (Figure 4(c)). A comparative performance analysis of the proposed design with existing designs is reported in Table 2 with enviable gate count besides other parameters. The results shows that the proposed design is much more effective than the existing designs.

The advantage of our method is in the implementation of this logic at gate level. Thus, once the required gates have been designed and an appropriate synthesis framework has been established, fault-tolerant implementation requires no extra expenditure in design or verification effort.

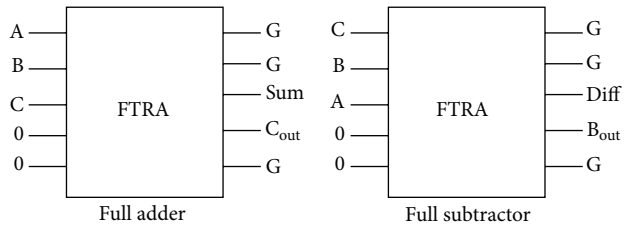


(a) Block diagram fault-tolerant adder

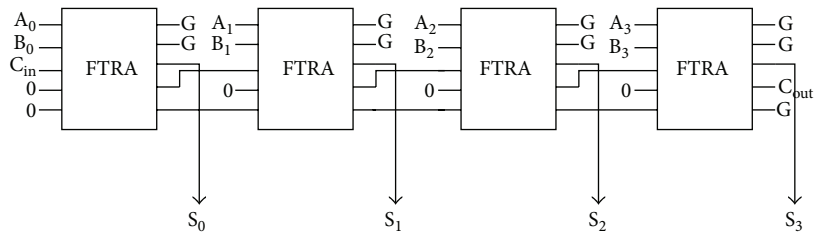


(b) Quantum implementation of fault-tolerant adder

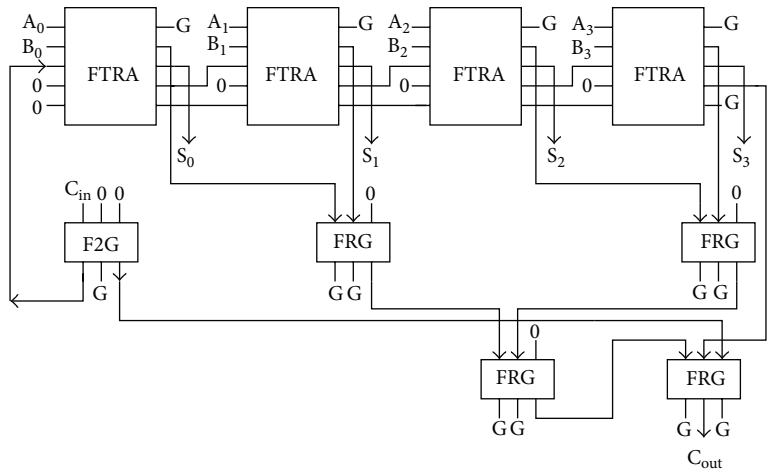
Figure 3: Proposed fault-tolerant reversible adder.



(a) Fault-tolerant full adder and subtractor



(b) Fault-tolerant ripple carry adder



(c) Fault-tolerant carry-skip adder

Figure 4: Implementation of different logic circuit with proposed FTRA.

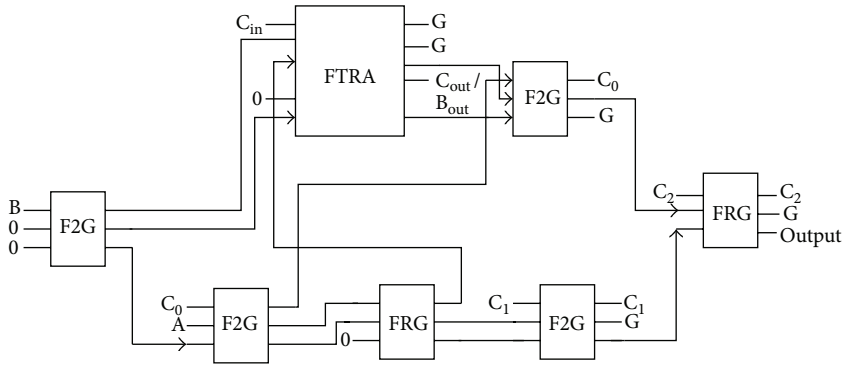


Figure 5: Fault-tolerant ALU with proposed FTRA.

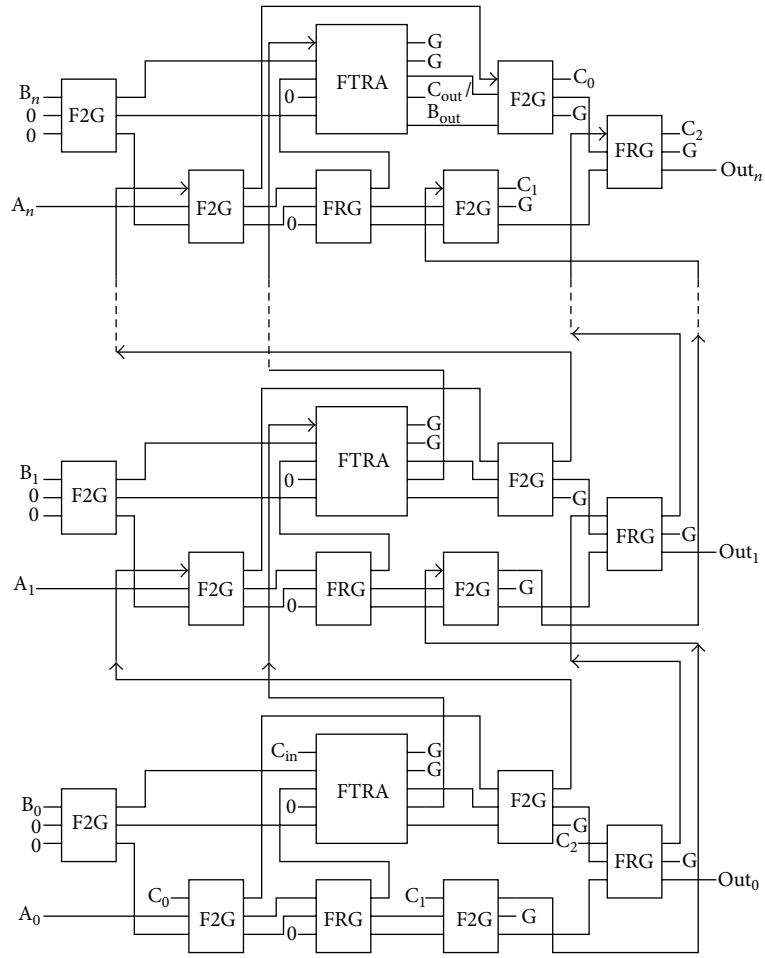


Figure 6: Implementation of n-bit fault-tolerant ALU.

Table 2: Performance analysis of different fault-tolerant full adders.

Parameter	[7]	[8]	[9]	[10]	Proposed
Gate count	5	6	2	4	1
Quantum cost	25	18	14	11	8
Garbage outputs	4	6	3	3	3
Constant inputs	2	5	2	2	2
Logical calculations	$8\alpha + 16\beta + 8\delta$	$12\alpha + 8\beta + 4\delta$	$8\alpha + 6\beta + 2\delta$	$9\alpha + 4\beta + 3\delta$	$13\alpha + 4\beta + \delta$

α: "two-input EXOR calculation"; β: "two-input AND calculation"; δ: "NOT calculation."

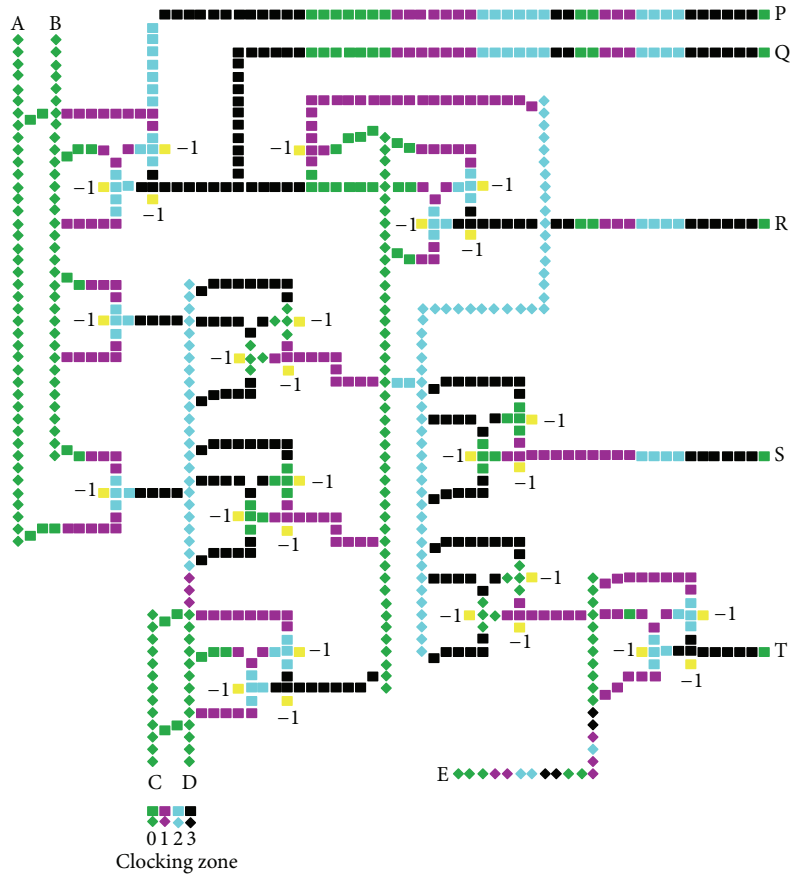


Figure 7: QCA implementation of fault-tolerant adder.

Table 3: Different function of ALU.

C0	C1	C2	Output	Function
0	0	0	AB	AND
0	0	1	$\overline{A + B}$	NOR
0	1	0	$\overline{AB}$	NAND
0	1	1	A + B	OR
1	X	0	$A \oplus B \oplus C$	ADD
1	X	1	$A \oplus B \oplus C$	SUB

4.1. Design of Fault-Tolerant Arithmetic Logic Unit (ALU). The reversible fault-tolerant 1-bit ALU is designed with one FTRA gate, two Fredkin gates, and four Double-Feynman gates. Thus the design uses a total of 7 gates and has a quantum cost of 26 (Figure 5). It produces 5 garbage outputs and uses 4 constant inputs. The various operations performed by the proposed FTRA-ALU is shown in Table 3. The total logical operations performed is $21\alpha + 10\beta + 5\delta$. The main advantage of the proposed ALU logic is its programmable feature; that is, just programming the constants C1, C2, and C3, different ALU functions are implemented. Besides its fault tolerance, this programmable feature adds more flexibility in reversible ALU. Figure 6 shows the design of an n-bit fault-tolerant ALU which is synthesized by cascading the 1-bit ALU module explored in Figure 5.

5. FTRA Gates in QCA Computing

To demonstrate the application of the proposed fault-tolerant design approach to reversible adder in emerging nano-technologies, Quantum-dot cellular automata (QCA) technology is considered because reversible logic has potential applications in QCA computing. The QCA implementation of the proposed FTRA gate is shown in Figure 7. The design requires 27 MVs and has a delay of 12 clock zones. In the following section, the fault tolerance capability is established quantitatively. FTRA simulation shown in Figure 8 is performed by fixing D and E to 0. In this simulation result, R generates sum, and S propagates carry.

6. Fault Tolerance of Proposed Logic Gate

In QCA manufacturing, defects can occur during the synthesis and deposition phases, although defects are most likely to take place during the deposition phase [16]. Researchers have shown that QCA cells are more susceptible to missing and additional QCA cell defects [17]. In additional cell defect, an additional cell is deposited on the substrate. The missing cell defect occurs due to the missing of a particular cell. Researchers have been addressing the design and test of QCA circuits assuming the single missing/additional cell defect model.

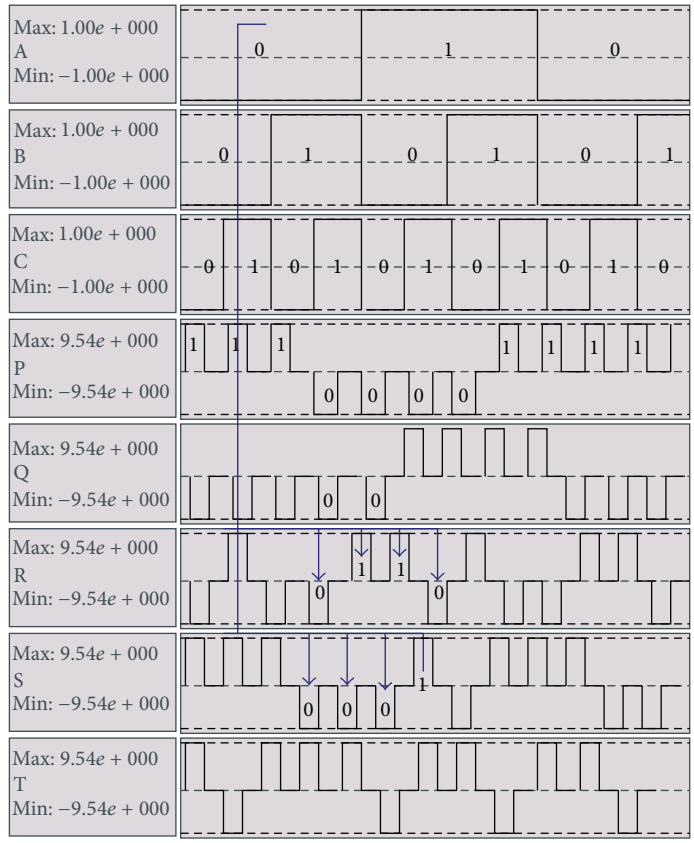


Figure 8: Simulation result of fault-tolerant QCA adder.

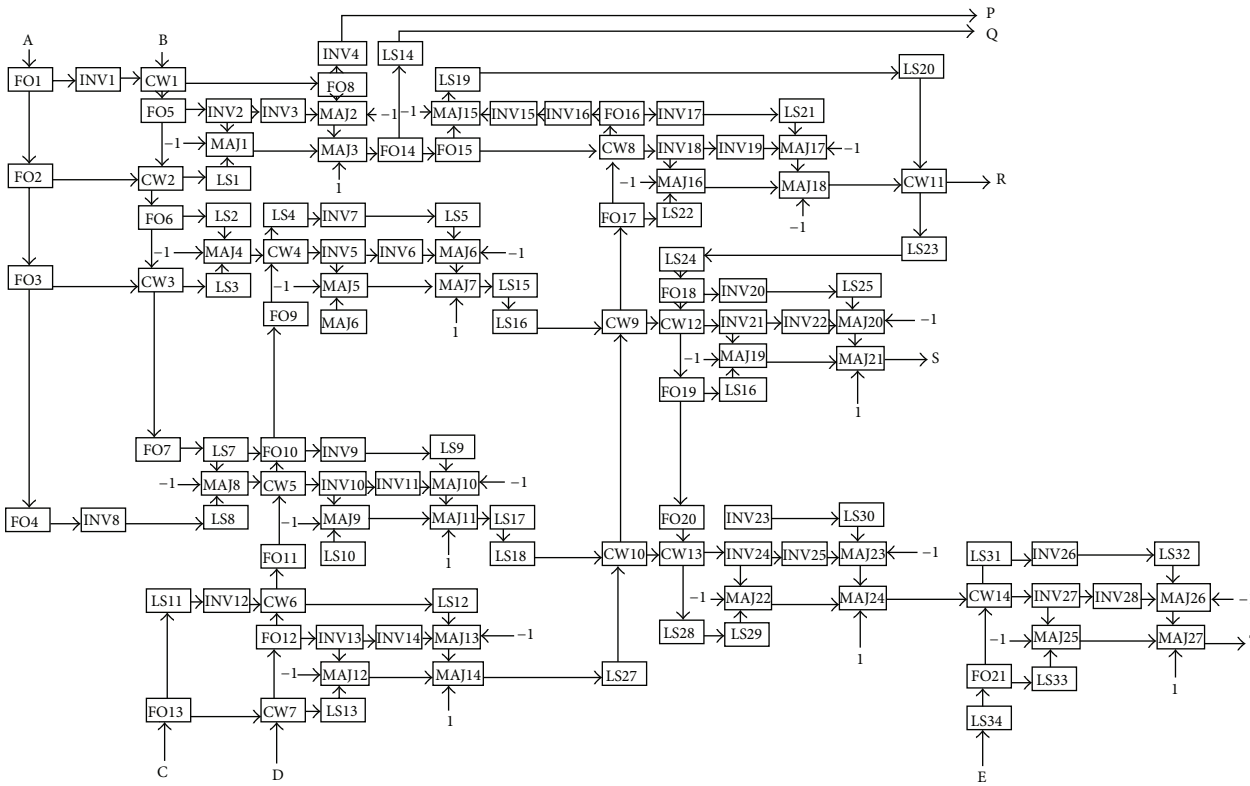


Figure 9: HDLQ modelling of QCA-based fault-tolerant adder.

Table 4: Fault pattern of proposed fault-tolerant adder.

Input	Output	Fault pattern											Success rate	FT%
		1	2	3	⋯	43	44	45	⋯	76	77	78		
a_0	a_0	a_{16}	a_{12}	a_0	⋯	a_2	a_1	a_0	⋯	a_{12}	a_1	a_0	32/78	41.02
a_1	a_1	a_{17}	a_{13}	a_1	⋯	a_3	a_0	a_1	⋯	a_1	a_0	a_0	34/78	43.59
a_2	a_7	a_{23}	a_8	a_7	⋯	a_5	a_6	a_7	⋯	a_7	a_6	a_7	38/78	48.72
a_3	a_6	a_{22}	a_8	a_7	⋯	a_4	a_7	a_6	⋯	a_6	a_6	a_6	38/78	48.72
a_4	a_4	a_{20}	a_{11}	a_4	⋯	a_6	a_5	a_4	⋯	a_5	a_4	a_4	37/78	47.43
a_5	a_5	a_{21}	a_{10}	a_5	⋯	a_7	a_4	a_5	⋯	a_5	a_5	a_5	39/78	50.00
a_6	a_3	a_{19}	a_{15}	a_3	⋯	a_1	a_2	a_3	⋯	a_3	a_2	a_3	40/78	51.28
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
a_{30}	a_{17}	a_{13}	a_{17}	a_{19}	⋯	a_{19}	a_{16}	a_{17}	⋯	a_{17}	a_{16}	a_{17}	41/78	52.56
a_{31}	a_{16}	a_{12}	a_{16}	a_{18}	⋯	a_{18}	a_{17}	a_{16}	⋯	a_{16}	a_{16}	a_{16}	42/78	53.78
Average FT = fault tolerance														47.38

In the proposed work, the QCA layout of the FTRA gate is converted into the corresponding hardware description language notations using the HDLQ Verilog library [18]. The HDLQ design tool, Verilog equivalent for QCA, consists of a Verilog HDL library of QCA devices, that is, MV, INV, FO, Crosswire (CW), and L-shape wire with fault injection capability. The HDLQ-modeled design of the FTRA gate is shown in Figure 9, and an exhaustive testing of the HDLQ model of the FTRA gate is conducted with 32 input patterns in the presence of all possible single missing/additional cell defects. The design is simulated using the Verilog HDL simulator in the presence of faults to determine the corresponding outputs.

Testing of the FTRA gate generated 78 unique fault patterns at the output, as shown in Table 4. Due to huge volume of data, the fault pattern table is partially shown. In the fault patterns study shown in the Table 4, a_i is the five-bit pattern with an equivalent decimal value of i. For example, a_0 represents 00000 (decimal 0), and a_{31} represents 11111 (decimal 31). In Table 4, first two columns present the correct behaviour of FTRA gate, that is, for a particular input vector corresponding expected output vector. Each row of the Table 4 represents the output generated after the fault injection of different 78 modules of the HDLQ model (Figure 9), for example, for given input a_0, after the fault injection of different modules, the generated fault pattern is $a_0, a_{16}, a_{12}, \ldots, a_1, a_0$. From those fault patterns, we observed that there are average 47.38% successful patterns that produce the correct output, even when there is a fault.

7. Conclusions

This work presents a novel architecture of fault-tolerant reversible adder (FTRA) gate. Experimental results establish the fact that the proposed FTRA achieved significant improvements in reversible circuits over the existing ones. A reversible arithmetic logic unit is synthesized based on the FTRA proposed. This is first attempt to synthesize a fault-tolerant full adder/subtractor using only single reversible logic block (FTRA) with optimal quantum cost to avoid wire-crossing bottleneck. Also, the application of this fault-tolerant logic in QCA nanotechnology gets an extra advantage in fault-tolerant computing with effective 47.38% fault-free output in the presence of all possible single missing/additional cell defects.

Though, the clocking structure beneath the QCA cell layer is also very important and nontrivial research issue.

Acknowledgment

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