Hindawi
Mathematical Problems in Engineering
Volume 2017, Article ID 4157165, 14 pages
https://doi.org/10.1155/2017/4157165

Research Article

Research on Control Strategy of AC-DC-AC Substation Based on Modular Multilevel Converter

Fei Chang, Zhongping Yang, and Fei Lin

School of Electrical Engineering, Beijing Jiaotong University, Beijing 100044, China

Correspondence should be addressed to Fei Chang; 14117397@bjtu.edu.cn

Received 22 February 2017; Revised 21 August 2017; Accepted 10 September 2017; Published 8 November 2017

Academic Editor: Yakov Strelniker

Significant disadvantages in power quality especially the unbalance problem and neutral sections restrict the evolution of conventional traction power supply system. A new traction power supply system based on three-phase to single-phase converter is studied, which can transfer active power from three-phase grid to single-phase catenary. One catenary section could be utilized in the new traction power supply system instead of the multiple split sections in conventional system. Three-phase to single-phase converter is the core equipment of new traction power system. MMC (modular multilevel converter) structure of AC-DC-AC substation is proposed in this paper. To solve the problem of the capacitor voltage balancing in MMC, a parallel sorting algorithm based on field programmable gate array (FPGA) is studied. And the correctness and effectiveness of the algorithm are verified by experiments. In addition, it is inevitable that the AC grid voltage will be unbalanced caused by the fault in the new system. Therefore, this paper focuses on the analysis of the effect of the unbalanced grid voltage on the operating characteristics of the MMC system. Finally, the correctness of the theoretical analysis is verified by simulation.

1. Introduction

A traditional traction power system typically uses two split catenaries, as shown in Figure 1(a), so there is neutral section in one substation (SS) and between adjacent SS [1]. When the locomotive is passing through neutral section, the traction and speed will be lost. Meanwhile the system must mitigate critical power quality problems, such as unbalance, harmonic, and reactive power [2]. Compensator-based technologies have been installed to improve the power quality in railway traction power system [3, 4]. The scheme of one catenary line based on a power flow controller (PFC) was used, as shown in Figure 1(b); this scheme was called a cophase traction power supply system [5]. A PFC can balance active power and compensate reactive power and filter harmonic. Although the neutral section at the exit of the substation was canceled in cophase system, that between adjacent SS still exists. To connect all catenaries from different substations, a new traction power supply system is proposed in [6] that is based on a three-phase to single-phase converter as the critical piece of equipment in the substation, as shown in Figure 1(c). The system transfers active power from the isolated three-phase grid to a one-phase traction line and provides the output voltage with a controlled frequency, phase, and amplitude. Based on the control strategy of single-phase converter proposed in this paper, the amplitude and phase of the output voltage of each traction substation can be ensured the same. Therefore, the feeder line between different substations can be connected directly.

Japan Tokaido Shinkansen railway uses 60 Hz single-phase AC; since 2003, there have been 3 sets of 60 MVA EFC (Electronic Frequency Converter) installation and operation. EFC transforms three-phase 50 Hz AC into 60 Hz single-phase AC, and it has the ability to realize the same phase power supply. Figure 2 is the EFC topology, which uses a H-bridge cascaded multiple AC-DC-AC topology.

At present, the European cophase power supply equipment manufacturers are mainly ABB and Siemens company. The main circuit structure of ABB company adopts diode clamped cascaded AC-DC-AC topology, as shown in Figure 3; the main circuit structure of Siemens company adopts modular multilevel direct AC-AC conversion (MMDC) topology, as shown in Figure 4.

MMC technology can be regarded as an important milestone in the history of the development of flexible HVDC

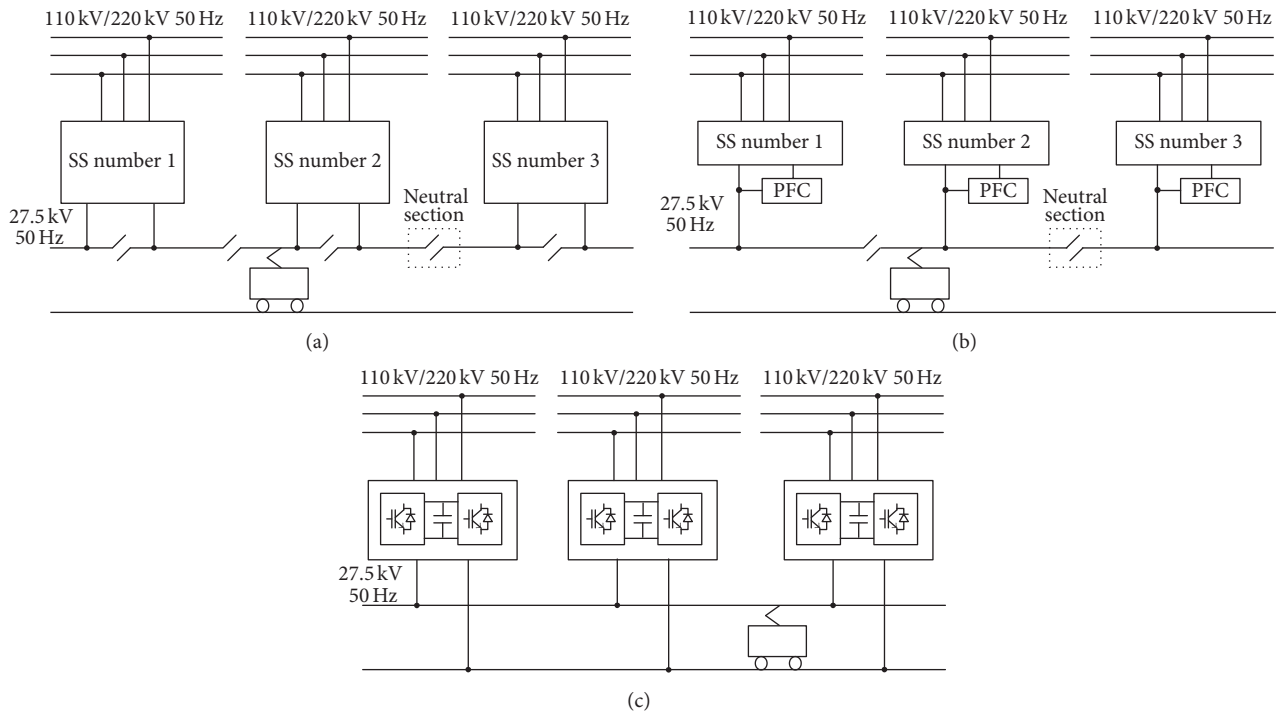

Figure 1: Three types of traction power supply systems: (a) traditional system; (b) cophase system; and (c) new traction power supply system.

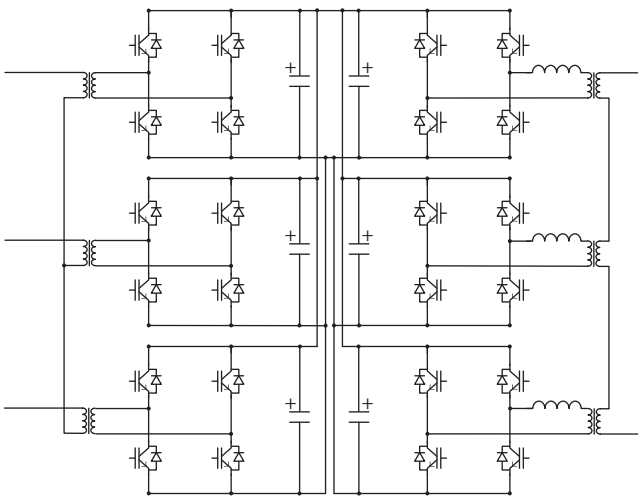

Figure 2: H-bridge cascaded multiple AC-DC-AC topology.

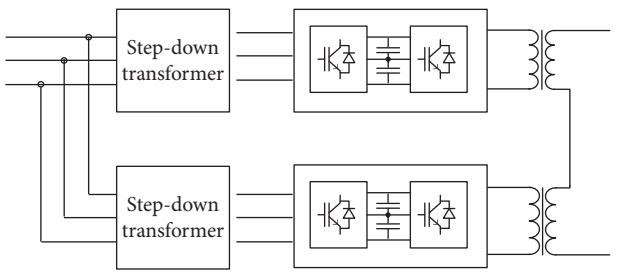

Figure 3: Diode clamped cascaded AC-DC-AC topology.

transmission. Compared with the conventional two-level or three-level converter, modular cascade structure of MMC is easy to achieve high voltage level, to avoid the defects of static and dynamic voltage balancing, large switching loss, and high harmonic content of the device. Figure 5 is the MMC structure of AC-DC-AC substation.

Finally, Table 1 compares the four circuit topologies of cophase power supply device.

In this paper, the capacitor voltage balancing problem of MMC was studied firstly and a parallel sorting algorithm based on field programmable gate array (FPGA) was studied.

In addition, it is inevitable that the AC grid voltage will be unbalanced caused by the fault, for example, the single-phase grounding fault. It is important to analyze the effect of asymmetric grid voltage on the operation characteristics of the system. In [6, 7], the classical dq decoupling control is used in the rectifier side. However, this control is only applicable to the balanced grid voltage. In this paper, the influence of negative-sequence current is analyzed in detail, and the unified control of positive and negative-sequence current is realized by using PR controller.

2. Capacitor Voltage Balancing Control

An important challenge in MMC is balancing the flying-capacitor voltage. There are two primary approaches for balancing the capacitor voltage. One method uses proportional integral (PI) controller [8, 9], which is suitable for less submodules because each capacitor voltage requires a PI controller. The other method is the capacitor voltage sorting algorithm which is suitable for more submodules [10, 11].

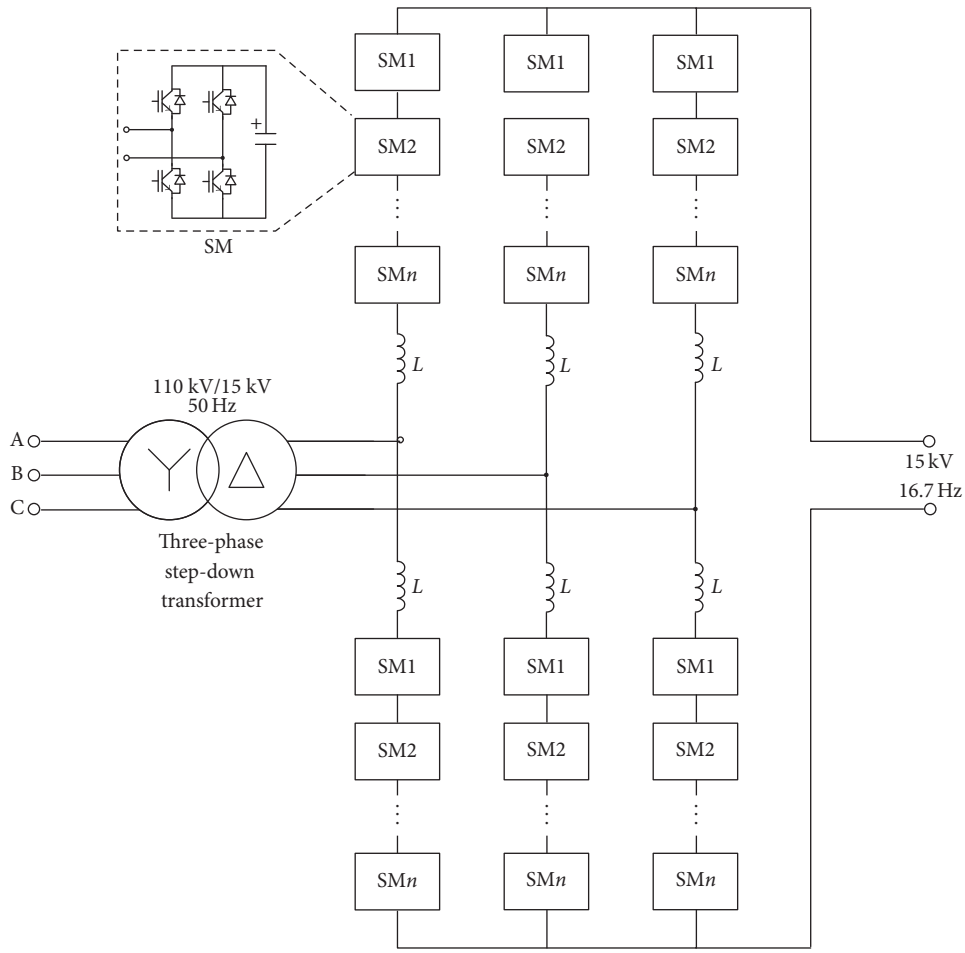

Figure 4: MMDC circuit topology.

Traditional sorting methods (e.g., the bubble sorting method) rely on serial processing, so they are suitable for implementation in DSP, and they need large computation time and have no real-time performance. Based on FPGA hardware technology, a parallel real-time sorting algorithm is studied in this paper [12]. The algorithm uses the FPGA hardware features with parallel computing and can be computed in four clock cycles, and the computation time does not vary with changes in the number of submodules.

2.1. Principle of the Parallel Sorting Algorithm Based on FPGA. The algorithm applied to the following examples illustrates the following specific implementation steps while assuming that the bridge arm capacitor voltage array An is equal to {500, 510, 552, 542, 531, 573, 584, 521, 563, 500 V} for ($n = 0, \ldots, 9$).

(1) First Clock Cycle: Pairwise Comparisons for All Capacitor Voltage Values. Specified herein, Am and An are compared: if $Am > An$, then the comparison result is $Z = 1$; otherwise $Z = 0$. Thus, the original data in the first output is 1 or 0, respectively. The comparison results between the voltage values are shown in Table 2.

(2) Second Clock Cycle. The comparison value of the capacitor voltage is recorded to determine the sorting position of the capacitor voltage in the array. As shown in Table 2, the order of each capacitor voltage from small to large is {$A0$, $A9$, $A1$, $A7$, $A4$, $A3$, $A2$, $A8$, $A5$, $A6$}.

(3) Third Clock Cycle. The capacitor voltage value is assigned to the corresponding sorting space.

(4) Fourth Clock Cycle. The sorting results of the capacitor voltage are output.

Figure 6 is the simulation result of the sorting design in QUARTUS. In Figure 6, in0~in9 are the 10 capacitor voltage values; after four clock cycles, the output sorting results are out0~out9, respectively.

2.2. Performance Analysis of the Parallel Sorting Algorithm

2.2.1. Time Complexity. Processing of the parallel sorting algorithm only requires four clock cycles in the FPGA, and the time complexity is constant. If the clock cycle of the FPGA is 10 ns, the time required to complete the sorting algorithm is 40 ns. However, using traditional sorting algorithms, such

Table 1: Comparison of the circuit topology of advanced cophase power supply device.

Topology type	Diode clamped cascaded AC-DC-AC topology (ABB)	MMDC circuit topology (Siemens)	H-bridge cascaded multiple AC-DC-AC topology (Japan Toshiba)	MMC AC-DC-AC topology (studied in this paper)
Input/output decoupling performance	Excellent	Good	Excellent	Excellent
Input/output transformer	Special single-phase input/output transformer, complex structure and large quantity	Normal three-phase input transformer, no need single-phase output transformer	Special single-phase input/output transformer, complex structure and large quantity	Normal three-phase input transformer, no need single-phase output transformer
Input/output filter	Need	No need	Need	No need
Converter efficiency (excluding transformers)	About 95%	≥99%	About 96%	≥98%
Area covered	Larger	Larger	Large	Larger
Manufacturing cost	Higher	Higher	High	Higher

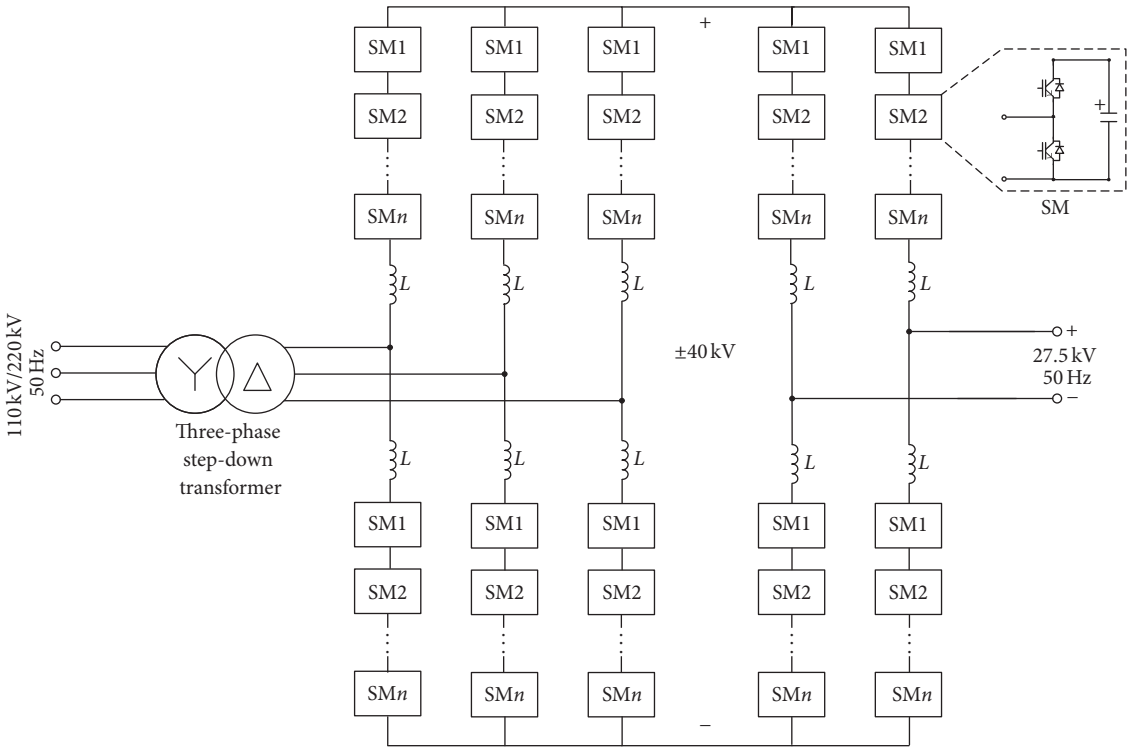

Figure 5: MMC structure of AC-DC-AC substation.

as bubble sorting, the time complexity is $n(n-1)/2$. If there are 100 capacitor voltages, the computation time required to complete the bubble sorting algorithm is equal to 49.5 μs. Obviously, this computation time is far greater than that of the parallel sorting algorithm.

2.2.2. Space Complexity. Due to the need of full parallel processing, the parallel sorting algorithm takes up a large amount of processing space. Based on the calculated statistics, if the number of the capacitor voltages is equal to n, then the number of comparators required is equal to $(n-1)^2$. Because the number of logic elements (LE) in the FPGA occupied by each comparator is approximately 5, the total number of LE is $5(n-1)^2$. If each bridge arm has 100 submodules, nearly 50,000 LE are needed. Therefore, a high performance FPGA is needed in the practical application, which will increase the cost of the hardware.

Table 2: Comparison of capacitor voltage.

	$A_0(500)$	$A_1(510)$	$A_2(552)$	$A_3(542)$	$A_4(531)$	$A_5(573)$	$A_6(584)$	$A_7(521)$	$A_8(563)$	$A_9(500)$	Accumulated value
$A_0(500)$		0	0	0	0	0	0	0	0	0	0
$A_1(510)$	1		0	0	0	0	0	0	0	1	2
$A_2(552)$	1	1		1	1	0	0	1	0	1	6
$A_3(542)$	1	1	0		1	0	0	1	0	1	5
$A_4(531)$	1	1	0	0		0	0	1	0	1	4
$A_5(573)$	1	1	1	1	1		0	1	1	1	8
$A_6(584)$	1	1	1	1	1	1		1	1	1	9
$A_7(521)$	1	1	0	0	0	0	0		0	1	3
$A_8(563)$	1	1	1	1	1	0	0	1		1	7
$A_9(500)$	1	0	0	0	0	0	0	0	0		1

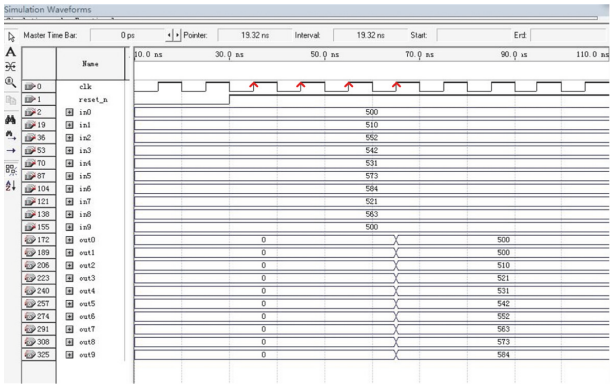

Figure 6: Simulation result of the sorting design.

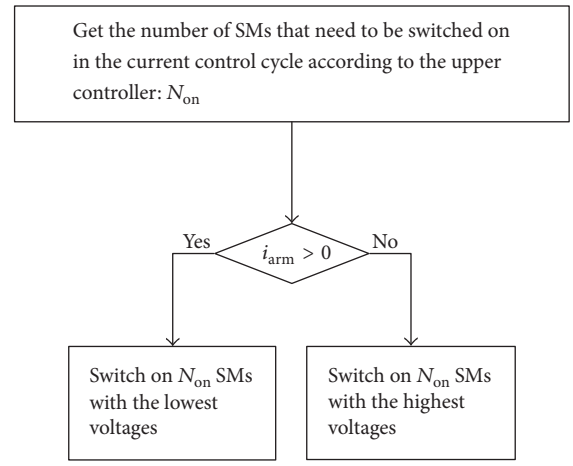

Figure 7: Flow chart of capacitor voltage balancing control.

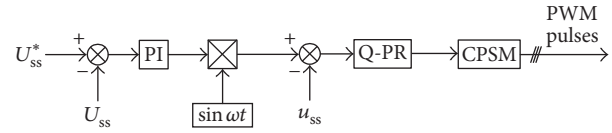

Figure 8: Control strategy of single-phase converter.

2.3. Flow Chart of Capacitor Voltage Balancing Control. The specific implementation process of the MMC capacitor voltage balancing control is shown in Figure 7.

N_{on} is the number of SMs that need to be switched on in the current control cycle according to the upper controller, and i_{arm} is the corresponding arm current.

The switching principles of capacitor voltage balancing algorithm are thus summarized as follows. When the arm current charges the capacitors, it switches on the SMs with the lowest capacitor voltages while switching off those with the highest voltages. When the arm current discharges the capacitors, the SMs with the highest capacitor voltages are switched on while those with the lowest voltages are switched off.

3. Control of Single-Phase Converter

This paper presents a control strategy of single-phase converter, as shown in Figure 8. The outer loop controls the RMS of the voltage, while the inner loop controls the instantaneous value of the voltage.

In the outer loop, the RMS of the single-phase voltage U_{ss} is compared with the reference value U_{ss}^*; the error signal is through a PI regulator and multiplied by a standard sinusoidal signal; the result value is then used as a reference value for the inner loop. A single-phase traction converter is controlled by the outer loop, and the RMS of the voltage can theoretically be identical to the steady-state response to ensure that when the load changes or when the system is disturbed, the RMS of the voltage remains constant.

The phase synchronization of sinusoidal signals can be realized by GPS between substations. Thus, the amplitude and phase of the output voltage of each traction substation can be ensured the same. There is no circulating current between substations, and there is no master-slave relationship between substations, and any substation fault can be supplied by two adjacent substations, and the system reliability is high.

In the inner loop, the instantaneous value of the single-phase voltage u_{ss} is compared with the reference value obtained by the outer loop, and the error value passes through the Q-PR regulator to get a reference wave and that compared with the triangular wave to form the trigger pulse. In the inner loop, a Q-PR regulator instead of a PI regulator can achieve no error control of the AC voltage. The instantaneous value

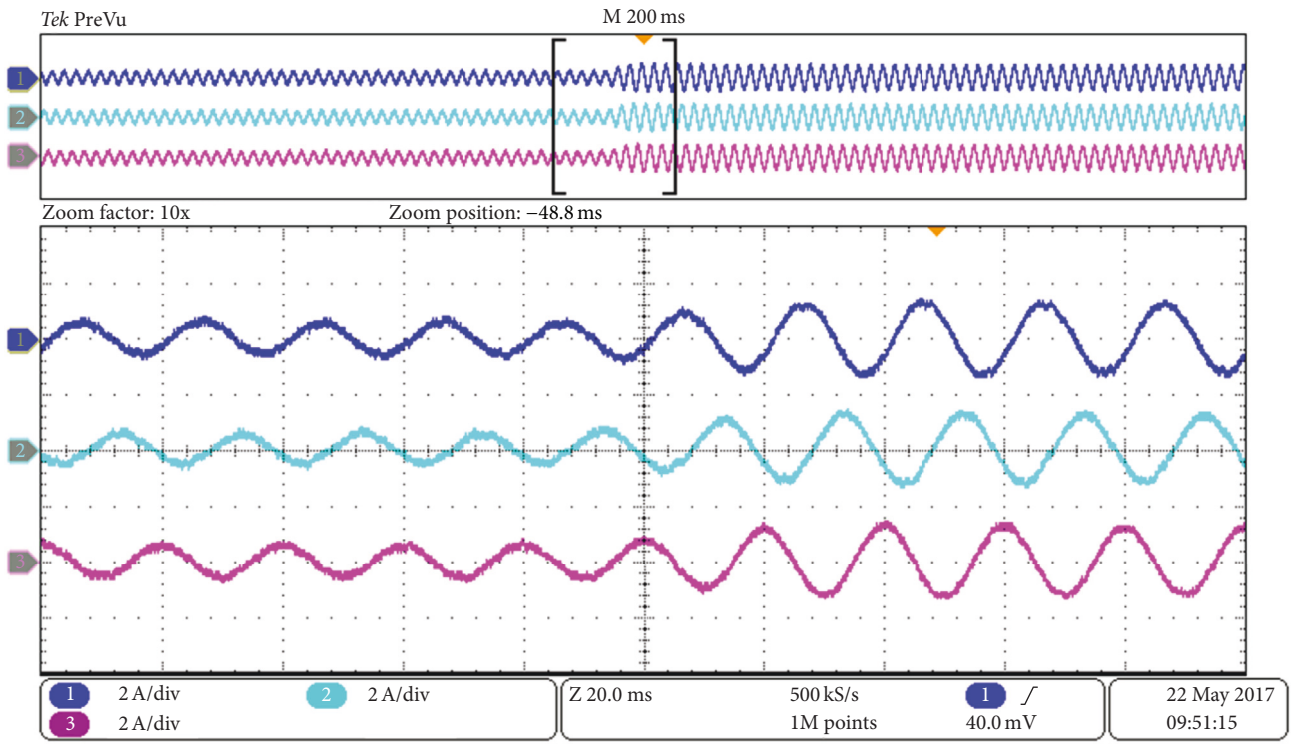

Figure 9: Grid side current.

Table 3: Experimental parameters.

Parameters	Values
Rated DC voltage	120 V
Number of SMs of each arm	4
Arm inductance	5 mH
Capacitance of each SM	2000 μF
Carrier frequency	1 kHz

of the output voltage is controlled by the inner loop so that the voltage can track a given sine wave to maintain a good sinusoidal output waveform.

4. Experimental Verification

Experimental verification is carried out on the hardware in the loop physical experiment platform based on DSP + FPGA and RT-LAB. The experimental structure of the system is shown in Figure 5, and the experimental parameters are shown in Table 3.

Figure 9 is the three-phase grid current. As can be seen, when the load power is increased, the three-phase current of the power grid is fast response, and the three-phase current is symmetrical in the whole process, and the harmonic content is low. Figure 10 is the voltage and current of traction side. During the whole experiment, the single-phase traction voltage is stable in the 40 V, the single-phase traction current can be quick response when the load changes. In the whole process, the total harmonic distortion of single-phase traction voltage and current is low, and the power factor is close to 1, which can provide high quality power supply for electric locomotive. Figure 11 is MMC capacitor voltage of grid side. Because of the limitation of the number of channels of the oscilloscope, the capacitor voltage waveform of the first submodule of the upper and lower bridge arm of phase A is given. Meanwhile, in order to observe the ripple component of capacitor voltage, the oscilloscope waveform is not DC coupled, so it only shows the AC component of the capacitor voltage. It can be seen that the submodule capacitor voltage of the upper and lower bridge arm is complementary and stable in the whole power step. Also the fluctuation range of the capacitor voltage is not more than 5%. In addition, the sorting time is 40 ns that verified the effectiveness of the capacitor voltage balancing algorithm in this paper.

5. Characteristic Analysis and Control Strategy for MMC in Rectifier Side under Unbalanced Grid Voltage

5.1. Circular Interaction among the Voltage and Current Quantities of the MMC. The structure of the main circuit and the structure of a single submodule (SM) of the MMC converter are shown in Figure 12. Three-phase MMC converter is composed of six bridge arms, with each bridge arm consisting of N cascaded SM.

As shown in Figure 13, a SM is used as an example. In this figure, i is used to denote the ith SM in this arm. Assuming that the arm current and the switching function of this SM are known, the interaction of the voltage and current quantities can be described as follows [13].

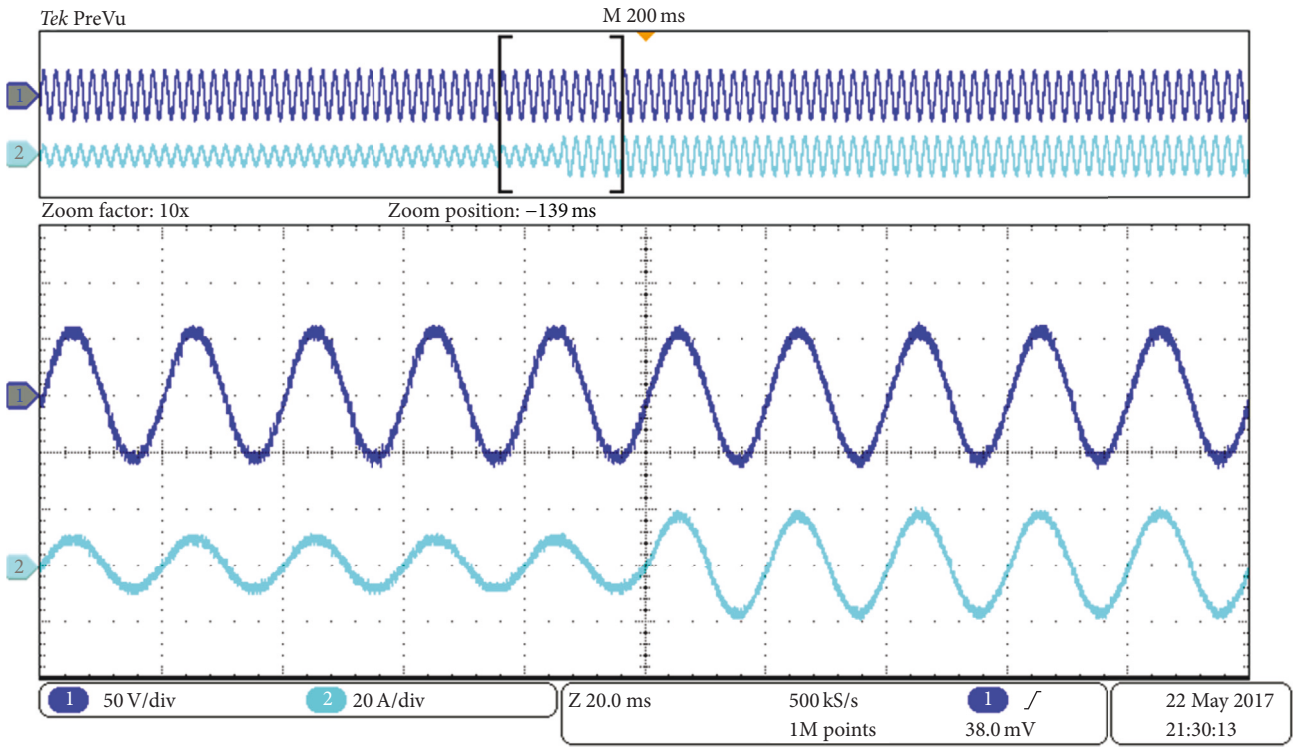

Figure 10: Voltage and current of traction side.

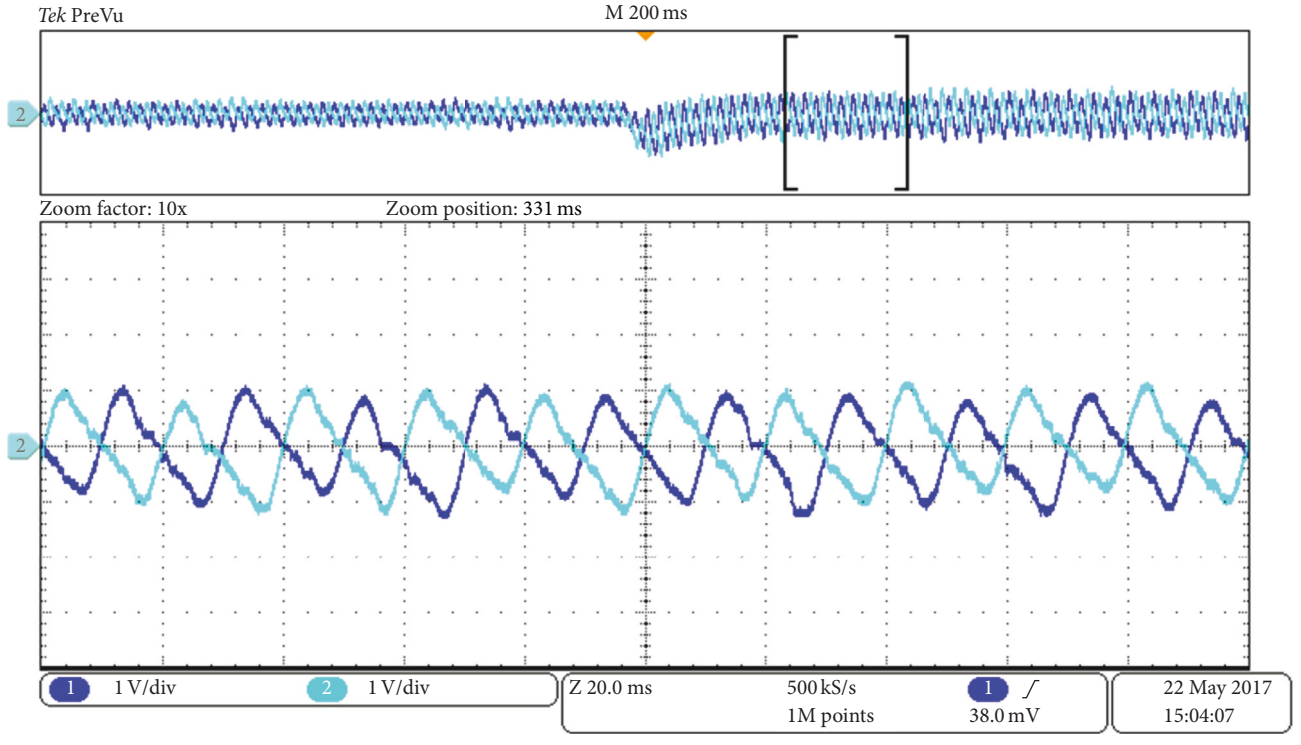

Figure 11: MMC capacitor voltage of grid side.

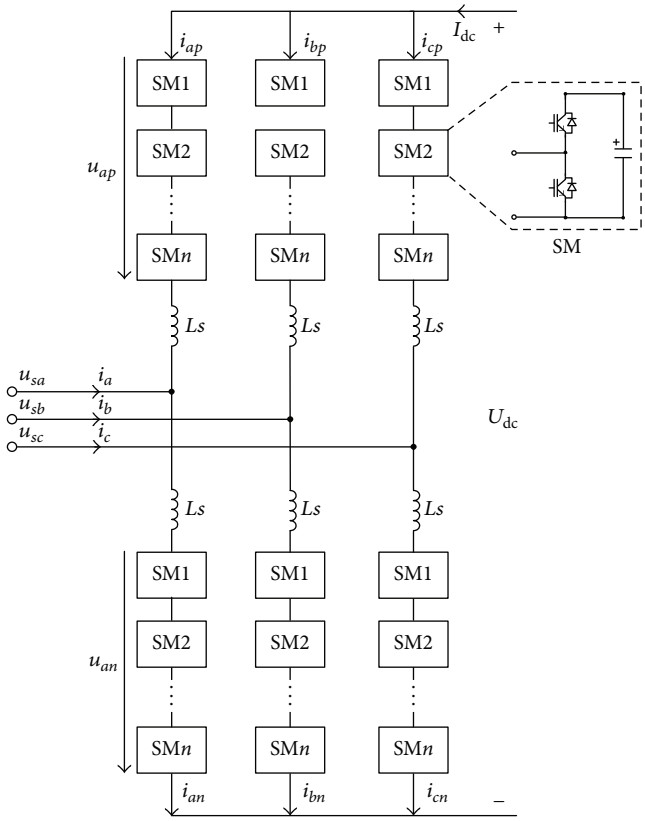

Figure 12: Circuit diagram of MMC.

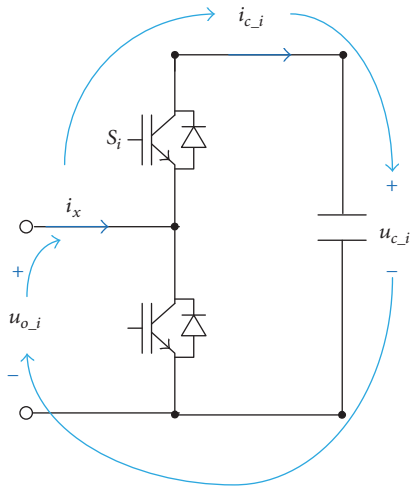

Figure 13: Interaction among the voltage and current quantities of a SM.

(1) Capacitor Current. The bridge arm current will be coupled to the DC side of the converter through the switching action and will flow into the DC capacitor. For the ith SM of this arm, the relationship between the capacitor current and the switching function is as follows:

$$i_{c\_i} = S_i i_x, \tag{1}$$

where $S_i(t)$ denotes the switching function of this SM. $S_i(t) = 1$, when S_1 is on and S_2 is off; $S_i(t) = 0$, when S_1 is off and S_2 is on.

(2) Capacitor Ripple Voltage. The current shown in (1) causes a voltage ripple in the capacitor. The nth harmonic component in the capacitor current causes a corresponding voltage ripple with nth harmonic frequency and its time-varying function is expressed as follows:

$$u_{c\_i}(\omega_n) = \frac{i_{c\_i}(\omega_n)}{j\omega_n C_d}, \tag{2}$$

where C_d is the capacitance of the SM capacitor and ω_n is the nth harmonic frequency.

(3) Ripple Voltage of the SM Terminal. The DC side ripple voltage of the SM is coupled to the AC port of the SM through the switching action. The corresponding ripple voltage in the AC port is as follows:

$$u_{o\_i} = S_i u_{c\_i}. \tag{3}$$

(4) Ripple Voltage of the Phase. Each bridge arm is composed of N cascaded SM, and each phase consists of an upper and a lower bridge arm, so the total ripple voltage of the phase arm is as follows:

$$\Delta u_{\text{ph}} = \sum_{i=1}^{N} \Delta u_{p\_o\_i} + \sum_{i=1}^{N} \Delta u_{n\_o\_i}, \tag{4}$$

where Δu_{ph} denotes the ripple voltage across the phase and $\Delta u_{p\_o\_i}$ and $\Delta u_{n\_o\_i}$, respectively, denote the AC side ripple voltage of the ith SM in the upper and lower bridge arms.

5.2. Characteristic Analysis for MMC in Rectifier Side under Unbalanced Grid Voltage. When the asymmetrical short-circuit fault occurs in AC grid, as the connection of transformer is usually Y/Δ or Δ/Y which can isolate zero-sequence component, so the effect of negative-sequence current is studied here. Negative-sequence network is shown in Figure 14, the points P and N are similar to the neutral point of the three-phase negative-sequence network, and the electric potential in the AC circuit can be considered to be the same. So it can be considered that the negative-sequence current will not flow into the DC side, only exists in the AC side and the converter, and is the symmetrical distribution in the upper and lower bridge arm of the converter. The simplified equivalent circuit is shown in Figure 15:

$$\dot{I}^{-} = \frac{\dot{U}^{-}}{Z_{T\sigma} + Z_L/2} = -2\dot{I}_p^{-} = 2\dot{I}_n^{-}, \tag{5}$$

where $\dot{I}^{-}$ is the negative-sequence current, $\dot{I}_p^{-}$ and $\dot{I}_n^{-}$ are, respectively, the negative-sequence current in the upper and lower bridge arm, $\dot{U}^{-}$ is the negative-sequence voltage, $Z_{T\sigma}$ is the impedance of the transformer and $Z_{T\sigma} = \omega L_{T\sigma}$, Z_L is the impedance of the bridge arm, and $Z_L = \omega L_s$.

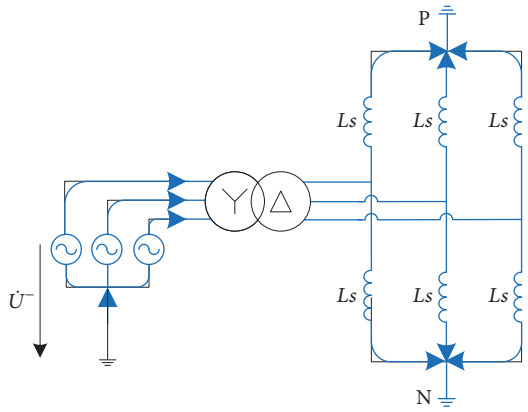

Figure 14: Negative-sequence path.

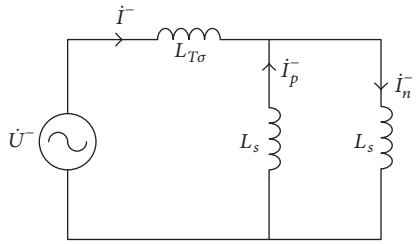

Figure 15: Negative-sequence equivalent circuit.

The three-phase instantaneous value of negative-sequence current in AC system can be expressed as follows:

$$\begin{aligned} i_a^-(t) &= I_m^- \sin\left(\omega t - \varphi^-\right), \\ i_b^-(t) &= I_m^- \sin\left(\omega t - \varphi^- + \frac{2}{3}\pi\right), \\ i_c^-(t) &= I_m^- \sin\left(\omega t - \varphi^- - \frac{2}{3}\pi\right), \end{aligned} \tag{6}$$

where $i_a^-(t)$, $i_b^-(t)$, and $i_c^-(t)$, respectively, denote three-phase negative-sequence current and I_m^- and φ^- denote amplitude and phase of negative-sequence current, respectively.

The average switching function of the converter can be expressed as follows:

$$\begin{aligned} S_{ap}(t) &= \frac{1}{2} - \frac{m}{2}\sin(\omega t), \\ S_{an}(t) &= \frac{1}{2} + \frac{m}{2}\sin(\omega t), \end{aligned} \tag{7}$$

where $S_{ap}(t)$ and $S_{an}(t)$ are, respectively, the average switching functions of the SM in the upper and lower arms in phase A and m is the modulation index.

(1) Capacitor ripple current caused by negative-sequence current is as follows.

Capacitor current of the upper bridge arm in phase A can be expressed as follows:

$$\begin{aligned} \Delta i_{cap}^-(t) &= S_{ap}(t) \cdot \left[-\frac{1}{2} i_a^-(t)\right] \\ &= \left[\frac{1}{2} - \frac{m}{2}\sin(\omega t)\right]\left[-\frac{I_m^-}{2}\sin\left(\omega t - \varphi^-\right)\right] \\ &= -\frac{I_m^-}{4}\sin\left(\omega t - \varphi^-\right) - \frac{mI_m^-}{8}\cos\left(2\omega t - \varphi^-\right) \\ &\quad + \frac{mI_m^-}{8}\cos\varphi^-. \end{aligned} \tag{8}$$

Similarly, capacitor current of the lower bridge arm in phase A is

$$\begin{aligned} \Delta i_{can}^-(t) &= S_{an}(t) \cdot \left[\frac{1}{2} i_a^-(t)\right] \\ &= \left[\frac{1}{2} + \frac{m}{2}\sin(\omega t)\right]\left[\frac{I_m^-}{2}\sin\left(\omega t - \varphi^-\right)\right] \\ &= \frac{I_m^-}{4}\sin\left(\omega t - \varphi^-\right) - \frac{mI_m^-}{8}\cos\left(2\omega t - \varphi^-\right) \\ &\quad + \frac{mI_m^-}{8}\cos\varphi^-. \end{aligned} \tag{9}$$

The capacitor current for phases B and C can be obtained in a similar manner:

$$\begin{aligned} \Delta i_{cbp}^-(t) &= -\frac{I_m^-}{4}\sin\left(\omega t - \varphi^- + \frac{2}{3}\pi\right) \\ &\quad - \frac{mI_m^-}{8}\cos\left(2\omega t - \varphi^-\right) \\ &\quad + \frac{mI_m^-}{8}\cos\left(\varphi^- + \frac{2}{3}\pi\right), \\ \Delta i_{cbn}^-(t) &= \frac{I_m^-}{4}\sin\left(\omega t - \varphi^- + \frac{2}{3}\pi\right) \\ &\quad - \frac{mI_m^-}{8}\cos\left(2\omega t - \varphi^-\right) \\ &\quad + \frac{mI_m^-}{8}\cos\left(\varphi^- + \frac{2}{3}\pi\right), \\ \Delta i_{ccp}^-(t) &= -\frac{I_m^-}{4}\sin\left(\omega t - \varphi^- - \frac{2}{3}\pi\right) \\ &\quad - \frac{mI_m^-}{8}\cos\left(2\omega t - \varphi^-\right) \\ &\quad + \frac{mI_m^-}{8}\cos\left(\varphi^- - \frac{2}{3}\pi\right), \end{aligned}$$

$$\Delta i_{ccn}^{-}(t) = \frac{I_m^-}{4}\sin\left(\omega t - \varphi^- - \frac{2}{3}\pi\right) - \frac{mI_m^-}{8}\cos\left(2\omega t - \varphi^-\right) + \frac{mI_m^-}{8}\cos\left(\varphi^- - \frac{2}{3}\pi\right). \tag{10}$$

From formulas (8)–(10) it can be seen that the amplitude of fundamental-frequency component of capacitor current caused by negative-sequence current is $I_m^-/4$, the amplitude of the second-order harmonic component is $mI_m^-/8$, and the DC component is $(mI_m^-/8)\cos\varphi^-$.

(2) Under normal operating conditions, the DC component of the three-phase capacitor current is

$$\begin{aligned} i_{cap\_dc} &= i_{can\_dc} = \frac{I_{da}}{2} - \frac{mI_m^+}{8}\cos\varphi^+, \\ i_{cbp\_dc} &= i_{cbn\_dc} = \frac{I_{db}}{2} - \frac{mI_m^+}{8}\cos\varphi^+, \\ i_{ccp\_dc} &= i_{ccn\_dc} = \frac{I_{dc}}{2} - \frac{mI_m^+}{8}\cos\varphi^+. \end{aligned} \tag{11}$$

The DC component is zero during the steady-state, which reflects the balance between the *ac*-side active power and the *dc*-link side active power. Therefore,

$$I_{da} = I_{db} = I_{dc} = \frac{mI_m^+}{4}\cos\varphi^+ = \frac{I_d}{3}, \tag{12}$$

where I_{da}, I_{db}, and I_{dc}, respectively, denote the three-phase DC current; I_d denotes the DC current; I_m^+ and φ^+ denote amplitude and phase of positive-sequence current, respectively.

Under unbalanced grid voltage, the DC component of the capacitor current is

$$\begin{aligned} i'_{cap\_dc} &= i'_{can\_dc} = \frac{I'_{da}}{2} - \frac{mI_m^+}{8}\cos\varphi^+ + \frac{mI_m^-}{8}\cos\varphi^-, \\ i'_{cbp\_dc} &= i'_{cbn\_dc} = \frac{I'_{db}}{2} - \frac{mI_m^+}{8}\cos\varphi^+ + \frac{mI_m^-}{8}\cos\left(\varphi^- + \frac{2}{3}\pi\right), \\ i'_{ccp\_dc} &= i'_{ccn\_dc} = \frac{I'_{dc}}{2} - \frac{mI_m^+}{8}\cos\varphi^+ + \frac{mI_m^-}{8}\cos\left(\varphi^- - \frac{2}{3}\pi\right). \end{aligned} \tag{13}$$

Similarly, the DC component of the capacitor current should be zero, so the three-phase DC current is

$$\begin{aligned} I'_{da} &= \frac{m}{4}\left(I_m^+\cos\varphi^+ - I_m^-\cos\varphi^-\right), \\ I'_{db} &= \frac{m}{4}\left[I_m^+\cos\varphi^+ - I_m^-\cos\left(\varphi^- + \frac{2}{3}\pi\right)\right], \\ I'_{dc} &= \frac{m}{4}\left[I_m^+\cos\varphi^+ - I_m^-\cos\left(\varphi^- - \frac{2}{3}\pi\right)\right]. \end{aligned} \tag{14}$$

From formula (14) it can be seen that the distribution of DC current in the three-phase bridge arm is no longer symmetrical under unbalanced grid voltage, and the DC current is determined by the amplitude and phase of the negative-sequence current, but still keeping the following relationship: $I'_{da} + I'_{db} + I'_{dc} = I_d$. So the DC current caused by the negative-sequence current has the nature of the DC circulating current, which is to regulate the three-phase energy balance.

(3) Capacitor ripple voltage caused by negative-sequence current is as follows.

The fundamental-frequency component of the capacitor ripple voltages in the upper and lower arms can be obtained as

$$\begin{aligned} \Delta u_{cap1}^{-}(t) &= -\frac{1}{j\omega c_d}\cdot\frac{I_m^-}{4}\sin\left(\omega t - \varphi^-\right) \\ &= \frac{I_m^-}{4\omega c_d}\cos\left(\omega t - \varphi^-\right), \\ \Delta u_{can1}^{-}(t) &= -\frac{I_m^-}{4\omega c_d}\cos\left(\omega t - \varphi^-\right). \end{aligned} \tag{15}$$

The second-order harmonic component of the capacitor ripple voltages in the upper and lower arms can be obtained as

$$\begin{aligned} \Delta u_{cap2}^{-}(t) &= \Delta u_{can2}^{-}(t) \\ &= -\frac{1}{j2\omega c_d}\cdot\frac{mI_m^-}{8}\cos\left(2\omega t - \varphi^-\right) \\ &= -\frac{mI_m^-}{16\omega c_d}\sin\left(2\omega t - \varphi^-\right). \end{aligned} \tag{16}$$

The ripple voltages on the *ac* side of the SM in the upper and lower arms can be expressed as

$$\begin{aligned} &\Delta u_{sm\_ap}(t) \\ &\quad = \left[\frac{1}{2} - \frac{1}{2}m\sin(\omega t)\right]\left[\Delta u_{cap1}^{-}(t) + \Delta u_{cap2}^{-}(t)\right], \\ &\Delta u_{sm\_an}(t) \\ &\quad = \left[\frac{1}{2} + \frac{1}{2}m\sin(\omega t)\right]\left[\Delta u_{can1}^{-}(t) + \Delta u_{can2}^{-}(t)\right]. \end{aligned} \tag{17}$$

The sum of the ripple voltage of all SMs in one phase forms a ripple voltage across this phase. According to (17), the ripple voltage across this phase is expressed as

$$\begin{aligned} \Delta u_a^-(t) &= N\Delta u_{sm\_ap}(t) + N\Delta u_{sm\_an}(t) \\ &= -\frac{3NmI_m^-}{16\omega c_d}\sin\left(2\omega t - \varphi^-\right) - \frac{NmI_m^-}{8\omega c_d}\sin\varphi^-. \end{aligned} \tag{18}$$

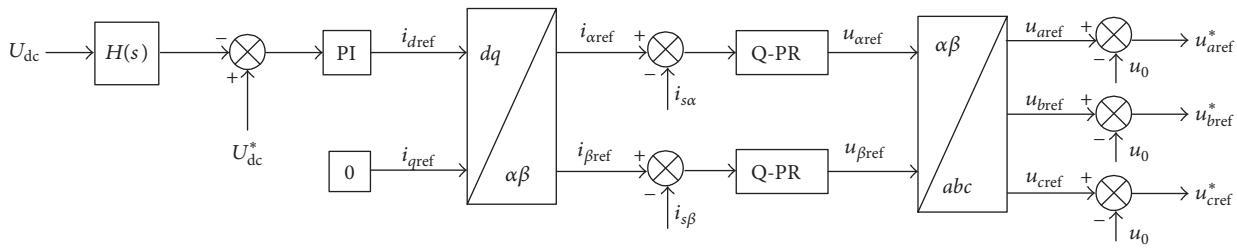

Figure 16: Control strategy of MMC under unbalanced grid voltage.

The ripple voltage for phases B and C can be obtained in a similar manner:

$$\begin{aligned}\Delta u_b^-(t) &= -\frac{3NmI_m^-}{16\omega c_d}\sin\left(2\omega t-\varphi^-\right)\\ &\quad -\frac{NmI_m^-}{8\omega c_d}\sin\left(\varphi^- +\frac{2}{3}\pi\right),\\ \Delta u_c^-(t) &= -\frac{3NmI_m^-}{16\omega c_d}\sin\left(2\omega t-\varphi^-\right)\\ &\quad -\frac{NmI_m^-}{8\omega c_d}\sin\left(\varphi^- -\frac{2}{3}\pi\right).\end{aligned} \tag{19}$$

From formulas (18)-(19) it can be seen that the second-order harmonic component of the capacitor ripple voltages in one phase is

$$\begin{aligned}\Delta u_{a2}^-(t) &= \Delta u_{b2}^-(t) = \Delta u_{c2}^-(t)\\ &= -\frac{3NmI_m^-}{16\omega c_d}\sin\left(2\omega t-\varphi^-\right).\end{aligned} \tag{20}$$

In summary, the effects of negative-sequence current include the following: the DC component of the three-phase circulating current is not symmetrical; the amplitude of the capacitor ripple voltage of the SM is increased; there is the second-order harmonic component in the DC voltage.

5.3. Control Strategy for MMC in Rectifier Side under Unbalanced Grid Voltage. The control strategy of three-phase converter based on the $\alpha\beta$ coordinate system is shown in Figure 16 [14]. A stable DC-link voltage is required in order for the converter to work properly. This can be achieved by introducing a PI controller to maintain the DC-bus voltage U_{dc} at the DC-bus reference voltage U_{dc}^*. Because of the double-frequency ripple component in the DC-bus voltage, in a low-pass filter, such as the hold filter

$$H(s) = \frac{1-e^{-Ts/2}}{Ts/2}, \tag{21}$$

where T is the fundamental period of the system, $H(s)$ can be adopted to measure the DC component of U_{dc} for feedback.

Firstly, according to the DC voltage outer loop, the reference value i_{dref} of the d-axis current is obtained. Since the three-phase converter is mainly used for active power transmission from the three-phase grid, the reference value i_{qref} of the q-axis current is set to 0. Secondly, the reference values $i_{\alpha ref}$ and $i_{\beta ref}$ of the current inner loop are obtained by a $dq/\alpha\beta$ coordinate transformation, and then, by comparison with the actual current values $i_{s\alpha}$ and $i_{s\beta}$ in the $\alpha\beta$ coordinate system, the errors between references and actual currents are used to generate the voltage references $u_{\alpha ref}$ and $u_{\beta ref}$ through the quasi-proportional resonant (Q-PR) regulator. The transfer function of Q-PR is as follows [14, 15]:

$$G_{\text{Q-PR}}(s) = K_p + \frac{2\omega_c s}{s^2+2\omega_c s+\omega_0^2}K_r, \tag{22}$$

where K_p is the proportional coefficient, K_r is the resonant coefficient, ω_c is the cut-off frequency which generally ranges from 5 to 15 rad/s, and ω_0 is the resonant frequency.

Thirdly, the three-phase voltage modulation waves u_{aref}, u_{bref}, and u_{cref} can be obtained by a $\alpha\beta/abc$ transformation. In addition, the three-phase voltage modulation wave is changed from the sine wave to the flat top wave because of the injection of zero-sequence voltage which can effectively improve the utilization of the DC voltage.

The expression of u_0 is as follows:

$$\begin{aligned}u_0 = 0.5\big(&\max\left(u_{aref}, u_{bref}, u_{cref}\right)\\ &+\min\left(u_{aref}, u_{bref}, u_{cref}\right)\big).\end{aligned} \tag{23}$$

The three-phase modulation voltage after the injection of zero-sequence voltage is as follows:

$$\begin{aligned}u_{aref}^* &= u_{aref}-u_0,\\ u_{bref}^* &= u_{bref}-u_0,\\ u_{cref}^* &= u_{cref}-u_0.\end{aligned} \tag{24}$$

Finally, the voltage references u_{aref}^*, u_{bref}^*, and u_{cref}^* are easy to generate the pulse width modulation (PWM) signals to drive the three-phase converter.

5.4. Simulation Results. A simulation model for a 10 MW/±40 kV MMC system was constructed using PSCAD/EMTDC to verify the theoretical analysis for the electrical quantities of the MMC. The system structure is shown in Figure 5, and the simulation parameters are shown in Table 4. When $t = 3$ s, the grounding short-circuit fault of phase A occurs, and the duration time of fault is 1 s.

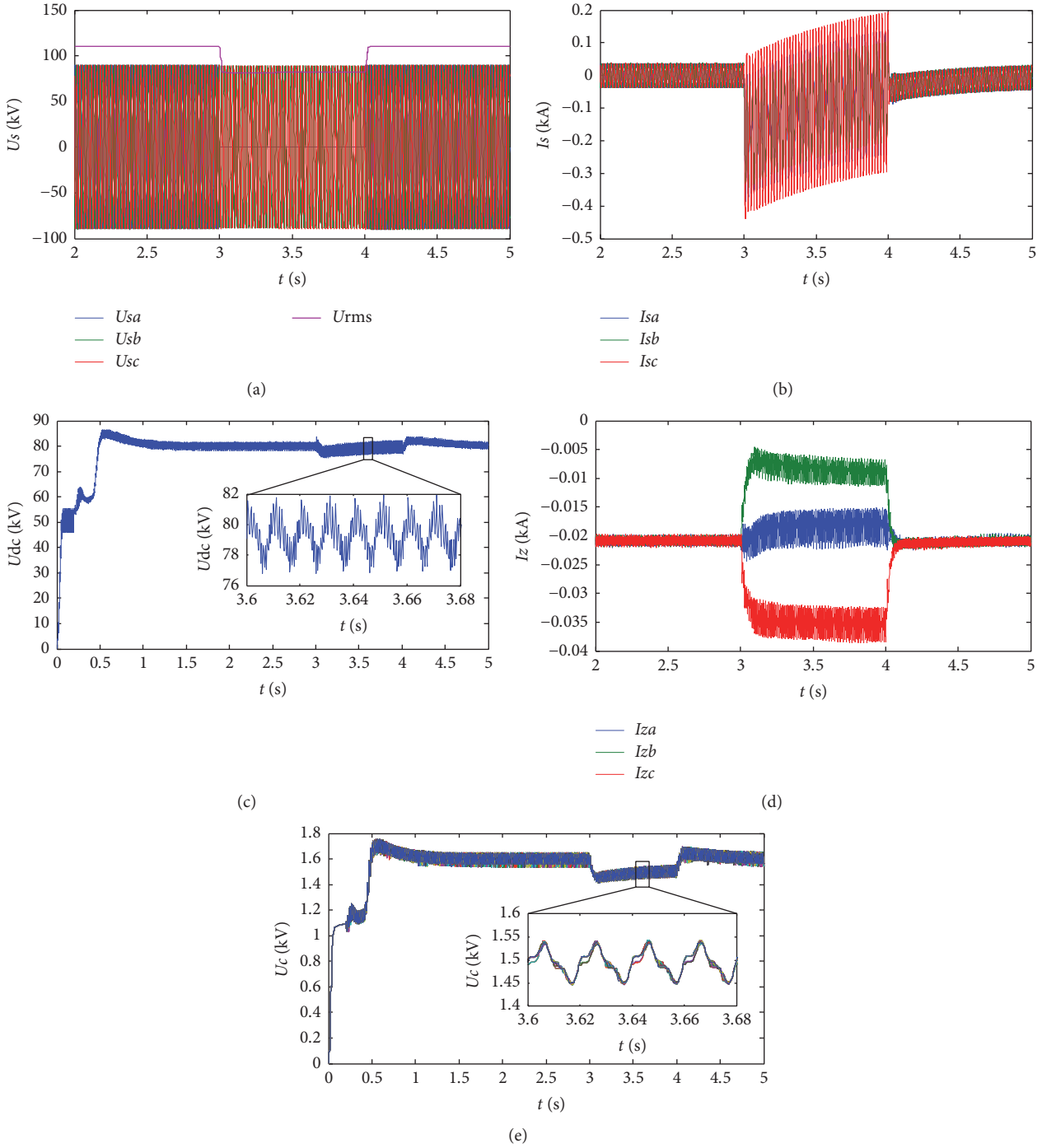

FIGURE 17: Simulation results without suppressing the negative-sequence current. (a) Phase voltage of AC grid. (b) Phase current of AC grid. (c) DC voltage. (d) DC component of the circulating current. (e) Capacitor voltage.

As can be seen from Figure 17, the grounding short-circuit fault of phase A occurs when $t = 3$ s (Figure 17(a)), and the three-phase current of AC grid is seriously asymmetric (Figure 17(b)); there is the second-order harmonic component in the DC voltage (Figure 17(c)); the DC component of the three-phase circulating current is not symmetrical (Figure 17(d)); the amplitude of the capacitor ripple voltage of the SM is increased (Figure 17(e)). In summary, the simulation results verify the correctness of the theoretical analysis.

In Figure 18, similarly, the grounding short-circuit fault of phase A occurs when $t = 3$ s (Figure 18(a)). Because the negative-sequence current is suppressed, the three-phase current of AC grid is symmetric (Figure 18(b)). The second-order harmonic component in the DC voltage (Figure 18(c)), the DC component of the three-phase circulating current

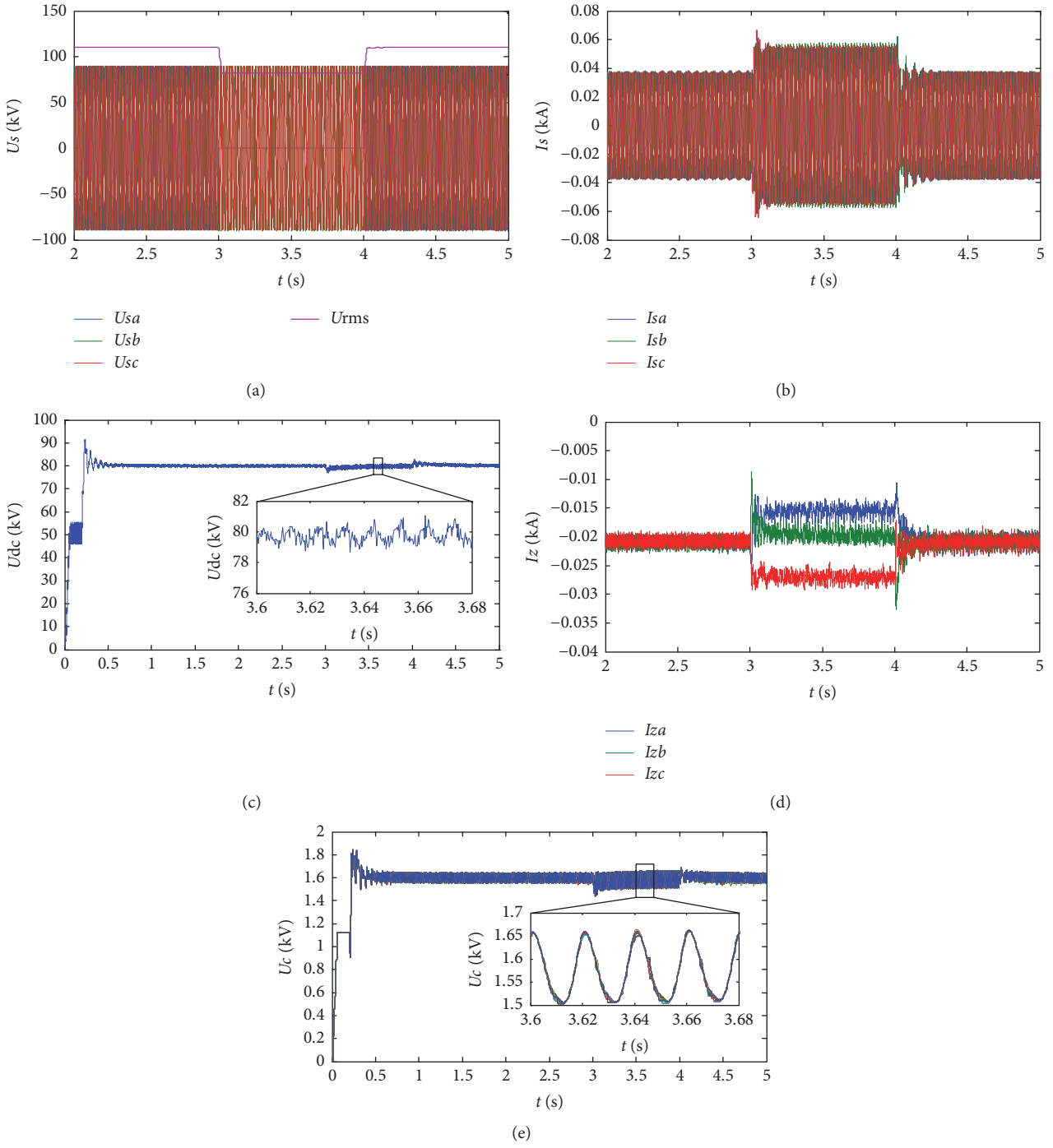

FIGURE 18: Simulation results with suppressing the negative-sequence current. (a) Phase voltage of AC grid. (b) Phase current of AC grid. (c) DC voltage. (d) DC component of the circulating current. (e) Capacitor voltage.

(Figure 18(d)), and the amplitude of the capacitor ripple voltage of the SM (Figure 18(e)) all decreased; but they can not be completely eliminated, due to the existence of negative-sequence voltage.

6. Conclusions

In this paper, we studied the control strategy of the AC-DC-AC substation based on MMC. Firstly, a parallel sorting algorithm based on FPGA to solve the MMC capacitor voltage balancing problem was studied. This algorithm can be performed in four clock cycles, and the computation time does not vary with changes in the number of submodules. And the experimental results verify the correctness of the sorting algorithm. Secondly, the effect of negative-sequence current on MMC is analyzed in theory and the correctness of the theoretical analysis is verified by simulation. The effects mainly include the following: the DC component of the

Table 4: Simulation parameters of MMC.

Parameters	Values
Rated capacity of MMC	10 MVA
Transformer ratio (Y/Δ)	110 kV/40 kV
Rated DC voltage of MMC	±40 kV
Number of SMs of each arm	50
Capacitance of each SM	1400 μF
Arm inductance	140 mH

three-phase circulating current is not symmetrical; the amplitude of the capacitor ripple voltage of the SM is increased; and there is the second-order harmonic component in the DC voltage. Also, the effective suppression of negative-sequence current is achieved by using PR controller.

Conflicts of Interest

The authors declare no conflicts of interest.

References

[1] L. Battistelli, M. Pagano, and D. Proto, "2× 25-kV 50 Hz high-speed traction power system: Short-circuit modeling," *IEEE Transactions on Power Delivery*, vol. 26, no. 3, pp. 1459–1466, 2011.

[2] Z. Shu, S. Xie, and Q. Li, "Single-phase back-to-back converter for active power balancing, reactive power compensation, and harmonic filtering in traction power system," *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 334–343, 2011.

[3] C. Wu, A. Luo, J. Shen, F. J. Ma, and S. Peng, "A negative sequence compensation method based on a two-phase three-wire converter for a high-speed railway traction power supply system," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 706–717, 2012.

[4] A. Luo, F. Ma, C. Wu, S. Q. Ding, Q.-C. Zhong, and Z. K. Shuai, "A dual-loop control strategy of railway static power regulator under V/V electric traction system," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 2079–2091, 2011.

[5] L. Qunzhan, Z. Jinsi, and H. Weijun, "Study of a new power supply system for heavy haul electric traction," *J. China Railw. Soc*, vol. 10, no. 4, pp. 23–31, 1988 (Chinese).

[6] X. He, Z. Shu, X. Peng et al., "Advanced cophase traction power supply system based on three-phase to single-phase converter," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5323–5333, 2014.

[7] X. He, A. Guo, X. Peng, Y. Zhou, Z. Shi, and Z. Shu, "A traction three-phase to single-phase cascade converter substation in an advanced traction power supply system," *Energies*, vol. 8, no. 9, pp. 9915–9929, 2015.

[8] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737–1746, 2009.

[9] X. Li, Q. Song, J. Li, and W. Liu, "Capacitor voltage balancing control based on CPS-PWM of modular multilevel converter," in *Proceedings of the 3rd Annual IEEE Energy Conversion Congress and Exposition, ECCE 2011*, pp. 4029–4034, usa, September 2011.

[10] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 662–669, 2005.

[11] Q. Tu, Z. Xu, and L. Xu, "Reduced Switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Transactions on Power Delivery*, vol. 26, no. 3, pp. 2009–2017, 2011.

[12] S. Tingwei and J. Changjiang, "Parallel full comparison sorting algorithm based on FPGA," in *Digital Technology and Application*, vol. 10, pp. 126-127, 5 edition, 2013.

[13] Q. Song, W. Liu, X. Li, H. Rao, S. Xu, and L. Li, "A steady-state analysis method for a modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3702–3713, 2013.

[14] Q.-C. Zhong and T. Hornik, "Control of Power Inverters in Renewable Energy and Smart Grid Integration," *Control of Power Inverters in Renewable Energy and Smart Grid Integration*, 2012.

[15] Q.-C. Zhong and G. Weiss, "Synchronverters: Inverters that mimic synchronous generators," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1259–1267, 2011.