Upgrade of the ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC

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***Abstract*—The Large Hadron Collider (LHC) has envisaged a series of upgrades towards a High Luminosity LHC (HL-LHC) delivering five times the LHC nominal instantaneous luminosity. The ATLAS Phase II upgrade, in 2024, will accommodate the upgrade of the detector and data acquisition system for the HL-LHC. The Tile Calorimeter (TileCal) will undergo a major replacement of its on- and off-detector electronics. In the new architecture, all signals will be digitized and then transferred directly to the off-detector electronics, where the signals will be reconstructed, stored, and sent to the first level of trigger at the rate of 40 MHz. This will provide better precision of the calorimeter signals used by the trigger system and will allow the development of more complex trigger algorithms. Changes to the electronics will also contribute to the reliability and redundancy of the system.**

Three different front-end options are presently being investigated for the upgrade, two of them based on ASICs, and a final solution will be chosen after extensive laboratory and test beam studies that are in progress. A hybrid demonstrator module is being developed using the new electronics while conserving compatibility with the current system. The status of the developments will be presented, including results from the several tests with particle beams.

1. Introduction

The Large Hadron Collider (LHC) is a proton-proton collider with 14 TeV center of mass energy and design luminosity of $10^{34}\ cm^{-1}s^{-1}$. A series of upgrades have been planned which will have an increased average luminosity 5-7 times larger than the nominal Run-2 value. The ATLAS detector [1] is one of the two general purpose particle detectors at the LHC, and it consists of multiple sub-detectors which are designed to detect interesting particle physics events in 40 million bunch-crossings per second. The Tile Calorimeter is the central hadronic calorimeter in the central region of ATLAS (Fig. 1 (top)). Its purpose is to measure energies and directions of hadrons, τ-jets and leptons and contribute to the measurement of the missing transverse energy. It's comprised of two Extended Barrels and a central Long Barrel divided in two sections, each divided into 64 slices. They are made out of alternating thin steel plates and scintillating tiles (Fig. 1 (bottom)). Wavelength shifting fibers coupled to the tiles collect the light produced in the scintillators and are read out by photomultiplier tubes (PMTs).

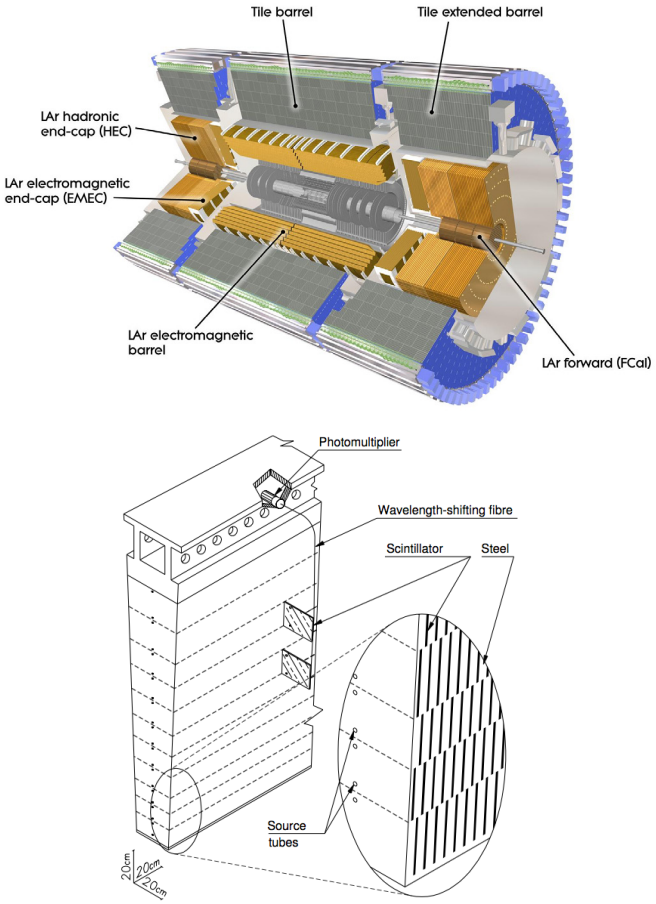

Figure 1. Artistic representation of the ATLAS calorimeters (top) and a Tile Calorimeter module slice (bottom).

2. Upgrade of the Tile Calorimeter

The Phase-II upgrade of the ATLAS Tile Calorimeter will culminate in 2024 for the HL-LHC. The detector components (absorber, scintillating tiles, fibers, and PMTs) are

largely in good shape and do not have to be replaced. However, the readout electronics are being completely redesigned and will provide data to the trigger at 40 MHz instead of at 100 kHz, with full cell energy precision instead of analog sums in projective towers.

A demonstrator project was defined in order to assess the long term performance of the upgraded system. The Demonstrator super-drawer is composed of four independent mini-drawers (Fig. 2 (top)), each of them equipped with 12 front-end boards of one of the three different options, shown in Fig. 3, one MainBoard for the corresponding front-end option, one Daughter Board that handles data processing and communications with the back-end electronics, one high voltage regulation board from the two options available, one adder base board plus 3 adder cards for the summation of the analog trigger signals to send to the Trigger, and one new Low Voltage Power Supply (LVPS). A fully functional demonstrator is integrated into the current ATLAS Timing, Trigger and Control (TTC) and Data Adquisition system (DAQ). The new low voltage system is designed with a high degree of redundancy, and supply voltages are generated using point-of-load regulators fed from 10V LV supplies. Active dividers in the base of each PMT block increase the linearity of the gain with High Voltage (HV). The chassis that houses the PMT blocks has been redesigned including a cable carrier for easier access during maintenance periods. The single design of the Daughter Board is equipped with a GBTx chip [2] that performs clock synchronization and recovery. The Daughter Board controls and configures the mini-drawers, and performs data serialization and duplicate transfer of the data out to the back-end electronics through the two dual QSFP+ links.

Due to the increase in radiation damage, the front-end pipeline memories will be shifted to the off-detector Tile PreProcessor (PPr) electronics, which will contribute to the serviceability of the system. A functional prototype of the Tile PPr [3] has been designed and produced by the University of the Witwatersrand in collaboration with the Instituto de Fisica Corpuscular in Valencia. A picture of the Tile PPr prototype is shown in Fig. 2 (bottom). Each PPr reads out one mini-drawer through one 10 Gbit Quad Small Form-factor Pluggable (QSFP) link, and serves a complete super-module. Data read-out and control is implemented over Ethernet using the IPBus protocol [4]. Furthermore it is equipped with a SFP module in order to send data to the existing Read-Out Drivers (RODs) resulting in a transparent integration into the data flow.

Each of the three front-end options processes the PMT signals, performs slow integration for Cesium calibration, and provide a Charge Injection System (CIS) for calibration purposes. The redesigned 3-in-1 cards provide pulse shaping with discrete components, bi-gain amplification (1x, 32x), and an analog trigger output compatible with the current Level 1 trigger system. Contrary to the QIE [5] that is a charge conveyor in an ASIC with no pulse shaping for the signal digitization. The third option is an ADC in an ASIC design called FATALIC [6], which has active pulse shaping and tri-gain amplification (1x, 8x, 64x) for the signal digitization. A picture of each of the front-end options is shown in Fig. 3.

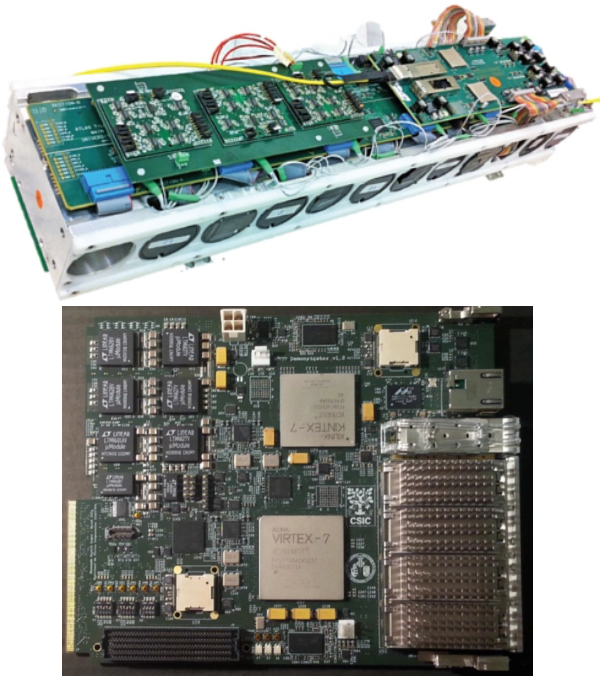

Figure 2. Picture of the top side of a mini-drawer (top) and the Tile PPr prototype motherboard (bottom).

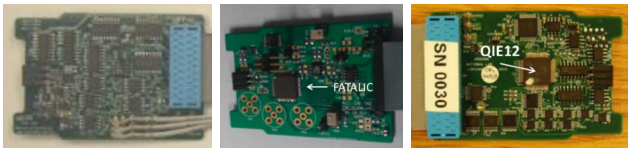

Figure 3. Pictures of the three front-end readout options: 3-in-1 (left), FATALIC (middle), QIE (right).

3. Testbeam campaigns

The three test-beam campaigns took place in 2015 and 2016 with the aim of testing the performance of the upgrade electronics with very good results. Several modules were equipped with these electronics and exposed to different beam particles (electrons, muons and hadrons) during these campaigns. The primary objective was to assess the status of the demonstrator based on the front-end baseline option, the modified 3-in-1. Attention was put also on the two alternative front-end options, QIE and FATALIC.

Calibration of the redesigned 3-in-1 board shows a strong performance for the upgrade system (Fig. 4). Achieved linearity is 0.3% and equivalent energy resolution is less than 0.1%. Performance results of the FATALIC (Fig. 5) and QIE (Fig. 6) are also very promising, with very little noise. Particle response will be measured again in the two test-beam campaigns scheduled for June and September of 2017

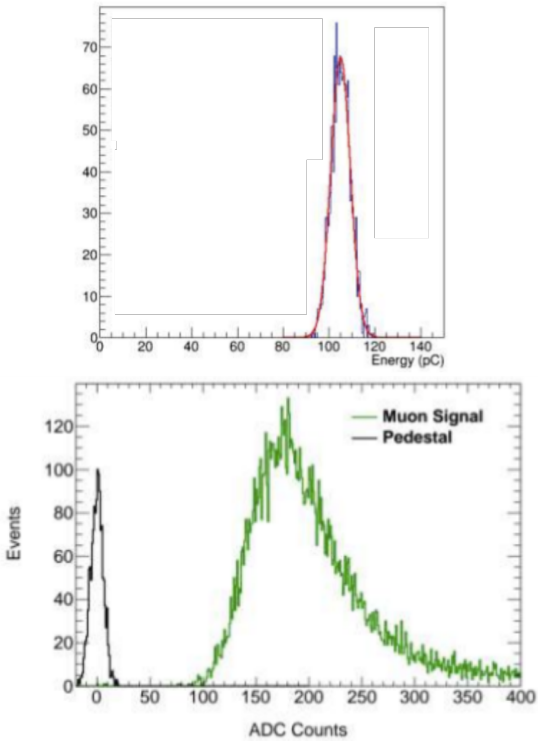

Figure 4. 3in1: Energy distribution for 100 GeV electrons (top), and muons signal response (bottom).

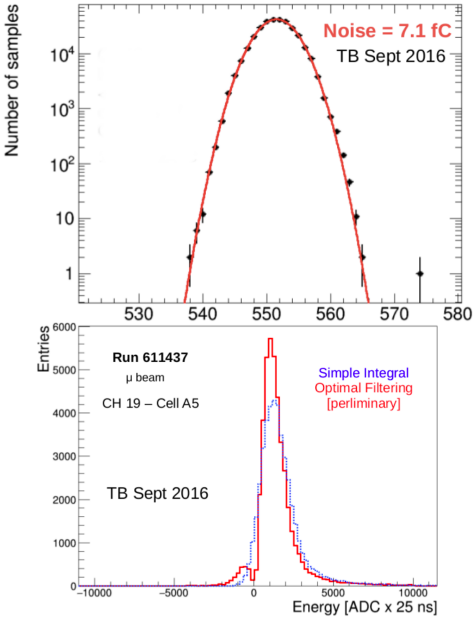

Figure 5. FATALIC: Electron signal response (top), and muons signal response (bottom).

4. Conclusions

The upgrade Phase-II program of the Tile calorimeter is progressing well. Three test-beam campaigns have taken place up to now to evaluate the performance of the three different front-end options looking forward for a drop-down selection in 2017. The reliability and stability of the system has been visibly improved with respect to the 2015 test-beam. The Demonstrator analog trigger signals output has been integrated successfully into the TDAQ infrastructure for the commissioning of the hybrid Demonstrator. The FE and HV option final selection process has been defined based on extensive comparison of the performances and other criteria. The Tile calorimeter system plans to complete the R&D stage and take a decision by the end of summer.

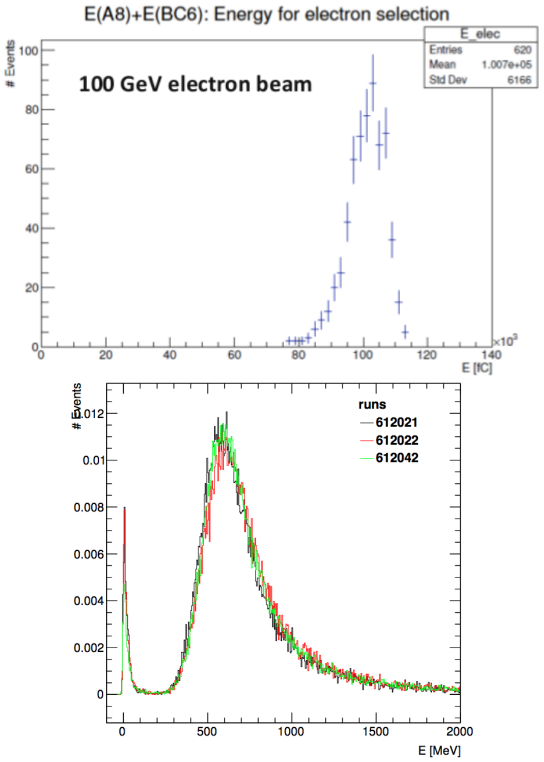

Figure 6. QIE: Energy distribution for 100 GeV electrons (top), and muons signal response (bottom).

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