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Review Article

A Review of Implementing ADC in RFID Sensor

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The general considerations to design a sensor interface for passive RFID tags are discussed. This way, power and timing constraints imposed by ISO/IEC 15693 and ISO/IEC 14443 standards to HF RFID tags are explored. A generic multisensor interface is proposed and a survey analysis on the most suitable analog-to-digital converters for passive RFID sensing applications is reported. The most appropriate converter type and architecture are suggested. At the end, a specific sensor interface for carbon nanotube gas sensors is proposed and a brief discussion about its implemented circuits and preliminary results is made.

1. Introduction

In the last years, many technological developments have dramatically expanded the functionality of RFID. Advances in microelectronics, embedded software, and RF/microwave-circuit integration are making new RFID applications possible [1]. Among these new applications, the use of passive RFID tags as environmental sensors has a huge number of possibilities [2], including the Internet of Things (IoT) [3] and human care assisting solutions [4].

There are too many ways to transform a RFID tag into a RFID sensor. Some of them exploit the sensitivity of the tag antenna to the physical characteristics of its surrounding environment or its influence on RFID chip response as reported in [5–7]. However, if the addition of sensing capabilities to passive RFID transponder is made by integrating a sensor interface to the digital core of tag's chip, a full set of components should be developed: more specifically, an analog-to-digital converter (ADC), a signal conditioning circuit to the sensors, and a multiplexing circuit to allow interfacing multiple sensors.

The key component for these augmented tags is clearly the analog-to-digital converter. When looking for possible solutions, the designer will face a huge number of architecture topologies and different approaches to implement it. This reality brings flexibility to design stage but also some incertitude about the rightest choice. In this context we present a survey analysis on the most suitable ADCs for RFID sensing applications.

2. Sensors Connected through the Digital Side

RFID tags with sensors connected through the digital side do not have any modification in the analog front-end circuit or antenna. The sensing data is usually transmitted to the reader upon a specific requesting command according to the communication protocol. The main advantages of this solution are its compatibility with the current RFID standards and its capability to interface multiple sensors.

A sensing tag compliant with an existing RFID standard will not need any modification on the corresponding reader's hardware or firmware to be read. It means that all existing commercial readers are potentially capable to get the sensing data of these improved RFID tags.

The capability to interface multiple sensors, in spite of the increased complexity on the tag circuitry, is also a notable advantage. Different kinds of sensors can be embedded on the same tag and almost any kind of sensor can be adopted (limited by the power consumption) making it a powerful sensing device.

The main challenge to design the components of the sensors interface is to meet the time and power constraints. Since all energy available in a given transponder is delivered by the reader, all steps of sensing, signal conditioning, and analog-to-digital conversion must be done as fast as possible to allow storing or transmitting the digital result before the end of communication and consequently end of powering energy. In other words, the protocol timeout constraints prohibit minimizing speed rates to save power.

3. Power Constraints

The major constraint for all passive RFID transponders is the limited amount of available power. A study on the main concerning about power constraints of HF RFID systems operating at free space is covered by this section. Systems embedded in different medium or in mixed medium needs a more complex analysis [23].

Near the field, the magnitude of the magnetic field along the central axis of a circular loop antenna can be calculated by

$$|H| = \frac{NIR^2}{2\sqrt{\left(R^2 + d^2\right)^3}}, \quad (1)$$

where N is number of windings, I is the current through the antenna, R is the antenna radius, and d is the distance from the center of antenna plane [24]. Far from the field, that is, for $d > \lambda/2\pi$, the magnitude of the magnetic field can be calculated by [25]

$$|H| = \frac{NIR^2}{4}\sqrt{\left(\frac{1}{d^3} - \frac{\omega^2}{dc^2}\right)^2 + \left(\frac{\omega}{cd^2}\right)^2}. \quad (2)$$

For the 13.56 MHz ISM band (13.56 MHz ± 7 kHz) European regulations limit the magnetic field strength to 60 dBμA/m at 10 m from the reader [26], while current American FCC rules limit to 42 dBμA/m at 10 m from the reader. This difference should be harmonized in the near future [27]. Considering both regulations, (1) and (2) can be used to calculate the magnetic field strength generated by a reader operating at maximum power limit as depicted in Figure 1. The magnetic field strength generated by a typical HF reader along its central axis is also represented as referential.

According to the ISO/IEC 15693-2 [28] the RFID transponders should be able to operate at a magnetic field of 150 mA/m (103.5 dBμA/m). This field strength corresponds to a maximum operating distance of approximately 1 meter by European regulations or 50 centimeters by American FCC rules. However, RFID tags featuring a power consummation below the standard defined limit can operate at longer distances. Theoretically the maximum operating distance will be the limit of far field to near field, where the magnetic coupling is no more possible. This corresponds to approximately 3.5 meters for 13.56 MHz. In other words, RFID HF tag consuming less than 69.7 dBμA/m or 51.7 dBμA/m will be able to operate at the maximum distance of 3.5 m

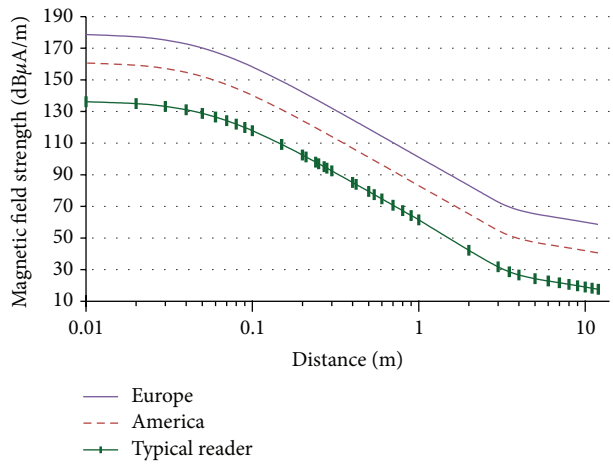

Figure 1: Maximum allowed magnetic field strength for 13.56 MHz ISM band according to European and American regulations (60 dBμA/m @ 10 m and 42 dBμA/m @ 10 m, resp.). The lower curve represents the magnetic field strength of a typical HF reader (square coil, 10 × 10 cm, 6 turns, 125 mA).

under European and American regulations, respectively. When the ISO/IEC 14443-2 (NFC standard) [29] is adopted, the minimum magnetic field required for a transponder operation is 1.5 A/m (123.5 dBμA/m), which corresponds to a maximum communicating distance of 42 centimeters by European regulations or 20 centimeters by American FCC rules.

A recent NF4 NFC tag chip, developed by EM Microelectronic, requires only 0.7 A/m (116.9 dBμA/m) for activation [30] (less than a half of the minimum required by ISO/IEC 14443-2), being able to operate at approximately 54 centimeters of distance from the reader (considering European regulations). Taking such commercial solution as the state of the art, it is possible to conclude that similar tags including some sensing circuitry will operate below 54 centimeters, since the sensor interface and the sensor itself will draw more energy, requiring a strongest field to be powered. Evidently, active RFID sensor tags can operate at longer distances, since their energy is not provided by reader's communication field.

4. Timing Constraints

Besides the above explained power constraints, sensor interface circuits and sensor itself should comply with timing constraints imposed by standardized communication protocol. The time constraint related to the chosen protocol should be taken into account for circuit design and choice of sensors. Analog-to-digital converter and signal conditioner are usually the most time consuming circuits:

$$T_{\mathrm{AFE}} + T_{\mathrm{Core}} + T_{\mathrm{ADC}} + T_{\mathrm{SCC}} + T_{\mathrm{MUX}} + T_{\mathrm{Sens}} \leq T_1, \quad (3)$$

where T_{AFE} is the response time of the analog front-end circuit for a transmission operation, T_{Core} is the time need by the digital tag's core to complete all operations related to command decoding and sensor interface control, T_{ADC} is

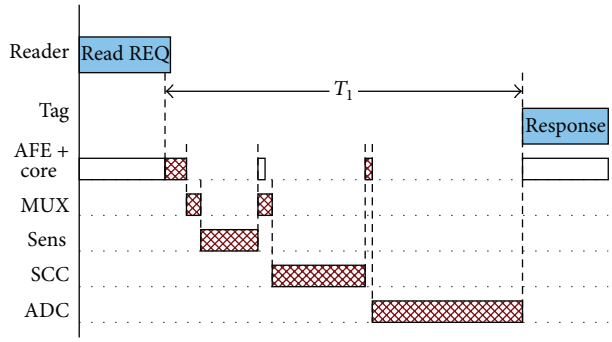

Figure 2: Time diagram of a full sensor reading sequence. Only crosshatch slices are taken into account for total T_1 time internal.

the time interval of one complete analog-to-digital conversion (including sample holding time), and T_{SCC} and T_{MUX} are the time consumed by signal conditioning circuit and multiplexer, respectively, before to deliver the sensor signal to ADC. T_{Sens} is the response time of the sensor, that is, the time between its powering and a correct output. Finally, T_1 is the maximum allowed time for a tag to reply on a reading alike request. The time diagram of a full sensor reading sequence performed by a RFID sensing tag is depicted in Figure 2.

For HF tags complaint with ISO/IEC 15693 protocol, the timeout constraint for T_1 is defined as [31]

$$T_1 = \begin{cases} \dfrac{4192}{f_C}, & \text{minimum,} \\ \dfrac{4224}{f_C}, & \text{nominal,} \\ \dfrac{4256}{f_C}, & \text{maximum.} \end{cases} \quad (4)$$

For NFC complaint tags, the ISO/IEC 14443 protocol defines the timeout constraint for T_1 as [32]

$$T_1 = \begin{cases} 4096 * \dfrac{2^0}{f_C}, & \text{minimum,} \\ 4096 * \dfrac{2^4}{f_C}, & \text{nominal,} \\ 4096 * \dfrac{2^{14}}{f_C}, & \text{maximum.} \end{cases} \quad (5)$$

Solving both (4) and (5) for the nominal carrier frequency (13.56 MHz), the minimum and maximum timeouts are 309.14 μs/313.86 μs for ISO/IEC 15693 protocol and 302.06 μs/4949 ms for ISO/IEC 14443 protocol. This way, a sensing system targeting both standards should consider the most restrictive timing limits, that is, 309.14 μs as the minimum timeout and 313.86 μs as the maximum timeout.

5. Cost and Size Constraints

The size of passive RFID tags is usually constrained by its antenna size since all other components are integrated on a tiny silicon chip plus a small tuning capacitor (sometimes even the tuning capacitor is integrated on the chip), taking an area of no more than some few square millimeters. Furthermore, the antenna type and size have also a huge impact on tag costs. This way, aspects of cost and size are treated together, departing from the tag antenna characteristics.

There are basically three types of antennas currently adopted for HF RFID tags:

(i) Ferrite core coil antenna.

(ii) Planar spiral coil antenna.

(iii) Air core copper wire coil antenna.

Ferrite core coil antennas presents a small aperture but allows a very good read range when well aligned with the interrogator reading field. In spite of its small form factor, it is still being a not flexible and thicker component, which makes it not convenient for integration with stickers, product labels, or other common applications where a flat element is desirable. Moreover, its cost is typically ten times greater than the equivalent printed coil in high volume [33].

Planar spiral antenna is one of the most common types currently in use. They can be fabricated with copper over FR4 (or similar substrate) by etching process or printed with some conductive ink over paper or a polymer substrate. The last one is the most cost effective, allowing mass production, but is also the less robust solution. Its low cost and physical characteristics makes this type of antenna the best suited for mass consumer applications.

Air core copper wire coil antenna is an alternative for planar spiral coils. Similar coil shapes implemented in planar solutions can be made in air core wire coil but taking the benefit of a lower parasitic series resistance and the possibility to stack multiple wire turns to reduce the inner or outer coil dimension. Furthermore, since its terminals are wire ends, it can be easily connected to IC pads or other standard electronic components without dedicated machinery. They are usually thicker and more expensive than printed planar spiral ones.

Generally speaking, the minimum area of a given tag antenna is constrained by the power required by its circuitry and the desired operating distance from the reader. As much as the power consumption increases, bigger will be the area of antenna needed to harvest this energy from the reader at the same distance. Longer communication distances will also require bigger antennas to provide the same amount of energy.

The impact of the required power over the tag size can be estimated regarding the elementary model of an HF RFID tag front-end with a resistive load (Figure 3) and its corresponding Q factor equation [24]

$$Q = \frac{1}{R_P/\omega L + \omega L/R_L}, \quad (6)$$

where R_P is the parasitic series resistance of antenna, L is the inductance of antenna, ω is the carrier frequency, and R_L is the load resistance.

For evaluation purposes, two sets of planar square spiral coil antennas were designed and simulated. Considering that

Table 1: Q factor and conductive ink area for two sets of planar spiral coils.

Coil area (mm^2)	Approach 1		Approach 2	
	Q	Ink area (mm^2)	Q	Ink area (mm^2)
144	28.98	57.56	28.98	57.56
225	21.60	76.76	30.40	100.71
324	16.85	95.96	30.46	130.15
441	13.67	115.16	29.69	168.92
576	11.44	134.36	29.24	167.75

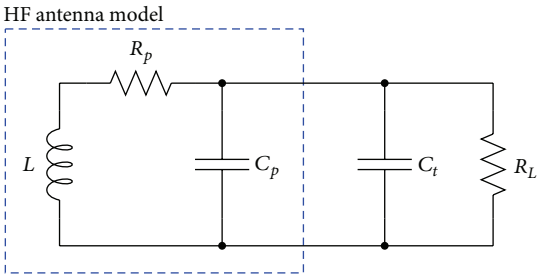

Figure 3: Elementary model of an HF RFID tag front-end and load.

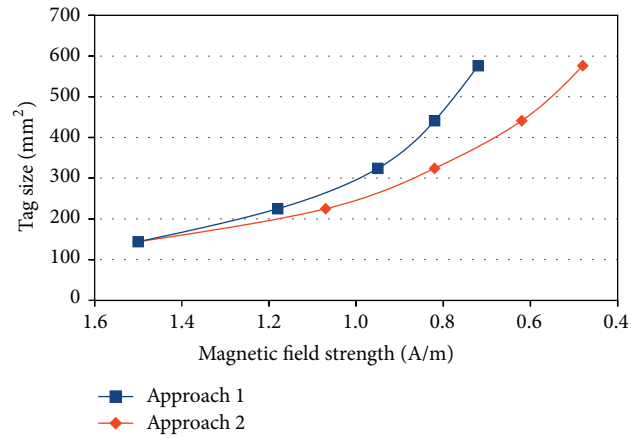

Figure 4: Minimum HF tag size according to two different approaches. Approach 1: coil tracks were designed with minimal width to save conductor costs. Approach 2: coil tracks where designed with optimal width and number of turns to keep the same quality factor.

the amount of conductive ink is an important parameter for the cost of printed antennas, the design approach of the first set of coils took the ink savings as the main priority, regardless Q factor. For the second set, coils were designed taking the Q factor as the main priority, regardless the amount of conductive ink needed. The resulting Q factor and the total ink area for each coil is presented on Table 1. For both sets a fixed resistance of 3 kΩ was adopted as circuit load.

The two sets of tag antennas were simulated considering the losses of a full bridge rectifying circuit, coil parasitics and proper tuning capacitors for 13.56 MHz carrier frequency. All simulations were performed to obtain the minimum magnetic field strength needed to deliver 1.6 mW to the load. Simulation results are depicted on Figure 4.

As one can see, the relationship between cost, size, and power demand is quite evident. As much as the field strength decreases, bigger is the coil area needed to provide the same power to the load. Cost reduction with conductive ink also impacts the coil area. For all simulations, the magnetic field strength was considered uniform and constant along of whole coil area. Evidently, in real case this convenient assumption will be seldom satisfied, making necessary bigger coils for practical operations [34].

When RFID tags with sensing capabilities are considered, the cost of integrated sensors and the sensor integration itself may take values much higher than those involving antenna fabrication and chip integration. Temperature sensors for usual environment conditions (−20 to 50 Celsius) can be easily integrated with the tag circuitry at very low cost. A light sensor can be easily integrated onto a chip but needs a special care on tag packaging to allow the light entrance. However, other sensors may need a special fabrication process which is not compatible with current CMOS processes used for tag circuit fabrication. Its integration requires more complex and expensive techniques, besides the additional costs of a dedicated packaging.

For mass production at low cost the most promising alternative are fully printed sensors (or *thick film* sensors). Its fabrication processes can be easily adequate with the process of printed antennas. Furthermore, some printed and flexible sensors such as photodetectors, temperature sensors or gas sensors are transitioning from R&D to mass production [35].

6. Sensor Interface

A generic diagram of a passive RFID tag with a multiple sensor interface integrated to its digital core is shown on Figure 5. The sensor interface is composed by three main components: a multiplexer, a signal conditioner, and an analog-to-digital converter.

Once the energy is the most scarce resource in such systems, the role of the multiplexer is not only to select the sensor signal to be processed but also to select the sensor witch should be powered, keeping others unconnected to save that power. Even the selected sensor should be switched off as soon as the ADC sample-and-hold circuit finishes its job. Some sensors need a significant warm-up time before to be ready for correct readings. These kinds of sensors are not appropriated for passive RFID solutions and should be avoided if possible.

The signal conditioning circuit is also a very common need when a sensor signal should be sent to a analog-to-digital converter. Although its clear importance, the signal conditioning circuit should be minimized in order to save power. Generally speaking, four different solutions are proposed for this block, being only one (the last) a real signal conditioning:

(i) *Bypass and ADC Input Range Statically Adjusted*. If the adopted ADC has an adjustable input range and only one sensor is interfaced or multiple sensors with similar output voltage range, the input range of A/D

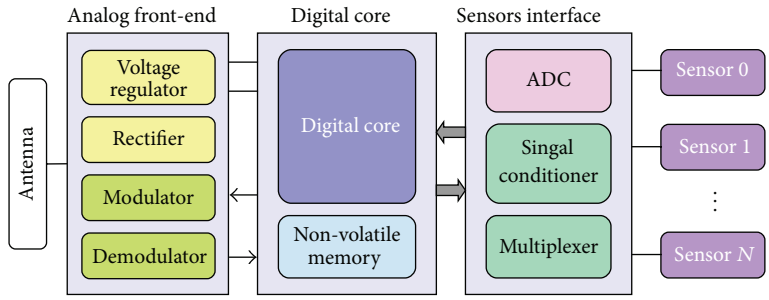

Figure 5: A generic diagram for a passive RFID tag integrated with a multiple sensor interface.

converter can be adjusted to fit the sensor signal range and the signal conditioning circuit eliminated. This solution is very light in terms of power consumption but in practice can only be adopted in some cases because ultralow power ADCs usually have a limited capability of input range adjusting, specially for small differences between minimum and maximum voltages.

(ii) *ADC Input Range Dynamically Adjusted*. If the adopted ADC has an adjustable input range and multiple sensors with nonsimilar output voltages are interfaced, the input range of the analog-to-digital converter can be dynamically adjusted to fit the signal range of the selected sensor according to previous established values stored into tags memory or physically defined component values. Once more, the major problem is the limited capability of ADC input range adjusting.

(iii) *Bypass and High Resolution ADC*. This solution consists in adopting an ADC with a resolution much higher than the needs of target application in order to avoid spending power with analog signal conditioning. Although the consummation of a high resolution ADC is higher than the similar one with a minimum adequate resolution, the additional power can be smaller than the necessary to support an analog conditioning circuit.

(iv) *Signal Conditioning*. Depending on the sensor, different signal treatments can be necessary. The most common treatments considering a voltage signal are offset and gain adjusts. Instrumentation amplifiers (IAs) are usually employed in conventional sensor signal conditioning circuits. However, conventional IAs are too much power consuming for passive RFIDs. Even the best current commercial low power devices [36, 37] consumes about of 72 μW which is almost twelve times the whole power requested by the best commercial UHF tag. In other hand, application specific IAs have been reported at much lower power consuming like 3 μW [38], 1.8 μW [39] and even 192 nW [40], indicating that its use is possible for RFID sensing tags at HF and UHF as well.

Notwithstanding, sensing RFID tags for some specific applications can dispense the ADC, the multiplexer and even have a conditioning circuit as simple as a RC. The detection of product seal violation [41] is a good example of sensing RFID tags without an analog-to-digital converter. The threshold detection of a given quantity can also be implemented using a simple Schmitt trigger gate and some few components. In this case, the sensing tag will not be able to provide a precise information about the quantity magnitude but only its placement below or above a previous defined threshold.

Although the ADC is not a mandatory component to read sensors through the digital side of a RFID transponder, a generic sensor interface should have at least one, specially if the information about the quantity magnitude should be acquired. Since the ADC is usually the most complex and critical component of the sensor interface, its design tends to be the major challenge. Its characteristics also have influence over the signal conditioning circuit or are influenced by it. A right choice on the most appropriated converter type and implementation approach is very important at this point. A more careful analysis about analog-to-digital converters for passive RFID sensing applications will be carried out on the next section.

7. ADCs for RFID Sensing Applications

A good indication of the most appropriated ADCs for RFID sensing applications can be found looking for the most energy-efficient implementations reported on VLSI and ISSC conferences. Taking the power consumption as the main guideline, the figure of merit (FOM) of more than 400 analog-to-digital converters reported on VLSI and ISSC [42] over the last ten years were classified according to its type and represented on Figure 6.

Since 2007 the most efficient converter year after year is the successive approximation register (SAR) [43], followed by pipeline and Delta-Sigma types. More specifically, except by the converter proposed by Patil et al. [17], all ADCs featuring a FOM below 7 fJ/Conversion-step are SAR type with a capacitive DAC implementing some variation of the charge redistribution approach, first proposed by [44].

When the figure of merit of all the reported CMOS ADCs since 1997 to the present are organized by the technology node, the result is a clear advantage of SAR type for all nodes below 350 nm as can be seen in Figure 7.

Table 2: The most efficient converters reported on VLSI and ISSCC since 2008.

Ref.	Type	FOM (fJ/Conv-step)	fs (MHz)	P (uW)	ENOB	Tech. (nm)
[8]	SAR	4.4	1.00	1.90	8.7	65
[9]	SAR	6.3	1.10	1.20	7.5	40
[10]	SAR	6.5	4.00	17.44	9.4	90
[11]	SAR	3.2	0.10	0.17	9.1	90
[12]	SAR	2.2	0.04	0.10	10.1	65
[13]	SAR	2.4	0.50	0.50	8.7	90
[14]	SAR	2.0	0.25	0.20	8.6	90
[15]	SAR	4.4	0.03	0.35	11.3	65
[16]	SAR	0.9	0.20	0.08	8.9	40
[17]	Async.	3.7	80.00	24.00	6.4	28
[18]	SAR	2.4	0.08	0.11	9.1	65
[19]	SAR	6.6	0.10	0.12	7.5	180
[20]	SAR	1.5	0.10	0.09	9.2	65
[21]	SAR	5.5	6.40	46.00	10.4	40

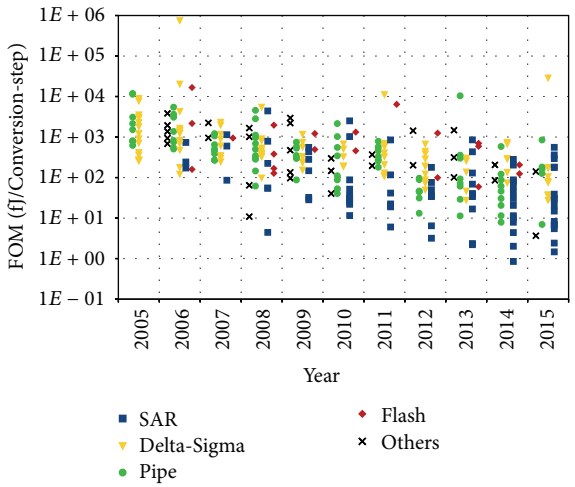

Figure 6: Figure of merit (FOM) of the reported ADCs on ISSCC and VLSI over the last ten years.

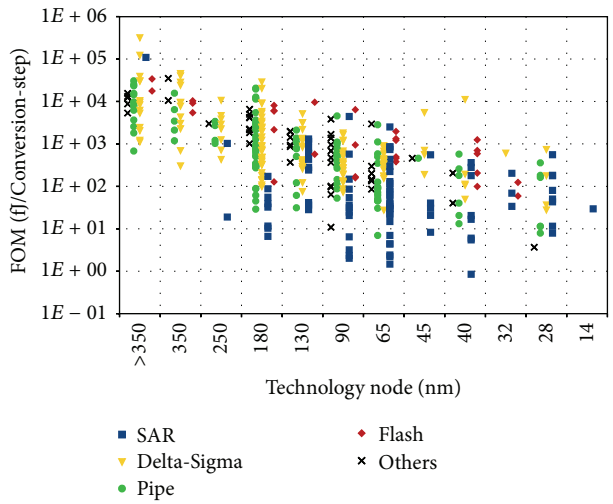

Figure 7: Figure of merit (FOM) of the reported ADCs on ISSCC versus technology node. Only designs on CMOS processes were considered.

The most efficient converters reported on VLSI and ISSCC since 2008 are listed with more details on Table 2. The limit of 7 fJ/Conversion-step was arbitrary chosen.

Almost all these converters were implemented in CMOS 90 nm or below. A remarkable exception was proposed by Jeong et al. [19]. A 7.5 ENOB SAR ADC achieving a very low FOM and very low power consumption (about of 100 nW) using a relatively old technology (180 nm). In fact, this is only reported ADC above 90 nm featuring a FOM below 10 fJ/Conversion-step. The converter uses a charge recycling technique which saves previous sample MSB voltage and reuses it throughout subsequent conversions, preventing unnecessary switching of large MSB capacitors as well as conversion cycles.

It is important to note that a good analog-to-digital converter for passive RFID sensing applications should have not only a low FOM but also very low power consumption. Some solutions as the asynchronous converter proposed in [17] or the pipeline converter proposed in [45] achieves a very low FOM but under high sampling rates and higher overall power consumption than other similar solutions with lower sampling rates.

In spite of the the very good results achieved by recent ADCs on Table 2, there are other aspects to be considered before to choose a specific design for a given application. The target technology node, silicon area, operating temperature and calibration procedures are only some of most common aspects. All the things considered, the choice can fall on an ADC which the power consumption is not exactly the lowest one. Fortunately, depending on the operating distance and the size of tag antenna, the power available to an HF RFID tag can be quite high. For instance, the power induced onto a tag load by the typical HF RFID reader refereed on Figure 1

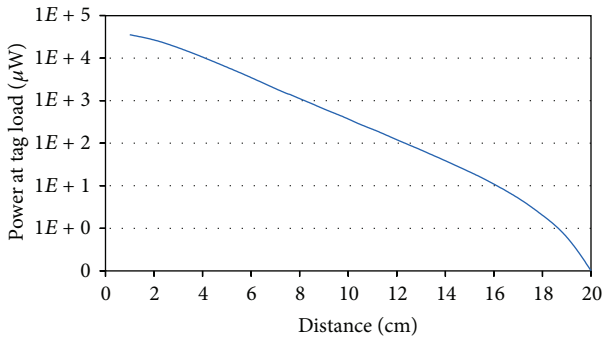

Figure 8: Power induced onto a tag load by a typical HF RFID reader according to its distance from the reader. The reader antenna is a square coil, 10 × 10 cm, 6 turns, and 125 mA. The tag is equipped with a square spiral planar coil, 12 × 12 mm, 8 turns.

was simulated according to its distance from the reader. For this simulation a tag equipped with a small square spiral planar coil (12 × 12 mm, 8 turns) connected to a 3 kΩ load was assumed. Simulation results are presented in Figure 8.

As one can see, there is virtually no power issues for short distances. On the other hand, for communication distances above 14 cm the available power is only some few μW, requiring a more careful choice of the analog-to-digital converter. At 14 cm, the available power to the tag load is about of 39 μW. The standard tag circuitry consumes between 15 and 25 μW. It means that the power portion left for the whole sensing circuitry (ADC + signal conditioner + sensor multiplexer) is about of 14 to 24 μW. Since the Signal conditioner uses to demand a significant power, is reasonable assume that the the power left to the ADC will not be more than a half of this total, that is, 7 μW.

According to the previous timing analysis (Section 4), the maximum and minimum timeouts for HF RFID tags complaint with both ISO/IEC 15693 and 14443 standards, are between 309.14 μs and 312.86 μs. Considering that part of this time will be consumed by the tag's logic core, analog front-end and sensor interface component delays, the time left for one analog-to-digital conversion will be slightly smaller. In practice it will correspond to conversion data rates between 3.5 and 5 kSample/s.

Summarizing, in order to be appropriate for passive HF RFID sensing at a reasonable distance from reader, an ADC should have a maximum power consumption of 7 μW, assuming the worst case and leaving some power margin to other sensor interface blocks and the sensor itself. Concerning the timing constraints, a minimum sample rate of 3.5 kSample/s should be satisfied. Only three ADCs listed on Table 2 do not fulfill these conditions. All others are SAR type and satisfy both constraints with a good margin.

In fact, the charge redistribution SAR ADC is a very suitable solution for passive RFID sensing as demonstrated by Brenk et al. in [46]. An ultra-low power 8-bit SAR ADC has been designed and used to implement a passive temperature sensor UHF RFID tag able to establish a stable communication up to 6.5 m from the reader.

8. Proposed Sensor Interface

Recent researches in nanotechnology field demands for small sized gas reactors called micro- and nanoreactors [47–49]. Essentially, these reactors are small volume chambers, typically less than 1 mL, equipped with gas input and output channels and micro-sensors inside. The design and construction of these systems aims at a comprehensive control of factors such as size, configuration, surface quality, integration, and costs. Works on high performance mass and pressure sensors based on carbon nanotubes have already been reported [50, 51]. The micro- and nanoreactors are at the base of high performance nanodevices, allowing a more detailed assessment of physical and chemical processes occurring inside and on the surface of the nanostructures as compared with more conventional sensors.

A common issue with these micro-reactors is connecting the inside sensors to outside world where all measuring instruments are placed. In conventional approaches these connections pass through the chamber walls by mean of metal pins electrically insulated from the body using some hard material like borosilicate sealing glass. The problem with that solution is the inconvenient gas leakage caused by failures in insulation material due to the stress they are submitted. This problem can be eliminated replacing pins and insulator by some kind of wireless communication. For that, an RFID solution is proposed.

Since the main goal is eliminating all sensor pins, the distance between tag and reader is not a big issue. Moreover, since all intended gas reactions can be well monitored taking 5 samples per second, a HF RFID system can nicely satisfy all requirements. In addition, an integrated solution containing sensors and all the measuring circuitry could help the adoption of these reactors for non-scientific applications.

Although the possibility of operate close to the reader antenna, where the magnetic field strength is high, the available energy to the tag should not be too high due to the small communication inductor ("antenna") which area is very limited by internal micro-reactor dimensions. On the other hand, the accuracy required by such scientific applications demands a good signal conditioning circuit which prohibits some power saving alternatives.

The proposed interface and sensors to be integrated on a passive HF RFID tag are briefly explained on the next sections.

8.1. Temperature Sensor. The temperature is an important player on most chemical reactions. Additionally, the behavior of carbon nanotube gas sensors is also influenced by environment temperature. The capacity to measure it simultaneously to gas measurements gives to the system valuable information to improve its accuracy.

A low power temperature sensor was designed based on the Zero Temperature Coefficient (ZTC) concept. According to [52], most of current CMOS technologies present a specific biasing point where temperature effect over the carrier mobility and voltage threshold cancel each other for a wide range of temperatures. If the ZTC point of a given transistor is known, it is possible to design a temperature independent

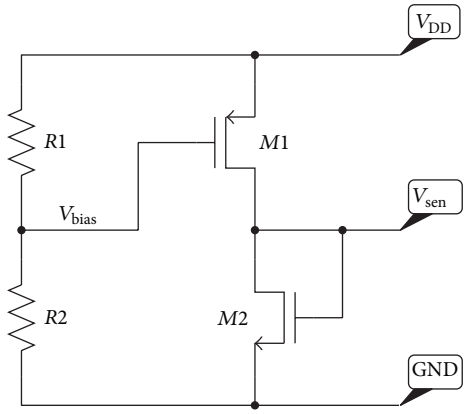

Figure 9: Low power temperature sensor based on ZTC characteristic of MOS devices.

constant current source in s very simple way. If such constant current is applied through a diode connected MOS, its V_{GS} will be given by [53]

$$V_{GS} = V_{GSF} + \alpha_{VT} T \left(1 - \sqrt{\frac{I_D}{I_{DF}}}\right), \quad (7)$$

where V_{GSF} and I_{DF} are the gate-to-source voltage and drain current of the current source MOS operating at ZTC point and α_{VT} is the threshold voltage temperature coefficient. So, under constant drain current the gate-source voltage is proportional to the temperature.

The implemented low power temperature sensor is depicted in Figure 9. $M1$ is the constant current source biased at ZTC point by $R1$ and $R2$. $M2$ is the sensing device. The circuit was designed to operate under a 1 V power supply, the current through $M1$ was about 10 nA and $R1$, $R2$ totaling about of 10 MΩ. The total power consumption of whole sensor is about of 110 nW.

The sensor was fabricated in 180 nm CMOS process (Figure 16) and tested for a temperature range from −30 to 130°C (−22 to 266°F). The simulated and measured response of the designed temperature sensor are shown in Figure 10.

As one can see, the empirical response of the temperature sensor is even more linear than the simulated one. Since the observed deviation of the simulated output from the ideal linear behavior is mostly related to the variation of the ZTC operation point of $M1$ (Figure 9), this improved response is probably due to a small variation in threshold voltages of fabricated MOS transistors or due to a fortunate combination of mutual canceling effects in designed layout which places high sized biasing resistors and a very large pMOS transistor.

The temperature error between the measured sensor output and an ideal linear response within the entire tested temperature range is represented on Figure 11. The highest absolute error occurs in 130°C, being approximately 1.8°C, or 1.38%. The absolute error remains smaller than 0.1°C for temperatures bellow 60°C and smaller than 0.5°C for temperatures between 60°C and 115°C.

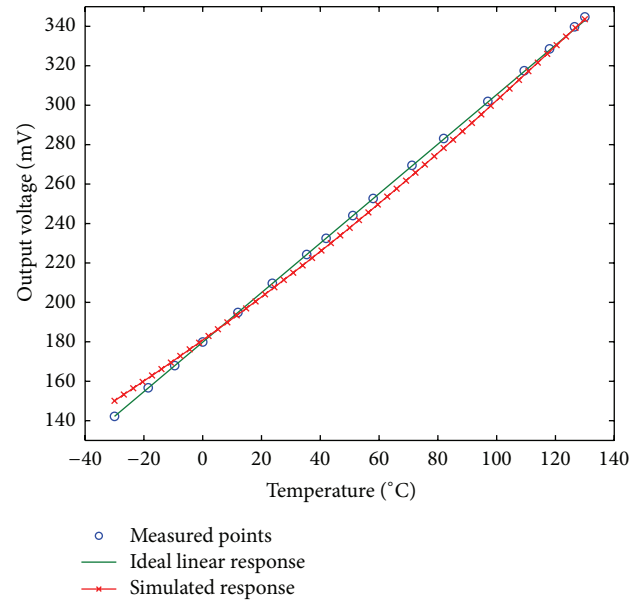

Figure 10: Measured and simulated response of fabricated temperature sensor.

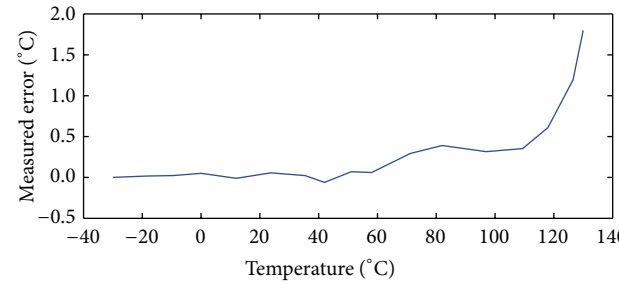

Figure 11: Temperature error between the measured sensor output and an ideal linear response within a −30 to 130°C temperature range.

8.2. Carbon Nanotube Gas Sensor. Carbon nanotubes (CNTs) present a high surface-to-volume ratio which makes them very suitable for gas sensing applications [54]. Its main advantage over conventional gas sensors, based on semiconducting metal oxides (MOX), is its low energy consumption. In addition, CNT based gas sensors are very sensitive and can be decorated by nanoparticles sensitive to the gases of interest, achieving an improved performance on gas sensing.

There are basically two different configurations for carbon nanotube sensors: field effect transistors and chemiresistors. Field effect transistors based on single-wall carbon nanotubes are very sensitive but need a complex fabrication process [55]. Chemiresistive CNT sensors do not needs a so complex fabrication process and can be made in two different ways [56]:

(i) Thin films of mixed metallic and semiconducting CNTs deposited between two electrodes.

(ii) Microsensor formed by a small quantity of CNTs connecting two electrodes separated by few micrometers.

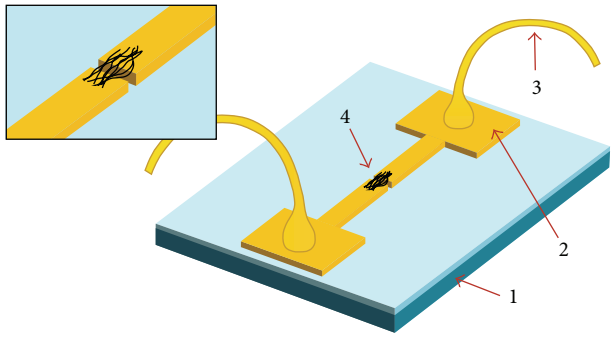

Figure 12: Schematic drawing of the CNT gas microsensor. Oxidized silicon substrates (1), gold patterned electrodes (2), wire bonding connections (3), and the gap with DEP deposited carbon nanotubes (4) compose the device. The inset shows a closer view of the CNTs deposited between the gold electrodes [22].

Thin film sensors are usually simpler to build when compared with micro-sensors. Common manufacturing approaches are chemical deposition and jet printing [57, 58]. In spite of its simplicity, thin film CNT sensors get easily contaminated by gases or other substances. That contamination changes the sensor response and usually requires a special treatment to be removed.

On the other hand, CNT microsensors are fabricated by micromanufacturing techniques, which are clearly more complex than chemical deposition or jet printing but are less sensitive to contamination since the contaminants can be evaporated from the surface of carbon nanotubes by a pulse of current. Additionally, the reduced size of these microsensors, allied with their high sensitivity due to strong self-heating by Joule effect [56], makes them very attractive to be used in microreactors. A schematic drawing of the CNT gas microsensor is depicted on Figure 12.

A previous microreactor containing one CNT microsensor inside has already been fabricated following the same directions explained, but without any embedded electronics, being all measurements made from outside [22, 59].

8.3. Multiplexer. Following the previous explained guidelines, a five-input sensor multiplexer was conceived as shown in Figure 13. Primary selection is made by 3 : 8 digital MUX commanded by the digital tags core (lines $s0$ to $s2$). The four first addresses correspond to four external CNT sensors (Sens_0 to Sens_3) and the last address corresponds to the internal temperature sensor (not shown). The selection of an external sensor connects its left side to ground by the corresponding switch ($M0$ to $M3$) and its right side to the output (V_{out}) through the corresponding analog transmission gate (SW0 to SW3).

All external sensors have two biasing lines, v_read and v_clear, controlled by read_sens and clear_sens inputs. The v_read line is intended to reading operations, so it brings a small current to the selected carbon nanotube sensor through the corresponding biasing resistor ($Rr0$ to $Rr3$) forming a simple voltage divider proportional to sensor response. The v_clear line is intended to clear the selected sensor by mean of a short duration current pulse (about of 10 μA during few microseconds). For that, appropriated values of resistance should be used for $Rc0$ to $Rc3$ resistors. Since the exact resistance value of each CNT microsensor is not well determined (depending on the amount and characteristics of deposited nanotubes), both Rr and Rc resistors are placed externally to the chip.

8.4. Signal Conditioning Circuit. The CNT gas microsensors designed for this system are planned to present a gas free resistance between 80 kΩ and 100 kΩ. Previous experiments indicate a resistance variation between −0.001% and +20% under gas exposure [59]. If a 4 μA biasing current is applied to the sensor, the minimum resistance variation will correspond to a 2.347 μV variation on the sensor signal. Such small voltage signal requires a 108 dB gain stage in order to fit in a 600 mV input rage ADC, so a signal amplification stage is mandatory for this specific application.

To achieve the desired gain keeping a minimal interference on the signal, an instrumentation amplifier (IA) is required. Very low power implementations have been reported with capacitively-coupled topologies [39, 40] which make them attractive for passive RFID sensing. However, due to the need for a high linearity device with a programmable gain, a traditional resistive feedback IA has been chosen. Moreover, the short distance between tag and reader ensures enough power to feed this device. The proposed signal conditioning circuit is represented in Figure 14.

The gain adjustment, needed to adequate the voltage range of different CNT microsensors, is defined by a 4-bit word (Gain) which controls the programmable gain amplifier (PGA). The zero adjust is obtained by an 8-bit capacitive DAC connected to the positive IA input and controlled by ZeroAdj digital input. Both Gain and ZeroAdj words are informed by the digital core of the tag. The power consumption of the complete signal conditioning circuit designed in 180 nm CMOS technology, with a 1.2 V supply voltage, achieves about of 9 μW in simulation.

8.5. Analog-to-Digital Converter. As demonstrated in Section 7, the charge redistribution SAR ADC is a very suitable solution for passive RFID sensing. For this reason, an 8-bit capacitive SAR ADC was chosen for this application. Its DAC working principle is based on the charge sharing between binary weighted capacitors, using only CMOS controlled switches as depicted in Figure 15. Its conversion sequence can be resumed in 10 steps as follows:

(i) ϕ_1: switch S_1 is turned to V_{in} and switches b_0 to b_7 are turned to S_1 node connecting all lower capacitance plates to V_{in} potential. At the same time, switches S_{2a} and S_{2b} are closed discharging any residual voltage on the nodes V_x and V_{OUT} and setting V_{OUT} to zero.

(ii) ϕ_2: switches S_{2a} and S_{2b} are opened and switch S_1 is turned to V_{REF-} setting the voltage on the upper capacitance plates to $V_{REF-} - V_{in}$.

(iii) ϕ_3: switch S_7 is turned to V_{REF+} setting and V_x node to $(V_{REF+} - V_{REF-})/2 - V_{in}$. Since the Cs capacitor

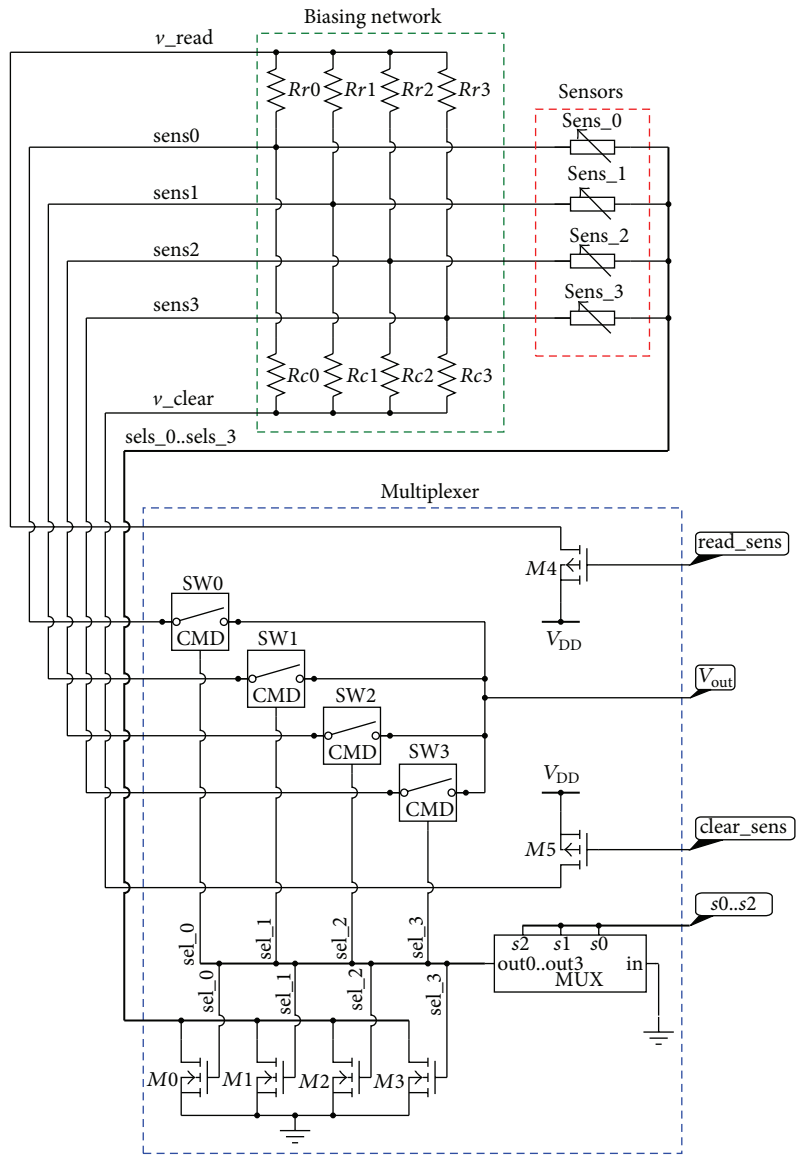

FIGURE 13: Schematic diagram of CNT sensors connected to a biasing network and multiplexing circuitry.

was discharged during ϕ_1 phase, this same potential will appear on V_{OUT}. At this point, the voltage signal on V_{OUT} node will indicate the value of b_7 output. A negative voltage means that the sampled voltage (V_{in}) is less than half the reference voltage, resulting as $b_7 = 0$ or $b_7 = 1$ otherwise. If the resulting bit was zero, the SAR controller should turn the S_7 switch back to V_{REF-}.

(iv) ϕ_4 to ϕ_{10}: the testing sequence described in previous step should be repeated for switches S_6 down to S_0. At the end of last step, all output bits ($b_0, \ldots, b_7$) will be known, completing the analog-to-digital conversion.

The successive approximation register in charge of all control signals was implemented by a finite state machine fully customized to save power. Moreover, once the conversion finishes the SAR cuts off its feeding clock to avoid unnecessary power consumption with gate switching.

With the view to improve the converter accuracy without increase the energy demand, a low power and low offset time domain comparator (TDC) [60] was used. The layout of all DAC capacitors and TDC main components were made according to common centroid techniques.

The ADC was fabricated in IBM 180 nm CMOS process. A chip photograph is shown in Figure 16. The total chip occupies 2.0 × 1.5 mm^2 and the ADC core area is 275 × 145 μm^2, including a Daisy Chain testing structure.

Static tests were performed in order to measure the differential non-linearity (DNL) and the integral nonlinearity (INL) which gives +0.98/−0.59 and +1.03/−3.30 LSB, respectively. High values are due a parasitic-nonlinear capacitances

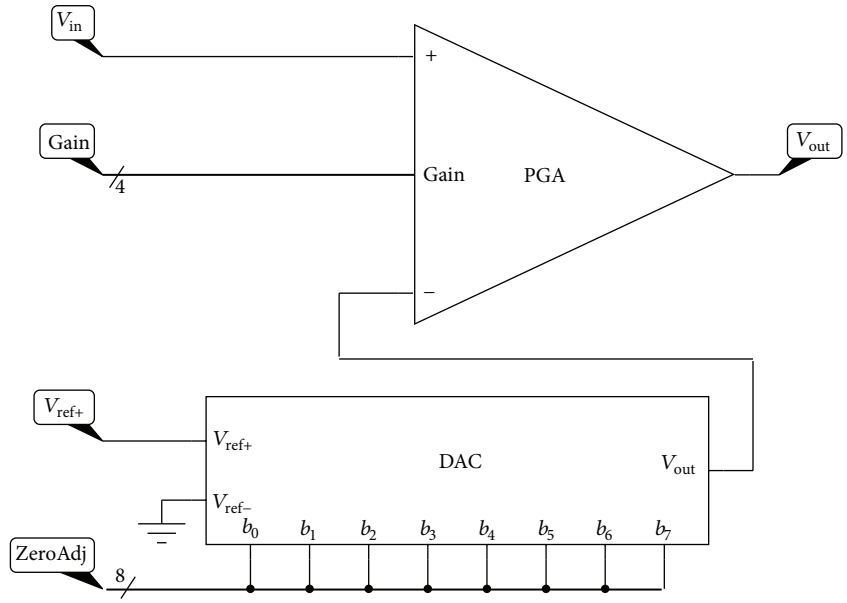

Figure 14: Proposed signal conditioning circuit.

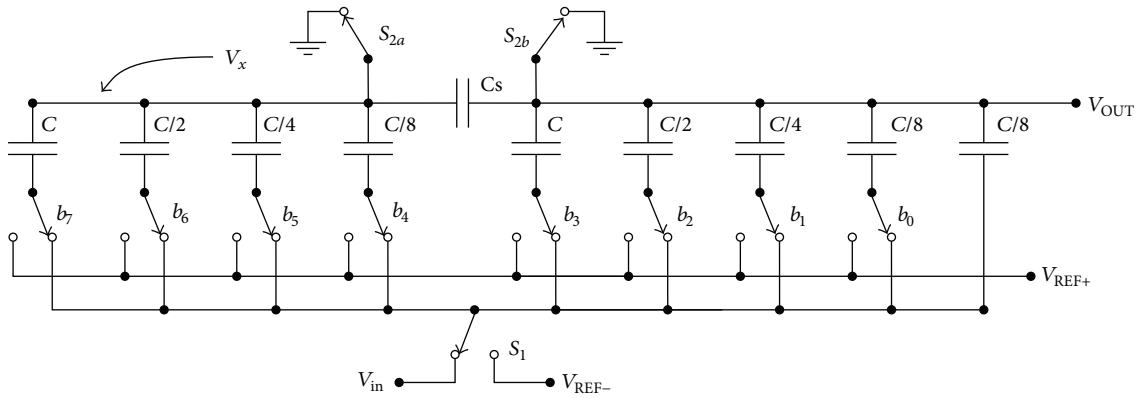

Figure 15: Capacitive DAC adopted for A/D converter.

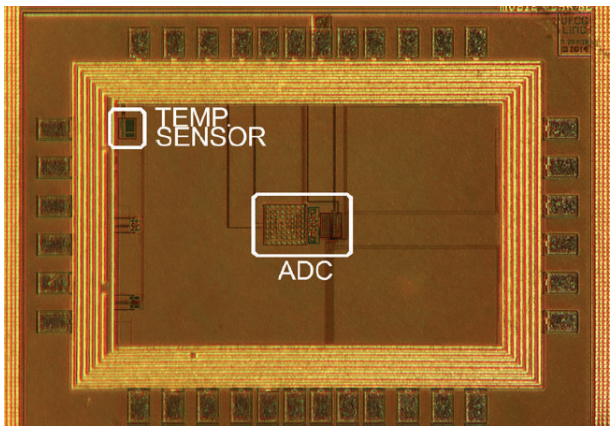

Figure 16: Micrograph of chip containing the proposed low power charge redistribution SAR ADC (at center) and the low power temperature sensor (at left).

which were underestimated during the design stage. The measured DNL and INL are presented in Figure 17.

The FFT spectrum was measured using 65536 points with 0 dB normalized sinusoid inputs at 2.92 kHz and 44.8 kHz as shown in Figures 18 and 19. The measured SNDR is 40.01 dB and the SFDR is 42.77 dB. Results indicate ENOB equals 6.35 bits. The total power consumption with 1 V of supply voltage is 6.01 μW at 100 kS/s which corresponds to a figure of merit (FoM) equals to 538 fJ/Conversion-step. Preliminary refined measurements indicate that about of 85% of whole consumption is only in successive approximation register (SAR) unit which is slightly greater than expected.

8.6. Overall Results. The overall simulated and measured results for power consumption and time delay are summarized in Table 3. The time delay of whole system is much lower than the maximum allowed by ISO 15693 and ISO 14443

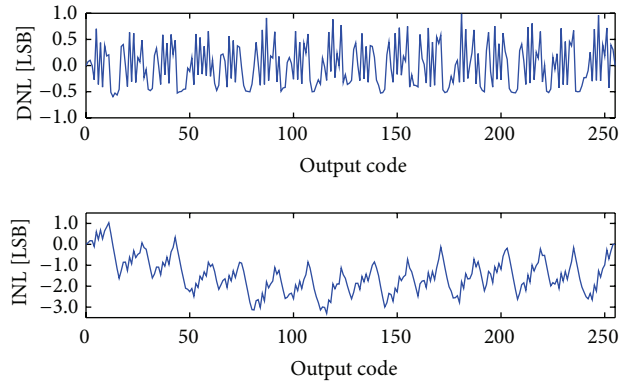

Figure 17: Measured DNL and INL error of fabricated ADC.

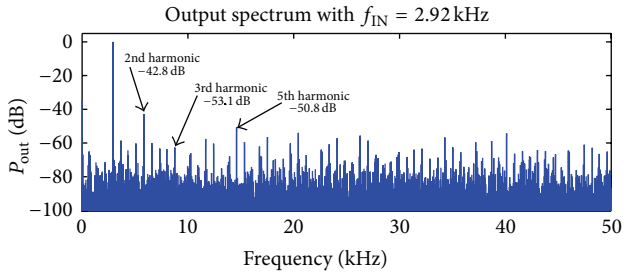

Figure 18: Output spectrum of designed ADC for an input frequency of 2.92 kHz.

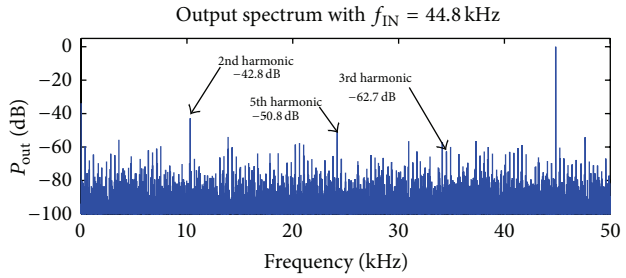

Figure 19: Output spectrum of designed ADC for an input frequency of 44.8 kHz.

standards, as discussed on Section 4. Although the analog-to-digital converters consume more energy than expected, its power consumption is still within the limits previously discussed. Moreover, the total power consumption is still compatible with a NFC system for a 10 to 14 cm distance range, according to the simulation results of Section 7.

Since the proposed system is a sensor interface for passive HF RFID tags, it could be integrated to a standard tag circuit as a single chip solution or connected with a RFID interface chip, like the NF-4 from EM Microelectronic [30], with the help of a simple glue logic circuit.

9. Conclusion

The general considerations to design a sensor interface for passive RFID tags was discussed. The power and timing constraints concerning HF tags was presented and a generic multisensor interface was proposed. A survey analysis on analog to digital converters was made over more than 300 reported converters. Analysis shows that, over the last eight years, the successive approximation register A/D based on capacitive DAC is the most appropriated solution achieving the best results in technology nodes below 350 nm. A specific sensor interface for carbon nanotube gas sensors was proposed. Simulation and measured results indicate that the designed system is more than ten times faster than the maximum time acceptable by the corresponding standard, leaving a wide time margin for core processing or system adjusts. Finally, the overall estimated and measured power consumption are compatible with the target application, which should be capable of operating at few centimeters from the reader antenna as intended.

Table 3: Power and time consumption of sensor and sensor interface according to simulation and testing results.

Device	Power consumption	Time delay
MUX	0.20 μW	1.0 μs
Signal conditioning circuit	9.00 μW	7.0 μs
ADC	6.10 μW	12.0 μs
CNT sensor	4.80 μW	10.0 μs
Temperature sensor	0.11 μW	—
Overall results	**20.21** μW	**30.0** μs

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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