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Research Article

Two Novel Quantum-Dot Cellular Automata Full Adders

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Quantum-dot cellular automata (QCA) is an efficient technology to create computing devices. QCA is a suitable candidate for the next generation of digital systems. Full adders are the main member of computational systems because other operations can be implemented by adders. In this paper, two QCA full adders are introduced. The first one is implemented in one layer, and the second one is implemented in three layers. Five-input majority gate is used in both of them. These full adders are better than pervious designs in terms of area, delay, and complexity.

1. Introduction

Quantum-dot cellular automata (QCA) is a new nanotechnology that can help us to reach low-power consumption, high device density, and high clock frequency. QCA size is smaller than CMOS it can, even be implemented in molecule or atom size. QCA power consumption is extremely lower than CMOS because there are not any current in the circuit and output capacity. The two important gates in QCA are three-input majority gate and inverter. In this paper, two novel QCA full adders are introduced in which the first one is implemented in one layer and the second one is implemented in three layers. They have five-input majority gate in their structure.

The rest of the paper is as follows. Section 2 describes QCA. Section 3 describes five-input majority gates. Two new full adders are presented in Section 4. Finally, Section 5 concludes the paper.

2. Quantum-Dot Cellular Automata (QCA)

Quantum-dot cellular automata (QCA), first proposed in 1993 by Lent et al. [1], is a structure made up of identical cells realized through a variety of technologies such as electrodynamic, ferromagnetic, and molecular [2].

A QCA cell a square shape, with four quantum dots in which just two electrons can stand at it. The electrons perch diagonally in the square for getting the farthest position from each other because of coulombic repulsive force. When the two electrons are positioned as in Figure 1(a), the polarization is (+1), and if they are positioned as in Figure 1(b), the polarization is (−1).

A QCA wire can be built by placing a row of cells as shown in Figure 2 when the first cell's polarization is +1, the other's polarization becomes +1, and when the input cell's polarization is −1, the other cell's polarization has the same value.

The most important gates in QCA are inverters and three-input majority gates. The inverter is shown in Figure 3(a), when the input cell has a value, the output cell become reversed. A three-input majority gate is made of three inputs, one device cell and one output as shown in Figure 3(b). If most of inputs have polarization +1, the device cell becomes +1. If most of inputs have polarization −1, the device cell becomes −1. The output cell's polarization follows the device cell's polarization.

AND gates and OR gates can be implemented by three-input majority gate. If one of the inputs be +1, then the three-input majority gate is like an OR gate (1). If one of the inputs be −1, then the three-input majority gate is like an AND gate (2):

$$\mathrm{Maj}(A, B, 1) = A + B, \tag{1}$$

$$\mathrm{Maj}(A, B, 0) = A \cdot B. \tag{2}$$

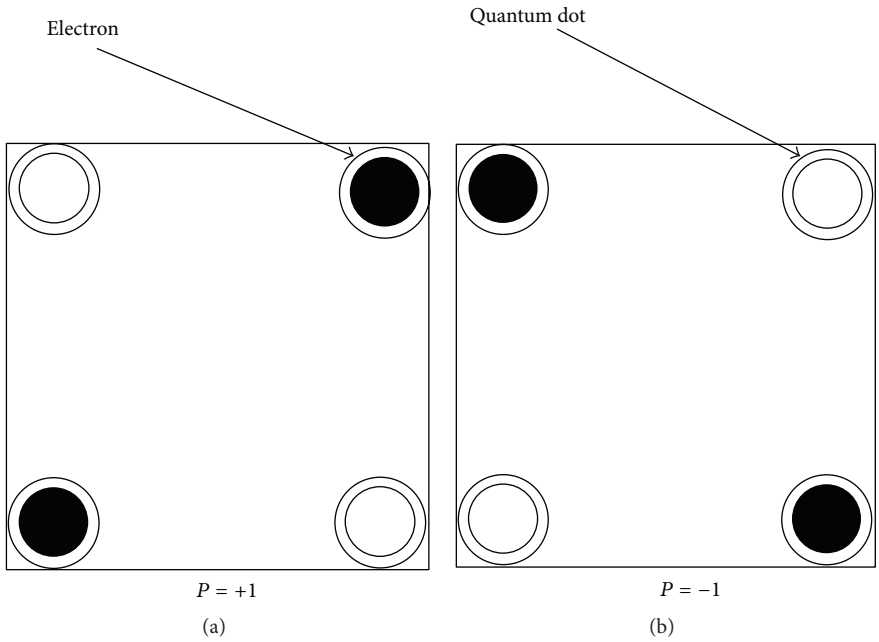

Figure 1: The polarization of cells.

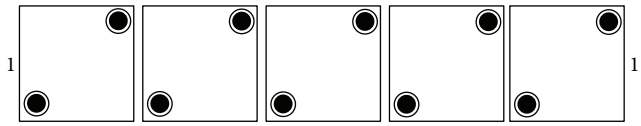

Figure 2: A QCA wire.

A QCA clocking zone is a group of QCA cells which is controlled by the same QCA clock. In QCA, four clocking zones are considered. The schematic of a QCA wire constructed using four clocking zones is shown in Figure 4(a). There is a 90° phase delay from one clocking zone to the next one as shown in Figure 4(b) [6].

3. Five-Input Majority Gates

For reaching our goal, we need another gate and it is called five-input majority gates.

There are many five-input majority gates which were proposed from 2007 until now. As shown in Figure 5, Azghadi et al. [3], Navi et al. [4, 5], Akeela and Wagh [2], and Hashemi et al. [6] introduced some five-input majority gates. These five-input majority gates have some advantages and disadvantages.

We examined and found that the five-input majority gate, which was proposed in [2], is the best choice for our full adder, because it has ordinary cells, the inputs and outputs are not surrounded by the other cells, and they can be accessed easily. This design is suitable to implement larger QCA circuits, so we choose it for our full adder.

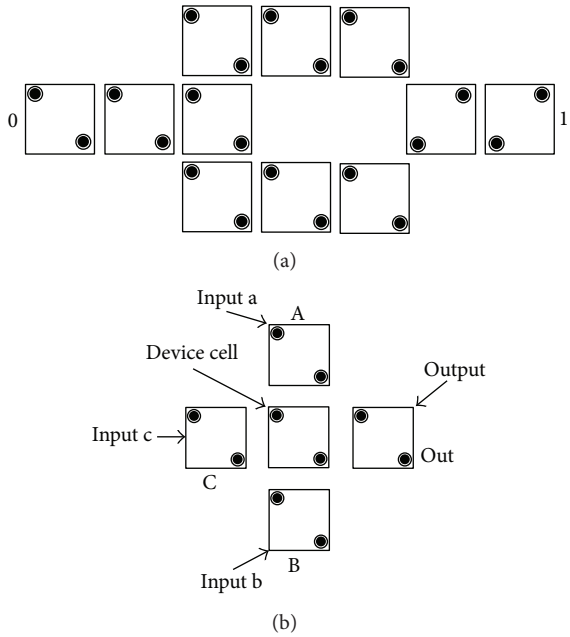

Figure 3: (a) A QCA inverter. (b) A QCA majority gate.

4. Two Novel QCA Full Adders

Many QCA full adders have been introduced until now. The first one is presented by Tougaw and Lent in 1994 [7]. As it is shown in Figure 6, it has five three-input majority gates and three inverters. This full adder uses QCA coplanar wire crossing scheme [6]. It is implemented in one layer, and it has 192 cells. In this design, QCA clocking concepts are not

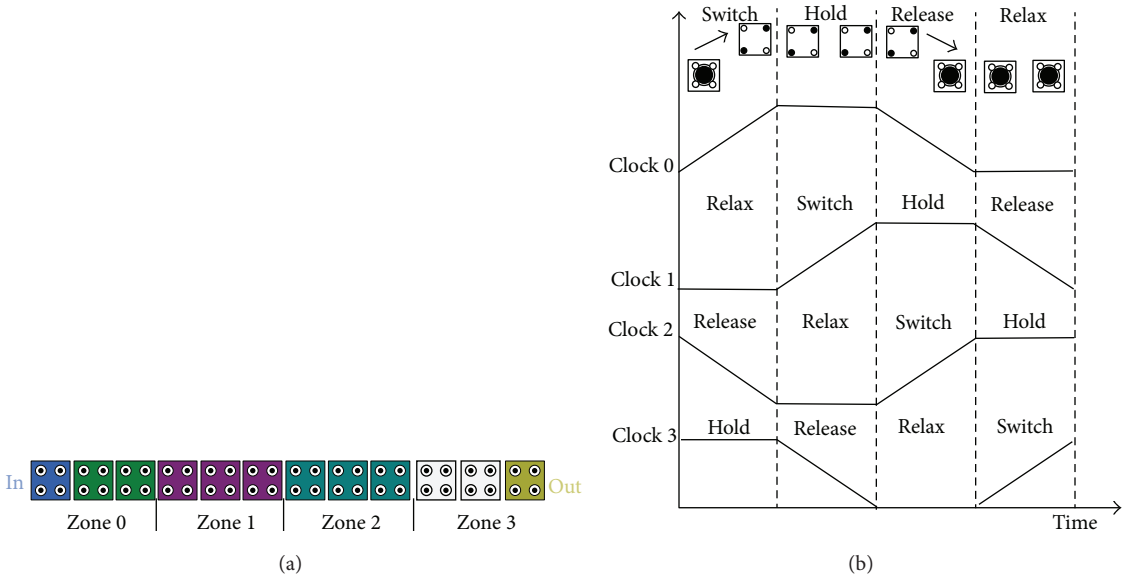

FIGURE 4: (a) A QCA wire with four clocking zones, (b) QCA clocks wave forms.

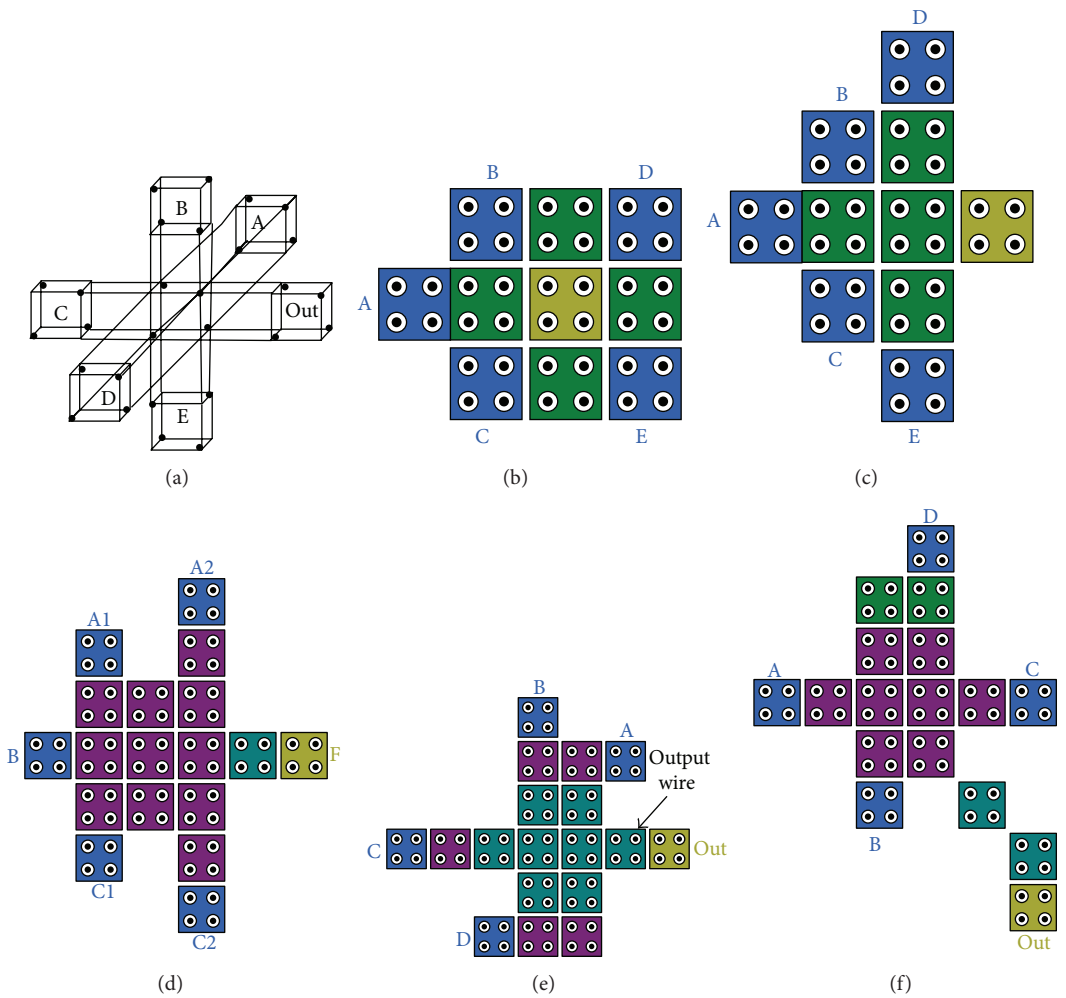

FIGURE 5: The proposed five-input majority gates in the literature ((a) [3], (b) [4], (c) [5], (d) [2], (e) [6], (f) [6]).

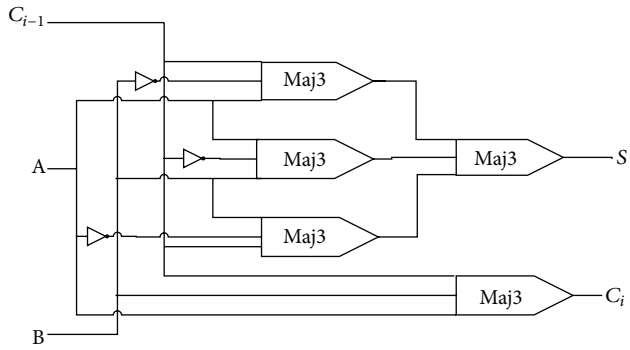

Figure 6: One-bit QCA full adder schematic [7].

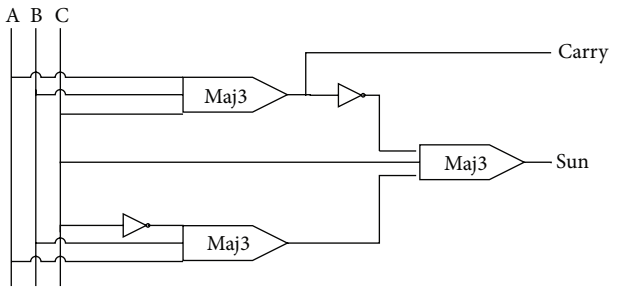

Figure 7: One-bit QCA full adder schematic [8].

considered [6]. Another QCA full adders using some logical structures is introduced by Vetteth et al. in 2002 [9], but the QCA clocking concepts are considered at it. For generating the output, it takes 3/5 clock cycles. Another QCA full adder is introduced by Wang et al. in 2003 [8], which is made of three three-input majority gates and two inverters. It takes 1/25 clock cycles to produce outputs. The schematic of this full adder is shown in Figure 7.

There are some QCA full adders that are implemented in three layers by Cho [10], Cho and Swartzlander [11, 12], Hänninen and Takala [13], Kim et al. [14], Zhang et al. [15], Navi et al. [4, 5], Sayedsalehi et al. [16], and Hashemi et al. [6].

In this paper, we proposed two QCA full adders in which the first one is implemented in one layer and the second one is implemented in three layers. In these designs, at first the carry value is calculated by a three-input majority gate (3), and then the carry value is inverted and is used as the two inputs of the five-input majority gate. The output of the five-input majority gate generates the some value:

$$\text{Carry} = \text{Maj3}\,(\text{A0}, \text{B0}, \text{C0})\,, \tag{3}$$

$$\text{Sum} = \text{Maj5}\left(\text{A0}, \text{B0}, \text{C0}, \text{Carry}', \text{Carry}'\right). \tag{4}$$

In this paper, two full adders were simulated by QCA designer software (version 2.0.3) [17]. The coherence vector computational engine was used in all simulations, and the important parameters are cell size = 18 nm × 18 nm, dot diameter = 5 nm, and radius of effect = 40 nm.

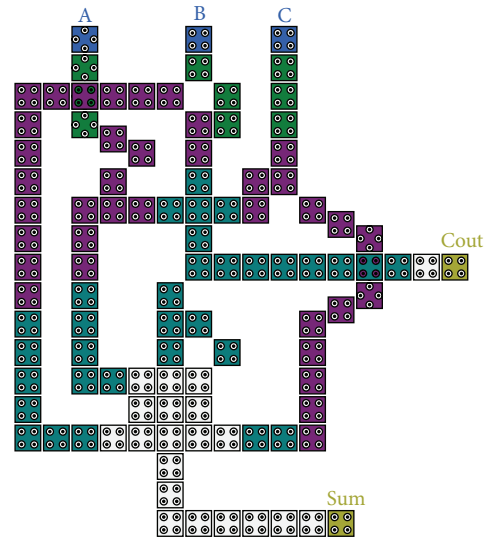

Figure 8: The first QCA full adder (it is implemented in one layer).

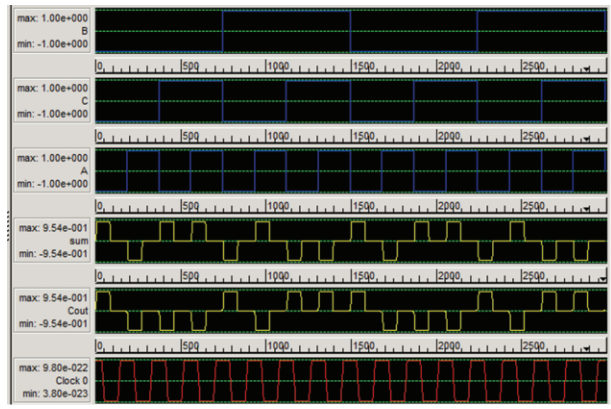

Figure 9: The simulation results of the first QCA full adder.

The first full adder uses QCA coplanar wire crossing scheme. As shown in Figure 8, this full adder takes one clock cycles to generate output. It has 104 QCA cells, and its area is 0.13 μm^2. The simulation result has been shown in Figure 9.

The second full adder is implemented in three layers. This full adder takes 0.75 clock cycles to generate output as shown in Figure 10. It has 63 QCA cells and its area is 0.05 μm^2. In this full adder like the previous full adder, the inputs and outputs are not surrounded by the other cells and they can be accessed easily; the sum value and the carry out value come out from the same side, and they are suitable to implement larger QCA circuits. The simulation result has been shown in Figure 11.

Table 1 compares our designs and the best previous designs. The first full adder is better than the previous designs which were implemented in one layer in terms of area, delay, and complexity. Also, the second one is better than the previous designs which were implemented in three layers in terms of delay and complexity.

Table 1: The comparison between our proposed designs and the best previous designs.

QCA full adders	Layer's number	Complexity (cells)	Area (μm^2)	Latency (clk cycle)
Coplanar QCA FA [8]	1	145	0.17	1.25
Proposed QCA FA in Figure 8	1	104	0.13	1
Multilayer QCA FA [6]	3	79	0.05	1.25
Proposed QCA FA in Figure 10	3	63	0.05	0.75

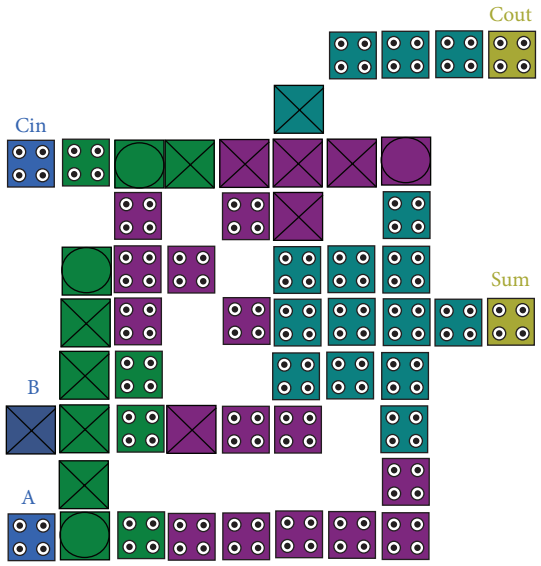

Figure 10: The second QCA full adder (it is implemented in three layers).

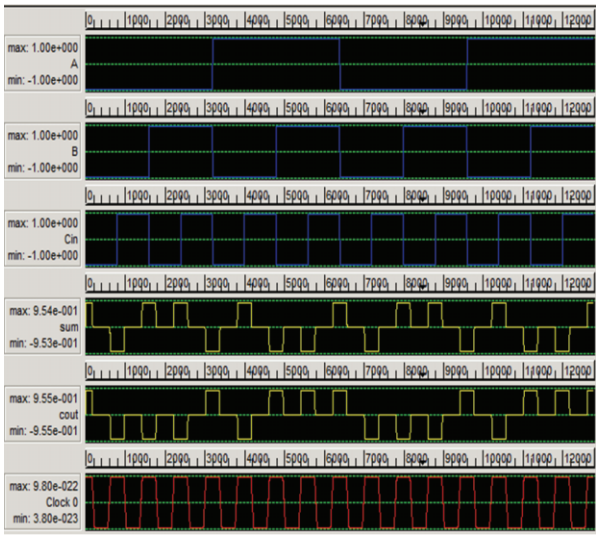

Figure 11: The simulation results of the second QCA full adder.

5. Conclusions

As mentioned earlier, low power consumption, high device density, and high clock frequency are the goal of QCA technology.

In this paper, two novel QCA full adders were proposed in which the first one is implemented in one layer and the second one is implemented in three layers. They have ordinary cells, and the inputs and outputs are not surrounded by the other cells and they can be accessed easily. The sum value and the carry out value come out from the same side and they are suitable to implement larger QCA circuits. The first full adder is better than the previous designs in terms of area, delay, and complexity. The second full adder is better than the previous designs in terms of delay and complexity but its area and the best previous designs area are equal.

Conflict of Interests

None of the authors have a direct financial relation with the commercial identity mentioned in the paper that might lead to a conflict of interests for the authors.

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