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Research Article

SiGe HBTs Optimization for Wireless Power Amplifier Applications

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This paper deals with SiGe HBTs optimization for power amplifier applications dedicated to wireless communications. In this work, we investigate the f_T-BV_{CEO} tradeoff by various collector optimization schemes such as epilayer thickness and dopant concentration, and SIC and CAP characteristics. Furthermore, a new trapezoidal base Germanium (Ge) profile is proposed. Thanks to this profile, precise control of Ge content at the metallurgical emitter-base junction is obtained. Gain stability is obtained for a wide range of temperatures through tuning the emitter-base junction Ge percent. Finally, a comprehensive investigation of Ge introduction into the collector (backside Ge profile) is conducted in order to improve the f_T values at high injection levels.

1. Introduction

SiGe heterojunction bipolar transistors (HBTs) integrated into BiCMOS technologies have been providing cost-effective solutions to many of the building blocks of RF and microwave transceivers. Power amplifiers have remained an exception to this trend for some time, but SiGe HBTs have emerged as competitive alternatives to III-V devices for RF power applications in wireless handsets and cell phones [1]. State-of-the-art SiGe/Si HBTs dedicated to power amplifier application present a f_T of 27 GHz with a BV_{CEO} of 8.5 V [2].

However, for similar breakdown voltages, the achieved Johnson's limit using SiGe power HBTs and their power-handling capability per unit emitter area are not comparable with III-V power devices since the minority carrier mobility and the bandgap are lower in Si compared with III-V counterparts [3].

To enhance SiGe HBTs performance in this field while maintaining its very competitive cost, further breakthrough in device design and optimization are mandatory.

In this paper, we focused on three main SiGe HBTs features improvements: device robustness, temperature behavior and HF characteristics.

The paper is organized as follows. First, process flow, RF power device structure and electrical device characteristics are illustrated. Results of static and dynamic performances are presented. Next, different optimization processes are described. These optimizations deal with collector tuning, Ge base profile engineering and Ge introduction into the collector layer. Finally, their impacts on the electrical characteristics are highlighted.

2. Device Structure Design and Fabrication Process

2.1. Process Flow Description. This study has been carried out on the 250 nm SiGe HBT architecture shown in Figure 1, which consists in a double polysilicon quasi-self-aligned structure. Basically, the process starts with a buried sub-collector layer and subsequently grown epitaxial collector layer, followed by deep trench isolation and sinker formation. The nonselective SiGe base epitaxy and oxide/poly stack are deposited. Oxide/poly stack is patterned and etched. Next, a polybase/oxide stack is deposited. In this stack, an emitter window is then patterned and etched, stopping on

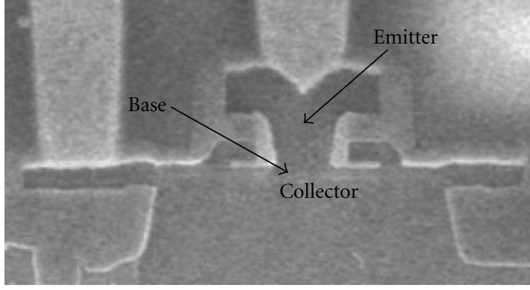

Figure 1: 0.25 μm SiGe HBT architecture SEM cross-section.

the oxide/poly stack. Selective collector implant is realized and then D-shape inside spacers are fabricated. Afterwards, the pedestal oxide is wet etched and arsenic in-situ doped poly-Si is deposited to form the emitter. After poly-emitter patterning, flash activation anneal, silicidation and contact formation completed the fabrication sequence. Trapezoidal Ge profile use for the SiGe:C base is presented on Figure 2.

The power SiGe HBT cell is presented on Figure 3. It consists in 8 emitter fingers, with drawn dimensions of $1.6 * 13.4\,\mu\text{m}^2$ for each finger. The values of ballasting resistors are carefully selected to warrant thermally stable device operation at high power levels.

2.2. Electrical Characterization of Fabricated Devices. Fabricated devices have ideal static characteristics down to very low V_{BE} (Figure 4). The current gain is 170. Peak f_T/f_{MAX} values are 26/38 GHz (Figure 5). Measured breakdown voltages are 6.45 and 19.25 for BV_{CEO} and BV_{CBO}, respectively.

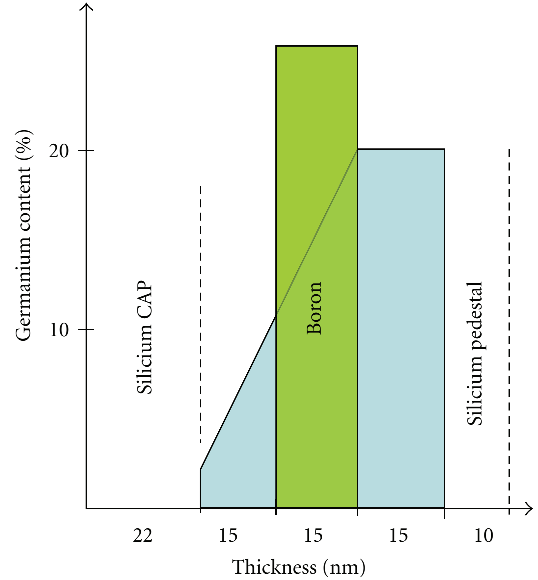

Figure 2: Trapezoidal Ge base profile.

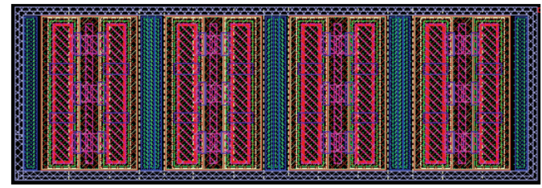

Figure 3: Power SiGe HBT cell.

3. DC/RF Performance Optimizations

3.1. Collector Tuning. In order to achieve high breakdown voltages (BV_{CBO} and BV_{CEO}) required for power amplification applications, epitaxial collector layer characteristics (thickness and doping concentration) have been optimized as well as dose and energy of the SIC implant.

The epitaxial collector layer thickness has been varied. Figure 6 shows BV_{CBO} improvement (from 16 to 23 V) with epitaxial collector layer thickness increase from 0.8 to 1.4 μm. BV_{CEO} is also improved from 6.5 to 11.2 V. However, due to the transit time rise associated with the increase of epitaxial collector layer thickness, the dynamic device response is reduced. In this case, maximum f_T value decreases from 26 to 15 GHz (Figure 6). Regarding BV_{CEO} optimization, variations on epitaxial collector layer doping concentration between $1 \cdot 10^{15}$ and $1 \cdot 10^{16}$ at/cm^3 have been realized. Decreasing epitaxial collector layer doping concentration, BV_{CEO} has been improved from 6.45 to 7.23 V. This results are obtained at constant $f_T * BV_{CEO}$ product.

BV_{CEO} enhancement also relies on SIC characteristics. Electrical results obtained for different SIC characteristics are presented in Table 1.

Standard implantation consists in phosphorus $2 \cdot 10^{12}$ cm^{-2}, 400 keV. Variations consist in dose as well as energy implant. Through energy implant increase and

Table 1: BV_{CEO} and maximum f_T value obtained for different SIC characteristics.

SIC dose implant (cm^{-2})	2.10^{12}	1.10^{12}	1.10^{12}
SIC energy implant (keV)	400	400	500
BV_{CEO} (V)	7.23	7.92	8.03
$f_{T\,max}$ (GHz) @ $V_{CE} = 1.5$ V	25.31	20.53	19.53

dose reduction, higher BV_{CEO} values are obtained, but always with a constant $f_T * BV_{CEO}$ product. In order to overpass this constant product, another way for optimization has been looked for. CAP thickness has been increased. The CAP thickness layer control the minority charge in the emitter. The latter impacts directly the emitter transit time as well as the Gummel number and so the current gain. Current gain reduction implies a BV_{CEO} increase. Moreover, the CAP thickness has an impact on the base-emitter space charge region that modifies the pinched base resistance. As a consequence CAP thickness increase reduces the current gain that enhances the breakdown voltage, reduces the emitter transit time that increases the transit frequency f_T. These results are summarized in Table 2. By that way, the $f_T * BV_{CEO}$ product is improved from 178 to 216 GHz $*$ V.

3.2. Ge Base Profile Engineering. It has been shown that current gain decrease at elevated temperatures in SiGe:C HBTs has become an issue [4]. Gain characteristic versus

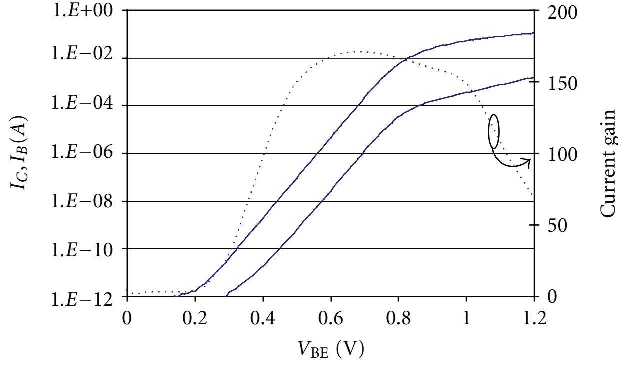

Figure 4: Static characteristics of power SiGe HBT cell.

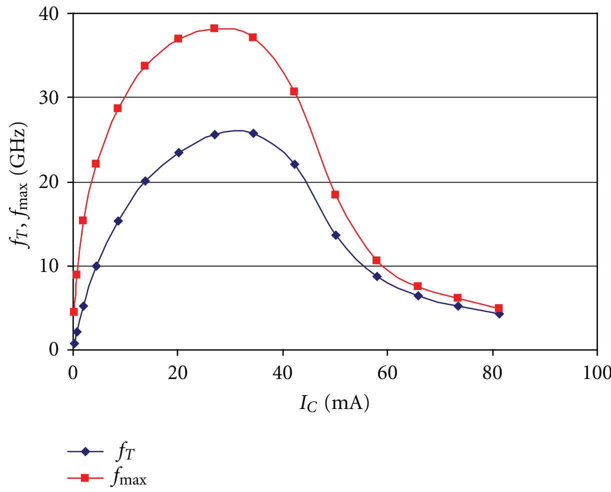

Figure 5: Dynamic characteristics of power SiGe HBT cell.

Table 2: Principal device parameters for different CAP thicknesses.

CAP thickness (nm)	16	22	33
Gain	224	208	176
BV_{CEO} (V)	6,56	6,59	6,90
Pinched base resistance (kΩ/□)	1,65	1,51	1,45
$f_{T\,max}$ (GHz) $V_{CE} = 1.5$ V	27,20	30,32	31,34
$f_{T\,max} * BV_{CEO}$ (GHz∗V)	178.44	199.90	216.18

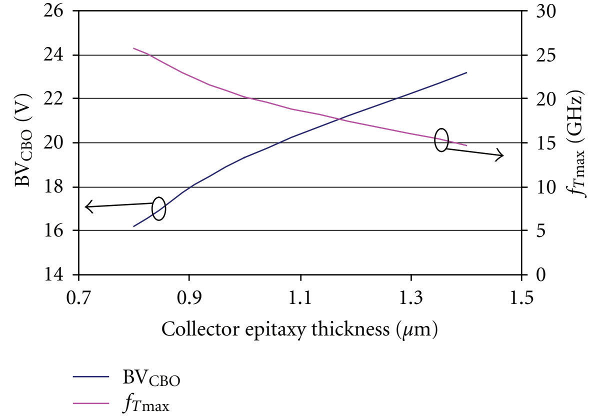

Figure 6: BV_{CBO} and $f_{T\,max}$ variations with epitaxial collector thickness.

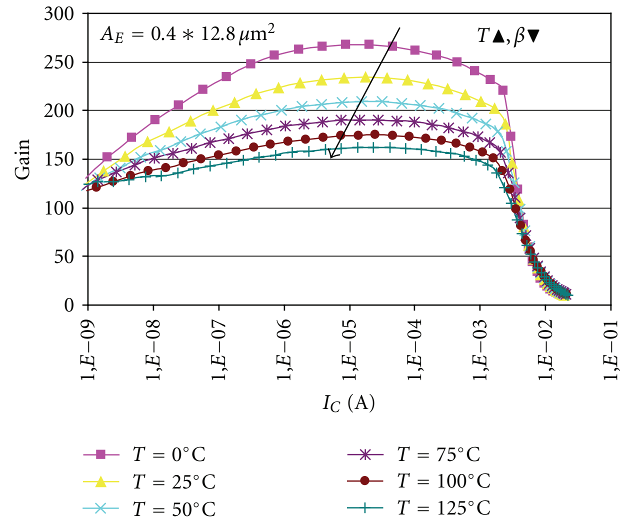

Figure 7: Gain characteristics versus temperature for standard Ge base profile.

temperature obtained for standard germanium base profile device has been plotted in Figure 7.

Strong variation of maximum gain value with temperature is observed. Analyzing the current gain equation given below, we see that the temperature-dependence of β can be minimized when the term in the exponential function is close to zero. ΔE_G represents the bandgap narrowing in the base due to the presence of germanium content and ΔE_g represents the bandgap narrowing due to high doping effects. Temperature stability can be obtained when $\Delta E_G \approx \Delta E_g$.

$$\beta = \frac{I_C}{I_B} = \gamma \frac{D_n}{D_p} \frac{W_E}{W_B} \frac{N_{DE}}{N_{AB}} \exp\left(\frac{\Delta E_G - \Delta E_g}{kT}\right). \quad (1)$$

For this purpose, devices having special germanium profiles in the base with different Ge content at the base-emitter junction have been fabricated (see Figure 8). All along the Ge base profile, constant carbon dose is present. The main advantage of these Ge profiles is a precise control of base-emitter Ge content associated with beneficial Ge grading effect. Base-emitter Ge content has been varied from 3 to 6%. For the 3% Ge profile device, which results in best gain stability, device current gain versus temperature has been plotted in Figure 9. Over a wide range of temperature, (from −25°C to 125°C), the current gain is constant close to 100. Specific efforts have been made to improve the maximum current gain value. Reducing base boron concentration by 15%, gain of 110 with unchanged temperature stability is obtained.

Input impedance (Z_{in}) of the device for different temperature has been monitored. Connecting a vector network analyzer with couplers at the input of an automated tuner

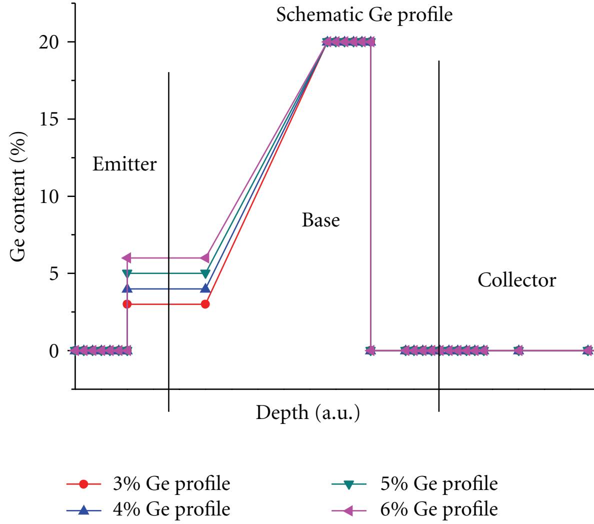

FIGURE 8: Special Ge base profile with different base-emitter junction Ge content.

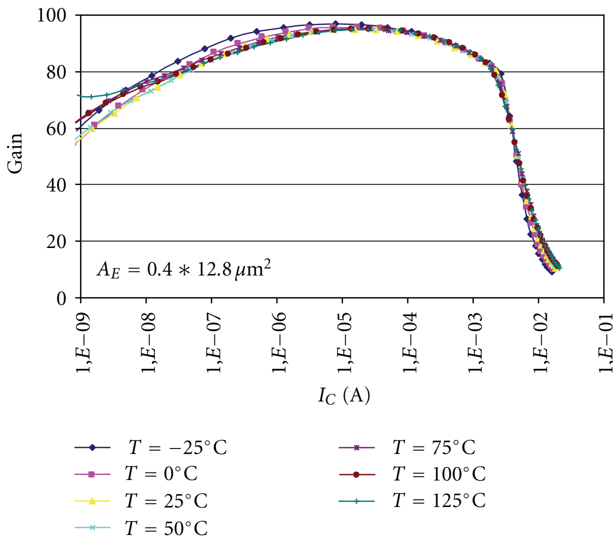

FIGURE 9: Current gain versus temperature for 3% Ge profile device.

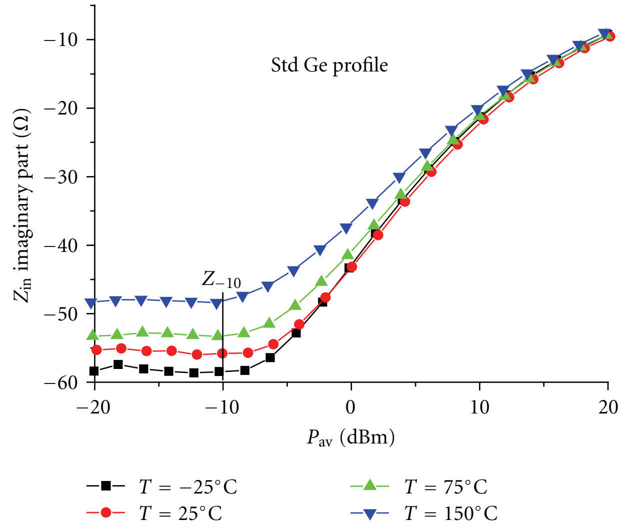

FIGURE 10: Imaginary part of Z_{in} versus input power as a function of temperature for standard Ge profile.

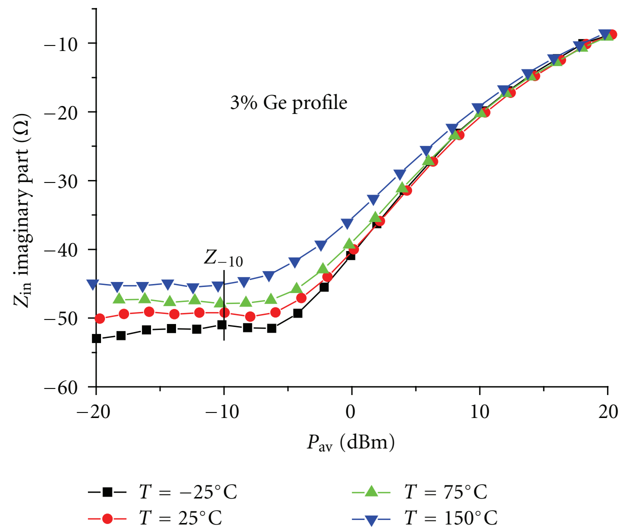

FIGURE 11: Imaginary part of Z_{in} versus input power as a function of temperature for 3% Ge profile.

system allows the device under test input impedance to be accurately measured during load and source pull tests. This impedance was characterized for an operating point of $V_{CE} = 3.6$ V and $I_C = 30$ mA. An operation frequency of 900 MHz was used for load-pull comparison. Knowing Z_{in} temperature-dependence, input and interstage-matching circuits design is facilitated.

The imaginary part of Z_{in} versus input power as a function of temperature for standard and 3% Ge profile has been plotted on Figures 10 and 11. At −10 dBm input power, input impedance variation with temperature for 3% Ge profile is 12% compared to 18% for standard Ge profile. For low power level, lower temperature-dependence with optimal 3% Ge profile is obtained. This fact is highlighted by Figure 12, which shows the imaginary part variation

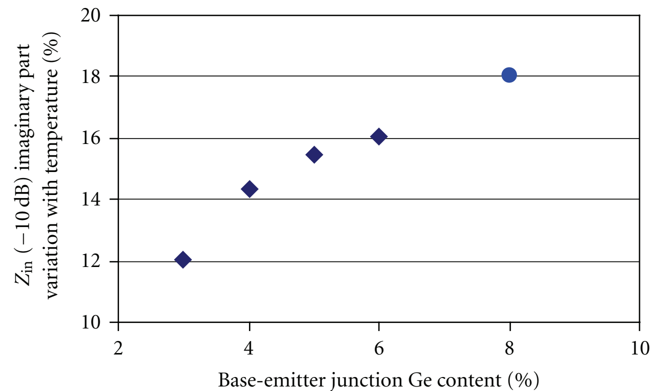

FIGURE 12: Imaginary part variation of the input impedance with temperature for a −10 dBm input power.

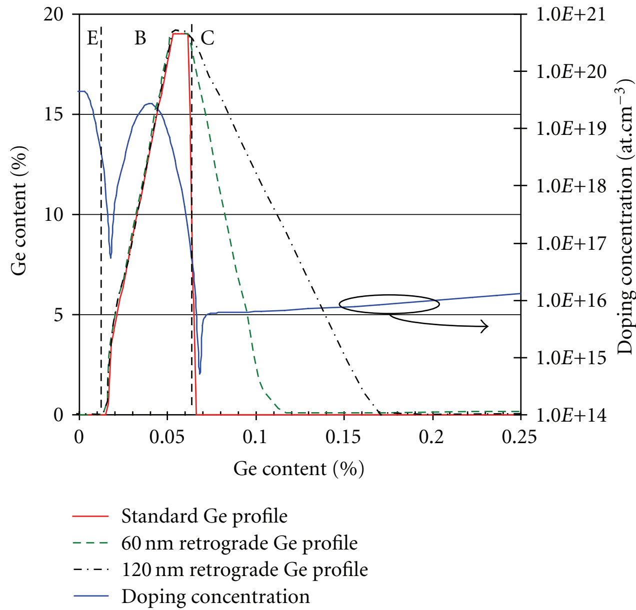

Figure 13: Simulated Ge profiles.

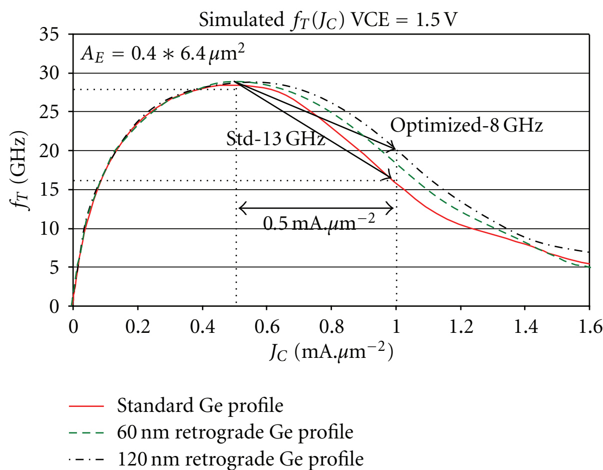

Figure 14: Simulated f_T versus J_C characteristics.

of the input impedance with temperature for a −10 dBm input power. A temperature-dependence reduction with emitter-base junction Ge percent decrease is clearly observed. Thereby, circuit mismatch linked to input impedance variation with temperature is reduced.

3.3. Investigation of Retrograde Ge Profile in the Collector. Physical simulations for HBTs with three different Ge profiles have been performed. Figure 13 shows the standard Ge profile together with two additional Ge profile shapes that extend deep into the collector (60 and 120 nm retrograde Ge profile) (see [5–7]). The simulated structure is in agreement with the HBT topology presented in Figure 1. Figure 14 represents simulated f_T versus J_C characteristics. For the device featuring the 120 nm retrograde Ge profile, f_T drops

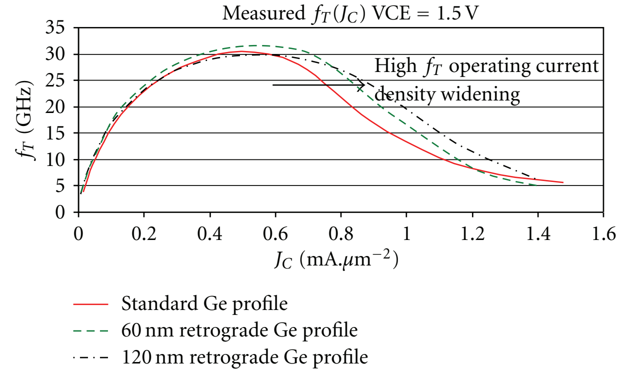

Figure 15: Measured f_T versus J_C characteristics.

only by a value of 8 GHz as J_C increases from 0.5 to 1 mA$\cdot\mu$m^{-2}as opposed to a drop of 13 GHz in the case of the standard Ge profile. The high current range showing an improved f_T is clearly widened. This studied confirms the work done by Liang et al. [7].

The three above-described Ge-profile design structures were fabricated in the same wafer lot under identical processing conditions. Figure 15 presents the comparison between the measured f_T versus J_C characteristics. f_T maximum value close to 32 GHz is obtained for 60nm retrograde Ge profile. As the Ge retrograde profile extends wider into the collector, the device shows a higher f_T in the high current density range.

4. Conclusion

In this work, f_T-BV$_{CEO}$ behavior for various collector optimization schemes such as epilayer thickness and dopant concentration, SIC and CAP characteristics has been demonstrated. Furthermore, based on a mature 250 nm technology, an optimized SiGe:C base profile has been fabricated with a special carefully designed Ge profile dedicated to current gain stability for a wide temperature. The associated input impedance temperature-dependence reduction has also been highlighted. That way circuit design is facilitated. Finally, device simulation pointed out the improvement of high injection operation and f_T performance through the Ge retrograde profile in the collector, which has been confirmed by measurements. The devices with optimized profile exhibit improved f_T maximum value and wider f_T operating current density range, suitable for PA applications.

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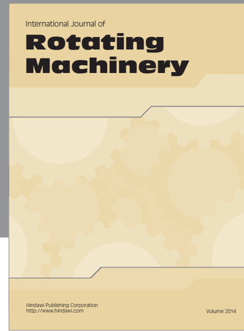
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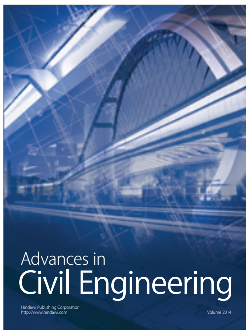
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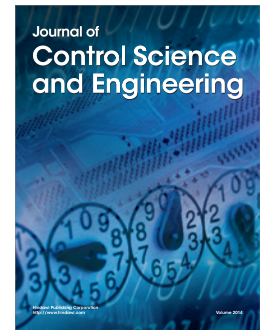
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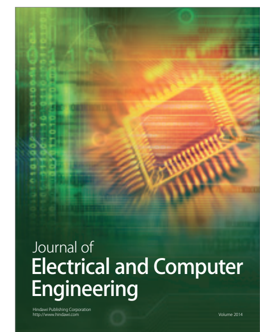
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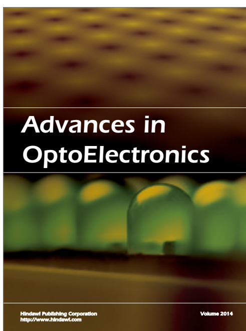
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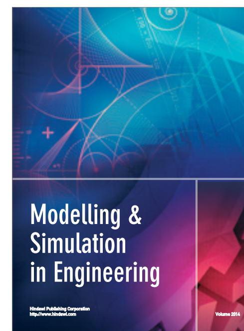
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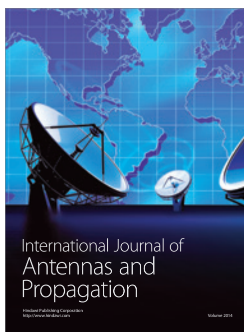
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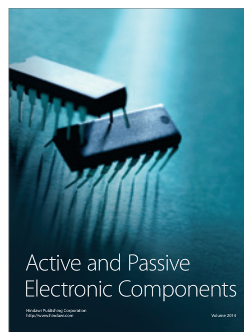
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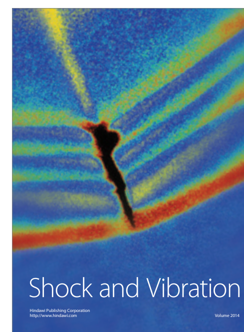
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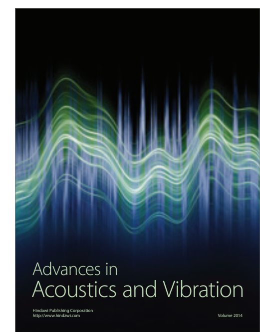
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