Hindawi Publishing Corporation
Journal of Electrical and Computer Engineering
Volume 2013, Article ID 145314, 9 pages
http://dx.doi.org/10.1155/2013/145314

Research Article

Divide-by-Three Injection-Locked Frequency Dividers with Direct Forcing Signal

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Received 9 April 2013; Accepted 14 June 2013

Academic Editor: Jose Silva-Martinez

Divide-by-three frequency dividers with direct forcing signal are analyzed, and the actual locking mechanism underlying their operation is highlighted. In particular, it is shown that the locking mechanism cannot be explained with the mixing between signals, as commonly made in the literature. An analytical procedure based on the averaging method is developed for solving the equation describing such dividers, and the first approximation to the oscillation in the locked states is predicted. The amplitude and phase of the output voltage in steady state as well as the locking range are derived in terms of the circuit parameters, obtaining useful design guidelines. The derived results are shown to be very close to SPICE simulations for a 0.13 um RF-CMOS process.

1. Introduction

Frequency dividers are key building blocks of RF integrated circuits, as they allow us to scale down the high frequency of the signal from the voltage controlled oscillator (VCO) to a relatively low frequency required for the phase locking in a Phase-Locked Loop (PLL). As an alternative to the widely used digital dividers, based on Current-Mode Logic (CML) flip flops [1], and to Miller dividers [2], some topologies of *LC*-CMOS analog dividers have been devised that allow higher operation frequencies with lower power consumption. These dividers are called Injection-Locked Frequency Dividers (ILFDs) as they rely on the well-known phenomenon of subharmonic synchronization (or injection-locking) that happens in a basic differential *LC* oscillator perturbed by an external periodic signal [3].

In applications, ILFDs with division ratios greater than two are often needed to reduce the overall power consumption and the chip area that the cascade of dividers with a low division ratio involves. Therefore, frequency dividers, able to divide by 3, 4, and more, were recently designed which, in addition, feature a wide locking range (*LR*) needed in practical PLLs. Moreover, the division by an odd number, and in particular for three, can be a particularly advantageous solution in some designs, as in multiband frequency synthesizers [4, 5]. In particular, the use of a divide-by-three ILFD enables a simple architecture for dual-band operation, when the ratio between the frequencies is three, as it happens for W and K bands [6]. For this reason, designing low-voltage divide-by-three ILFDs with a wide locking range has become a topic of relevant interest [7–9].

To perform the divide-by-three function, a variety of designs suitable for operation at high frequencies have been proposed, which include particular circuit arrangements aimed mainly at widening the lock range. They are basically made by a differential *LC* oscillator and an injection circuit providing a current signal that perturbs the oscillator. In divide-by-three ILFDs with direct forcing of the injection signal, the current signal is injected directly in the oscillator across the *LC*-tank and the locking takes place according to a mechanism different from the mixing between signals [10], usually invoked to explain the process of frequency division [11–13]. The purpose of this work is to complete the investigation in [10] with the aim to provide useful results for the design of these dividers. Using the behavioral model introduced in [10], which consists of a nonlinear differential equation of the second order, and the procedure of solution of that equation, based on the method of averaging, we were able

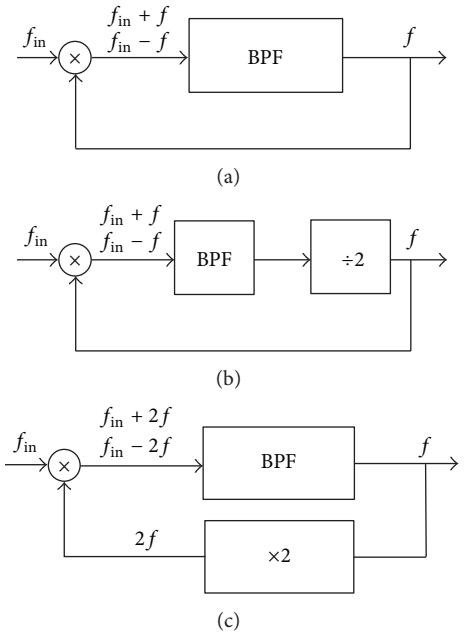

Figure 1: (a) Model of the Miller divide-by-two ILFD [2]. (b) Model of a divide-by-three ILFD based on a divide-by-two ILFD [7]. (c) Model of a divide-by-three ILFD based on a frequency multiplier [8].

to find the amplitude and phase of the output voltage in steady state, and the locking range in explicit form as a function of the relevant circuit parameters. Then, the dependence of the circuit performances on the circuit parameters is investigated. The application of the derived formulas leads to results that are in good agreement with SPICE simulations for a 0.13 um RF-CMOS process. A preliminary review of the preexisting results is also given in order to show how their limitations are overcome by presented results.

2. Principles of Operation of Divide-by-Three Circuits

The first analog frequency divider based on a mixer and a band-pass filter (BPF) was proposed by Miller and its block diagram is shown in Figure 1(a) [2]. It is easy to verify that it can operate as a divide-by-two frequency divider. Upon multiplication of the input and output signals, the mixer generates components at $f_{in} + f$ and $f_{in} - f$, where f is the frequency of the output signal. If the former component is suppressed by the low-pass filter but the latter is not, then $f_{in} - f = f$ and, hence, $f = f_{in}/2$.

The combined effect of a mixing nonlinearity and of a band-pass filter has become the common characteristic of all divide-by-two injection-locked frequency dividers used in practical applications [14, 15]. General models to analyze injection-locked frequency dividers were presented in papers [11, 12], which implicitly assume that the divider operation is based on a mixing effect.

Divide-by-three circuits have been developed starting from the approach used for divide-by-two frequency dividers, even if some modifications were needed in order to obtain a division by a number different from two. The approach in [7] is based on the model in Figure 1(b) and employs a divide-by-two frequency divider in the feedback loop. The mixer generates components at $f_{in} + f$ and $f_{in} - f$. The component $f_{in} + f$ is filtered out by the band-pass filter and the component $f_{in} - f$ is injected into the divide-by-two frequency divider. Thus, the output frequency can be derived as $(f_{in} - f)/2 = f$ and, hence, $f = f_{in}/3$. Consequently, the output frequency is locked at one-third of the input frequency.

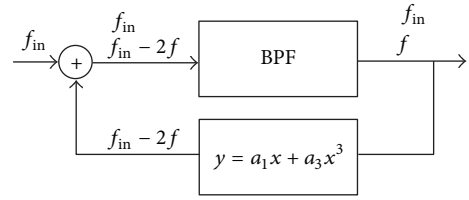

Figure 2: Model of a divide-by-three injection-locked frequency divider with a direct application of the forcing signal.

However, the most widely used approach to realize a divide-by-three frequency divider exploits a circuit nonlinearity to produce a second harmonic of the output voltage, as shown in Figure 1(c) [8]. In this case, the input signal at frequency f_{in} is mixed with the feedback signal at frequency $2f$ to produce harmonic components at frequency $f_{in} \pm 2f$. However, only the desired component at frequency $f_{in} - 2f$ passes through the band-pass filter, while all other harmonic terms are suppressed. Thus, $f_{in} - 2f = f$ leads to $f = f_{in}/3$. Many improvements have been proposed in the literature, mainly aimed at widening the locking range through the use of additional inductors, even if in all the cases an input nonlinearity is present that performs a mixing between the input and the feedback signals.

Here, we show that a divide-by-three circuit can operate according to a different principle of operation, that does not employ a mixing between the input and the output signals, as it happens when a forcing signal is directly applied to the *LC*-tank. In the model in Figure 2, the input signal is added to the feedback signal and passes, even if attenuated, through the band-pass filter. Thus, the output signal has a frequency component at frequency f_{in} in addition to its main component at frequency f. If the feedback nonlinearity is a cubic polynomial, the feedback signal will have a component at frequency $f_{in} - 2f$, which will pass through the filter. Thus, imposing $f_{in} - 2f = f$, it results $f = f_{in}/3$.

Note that the model in Figure 2 can be seen as a particular case of the general model of ILFDs, presented in [11] and shown in Figure 3(a), when the nonlinearities are set equal to $i_{in}(v, v_{in}) = kv_{in}$ and $i_{nl}(v) = a_1 v + a_3 v^3$, and $H(s)$ represents the transfer function of a band-pass filter, usually made of an *LC*-tank. Taking into account that the model in Figure 3(a) is equivalent to the circuit in Figure 3(b), let us simulate this circuit with $i_{in} = kv_{in}$, and $i_{nl}(v) = a_1 v + a_3 v^3$, in order to verify that the proposed model is useful to implement a divide-by-three ILFD. The signal waveforms in Figure 4(a) show that

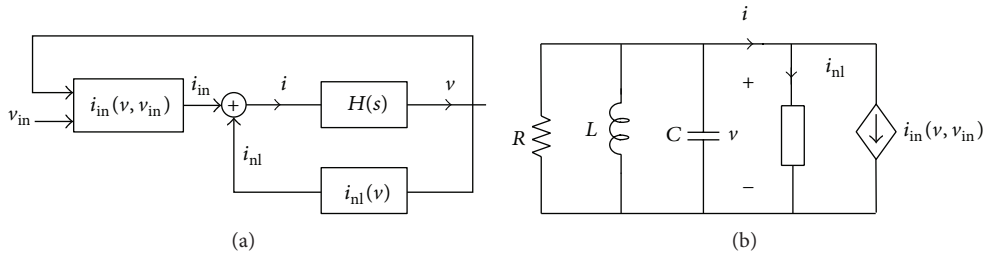

Figure 3: (a) General model of an injection locked frequency divider and (b) its representation as forced LC-tank [11].

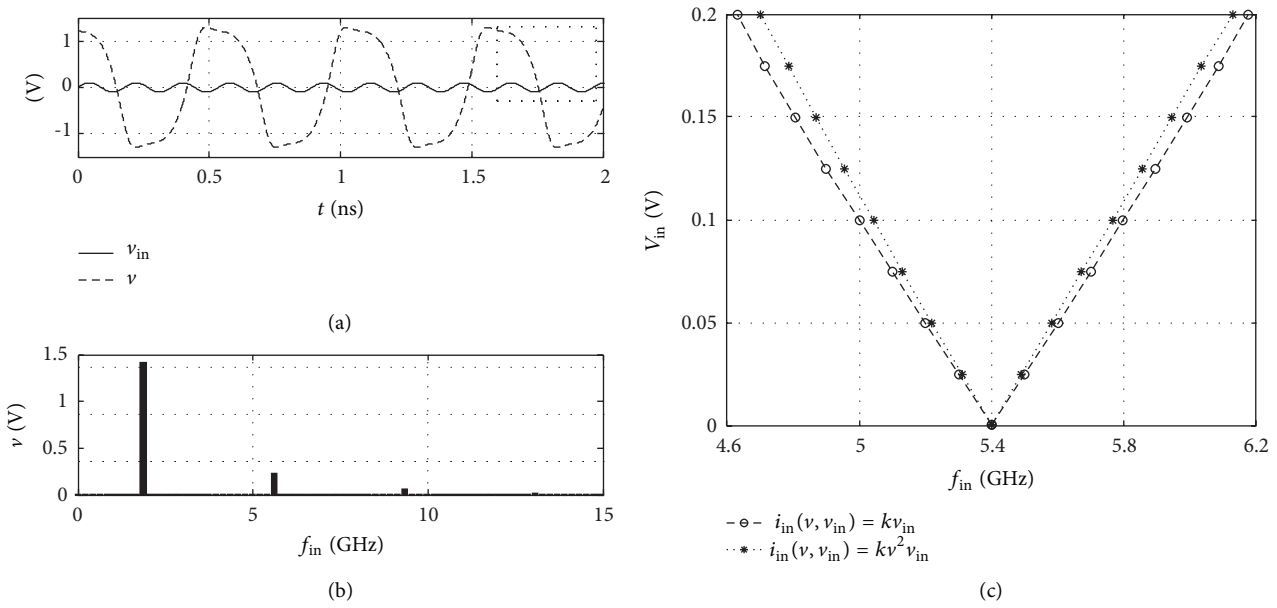

Figure 4: SPICE simulations of the circuit in Figure 3(b) with $i_{nl}(v) = a_1 v + a_3 v^3$, $i_{in}(v, v_{in}) = kv_{in}$, $a_1 = -12\,\text{mA/V}$, $a_3 = 8\,\text{mA/V}^2$, $k = -32\,\text{mA/V}^2$, $L = 10\,\text{nH}$, $R = 905\,\Omega$, $C = 635.45\,\text{fF}$, $V_{in} = 0.1\,\text{V}$, $f_{in} = 5.6\,\text{GHz}$. (a) Time waveforms of the input and output signals. (b) Frequency spectrum of the output signal. (c) Arnold tongues obtained by simulating the circuit in Figure 3(b) with $i_{in}(v, v_{in}) = kv_{in}$ and with $i_{in}(v, v_{in}) = kv^2 v_{in}$.

the output signal, v, has a fundamental component equal to one-third of the input frequency, and, thus, the circuit operates as a divide-by-three ILFD. Its frequency spectrum in Figure 4(b) confirms the presence of a third harmonic in the output signal, that is a component at frequency $f_{in} = 3f$ in addition to its main component at frequency f.

Model in Figure 3(b) gives us also the possibility of easily comparing the case when the injection nonlinearity includes a mixing nonlinearity and the case when a mixing is not present. To this end, we calculated the locking ranges for the divide-by-three mode of operation of the equivalent circuit in Figure 3(b) with $i_{in}(v, v_{in}) = kv_{in}$ (corresponding to the block diagram in Figure 2), and then with $i_{in}(v, v_{in}) = kv^2 v_{in}$ (corresponding to the block diagram in Figure 1(c)). The results reported in Figure 4(c) not only show that both circuits can operate as a divide-by-three ILFD but also using the same value of k, the locking range of the circuit without mixing, that is, $i_{in}(v, v_{in}) = kv_{in}$, is wider than the other one. Thus, we can conclude that dividers can be efficiently realized without performing a mixing between the input and the output signals.

3. Circuit Analysis and Design

The divide-by-three circuit in Figure 5 performs the frequency division without involving a mixing between the input and output signals, but is characterized by the direct application of the forcing signal on the tank of the LC oscillator. The circuit is formed by the parallel connection of an LC-tank, an active circuit consisting of two complementary pairs of cross-coupled devices (Figure 6(a)) and an injection circuit consisting of two complementary MOS switches (Figure 6(b)). Thus, the current i of the LC-tank consists of a component $i_{nl}(v)$ due to the active part and a component i_{in} due to the injection circuit. In general, the current i_{in} depends not only on the synchronization signal v_{in} but also on the voltage v and thus is written in the form $i_{in}(v, v_{in})$.

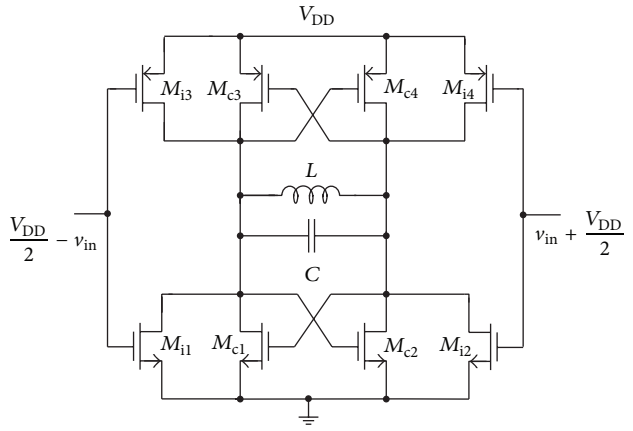

Figure 5: Circuit diagram of a divide-by-three LC-CMOS frequency divider with a direct forcing signal.

Analytical expressions of the functions $i_{nl}(v)$ and $i_{in}(v, v_{in})$ can be determined by assuming that the ILFD operates under a small-injection regime, so that the current $i(v, v_{in}) = i_{nl}(v) + i_{in}(v, v_{in})$ applied to the LC-tank can be written as $i(v, v_{in}) = i(v, 0) + g_1(v)v_{in}$ with $i(v, 0) = i_{nl}(v) + i_{in}(v, 0)$ and $g_1(v) = \partial i/\partial v_{in}|_{v_{in}=0}$. SPICE simulations of the circuits in Figure 6 for $v_{in} = 0$ show that the current $i(v, 0)$ can be well approximated by a cubic polynomial $i(v, 0) = a_1 v + a_3 v^3$ (Figure 7(a)) [16, 17]. On the other hand, the function $g_1(v)$, calculated through a finite difference approximation, can be modeled by a constant function $g_1(v) = k$ (Figure 7(b)). Thus, the current $i(v, v_{in})$ applied to the LC-tank can be written as

$$i\left(v, v_{in}\right) = a_1 v + a_3 v^3 + k v_{in} \tag{1}$$

and the circuit in Figure 5 is amenable to the block diagram in Figure 8, where $H(s)$ is the LC-tank transfer function, and to the equivalent circuit in Figure 3(b). As the block diagram in Figure 8 is reducible to the diagram in Figure 2, we conclude that the circuit in Figure 6 is able to operate as a divide-by-three ILFD.

The main design parameter of a frequency divider is the locking range, which can be analytically related to the circuit parameters as shown below. The circuit in Figure 3(b) is described by

$$\frac{d^2 v}{dt^2} + \frac{1}{RC}\frac{dv}{dt} + \omega_0^2 v = -\frac{1}{C}\frac{d}{dt} i\left(v, v_{in}\right), \tag{2}$$

where $\omega_0 = 1/\sqrt{LC}$ is the resonant frequency of the LC-tank. Assuming that the circuit operates as a divide-by-three ILFD under the action of the signal $v_{in} = V_{in}\cos(3\omega t)$, we seek a solution of (2) in the form $v = w + h$ where $w = W\cos(\omega t + \theta)$ is the first harmonic of v and h the sum of the remaining harmonics. Also the current $i(v, v_{in})$ in the LC-tank is decomposed into a component equal to its first harmonic and a component equal to the sum of the remaining harmonics, that is,

$$i\left(v, v_{in}\right) = i_1\left(w + h, v_{in}\right) + i_h\left(w + h, v_{in}\right). \tag{3}$$

Taking into account that the output harmonics of the nonlinearity $i(v, v_{in})$ depend slightly on the harmonics h of the voltage v, that is, $i_h(w + h, v_{in}) \cong i_h(w, v_{in})$, by virtue of (1) we obtain

$$i_h\left(w, v_{in}\right) = kV_{in}\cos\left(3\omega t\right) + \frac{1}{4}a_3 W^3 \cos\left(3\omega t + 3\theta\right). \tag{4}$$

Note that i and v represent the input and the output quantities, respectively, of the band-pass filter in the model in Figure 2, which are decomposed in the fundamental component at frequency $\omega = 2\pi f = 2\pi\left(f_{in} - 2f\right)$ and in the harmonic components. Equation (4) shows that the harmonic component of the input quantity of the filter has frequency $3\omega = 2\pi f_{in}$, as shown in Figure 2.

By virtue of (3), (2) can be rewritten in the form

$$\left(\frac{d^2}{dt^2} + \frac{1}{RC}\frac{d}{dt} + \omega_0^2\right)(w + h) = -\frac{1}{C}\frac{d}{dt} i_1\left(w + h, v_{in}\right) - \frac{1}{C}\frac{d}{dt} i_h\left(w, v_{in}\right) \tag{5}$$

and can be decomposed into the following two equations for the fundamental and higher harmonics

$$\left(\frac{d^2}{dt^2} + \frac{1}{RC}\frac{d}{dt} + \omega_0^2\right) w = -\frac{1}{C}\frac{d}{dt} i_1\left(w + h, v_{in}\right), \tag{6}$$

$$\left(\frac{d^2}{dt^2} + \frac{1}{RC}\frac{d}{dt} + \omega_0^2\right) h = -\frac{1}{C}\frac{d}{dt} i_h\left(w, v_{in}\right). \tag{7}$$

We will first solve (7) for h and, then, exploiting the solution of (7), we will solve (6) for w. Thus, taking into account that the first term in (7) is greater than the second and third one, that is, $9\omega^2 \gg \omega_0^2 \approx \omega^2$, (7) can be reduced to

$$\frac{d}{dt} h = -\frac{1}{C} i_h\left(w, v_{in}\right) \tag{8}$$

and its solution provides the harmonics of the output voltage, that is,

$$h = -\frac{kV_{in}}{3C\omega}\sin\left(3\omega t\right) - \frac{a_3 W^3}{12C\omega}\sin\left(3\omega t + 3\theta\right). \tag{9}$$

Note that, taking into account that $v = w + h$ with $w = W\cos(\omega t + \theta)$, (9) implies that the output voltage contains a component at frequency $\omega = 2\pi f$ and a component at frequency $3\omega = 2\pi f_{in}$, as represented in the block diagram in Figure 2.

By using (9) in (1), the expression of the current applied to the LC-tank is obtained:

$$i\left(w + h, v_{in}\right) = a_1\left(W\cos\left(\omega t\right) - \frac{kV_{in}}{3C\omega}\sin\left(3\omega t\right) - \frac{a_3 W^3}{12C\omega}\sin\left(3\omega t + 3\theta\right)\right)$$

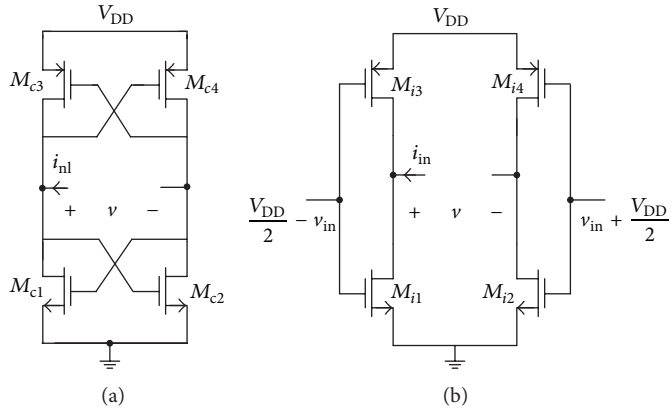

Figure 6: (a) Active part of the ILFD in Figure 5; (b) injection circuit of the ILFD in Figure 5.

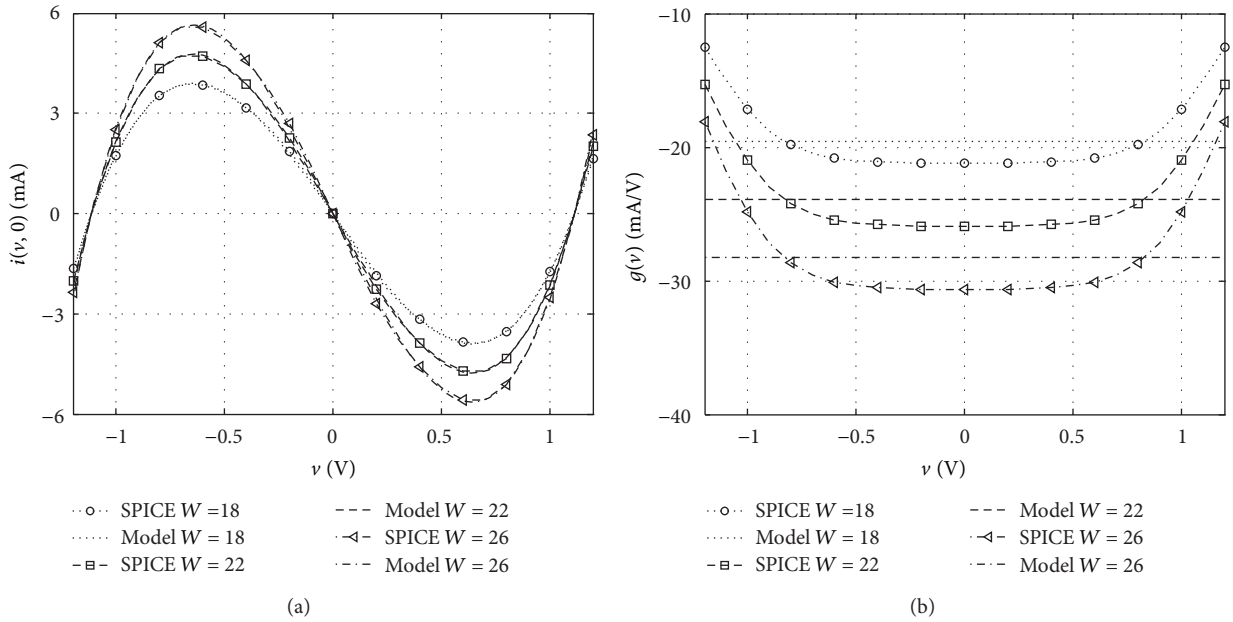

Figure 7: Current-voltage characteristics of the circuits in Figure 6. (a) Total current $i(v, 0) = i_{nl}(v) + i_{in}(v, 0)$ for $v_{in} = 0$. (b) Voltage-controlled transconductance $g_1(v)$. SPICE simulations are obtained by using BSIM3 transistor models (MOSIS-IBM 8RF 0.13 μ technology), with $V_{DD} = 1.2$ V. Analytical models are obtained by using polynomial approximations $i(v, 0) = a_1 v + a_3 v^3$ and $g_1(v) = k$.

$$+ a_3 \left(W \cos(\omega t) - \frac{kV_{in}}{3C\omega} \sin(3\omega t) - \frac{a_3 W^3}{12C\omega} \times \sin(3\omega t + 3\theta) \right)^3 + kV_{in} \cos(3\omega t). \tag{10}$$

Expression (10) allows us to calculate the fundamental harmonic of $i(w + h, v_{in})$, that is $i_1(w + h, v_{in})$, and in particular, the coefficients of cosine and sine Fourier components of the fundamental harmonic, that is,

$$I^c = \frac{1}{\pi} \int_0^{2\pi} i(w + h, v_{in}) \cos(\alpha)\, d\alpha,$$
$$I^s = \frac{1}{\pi} \int_0^{2\pi} i(w + h, v_{in}) \sin(\alpha)\, d\alpha \tag{11}$$

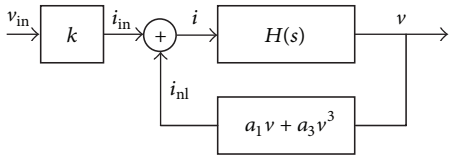

Figure 8: Block diagram of the injection locked frequency divider in Figure 5.

with $\alpha = \omega t + \theta$. It results in that

$$I^c = a_1 W\left(1 + \frac{a_3 k^2 V_{in}^2}{6a_1 C^2\omega^2}\right) + \frac{3}{4}a_3 W^3\left(1 + 2\left(\frac{a_3 W^2}{12C\omega}\right)^2\right) + \frac{a_3 W^2}{4C\omega}kV_{in}\left(\sin(3\theta) + 4\left(\frac{a_3 W^2}{12C\omega}\right)\cos(3\theta)\right),$$
$$I^s = -\frac{a_3^2 W^5}{16C\omega} - \frac{a_3 W^2}{4C\omega}kV_{in}\cos(3\theta). \quad (12)$$

Taking into account that the third harmonic of the output voltage is quite smaller than the fundamental, that is $a_3 W^3/(12C\omega) \ll W$, it is possible to simplify (12), obtaining

$$I^c = a_1 W\left(1 + \frac{a_3 k^2 V_{in}^2}{6a_1 C^2\omega^2}\right) + \frac{3}{4}a_3 W^3 + \frac{a_3 W^2}{4C\omega} \times kV_{in}\sin(3\theta), \quad (13)$$
$$I^s = -\frac{a_3^2 W^5}{16C\omega} - \frac{a_3 W^2}{4C\omega}kV_{in}\cos(3\theta).$$

Once obtained the expression of $i_1(w + h, v_{in})$ in explicit form, or equivalently of I^c and I^s, (6) can be solved by using the averaging method [11, 18] and the following equations for the locked states are obtained:

$$W = -RI^c, \quad \omega = \omega_0 + \frac{1}{2CW}I^s. \quad (14)$$

Equation (13) reduces (14) to

$$W = -RI^c, \quad (15)$$
$$\omega = \omega_{fr} - \omega_0\frac{a_3 WL}{8C}kV_{in}\cos(3\theta), \quad (16)$$

where

$$\omega_{fr} = \omega_0 - \omega_0\frac{a_3^2 W^4 L}{32C}. \quad (17)$$

It is interesting to observe that if $V_{in} = 0$, that is, if the circuit operates as a free-running oscillator, (16) predicts that the output oscillation frequency ω is different from the tank resonant frequency ω_0 and it is equal to ω_{fr}. This is a consequence of the known nonlinear effect of harmonics

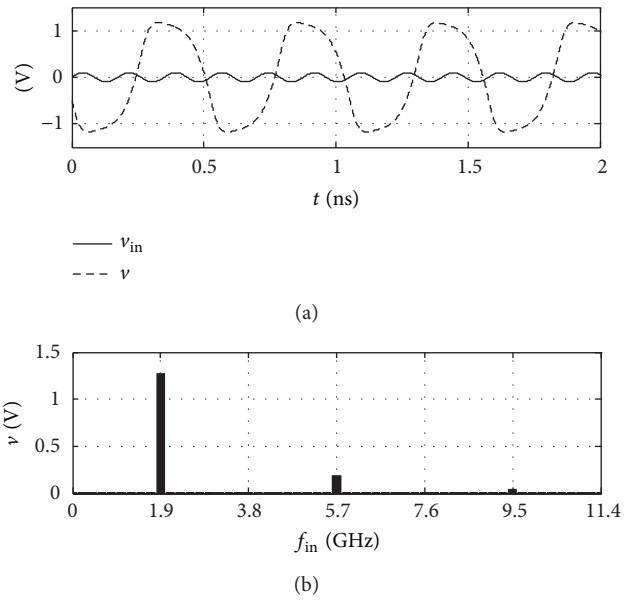

Figure 9: SPICE simulation of the circuit in Figure 5 obtained by using BSIM3 transistor models in MOSIS-IBM 8RF 0.13 μ technology and $W/L_c = W/L_i = 24/0.12, W/L_{PMOS} = 4.5W/L_{NMOS}$, $V_{DD} = 1.2$ V, $L = 10$ nH, $R = 905\,\Omega$. (a) Voltages at the input and output terminals. (b) Frequency spectrum of the output voltage.

on the oscillation frequency [19]. Moreover, (16) highlights an unknown aspect of the frequency entrainment process, namely, that the action of the external signal on the LC oscillator manifests itself by a frequency deviation from the actual frequency of the free-running oscillation. Note also that (17) can be used to estimate the equivalent capacitance C, which includes the device parasitics, starting from the free-running frequency.

Assuming that the frequency shift due to the harmonics does not significantly change in presence of the input signal, that is, assuming ω_{fr} as a constant in (16), we can solve (15) and (16) for W and θ in explicit form, obtaining

$$W = \sqrt{\frac{4(-aR-1)}{3Rc} - \frac{1}{6}\left(\frac{rV_{in}}{C\omega_0}\right)^2 - \frac{rV_{in}}{18C\omega_0}\sqrt{\frac{48(-aR-1)}{Rc} - q}}, \quad (18)$$

$$\theta = \frac{1}{3}\arccos\left(\frac{8C^2\omega_0}{cWrV_{in}}(\omega_{fr} - \omega)\right), \quad (19)$$

with

$$q = 7\left(\frac{rV_{in}}{C\omega_0}\right)^2 + \left(\frac{48C^2\omega_0}{crV_{in}}(\omega_{fr} - \omega)\right)^2. \quad (20)$$

The values of ω for which a solution (W, θ) does exist are the values of ω for which the locking occurs. The minimum

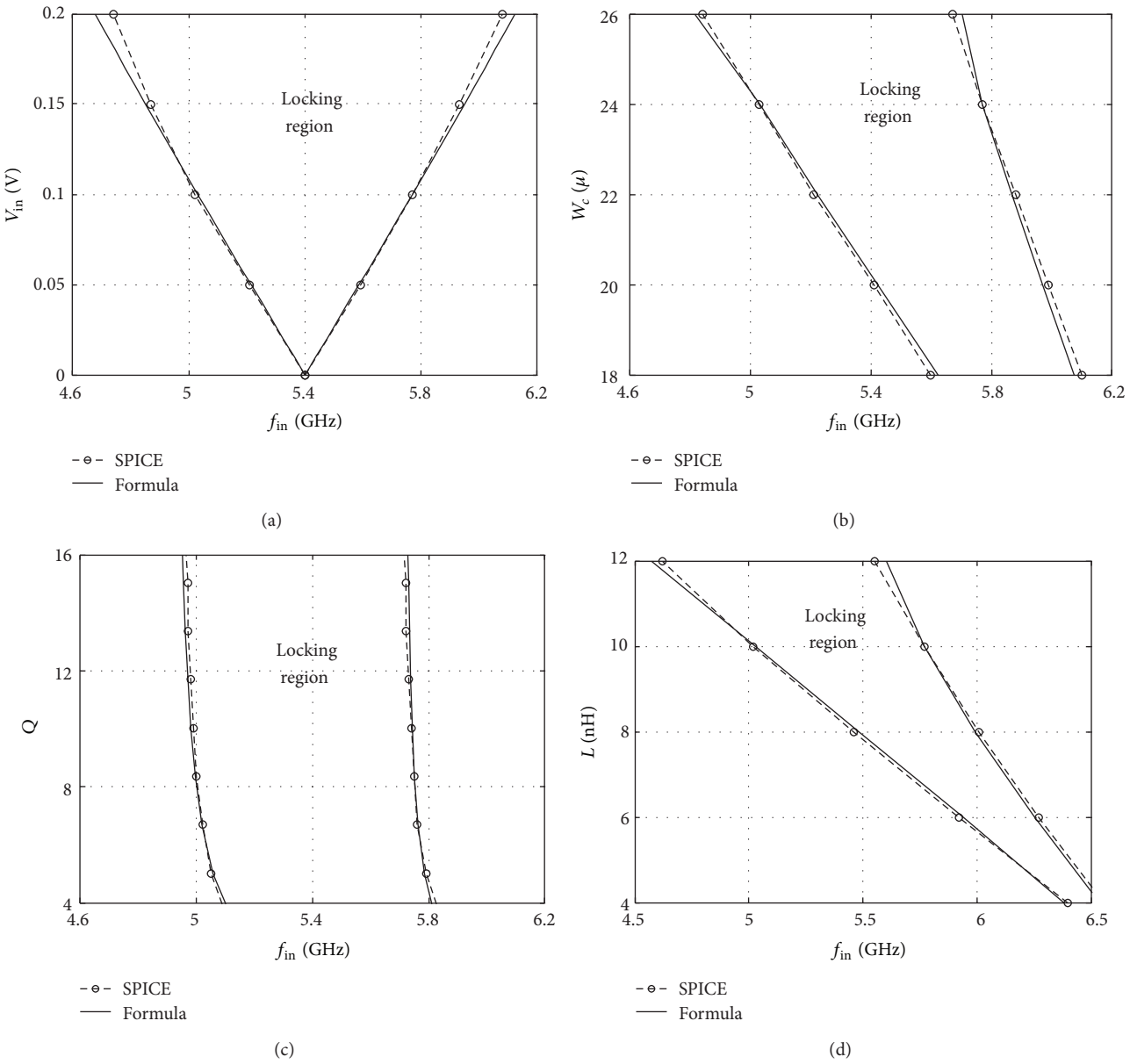

FIGURE 10: Locking regions for the divide-by-three ILFD in Figure 5, obtained by SPICE simulations (lines with circles) and by using analytical equations (lines without circles). For SPICE simulations, BSIM3 transistor models in MOSIS-IBM 8RF 0.13 μ technology with $V_{DD} = 1.2$ V have been used. (a) Locking range as a function of the input amplitude ($L = 10$ nH, $R = 905\,\Omega$). (b) Locking range as a function of the transistor sizes ($W/L_c = W/L_i$, $L = 10$ nH, $R = 905\,\Omega$). (c) Locking range as a function of the tank resistance ($W/L_c = W/L_i = 24/0.12$, $W/L_{PMOS} = 4.5W/L_{NMOS}$). (c) Locking range as a function of the L/C ratio keeping the LC product constant ($LC = 10$ nH 446.6 fF).

and the maximum values of ω define the output-referred locking range and are equal to

$$\omega_{min} = \omega_{fr} - \omega_0 \frac{kV_{in}Lr\sqrt{a_3\left|a_1 + R^{-1}\right|}}{4\sqrt{3}C},$$
$$\omega_{max} = \omega_{fr} + \omega_0 \frac{kV_{in}Lr\sqrt{a_3\left|a_1 + R^{-1}\right|}}{4\sqrt{3}C}, \quad (21)$$

where

$$r = \sqrt{1 - \frac{21La_3Rk^2V_{in}^2}{144C\left|a_1R + 1\right|}}. \quad (22)$$

The input-referred locking range is equal to the output-referred locking range multiplied by the division ratio $n = 3$. Taking into account that $r \approx 1$, (21) provides a very simple expression of the locking range as a function of the active and passive circuit parameters, which can be usefully employed for the design of ILFD with direct forcing signal. Note that all

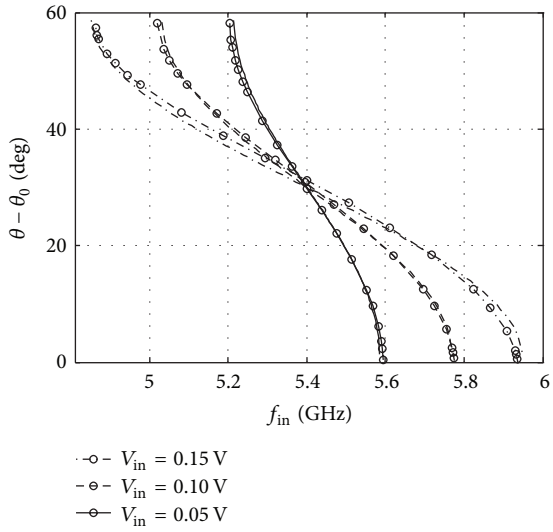

Figure 11: Phase difference between the input and output signals for the divide-by-three ILFD in Figure 5 with $L = 10$ nH and $R = 905\,\Omega$. SPICE simulations are obtained by using BSIM3 transistor models in MOSIS-IBM 8RF 0.13 μ technology with $V_{DD} = 1.2$ V, $W/L_c = W/L_i = 24/0.12$, $W/L_{PMOS} = 4.5W/L_{NMOS}$. Analytical results are obtained by using (19).

the formulas based on the mixing principle predicts that the locking range is zero in this case [11–13].

4. Circuit Simulation

SPICE simulations of the circuit in Figure 5 were performed by using BSIM3 models of active devices in 0.13 μm technology. Time waveforms of the input and output voltages, reported in Figure 9(a), demonstrated that the circuit under study can actually operate as a divide-by-three ILFD.

Moreover, SPICE simulations were performed to investigate the dependence of the locking range on the circuit parameters and to determine the accuracy of analytical expressions deduced in previous section. The locking region in the (f_{in}, V_{in}) plane is reported in Figure 10(a) and the modification of the locking region as a function of the transistor sizes of the tank quality factor and of the inductor values is reported in Figures 10(b), 10(c), and 10(d), respectively. The comparison of the SPICE results with the results obtained by analytical expression (21), also reported in Figure 10, shows a good accuracy of (21), which can be effectively used to design the ILFD in Figure 5.

It is interesting to observe that, according to SPICE simulations and to the prediction of (21), the width of the frequency range of locking increases with the transistor size, which is proportional to a_1 and a_3, but the center of the locking range moves toward lower frequencies due to the parasitic capacitances (Figure 10(b)). Moreover, the width of the locking range does not depend on the quality factor of the tank (Figure 10(c)) and, thus, it is not necessary to keep low the quality factor in order to widen the locking range as it happens in other ILFD topologies. Finally, we note that the increasing of the L/C ratio for a constant LC product (Figure 10(d)) widens the locking range but shifts it toward lower frequencies due to nonlinear effects, as predicted by (17).

Finally, the phase relationship between the input and output signals was investigated. SPICE simulations reported in Figure 11 show that a wide variation is present when the input frequency varies within the locking range. Analytical results obtained by applying (19) and reported in Figure 11 show that presented formula provides an acceptable approximation to the numerical results. However, formulas are not able to predict a constant phase offset $\theta_0 = 7^\circ$, that is, due to the reactive behavior of nonlinearities, which were here assumed to be memoryless. Thus, we conclude that, even if small discrepancies are present between numerical and analytical results, formulas are able to capture the main characteristics of the direct forcing injection, providing fairly accurate approximation to numerical results.

5. Conclusions

We have shown that in the injection-locked dividers wherein the external synchronization signal is applied directly to the LC-tank, the synchronization mechanism takes place according to a process that cannot be explained by the simple mixing between the input and output signals. This is the case of some divide-by-three circuits, of which we analyzed in detail a particular implementation. Then, a method for the approximate calculation of oscillation in the synchronous states was exposed that allows us to determine the amplitude and the phase of the oscillation and the interval of locking in explicit form as a function of the circuit parameters. These expressions, which are relatively simple and useful for design, provide sufficiently accurate results as shown by numerical simulations.

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