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Research Article

DFAL: Diode-Free Adiabatic Logic Circuits

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The manufacturing advances in semiconductor processing (continually reducing minimum feature size of transistors, increased complexity and ever increasing number of devices on a given IC) change the design challenges for circuit designers in CMOS technology. The important challenges are low power high speed computational devices. In this paper a novel low power adiabatic circuit topology is proposed. By removing the diode from the charging and discharging path, higher output amplitude is achieved and also the power dissipation of the diodes is eliminated. A mathematical expression has been developed to explain the energy dissipation in the proposed circuit. Performance of the proposed logic is analyzed and compared with CMOS and reported adiabatic logic styles. Also the layout of proposed inverter circuit has been drawn. Subsequently proposed topology-based various logic gates, combinational and sequential circuits and multiplier circuit are designed and simulated. The simulations were performed by VIRTUOSO SPECTRE simulator of Cadence in 0.18 μm UMC technology. In proposed inverter the energy efficiency has been improved to almost 60% up to 100 MHz in comparison to conventional CMOS circuits. The present research provides low power high speed results up to 100 MHz, and proposal has proven to be used in power aware high-performance VLSI circuitry.

1. Introduction

During the past decade, use of adiabatic logic circuits with energy recovery scheme has received considerable attention in high performance low-power applications such as radio-frequency identification (RFID) tags, smart cards, and sensors because they outperforms in energy efficiency without sacrificing noise immunity and driving ability over their CMOS counterparts. The power consumption in conventional CMOS circuits is proportional to the load capacitance and square of the supply voltage [1, 2], thus researchers have been focused on scaling of the supply voltage and reducing the capacitance to reduce power consumption. For scaling the supply voltage the transistor threshold voltage (V_t) must also be scaled down proportionally, however reducing the transistor threshold voltage V_t results in proportional increase in subthreshold leakage current. Further the circuit capacitance can be minimized by reducing the sizes of devices but this affects the driving ability of the circuit [3].

Due to the above limitations, in recent years adiabatic systems have been used to reduce power consumption. Various adiabatic logic circuits have been proposed [3–21] working on the energy recovery [4] principle. The term "adiabatic" is derived from a reversible thermodynamic process [5] and it stands for a system where a transformation takes place in such a way that no gain or loss of heat/energy occurs. Ideally the heat/energy loss can be made almost zero if the transformation takes place sufficiently slowly [6]. The main idea in an adiabatic charging is that transitions are considered to be sufficiently slow so that all the nodes are charged or discharged at a constant current. In this way power dissipation is minimized by decreasing the peak current flow [7] through the transistors. This is made possible by replacing the DC power source by ramp like power/clock signals [8, 9]. The energy that is stored in the capacitors during charging is recovered and used in the subsequent computations [10, 11]. It must be noted that systems based on the above mentioned theory of charge recovery are not necessarily reversible. The

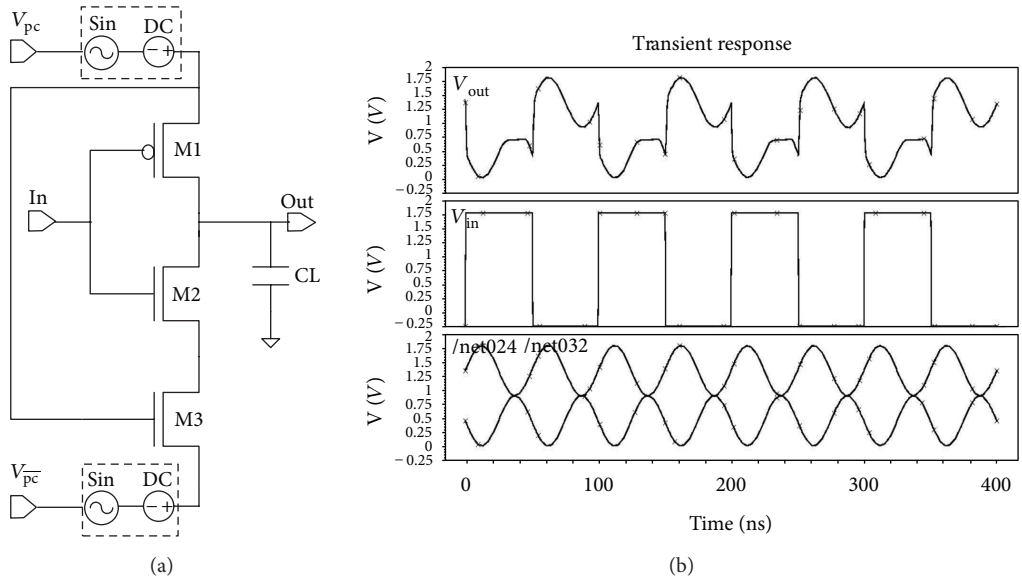

Figure 1: Proposed DFAL inverter topology (a) circuit diagram, (b) simulation waveforms using VIRTUOSO SPECTRE simulator of Cadence in 0.18 μm UMC technology.

reversible energy recovery circuits have the control signal(s) coming from the next stage, so the design overhead for applying such logic in a large system is considerable [12].

In this paper, the additional challenges with recently reported adiabatic families [13–16] have been explored and their solution is proposed through a novel diode free adiabatic logic (DFAL) circuit which is static in nature. Further we have also proposed various DFAL based logic circuits and compare their performances with the recently reported adiabatic circuits and conventional CMOS circuit. The purpose is to improve the overall performance without adding complexity and degrading output amplitudes. DFAL inverter circuit has almost 60% of energy saving compared to CMOS circuit.

The paper is structured into six sections. First of all the limitations of recently reported adiabatic circuit is provided in Section 2. Section 3 describes the structure and operation, mathematical analysis, power efficiency and delay with frequency and load capacitances, and layout of the proposed inverter circuit. Section 4 consists of comparison of proposed circuit with existing adiabatic circuits. Section 5 includes DFAL based logic circuits. Section 6 has concluding remarks.

2. Limitations in the Recently Reported Adiabatic Logic Circuits

The recently reported adiabatic circuits like 2PASCL, GFCAL, CEPAL and QSERL mainly suffer from the following imperfections:

(1) output amplitude degradation;

(2) large delay;

(3) complex circuit structure.

The GFCAL [13] circuit has diodes in the charging and discharging path, voltage drop across the diode due to cut-in voltage (V_γ) causes power dissipation when current flow across it. Also, diode based logic families suffers from output amplitude degradation. Though GFCAL have very less power dissipation in comparison to other adiabatic logic families but it suffers from very large delay at its output and amplitude degradation. Unlike GFCAL circuit, QSERL [14] circuit has two power clocks with two phases. Due to the hold phases it suffers from floating output which results in lack in robustness. The CEPAL [15] circuit has excellent driving ability and robustness, also its throughput does not depend on the frequency ratio; however it is not so power efficient in comparison to the others. Also it have one extra diodes in its charging and discharging path both, which will cause large area and other problems. The 2PASCL [16] circuit design does not have diodes in its charging path, thus current flows only through the transistor during charging which will reduce the drawbacks related to the diode based circuits. Also instead of using ramp or sinusoidal power clocks here split level sinusoidal power clocks are used, which have certain advantages like reduced delay and power dissipation at the output, higher output amplitude, and so forth. 2PASCL circuit structure is simple and similar to static CMOS circuit in comparison to GFCAL and CEPAL circuits. However the diode used in the pull up network and diode in the pull down network to recycle the charge from output node causes power dissipation, which cannot be avoided.

3. Diode Free Adiabatic Logic Circuits (DFAL)

3.1. Proposed Circuit Structure. Figure 1 shows the circuit diagram and simulated waveforms verifying the operation of

Table 1: Specifications for simulation.

Process/MOS model	0.18 μm CMOS/BSIM3v3.2
Simulator	VIRTUOSO SPECTRE: CADENCE
MOS dimensions	0.24/0.18 for all logic circuits*
Clock rate (f_{pc})	Two times the data rate (f_{in})

*All sizes are in μm.

an inverter based on DFAL circuit. The attractive feature of proposed topology is that it is diode free; there is not any diode in its charging or discharging path. In our proposal, split level sinusoidal power clock supply V_{PC} and $V_{\overline{PC}}$ are used. One clock is in phase while the other is inverted. The voltage level of V_{PC} exceeds that of $V_{\overline{PC}}$ by a factor of $V_{PC}/2$, this will minimize the voltage difference between the electrodes and consequently power dissipation is reduced. Split level clock charges/discharges the load capacitance comparatively slowly than the other adiabatic power clocks. Since the efficiency of adiabatic logic circuits depends upon how slowly the load capacitance is charged or discharged so power dissipation is minimized further.

The schematic of DFAL resembles the static CMOS logic; however circuit operates in adiabatic manner. The nMOS transistor (M3) in the pull down network adjacent to the M2 is used to replace the diode for the discharging. Power clock (V_{PC}) controls the turning ON and OFF of this transistor (M3). The main power dissipation in reported adiabatic circuits in their discharging path occurs at the (MOS) diodes due to the threshold voltage drop (nonadiabatic loss) whereas in our proposed circuit it is due to the ON resistance (adiabatic loss) of channel of MOS transistor M3. The power dissipation due to this ON resistance (of M3) is significantly lower than the power dissipation due to the threshold voltage drop through diodes. Also M3 is used to recycle charges from the output node hence the adiabatic losses can be recovered further. However the losses cannot be completely recovered and power dissipation cannot be removed completely because the proposed logic circuit is non reversible. Hence by using MOS transistor M3, power dissipation is hugely reduced compared to the diode based adiabatic circuits.

3.2. Circuit Operation. Depending on the supply clock signal phases, circuit operation is divided into two stages, evaluation and hold. In evaluation phase V_{PC} swings up while $V_{\overline{PC}}$ swings down; however in hold phase V_{PC} swings down and $V_{\overline{PC}}$ swings up as shown in Figure 1(b).

In evaluation phase, when the output node is LOW and pMOS tree is turned ON, load capacitance C_L is charged through pMOS transistor (M1) resulting in the HIGH state at the output. Further when output node is HIGH and nMOS tree turns ON, discharging and recycling of charges to the power clock ($V_{\overline{PC}}$) via nMOS transistor (M2 and M3) occurs, resulting in the output logic state to be LOW.

In hold phase, when output node is LOW and nMOS tree is ON, no transitions occur at the output. The same process happens when the output node is HIGH and pMOS tree is ON. Due to the hold phase, dynamic switching is reduced and thus energy dissipation is also reduced.

3.3. Mathematical Analysis. In Figure 1(a) the supply clocks V_{PC} and $V_{\overline{PC}}$ are composed from sinusoidal and DC waveforms and they can be expressed as:

$$V_{PC} = \frac{V_{dd}}{4}\sin(\omega t + \theta) + \frac{3}{4}V_{dd},$$
$$V_{\overline{PC}} = \frac{V_{dd}}{4}\sin(\omega t + \theta) + \frac{1}{4}V_{dd}. \quad (1)$$

The energy dissipation in proposed inverter is as follows:

$$E_{DFAL} = E_{charg} + E_{dischrg}$$
$$= 0.5C_L{V_{tp}}^2 + 0.5C_L\left(V_{\overline{PC}_{p\text{-}p}} - V_{tn}\right)V_{tn}. \quad (2)$$
$$\text{(Through M1)} \quad \text{(Through M2, M3)}.$$

V_{tp} and V_{tn} are the threshold voltages of pMOS and nMOS respectively and $V_{\overline{PC}_{p\text{-}p}}$ is the split level sinusoidal power supply, 180 degree out of phase with $V_{PC_{p\text{-}p}}$ supply. C_L is the load capacitance.

3.4. Power Efficiency and Delay with Frequency. To check the performance of the proposed circuit, both proposed DFAL as well as conventional CMOS inverters have been simulated and their power and delay were measured and compared with the variation in transition frequency. The specifications used for simulation are shown in Table 1.

The input and supply frequencies are varied simultaneously (keeping the supply frequency (f_{pc}) two times the input frequency (f_{in}) from 1 MHz to 100 MHz and load capacitance is set to 20 fF and power and delay were measured for 10 cycles of charging/discharging as shown in the Figure 2. It may be observed that as frequency increases, power dissipation of both the inverters increases whereas proposed DFAL inverter have lesser power dissipation at each frequency in comparison to conventional CMOS.

However a continuous decrease in delay for both the inverters with frequency is observed. Initially proposed DFAL inverter has larger delay than CMOS but as frequency reaches around 20 MHz the difference between their delays are reduced and after that, around at 50 MHz both the inverters have almost equal delay. Thus it is clear from the above analysis that as both power and speed is improved so overall PDP of proposed inverter is improved in comparison to conventional CMOS throughout the whole frequency range of Figure 2. This shows that our proposed inverter can be used in a wide range of frequencies with improved performance than CMOS.

3.5. Power Efficiency and Delay with Load Capacitance. To check the driving ability of the proposed DFAL inverter with CMOS inverter, we tested the inverters by adding extra capacitive load at the output node one by one from 10 fF to 200 fF. Clock rate and data rate were kept fixed at 80 MHz and 40 MHz, respectively, and power and delay were measured for 10 cycles of charging/discharging. When load capacitance is gradually increased from 10 fF to 200 fF as shown in Figure 3, power dissipation of both the inverters increases

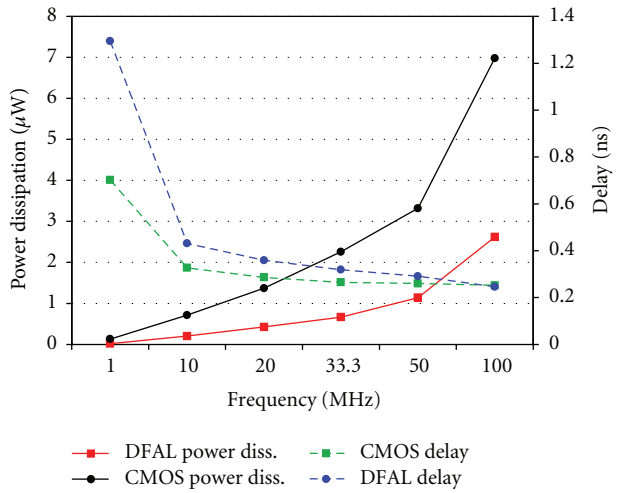

Figure 2: Power dissipation and delay of inverters with frequency.

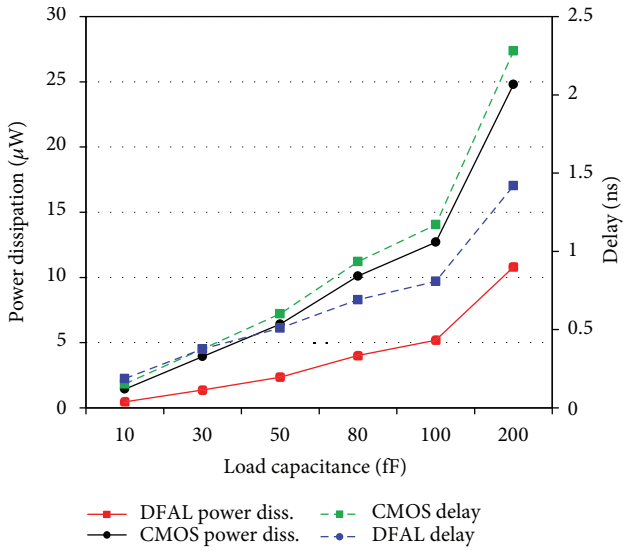

Figure 3: Power dissipation and delay of inverters with load capacitance.

correspondingly; however our proposed inverter has good power efficiency than CMOS at each point.

It may be observed that while increasing the load capacitance, delay in inverters output stage increases and both the inverters have almost equal delay at lower value of load capacitances. However after 40 fF (load capacitance) delay of CMOS inverter becomes larger than the proposed DFAL inverter. This shows that even at larger loads power dissipation and delay of proposed DFAL inverter is reduced and thus the overall PDP improves significantly in comparison to CMOS.

The power, delay, PDP, percentage of energy saving and adiabatic gain with frequency and load capacitance of conventional CMOS, and proposed DFAL inverters have been measured as shown in Tables 2 and 3, respectively. It may be observed that proposed inverter provide almost 60% of energy saving and around 2.5 of adiabatic gain at all observed frequencies and load capacitances. Adiabatic Gain "G" is defined as the ratio between the energy dissipated by a traditional CMOS gate and the equivalent adiabatic gate [17]. Higher adiabatic gain shows better energy efficiency.

3.6. Layout/Area. The layout of proposed DFAL inverter circuit has been drawn as shown in Figure 4. From the layout it has been characterized that the chip area of proposed inverter is slightly higher than the CMOS due to the extra nMOS in discharging path. Proposed inverter has 13.86 μm^2 adiabatic area while CMOS inverter has 10.59 μm^2. Thus the proposed logic requiring fewer transistors is comparable to

Table 2: Comparison of power, delay and PDP with frequency at 20 fF in 10 cycles of charging/discharging.

Inverters	1 MHz	10 MHz	20 MHz	33 MHz	50 MHz	100 MHz
			Power dissipation (μW)			
CMOS	0.131	0.714	1.37	2.26	3.32	6.98
Proposed	0.019	0.204	0.426	0.666	1.14	2.62
			Delay (ns)			
CMOS	0.702	0.327	0.286	0.265	0.26	0.252
Proposed	1.29	0.431	0.359	0.319	0.291	0.246
			PDP (fJ)			
CMOS	0.092	0.23	0.39	0.6	0.86	1.76
Proposed	0.026	0.088	0.153	0.21	0.33	0.64
			Energy saving %			
	71.7	61.7	60.7	65	61.6	63.6
			Adiabatic gain			
	3.54	2.61	2.54	2.86	2.6	2.75

Table 3: Comparison of power, delay and PDP with load capacitance at f_{pc} = 80 MHz and f_{in} = 40 MHz in 10 cycles of charging/discharging.

Inverters	10 fF	30 fF	50 fF	80 fF	100 fF	200 fF
			Power dissipation (μW)			
CMOS	1.44	3.93	6.42	10.1	12.7	24.8
Proposed	0.463	1.36	2.35	4	5.18	10.8
			Delay (ns)			
CMOS	0.152	0.376	0.601	0.934	1.166	2.275
Proposed	0.187	0.376	0.51	0.691	0.808	1.42
			PDP (fJ)			
CMOS	0.219	1.48	3.86	9.43	14.8	56.4
Proposed	0.087	0.511	1.19	2.77	4.19	15.34
			Energy saving %			
	60.2	65.4	69.1	70.6	71.6	72.8
			Adiabatic gain			
	2.51	2.89	3.24	3.40	3.53	3.67

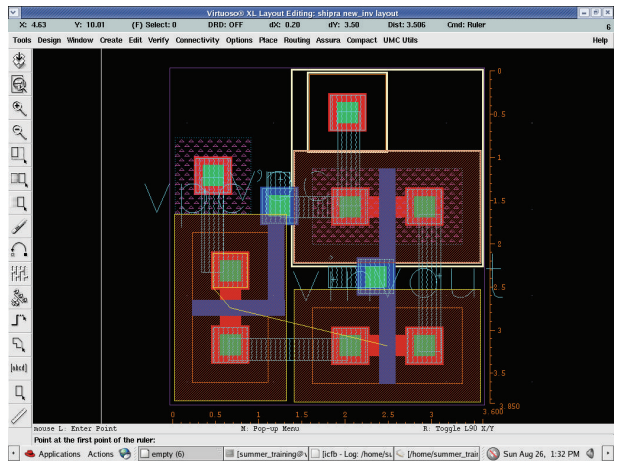

Figure 4: Layout of proposed DFAL inverter.

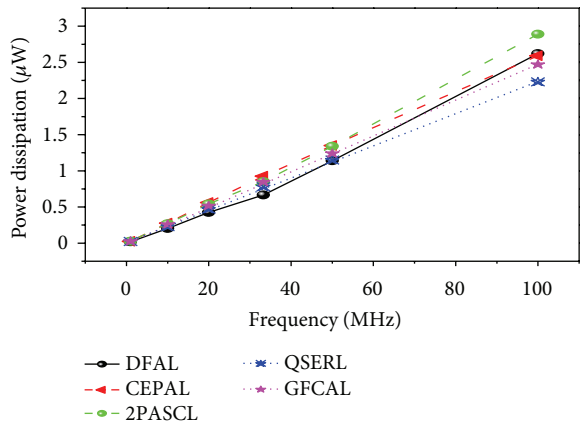

Figure 5: Power dissipation of inverters with frequency.

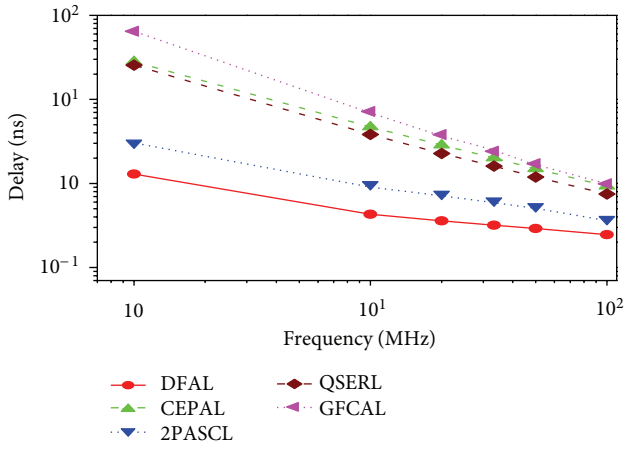

Figure 6: Delay of inverters with frequency.

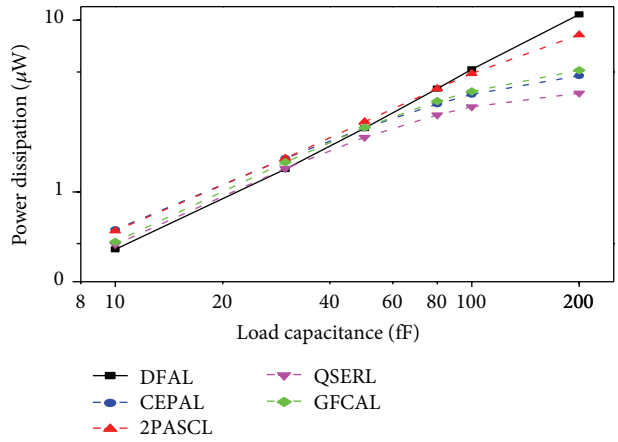

Figure 7: Power dissipation of inverters with load capacitance.

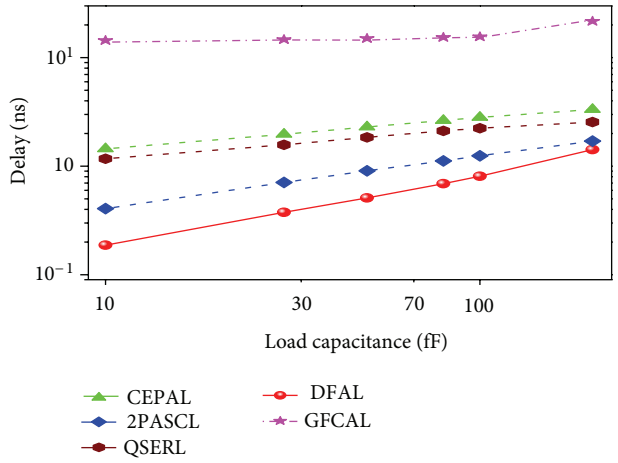

Figure 8: Delay of inverters with load capacitance.

the CMOS, it needs less complex layout design and can be used to build larger circuits on a single chip.

4. Comparison of Proposed DFAL Circuit with Existing Adiabatic Logic Circuits

The existing recently reported adiabatic logic inverter circuits (CEPAL, 2PASCL, QSERL, and GFCAL) are simulated with similar circuit parameters as shown in Table 1. Performances of several inverters based on different adiabatic topologies have been evaluated in terms of power and delay with variation in input frequency and load capacitances. For frequency analysis load capacitance is set to 20 fF and for load analysis, frequency of power clock and input is set to 80 MHz and 40 MHz, respectively.

4.1. Variation in Frequency. Figure 5 shows the trend of power dissipation with frequency for CEPAL, 2PASCL, QSERL, GFCAL, and our proposed DFAL inverters. All the inverters follow the similar trend, that is, the increasing power dissipation with frequency. However it may be noted that the proposed DFAL inverter has lowest power dissipation in a wide range of frequencies that is, up to 50 MHz. After certain frequency (50 MHz) the QSERL and GFCAL inverters have lower power dissipation than proposed DFAL inverter, but have very low output logic levels which leads to completely incorrect output whereas the proposed DFAL inverter has sufficient output logic levels and acceptable output signals. Thus the proposed DFAL inverter will be a good choice even at higher frequencies than the other adiabatic inverters.

It may be observed from the Figure 6 that the delay at the output stage of all the inverters increases with frequency whereas proposed inverter has lowest delay at all points in the graph. The observation from Figures 5 and 6 confirms the improved performance of proposed DFAL inverter (assuring improved overall PDP) in comparison to the recently reported adiabatic inverters.

4.2. Variation in Load Capacitances. When load capacitance at the inverter output stage is varied from 10 fF to 200 fF, power dissipation in all the inverters increases whereas proposed DFAL inverter has lowest dissipation in wide range of capacitances. After certain large capacitance (here 60 fF in Figure 7), output logic levels of other adiabatic inverters is so reduced that they will produce incorrect output logic and

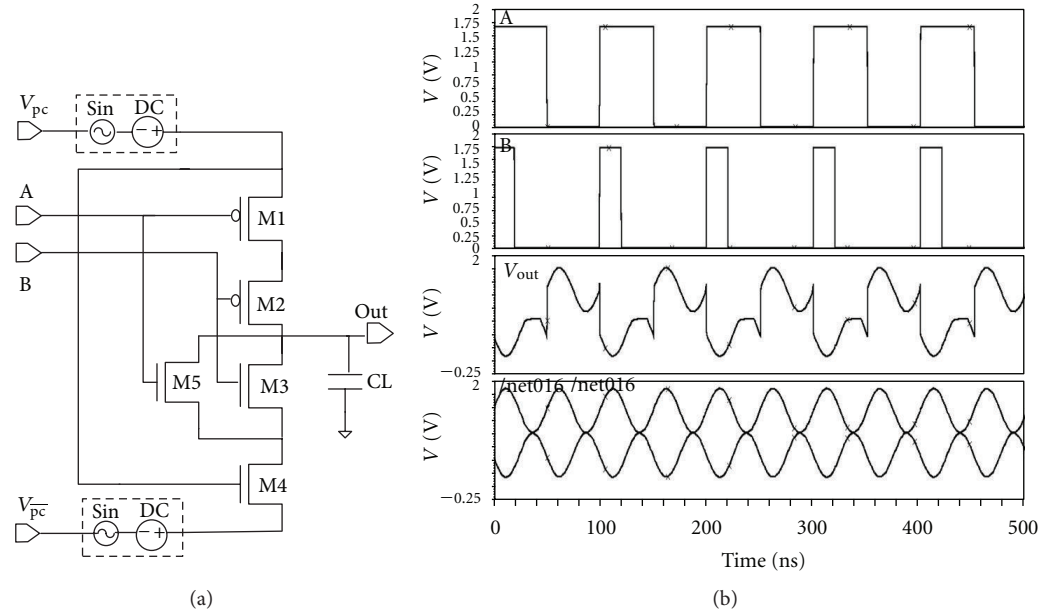

Figure 9: Proposed DFAL NOR gate (a) circuit diagram, (b) simulation waveforms.

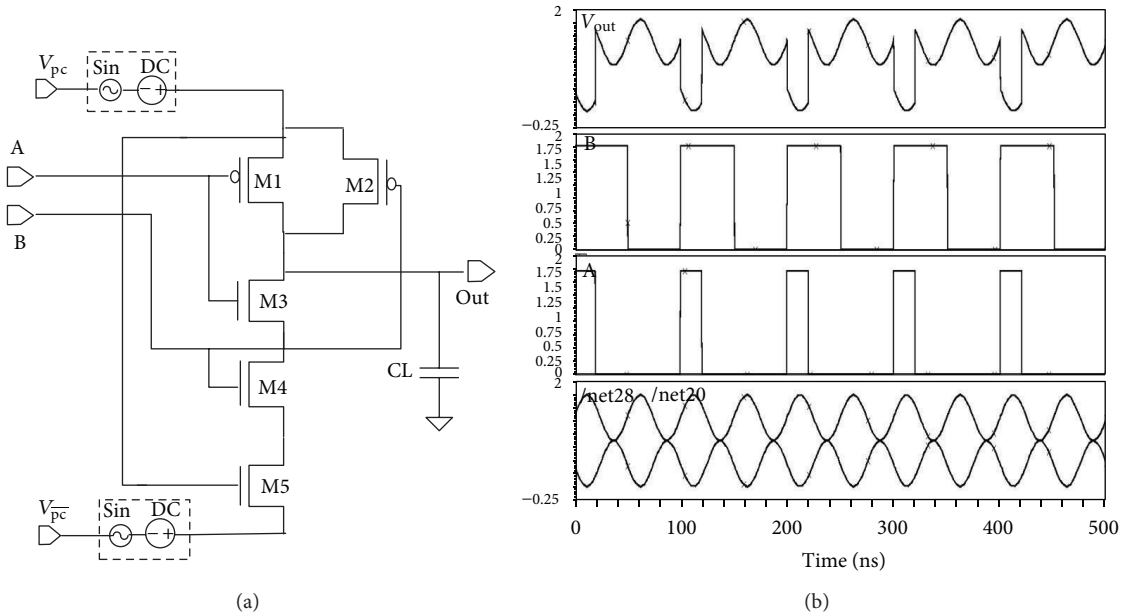

Figure 10: Proposed DFAL NAND gate (a) circuit diagram, (b) simulation waveforms.

lower power dissipation than the proposed inverter whereas proposed inverter has correct and sufficient output logic levels even at such a high load capacitances.

Delay at the output node of each inverter increases with load capacitances and GFCAL has worst delay while our proposed DFAL inverter has lowest delay at each load capacitances as shown in Figure 8. Thus these observations show that our proposed DFAL inverter performs well with high loads also.

5. Proposed DFAL-Based Logic Circuits

The NAND and NOR gates are universal gates and are used to design complex digital circuits. Exclusive-OR gates are well known for their roles in larger circuits such as full adders and parity checkers. As we cannot build adiabatic circuits by simply using conventional method [18] therefore an optimized design of these gates can certainly benefit the performance of the larger circuits. In the following subsections various logic gates and circuits have been presented based on DFAL circuits.

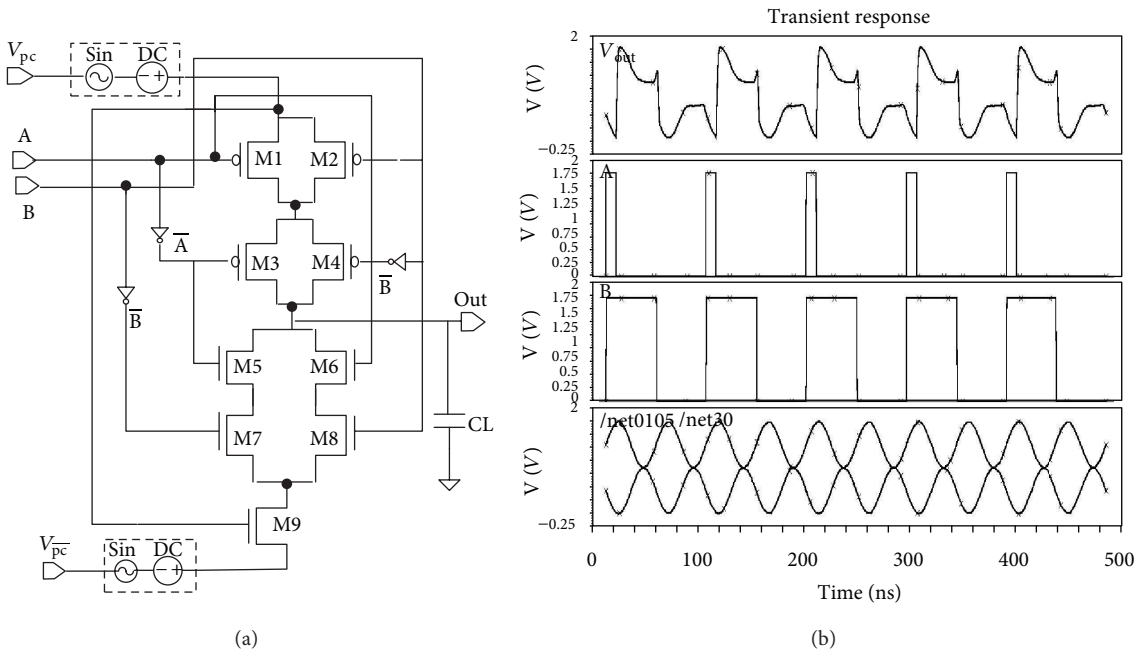

Figure 11: Proposed DFAL XOR gate (a) circuit diagram, (b) simulation waveforms.

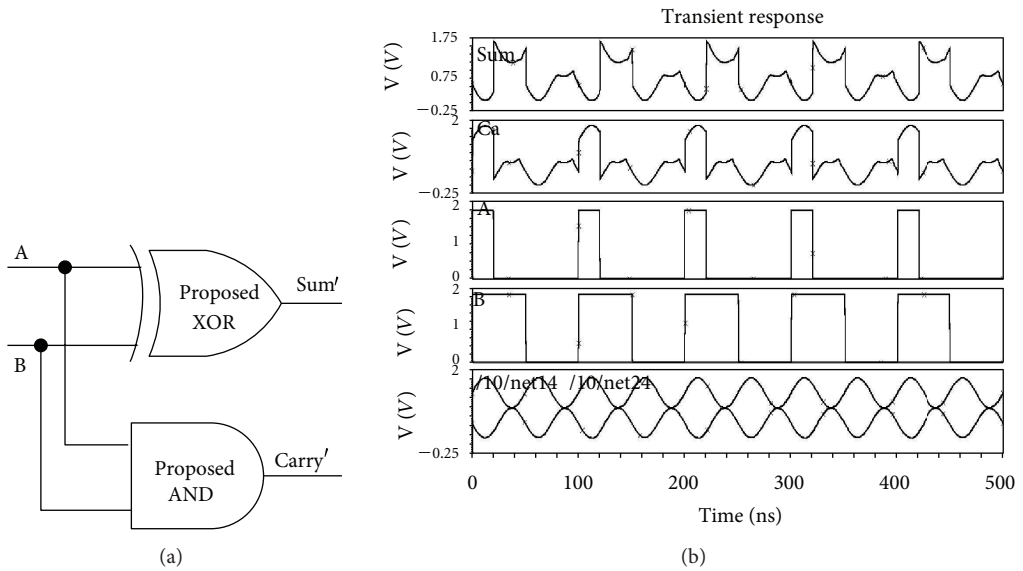

Figure 12: Proposed DFAL Half Adder (a) circuit diagram, (b) simulation waveforms.

5.1. Proposed DFAL NOR Gate. Circuit diagram of proposed DFAL NOR gate is shown in Figure 9(a). It has two p-channel MOSFETs (M1 and M2) and two nMOS transistors (M3 and M5) and a discharging nMOS transistor M4 whose gate is directly connected with a split level sinusoidal power clock (V_{PC}). Gates of M1 and M5 are connected with an input A and M2 and M3 with another input B.

The simulated timing waveforms for input strings A = "1100110011001100", B = "1000100010001000" and output = "0011001100110011" are shown in Figure 9(b).

5.2. Proposed DFAL NAND Gate. Circuit diagram of proposed DFAL NAND gate is shown in Figure 10(a). It has two p-channel MOSFETs (M1 and M2 connected in parallel) and two nMOS transistors (M3 and M4 connected in series). Output load capacitance is discharged through nMOS transistors M3, M4 and a discharging transistor M5 whose gate is directly connected with a split level sinusoidal power clock (V_{PC}). Gates of M1 and M3 are tied together with an input A and M2 and M4 with another input B.

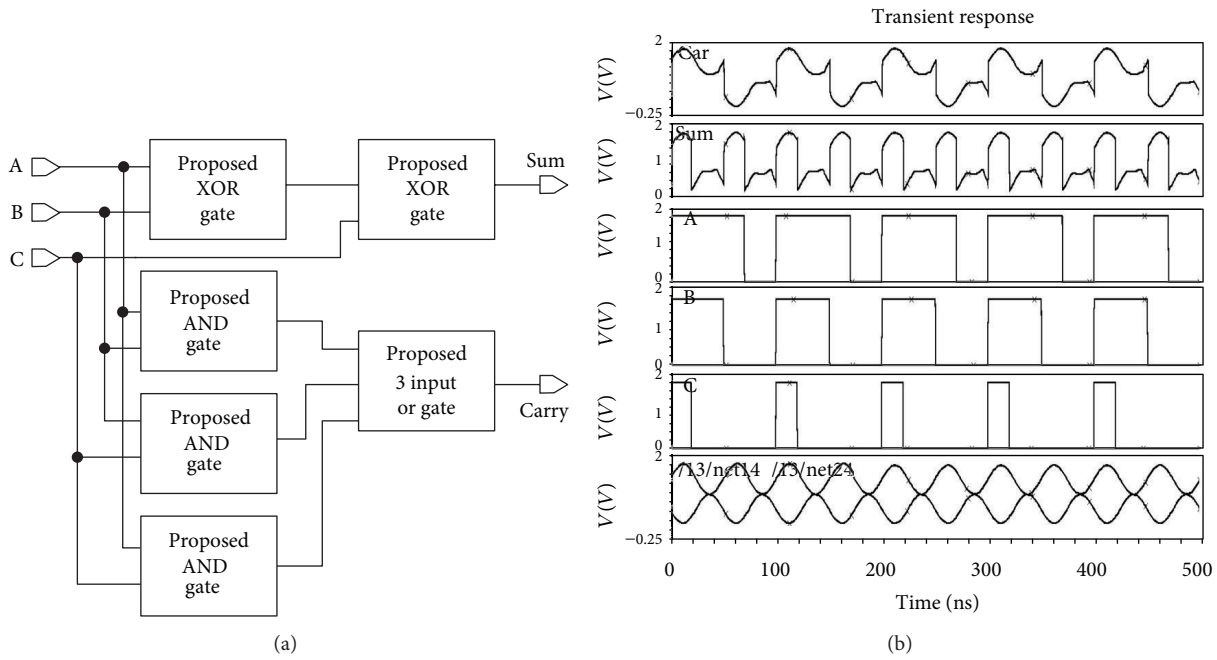

Figure 13: Proposed DFAL Full Adder (a) circuit diagram, (b) simulation waveforms.

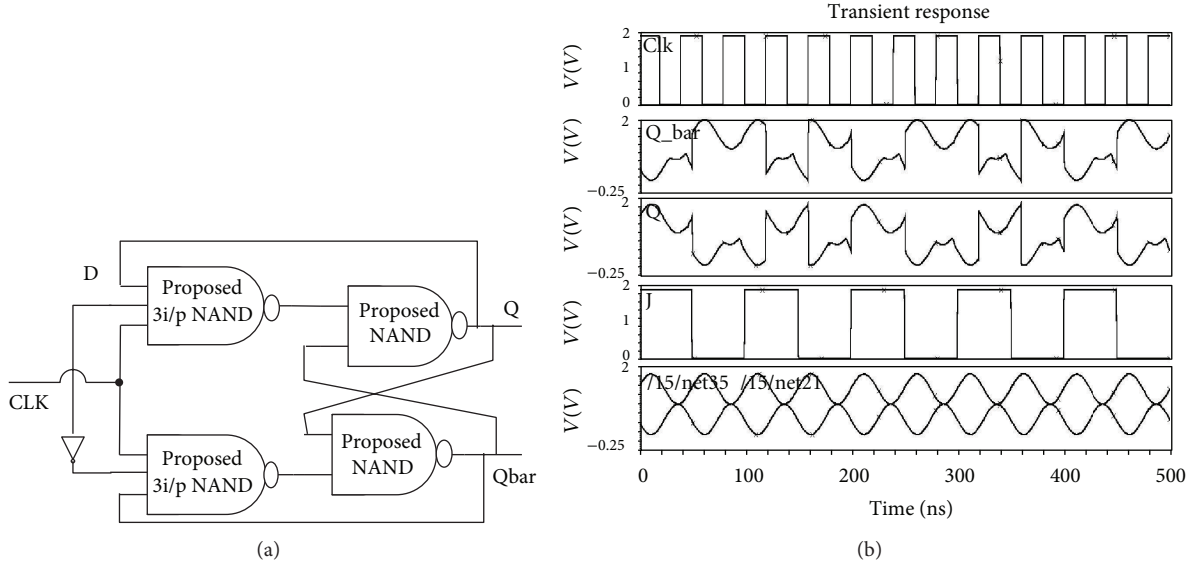

Figure 14: Proposed DFAL D flip flop (a) circuit diagram, (b) simulation waveforms.

The simulated timing waveforms for input strings B = "11001100110011001100", A = "10001000100010001000" and output = "01110111011101110111" are shown in Figure 10(b).

5.3. Proposed DFAL XOR Gate. The structure of proposed DFAL XOR gate is shown in Figure 11(a). It has four p-channel MOSFETs (M1, M2 in parallel and M3, M4 in parallel) and four nMOS transistors (M5 and M7 connected in parallel with M6 and M8). Gates of M1 and M6 are tied together with an input "A" and M3 and M5 with complement of that input. Gates of M2 and M8 are tied together with an input "B" and M4 and M7 with complement of that input. A discharging transistor M9 is also used whose gate is directly connected with a split level sinusoidal power clock (V_{PC}).

The simulated timing waveforms for input strings B = "11001100110011001100", A = "10001000100010001000" and output = "01000100010001000100" are shown in Figure 11(b).

5.4. Proposed DFAL Half Adder. The proposed DFAL half adder consists of a proposed DFAL XOR gate and a proposed DFAL AND gate as shown in Figure 12(a). Outputs of the half adder are SUM' (XOR gate output) and CARRY' (output

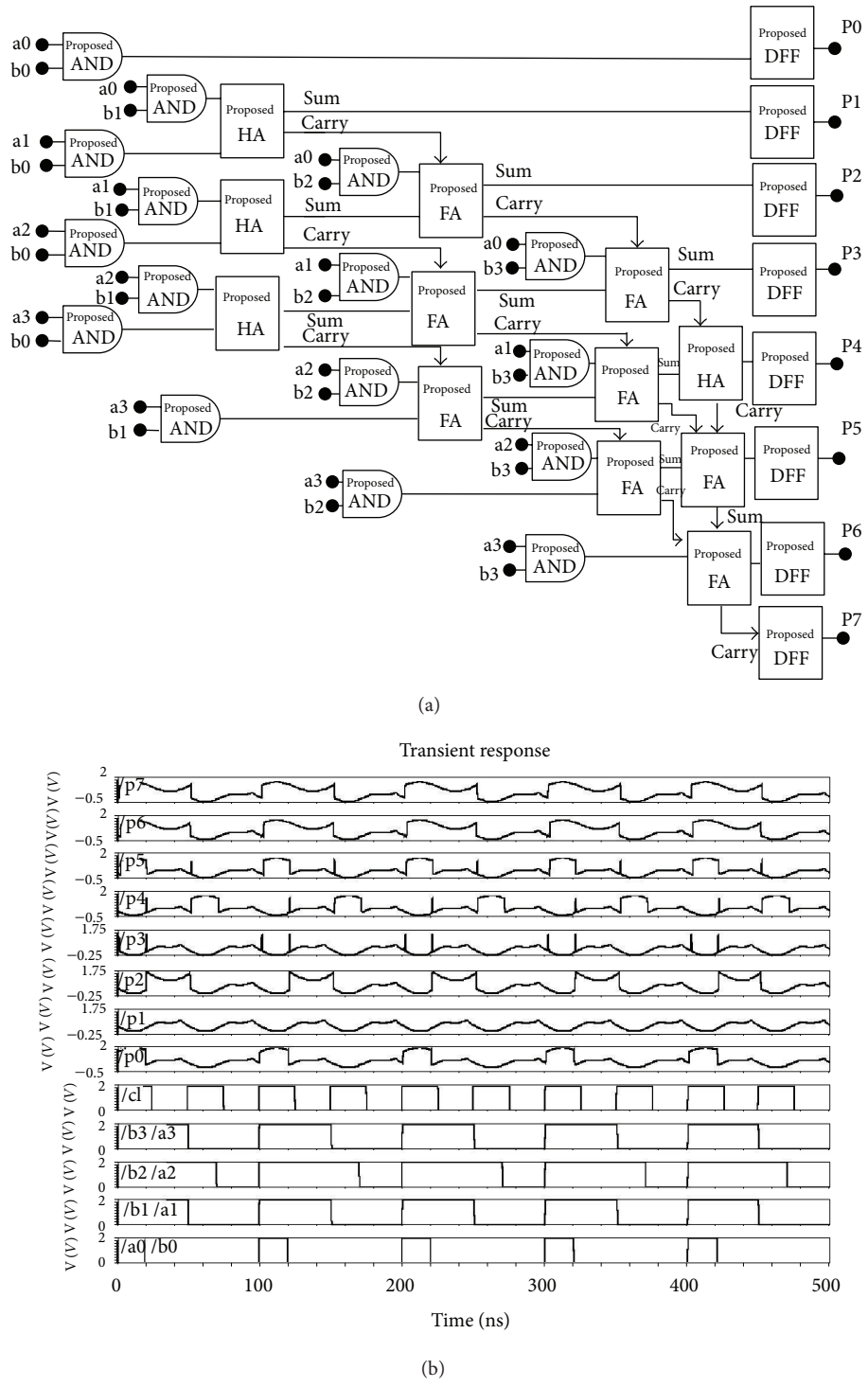

Figure 15: Proposed DFAL Multiplier (a) circuit diagram, (b) simulation waveforms.

of AND gate). The simulated output strings for input strings A = "11001100110011001100", B ="11001100110011001100" are SUM' = "01000100010001000100" and CARRY = "10001000100010001000" as shown in Figure 12(b).

5.5. Proposed DFAL Full Adder. Proposed DFAL full adder circuit is made from two DFAL XOR gates, three DFAL AND gates and one 3 input DFAL OR gate as shown in Figure 13(a). Outputs SUM and CARRY for inputs A = "10001000100010001000", B = "11001100110011001100" and C = "11101110111011101110" are "10101010101010101010",

Table 4: Comparison of proposed DFAL and CMOS circuits at f_{pc} = 100 MHz, f_{in} = 50 MHz in 10 cycles of charging/discharging.

Circuits	NOT	NAND	NOR	XOR	HA*	FA*	Dff*	Multiplier
Power dissipation (μW)								
CMOS	0.247	0.563	0.367	0.885	2.41	7.97	5.02	136
Proposed	0.041	0.17	0.107	0.216	0.281	0.719	0.786	32.3
Delay (ns)								
CMOS	0.003	0.004	0.005	0.12	0.12	0.25	0.23	0.88
Proposed	0.005	0.007	0.0054	0.11	0.15	0.45	0.37	1.71
PDP (fJ)								
CMOS	0.00074	0.0023	0.002	0.11	0.29	1.99	1.15	119.6
Proposed	0.0002	0.0012	0.0006	0.02	0.04	0.324	0.29	55.2
Energy saving %								
	72.9	47.8	70	81.8	86.2	83.7	74.7	53.8
Adiabatic gain								
	3.7	1.91	3.33	5.5	7.25	6.14	3.96	2.16

*Half adder, full adder, D flip-flop.

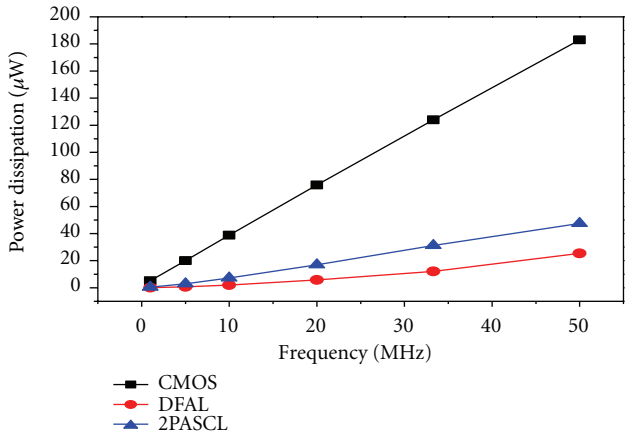

Figure 16: Power dissipation comparison of 4 × 4 bit multiplier with frequency.

"11001100110011001100", respectively, as shown in Figure 13(b).

5.6. Proposed DFAL D Flip-Flop. The structure of proposed DFAL D flip flop is shown in Figure 14(a), it consists of two DFAL 3 input NAND gates and two DFAL 2 input NAND gates and a DFAL inverter circuit. Simulated timing waveforms for inputs D = "11001100110011001100" and CLK = "10101010101010101010" outputs Q = "11001100110011001100" and Qbar = "00110011001100110011" are shown in Figure 14(b).

5.7. Proposed Adiabatic 4 × 4 bit Multiplier. As the proposed DFAL circuit has lower PDP in comparison to the recently reported adiabatic circuits so we can build larger circuits [19] based on our proposed DFAL circuits without adding any performance loss. A 4 × 4 bit DFAL array multiplier is presented and its performance with variation in input frequency has been evaluated.

The 4 × 4 bit DFAL array multiplier circuit consists of DFAL AND gates, DFAL half adders, DFAL full adders and DFAL D flip flops as shown in Figure 15(a). D flip flops are used to store the 8 bit signals. The simulated input and output timing waveforms verifies the multiplier operation as shown in Figure 15(b).

Specification for simulation is same as given in Table 1 and data rate is fixed at 10 MHz for all the inputs. For input strings of first period's first half cycle of Clock (CLK), a3a2a1a0 = "1111" and b3b2b1b0 = "1111", outputs are p7p6p5p4p3p2p1p0 = "11100001". Similarly for first period's second half cycle of Clock, a3a2a1a0 = "1110" and b3b2b1b0 = "1110" outputs are p7p6p5p4p3p2p1p0 = "11000100". For second period's first half cycle of Clock (CLK), a3a2a1a0 = "0100" and b3b2b1b0 = "0100", outputs are p7p6p5p4p3p2p1p0 = "00010000".

To check and compare the performance of proposed DFAL multiplier with CMOS and recently reported (2PASCL) multipliers [20], the input and supply frequencies are varied simultaneously (keeping the supply frequency two times the input frequency) from 1 MHz to 100 MHz and corresponding power dissipations for different multipliers have been measured as shown in Figure 16. DFAL multiplier has very low-power dissipation than CMOS and 2PASCL based multipliers due to the removal of diodes from charging and discharging path of 2PASCL circuits.

As frequency increases, difference in power dissipation levels between DFAL and CMOS and 2PASCL multiplier also increases and our circuit proved to be better in terms of power. The results from Figure 16 indicate approximately 86% of power reduction in comparison to CMOS and 47% in comparison to 2PASCL circuits.

The power, delay, PDP, percentage energy saving and adiabatic gain of conventional CMOS, and proposed DFAL-based various gates and logic circuits are shown in Table 4. It may be observed that proposed DFAL circuit provides almost

50% of energy saving and around 1.9 of adiabatic gain for all the circuits.

6. Conclusion

Diode free adiabatic logic (DFAL) family is a novel adiabatic logic family. The simulation results and comparative performance evaluation revealed that power consumption and overall PDP in the DFAL logic family are considerably lower than the CMOS and other reported adiabatic families thus the proposed DFAL family outperforms and provides almost 50% of energy saving at 50 MHz for all the DFAL based logic circuits. Specifically we presented a 4×4 bit array multiplier to validate the operating capability of larger circuits based on DFAL which has almost 53% of energy saving than CMOS multiplier at 50 MHz. The proposed DFAL circuit would be very effective for reducing the charging energy of analog to digital converters and liquid crystal displays and is advantageous in low-power and high-speed VLSI applications.

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