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Research Article

Additional High Input Low Output Impedance Analog Networks

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This paper presents some additional high input low output impedance analog networks realized using a recently introduced single Dual-X Current Conveyor with buffered output. The new circuits encompass several all-pass sections of first- and second-order. The voltage-mode proposals benefit from high input impedance and low output impedance. Nonideality and sensitivity analysis is also performed. The circuit performances are depicted through PSPICE simulations, which show good agreement with theory.

1. Introduction

In the recent past, realization of configurable analog networks has assumed special significance for modern analogue signal processing applications. The feature is quite suited while designing analog blocks with easy configurability, so as to be employed in field programmable analog arrays (FPAAs). Simple analog blocks with this feature were reported earlier and further researched in most recent works [1–3]. Whereas configurability gives rise to the possibility of several electronic functions from a single topology, cascadability results in practical utility of analog blocks for designing more complex networks without additional coupling elements in form of buffers [4–6]. The most recent analog circuit topology benefits from these features by being suited for a number of first-order electronic functions and offering high input impedance and low output impedance [5]. The two features together are just another step towards reducing circuit components enabling portable high performance systems with ease for FPAA implementations [7, 8]. It may be noted that analog filters continue to appear in open literature as a potential analog block for larger subsystems [2–6, 9–12].

This paper presents additional first- and second-order all-pass filters with the features of high input and low output impedance. State-of-the-art floating simulators have been employed to overcome the drawbacks of passive inductors [13]. It may be noted that floating inductor simulators using current conveyors have been researched well in the literature [14–17]. Transformation technique has further been employed to realize simpler alternative with lesser circuit complexity. Extensive simulations are performed to validate the proposed theory, which not only justify the proposed theory but also provide advancement to the existing knowledge.

2. Additional First-Order All-Pass Filters

The symbol and CMOS implementation of newly developed second generation Dual-X Current Conveyor (DXCC-II) with buffered output are shown in Figure 1. A newly developed DXCC-II is characterized in matrix form by the following relationship:

$$\begin{bmatrix} I_Y \\ I_{Z+} \\ I_{Z-} \\ V_{X+} \\ V_{X-} \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_Y \\ V_Z \end{bmatrix}. \quad (1)$$

The new additional voltage-mode first-order all-pass filter topology is shown in Figure 2. It may be noted that interchanging the positions of $X+$ and $X-$ yields the topology

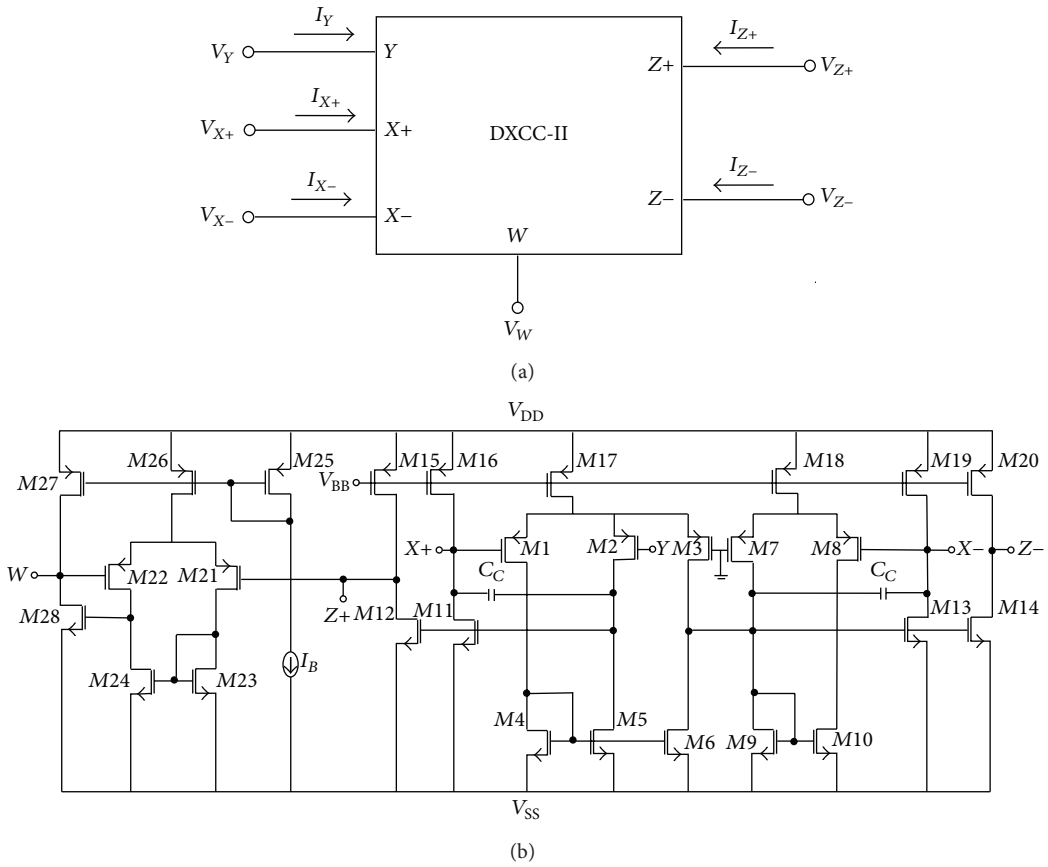

Figure 1: (a) Symbol of DXCC-II with buffer, (b) CMOS implementation of DXCC-II with buffer [5].

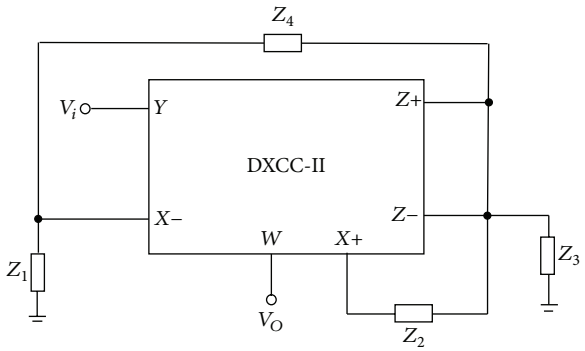

Figure 2: Topology extension by interchanging X ports of a recent work [5].

of [5], a fact not mentioned therein. The given topology is characterized by the general transfer function for continual signals in "s" domain as

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_2Z_3Z_4 + 2Z_1Z_2Z_3 - 2Z_1Z_3Z_4}{Z_1Z_2Z_4 + 2Z_1Z_2Z_3 + 2Z_1Z_3Z_4}. \quad (2)$$

Specialization of the impedances in Figure 2 yields missing circuits of voltage-mode first-order all-pass filters as listed in Table 1. The circuits of Filter 1 and Filter 2 use two passive components. In the circuit of Filter 1, Z_2 and Z_4 are retained with Z_2 as a resistor and Z_4 as a capacitor while open-circuiting Z_1 and Z_3. In the circuit of Filter 2, Z_2 and Z_4 are retained with Z_2 as a capacitor and Z_4 as a resistor while open-circuiting Z_1 and Z_3. No matching condition is required in both of the circuits of Filter 1 and Filter 2. In the last two circuits of Filter 3 and Filter 4 three components are used in each case. In the circuit of Filter 3, Z_1, Z_2, and Z_3 are retained with Z_1, Z_3 as capacitors and Z_2 as a resistor while open-circuiting Z_4. In the circuit of Filter 4, Z_1, Z_2, and Z_3 are retained with Z_1, Z_3 as resistors and Z_2 as a capacitor while open-circuiting Z_4. The circuits of Filter 1 and Filter 2 enjoy the advantage of single resistor control. The circuit of Filter 3 also enjoys the feature of single resistor control but is noncanonical. It also employs both capacitors in grounded form. The circuit of Filter 4 is canonical by employing single capacitor but requires matched grounded resistors. It is also to be noted that other useful first-order analog functions (e.g., lossy and loss less integrators, high pass filter, etc.) are also realizable from the modified general topology of Figure 2.

3. Second-Order Filters

Selection of the impedances in Figure 2 yields a circuit of second-order voltage-mode all-pass filter by retaining all impedances Z_1, Z_2, Z_3, and Z_4. The selection of impedances is Z_1 and Z_3 as capacitive reactance ($Z_1 = 1/sC_1$,

Table 1: First-order voltage-mode all-pass filters.

Circuits ↓	Choice of passive components				Matching condition	Filter type
	Z_1	Z_2	Z_3	Z_4		
Filter 1	Open circuit	R_2	Open circuit	$1/sC_1$	No	Inverting
Filter 2	Open circuit	$1/sC_2$	Open circuit	R_4	No	Noninverting
Filter 3	$1/sC_1$	R_2	$1/sC_3$	Open circuit	$C_1 = C_3$	Inverting
Filter 4	R_1	$1/sC_2$	R_3	Open circuit	$R_1 = R_3$	Noninverting

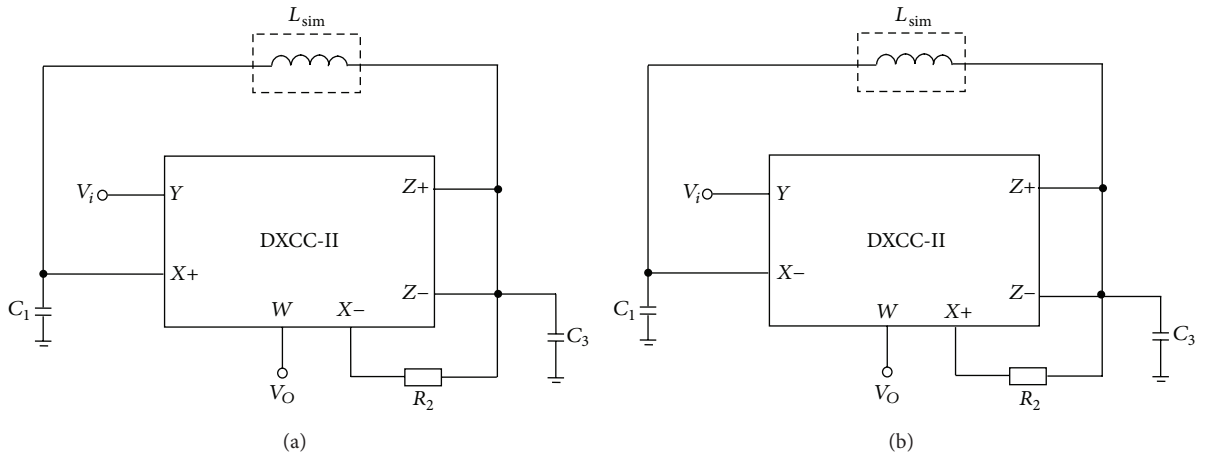

Figure 3: (a) Proposed second-order all-pass filter using simulated inductor. (b) Another circuit obtained by interchanging X ports.

$Z_3 = 1/sC_3$, resp.) Z_2 as resistive, and Z_4 is taken as inductive reactance ($Z_4 = sL_4$). It is a well-known fact that real inductors are not used in integrated analog systems due to their bulky size, which became a motivating factor for the introduction of active-RC networks long back. In the circuit proposed here, simulated floating inductor [13] is used in place of the real inductor. The DXCC-II based circuit of [13] realizes a resistor less floating inductor. The new proposed voltage-mode second-order all-pass filter using simulated inductance ($L_4 \equiv L_{sim}$) is shown in Figure 3(a). Another circuit is obtained by interchanging the positions of the $X+$ and $X-$ terminals and is shown in Figure 3(b). The transfer function of the proposed circuits of Figures 3(a) and 3(b) is given as

$$\frac{V_o(s)}{V_i(s)} = k\frac{s^2L_{sim}C_1R_2 - 2sL_{sim} + 2R_2}{s^2L_{sim}C_3R_2 + 2sL_{sim} + 2R_2}, \tag{3}$$

where $k = +1$ for the circuit of Figure 3(a) and $k = -1$ for the circuit of Figure 3(b).

The expressions for pole-ω_0 and Q are given in (4) and (5), respectively:

$$\omega_0 = \sqrt{\frac{2}{C_3L_{sim}}}, \tag{4}$$

$$Q = R_2\sqrt{\frac{C_3}{2L_{sim}}}. \tag{5}$$

From (4) and (5), it is found that the Q can be tuned independent of ω_0 by adjusting the value of R_2.

Sensitivity figures for pole-ω_0 and Q are given as follows:

$$S_{C_3}^{\omega_0} = S_{L_{sim}}^{\omega_0} = -\frac{1}{2}, \qquad S_{R_2}^{\omega_0} = 0,$$
$$S_{R_2}^{Q} = 1, \qquad S_{C_3}^{Q} = -S_{L_{sim}}^{Q} = \frac{1}{2}. \tag{6}$$

From (6), the sensitivity figures for the proposed circuits are found to be less than or equal to unity in magnitude which implies good sensitivity performance.

It is now to be emphasized that inductance simulator value is as $L_{sim} = (C/g_{m1}g_{m2})$, where g_{m1} and g_{m2} are transconductance of transistors used in simulated inductor, which can be controlled by the gate voltages of those transistors [13]. Here, g_{mi} $(i = 1, 2)$ is the transconductance of the ith MOS transistor and is given as

$$g_{mi} = 2\mu C_{ox}\left(\frac{W}{L}\right)_i (V_{Gi} - V_{Ti}), \quad \text{where } i = 1, 2. \tag{7}$$

By substituting the value of L_{sim} in (3), the transfer function becomes

$$\frac{V_o(s)}{V_i(s)} = k\frac{s^2CC_1R_2 - 2sC + 2R_2g_{m1}g_{m2}}{s^2CC_3R_2 + 2sC + 2R_2g_{m1}g_{m2}}. \tag{8}$$

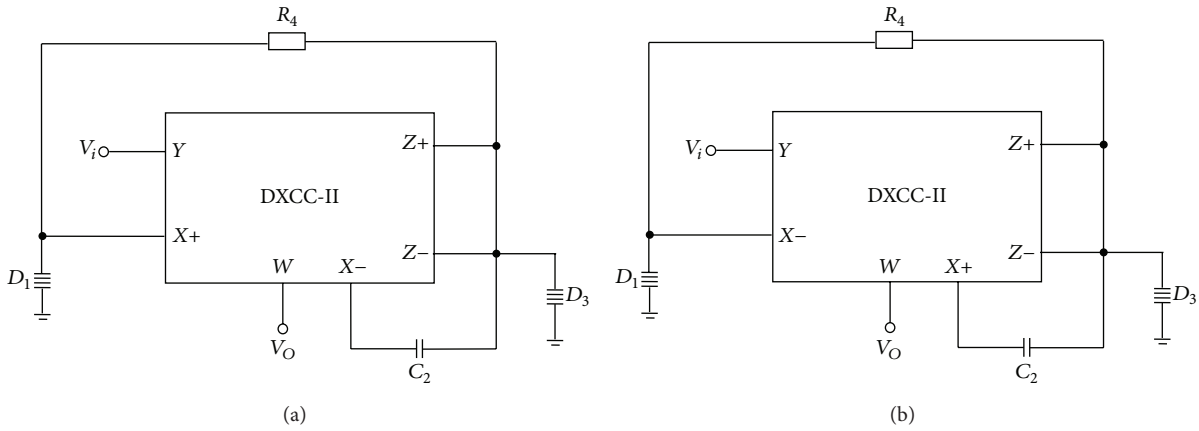

Figure 4: (a) Proposed second-order all-pass filter using frequency transformation. (b) Another circuit obtained by interchanging X ports.

The expressions for pole-ω_0 and Q are also modified and given in (9) and (10), respectively:

$$\omega_0 = \sqrt{\frac{2g_{m1}g_{m2}}{C_3C}}, \tag{9}$$

$$Q = R_2\sqrt{\frac{C_3g_{m1}g_{m2}}{2C}}. \tag{10}$$

Sensitivity figures for pole-ω_0 and Q are now given as follows:

$$\begin{aligned} &S^{\omega_0}_{g_{m1},\,g_{m2}} = -S^{\omega_0}_{C_3} = -S^{\omega_0}_{C} = \frac{1}{2}, \qquad S^{\omega_0}_{R_2} = 0, \\ &S^{Q}_{R_2} = 1, \qquad S^{Q}_{C_3} = S^{Q}_{g_{m1},\,g_{m2}} = -S^{Q}_{C} = \frac{1}{2}. \end{aligned} \tag{11}$$

All the sensitivity figures given in (11) are still less than or equal to unity in magnitude, which suggests good sensitivity performance.

Another possible circuit design is to use frequency transformation method [18]. In frequency transformation, all the impedances are scaled by the frequency-dependent factor $1/s$. Such an impedance-level scaling operation is quite appropriate, because this operation does not affect the transfer function. The motivation behind this scaling operation is that scaling inductive impedance sL by $1/s$ leaves the circuit with the resistor of the same value, $R = L$, and the inductor is eliminated. However, so as not to change the transfer function in the scaling operation, all components must be scaled by the same factor. Therefore, the three passive elements are, namely,

$$Z_R = R, \qquad Z_L = sL, \qquad Z_C = \frac{1}{(sC)}. \tag{12}$$

After transformation $(1/s)$ yields the new components

$$Z'_R = \frac{R}{s}, \qquad Z'_L = L, \qquad Z'_C = \frac{1}{(s^2C)}. \tag{13}$$

Such scaling actually results in a transformation of the elements: a resistor (R) becomes a capacitor of value "$1/R$," an inductor (L) becomes a resistor of value "L," and a capacitor (C) becomes a frequency-dependent negative resistor (FDNR) and is denoted by "D" and symbolized as four parallel lines. The resulting circuit after frequency transformation is shown in Figure 4(a). Another circuit is obtained by interchanging the positions of the $X+$ and $X-$ terminals and is shown in Figure 4(b). Here, the active realization of FDNR using DXCC-II may be used [19]. The active realization of FDNR has the advantage of using a single active element and tunability by means of control voltage. The impedance function [19] is given for the ideal case $[Z] = 1/s^2D_{\text{eq}} = 2/s^2C^2R$ for $C_1 = C_2 = C$.

The transfer function of the proposed circuits of Figures 4(a) and 4(b) is given as

$$\frac{V_o(s)}{V_i(s)} = k\frac{s^2C_1^2R_1R_4 - 4sC_2R_4 + 4}{s^2C_3^2R_3R_4 + 4sC_2R_4 + 4}, \tag{14}$$

where $k = +1$ for the circuit of Figure 4(a) and $k = -1$ for the circuit of Figure 4(b).

The expressions for pole-ω_0 and Q are given in (15) and (16), respectively:

$$\omega_0 = \frac{2}{C_3\sqrt{R_3R_4}}, \tag{15}$$

$$Q = \frac{C_3}{2C_2}\sqrt{\frac{R_3}{R_4}}. \tag{16}$$

Sensitivity figures for pole-ω_0 and Q are given as follows:

$$\begin{aligned} &S^{\omega_0}_{C_3} = -1, \qquad S^{\omega_0}_{R_3} = S^{\omega_0}_{R_4} = -\frac{1}{2}, \qquad S^{\omega_0}_{C_2} = 0, \\ &S^{Q}_{C_2} = -S^{Q}_{C_3} = -1, \qquad S^{Q}_{R_3} = -S^{Q}_{R_4} = \frac{1}{2}. \end{aligned} \tag{17}$$

From (17), the sensitivity figures for the proposed circuits are all less than or equal to unity in magnitude which implies good sensitivity performance.

As an application of second-order voltage-mode all-pass filter, a sinusoidal oscillator producing two-phase signals is

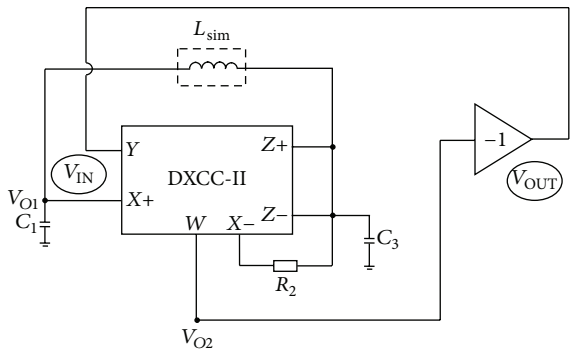

Figure 5: Proposed voltage mode sinusoidal oscillator.

next given. The circuit is shown in Figure 5; it consists of a voltage-mode second-order all-pass filter and a unity gain inverter, with the output of the inverter being fed back to the input of the first stage. It may be noted that the inverter (gain = −1) is realized using DXCC-II itself with input and output at Y and $X-$, respectively. The system loop gain (defined as V_{OUT}/V_{IN}, Figure 5) is given by

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = (-1)\frac{s^2L_{sim}C_1R_2 - 2sL_{sim} + 2R_2}{s^2L_{sim}C_3R_2 + 2sL_{sim} + 2R_2}. \quad (18)$$

If loop gain is set to unity at $s = j\omega$, the circuit shown in Figure 5 can be set to provide two-phase sinusoidal oscillation with oscillation frequency as

$$f_0 = \frac{1}{\Pi\sqrt{2L_{sim}C_3}}. \quad (19)$$

The circuit provides two voltage outputs V_{O1} and V_{O2}. The voltage outputs marked in Figure 5 are related as $V_{O1} = -V_{O2}$.

4. Nonideal Analysis

A nonideal DXCC-II is characterized by the following port relationship:

$$\begin{bmatrix} I_Y \\ I_{Z+} \\ I_{Z-} \\ V_{X+} \\ V_{X-} \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \alpha_p & 0 & 0 & 0 \\ 0 & \alpha_n & 0 & 0 \\ 0 & 0 & \beta_p & 0 \\ 0 & 0 & -\beta_n & 0 \\ 0 & 0 & 0 & \gamma \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_Y \\ V_Z \end{bmatrix}. \quad (20)$$

Here, α_p and α_n are the current transfer gains from $X+$ and $X-$ terminals to $Z+$ and $Z-$ terminals, respectively, β_p and β_n are the voltage transfer gains from Y input terminal to $X+$ and $X-$ terminals, respectively, and γ is the voltage transfer gain from $Z+$ terminal to W terminal (buffered output). However, these transfer gains are close to unity up to very high frequencies [20]. Using (20), the proposed circuits of voltage-mode second-order all-pass filter using simulated inductor as shown in Figures 3(a) and 3(b) are reanalyzed so as to yield the following voltage transfer function:

$$\frac{V_o(s)}{V_i(s)} = k\gamma\frac{s^2\alpha_p\beta_pL_{sim}C_1R_2 - sL_{sim}\beta_n(1+\alpha_n) + R_2\beta_p(1+\alpha_p)}{s^2L_{sim}C_3R_2 + sL_{sim}(1+\alpha_n) + R_2(1+\alpha_p)}, \quad (21)$$

where $k = +1$ for the circuit of Figure 3(a) and $k = -1$ for the circuit of Figure 3(b).

The expressions for pole-ω_0 and Q are given as follows:

$$\omega_0 = \sqrt{\frac{1+\alpha_p}{C_3L_{sim}}}, \qquad Q = \frac{R_2}{1+\alpha_n}\sqrt{\frac{C_3(1+\alpha_p)}{L_{sim}}}. \quad (22)$$

Active and passive sensitivity figures for pole-ω_0 and Q are given as

$$S_{C_3}^{\omega_0} = S_{L_{sim}}^{\omega_0} = -\frac{1}{2}, \quad S_{R_2}^{\omega_0} = 0, \quad S_{\alpha_p}^{\omega_0} = \frac{\alpha_P}{2(1+\alpha_p)}, \quad S_{\alpha_n}^{\omega_0} = 0, \quad S_{R_2}^{Q} = 1, \quad S_{C_3}^{Q} = -S_{L_{sim}}^{Q} = \frac{1}{2}, \quad S_{\alpha_p}^{Q} = \frac{\alpha_p}{2(1+\alpha_p)}, \quad S_{\alpha_n}^{Q} = -\frac{\alpha_n}{1+\alpha_n}. \quad (23)$$

Using (20), the proposed circuits of voltage-mode second-order all-pass filter using frequency transformation as shown in Figures 4(a) and 4(b) are reanalyzed so as to yield the following voltage transfer function:

$$\frac{V_o(s)}{V_i(s)} = k\gamma\frac{s^2\alpha_p\beta_pC_1^2R_1R_4 - 2s\beta_nC_2R_4(1+\alpha_n) + 2\beta_p(1+\alpha_p)}{s^2C_3^2R_3R_4 + 2sC_2R_4(1+\alpha_n) + 2(1+\alpha_p)}, \quad (24)$$

where $k = +1$ for the circuit of Figure 4(a) and $k = -1$ for the circuit of Figure 4(b).

The expressions for pole-ω_0 and Q are given as follows:

$$\omega_0 = \frac{1}{C_3}\sqrt{\frac{2(1+\alpha_p)}{R_3R_4}}, \qquad Q = \frac{C_3}{C_2(1+\alpha_n)}\sqrt{\frac{R_3(1+\alpha_p)}{2R_4}}. \quad (25)$$

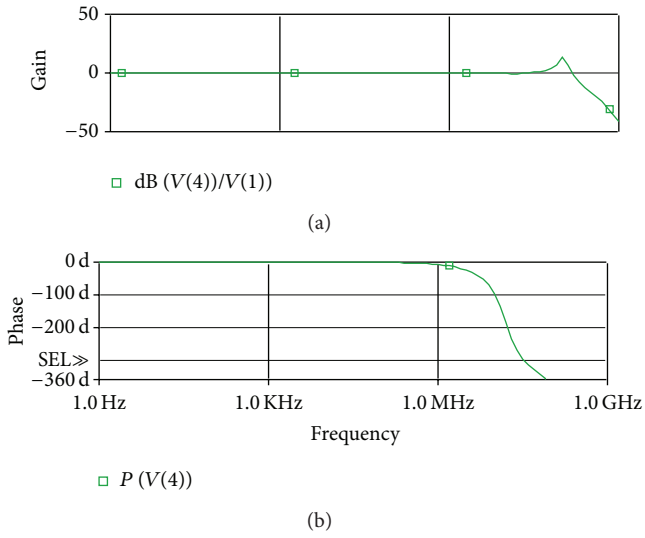

Figure 6: Gain (dB) and phase (deg) response of second-order voltage-mode all-pass filter of Figure 3(a).

Active and passive sensitivity figures for pole-ω_0 and Q are given as

$$S_{C_3}^{\omega_0} = -1, \quad S_{R_3}^{\omega_0} = S_{R_4}^{\omega_0} = -\frac{1}{2}, \quad S_{C_2}^{\omega_0} = 0,$$
$$S_{\alpha_p}^{\omega_0} = \frac{\alpha_p}{2\left(1+\alpha_p\right)}, \quad S_{\alpha_n}^{\omega_0} = 0,$$
$$S_{C_2}^{Q} = -S_{C_3}^{Q} = -1, \quad S_{R_3}^{Q} = -S_{R_4}^{Q} = \frac{1}{2}, \tag{26}$$
$$S_{\alpha_p}^{Q} = \frac{\alpha_p}{2\left(1+\alpha_p\right)}, \quad S_{\alpha_n}^{Q} = -\frac{\alpha_n}{1+\alpha_n}.$$

Equation (22) and (26) shows that the sensitivity figures are all less than or equal to unity in magnitude which implies good sensitivity performance. Sensitivity of filter parameters to current transfer gains will remain less than unity for the ideal value of current transfer gains which is equal to unity.

5. Parasitic Considerations

The next study on the proposed circuits is carried out for the effect of parasitics involved with the used current conveyor. It assumes special significance for evaluating the real performance of any analog circuit. The various parasitics involved with a typical current conveyor [21] are well known to potential readers and will only be reviewed briefly. The various parasitics of the DXCC-II used in the proposed circuits are port Z parasitics in the form of $R_Z//C_Z$, port Y parasitic in the form of $R_Y//C_Y$ and port X parasitics. The proposed circuits are re-analyzed by taking into account the above parasitic effects. A re-analysis of the proposed circuit of voltage-mode second order all-pass filter using simulated inductor as shown in Figure 3(a) yields:

$$\frac{V_o(s)}{V_i(s)} = -\frac{s^2 L_{\text{sim}} C_1' R_2' - 2sL_{\text{sim}} + 2R_2'}{s^2 L_{\text{sim}} C_3' R_2' + 2sL_{\text{sim}} + 2R_2'}, \tag{27}$$

where $R_2' = R_2 + R_{X-}$, $C_1' = C_1 + C_{X+}$, and $C_3' = (C_3 + C_{Z+} + C_{Z-})$.

From (27), it is clear that the parasitic resistances/capacitances merge with the external value. Such a merger does cause slight deviation in circuit's parameters. It can be further observed from (27) that the order of transfer function of second-order all-pass filter is not changed. The modified expressions for pole-$\omega 0$ and Q with parasitic effects are also given as

$$\omega_0 = \sqrt{\frac{2}{C_3' L_{\text{sim}}}}, \tag{28}$$

$$Q = R_2' \sqrt{\frac{C_3'}{2L_{\text{sim}}}}. \tag{29}$$

Next, it is seen from (28) that the pole frequency would slightly be deviated (in deficit) because of these parasitics. The expression showing the effects of parasitics on pole-Q is also given in (29). The pole-Q would also deviate slightly because of the parasitics. The deviation is expected to be small for an integrated DXCC-II.

6. Simulation Results

The new proposed circuits are verified through PSPICE simulations. The simulations are based on 0.5 μm, TSMC, CMOS parameters. Table 2 shows the dimensions of MOS parameters which are used in CMOS implementation of DXCC-II of Figure 1(b). The supply voltages used are ±2.5 V, $V_{BB} = -0.6$ V, $C_C = 0.06$ pF, and $I_B = 25\,\mu$A. The proposed voltage-mode second-order circuit of all-pass filter using simulated inductor has been designed at the pole frequency of 15.92 MHz. For the circuit of voltage-mode second-order all-pass filter (Figure 3(a)) resistance used is $R_2 = 20$ KΩ, capacitors used are of values $C_1 = C_3 = 1$ pF, and, for the resistor less floating simulated inductor, the dimensions of the NMOS transistors are $W/L = 2\,\mu$m/0.5 μm. The bias voltages are selected to be 0.78 V so as to obtain a resistance of 20 kΩ across each one of the MOS transistor. The capacitance C is set to 2 pF so as to realize a floating inductance of 0.2 mH. The gain and phase response of the circuit of Figure 3(a) are shown in Figure 6, which shows the pole frequency as 15.85 MHz with a percentage error of 0.44%. The usefulness of new circuits is to be especially emphasized keeping in view the design frequency which is quite high. The input-output waveforms for voltage-mode second-order all-pass filter are shown in Figure 7. The Fourier spectrum of output is shown in Figure 8. The THD is found to be 1.5% which is also moderately low. The plot of THD variation at output with the amplitude of the input voltage is shown in Figure 9. Furthermore, the circuit of second-order voltage-mode all-pass filter using FDNR (Figure 4(a)) is also simulated.

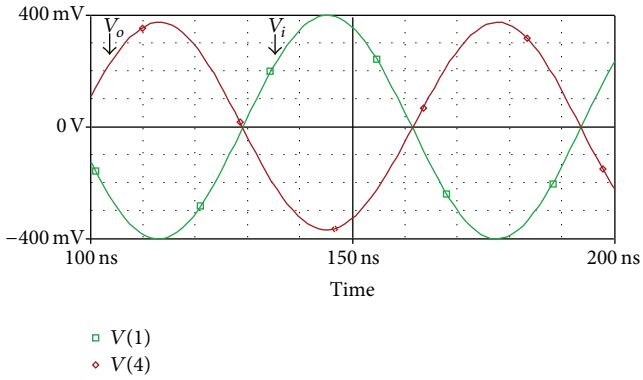

Figure 7: Input/output waveforms at 15.92 MHz.

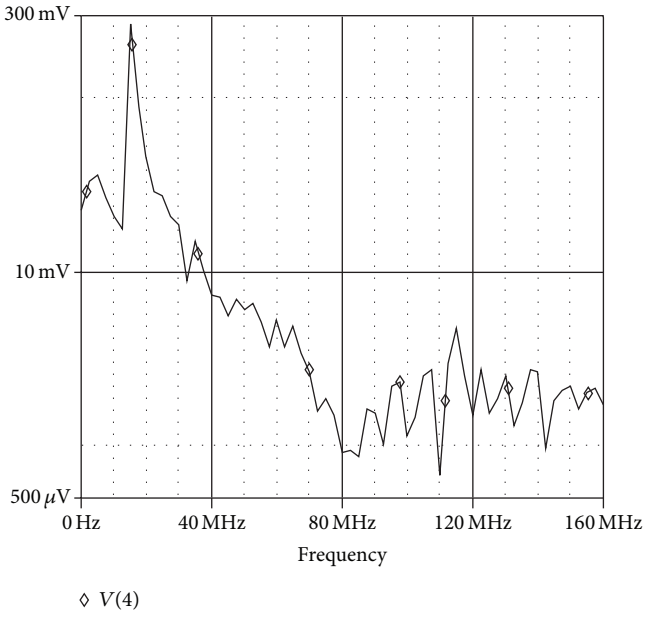

Figure 8: Fourier spectrum of output waveform at 15.92 MHz.

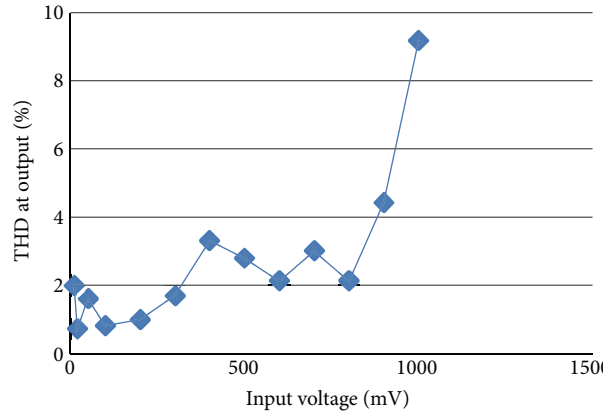

Figure 9: THD variation at output with signal amplitude at 15.92 MHz.

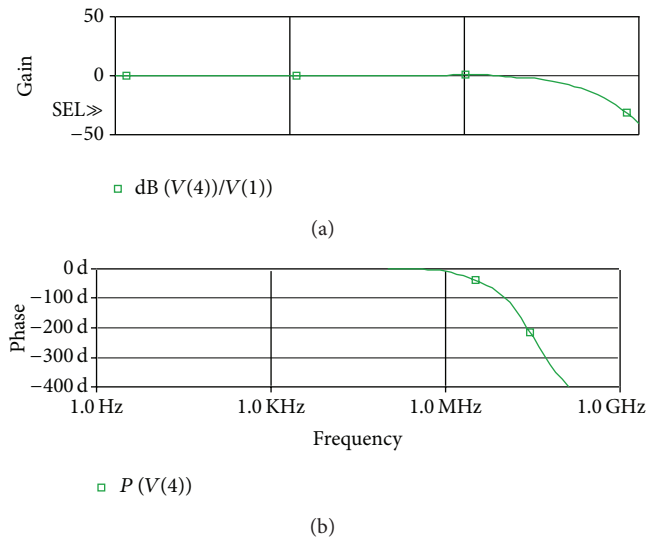

Figure 10: Gain (dB) and phase (deg) response of second-order voltage-mode all-pass filter of Figure 4(a).

The gain and phase response of the circuit of Figure 4(a) are given in Figure 10. The circuit of Figure 4(a) was designed using $C_2 = 10\,\text{pF}$, $R_4 = 4\,\text{k}\Omega$, and, for the realization of resistor less FDNR, the dimensions of the NMOS transistor are selected as $W/L = 4\,\mu\text{m}/1\,\mu\text{m}$. The bias voltage is selected to be 1.2 V so as to obtain a resistance of 1.6 kΩ across the MOS transistor. The capacitances are set as $C_{D11} = C_{D12} = 50\,\text{pF}$ and $C_{D31} = C_{D32} = 50\,\text{pF}$ to realize FDNR1 (D_1) and FDNR3 (D_3), respectively. The theoretical pole frequency used in this design was 25.18 MHz. The simulated pole frequency was found to be 25 MHz, which is very close to the theoretical value and only 0.71% in error.

The Monte Carlo analysis of the second order voltage-mode all-pass filter (Figure 3(a)) was next performed taking 5% Gaussian deviation in the each passive component (C_1, R_2, C_3, and L_{sim}). The analysis was done for 5 runs. The gain and phase response with Monte Carlo analysis is shown in Figure 11 and time domain result for Monte Carlo analysis is shown in Figure 12. As depicted from Monte-Carlo analysis results, the proposed filter has good sensitivity performances.

Table 2: Dimensions of MOS transistors in DXCC-II of Figure 1(b).

Transistors	W (μm)/L (μm)
$M1$, $M2$, $M4$, $M5$, and $M15$–20	4/0.5
$M3$, $M6$–10	8/0.5
$M11$–14	32/0.5
$M21$, $M22$, $M25$, and $M26$	2.5/0.5
$M27$	10/0.5
$M23$, $M24$	50/0.5
$M28$	100/0.5

7. Conclusion

This work presents four additional voltage-mode first-order all-pass filters and second-order all-pass filters with high

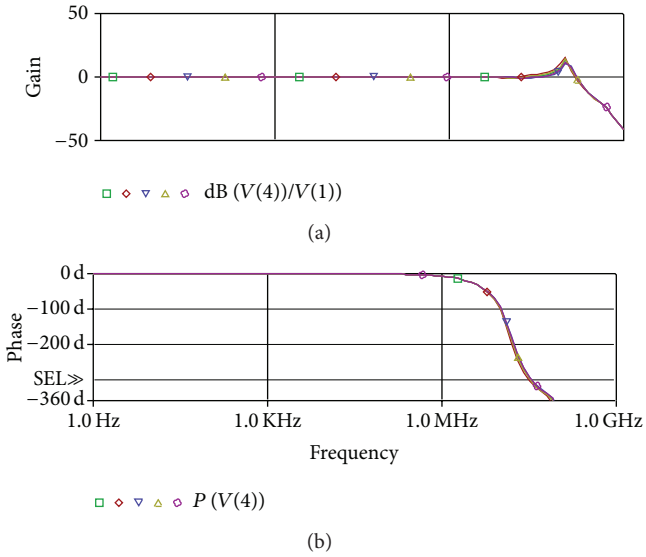

Figure 11: Monte Carlo analysis of Figure 3(a) showing gain (dB) and phase (deg) response.

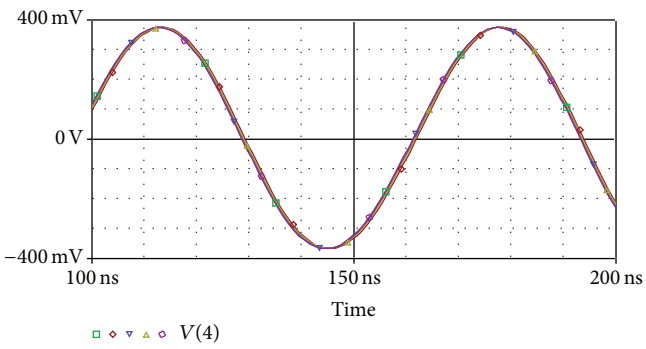

Figure 12: Monte Carlo analysis of Figure 3(a) showing output for 5 runs.

input and low output impedance in each case. The circuits are based on the recently introduced active element, namely, Dual-X Current Conveyor with buffered output. As an application of the second-order voltage-mode all-pass filter, a voltage-mode oscillator configuration is given. Nonideal analysis of the proposed circuits is performed, and parasitic considerations are also discussed. The proposed circuits enjoy good active and passive sensitivities. Simulations results are given to confirm the presented theory.

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