Hindawi Publishing Corporation
Mathematical Problems in Engineering
Volume 2015, Article ID 512471, 11 pages
http://dx.doi.org/10.1155/2015/512471

Research Article

A Hybrid MMC Topology with dc Fault Ride-Through Capability for MTDC Transmission System

Xinhan Meng,[1] Ke-Jun Li,[1] Zhuodi Wang,[1] Wenning Yan,[1] and Jianguo Zhao[2]

[1]*School of Electrical Engineering, Shandong University, Jinan 250061, China*
[2]*State Grid of China Technology College, Jinan 250002, China*

Correspondence should be addressed to Ke-Jun Li; lkjun@sdu.edu.cn

Received 1 April 2015; Revised 18 July 2015; Accepted 21 July 2015

Academic Editor: Ruben Specogna

This paper proposes a hybrid modular multilevel converter (MMC) topology based on mismatched-cascade mechanism. The blocking conditions of different submodule (SM) structures under dc fault are analyzed and a series double submodule is presented. With series-double submodules and mismatched-cascade submodules, the proposed hybrid MMC can ride-through the dc side short-circuit fault and provide an output voltage with the feature of low harmonic content. This hybrid MMC topology can be used in the VSC based multiterminal dc (VSC-MTDC) transmission system. The dc fault ride-through properties of the new structure and the total harmonic distortion (THD) are analyzed compared with the previous full-bridge and clamp-double architectures. An appropriate fault blocking procedure is presented, and a typical four-terminal dc transmission simulation system is given in the power system simulation software. Finally, simulation of steady-state and dc bipolar short-circuit fault verifies that the MTDC system based on this new hybrid MMC topology is stabilized and can block the dc fault and return the nonfault parts to normal.

1. Introduction

With the development of power electronic technology, the voltage source converter (VSC) based on full-controllable electric semiconductor device is widely applied to high voltage direct current transmission field. Compared to the traditional HVDC, VSC based high voltage dc (VSC-HVDC) transmission system has the advantages such as flexible power control, reactive power compensation, supplying power to passive network, and forming multiterminal dc network [1–5]. According to the different structures of voltage source converter, VSC-HVDC can be divided into two kinds: the low level traditional VSC-HVDC and modular multilevel converter based high voltage dc (MMC-HVDC) transmission system. MMC-HVDC is superior to the low level VSC-HVDC in the following aspects: it has lower switching frequency, lower switching loss, and higher scalability; it does not need to switch the serial IGBTs at the same time and can be applied in high voltage occasion. Consequently, it has been rapidly developed for the last few years [6–8].

The present research of VSC-HVDC is mostly focused on half-bridge MMC (HBMMC) and its control strategies. However, half-bridge MMC cannot clear the fault current when dc fault occurs because of the freewheeling diode [9, 10]. At the same time, high power dc current breaker for HVDC applications is not sufficiently mature and cost-effective [11]. So, when dc fault occurs, the common method is to turn off the whole dc system with ac circuit breakers [12]. This approach costs lots of time and reduces the reliability of VSC-HVDC system. To avoid dc fault, cable with low failure rate is used as transmission lines, but this increases the engineering cost and is easily restricted by the working environment. Thus, the present VSC-HVDC technology could hardly be used in long distance or multiterminal dc transmission system [13, 14].

To overcome the shortcomings of traditional MMC, different topologies have been addressed by many scholars. References [15, 16] propose an MMC-HVDC system based on full-bridge MMC (FBMMC) topology. FBMMC can block the fault current when dc fault occurs. However, as too many IGBTs are needed, under the same dc voltage and power level, FBMMC's engineering investment and operation cost is high, which limits its application in engineering practice.

In order to reduce the IGBT used quantity and make the converter capable of blocking dc fault, a new kind of clamp-double MMC (CDMMC) is proposed [14, 17, 18]. When a fault occurs on the dc side, CDMMC turns off IGBTs immediately and utilizes the diode reversed-phase blocking ability to complete the fault handling process. CDMMC needs less semiconductors than FBMMC and also has the ability to block dc fault. However, due to the characteristics of parallel structure, the equivalent capacitance in a bridge arm shows two kinds of states according to the different flows of short-circuit current. So it requires longer time to cut off the short-circuit current, and its dc fault blocking ability is inferior compared with FBMMC [14, 19].

The contribution of this paper is to analyze the equivalent states of various MMC topologies under the dc short-circuit fault and propose an improved MMC topology to improve its performance. Based on the mismatched-cascade mechanism and the principle of dc fault blocking, a hybrid MMC topology which has dc fault ride-through capability and is very suitable for MTDC system is presented. According to the "handshaking method" of MTDC system [20, 21], the process of clearing dc fault and recovering nonfault lines is explained in detail. Finally, a typical four-terminal dc system is introduced and a simulation model is built to verify the system characteristics under the bipolar short-circuit fault which is the most serious dc fault.

This paper is organized as follows: after introduction, the dc fault blocking analysis, which includes analyzing the fault blocking principle and the current paths of different submodules under blocking states, is explained in detail in Section 2. In Section 3, a new topology of hybrid MMC based on the mismatched-cascade mechanism is introduced. In Section 4, a four-terminal dc simulation model is built to explain the application of the new hybrid MMC in MTDC transmission system, including the process to remove the fault lines and recover the nonfault lines under the dc fault. This new hybrid MMC used in MTDC system is tested with the steady-state and dc bipolar short-circuit fault simulations in Section 5. The conclusion of this paper is made in Section 6.

2. Fault Blocking Ability Analysis

2.1. Fault Blocking Principle. An MMC topology consists of two arms per each phase where each arm is comprised of n series-connected submodules and a series-connected inductor. These submodules of each bridge arm can be replaced with an ideal voltage source. After the treatment of presenting network parameter by per-unit value normalization, the equivalent circuit under dc fault state is shown in Figure 1.

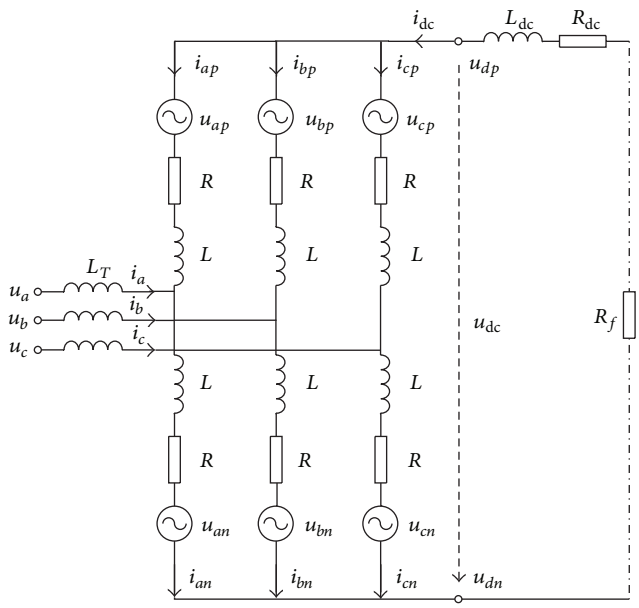

Figure 1: Equivalent circuit under dc fault state.

Considering the upper and lower loops, the dynamics of the converter can be described as follows:

$$u_k - L_T\frac{di_k}{dt} = -L\frac{di_{kp}}{dt} - Ri_{kp} - u_{kp} + u_{dp}$$
$$u_k - L_T\frac{di_k}{dt} = L\frac{di_{kn}}{dt} + Ri_{kn} + u_{kn} + u_{dn}$$

$$i_k = i_{kn} - i_{kp}$$
$$i_{dc} = \sum_k i_{kp} = \sum_k i_{kn}, \tag{1}$$

where $k = a, b, c$ and L, R, and L_T represent the equivalent values of the inductance, resistance, and transformer leakage inductance.

The dynamics of the dc fault current i_{dc} and voltage u_{dc} are expressed as

$$i_{dc} = C_{eq}\frac{d\sum_k u_{kp}}{dt} = C_{eq}\frac{d\sum_k u_{kn}}{dt}$$
$$u_{dc} = u_{dp} - u_{dn} = -L_{dc}\frac{di_{dc}}{dt} - \left(R_{dc} + R_f\right)i_{dc}, \tag{2}$$

where L_{dc} and R_{dc} represent the equivalent values of the dc side inductance and resistance, R_f represents the equivalent value of the short-circuit fault resistance, and C_{eq} represents the equivalent value of the capacitance under the fault state.

Combining these aforementioned equations, the following equation can be obtained:

$$\frac{d^2i_{dc}}{dt^2} + \frac{R_e}{L_e}\frac{di_{dc}}{dt} + \frac{1}{L_eC_e}i_{dc} = 0, \tag{3}$$

where $L_e = 2L/3 + L_{dc}$, $R_e = 2R/3 + R_{dc} + R_f$, and $C_e = 3C_{eq}$.

Thus, the fault equivalent circuit is a second-order oscillated discharging circuit. When dc fault occurs, the dc side fault current can be determined by the derivative of (3) at $t = 0$, which is expressed by

$$i_{dc} = e^{-t/\tau}\left[-\frac{I_{dc0}\omega_0}{\omega}\sin(\omega t - \alpha) - \frac{U_{dc0}}{\omega L_e}\sin(\omega t)\right], \tag{4}$$

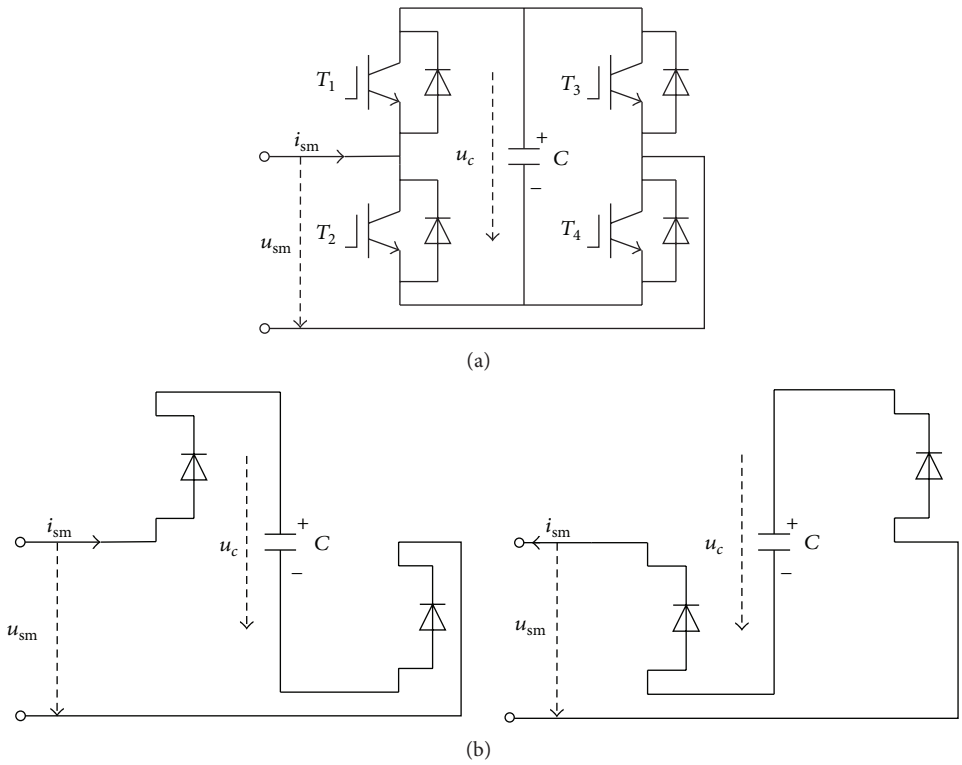

Figure 2: Schematic and block operation mode of FBSM: (a) schematic of FBSM; (b) block operation mode of FBSM.

where I_{dc0} and U_{dc0} are the initial values of i_{dc} and u_{dc}. $\tau = 2L_e/R_e$, $\omega = \sqrt{1/(L_eC_e) - [R_e/(2L_e)]^2}$, $\omega_0 = \sqrt{1/(L_eC_e)}$, and $\alpha = \arctan(\omega\tau)$.

The short-circuit fault current can be calculated by (4). The discharge process before converter blocking is an oscillated discharge procedure which has already known the initial conditions. The equivalent value of the capacitance changes after the converter blocking. If and only if the equivalent capacitor voltage under any circuit state is larger than the ac line voltage amplitude, the short-circuit current can be reduced to zero by the antiparallel diodes. Then, the dc fault would be blocked.

2.2. SM Circuit Topologies under Blocking States

2.2.1. Full-Bridge Submodule. The full-bridge submodule is as shown in Figure 2(a). The control system sends blocking signals to all the IGBTs on the bridge arms when dc fault is found. The path of the short-circuit current is shown in Figure 2(b). The SM's equivalent capacitor voltage after blocking is in the opposite direction with the ac side voltage. Thus, the short-circuit current is blocked from feeding into the converter. However, because a full-bridge submodule needs four IGBTs, the number of required components is doubled to that of the half-bridge submodule needs. So, the full-bridge submodule based MMC is not cost-effective.

2.2.2. Clamp-Double Submodule. The clamp-double submodule, as shown in Figure 3(a), is constituted by two equivalent half-bridge SMs and an IGBT with freewheeling diode. When the dc side fault occurs, the CDSM is switched to the block mode, as shown in Figure 3(b). The equivalent capacitor voltage can stop the fault current from feeding into the converter. However, the equivalent capacitor voltages of a SM are different when the flow of the fault current i_{sm} changes. If $i_{sm} > 0$, the voltage is $2U_c$; otherwise, it turns to be U_c. Correspondingly, the equivalent capacitances are $C_0/2$ and $2C_0$ for each of them separately. Thus, during the dc fault periods, the system charges the SM capacitors repeatedly. This leads to the delay of fault blocking time.

2.2.3. Series-Double Submodule. As the HBSM has the advantages of having simple structure and mature control strategy and being economical, reliable, and efficient, the series-double submodule (SDSM) presented is based on two HBSMs, as shown in Figure 4(a). Between the two HBSMs, there is an IGBT with freewheeling diode to isolate them. SDSM features are economical, reliable, and efficient as HBSM and can block dc fault. Under steady-state operations, the middle IGBT is turned on, and the SDSM is equivalent to two HBSMs in series. At this point, the SDSM's control strategy is simple as the HBSM's. When the dc side fault happens, the control system sends blocking signals to all the IGBTs. As shown in Figure 4(b), no matter how the current flow direction is, the equivalent capacitor voltage of SDSM is $2U_c$, and the voltage direction is opposite to the alternating voltage direction at any moment. So the short-circuit current from the ac system is blocked, and the SDSM based MMC has the dc fault ride-through capability.

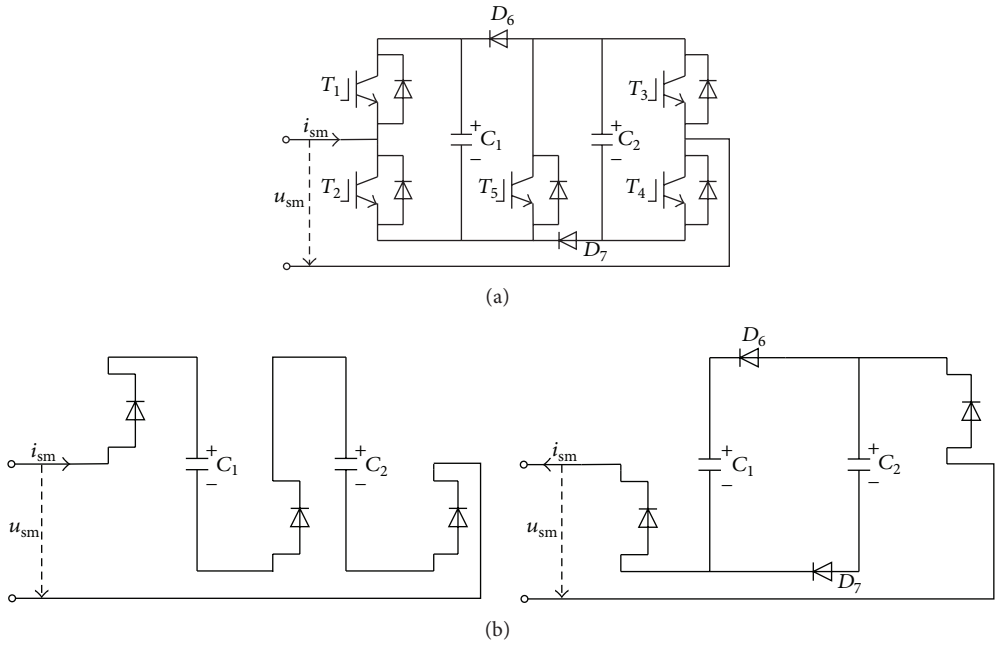

Figure 3: Schematic and block operation mode of CDSM: (a) schematic of CDSM; (b) block operation mode of CDSM.

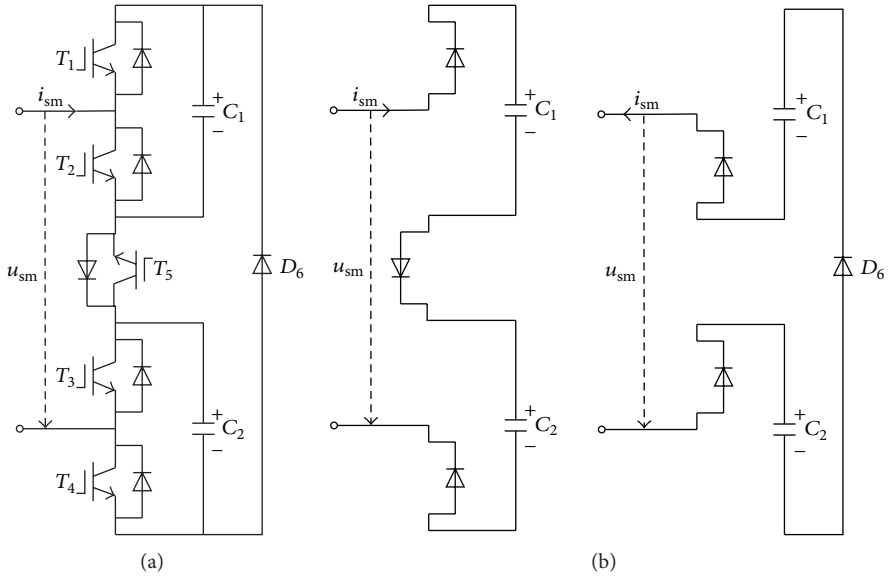

Figure 4: Schematic and block operation mode of SDSM: (a) schematic of SDSM; (b) block operation mode of SDSM.

As shown in Table 1, SDMMC needs less semiconductors and has the same dc fault blocking capability compared to FBMMC. As for CDMMC, due to the characteristics of parallel structure, the equivalent capacitance in a bridge arm shows two kinds of states according to the different flows of short-circuit current, as shown in Figure 3(b). So it requires longer time to cut off the short-circuit current, and its dc fault blocking ability is inferior compared with FBMMC and SDMMC. The comparison of dc fault blocking time of various MMC configurations is shown in Figure 5. In consideration of the number of semiconductors used and power losses, SDMMC is better than FBMMC. Power losses are represented by the estimated power losses, which is the ratio of converter's losses (primarily the IGBT switching losses) and the rated capacity of MMC. Among these, the switching losses are calculated by the on-off time and the single switch loss of IGBT. The estimated power losses in Table 1 are under the circumstances when N is equal to 10. So SDSM is a kind of good submodule topology applied into MMC structure with dc fault ride-through capability.

Also, SDSM has a weakness as well as these advantages above. When all the IGBTs are blocked, the semiconductors

Table 1: Comparison of the MMC configurations with various SMs.

Features	Half-bridge MMC	Full-bridge MMC	Clamp-double MMC	Series-double MMC
SM circuit	HBSM	FBSM	CDSM	SDSM
dc fault blocking capability	×	√	√	√
Blocking time	×	18 ms	24 ms	18 ms
Number of SMs per arm	$2N$	$2N$	N	N
Number of IGBTs per arm	$4N$	$8N$	$5N$	$5N$
Number of diodes per arm	$4N$	$8N$	$7N$	$6N$
Number of capacitors per arm	$2N$	$2N$	$2N$	$2N$
Voltage levels	$2N + 1$	$2N + 1$	$2N + 1$	$2N + 1$
Estimated power losses	0.69%	0.96%	0.83%	0.83%

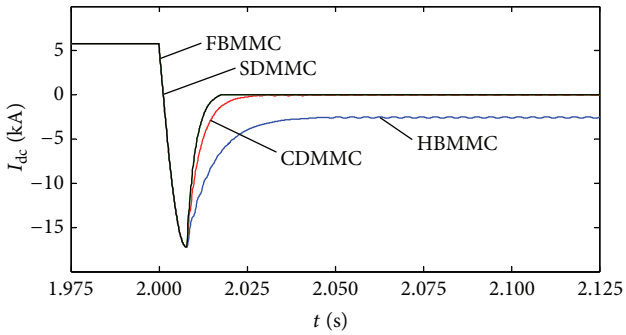

Figure 5: dc fault blocking time of various MMC configurations.

T_5 and D_6 need to support doubling the blocking voltage (i.e., $2U_c$). So the related semiconductors (T_5 and D_6) need a special design to overcome this larger voltage than other ones. A common method is to be realized by series connection of two semiconductors. In this instance, the number of IGBTs per arm needed by SDMMC is increased from $5N$ to $6N$. It is a little more than CDMMC needed, but still less than FBMMC used. So the power losses produced by SDMMC (T_5 is replaced by the series connection of two semiconductors) are less than FBMMC but are a little more than CDMMC. However, as shown in Figure 5 and Table 1, SDMMC is better than CDMMC in dc blocking time. It will save 25% time than the CDMMC to block the dc fault. Consequently, in consideration of the double blocking voltage problem, the proposed SDMMC still has its special advantages compared with other MMC configurations.

3. Topology of Mismatched-Cascade Mechanism Based Hybrid MMC

3.1. Application of Mismatched-Cascade Mechanism. Mismatched-cascade mechanism can be used to improve the quality of step wave. Firstly, it produces a small range of dislocations to the basic waveform. Secondly, it stacks these mismatched waveforms to produce a more meticulous waveform. Mismatched-cascade mechanism based MMC is constituted by adding a mismatched-cascade submodule (MCSM) to the former structure. The MCSM is formed by connecting some half-bridge units in series, as shown in Figure 6.

m represents the number of half-bridge units in an MCSM. U_{mc} represents the nominal voltage of the half-bridge unit capacitor, and it must be restricted as

$$U_{mc} = \frac{U_c}{m+1}. \tag{5}$$

When $n = 4$, $m = 2$, for example, then $U_{mc} = U_c/3$; the output voltage waveform in the effect of MCSM and the switching mode of SMs are shown separately in Figure 7 and Table 2. As the upper and lower bridges are symmetrical, the output voltage waveform only considers the condition of $u_a > 0$.

When the number of half-bridge units in upper bridge's MCSM is $m_p = 1$, correspondingly, the number of half-bridge units in lower bridge's MCSM is $m_n = 1$; the output voltage waveform remains precisely unchanged. However, when m_p increases and m_n decreases, on the contrary, the output voltage levels can produce small dislocations, as shown in Figure 7. The FFT analysis demonstrates that the output voltage has a better quality (THD is changed from about 12% to 4%) after the MCSMs are added to the MMC structure.

After the MCSM applied, the number of output voltage levels is changed from $(n + 1)$ to N_{out}:

$$N_{out} = (n+1)(m+1). \tag{6}$$

When $n = 20$, $m = 2$, for example, the number of output voltage levels will be changed from 21 to 63 after the MCSM applied. And the voltage total harmonic distortion (THD) under different modulation ratio k is shown in Figure 8.

Thus, it can be observed that only an MCSM is needed to increase the number of output voltage levels several times over, and the structure of MMC is not changed sharply. This will reduce the harmonic content of output waveform largely.

3.2. Topology of Hybrid MMC. Based on the fault blocking principle shown in Section 2 and the mismatched-cascade mechanism shown above, a hybrid MMC topology is presented here. As stated above, HBSM has the advantages of having simple structure and mature control strategy and being economical, reliable, and efficient. SDSM has the dc fault ride-through capability. And MCSM can optimize

Table 2: Switching mode of SMs under different output states.

Number of SMs switched		Number of HBSMs switched in MCSM		Output voltage
Upper bridge	Lower bridge	Upper bridge	Lower bridge	
2	2	1	1	0
2	2	0	2	U_{mc}
1	3	2	0	$2U_{mc}$
1	3	1	1	$3U_{mc}$
1	3	0	2	$4U_{mc}$
0	4	2	0	$5U_{mc}$
0	4	1	1	$6U_{mc}$
0	4	0	2	$7U_{mc}$

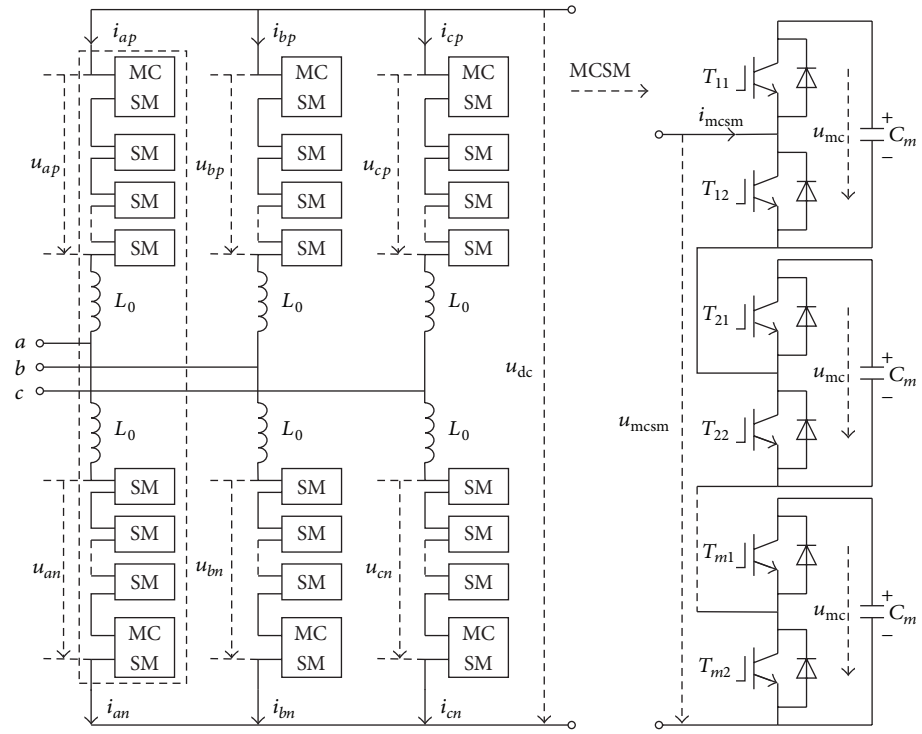

Figure 6: Topology structure of mismatched-cascade based MMC.

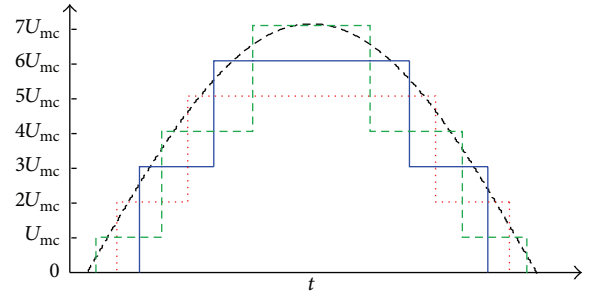

Figure 7: Schematic diagram of voltage waveform in the effect of MCSM.

the quality of output voltage waveform. So it is considered to connect them to build a hybrid MMC which has all these advantages. In the hybrid MMC, N_S represents the minimum number of SDSMs which a bridge arm needed. Considering the constraint conditions of dc fault blocking, the equivalent capacitor voltage must be larger than the reversed alternating voltage at any moment. So N_S must follow the principle as follows:

$$N_S \geq \frac{\sqrt{3}U_m}{4U_c}, \tag{7}$$

where U_m represents the maximum value of ac side phase voltage and U_c represents the voltage of a single capacitor in SDSM. On equal conditions, the reverse voltage is larger when N_S increases, and so the blocking time needed is shorter. Thus, the hybrid MMC needs more time to block the dc fault than the MMC made up by SDSM only. To balance dc fault blocking capacity and economical efficiency, under the premise of meeting the requirement of fault blocking time, the number of SDSMs will be decreased as much as possible.

Table 3: dc fault clearing time in different combinations of N_H and N_S.

Scheme	N_H	N_S	dc fault blocking time/ms	Number of IGBTs used in a single-bridge arm	THD	Efficiency of each scheme	Estimated power losses
1	12	4	25	44	0.04	0.477	0.79%
2	8	6	16	46	0.04	0.457	0.79%
3	4	8	12	48	0.04	0.438	0.79%

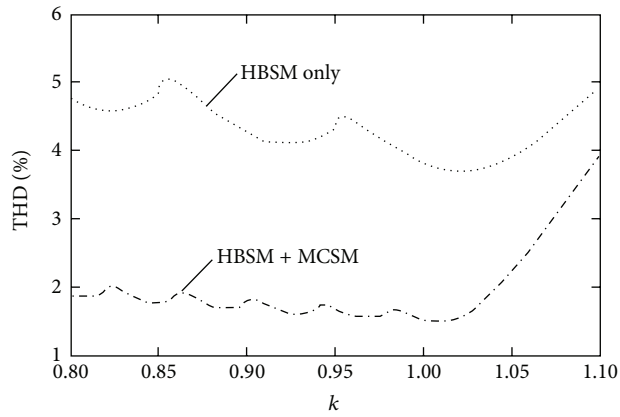

Figure 8: The voltage THD changed after the MCSM applied.

Here N_H is defined to represent the number of HBSMs on a bridge arm, and N_S is the number of SDSMs used. When the total voltage level number N_P is fixed, N_H and N_S should follow the principle as follows:

$$N_H + 2N_S + 1 = N_P. \tag{8}$$

To determine the appropriate proportional relation of the number of HBSMs and SDSMs, a simulation model for hybrid MMC was built in PSCAD/EMTDC, and the dc fault blocking time in different combinations of N_H and N_S was measured as shown in Table 3.

As the SDSM is constituted by two HBSMs, and the middle IGBT is turned on under steady-state operations, the SDSM is equivalent to two HBSMs in series. So the THDs and the estimated power losses of schemes 1~3 are almost equal. The efficiency of each scheme means each IGBT's contribution to the total output levels. It is the ratio of the output levels and the number of IGBTs used in a single-bridge arm. From Table 3, it can be observed that scheme 1 has the highest efficiency among all the three schemes since the blocking time is the longest too. However, as all the blocking time is less than 30 ms which is short enough to block the fault, scheme 1 is able to meet the dc fault blocking time requirement when the target is not too strict. Under such circumstances, the required number of IGBTs is suitable, and the hybrid MMC based transmission project is economical.

When MCSM is added, the total voltage level number would be changed from N_P to N'_P. N_M is defined to represent the number of half-bridge units in an MCSM. Then, N'_P should be processed as

$$N'_P = (N_H + 2N_S + 1) \times (N_M + 1). \tag{9}$$

This means that the output voltage level number is increased several times over when adding MCSM to the hybrid MMC.

4. Application of Hybrid MMC in MTDC Transmission System

The multiterminal direct current (MTDC) transmission system can be divided into series, parallel, and hybrid forms, by the different connection modes. Parallel connection mode is the most popular one owing to its characteristics of simplicity, flexibility, and expandability [5]. In this section, a typical parallel four-terminal direct current transmission system is utilized to analyze the procedure of the hybrid MMC-MTDC transmission system blocking dc side fault.

Reference [20] proposes a "handshaking method" and its procedure to deal with the dc fault in two levels' VSC-MTDC transmission system. Using this method, the voltage stability and power recovery after failure can be insured. However, as circuit breakers are needed to cut off the short-circuit current from ac side, the time required to block the fault and recover the rest is too long. Meanwhile, the hybrid MMC presented has the dc fault ride-through capability by itself, so the hybrid MMC based MTDC transmission system can process the dc fault much faster.

As is shown in Figure 9, hybrid MMC is applied in this four-terminal MTDC. $S_1 \sim S_8$ are the disconnecting switches in each dc transmission line. Based on this system, the process of the presented hybrid MMC-MTDC removing the fault lines and recovering the nonfault lines under dc side fault is as follows.

Step 1. Each converter monitors the dc side bus voltage and current in real time. Using the dc fault detection method [20, 21], and combined with the system parameters, the control system is able to acquire when the dc fault occurs and which kind of it.

Step 2. After the dc fault is detected, according to the changes of current, voltage, and power flow at the dc side bus of each MMC, the potential fault lines can be detected [22].

Step 3. The disconnecting switches in the potential fault lines are marked, so that the fault lines can be isolated after the dc fault blocking.

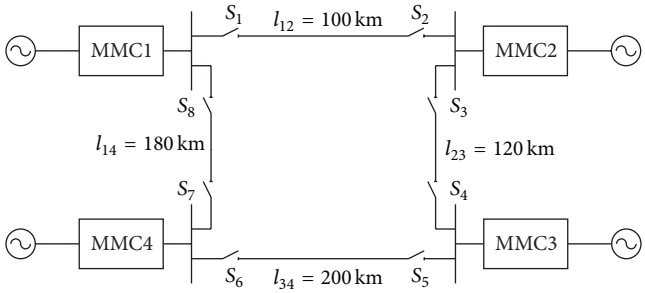

Figure 9: Structure of four-terminal MMC-MTDC system.

Step 4. Blocking signals are sent to the SMs which have the dc fault ride-through capability in the hybrid MMC. At the same time, all the by-pass switches paralleled with other SMs are turned on to protect the semiconductor devices in them. Considering the delay time of detecting fault and blocking IGBTs, the time needed for MMC to deal with the dc fault is within 5~10 ms.

Step 5. The disconnecting switches marked in Step 3 are turned off. According to the simulation results and the dc fault clearing time listed in Table 3, the switches should be disconnected at about 30 ms after the converters receive blocking signals.

Step 6. The control system sends unblocking signals to the converters to unblock all the IGBTs in MMC and turns off the by-pass switches in Step 4.

Step 7. The converters are set to run in constant dc voltage control mode until the dc bus voltage increases to its rated value. At the moment, the disconnecting switches in the potential fault lines measure the voltages on their both sides. If the voltage difference is less than a certain value, the switch would close itself.

Step 8. After the switches in the nonfault lines closed, all of the converters are set to their original modes. And then, the fault line is isolated and the nonfault lines are returned to service. The hybrid MMC-MTDC transmission system reaches a new steady state under the presupposed operating conditions.

5. Simulation Analysis

To verify the reliability of the represented hybrid MMC-MTDC transmission system and its capability to block dc fault, a four-terminal MTDC simulation model is built in PSCAD/EMTDC. Where MMC1 uses the constant dc voltage and ac voltage control mode, MMC2 adopts the dc voltage drop and constant ac voltage control mode; both MMC3 and MMC4 take the constant active and reactive power control mode. Each bridge arm in hybrid MMC is consisted by 12 HBSMs, 4 SDSMs, and 1 MCSM, and an MCSM is made up by 4 half-bridge units. According to (9), the maximum number of output voltage levels is changed from 21 to 105 after MCSM added. It reduces the harmonic content of output waveform immensely.

The parameters of this hybrid MMC-HVDC simulation system are listed in Table 4. The power direction flows into the converter are set as positive. The converter transformers adopt the YNd11 connection scheme. The converters are connected by high voltage direct current cable, and the unit of distance impedance is 0.01 Ω/km.

5.1. Steady-State Simulation and Analysis. When the hybrid MMC-MTDC transmission system is under the steady-state operation, the active power of MMC3 is changed from 50 MW to 80 MW and the active power of MMC4 is changed from 100 MW to 50 MW at 0.6 seconds. The active power of MMC3 is changed from 80 MW to 100 MW and the active power of MMC4 is turned from 50 MW to −50 MW at 0.8 seconds. The reactive power of MMC4 is turned from −50 Mvar to 50 Mvar at 1.0 second. The active power of MMC3 and MMC4 is resumed to 80 MW and 100 MW at 1.2 seconds. The simulation waveforms are shown in Figure 10.

As shown in Figure 10, since MMC1 adopts the constant dc voltage control mode and the power change is within the adjustable range, the active power imbalance is compensated by MMC1 at the time of 0.6 seconds. The active power of MMC4 is changed significantly at the time of 0.8 seconds and the power flow turns to the opposite direction. According to the dc voltage control mode of MMC2, both MMC1 and MMC2 are needed to compensate the active power and stabilize the dc voltage. Meanwhile, the dc voltage of MMC4 is changed from slightly larger to less than 400 kV, so that MMC4 can absorb the active power from the system. At the time of 1.0 second, the reactive power of MMC4 changes from −50 Mvar to 50 Mvar and the dc voltage of MMC4 tends towards stability after a slight oscillation. During this process, the other converters' dc voltages always keep stable. It means that the change of reactive power rarely has influence on the stability of the dc system. At the time of 1.2 seconds, the power of MMC3 and MMC4 recovered, so MMC1 and MMC2 changed their output to maintain the system stability. During the whole process, after the changes of parameters, the system restores to a steady state within a short time (less than 50 ms), and the fluctuation is within ±1%. All of these indexes meet the requirements of the system stability.

5.2. Simulation of the DC Bipolar Short-Circuit Fault. To verify the capability of the new hybrid MMC-MTDC under dc side fault and analysis of the characteristic of nonfault lines' recovery, a dc fault in lines 1-2 close to MMC1 is set at the time of 2 seconds. The dc fault can be divided into three kinds: monopolar grounding fault, tripping fault, and bipolar short-circuit fault. In all the three kinds of dc faults, the bipolar short-circuit fault causes the most serious effect [23]. So, to make the focal points stand out, only bipolar short-circuit fault is simulated and analyzed in this section. Combined with the control strategy presented in Section 4, a hybrid MMC based four-terminal dc transmission system is built in PSCAD/EMTDC, and the waveforms of fault state simulation are shown in Figure 11.

Table 4: Parameters of the hybrid MMC-HVDC simulation system.

Parameters	MMC1	MMC2	MMC3	MMC4
Rated capacity of MMC	400 MVA	300 MVA	100 MVA	100 MVA
ac bus voltage	220 kV	220 kV	110 kV	110 kV
dc bus voltage	±200 kV			
Rated capacity of transformer	400 MVA	320 MVA	120 MVA	120 MVA
Ratio of transformer	220 kV/230 kV		110 kV/230 kV	
Leakage reactance	0.1 pu			
Bridge arm reactance	32 mH	55 mH	165 mH	165 mH
HBSMs' number	12			
SDSMs' number	4			
MCSMs' number	1			
SM capacitance	3400 μF	2550 μF	850 μF	850 μF

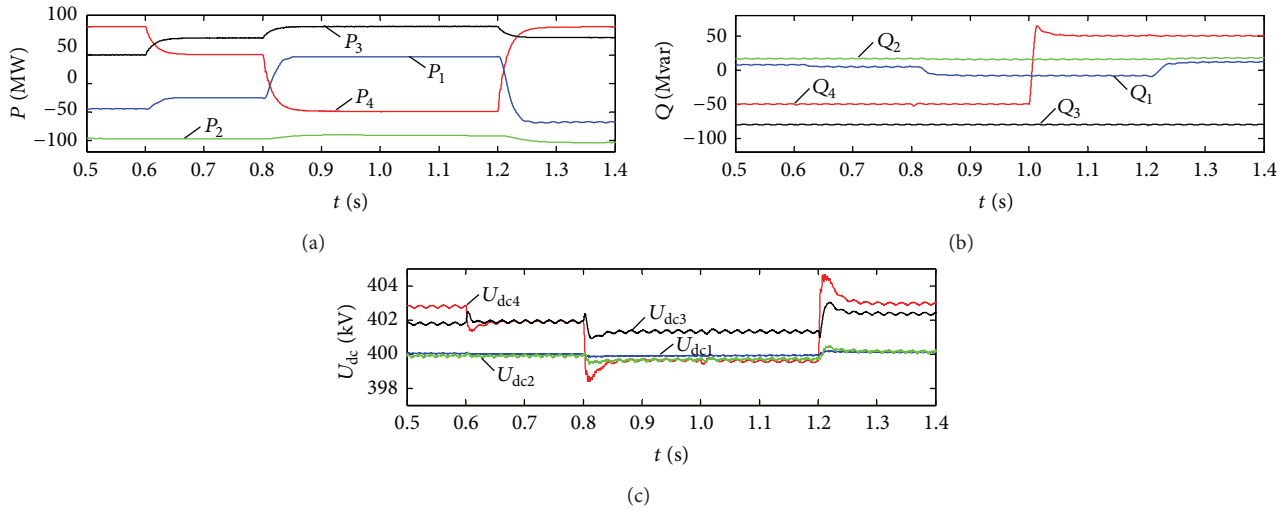

Figure 10: Waveforms of steady-state simulation: (a) active power variations; (b) reactive power variations; (c) dc voltage variations.

As shown in Figures 11(a) and 11(b), after the dc fault occurs, the hybrid MMC blocks itself; then the active power and reactive power reduce to zero within 35~40 ms. When the converter is unblocked, the dc voltage recovers to 400 kV; then the active power and reactive power turn to their new steady states. Due to the fact that the fault lines have been isolated and that the system network parameters have been changed, the transmission power of MMC1 and MMC2 changes from the original state to a new steady state.

As shown in Figures 11(c) and 11(d), after the dc fault occurs, the fault current increases sharply and the dc voltage falls off due to the capacitor discharge and the ac side through fault current. Then, the control system sends blocking signals to block the hybrid MMC. After blocking, the capacitor voltage stops the ac current from flowing into the dc side. Then, the short-circuit current and dc voltage go down to zero, respectively. After that, the disconnecting switches are turned off, and unblocking signals are sent to the converters. At the same time, all the converters are set to run in constant dc voltage control mode until the dc bus voltages increase to their rated values. At this moment, the disconnecting switches in the nonfault lines detect the voltage differences are less than the set value and close themselves. At last, all the converters are set to their original modes and i_{dc} rises to a new steady value.

As shown in Figures 11(e) and 11(f), the SMs' voltages stay near the rated voltage value 20 kV. So, after the fault line is removed, there is no need to charge the capacitors in the SMs again, and then the recovery time will not be too long.

As shown in Figures 11(g) and 11(h), the ac side current decreases to zero during the blocking time and recovers to the steady value when the system is put into operation again. During this process, there is no off-limit condition, and the ac voltage variation is less than 5%. So, all the results indicate that the dc fault can hardly influence the ac system and the new hybrid MMC-MTDC transmission system is stable during the fault process.

6. Conclusions

In this paper, the mismatched-cascade mechanism and dc fault blocking principle are implemented in a hybrid MMC topology. Firstly, the dc fault blocking principle and different topologies of submodules are presented to analyse the fault

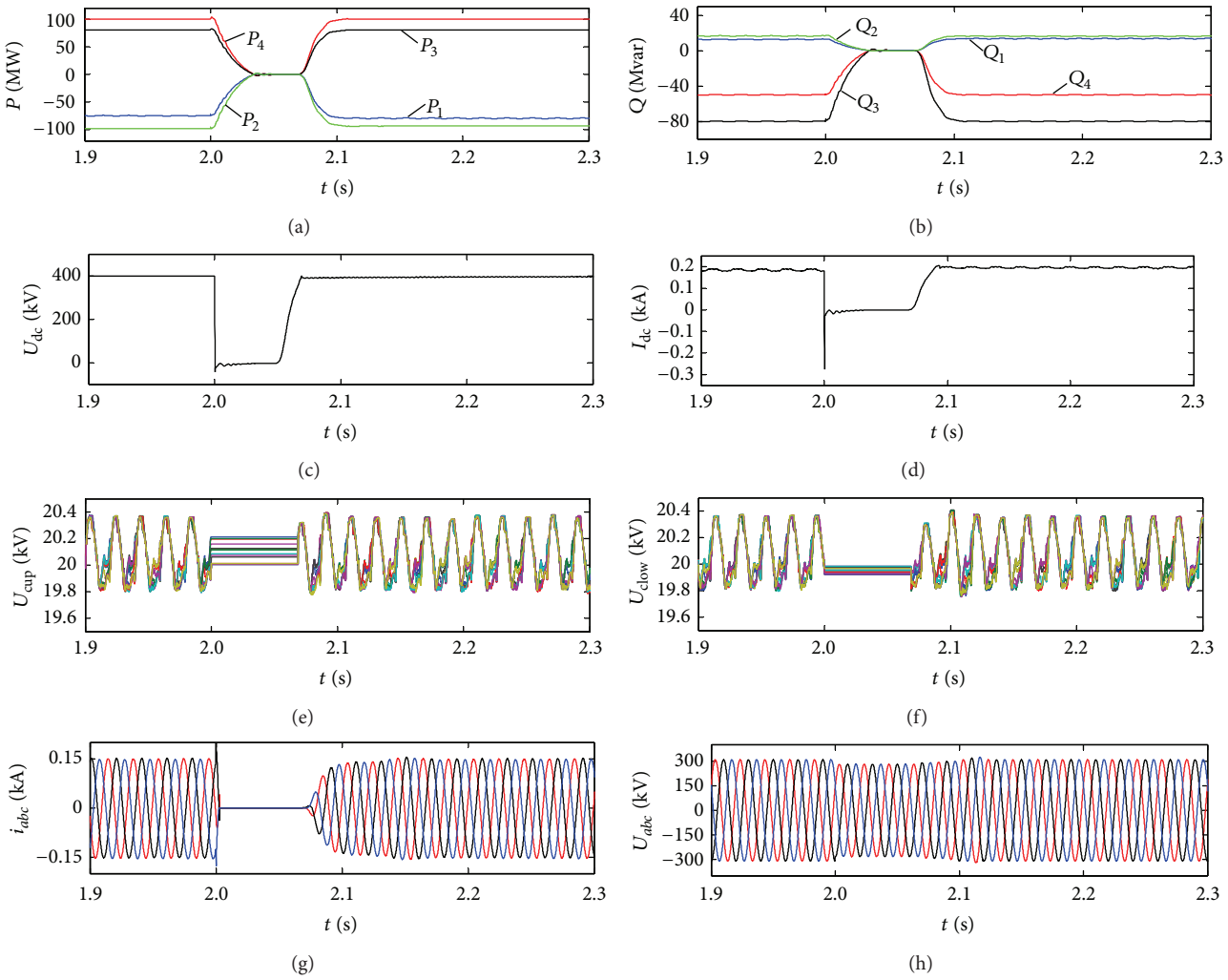

FIGURE 11: Waveforms of fault state simulation: (a) and (b) active and reactive power variations; (c) and (d) dc voltage and current of MMC1; (e) and (f) upper and lower bridge SM capacitor voltages; (g) and (h) ac side three-phase voltage and current of MMC1.

ride-through capability. A new kind of series-double submodule is proposed. Based on this submodule, the MMC can block dc fault and the number of semiconductor devices is reduced. A new hybrid MMC topology constituted by half-bridge SM, series-double SM, and mismatched-cascade SM is proposed. The effect of this kind of MMC to block dc fault is verified by simulation in PSCAD/EMTDC. Then, an MTDC transmission system based on this hybrid MMC and its process to remove the fault lines and recover the nonfault lines are presented. Finally, a four-terminal dc simulation model is built. Based on this model, both steady state and fault state are analyzed by simulations. According to test results, it is shown that dc system based on this new kind of hybrid MMC can block the dc fault accurately and quickly. And the nonfault parts can be restored to normal operation. With the fault blocking ability and feasible control strategy, this hybrid MMC presented can be applied into connecting the renewable source to power grid and forming multiterminal dc network.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the republication of this paper.

References

[1] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: an overview," *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 592–602, 2009.

[2] Y. Wei, Q. He, Y. Sun, Y. Sun, and C. Ji, "Improved power flow algorithm for VSC-HVDC system based on high-order Newton-type method," *Mathematical Problems in Engineering*, vol. 2013, Article ID 235316, 10 pages, 2013.

[3] N. R. Chaudhuri, R. Majumder, B. Chaudhuri, and J. Pan, "Stability analysis of VSC MTDC grids connected to multimachine AC systems," *IEEE Transactions on Power Delivery*, vol. 26, no. 4, pp. 2774–2784, 2011.

[4] S. Cole, J. Beerten, and R. Belmans, "Generalized dynamic VSC MTDC model for power system stability studies," *IEEE Transactions on Power Systems*, vol. 25, no. 3, pp. 1655–1662, 2010.

[5] O. Gomis-Bellmunt, J. Liang, J. Ekanayake, R. King, and N. Jenkins, "Topologies of multiterminal HVDC-VSC transmission for large offshore wind farms," *Electric Power Systems Research*, vol. 81, no. 2, pp. 271–281, 2011.

[6] R. Marquardt, "Modular multilevel converter: an universal concept for HVDC-networks and extended dc-bus-applications," in *Proceedings of the International Power Electronics Conference*, pp. 502–507, Sapporo, Japan, June 2010.

[7] J. Dorn, H. Huang, and D. Retzmann, "A new multilevel voltage-sourced converter topology for HVDC applications," in *Proceedings of the Conference International des Grands Reseaux Electriques*, pp. 1–8, Paris, France, 2008.

[8] R. José, L. G. Franquelo, K. Samir et al., "Multilevel converters: an enabling technology for high-poer applications," *Proceedings of the IEEE*, vol. 97, no. 11, pp. 1786–1817, 2009.

[9] P. Bordignon, M. Marchesoni, G. Parodi, and L. Vaccaro, "Modular multilevel converter in HVDC systems under fault conditions," in *Proceedings of the 15th European Conference on Power Electronics and Applications*, pp. 1–10, Lille, France, September 2013.

[10] X. Chen, C. Zhao, and C. Cao, "Research on the fault characteristics of HVDC based on modular multilevel converter," in *Proceedings of the IEEE Electrical Power and Energy Conference (EPEC '11)*, pp. 91–96, Winnipeg, MB, Canada, October 2011.

[11] C. M. Franck, "HVDC circuit breakers: a review identifying future research needs," *IEEE Transactions on Power Delivery*, vol. 26, no. 2, pp. 998–1007, 2011.

[12] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, and L. Li, "Protection of nonpermanent faults on DC overhead lines in MMC-based HVDC systems," *IEEE Transactions on Power Delivery*, vol. 28, no. 1, pp. 483–490, 2013.

[13] F. Chang, Z. Yang, Y. Wang, F. Lin, and S. Liu, "Fault characteristics and control strategies of multiterminal high voltage direct current transmission based on modular multilevel converter," *Mathematical Problems in Engineering*. In press.

[14] T. Modeer, H.-P. Nee, and S. Norrga, "Loss comparison of different sub-module implementations for modular multilevel converters in HVDC applications," in *Proceedings of the 14th European Conference on Power Electronics and Applications (EPE '11)*, pp. 1–7, Birmingham, UK, September 2011.

[15] C. Zhao, J. Xu, and T. Li, "DC faults ride-through capability analysis of full-bridge MMC-MTDC system," *Science China Technological Sciences*, vol. 56, no. 1, pp. 253–261, 2013.

[16] R. Marquardt, "Modular multilevel converter topologies with DC-short circuit current limitation," in *Proceedings of the 8th IEEE International Conference on Power Electronics and ECCE Asia (ICPE & ECCE '11)*, pp. 1425–1431, IEEE, Jeju, Republic of Korea, May-June 2011.

[17] D. R. Trainer, C. C. Davidson, C. D. M. Oates, N. M. Macleod, D. R. Critchley, and R. W. Crookes, "A new hybrid voltage sourced converter for HVDC power transmission," in *Proceedings of the Conference International des Grands Reseaux Electriques*, pp. 1–12, Paris, France, 2010.

[18] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, D. R. Critchley, and R. W. Crookes, "A new hybrid multi-level voltage-source converter with DC fault blocking capability," in *Proceedings of the 9th IET International Conference on AC and DC Power Transmission (ACDC '10)*, pp. 1–5, London, UK, October 2010.

[19] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits," *IEEE Transactions on Power Delivery*, vol. 30, no. 1, pp. 385–394, 2015.

[20] L. Tang and B.-T. Ooi, "Locating and isolating DC faults in multi-terminal DC systems," *IEEE Transactions on Power Delivery*, vol. 22, no. 3, pp. 1877–1884, 2007.

[21] J. Yang, J. E. Fletcher, and J. O'Reilly, "Short-circuit and ground fault analyses and location in VSC-based DC network cables," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3827–3837, 2012.

[22] L. Tang and B.-T. Ooi, "Protection of VSC-multi-terminal HVDC against DC faults," in *Proceedings of the IEEE 33rd Annual Power Electronics Specialists Conference (PESC '02)*, vol. 2, pp. 719–724, June 2002.

[23] D. Schmitt, Y. Wang, T. Weyh, and R. Marquardt, "DC-side fault current management in extended multiterminal-HVDC-grids," in *Proceedings of the 9th International Multi-Conference on IEEE Systems, Signals and Devices*, pp. 1–5, Chemnitz, Germany, March 2012.