Research Article

Superior Antireflection Coating for a Silicon Cell with a Micronanohybrid Structure

Hsi-Chien Liu[1] and Gou-Jen Wang[1,2,3]

[1] Department of Mechanical Engineering, National Chung Hsing University, Taichung 40227, Taiwan
[2] Graduate Institute of Biomedical Engineering, National Chung Hsing University, Taichung 40227, Taiwan
[3] Program in Tissue Engineering and Regenerative Medicine, National Chung Hsing University, 250 Kuo-Kuang Road, Taichung 40227, Taiwan

Correspondence should be addressed to Gou-Jen Wang; gjwang@dragon.nchu.edu.tw

The object of this paper is to develop a high antireflection silicon solar cell. A novel two-stage metal-assisted etching (MAE) method is proposed for the fabrication of an antireflective layer of a micronanohybrid structure array. The processing time for the etching on an N-type high-resistance (NH) silicon wafer can be controlled to around 5 min. The resulting micronanohybrid structure array can achieve an average reflectivity of 1.21% for a light spectrum of 200–1000 nm. A P-N junction on the fabricated micronanohybrid structure array is formed using a low-cost liquid diffusion source. A high antireflection silicon solar cell with an average efficiency of 13.1% can be achieved. Compared with a conventional pyramid structure solar cell, the shorted circuit current of the proposed solar cell is increased by 73%. The major advantage of the two-stage MAE process is that a high antireflective silicon substrate can be fabricated cost-effectively in a relatively short time. The proposed method is feasible for the mass production of low-cost solar cells.

1. Introduction

Solar cells are powered by the photoelectric conversion of solar light. Thus, it is desirable that the light reflectance of the cell surface be as low as possible to enable complete absorption of the solar energy. Current antireflection approaches can be categorized into two categories. The first approach is to coat an antireflection layer on the cell surface to reduce light reflection. Plasma enhanced chemical vapor deposition (PECVD) of a thin layer of hydrogenated silicon nitride (SiNx:H) on the cell surface is a commonly adopted method [1]. Solar light within a specific wave range can thus be effectively absorbed. Wider spectrum absorption requires multiple antireflection coatings. Hence, the antireflection coating approach is relatively costly, complicated, and difficult to mass produce. The other approach is to texturize the cell surface so that different wavelengths of light can be efficiently absorbed through multiple reflections. This approach enables a wider spectrum of solar light to reach the

P-N junction of the solar cell, thus enhancing its short circuit current and photoelectric conversion efficiency.

In recent years, physical and chemical etching methods have been adopted for roughening the surface of the wafer substrate. Physical etching can be accomplished by reactive ion etching and creates a rough structure that possesses less than 20% reflectivity in the visible light spectrum [2]. The chemical approach uses potassium hydroxide (KOH) for alkaline etching or hydrogen fluoride acid (HF) for acid etching, and it can result in a rough surface with a reflectivity of around 17% under irradiation of visible light [3]. Wet chemical etching, using KOH to fabricate the pyramid structure, is a commonly used approach in the industry. Compared to physical etching, KOH-based wet etching is more cost effective, faster, and more feasible for mass production of large-area cells. However, the pyramid structure can reach a minimum reflectivity of 12% and can only absorb the solar energy of visible light. Moreover, a thin layer of silicon nitride (SiN) over the pyramid structure is required to assure the

TABLE 1: Materials, specifications, and vendors.

Material	Specification	Vendor
N-type silicon (100) wafers (monocrystalline)	$1 \sim 3\,\Omega$-cm	Wafer Works, Taiwan
AgNO$_3$	99.8%	Union Chemical Works, Taiwan
HF	55%	Choneye, Taiwan
HNO$_3$	69%	Union Chemical Works, Taiwan
Acetone	99.5%	Sigma-Aldrich
Polyethylene glycol	MW: 1000	Echo Chemical, Taiwan
Borosilicafilm	$C_o = 1 \times 10^{20}$	Emulsitone, USA
Phosphorosilicafilm	$C_o = 5 \times 10^{20}$	Emulsitone, USA

antireflective property. Therefore, silicon nanostructures have been adopted to enhance the antireflectivity [4–9]. Besides chemical wet etching, electrochemical etching, plasma etching, oxidation, and nanogold-catalyzed chemical etching can also be used to fabricate a rough structure with 5% less reflectivity.

Recent investigations observed that semiconductor silicon exhibits an electrochemical reaction in an HF solution. Accordingly, electroless metal deposition and electroless etching have been adopted for fabricating silicon nanowires for micronanoelectrical devices [10–18]. Further studies indicated that silicon nanowire structures possess the antireflective property in the ultraviolet (UV), visible light, and infrared (IR) spectra. Thus, silicon nanowiring is fast substituting chemical vapor deposition (CVD) as a way to reduce the reflectivity in the SiN layer [1]. Garnett and Yang [19] used silver nitrate (AgNO$_3$) as the etchant for electroless etching of silicon nanowire arrays, followed by the fabrication of the P-N junction through PECVD using boron trichloride (BCl$_3$) gas. The fabricated solar cell exhibited a short circuit current density (J_{sc}) of 4.28 mA/cm^2 and an open circuit voltage (V_{oc}) of 0.29 V. A photoelectric conversion efficiency (η) of 0.46% was achieved. Tang et al. [20] made use of the CVD approach to fabricate the P-N junction and then grew silicon nanowires using gold nanoparticles as the catalyst. Uncharged polymethyl methacrylate (PMMA) was employed to reduce the leakage current effect. A solar cell having a J_{sc} of 7.6 mA/cm^2 and an η of 2.73% was produced. In 2009, the National Renewable Energy Laboratory (NREL), USA [21], used chloroauric acid (HAuCl$_4$) as the etchant for electroless etching of nanoporous Si. The thermal oxidation process was then applied to deposit a silicon dioxide (SiO$_2$) passivation layer on the P-N junction surface to reduce the leakage current and indirectly enhance the short circuit current. The resulting solar cell had a high J_{sc} of 34.067 mA/cm^2, a V_{oc} of 0.6123 V, and an η of 16.8%. In 2011, the NREL etched nanostructures on the pyramid microstructure using HAuCl$_4$ to obtain an average reflectivity of 2.7% in the light spectrum of 350–1000 nm. The J_{sc}, V_{oc}, and η of the fabricated solar cell were 35.6 mA/cm^2, 0.615 V, and 17.1%, respectively [22]. Thereafter, tetramethylammonium hydroxide (TMAH)

was employed to smoothen the surface structure of the nanoporous silicon, so that the recombination of electron-hole pairs could be reduced. A solar cell having a J_{sc} of 36.45 mA/cm^2, a V_{oc} of 0.628 V, and an η of 18.2% was produced [23].

The above-mentioned studies indicate the development trends of solar cells, namely, the use of inexpensive processes to produce high photoelectric conversion efficiency devices. In this study, we propose a cost-effective solar cell production method comprising fabrications of a high antireflection micronanohybrid silicon substrate and the P-N junction using a liquid diffuser. The high antireflection micronanohybrid silicon substrate is fabricated by a two-stage metal-assisted (MAE) etching method using an AgNO$_3$ and HF mixing solution as the etchant to grow nanowires on a KOH wet-etched microstructure pyramid array.

2. Materials and Methods

2.1. Materials. The materials used in this study are listed in Table 1.

2.2. Methods

2.2.1. Fabrication of a High Antireflection Micronanohybrid Structure Array. An AgNO$_3$ and HF mixing solution is adopted as the etchant for the MAE. The silver ions in the etchant acquire electrons from the silicon substrate and are reduced to silver atoms, which are then deposited on the surface of the silicon substrate. Simultaneously, the silicon atoms donate electrons and are oxidized to SiO$_2$. The SiO$_2$ is then etched by the HF solution with zero applied potential. Silicon nanowire arrays can be fabricated through consecutive reduction and oxidation (redox) reactions [24–26]. In this study, the MAE method is used for fabricating a high antireflection micronanohybrid structure array. In the first stage, short-time etching using highly concentrated AgNO$_3$ is executed to deposit a coniferous-like silver layer on the wafer surface of the KOH-etched micropyramid array. Then, relatively long-time etching using a lower concentration of AgNO$_3$ is implemented for producing a bolt upright and uniform silicon nanowire array on each micropyramid. The fabrication procedures are described as follows.

(1) Wafer cleaning: clean the wafer sequentially and ultrasonically in acetone, ethanol (EtOH), and distilled water for 30 min. Immerse the washed silicon wafer in diluted HF acid for 2-3 min to remove the oxide layer from the wafer surface. Then, rinse the wafer with distilled water.

(2) Micropyramid array fabrication: prepare the wet-etching etchant with a weight ratio of DI: KOH (40 wt%): IPA = 70 : 2 : 5. Use it to wet-etch the micropyramid array on the cleaned wafer substrate. Then, remove the oxide layer from the wafer surface by immersing the wet-etched wafer into dilute HF acid for 2-3 min.

(3) Two-stage MAE: conduct the first stage of the MAE using AgNO$_3$ (0.34 M) and HF (4.6 M) mixing etchant under various processing times. Then, process the second stage of the MAE using AgNO$_3$ (0.03 M) and HF (5.6 M) mixing etchant under various processing times. Both stages are conducted at 40°C. The optimal processing times for stages 1 and 2 were arrived at by exploring 30 designed processing time combinations between the stages, as tabulated in Table 2.

(4) Removal of silver conifers: during the MAE process, the reduced silver nanoparticles dispersedly distribute on the wafer surface. After MAE, the reduced silver nanoparticles are removed by immersing the wafer into a solution of nitric acid (HNO$_3$) for 5 min.

(5) SiO$_2$ layer removal: remove the bottom SiO$_2$ layer using an HF and distilled water mixing solution (ratio = 1 : 3).

2.2.2. Property Characterization of the Synthesized Micronanohybrid Silicon Substrate. The morphology of the micronanohybrid silicon substrates was characterized using a field emission scanning electron microscope (FESEM) (JSM-6700F, JEOL). The reflectivity for the light spectrum of 200–1000 nm was measured by a variable-angle UV, visible (VIS), and near IR (UV/VIS/NIR) spectrophotometer (Hitachi U-4100).

2.2.3. Growth of the P-N Junction. Instead of the commonly used CVD process, the less expensive silica film was adopted as the diffuser for the growth of the P-N junction. The growth procedures are described below.

(1) Silica film spin coating: spin coat a 0.5 mm thick silica film on the micronanohybrid silicon substrate. Then, volatilize the contained organic solvent at 100°C for 60 min.

(2) Thermal diffusion: place the silica-film-coated silicon substrates in a high temperature furnace to process the thermal diffusion. The processing time should be set to 60 min, and several diffusion temperatures (950, 1000, 1050, 1100, and 1150°C) should be selected to obtain optimal diffusion. Then, remove the glass oxide layer on the wafer surface by immersing the wet-etched wafer into diluted HF acid for 2-3 min. Wash the remaining HF solution using distilled water.

(3) Sheet resistance measurement: use a four-point probe for the sheet resistance measurement.

2.2.4. Cell Fabrication and Photoelectric Conversion Efficiency Measurement. E-gun sputtering using metal masks was adopted for the fabrication of the front fishbone positive titanium electrode and the back negative silver electrode. The thicknesses of the front and back electrodes were 50 and 200 nm, respectively. The electrode sputtered silicon substrate was placed in a nitrogen-filled high temperature furnace at 400°C for 30 min to grow the ohmic contact. The photoelectric conversion efficiency was measured.

Table 2: Processing time combinations between stage 1 and stage 2.

Stage	Processing times				
1	20 s	25 s	30 s	35 s	40 s	45 s
2	2 min	5 min	7 min	10 min	15 min

3. Results and Discussion

3.1. Fabrication Results of the Micronanohybrid Structure Array. The highly concentrated AgNO$_3$ (0.34 M) used in the first MAE stage helped in quickly obtaining the required amounts of reduced silver atoms needed to uniformly cover the entire surface of the pyramid array. However, the height of a wet-etched pyramid is about 3–5 μm. A relatively higher concentration of AgNO$_3$ results in a rapid redox reaction between the silver ions and the silicon substrate. As a result, the pyramid could be completely etched away in a long etching process. Therefore, the etching duration for the first etching stage was set to range from 20 to 45 sec. The second etching stage was employed to uniformly etch the silicon substrate downward under the silver-atom-covered area. Hence, a relatively low AgNO$_3$ concentration (0.03 M) was selected, and a longer etching time (1–5 min) was designed.

Figure 1 illustrates the SEM images of the fabricated micronanohybrid structures subjected to a 30 sec first-stage etching and various second-stage etching processing times. The straight etched nanowires cover the entire surface of the pyramid array, including the pyramid structure and the recesses between the pyramids. The length of the etched nanowires increases with increased etching time. The top view, illustrated by the inset in each image, indicates the hybrid structure of the pyramids and the nanopores.

It has been reported [27] that the antireflectivity of a nanosilicon substrate is closely proportional to nanowire length. Therefore, the second-stage processing time was set at 5 min to further investigate the antireflectivity of the micronanohybrid structure. Figure 2 shows the morphologies of various micronanohybrid structures fabricated by combinations of a fixed second-stage etching time (5 min) and various first-stage etching times. For these micronanohybrid structures subjected to the first-stage processing time of 20 and 25 sec (Figures 2(a) and 2(b)), the nanowires are more intensive, but shorter, when compared with the other samples. The possible reason is that the relatively shorter first-stage etching time may be insufficient to reduce silver nanoparticles to a suitable size for effective downward etching during the second-stage process. When the first-stage processing time was extended to 30, 35, and 40 sec (Figures 2(c), 2(d), and 2(e)), the fabricated nanowires possessed good uniformity and had microscale lengths. However, further increases in the processing time (45 sec) resulted in a looser nanowire array with a bent shape (Figure 2(f)). An excessively long first-stage processing time might result in overdense coverage of silver nanoparticles on the pyramid array, thus resulting in inhomogeneous second-stage etching.

3.2. Antireflectivity Property of the Micronanohybrid Structure Array. As discussed in Section 3.1, nanowire arrays with
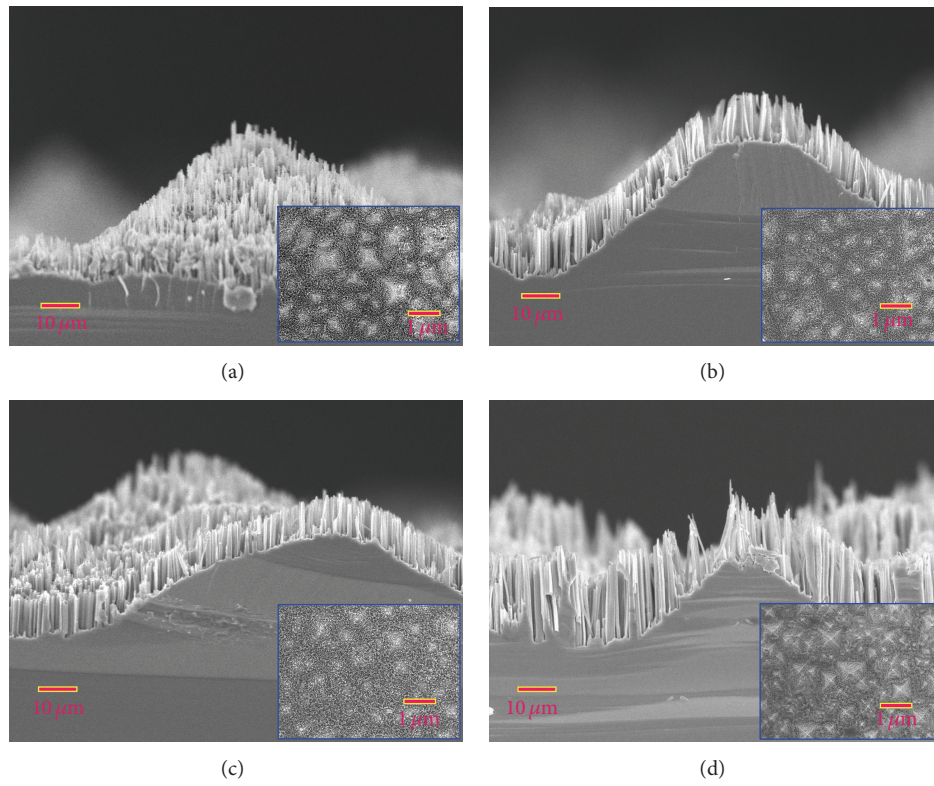
FIGURE 1: SEM images of micronanohybrid silicon substrates fabricated by combinations of a fixed first-stage processing time (30 sec) and various second-stage processing times: (a) 1 min, (b) 2 min, (c) 3 min, and (d) 4 min.
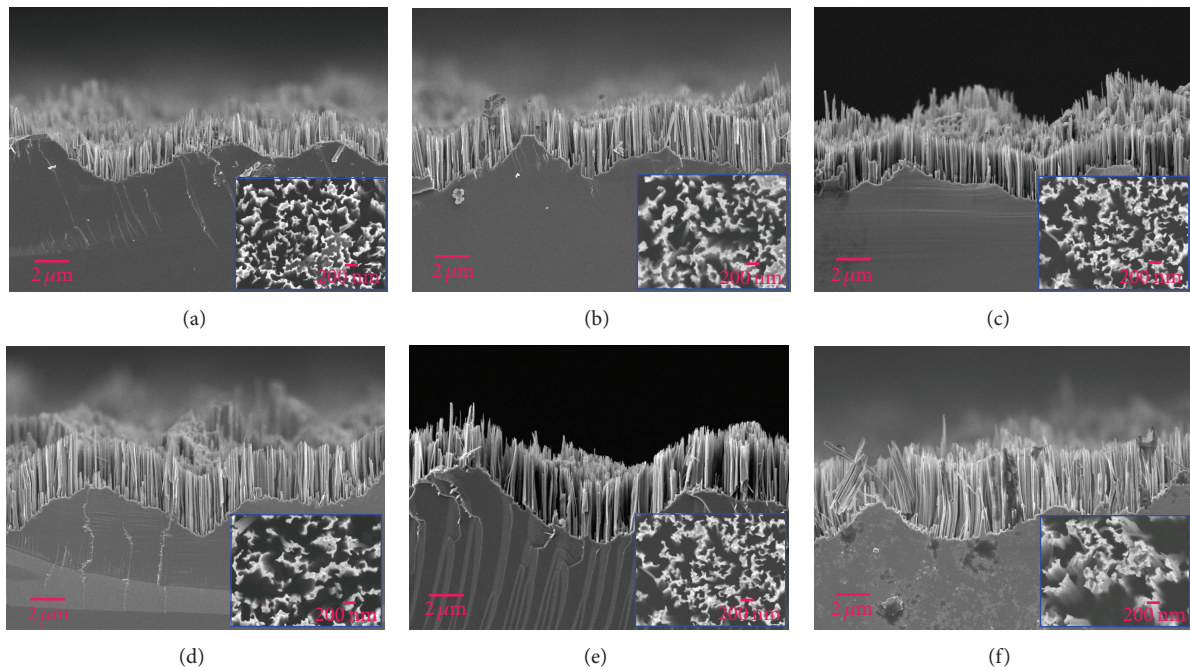

FIGURE 2: SEM images of micronanohybrid silicon substrates fabricated by combinations of a fixed second-stage processing time (5 min) and various first-stage processing times: (a) 20 sec, (b) 25 sec, (c) 30 sec, (d) 35 sec, (e) 40 sec, and (f) 45 sec.
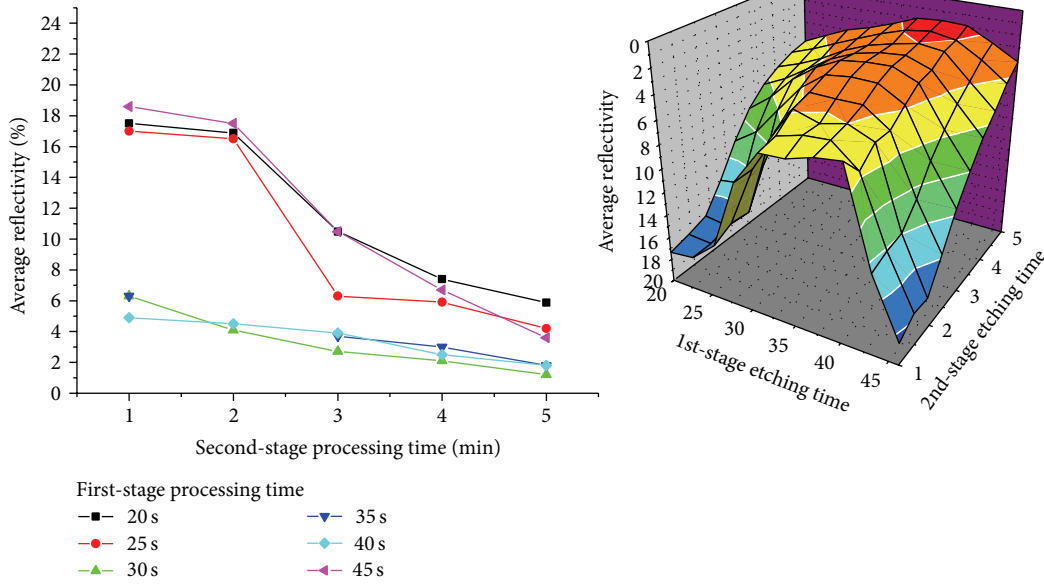
FIGURE 3: Relationship between the average reflectivity of a micronanohybrid structure fabricated by a certain two-stage MAE process and the corresponding etching time combination in the light spectrum of 200–1000 nm.

various heights could be fabricated by adjusting the processing time combinations of the first and second stages. The antireflectivity properties of the silicon substrates subjected to different processing time combinations were investigated. Figure 3 demonstrates the relationship between the average reflectivity of a silicon micronanohybrid structure fabricated by a certain two-stage MAE process and the corresponding etching time combination in the light spectrum of 200–1000 nm. For processes with a first-stage etching time of 20, 25, and 45 sec, the fabricated micronanohybrid structure arrays exhibited relatively higher reflectivity. For processes with a first-stage etching time of 30, 35, and 40 sec, the fabricated micronanohybrid structure arrays processed relatively lower reflectivity. Average reflectivity decreased with increasing second-stage processing times. When the second-stage processing time was 5 min, average reflectivity of less than 2% could be achieved. Up to a certain degree, the reflectivity measurement results agree with the morphologies of the fabricated hybrid structures shown in Figure 2, wherein processes with a first-stage etching time of 20, 25, and 45 sec could fabricate uniform and long hybrid microscale structures. The 3D graph shown in the inset represents average reflectivity as a function of processing time combination. The red area indicates the processing time combinations that resulted in average reflectivity of less than 2%, demonstrating that our two-stage fabrication method is capable of producing high antireflection micronanohybrid structures.

The above discussion reveals that the hybrid structure fabricated by the combinations of a first-stage processing time between 30 and 45 sec and a second-stage processing time of 5 min exhibits less than 2% reflectivity. Figure 4 further depicts the overall reflectivity for the light spectrum of 200–1000 nm for hybrid structures subjected to a 5 min second-stage processing time. It is evident that the reflectivity of
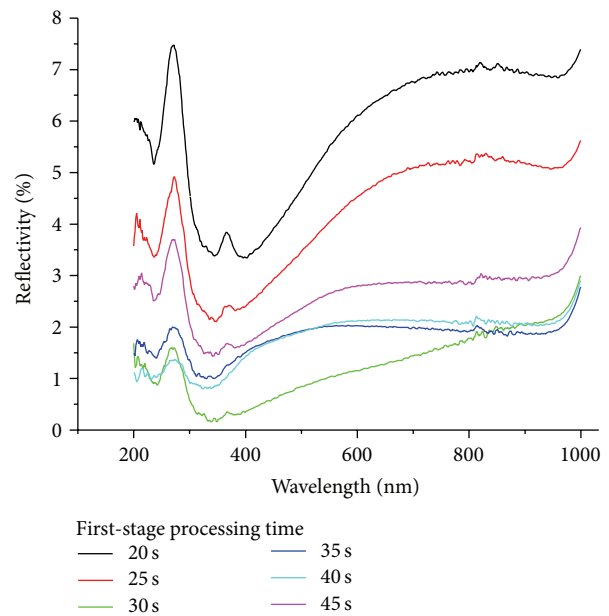

FIGURE 4: Reflectivity of the fabricated micronanohybrid structures subjected to the proposed two-stage MAE for the light spectrum of 200–1000 nm.

hybrid structures subjected to a first-stage processing time of 30 and 45 sec for the light spectrum of 200–1000 nm is less than 2%. The first-stage etching time of 30 sec could fabricate hybrid structures with relatively lower overall reflectivity. Table 3 tabulates the average reflectivity of the hybrid structures fabricated by combinations of a 30 sec first-stage processing time and various second-stage processing times. The 5 min second-stage processing time enabled the hybrid

TABLE 3: Average reflectivity of the two-stage MAE fabricated micronanohybrid structures subjected to a first-stage processing time of 30 sec for the light spectrum of 200–1000 nm.

Second-stage etching time (min)	Average reflectance (%)			
	200–400 nm	401–800 nm	801–1000 nm	200–1000 nm
1	4.26	5.49	8.16	5.85
2	5.26	3.45	4.41	4.16
3	3.16	3.34	3.51	3.54
4	1.96	2.19	2.57	2.32
5	0.74	1.12	1.97	1.21

FIGURE 5: Sheet resistance measurements.

FIGURE 6: Photoelectric conversion efficiency of the fabricated solar cells subjected to various diffusion temperatures (diffusion time = 60 min).
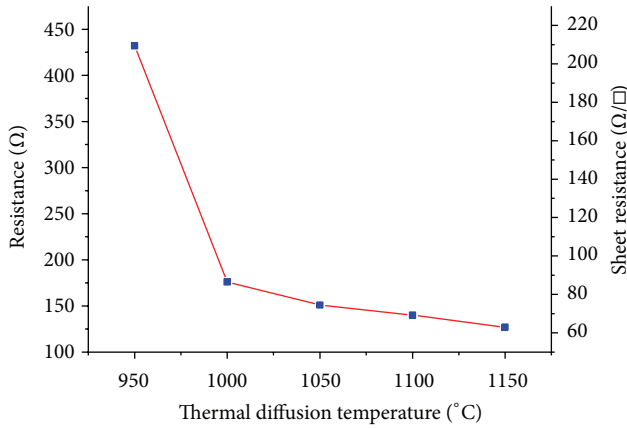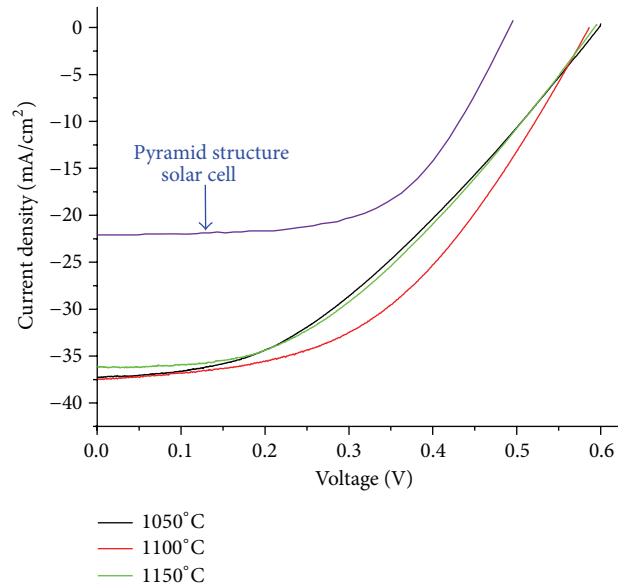
structures to have a low overall reflectivity of 1.21%, including 0.74% in UV, 1.12% in visible light, and 1.97% in IR.

3.3. Sheet Resistance Measurements. The hybrid structures with the best antireflectivity (first-stage processing time = 30 sec and second-stage processing time = 5 min) were then employed for the P-N junction synthesis using silica film.

Figure 5 shows the sheet resistance measurement results. The measured ranges of the resistance and sheet resistance are 100–$450\,\Omega$ and 60–$220\,\Omega/\square$, respectively. A diffusion temperature of 1000–1150°C could grow a P-N junction with sheet resistance within the scope of the ideal P-N junction surface sheet resistance 60–$200\,\Omega/\square$ [28–30]. Samples with P-N junction growth enabled by diffusion temperatures of 1000–1150°C were used for further cell fabrication.

3.4. Photoelectric Conversion Efficiency Measurements. The cell with the micronanohybrid structure having the best antireflectivity (first-stage processing time = 30 sec and second-stage processing time = 5 min) and a P-N junction grown using the silica film (diffusion time = 60 min) was employed for further photoelectric conversion efficiency measurements. Figure 6 displays the current versus voltage (I-V) curves for the pure pyramid cells and the hybrid structured cells under various diffusion times for P-N junction growth. The major variations among the hybrid structured cells grown under different diffusion times are the open circuit voltage (V_{oc}) and the fill factor (FF). It can

also be observed that the hybrid structured cells exhibited much higher short circuit current density (J_{sc}). The detailed data appear in Table 4. Although the average V_{oc} and J_{sc} of the pure pyramid cells were measured as 0.52 V and 21.57 mA/cm^2, respectively, a conversion efficiency (η) of 6.729% was achieved due to a relatively higher FF (60%). The most efficient hybrid structured cells (diffusion temperature = 1100°C) exhibited an efficiency of 12.319% ($V_{oc} = 0.60$ V, $J_{sc} = 37$ mA/cm^2, and FF = 56%). Compared with the pure pyramid cells, the large enhancement in J_{sc} can be attributed to the high antireflection property, while the relatively lower FF is due to the leakage current effects caused by the structural defects in the nanowires. Therefore, cells subjected to a diffusion temperature of 1100°C were then immersed in an HNO$_3$ solution to reduce leakage current effects by growing passivation layers on their surfaces.

A 1-2 nm thick passivation layer of SiO$_2$ was grown by immersing the cells into a 55% HNO$_3$ solution for 15 min. Figure 7 displays the I-V curve and the photoelectric properties of the cell with the added passivation layer. It can be seen that the I-V curve for a cell with the added passivation

TABLE 4: Photoelectric properties of the fabricated solar cells subjected to various diffusion temperatures.

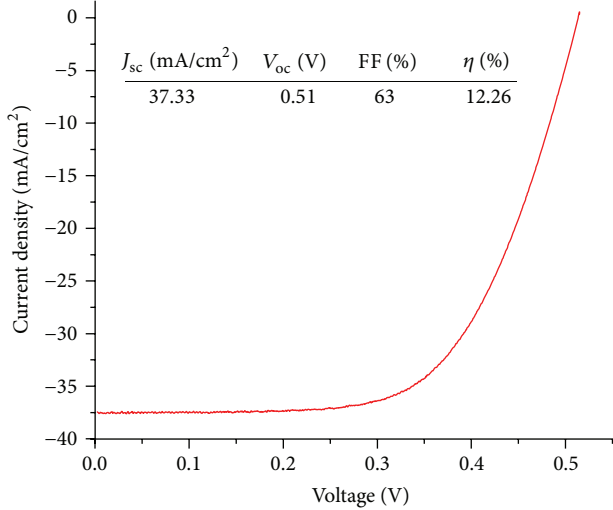| Thermal diffusion (°C)	J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	η (%)	R_{sh} (Ω)
1050°C	37.31	0.60	45	10.10	35.1
1100°C	37.54	0.586	56	12.319	41.7
1150°C	36.12	0.595	53	11.31	50.5
Pyramid structure	21.57	0.52	60	6.729	115

FIGURE 7: Photoelectric conversion efficiency measurement of the fabricated solar cells with a passivation layer.

J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	η (%)
37.33	0.51	63	12.26

TABLE 5: Photoelectric properties of the fabricated solar cells subjected to a diffusion time of 120 min.

J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	η (%)	R_{sh} (Ω)
37.401	0.56	63	13.01	58.9

The processing time for etching on an N-type high-resistance (NH) silicon wafer can be reduced to around 5 min. An inexpensive diffusion process using a liquid diffusion source was then employed to grow the P-N junction. To reduce leakage current effects, the HNO_3 solution was also used to generate a passivation layer on the cell surface. The fabricated hybrid structures exhibited a low average reflectivity of 1.21% in a wide light spectrum (200–1000 nm), including 0.74% in UV, 1.12% in visible light, and 1.97% in the IR spectra. A solar cell with the following photoelectric properties was obtained: $J_{sc} = 37.4$ mA/cm^2, $V_{oc} = 0.56$ V, FF = 63, and $\eta = 13.01\%$.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgment

layer begins to climb at 0.35 V, while that for a cell without this layer begins to climb at 0.1 V (Figure 6). Also, the FF increased from 56 to 63%, while the V_{oc} decreased from 0.586 to 0.51 V. These results imply that the passivation layer could effectively improve leakage current effects. The degradation in the V_{oc} can be attributed to the concentration variation of the diffusion source due to the redox reactions between HNO_3 and the substrate.

To further compensate for the concentration variation of the diffusion source, a longer diffusion time of 120 min was implemented to increase the diffusion depth. The photoelectric properties of the fabricated solar cells (i.e., those subjected to the diffusion process using a silica film for 120 min followed by passivation layer growth using HNO_3 solution for 15 min) are listed in Table 5. The J_{sc} and FF of the cells were about the same as those of the cells subjected to the 60 min diffusion process. However, the V_{oc} increased further to 0.56 V. Hence, the efficiency was enhanced to 13.01%.

4. Conclusion

This study developed a cost-effective method for the fabrication of high antireflection solar cells. A two-stage MAE process using an $AgNO_3$ and HF mixing solution as the etchant was adopted for the fabrication of a micronanohybrid silicon substrate. The process requires short-time etching using highly concentrated $AgNO_3$ in the first stage, followed by relatively long-time etching using less concentrated $AgNO_3$.

References

[1] J. Schmidt, M. Kerr, and A. Cuevas, "Surface passivation of silicon solar cells using plasma-enhanced chemical-vapour-deposited SiN films and thin thermal SiO$_2$/plasma SiN stacks," *Semiconductor Science and Technology*, vol. 16, no. 3, pp. 164–170, 2001.

[2] S. Winderbaum, O. Reinhold, and F. Yun, "Reactive ion etching (RIE) as a method for texturing polycrystalline silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 46, no. 3, pp. 239–248, 1997.

[3] P. Panek, M. Lipiński, and J. Dutkiewicz, "Texturization of multicrystalline silicon by wet chemical etching for silicon solar cells," *Journal of Materials Science*, vol. 40, no. 6, pp. 1459–1463, 2005.

[4] K. Tsujino and M. Matsumura, "Formation of a low reflective surface on crystalline silicon solar cells by chemical treatment using Ag electrodes as the catalyst," *Solar Energy Materials and Solar Cells*, vol. 90, no. 10, pp. 1527–1532, 2006.

[5] J. S. Yoo, I. O. Parm, U. Gangopadhyay et al., "Black silicon layer formation for application in solar cells," *Solar Energy Materials and Solar Cells*, vol. 90, no. 18-19, pp. 3085–3093, 2006.

[6] B. C. Chakravarty, J. Tripathi, A. K. Sharma et al., "The growth kinetics and optical confinement studies of porous Si for application in terrestrial Si solar cells as antireflection coating," *Solar Energy Materials and Solar Cells*, vol. 91, no. 8, pp. 701–706, 2007.

[7] C.-H. Sun, W.-L. Min, N. C. Linn, P. Jiang, and B. Jiang, "Templated fabrication of large area subwavelength antireflection gratings on silicon," *Applied Physics Letters*, vol. 91, no. 23, Article ID 231105, 2007.

[8] C. T. Wu, F. H. Ko, and C. H. Lin, "Self-organized tantalum oxide nanopyramidal arrays for antireflective structure," *Applied Physics Letters*, vol. 90, p. 171911, 2007.

[9] C. H. Sun, P. Jiang, and B. Jiang, "Broadband moth-eye antireflection coatings on silicon," *Applied Physics Letters*, vol. 92, no. 6, Article ID 061112, 2008.

[10] K. Nishioka, S. Horita, K. Ohdaira, and H. Matsumura, "Antireflection subwavelength structure of silicon surface formed by wet process using catalysis of single nano-sized gold particle," *Solar Energy Materials and Solar Cells*, vol. 92, no. 8, pp. 919–922, 2008.

[11] P. Gorostiza, R. Diaz, J. Servat, F. Sanz, and J. R. Morante, "Atomic force microscopy study of the silicon doping influence on the first stages of platinum electroless deposition," *Journal of the Electrochemical Society*, vol. 144, no. 3, pp. 909–914, 1997.

[12] P. Gorostiza, M. A. Kulandainathan, R. Díaz, F. Sanz, P. Allongue, and J. R. Morante, "Charge exchange processes during the open-circuit deposition of nickel on silicon from fluoride solutions," *Journal of the Electrochemical Society*, vol. 147, no. 3, pp. 1026–1030, 2000.

[13] S. Ye, T. Ichihara, and K. Uosaki, "Spectroscopic studies on electroless deposition of copper on a hydrogen-terminated Si(111) surface in fluoride solutions," *Journal of the Electrochemical Society*, vol. 148, no. 6, pp. C421–C426, 2001.

[14] G. J. Norga, M. Platero, K. A. Black, A. J. Reddy, J. Michel, and L. C. Kimerling, "Mechanism of copper deposition on silicon from dilute hydrofluoric acid solution," *Journal of the Electrochemical Society*, vol. 144, no. 8, pp. 2801–2810, 1997.

[15] D. Aurbach and Y. Cohen, "The application of atomic force microscopy for the study of Li deposition processes," *Journal of the Electrochemical Society*, vol. 143, no. 11, pp. 3525–3532, 1996.

[16] L. A. Porter Jr., H. C. Choi, J. M. Schmeltzer, A. E. Ribbe, L. C. C. Elliott, and J. M. Buriak, "Electroless nanoparticle film deposition compatible with photolithography, microcontact printing, and dip-pen nanolithography patterning technologies," *Nano Letters*, vol. 2, no. 12, pp. 1369–1372, 2002.

[17] C. Carraro, L. Magagnin, and R. Maboudian, "Selective metallization of silicon micromechanical devices," *Electrochimica Acta*, vol. 47, no. 16, pp. 2583–2588, 2002.

[18] F. C. Grozema, P. T. Van Duijnen, Y. A. Berlin, M. A. Ratner, and L. D. A. Siebbeles, "Intramolecular charge transport along isolated chains of conjugated polymers: effect of torsional disorder and polymerization defects," *Journal of Physical Chemistry B*, vol. 106, no. 32, pp. 7791–7795, 2002.

[19] E. C. Garnett and P. Yang, "Silicon nanowire radial p-n junction solar cells," *Journal of the American Chemical Society*, vol. 130, no. 29, pp. 9224–9225, 2008.

[20] Y. B. Tang, Z. H. Chen, H. S. Song et al., "Vertically aligned p-type single-crystalline GaN nanorod arrays on n-type Si for heterojunction photovoltaic cells," *Nano Letters*, vol. 8, no. 12, pp. 4191–4195, 2008.

[21] H.-C. Yuan, V. E. Yost, M. R. Page et al., "Efficient black silicon solar cells with nanoporous anti-reflection made in a single-step liquid etch," in *Proceedings of the 34th IEEE Photovoltaic Specialists Conference (PVSC '09)*, pp. 141–145, June 2009.

[22] F. Toor, M. R. Page, H. M. Branz, and H. C. Yuan, "17.1%-efficient multi-scale-textured black silicon solar cells without dielectric antireflection coating," in *Proceedings of the 37th IEEE Photovoltaic Specialists Conference (PVSC '11)*, pp. 20–24, 2011.

[23] J. Oh, H.-C. Yuan, and H. M. Branz, "An 18.2%-efficient black-silicon solar cell achieved through control of carrier recombination in nanostructures," *Nature Nanotechnology*, vol. 7, pp. 743–748, 2012.

[24] H. Morinaga, M. Suyama, and T. Ohmi, "Mechanism of metallic particle growth and metal-induced pitting on Si wafer surface in wet chemical processing," *Journal of the Electrochemical Society*, vol. 141, no. 10, pp. 2834–2841, 1994.

[25] J. S. Kim, H. Morita, J. D. Joo, and T. Ohmi, "The role of metal induced oxidation for copper deposition on silicon surface," *Journal of the Electrochemical Society*, vol. 144, no. 9, pp. 3275–3283, 1997.

[26] K. Peng and J. Zhu, "Morphological selection of electroless metal deposits on silicon in aqueous fluoride solution," *Electrochimica Acta*, vol. 49, no. 16, pp. 2563–2568, 2004.

[27] H. C. Liu and G. J. Wang, "Fabrication of high anti-reflection nanowires on silicon using two-stage metal-assisted etching," *Journal of Renewable and Sustainable Energy*, vol. 5, Article ID 053115, 2013.

[28] F. Granek, M. Hermle, D. M. Huljić, O. Schultz-Wittmann, and S. W. Glunz, "Enhanced lateral current transport via the front N$^+$ diffused layer of N-type high-efficiency back-junction back-contact silicon solar cells," *Progress in Photovoltaics: Research and Applications*, vol. 17, no. 1, pp. 47–56, 2009.

[29] D. S. Kim, M. M. Hilali, A. Rohatgi, K. Nakano, A. Hariharan, and K. Matthei, "Development of a phosphorus spray diffusion system for low-cost silicon solar cells," *Journal of the Electrochemical Society*, vol. 153, no. 7, pp. A1391–A1396, 2006.

[30] B. Paviet-Salomon, S. Gall, R. Monna, S. Manuel, and A. Slaoui, "Experimental and analytical study of saturation current density of laser-doped phosphorus emitters for silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 95, no. 8, pp. 2536–2539, 2011.