FEATURE ARTICLE

Overview of electroceramic materials for oxide semiconductor thin film transistors

Jin-Seong Park · H. Kim · Il-Doo Kim

Abstract The flat panel display (FPD) market has been experiencing a rapid transition from liquid crystal (LC) to organic light emitting diode (OLED) displays, leading, in turn, to the accelerated commercialization of OLED televisions already in 2013. The major driving force for this rapid change was the adaptation of novel oxide semiconductor materials as the active channel layer in thin film transistors (TFTs). Since the report of amorphous-InGaZnO (a-IGZO) semiconductor materials in 2004, the FPD industry has accelerated the development of oxide TFTs for mass-production. In this review, we focus on recent progress in applying electro-ceramic materials for oxide-semiconductor thin-film-transistors. First, oxide-based semiconductor materials, distinguished by vacuum or solution processing, are discussed, with efforts to develop high-performance, cost-effective devices reviewed in chronological order. The introduction and role of high dielectric constant - reduced leakage gate insulators, in optimizing oxide-semiconductor device performance, are next covered. We conclude by discussing current issues impacting oxide-semiconductor TFTs, such as field effect mobility and device stability and the proposed directions being taken to address them.

Keywords Electroceramics · Oxide semiconductors · Transistors · Displays · Gate insulators

Jin-Seong Park and H. Kim contributed equally to this work.

J.-S. Park
Division of Materials Science and Engineering, Hanyang University, 222 Wangsimni-ro Seongdon-gu, Seoul 133-791, Republic of Korea
e-mail: jsparklime@hanyang.ac.kr

H. Kim · I.-D. Kim (✉)
Department of Materials Science and Engineering, Korea Advanced Institute of Technology, 291 Daehak-ro, Yuseong-gu, Daejeon 305-701, Republic of Korea
e-mail: idkim@kaist.ac.kr

H. Kim
e-mail: hkim_2@naver.com

1 Introduction

Oxide semiconductors have, in recent years, become the focus of extreme interest for emerging electronic applications, such as flexible and transparent displays [1–5]. In particular, several display industries have intensively researched and demonstrated advanced flat-panel display (FPD) technology utilizing oxide semiconductors including electronic paper (e-paper), organic light-emitting diode displays (OLEDs) and liquid crystal displays (LCDs) [6, 7]. Figure 1 depicts the history of R&D trends relative to oxide-semiconductors and prototype display panels. Although efforts dedicated towards the research and development of oxide semiconductors have been relatively recent (see Fig. 1), by 2012, many FPD manufacturers (e.g., Samsung, LG, Sharp, and AUO) had already announced major investments in large AM (Active Matrix) OLED-production based on oxide-semiconductor devices. In 2013, a 55-in. AMOLED TV (LG Electronics), with options for flat or curved screens, reached commercial markets [8].

The first version of an oxide semiconductor TFT, which utilized evaporated SnO_2 as the channel layer in a bottom-gate-staggered configuration on a glass substrate, was reported in 1964 [9]. The earliest SnO_2 TFT exhibited poor electrical performance, including lack of saturation, positive curvature of the output characteristics, an almost negligible amount of transfer curve, and the inability to turn the device off. In 1968, the first ZnO-based TFT was reported which also did not saturate and could not be turned off by application of a gate voltage. Since then, metal oxide TFTs have been continually improved, so that they now exhibit desired characteristics [10].

LCD and OLED flat-panel-display products have traditionally been driven by amorphous silicon (a-Si) and low temperature poly-silicon (LTPS) thin-film-transistors, respectively. While commercial markets have been demanding high-end products with high resolution (4000×2000 pixels), high frame rates (over 240 Hz), and large size (more than 70 in.), conventional silicon-based TFTs have been unable to deliver

Fig. 1 Historical overview of developments in oxide-semiconductor based TFT-based devices
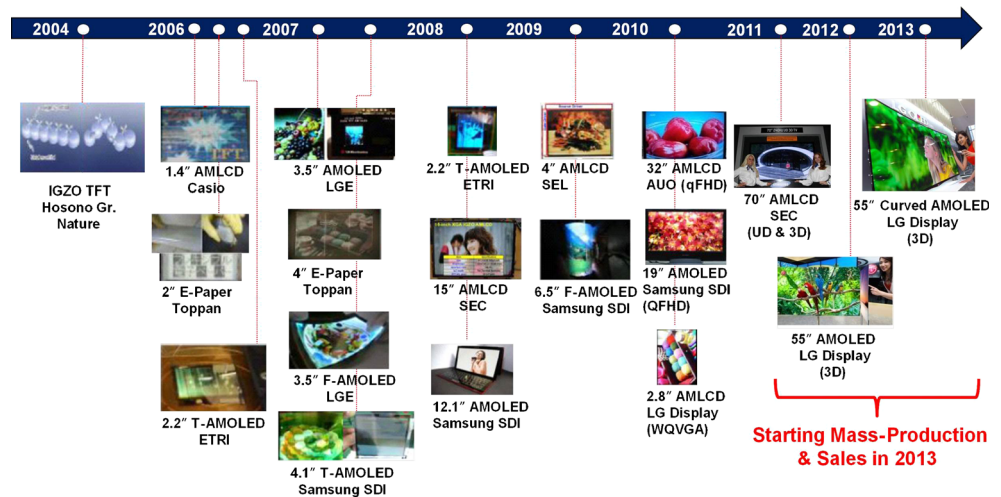
them. These TFTs have inherent limitations, with a-Si TFTs exhibiting relatively low mobility (<1 cm^2/V · s) and inferior bias stability, while LTPS TFTs suffer from non-uniform performance and high processing costs.

After the Hosono group reported the 'amorphous indium gallium zinc oxide' (a-IGZO) semiconductor in 2004 [11], amorphous oxide semiconductors (AOSs) were rapidly adopted as the channel layer in flexible and transparent TFT-based electronic devices. They have since been taking the place of a-Si and LTPS, given several key qualities, including high electrical mobility, amorphicity, and high optical transparency. Moreover, AOSs have a lower density-of-states (DOS), including tail and deep level states, compared to that of a-Si, resulting in superior electrical stability [12].

In this review, we report on recent developments in AOS TFT devices that address several major issues including the nature of the semiconducting oxides, gate insulators, and device instability. We begin by describing the historical development of oxide semiconductors from binary materials to multi-component materials, optimized for practical applications. Then we move on to introduce various gate insulators for producing high performance AOS TFTs, from their physical structures to their properties. Improvements in AOS TFTs by use of high-k gate insulators are also discussed. Finally, we introduce recent progress in minimizing device instability of AOS TFTs under gate bias, temperature, and illumination.

2 Oxide semiconductor materials

2.1 Operation of the TFTs and important device parameters

Before focusing on the issues related to the choice and optimization of the oxide semiconductor and dielectric materials, we briefly review the TFT and its operating characteristics to aid readers less familiar with this technology. TFTs are three terminal field-effect devices, as illustrated in Fig. 2(a). The TFT structure is assembled by the stacking of the gate, gate insulator, channel (oxide semiconductor), and source/drain electrodes (both top and bottom gate designs are illustrated) onto the substrate. During operation, the current flowing within the semiconductor channel between the "Source" and "Drain" electrodes are modulated by the electric field imposed between the gate and Drain. To insure that no current flows between Gate and Drain, when the Gate voltage is applied Gate electrode, a highly insulating layer is placed between the semiconductor and the Gate. Furthermore, a high relative dielectric constant of the Gate insulator insures efficient field modulation of the source to drain current even for small applied voltages.

Since carrier flow within the channel can be adjusted by application of an electric field at the insulator/semiconductor interface, these devices are known as "Field-Effect" devices. Confusion often exists about the distinction between TFTs and MOSFETs [Metal Oxide Semiconductor Field-Effect Transistor, the well-known device used in microelectronics, see Fig. 2(b)]. There are two important differences. The first relates to how the semiconductor layer is formed and/or deposited. Semiconductors in TFTs are "thin films", deposited by various thin film methods. But, MOSFETs are constructed on single-crystal (bulk) silicon wafers, requiring high temperature processes (exceeding 1000 °C). TFTs, on the other hand, are readily fabricated by low temperature processes on various inexpensive substrates such as glasses and plastics. The second difference relates to the carrier flow mode. The conductance in TFTs relies on an accumulation layer, while that in MOSFET is controlled by inversion layer formed in the interface between semiconductor and insulator. Thus, the n-type TFTs have n-type semiconductor layers but the n-type MOSFETs have p-type silicon substrates.

To understand the operation of TFTs, there are several important parameters [on/off ratio, field-effect mobility (μ_{fe}),
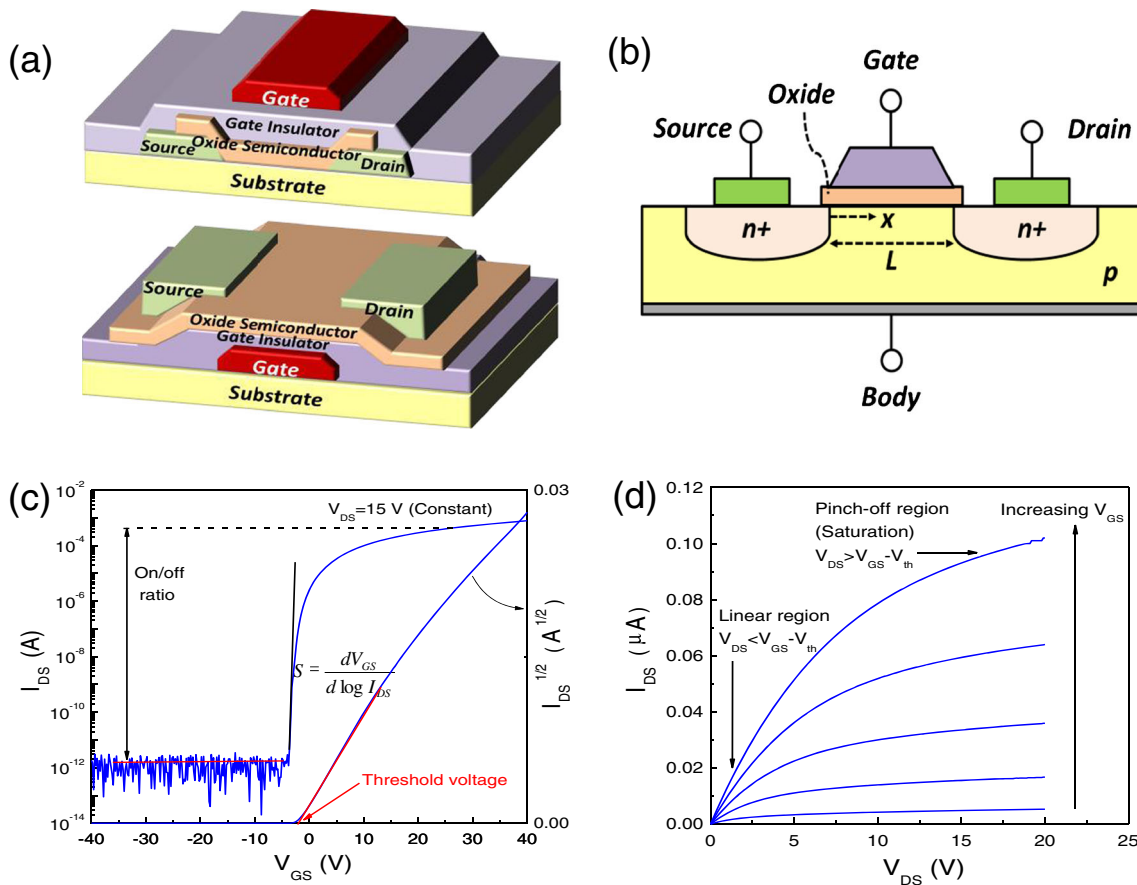
Fig. 2 (**a**) Common TFT device geometries used to fabricate oxide TFTs, which can be classified as top gate and bottom gate structure. (**b**) A schematic image of n-channel MOSFET device structure. Typical transfer (**c**) and output (**d**) electrical characteristics of oxide TFTs. Analysis of TFT characteristics are also shown including threshold voltage (V_{th}), subthreshold swing (S), and on/off ratio

threshold voltage (V_{th}), and subthreshold swing (S)], extracted from the transfer and output characteristics shown in Fig. 2(c) and (d).

On/off ratio This is defined as the ratio of the maximum to the minimum I_{DS} (drain current). As shown in Fig. 2(c), the minimum I_{DS} is given by the noise level of the measurement equipment or by the gate leakage current during the off position of the TFT device. The lower this value, the lower the leakage current and therefore power dissipation during the off state. Thus the on/off ratio of TFTs represents the ideality of the electronic switch characteristic.

Field-effect mobility (μ_{fe}) The mobility reflects the efficiency of charge carrier transport across the semiconductor layer, depending on device configurations (width, length, and thickness of semiconductor) and the nature and significance of the various scattering mechanisms (lattice vibration, ionized impurity, surface roughness, and other defects). In TFTs, the following two mobilities can be extracted depending on V_{DS}: linear field-effect mobility and saturation mobility.

At low V_{DS} ($V_{DS} \sim 0 \ll V_{GS}$), defined as linear field-effect mobility (μ_{lin}):

$$I_{DS} = \frac{W}{L} \mu_{lin} C_i \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (1)$$

At high V_{DS} ($V_{DS} \gg V_{GS} - V_{th}$), defined as saturation mobility (μ_{sat}):

$$I_{DS} = \frac{W}{2L} \mu_{sat} C_i (V_{GS} - V_{th})^2 \quad (2)$$

where W denotes the channel width, L the channel length, C_i the capacitance per unit area of the dielectric layer, V_{DS} the drain to source voltage, and V_{GS} the gate to source voltage.

Threshold voltage (V_{th}): The V_{th} is the gate voltage, at which significant current flow initiates (conducting channel or accumulation layer) between source and drain via the channel formed at the semiconductor/insulator interface,. The value is usually extracted from the $I_{DS}^{1/2}$ vs. V_{GS} characteristics, as shown in Fig. 2(c). The plot of $I_{DS}^{1/2}$ vs V_{GS} intersects the x-axis (V_{GS}) at the value of V_{th}.

Subthreshold swing (S): The inverse of the maximum slope of the transfer characteristics: This represents how rapidly I_{DS} increases by one decade under an increasing applied V_{GS}, i.e.,

$$S = \left(\frac{d\log(I_{DS})}{dV_{GS}} \bigg|_{Max} \right)^{-1} \qquad (3)$$

Small values of S (generally, 0.1~0.5 V/decade) reflect low power consumption for the microelectronic devices.

The output characteristics representative TFT operation,, where I_{DS} is plotted against V_{DS} for various V_{GS}, are shown in Fig. 2(d). As V_{DS} increases under constant V_{GS}, I_{DS} increases linearly and then saturates to a value (called "hard saturation"). Both characteristics are representative of TFT behavior and reflect the relative performance of the TFT.

3 Binary oxide semiconductors: ZnO, In₂O₃, SnO₂, and TiOₓ

The key binary oxide semiconductors (ZnO, In₂O₃, SnO₂, and TiOₓ etc.) of interest have wide band gaps (>3.0 eV) that allow the transmission of visible light [13]. Often even when undoped, they exhibit much higher electrical conductivities (10^{-2} Ω^{-1} cm^{-1} to 10^2 Ω^{-1} cm^{-1}) than other wide gap metal-oxide materials due to inherent high levels of n-type conductivity. This indicates that native shallow defects must exist including either oxygen vacancies, cation interstitials, or substitutional or interstitial hydrogen [14–16]. Because of such donors, these binary oxides exhibit relatively high carrier concentrations (>10^{18} cm^{-3}) and electron mobilities (>10 cm^2/V · s) even when deposited at room temperature. As a consequence, they have undergone intensive research as transparent conducting materials for various electronic devices (e.g., LCDs, OLEDs, and solar cells).

In 2003, following initial development of oxide semiconductors and their applications for display purposes, several active research groups revisited ZnO-based TFTs. Masuda et al. [17] reported a ZnO channel layer with bottom-gate structure, exhibiting low carrier concentration (<5× 10^{16} cm^{-3}). The ZnO layer was deposited onto a silicon substrate by pulsed-laser deposition (PLD) at a substrate temperature of 450 °C, under oxygen atmosphere. The ZnO TFTs showed hard saturation and ideal saturation output curves (drain current—drain voltage characteristics). The field-effect mobility (μ_{fe}) was about 1 cm^2/V · s for a depletion mode device. Hoffman et al. [18] also reported the electrical performance of ZnO TFTs prepared by the ion-beam sputter method. The device had a μ_{fe} of 2.5 cm^2/V · s and high drain current, on/off ratio of ~10^7 after annealing at 800 °C in oxygen. This enhancement in performance was attributed to the improvement of the ZnO crystallinity. However, the high

deposition and annealing temperature was still a significant problem for other electronic applications. Carcia et al. [19] suggested the potential suitability of room temperature grown ZnO films as the active channel layer of oxide TFTs prepared by radio-frequency (rf) magnetron sputtering. They fabricated ZnO TFTs with precise control of oxygen partial-pressure during sputter deposition, with the products exhibiting ideal output curves (μ_{fe} of >2 cm^2/V · s), and a drain current on/off ratio >10^6.

After publication of these results, many ZnO TFTs were reported with improved performance and with lowered deposition temperatures suitable for flexible and transparent electronics applications [20–23]. As shown in Fig. 3(a) and (b), Fortunato et al. [20] reported room temperature fabricated ZnO TFTs with invert-staggered structure (high mobility value: approximately 50 cm^2/V · s) by carefully optimizing oxygen partial pressure during ZnO growth. In fact, the control of oxygen partial pressure suggested a path to the fabrication of highly efficient and reliable TFTs, opening new doors towards the realization of transparent electronic circuits.

SnO₂ and In₂O₃ TFTs have also been investigated as channel layers by several groups. Presley et al. [24] demonstrated a staggered, bottom-gate SnO₂ TFT using AlTiOₓ as the gate insulator, and ITO (InSnOx) as the gate, source, and drain contact. The SnO₂ channel was deposited by rf magnetron sputtering and then subjected to rapid thermal annealing in oxygen at 600 °C. Based on optimizing the SnO₂ channel thickness (10–20 nm) on TFTs, the device performance exhibited a μ_{fe} of 2.0 cm^2/V · s and a drain current on/off ratio of 10^5. Unfortunately, SnO₂ TFTs did not appear extensively in binary oxide TFTs, because satisfactory n-type electrical properties (of SnO₂) were difficult to achieve at low deposition temperatures, unlike other binary oxide semiconductors.

The development of In₂O₃ TFTs was launched late because indium oxide (In₂O₃), while a well-known transparent conductive oxide (TCO) with high carrier concentration (>10^{19} cm^{-3}), shows some difficulty in having its carrier concentrations reduced to semiconducting levels (<10^{18} cm^{-3}). Lavareda et al. [25] reported InOₓ TFTs with bottom gate structure. They optimized the rf power and oxygen pressure during InOₓ deposition by 'radio-frequency plasma enhanced reactive thermal evaporation', resulting in broad ranges of electrical resistivity from 13.7 to 1.7×10^7 Ωcm. The InOₓ TFTs showed reasonable electrical performance, including μ_{fe} of 0.02 cm^2/V · s and drain current on/off ratio of 10^4. Following that, Vygranenko et al. [26] improved the electrical performance of In₂O₃ TFTs by using In₂O₃ channel layers deposited by ion-beam-assisted evaporation. They fabricated a reliable In₂O₃ TFT at room temperature, showing μ_{fe} of 3.3 cm^2/V · s, subthreshold swing (S) of 0.5 V/decade, and drain current on/off ratio of 10^6. They also suggested that achieving a high performance In₂O₃ device is dependent on precise control of the oxygen ion beam flux and interface
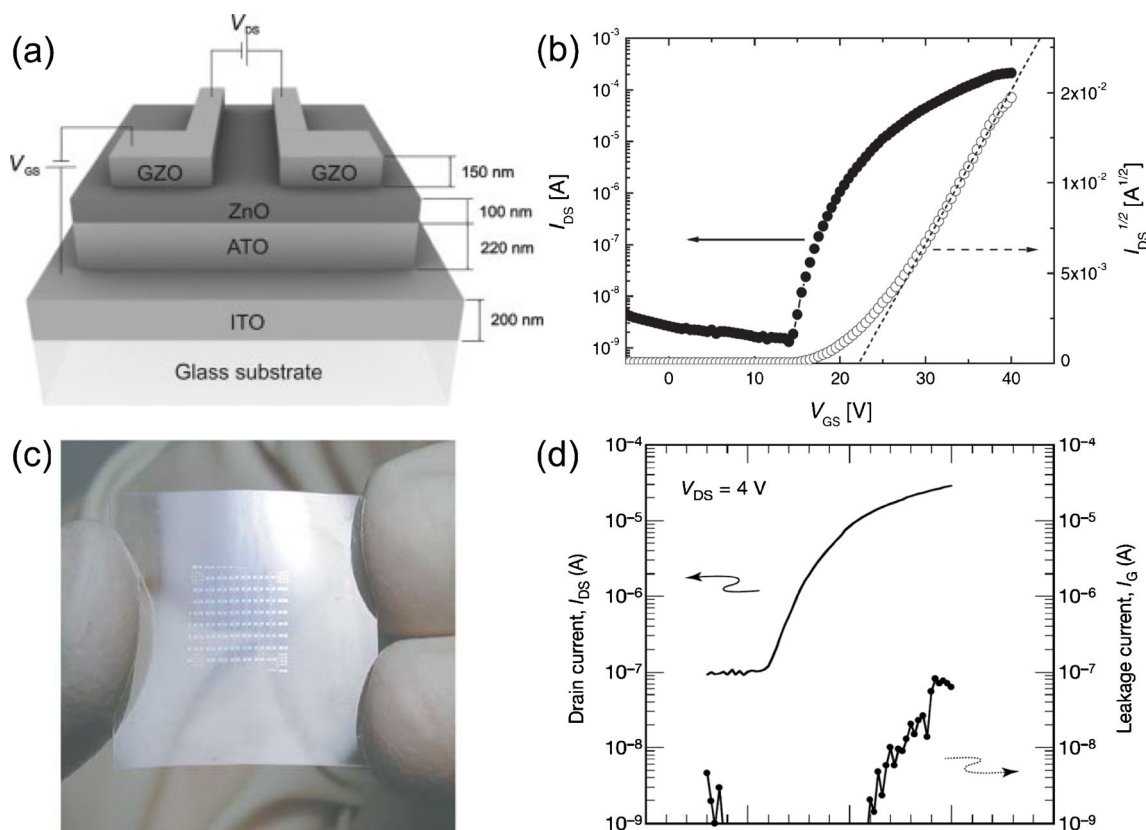
Fig. 3 (a) Schematic illustration of the ZnO-based TFT structure. The ZnO channel layer and the gate insulator, consisting of a superlattice of Al_2O_3 and TiO_2 (ATO,) are 100 and 220 nm in thickness, respectively. (b) Typical ZnO TFT transfer characteristics for V_{DS}=20 V. The ZnO TFT operates in the enhancement mode with a threshold voltage of 21 V and a saturation mobility of 20 $cm^2/V \cdot s$. Reprinted with permission from [20].

Copyright 2005, Wiley-VCH Verlag GmbH. (c) A photograph of the flexible *a*-IGZO TFT sheet. (d) Typical transfer characteristics of *a*-IGZO TFT before bending (threshold voltage of ~1.6 V and saturation mobility of ~8.3 $cm^2/V \cdot s$). Reprinted with permission from [11]. Copyright 2004, Macmillan Publishers Ltd

defects (In_2O_3/SiO_x). Moreover, Dhanajay et al. [27] investigated In_2O_3 TFTs fabricated at a substrate temperature of 100 °C as a function of active channel thickness (5–20 nm). They found that there is a reduction in grain boundary density in thicker films leading to a higher mobility (~34 $cm^2/V \cdot s$). This suggests that grain size control of the active layer is a key factor in obtaining better electrical performance with regard to mobility.

Recently, much more abundant and inexpensive titanium oxide (TiO_2) emerged as an alternative to that of indium oxide, given the known scarcity and expense of In.. In 2006, Katayama et al. [28] first reported a TiO_2 TFT with the rutile structure. A top-gate transistor structure with an MgO insulating buffer between TiO_2 semiconductor and amorphous $LaAlO_3$ gate insulator, was fabricated on ultra-smooth, rutile, single crystal substrate. The TiO_2 active layer was deposited by PLD and annealed at 700 °C in air. The device exhibited an on-to-off ratio exceeding 10^4 and μ_{fe} of 0.08 $cm^2/V \cdot s$. To fabricate a TiO_x TFT at lower temperature, Park et al. [29] used 'metal-organic chemical-vapor-deposition (MOCVD)-

grown TiO_2 active layer' or 'plasma-enhanced atomic-layer-deposition (PEALD)-grown TiO_x active layer', obtained at a deposition temperature of 250 °C, leading to reasonable TFT characteristics. TFTs optimized with N_2O plasma treatment showed μ_{fe} of 1.64 $cm^2/V \cdot s$, S of 1.86 V/decade, and drain current on/off ratio of 4.7×10^5. Also, Choi et al. [30] fabricated more practical TiO_x TFTs by direct-current (dc) magnetron sputtering. The device exhibited μ_{fe} of 0.69 $cm^2/V \cdot s$, subthreshold swing (S) of 2.45 V/decade, and drain current on-to-off ratio of 2.04×10^7 after rapid thermal annealing (RTA) in nitrogen gas. Very recently, Park et al. [31] reported that the conduction behavior of TiO_x materials is very different from that of ZnO materials due to electronic d-orbital ordering in TiO_x.

Table 1 summarizes the electrical properties and deposition conditions of binary oxide semiconductor based TFTs. Unfortunately, although there have been many efforts, over an extended period, to improve the electrical performance of these devices, and to improve the fabrication processes for binary oxide semiconductors, they have received little

Table 1 Summary of key process and property characteristics of binary oxide semiconductor thin film transistors [RF/DC (radio frequency/direct current) sputter, PE/AP ALD (plasma enhanced/atmospheric pressure atomic layer deposition), PLD (pulsed laser deposition), R.T. (room temperature), ND (no data)]

Channel Materials	Deposition Method	Mobility ($cm^2/V \cdot s$)	Subthreshold Swing (V/decade)	Process Temperature (°C)	Ref.
ZnO	rf sputter	>2	3	R.T.	[19]
ZnO	PLD	0031–0.97	ND	450	[17]
ZnO	Ion-beam sputter	0.3–2.5	ND	600–800	[18]
ZnO	ALD	4	ND	200	[21]
ZnO	AP ALD	10	ND	200	[22]
ZnO	rf sputter	27	1.39	R.T.	[23]
InO_x	Reactive evaporation	0.02	ND	R.T.	[25]
In_2O_3	Ion-beam evaporation	3.3	0.5	R.T.	[26]
In_2O_3	Reactive evaporation	34	ND	100	[27]
SnO_2	rf sputter	2	ND	600	[24]
TiO_x	PLD	0.08	ND	700	[28]
TiO_x	PEALD	1.64	1.86	250	[29]
TiO_x	dc sputter	0.69	2.45	400	[30]

attention. This is largely due to the fact that these oxides are polycrystalline, and are thereby inappropriate for use as the active layer in TFTs due to poor uniformity. Therefore, the search for amorphous oxide semiconductors with high electrical performance for large-area production has remained a challenging issue, in terms of practical fabrication approaches.

4 Multicomponent oxide semiconductors

An historic event in the early development of oxide semiconductors was the demonstration by Nomura et al. of amorphous "a-IGZO" TFTs on flexible substrates [11], as illustrated in Fig. 3(c) and (d). The channel layer, a 30 nm thick a-IGZO, was deposited by PLD at room temperature onto a polyethylene terephthalate (PET) substrate. These TFTs exhibited high field effect mobility (μ_{fe}~8.3 $cm^2/V \cdot s$). This report made a significant impact not only among academic researchers but also industrial engineers, given thermal stability of the amorphous phase of IGZO in air up to ~500 °C, and the ability to lower the carrier concentration below <10^{17} cm^{-3} without decreasing the electron mobility. Interestingly, the electronic configurations of In, Ga, and Zn are $(n-1)$ $d^{10}ns^0$, where n is the principle quantum number of the cations ($n \geq 5$). Those vacant s-orbitals have isotropic properties and spherical symmetry, enabling electronic conduction via direct overlap of the s-orbitals in neighboring cations even within the structural disorder characteristic of amorphous oxides. Moreover, the decrease in carrier concentration may be attributed to the Ga^{3+} ions, which tightly bind to oxygen ions and thereby suppress the formation of oxygen vacancies. After this discovery, multi-component oxide semiconductors have been rapidly developed with the dual strategy of forming amorphous structures together with controlled carrier concentrations. Table 2

summarizes historically important multi-component oxide semiconductors and their TFT properties.

Another approach has been focused on exchanging Ga with other elements such as Zr [40], Hf [41], La [49], Mg [50], and Si [44] to form amorphous In(Zr, Hf, La, Mg, Si)ZnO-matrices since these elements can act as carrier-suppressors within InZnO as well as network stabilizers. These carrier-suppressors normally have relatively high electro-negativities for binding oxygen strongly within a crystalline structure. Indeed, various multi-component, oxide semiconductors are being examined with the aim of improving the stability of devices by proper selection of carrier-suppressors. Park et al. [40], for example, reported the performance of a ZrInZnO-semiconductor device with its characteristics shown in Fig. 4(a) and (b) including a comparison with that of a-IGZO TFTs. The ZrInZnO films, produced by co-deposition by rf sputtering from InZnO and ZrO_2 targets had nanoscale ZrInZnO crystallites dispersed in an amorphous-phase matrix. The ZrInZnO TFTs exhibited μ_{fe} of 3.9 $cm^2/V \cdot s$, S of 0.98 V/decade, and drain current on-to-off ratio of 10^7 after a 350 °C anneal in a nitrogen atmosphere. In terms of device stability, the threshold voltage (V_{th}) shift after the application of biasing stress (drain current (I_{DS})=3 μA for 60 h) was only 0.99 V, better than those obtained for a-IGZO and ZnO TFT devices. In spite of the ZrInZnO investigation, it is still difficult to define the precise role of zirconium (Zr), in terms of influencing the electron mobility and device stability.

Kim et al. [41] reported the application of an amorphous HfInZnO thin-film as an oxide semiconductor layer [Fig. 4(c) and (d)]. They suggested that adding Hf (hafnium) could suppress growth of the columnar structure, and drastically decrease the carrier concentration and Hall mobility. Also, the TFTs exhibited a decrease of μ_{fe} and an improvement in device stability, as the amount of Hf increased in the HfInZnO

Table 2 Summary of key process and property characteristics of multi-component oxide semiconductor thin film transistors [a-/p-(amorphous/ poly-crystal structure), MOCVD (metal organic chemical vapor deposition)]

Channel Materials	Deposition Method	Mobility (cm^2/V · s)	Subthreshold Swing (V/decade)	Process Temperature (°C)	Ref.
a-ZnON	Reactive sputter	10	0.8	350	[32]
p-ZnON	ALD	6.7	0.67	150	[33]
MgZnO	MOCVD	40	0.25	450	[34]
a-InZnO	Sputter	20	1.2	R.T.	[35]
a-InZnO	Sputter	4.5	0.87	40	[36]
a-InZnO	Sputter	27 (19)	ND	600 (200)	[37]
a-InGaZnO	PLD	9	ND	R.T.	[11]
a-InGaZnO	Sputter	12	0.2	R.T.	[38]
a-InGaZnO	Sputter	35.9	0.59	350	[39]
ZrInZnO	Sputter	3.9	0.98	350	[40]
a-HfInZnO	Sputter	10	0.23	200	[41]
a-SnInZnO	Sputter	24.6	0.12	300	[42]
a-AlSnInZnO	Sputter	31.4	0.14	250	[43]
SiInZnO	Sputter	21.6	1.52	150	[44]
a-ZnSnO	Sputter	5–15 (20–50)	ND	300 (600)	[45]
a-ZnSnO	PLD	10	1.4	450	[46]
ZnSnO	Sputter	14	1.6	250	[47]
a-AlZnSnO	Sputter	10.1	0.6	180	[46]
GaZnSnO	Sputter	24.6	0.38	300	[47]
ZrZnSnO	Sputter	8.9	0.7	350	[48]

matrix. Therefore, the role of the carrier-suppressor appears to influence carrier concentration, Hall mobility, and device stability due to its high oxygen-bonding ability.

Cost-efficient ZnSnO-matrix-based oxide semiconductors have been under investigation with the addition of a variety of carrier-suppressors due to the high-cost and scarcity of indium and gallium [47, 51]. Cho et al. [51] reported an amorphous AlZnSnO TFT, that exhibited μ_{fe} of 10.1 cm^2/V · s, S of 0.6 V/ decade, and drain current on/off ratio of 10^9 after annealing at 180 °C. Later, Fortunato et al. [52] developed an amorphous GaSnZnO channel layer, produced by rf magnetron co-sputtering using gallium zinc oxide (GZO) and tin (Sn) targets. The GaSnZnO TFTs exhibited high electrical performance (μ_{fe} of 24.6 cm^2/V · s, S of 0.38 V/decade, and drain current on/off ratio of 8×10^7). The researchers suggested that high post-annealing (300 °C) treatment of a-GaSnZnO TFTs produced better electrical performance and stability than those of a-IGZO TFTs due to the Ga^{3+} and Sn^{4+} ions. There have been many similar demonstrations to date involving Si, Al, Zr, Hf, Ga, and Sn with InZnO and ZnSnO matrices, aimed at improving electrical performance (e.g., μ_{fe} and stability) [38–52].

Some researchers have raised concerns about such multi-component oxide semiconductors, considering the potential for achieving non-uniform composition distributions over large areas, and the narrow process-window zones during deposition. Thus, many still look to ZnO to solve both the crystal structure and electrical performance issues. Recently, several dopants (N, In, Sn and Hf) in a ZnO matrix were investigated leading to reasonable electrical performance (μ_{fe} over 10 cm^2/V · s) and an amorphous structure; comparable with amorphous multi-component oxide semiconductors (e.g. a-InGaZnO) [32–37].

Ye et al. [32] developed zinc oxynitride semiconducting materials through reactive sputtering in which competition, between reactions responsible for the growth of hexagonal zinc oxide (ZnO) and cubic zinc nitride (Zn$_3$N$_2$), is promoted. Interestingly, the zinc oxynitride films formed an amorphous, or highly disordered, nanocrystalline structures depending on the process conditions. The Hall-mobilities of the ZnON films were 47 and 110 cm^2/V · s; at 50 and 400 °C annealing temperatures, respectively. These TFTs also exhibited high electrical performance (saturation mobility of 10 cm^2/V · s, S of 0.38 V/decade, and drain current on-to-off ratio of 8×10^7). Very recently, Kim et al. reported that the substitution of nitrogen in ZnO could improve the stability of the device on exposure to illumination, since the nitrogen in ZnON may deactivate oxygen vacancies by raising the valence band above the defect levels [37].

5 Solution processed oxide semiconductors

As mentioned above, all of the oxide semiconductors discussed above were prepared as thin films under vacuum, given the focus on optimizing the electrical properties of semiconductor materials for incorporation into thin film
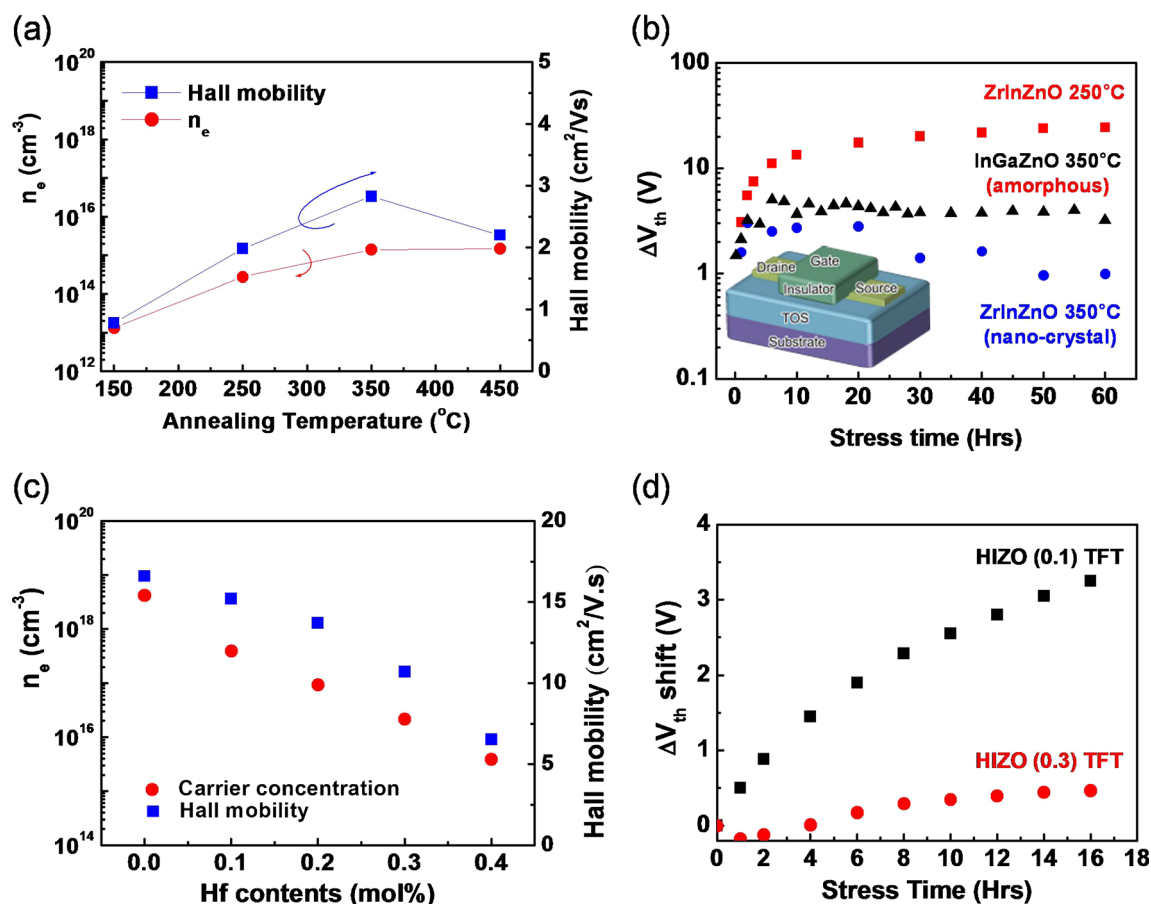
Fig. 4 (**a**) Carrier concentration and Hall mobility of ZrInZnO films for different annealing temperatures. (**b**) The variation of V_{th} for ZrInZnO TFTs annealed at 250 and 350 °C as a function of applied bias stress time. The stability data for a-InGaZnO TFT annealed at 350 °C is also presented. Reprinted with permission from [40]. Copyright 2009, Wiley-VCH Verlag GmbH. (**c**) Carrier concentration and Hall mobility as a function of Hf content (HfInZnO, HIZO) (**d**) The variation of V_{th} for the HIZO (Hf=0.1 mol%) and (Hf=0.3 mol%) TFTs as a function of bias temperature stability (BTS) time. The following condition of BTS was applied to both TFTs: V_{GS} of 20 V, V_{DS} of 10 V, and substrate temperature of 60 °C. The TFTs were kept under the BTS condition for 16 h. Reprinted with permission from [41]. Copyright 2009, American Institute of Physics

transistor devices. However, alternative electronic modules, such as printable display applications, are rapidly emerging. In this regard, solution-process methods are attractive means of fabricating oxide semiconductor materials suitable for low-cost, large area production. Oxide semiconductors, as shown in Fig. 5, are generally fabricated either by spin coating or printing an aqueous solution, and subsequent annealing in air, or in an inert atmosphere. The aprotic solvent is highly volatile and does not dissociate the metal ligand precursor. The liquid thin-film formed by the precursor, readily loses the solvent and forms a uniform film, which then absorbs moisture from the ambient air. Finally, a solid metal-oxide-thin-film is formed by the substitution reaction between water and metal ligands. Solution-processes can therefore offer an innovative cost-reducing means for increasing substrate size, reducing the number of mask steps, and eventually improving production yield [53].

Solution-processed oxide TFTs were initially fabricated with spin-coated ZnO films using Zn-nitrate [$Zn(NO_3)_2$-

$6H_2O$] in DI water. The electrical performance of the corresponding TFTs exhibited a mobility of 0.2 cm^2/V · s and an on/off ratio of 10^7 at an annealing temperature of 600 °C [54]. In terms of mobility, Ong et al. [55] were able to further increase the mobility of spin-coated ZnO-TFTs by controlled annealing at 500 °C to enhance the (002) preferred orientation of ZnO. Following this, the mobility of the TFT increased to a value as high as 5.25 cm^2/V · s. However, the process temperature is also an important factor that is critical in determining whether solution-processing is advantageous compared to other semiconductor or conventional vacuum processes. Cheng et al. [56] grew a ZnO film using chemical bath deposition (CBD) and subsequently annealing at 100 °C. They obtained a mobility of 0.25 cm^2/V · s out of a bottom-gate TFT.

Multi-component oxide TFTs have also been intensively manipulated to achieve an amorphous structure, high mobility (over 10 cm^2/V · s) and low process temperature (below 250 °C) since amorphous InGaZnO (a-IGZO), grown by

Fig. 5 A schematic illustration of solution-processed thin films based on nano-particle and precursor types
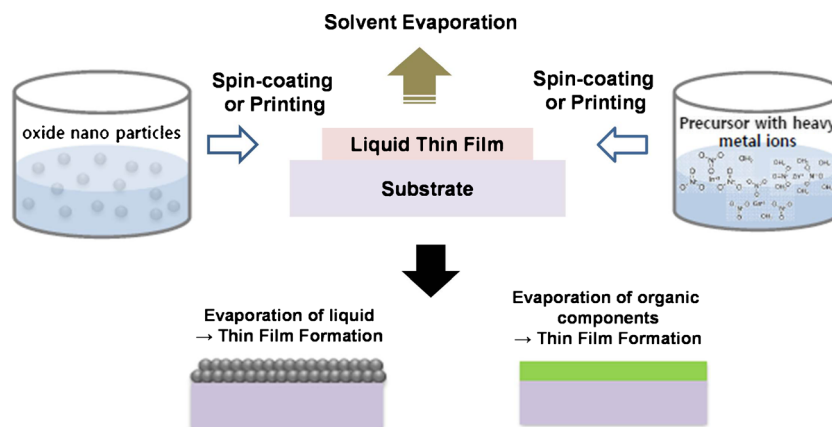
conventional vacuum processes, exhibited excellent physical and chemical properties, and electrical performance as well. Lee et al. [57] explored a general route to realize printable high-mobility-oxide semiconductors by annealing at 600 °C, using $ZnCl_2$, $InCl_2$, and $SnCl_2$ precursors dissolved in acetonitrile. The mobility values of bottom-gated TFTs with InZnO (spin-coating) and InZnSnO (ink-jet printing) were 16 and 7.4 $cm^2/V \cdot s$, respectively. Although many researchers have studied various precursors, oxide materials, and device structures, the performance of the resulting TFTs was not adequate, and mobility values were far too low, to compete with conventional vacuum processes.

Recently, in terms of high mobility and low processing temperature, four remarkably effective solution-processed approaches have been reported: 'Sol–gel on Chip', 'Combustion', 'Aqueous route', and 'Photochemical activation of Sol–gel Oxide by DUV (Deep-Ultraviolet) irradiation'.

The first process by Banger et al. [58] reported the formation of amorphous metal oxide semiconducting thin films (InZnO and InGaZnO) using a 'sol–gel on chip' hydrolysis approach from soluble metal alkoxide precursors, which resulted in an unprecedented high mobility of 10 $cm^2/V \cdot s$, reproducible and stable threshold voltages (V_{th}~0 V) and high operational stability at maximum process temperatures as low as 230 °C. At lower temperatures, the non-hydrolysed IZO samples exhibited very poor TFT performance with low mobility (>0.1 $cm^2/V \cdot s$) and large hysteresis (35 V), indicative of significant charge trapping at the semiconductor/dielectric interface. In contrast, devices fabricated using the hydrolysed process exhibited high mobility, small hysteresis (<1.2 V) and small sub-threshold slopes (S <0.5 V/decade) at annealing temperatures as low as 230 °C.

The second process reported by Kim et al. [59] used combustion-processing as a new general route to solution-growth of diverse electronic metal oxide films at temperatures as low as 200 °C, using self-energy-generating combustion chemistry. The combustion-synthesis-based oxide TFTs exhibited high mobilities (3.37 $cm^2/V \cdot s$ in In_2O_3, 1.76 $cm^2/$

$V \cdot s$ in ZnSnO, and 0.91 $cm^2/V \cdot s$ in InZnO) at low process temperatures (below 250 °C). This method therefore holds promise for achieving high-performance at low temperatures, with the opportunity to integrate amorphous oxide materials into novel electronic devices.

The third process is a simple and novel 'aqueous route' for fabricating oxide TFTs at annealing temperatures below 200 °C, suggested by several researchers [60–62]. The suggested aqueous route provides low-temperature oxide-formation and good stability by restricting the hydrolysis and condensation reactions within a solution state. An amorphous In_2O_3 thin film was obtained upon annealing at 175 °C, and the optimized TFT (200 °C) exhibited good uniformity and electrical performance (μ_{fe}=2.62±0.25 $cm^2/V \cdot s$, S=0.29±0.06 V/decade, and a turn-on voltage of 0 V) [60]. In addition, the starting Zn solutions were prepared by directly dissolving $Zn(OH)_2$ in aqueous ammonia solutions, to produce a so-called 'impurity-free precursor'. The use of zinc hydroxide allowed for low-temperature ZnO formation, indicating rapid, low-energy kinetics of metal-amine dissociation and simple dehydration and condensation reactions to form ZnO films [61, 62]. The undoped ZnO (140 °C under microwave-assisted annealing) and Li doped ZnO TFTs (300 °C annealing) exhibited remarkable performance: μ_{fe}~1.7 $cm^2/V \cdot s$ and 11.45 $cm^2/V \cdot s$ for undoped and Li-doped devices, respectively.

The fourth process is the DUV photochemical activation of sol–gel films. It plays an important role in forming high-performance, stable metal-oxide semiconductors because DUV irradiation induces efficient condensation and densification of oxide semiconducting films by photochemical activation at low temperature. As shown in Fig. 6, Kim et al. [63] reported that flexible a-IGZO TFTs, fabricated by DUV irradiation at room temperature, exhibited reasonably high mobility values of 14 and 7 $cm^2/V \cdot s$ with an Al_2O_3 gate insulator on glass and polymer substrates, respectively.

These four novel solution processes have mounted strong challenges to vacuum methods for achieving high-performance,
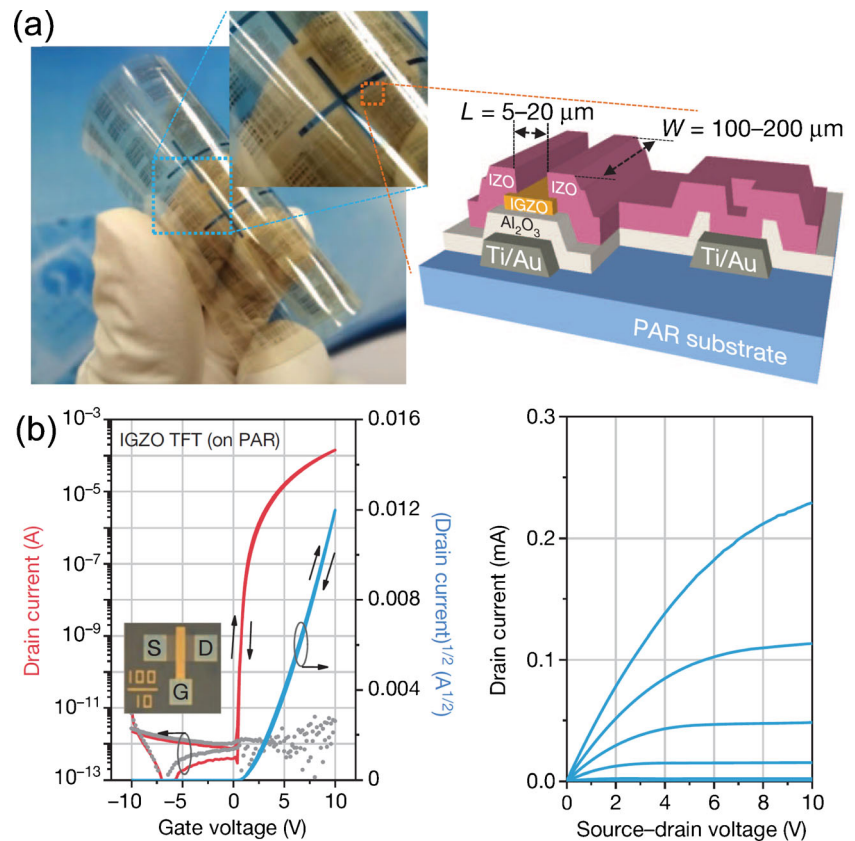
flexible, printed metal-oxide thin-film electronic devices. Although it is still necessary to improve the mobility and stability of these TFTs, it seems reasonable that solution-processed oxide TFTs will ultimately exhibit desired properties following continued development. Table 3 summarizes approaches used in solution-processed oxide semiconductors [53–73].

At present, in spite of promising research and frequent developments, the mobility and instability in oxide semiconductor TFTs must still be improved to realize the dream of achieving low cost non-silicon-based electronics. Fortunately, many researchers continue to search for more stable and efficient multi-oxide semiconductors, pursue an improved understanding of the mechanisms of instability, while considering how to achieve desired electrical properties, homogenous structures, lower-cost processes, process-adaptability for large areas, and bias-temperature-reliable materials.

6 Gate dielectric materials

High-k dielectric materials play an increasingly important role in the miniaturization of microelectronic components. The need to maintain a high capacity in spite of shrinking dimensions can no longer be accommodated by reductions in the thickness of

SiO_2 and other low-k dielectrics, as structures are moving towards the nm thickness range. As described previously, thin film transistors (TFTs) are composed of a semiconductor channel, gate insulator, source, drain, and gate electrodes. Among them, the semiconductor channel is the most important element since it governs the major characteristics of the device (e.g., field-effect mobility, on/off current ratio, threshold voltage, and subthreshold swing). In addition, the interface properties between the semiconductor channel layer and gate insulator are considered key parameters for improving reliability as well as performance (e.g., charge trap density, threshold voltage, and sub-threshold swing) of the TFTs. In particular, the operation voltage of TFTs is determined by the capacitance level, which is directly related to the dielectric constant and the thickness of dielectric layers [74–76]. According to Eqs. 1 and 2 describing the TFT drain current I_{DS} [77], a viable approach towards increasing the drain current, while operating at low bias, is to increase the capacitance of the dielectrics; for a planar structure, $C_i = \varepsilon_0(kA/d)$, where k is the dielectric constant, A the area of the electrodes, and d the dielectric thickness.

In this regard, significant attention has been paid to gate insulators, especially optimized for oxide TFTs because their switching voltage can be markedly reduced using high-k dielectric layers or very thin gate dielectric films, leading to

Table 3 Listing of solution-processed oxide semiconductors including key process and property characteristics

Material	Coating	Solut. Type	μ_{fe} (cm^2/V · s)	Temp. (°C)	Ref.
ZnO	SC	Precursor	0.2	700	[54]
ZnO	CBD	Precursor	0.25	100	[56]
ZnO	SC	Precursor	5.25	500	[55]
ZnSnO	SC/IJ	Precursor	16	600	[57]
ZnInO	IJ	Precursor	7.4	600	[57]
ZnO	IJ	Precursor	1.8	150	[64]
ZnZrO	SC	Precursor	0.0042	300	[65]
InZnO	SC	Precursor	7.3	500	[66]
nc-IGZO	SC	Precursor	7.84	400	[67]
IZTO	IJ	Precursor	30	600	[68]
AIO	SC	Precursor	19.6	350	[69]
a-ZnSnO	SC	Precursor	5	500	[70]
a-InZnO	SC	Precursor	5	350	[71]
ZnInSnO	SC	Precursor	10~100	400	[72]
InGaZnO	SC	Precursor	2.3	95	[73]
a-IZO a-IGZO	SC	Precursor	10	<250	[58]
In$_2$O$_3$ a-InZnO	SC	Precursor	3.37 1.76	<250 <250	[59]
In$_2$O$_3$	SC	Precursor	2.62	200	[60]
ZnO	SC	Precursor	1.7	140	[61]
Li-ZnO	SC	Precursor	11.45	300	[62]
a-IGZO	SC	Precursor	14	<100	[63]

SC spin coating, *IJ* ink jet, *CBD* chemical bath deposition

high capacitance values. Low-voltage operation in oxide-based TFTs result in cost savings by enabling use of lower-cost driver electronics and by low battery power consumption, making them suitable for portable applications. There are several types of dielectric layers which have been used in oxide-based TFTs. They include polymers [78, 79], high-k metal oxides [80, 81], SiO$_2$ [82, 83], Si$_3$N$_4$ [84, 85], and hybrid dielectrics composed of multi-layered films [86, 87].

SiO$_2$ layers have to date been widely utilized in most types of TFTs as the gate insulator due to their easy fabrication by chemical vapor deposition (CVD) and their optimized film properties, including precise thickness control and uniform large-area coverage. However, the rather low dielectric constant (~3.9) and relatively high growth temperatures (>300 °C) of SiO$_2$ layers are major limitations in the fabrication of SiO$_2$ dielectric layers on plastic substrates (i.e., polyethylene terephthalate or polycarbonate) with low glass-transition temperature. Although a high capacitance value can be obtained by the introduction of very thin SiO$_2$ dielectric layers (less than 20 nm), we note that pinhole formation and poor step-coverage on relatively rough plastic substrates are detrimental to the homogeneous coating of thin dielectric layers on plastic substrates [88, 89].

Similar problems are associated with polymer-based dielectric layers with relatively low dielectric constants. Although very low voltage operation has been successfully demonstrated through the use of several polymer dielectrics (i.e., SAM (self-assembled monolayer) [90, 91], SAS (self-assembled super-lattice) [92], CPB (cross-linked polymer blend) [93], PVA [poly(vinyl alcohol)] [94], PMMA [poly(methyl methacrylate)] [79], and PVP [poly(4-vinylphenol)] [95, 96]), good TFT performance with such layers has been achieved only on very smooth Si wafers or well-surface-treated, smooth-plastic substrates. Thus, inherent (bare) polymer substrates, characterized by rough surfaces (rms roughness ~3 nm), benefit from the use of high-k dielectrics given that high electric fields can be achieved with the use of thicker films (~200 nm) without need to increase the operating voltage.

The use of such high-k oxide films with sufficient thickness (>100 nm), leads to the suppression of pinhole formation and minimization of problems associated with step coverage. Normally, high temperatures are required to obtain the crystalline form of high-k, dielectric-oxide thin films, given their typical refractory nature. In 1999, researchers at IBM first demonstrated room temperature grown amorphous Ba(Zr,Ti)O$_3$ (BZT) thin films as a gate insulator [74]. The rf-sputtering method was used to grow 122 nm thick BZT films (k=17.3). The pentacene-based organic TFTs with BZT gate insulators showed much lower voltage operation (<14 V) as compared to that (~100 V) of the pentacene TFTs using SiO$_2$ dielectric layers [Fig. 7]. Although the IBM group successfully demonstrated the potential suitability of room-temperature grown high-k gate insulators combined with organic semiconductors for the first time, the relatively low breakdown characteristics and high leakage current characteristics of the gate insulators prepared at room temperature were major drawbacks. These need to be solved to provide stable and reliable operation of oxide TFTs. Here, we provide an overview of various gate oxide insulators in terms of structural, compositional and dielectric properties. A number of promising gate insulators have been suggested and developed, particularly for low voltage operation of oxide TFTs.

7 Binary oxide dielectrics

A number of binary oxide-based gate insulators with relatively high dielectric constant values (k=10–40) have been investigated as alternative gate dielectrics to replace SiO$_2$. These medium or high-k binary oxides include Al$_2$O$_3$, HfO$_2$, TiO$_2$, ZrO$_2$, Y$_2$O$_3$, La$_2$O$_3$, and Ta$_2$O$_5$, and their material properties (i.e., optical band gap, crystal structure, dielectric constant, and breakdown strength) were summarized in Table 4 [97–117]. In particular, the potential feasibility of the usage of high-k binary oxides (Al$_2$O$_3$ (k=8.5) [33], HfO$_2$ (k=20.1) [118], TiO$_2$ (k=40) [119], ZrO$_2$ (k=25) [120], Y$_2$O$_3$ (k=14)
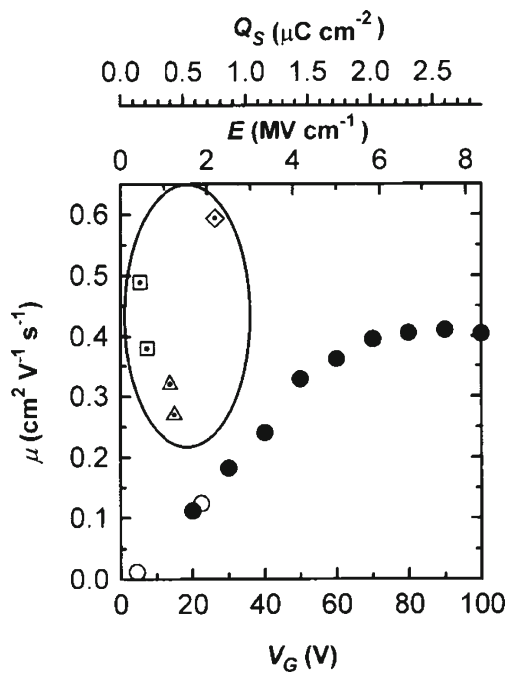
Fig. 7 Dependence of mobility on V_G, E, and Q_S. *Solid circles* refer to all three x axes and correspond to devices with 0.12-μm-thick SiO$_2$. *Open circles* refer only to E and Q_S axes (0.5-μm-thick SiO$_2$). *Dotted* symbols in ellipse refer to the E axis only. *Triangle*, BZT; *square*, BST; *diamond*, Si$_3$N$_4$ insulator. Reprinted with permission from [74]. Copyright 1999, AAAS

[39], La$_2$O$_3$ (k=10.8) [121], Ta$_2$O$_5$ (k=20.3) [121]) has been demonstrated for application in ZnO-based oxide TFTs, as summarized in Table 5. However, a common limitation of near room temperature grown high-k dielectric films is their tendency to suffer from poor leakage current characteristics, which is detrimental to TFTs operation. In addition, the large polarizability of the high-k insulators has an adverse effect on their mobility [119]. These issues should thus be carefully addressed to insure widespread application of high-k gas insulators. In general, a binary oxide with a high dielectric constant typically possesses a smaller band gap, which is can be correlated with lower breakdown strength. In contrast, a binary oxide with a wide band gap typically has a smaller dielectric constant. Therefore, it is very important to understand that adoption of binary oxides involves a trade-off between breakdown strength and dielectric constant. As an example, Pei et al. [123] fabricated HfO$_2$-Al$_2$O$_3$ (HfAlO) composite insulators by rf co-sputtering HfO$_2$ and Al$_2$O$_3$ ceramic targets. As shown in Fig. 8, their optimized HfAlO films $[(HfO_2)_{0.86}(Al_2O_3)_{0.14}]$ showed larger band gap (~5.58 eV) and smaller dielectric constant (~16), compared to those (~5.31 eV and ~17.7, respectively) of pure HfO$_2$. Eventually, they were able to significantly reduce the leakage current density from ~1×10^{-2} A/cm^2 to below 3×10^{-10} A/cm^2, at an electric field strength of 0.25 MV/cm. Kim et al. [124] also proposed new types of Mg$_2$Hf$_5$O$_{12}$ gate insulators to improve

Table 4 Summary of material properties of binary oxide insulators

Binary Oxide	Al$_2$O$_3$	HfO$_2$	TiO$_2$	ZrO$_2$	Y$_2$O$_3$	La$_2$O$_3$	Ta$_2$O$_5$
Optical Band gap, Eg (eV)	8.8 eV [97]	5.5~6.0 eV [98–100]	3.0~3.5 eV [101]	5.0~7.0 [102]	6 [97]	4.3~6 [97, 103]	4.4 [97]
Crystal Structure	Rhombohedral (Trigonal): >1000~1100 °C [104]	Monoclinic: <1022 °C; Tetragonal: 1022~2422 °C; Cubic: >2422 °C [105]	Tetragonal: Anatase: <600 °C; Rutile: >700 °C [106]	Monoclinic: <1170 °C; Tetragonal: 1170~2370 °C; Cubic: 2370~2680 °C [107, 108]	Monoclinic: <500 °C; Cubic: >500 °C [109]	Hexagonal: <300 °C; Cubic: >300 °C [110]	Orthorhombic: 400~1450 °C; Tetragonal: >1450 °C [111]
Relative Dielectric Constant	8.8 [112]	22~25 [99]	Anatase: 30; Rutile: 80~170 [106, 113]	22~24 [102]	13~17 [114]	27~30 [103, 112]	22 [112]
Breakdown Strength (MV/cm)	11.2~13.8 [115]	3.9~6.7 [115]	1.4~2.5 [106]	3.3~5.7 [115]	1.9~3.0 [116, 117]	3.3~5.6 [115]	2.1~3.7 [115]

Table 5 Comparison of key processing and property characteristics of ZnO-based oxide TFTs with binary oxide insulators

Gate Insulator Materials	Deposition Method	Mobility ($cm^2/V \cdot s$)	Subthreshold Swing (V/decade)	Process Temperature (°C)	Ref.
Al_2O_3 (k=8.5)	ALD	6.7	0.67	150	[33]
HfO_2 (k=20.1)	rf sputter	3.53	0.095	300	[118]
TiO_2 (k=40)	ALD	9.9	0.22	250	[119]
ZrO_2 (k=25)	rf sputter	28	0.56	R.T.	[120]
Y_2O_3 (k=14)	rf sputter	12	0.2	140	[39]
La_2O_3 (k=10.8)	ALD	0.77	1.2	150	[121]
Ta_2O_5 (k=20.3)	rf sputter	40.5	0.23	R.T.	[122]

leakage-current characteristics by combining relatively low-k MgO (k~10) and high-k HfO_2 (k=20.1), as shown in Fig. 9. Polycrystalline, single-phase $Mg_2Hf_5O_{12}$ thin films exhibited greatly enhanced leakage current characteristics ($<2 \times 10^{-7}$ A/cm^2) compared to that (2×10^{-5} A/cm^2) of HfO_2 thin films at 0.4 MV/cm and a high dielectric constant (k=22). The optical band gap of $Mg_2Hf_5O_{12}$ is ~0.16± 0.02 eV larger than that (5.67±0.02 eV) of HfO_2. $InGaZnO_4$ TFTs using $Mg_2Hf_5O_{12}$ gate insulators, which were fabricated on plastic substrates, showed a high field-effect mobility of 27.32 $cm^2/V \cdot s$ and a current on/off ratio of 4.01×10^6. These reports highlight the importance of the manipulation of composition to achieve high dielectric constants as well as improved breakdown strength.

For routine application of high-k binary oxides as gate dielectrics, further investigation of their chemical stability, interfacial trap density distribution, and related device instability have to be performed. Kwon et al. [125] studied the effect of gate dielectric material on the device stability of a-HfInZnO TFTs. It was observed that the Al_2O_3 gated device

exhibited a stability comparable to a conventional device with the SiO_2 gate dielectric (promising for future applications), while the HfO_2 device suffered from a huge negative threshold voltage shift (>11 V) during application of negative-bias-thermal illumination stress for 3 h [Fig. 10]. Their work suggests that HfO_2 normally contains a large number of trap sites or fixed charges, which have to be significantly reduced for its practical application. For example, Zou et al. [126] suggested that nitrogen incorporation into HfO_2 can effectively improve the interface quality and thus enhance the reliability of resulting a-IGZO TFTs with HfO_xN_y gate dielectrics. They demonstrated that the density of interface state (~5.2× 10^{11} eV^{-1} cm^{-2}) of the HfO_xN_y/a-IGZO device is smaller than that (~1.1×10^{12} eV^{-1} cm^{-2}) of the reference HfO_2/a-IGZO, because nitrogen incorporation in the dielectric film can effectively passivate unsaturated dangling bonds, and hinder the diffusions of Hf and Ga.

8 Perovskite-based oxide dielectrics

Among perovskite oxides, (Ba,Sr)TiO_3 (BST) has attracted much attention as a high-k dielectric material for application in storage capacitors of gigabit dynamic random-access memory (DRAM), ferroelectric random-access memory (FRAM), and electrically tunable microwave devices due to its superior properties (e.g., high dielectric constant, high dielectric breakdown strength, and low dissipation factor) [127–131]. In particular, the capacitive properties of BST can be tuned by more than 50 % at low bias levels (<5 V) resulting in similar percentage changes in frequency characteristics of tuned circuits [130, 131]. For the above-mentioned applications, BST films have been grown at high processing temperatures, typically above 600 °C, due to its refractory nature [128, 132]. However, layers of BST grown at high temperature are not suitable as gate insulator for oxide TFTs, particularly those fabricated on plastic substrates.

Dimitrakopolous et al. first proposed the potential use of room-temperature deposited barium strontium titanate BST film (k=16) as a high-k gate dielectric for making low-voltage operating organic TFTs [74]. Following this
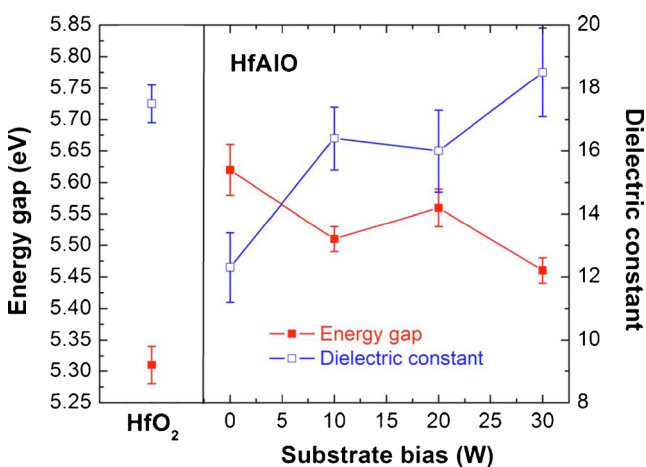

Fig. 8 Energy gap calculated from spectroscopic ellipsometry (SE) results and the dielectric constant determined from capacitance-voltage measurements in accumulation regime for HfAlO films deposited with different substrate biases. The values for pure HfO_2 are also presented. Reprinted with permission from [123]. Copyright 2009, The Electrochemical Society

Fig. 9 (a) The relationship between the dielectric constant and the electric field in HfO_2 and $Mg_2Hf_5O_{12}$ thin films deposited at room temperature. (b) The relationship between the leakage current characteristics and the electric field applied to the HfO_2 and $Mg_2Hf_5O_{12}$ thin films. Reprinted with permission from [124]. Copyright 2010, The Electrochemical Society
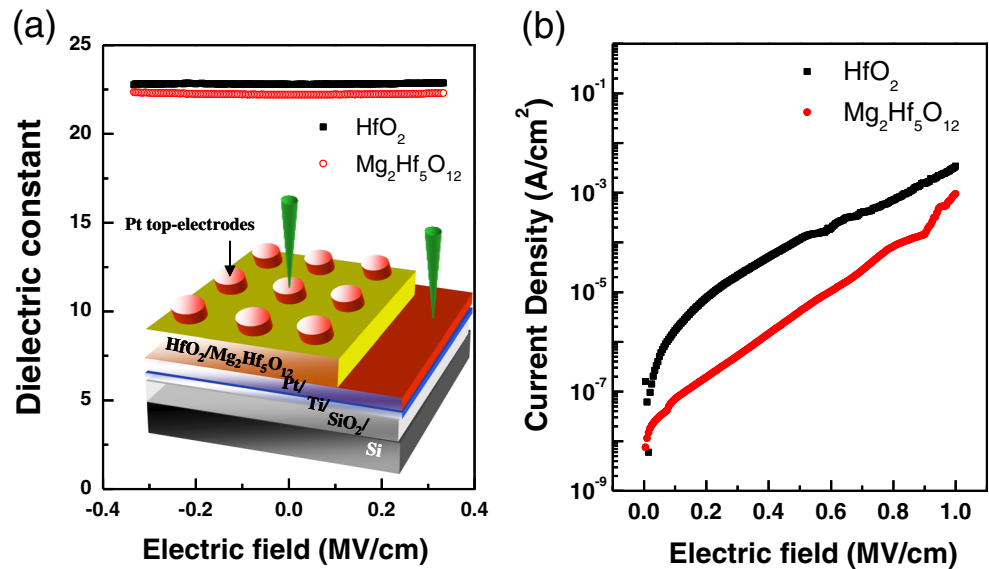
technological breakthrough, a number of research groups have searched for BST-based high-k gate insulators for ZnO-based oxide TFTs, as summarized in Table 6. The voltage-dependent, dielectric-constant characteristic of high-temperature-grown BST dielectrics with polycrystalline nature is an attractive feature for application in tunable microwave devices. However, this behavior is less desirable when attempting to achieve low-voltage and high-frequency

Fig. 10 (a) Evolution of the transfer characteristics for (a) SiNx/HIZO, (b) SiNx/HfOx/HIZO, and c SiNx/SiOx/HIZO devices as a function of the applied NBITS time for the HIZO TFT with various gate dielectric materials and structures. Reprinted with permission from [125]. Copyright 2010, American Institute of Physics
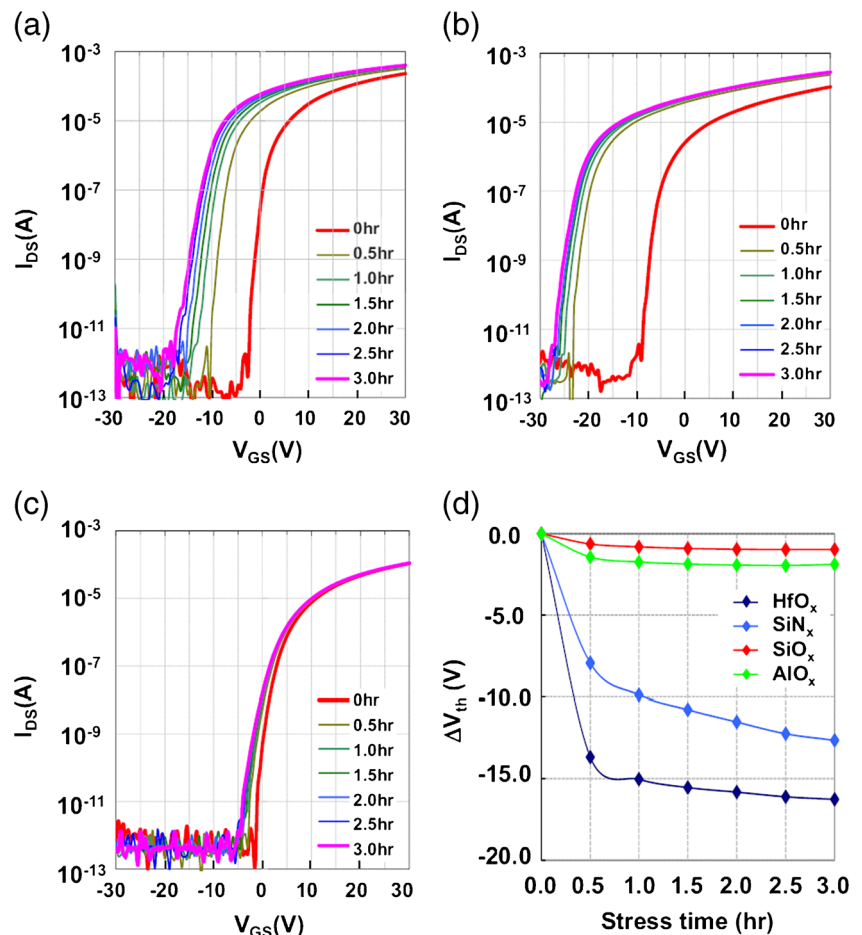
Table 6 Comparison of key processing and property characteristics of ZnO-based oxide TFTs with perovskite oxide insulators

Gate Insulator Materials	Deposition Method	Mobility (cm^2/V · s)	Subthreshold Swing (V/decade)	Process Temperature (°C)	Ref.
BST (k=28)	rf sputter	10	0.06	325	[133]
Mg-BST (k=28)	rf sputter	16.3	0.4	R.T.	[134]
Mn-BST (k=24)	rf sputter	1.0	ND	R.T.	[135]
Ni-BST (k=26.5)	rf sputter	2.2	0.21	300	[136]
MgO-BST (k=18)	rf sputter	10.9	0.46	R.T.	[137]
PMMA/BST (k=19.5)	rf sputter	10.2	0.44	R.T.	[138]

operating TFTs. Interestingly, room-temperature-grown BST films prepared by rf-sputtering exhibit an amorphous structure; thus the tunable dielectric behavior of BST films is not an issue [Fig. 11]. While the relative dielectric constant of the amorphous phase (k=28) is smaller than that of the polycrystalline phase (k >200), amorphous BST films with sufficiently high capacitance density possess a large voltage and frequency independent dielectric constant, which is desirable for the fabrication of room-temperature-processed, ZnO-based TFTs [inset of Fig. 11]. Kim et al. [133] fabricated high-performance top-contact bottom-gate a-IGZO TFTs utilizing a 170 nm thick amorphous BST as gate insulator. They demonstrated low-voltage operation (<3 V) with a high saturation mobility value of 10 cm^2/V · s, an excellent sub-threshold swing of 60 mV/decade, and a low threshold voltage of 0.5 V, as shown in Fig. 12. Li-Ping et al. [139] also reported the fabrication of low-voltage, depletion-mode-operating, indium-tin-oxide (ITO) TFTs gated by an amorphous BST gate dielectric. Their BST films, with a thickness of 400 nm,

showed a leakage current density of 6×10^{-8} A/cm^2 (at an applied electric field of 0.125 MV/cm) and a high dielectric constant of ~37. The ITO TFT devices exhibited a threshold voltage of −3.7 V, a sub-threshold swing of 0.5 V/decade, and
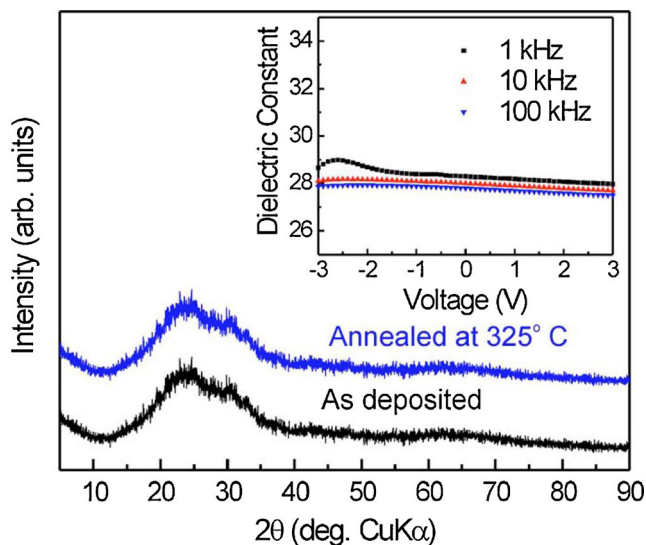

Fig. 11 XRD patterns of a-BST film on glass substrate as deposited at room temperature and after annealing at 325 °C for 1 h. *inset*: Dielectric constant measured on a Au/Ti/a-BST/ITO/glass sample as a function of bias voltage and at 1, 10, and 100 kHz. Reprinted with permission from [133]. Copyright 2008, American Institute of Physics
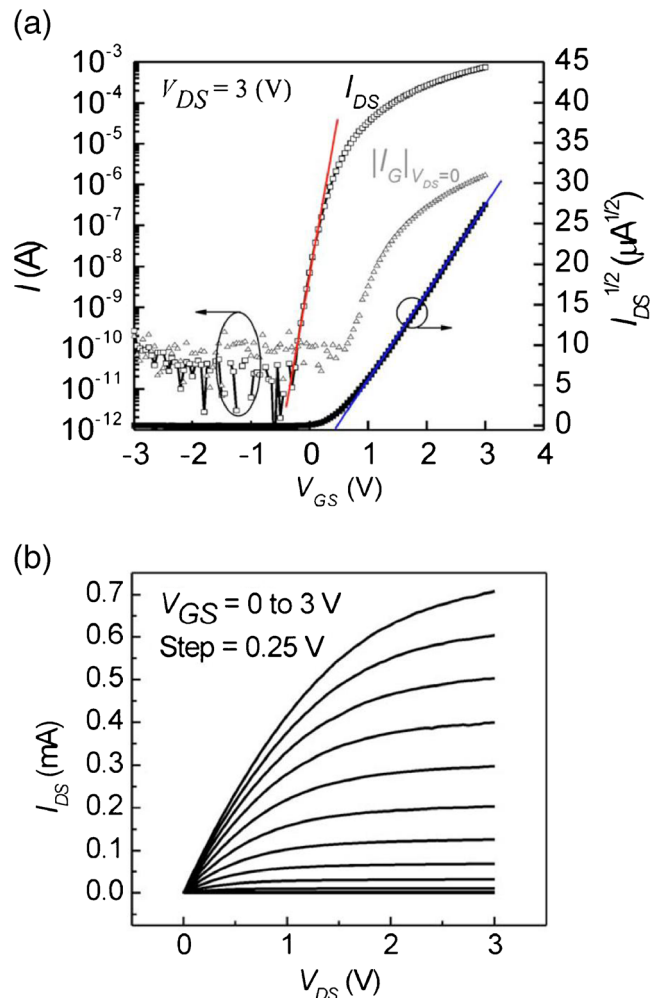
Fig. 12 Operation characteristics of sputtered a-BST/a-IGZO TFT with L=5 μm and W=1000 μm. (**a**) Transfer characteristics (*squares*) V$_{GS}$ was swept from −3 to +3 V and leakage current (*triangles*) at V$_{DS}$=0 V. (**b**) Output characteristics. V$_{DS}$ was swept from 0 to +3 V at each V$_{GS}$ varied from 0 to 3 V at 0.25 V steps. Reprinted with permission from [133]. Copyright 2008, American Institute of Physics

a field-effect mobility of 3.2 cm^2/V · s. While there have been some earlier promising results for high-performance TFTs with amorphous BST gate dielectrics, room-temperature grown BST films generally suffered from poor leakage current characteristics at voltages above 5 V, which is detrimental to stable operation of TFTs (see Fig. 13).

In order to improve leakage current characteristics (i.e., enhancement of breakdown strength, of room-temperature-grown BST thin films), doping the amorphous BST host with acceptor dopants (i.e., Mn, Ni, and Mg) which partially substitute for Ti on the B site of the A^{2+}B^{4+}O^{2-} perovskite structure, has been suggested [134–136]. On the basis of the similar ionic radii of Ti^{4+} (r_{eff}=0.605 Å) and Mg^{2+} (r_{eff}=0.72 Å) in six-fold oxygen coordination, we can assume that Ti^{4+} is replaced by Mg^{2+} in the BST lattice. For example, based on simple defect chemistry, negatively charged defects (Mg$_{Ti}''$) and a corresponding number of doubly ionized oxygen vacancies (V$_O^{..}$) are simultaneously formed to satisfy site balance and charge neutrality. This can be described as:

$$MgO \xrightarrow{TiO_2} Mg_{Ti}'' O_O + V_O^{..} \qquad (3)$$

In this case, Mg behaves as an acceptor-type dopant, which can prevent reduction of Ti^{4+} to Ti^{3+} by neutralizing the donor action of the oxygen vacancies. For example, at the low oxygen partial pressures used to deposit BST film, reduction

occurs with the formation of oxygen vacancies, resulting in n-type conductivity according to:

$$O_O \rightarrow V_O^{..} + 2e' + 1/2 \, O_2(g) \qquad (4)$$

where O$_O$, V$_O^{..}$, and e′ represent the oxygen ion on its normal site, the oxygen vacancy, and electron, respectively. By increasing in the oxygen vacancy concentration by Mg doping, reaction 4 is driven back to the left, causing a decrease in the concentration of electrons, and thereby an enhancement of the breakdown strength of Mg-doped BST thin films. In agreement with these arguments, the leakage current density (<5×10^{-8} A/cm^2 at 2 MV/cm) of 3 % Mg-doped BST film is markedly reduced compared to undoped BST films (<3×10^{-4} A/cm^2 at 0.4 MV/cm), as shown in Fig. 13. The valence state of an Mg ion is 2+, thus we can expect further reduction in the leakage current density in Mg-doped BST films compared to BST films doped by acceptors with the higher multi-valence states.. Kang et al. [134] suggested the potential suitability of a 3 % Mg-doped BST gate insulator for high field-effect mobility (16.3 cm^2/V · s) TFTs fabricated on PET substrates. Kim et al. [136] reported the successful integration of 1 % Ni-doped BST as a gate dielectric for ZnO TFTs exhibiting a very low operation voltage (4 V), field-effect mobility (2.2 cm^2/V · s), on/off current ratio (1.2×10^6), and subthreshold swing (0.21 V/decade). ZnO TFTs with 3 % Mn-doped BST showed a field-effect mobility of 1.0 cm^2/V · s and a low operating voltage of less than 7 V [135]. These results were based on a-BST small amounts of acceptor dopants (<5 %).

To further improve the leakage current properties of room-temperature-grown BST films, Kim et al. [137] fabricated MgO-BST composite thin films (i.e., excess MgO-loaded BST). With increasing MgO content, the leakage current was indeed significantly suppressed, as shown in Fig. 14. A remarkable reduction in the leakage current density (below ~1×10^{-7} A/cm^2 even up to an applied electric field of 0.5 MV/cm) could be achieved with a composition ratio of MgO$_{0.3}$BST$_{0.7}$. It is interesting to see the high resolution TEM image of MgO$_{0.3}$BST$_{0.7}$ film, suggesting a locally dispersed nanocrystalline MgO phase in an amorphous BST matrix (Fig. 15). The uniform distribution of MgO nanoparticles serves to suppress leakage current flow within the BST matrix due to their excellent insulating characteristics. Furthermore, low-voltage operation (4 V), high-performance a-IGZO TFT (μ_{fe}=10.9 cm^2/V · s) could be demonstrated by use of the MgO$_{0.3}$BST$_{0.7}$ gate dielectric on plastic substrates.
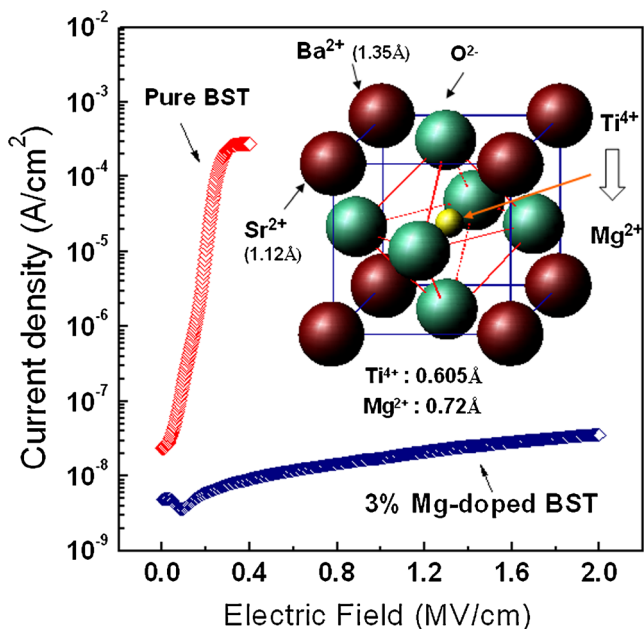

Fig. 13 Current-density-electric-field characteristics of pure BST and 3 % Mg-doped BST film. The *inset* shows a schematic structure for Mg substitution into Ti site in BST lattice. Reprinted with permission from [134]. Copyright 2007, American Institute of Physics

9 Pyrochlore based oxide dielectrics

Bi-based pyrochlore materials with A$_2$B$_2$O$_7$ composition (e.g., Bi$_{1.5}$Zn$_{1.0}$Nb$_{1.5}$O$_7$, hereafter, BZN) have been widely

Table 7 Comparison of key processing and property characteristics of ZnO-based oxide TFTs with pyrochlore oxide insulators

Gate Insulator Materials	Deposition Method	Mobility $(cm^2/V \cdot s)$	Subthreshold Swing (V/decade)	Process Temperature (°C)	Ref.
BZN (k=51)	rf sputter	1.13	ND	R.T.	[81]
BZN (k=70)	PLD	42	0.24	100	[140]
MgO/BZN (k=31.5)	rf sputter	5.4	ND	R.T.	[86]
MgO-BZN (k=32)	rf sputter	37.2	0.46	R.T.	[141]

investigated for various applications of voltage-tunable microwave devices and integrated decoupling capacitors [141–144]. Interestingly, the low dielectric loss tangent (tan δ) of 5×10^{-4} and the high resistivity ($\sim3\times10^{13}$ Ωcm) would normally make BZN films highly suitable for microwave regime applications, except for the fact that they exhibit low tunability [144]. However, for TFT operation, the low-voltage dependence of the dielectric constant ensures more predictable operation (Table 7). Kim et al. [81, 145] developed room-temperature-deposited, BZN gate insulators with enhanced leakage current characteristics ($<10^{-7}$ A/cm^2 for voltages below 4 V) and high relative dielectric constant (~51); thereby leading to low-voltage operating (<4 V) ZnO TFTs. Also, it is noted that the BZN films exhibit the highest relative dielectric constant (above 50), among room-temperature-grown, high-k gate insulators prepared by physical vapor deposition such as sputtering. Fu et al. [140] also successfully fabricated high-performance ZnO nanowire (NW) TFTs combined with low-temperature (~100 °C) PLD-grown BZN (k= 70) as gate insulator. The NW transistors exhibited a low

operation voltage (<3 V), a high field-effect mobility (~42 cm^2/V · s), and a steep subthreshold swing up to 0.24 V/decade. BZN films have a cubic, pyrochlore-like structure even for deposition at room temperature [see Fig. 16]. The BZN films exhibit a partially nanocrystalline morphology with a crystalline size distribution of 5–8 nm in diameter [inset of Fig. 17]. Therefore, the high dielectric constant achievable with BZN, even when processed at room temperature, can be understood on the basis of its crystalline-like structure (i.e., better short range order). However, room-temperature-deposited BZN films were shown still to be largely unreliable ($>5\times10^{-5}$ A/cm^2) with respect to their leakage current characteristics at high applied electric fields (above 0.3 MV/cm) [86, 146]. Therefore, further optimization was necessary to improve breakdown strength and reduce leakage current for room-temperature-grown BZN films.

MgO, with a relative dielectric constant of 9.96 and a high band gap of 7.3 eV, has been used as a protective or an intermediate buffer layer in various electronic devices due to its excellent insulation properties [147–149]. Lim et al. [86] demonstrated that the introduction of an insulating, MgO-capping layer onto the BZN films could improve the leakage current characteristics of BZN films (i.e., below 3×10^{-8} A/cm^2 at an applied electric field of 0.5 MV/cm). Recently, Cho et al. [146] reported the preparation of excess MgO-added BZN-composite thin films from a single composite target, rather than two-step thin-film deposition of BZN and MgO films. The two-step process is not desirable in terms of high processing cost and low manufacturing yield. The MgO$_{0.3}$BZN$_{0.7}$ composite gate insulators exhibited greatly enhanced leakage-current properties ($<2\times10^{-8}$ A/cm^2 at 0.3 MV/cm), while retaining an appropriate high relative dielectric constant of 32. Finally, the ZnO TFTs incorporating the MgO-BZN composite gate insulator showed superior TFT performance including a high field-effect mobility of 37.2 cm^2/V · s, a reasonable on/off ratio of 1.5×10^{5}, a sub-threshold swing of 0.46 V/decade, and a low threshold voltage of 1.7 V [see Fig. 18].

As a concluding remark, for the application of BZN- and BST-based oxides as gate insulators in oxide TFTs, it is highly necessary in future research to investigate the interfacial trap density and long-term device stability (i.e., temperature, illumination, mechanical stress, voltage, or current stability) under real operating conditions.
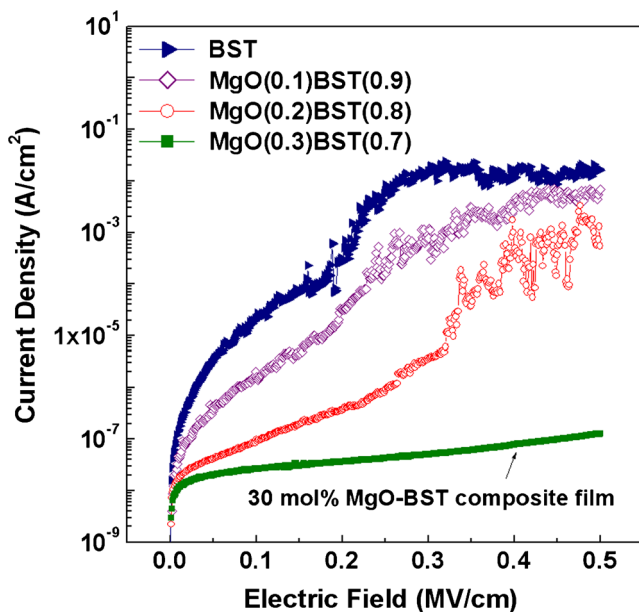

Fig. 14 Leakage current characteristics of pure BST and MgO-BST composite thin films deposited by PLD. Reprinted with permission from [137]. Copyright 2008, American Institute of Physics

Fig. 15 (a) HR-TEM image of pure BST thin films. The inset exhibits a selected area diffraction pattern of the BST thin film. (b) HR-TEM image of MgO-BST composite thin film. The *inset* shows the lattice fringe of the MgO nanoparticles. Reprinted with permission from [137]. Copyright 2008, American Institute of Physics
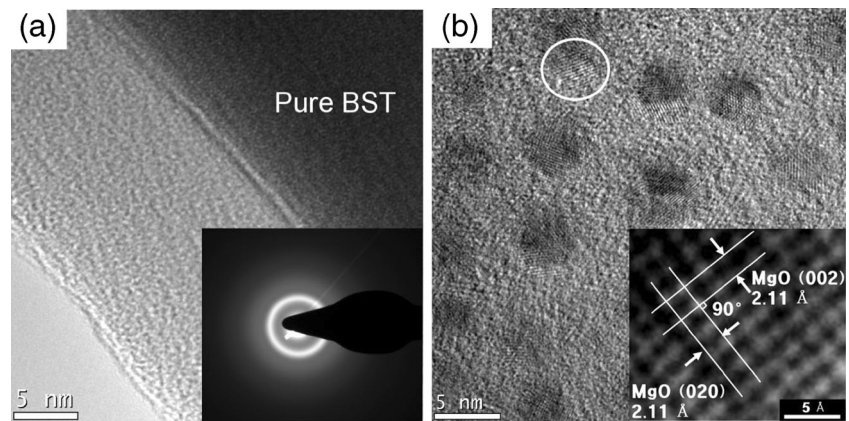
10 Current TFT oxide issues

Oxide semiconductor-based TFTs have been successfully developed and integrated into flat panel displays. Oxide TFTs including ZnO and InGaZnO$_4$ semiconducting channel layers have also driven the creation of novel transparent electronics. However, many researchers and engineers still have concerns regarding several challenging issues that need to be overcome in order to realize mass production of oxide semiconductor-based TFTs. In particular, further improvements in terms of mobility and stability are required. For this purpose, all constituent layers in TFTs, including oxide semiconductor, gate insulator, gate/source-drain electrode, and passivation layer

need to be carefully optimized. This work is summarized in Fig. 19.

11 Demand for higher mobility

The current flat panel display (FPD) industry is being driven towards the development of high definition ("Ultra Definition"), large area (>70 in.), high frame rate (>240 Hz), and three-dimensional (3D) displays. In order to realize such high-end products such as 3D televisions that do not require specialized glasses, using either active matrix liquid crystal displays (AMLCDs) or active-matrix, organic light-emitting-diode (AMOLED) panels, high-performance thin film transistor (TFT) devices acting as switching or driving elements are
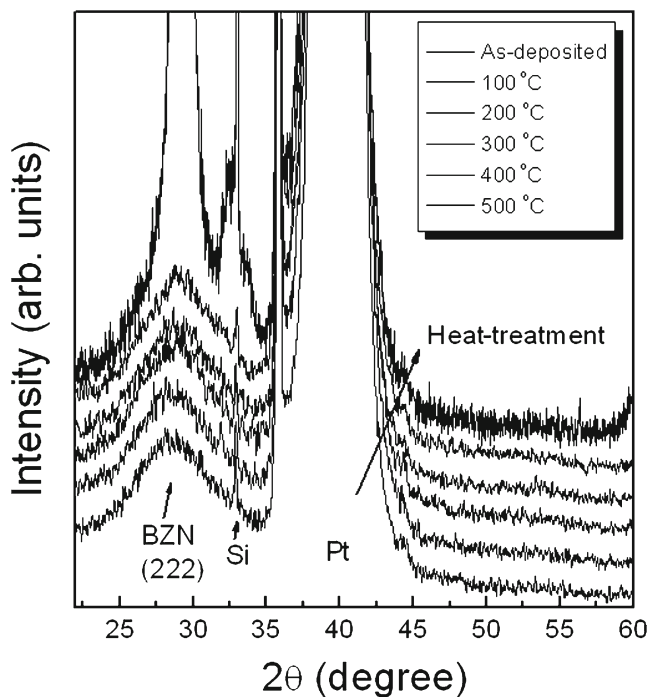

Fig. 16 X-ray diffraction pattern of BZN films as a function of annealing temperature. Reprinted with permission from [81]. Copyright 2006, American Institute of Physics
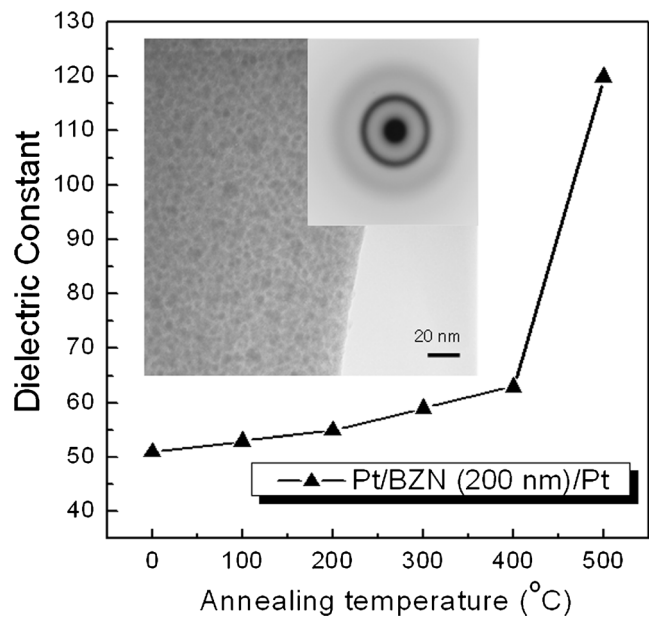

Fig. 17 Dielectric constant of BZN films as a function of annealing temperature. The *inset* shows diffraction pattern and TEM images of BZN films. Reprinted with permission from [81]. Copyright 2006, American Institute of Physics

Fig. 18 (**a**) A schematic diagram of ZnO-TFTs with $MgO_{0.3}BZN_{0.7}$ gate insulator on glass substrate, (**b**) output characteristics of ZnO-TFTs using a $MgO_{0.3}BZN_{0.7}$ insulator. V_{DS} was swept from 0 V to +6 V in step of 0.02 V, (**c**) transfer characteristics of ZnO-TFTs using a $MgO_{0.3}BZN_{0.7}$ insulator. V_{GS} was swept from −1 V to +6 V and from −1 V at V_{DS} of 4 V [channel length (L) of 150 μm and channel width (W) of 2000 μm]. Reprinted with permission from [146]. Copyright 2010, Elsevier
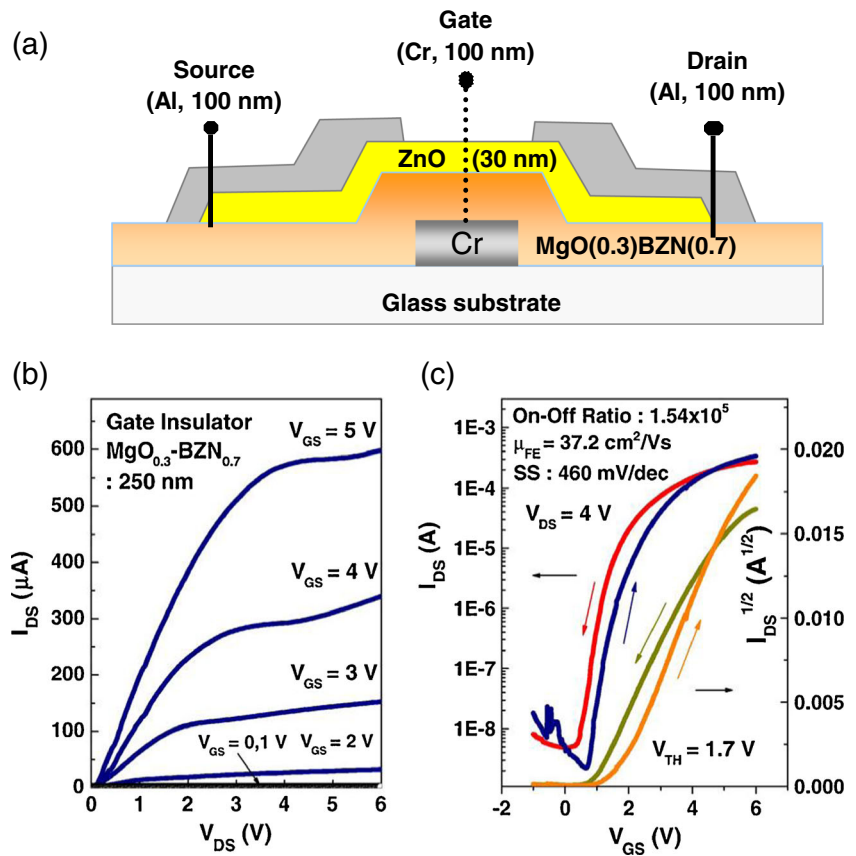
necessary, preferably with field-effect mobility values exceeding 20 cm^2/V · s [12, 150]. For example, for large AMOLED TVs, the mobility requirement is generally predicted to be over 30 cm^2/V · s (depending on display resolution and pixel-circuit designs) because OLED pixels need high current in order to emit light through current injection. Many researchers have reported various oxide semiconductor materials and structures that can achieve high-mobility TFTs [37, 151–153]. Interestingly, as we learn about the electronic nature of oxide semiconductors, we note that the mobility values are controllable in the range of 1–30 cm^2/V · s, as long as device-instability is not a concern [152, 153]. Also, some promising results have recently been demonstrated with ultra-high mobility (above 50 cm^2/V · s) in oxide-based TFTs, by adopting bilayer, active structures such as indium tin oxide (ITO)/IGZO or indium zinc oxide (IZO)/IGZO [87, 154]. Research on the selection and synthesis of tailored oxide-semiconducting layers, being proposed to obtain higher field effect mobility values, will be continued.

12 Stable and reliable oxide TFTs

The instability of oxide semiconductor-based TFTs is perhaps the most critical issue that may block the practical application of oxide TFTs for AMLCDs or AMOLED displays. Therefore, recent efforts have been focused on understanding device instability and improving long-term stability. To more systematically understand the instability phenomena of oxide TFTs, many research groups have considered four different types of practical stress conditions: negative/positive gate-bias, temperature, illumination, and environment (e.g., humidity) [155, 156]. Upon application of each stress, in general, the oxide TFT only exhibits a V_{th} shift without a significant change in mobility, as shown in Fig. 5. This may occur by either charge trapping at the channel/gate insulator interface, or by charge injection into the gate dielectric bulk. Occasionally, it has been found that the stressed devices spontaneously recover to their initial state after a relaxation period without any thermal annealing. Also, it is important to note that the V_{th} shift is significantly accelerated by applying two stress conditions simultaneously (e.g., negative gate-bias illumination stress) [157]. Although several groups have proposed a variety of possibilities such as oxygen vacancy, hole trapping, and electron injection, the origin of the related degradation mechanism is still unclear and under investigation.

In order to improve the stability of oxide TFTs, researchers have suggested various methods including optimized structures [82], suitable gate insulator materials [158], impermeable passivation layers [159], robust semiconductors [160],

Fig. 19 Schematic design strategy including various consideration factors to achieve high-mobility and high-stability oxide TFTs
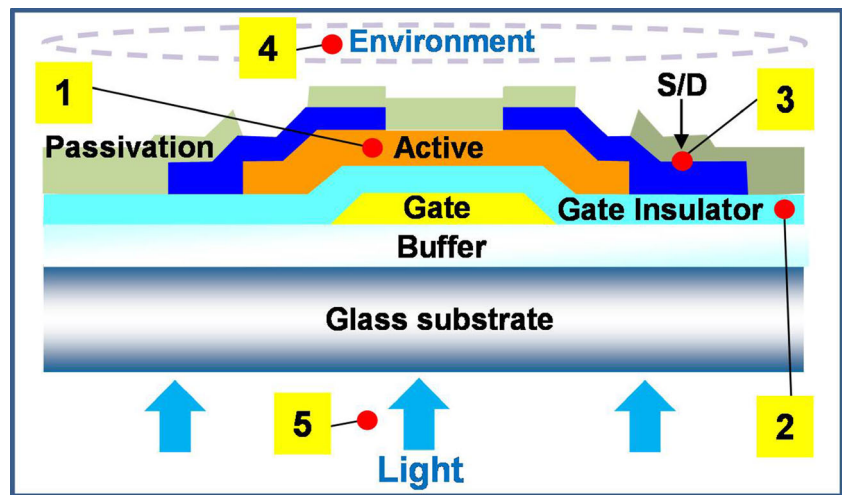
1 Active Engineering
- High mobility semiconductor (>20 cm^2/V·s)
- Low cost based semiconductor (indium or gallium free)
- Highly stable semiconductor (less oxygen defects)
- Low temperature process (flexible electronics)
- Amorphous phase (mass-production, etc)
- High Transparency (transparent electronics)
- Low cost process (atmospheric pressure process)

2 Gate Insulator Engineering
- Less hydrogen insulator
- Dense insulator
- Less defective insulator
- Low temperature process for flexible electronics

3 Improve Contact Resistance
- Low contact resistance
- Work-function alignment
- Low resistivity interconnection
- Interlayer process
- Intentional doping process

4 Water molecules/Passivations
- Less hydrogen content
- High gas diffusion barrier properties
- Less exposure to hydrogen related deposition process

5 Device Instability
- Understanding the mechanism of instability
- Analyzing the origins of defects physically/chemically
- Standard evaluation condition

and post-annealing treatments [161]. For instance, by comparing bottom-gate TFTs with a back-channel-etch (BCE) or an etch-stop (ES) structure, researchers found that the stability of an ES-type device was superior to that of a BCE type device, which may be attributable to the formation of defective interfacial layers [82]. For gate insulators, the superior stability of SiO$_2$ or Al$_2$O$_3$ gated devices can be attributed to the suppression of hole injection, or trapping in the gate

dielectric, owing to relatively large valence-band offset and lower hydrogen content [158]. In addition, low-permeable passivation layers (such as Al_2O_3 and $SiON_x$) resulted in better device stability, even under stress conditions [159]. Furthermore, it was revealed that robust oxide semiconductors normally contain higher oxygen content during the deposition process and post treatment [160, 161]. In summary, in terms of materials and structures, stable and reliable oxide TFTs have less hydrogen and higher oxygen composition to suppress V_{th} shifts when exposed to the four practical stress conditions.

Because the electronic conduction mechanisms in oxide semiconductors depend on the ability to control the types and concentration of defects such as oxygen vacancies and dissolved hydrogen, and the cation/oxygen stoichiometries, one is highly challenged to fabricate optimized and stable oxide TFTs using conventional processes, structures, and equipment. This follows from the unpredictable nature of defects that are generated or incorporated during the fabrication process. Thus the production of stable oxide TFTs that perform well in the final application remains challenging and will require very tight control of the processes, materials, and equipment as well as improvements in our ability to predict the impact of processing conditions on the defect and transport processes exhibited by the oxide semiconductor and dielectric layers.

13 Conclusion

Transistor circuits using low-temperature-processed oxide semiconductors such as ZnO and InGaZnO$_4$, have received intense attention for practical applications of high resolution AMLCD and AMOLED panels. In particular, low-voltage oxide transistors utilizing high-K dielectrics fabricated at or near room temperature have been successfully demonstrated. Room temperature processing of oxide semiconducting layers and gate insulators would render 3D integration of large stacks of active electronic device layers feasible. Low priced, flexible, oxide-TFT-based logic circuits such as inverters, ring oscillators and comparators, developed at low temperature, will serve as the key building blocks for future technology. To realize these technologies, more reproducible and robust oxide TFTs need to be developed and several key issues must be properly addressed. These issues include: (1) material tailoring of oxide semiconductors to achieve higher mobility and higher driving current, (2) interfacial control between high-k materials and oxide semiconductors, and (3) improved stability under bias, temperature, environmental and long-term use. In addition to recently commercialized IGZO-based TFTs, highly reliable and superior performance oxide TFTs would contribute to further progress in achieving products such as e-paper and e-books, and electronics integrated into textiles.

References

1. T. Kamiya, H. Hiramatsu, K. Nomura, H. Hosono, J. Electroceram. **17**, 267 (2006)
2. J.F. Wager, D.A. Keszler, R.E. Presley, *Transparent Electronics* (Springer, New York, 2008). ISBN 978-0-387-72341-9
3. J.K. Jeong, Semicond. Sci. Technol. **26**, 034008 (2011)
4. J.Y. Kwon, D.J. Lee, K.B. Kim, Electron. Mater. Lett. **7**, 1 (2011)
5. J.S. Park, W.-J. Maeng, H.-S. Kim, J.-S. Park, Thin Solid Films **520**, 1679 (2012)
6. J.-S. Park, T.-W. Kim, D. Stryakhilev, J.-S. Lee, S.-G. An, Y.-S. Pyo, D.-B. Lee, Y.G. Mo, D.-U. Jin, H.K. Chung, Appl. Phys. Lett. **95**, 013503 (2009)
7. T. Rield, P. Gorrn, W. Kowalsky, J. Disp. Technol. **5**, 501 (2009)
8. J.-S. Park, Inf. Disp. **29**, 16 (2013)
9. H.A. Klasens, H. Koelmans, Solid State Electron. **7**, 701 (1964)
10. G.F. Boesen, J.E. Jacobs, Proc. IEEE **56**, 2094 (1968)
11. K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, Nature **432**, 488 (2004)
12. T. Kamiya, K. Nomura, H. Hosono, Sci. Technol. Adv. Mater. **11**, 044305 (2010)
13. T. Minami, Semicond. Sci. Technol. **20**, S35 (2005)
14. R.B.H. Tahar, T. Ban, Y. Ohya, T. Takahashi, J. Appl. Phys. **83**, 2631 (1998)
15. K. Ellmer, J. Phys. D. Appl. Phys. **34**, 3097 (2001)
16. C.G. Van de Walle, Phys. Rev. Lett. **85**, 1012 (2000)
17. S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata, T. Kawai, J. Appl. Phys. **93**, 1624 (2003)
18. R.L. Hoffman, B.J. Norris, J.F. Wager, Appl. Phys. Lett. **82**, 733 (2003)
19. P.F. Carcia, R.S. McLean, M.H. Reilly, G. Nunes, Appl. Phys. Lett. **82**, 1117 (2003)
20. E.M.C. Fortunato, P.M.C. Barquinha, A.C.M.B.G. Pimentel, A.M.F. Gonçalves, A.J.S. Marques, L.M.N. Pereira, R.F.P. Martins, Adv. Mater. **17**, 590 (2005)
21. S.-H.K. Park, C.-S. Hwang, M. Ryu, S. Yang, C. Byun, J. Shin, J.-I. Lee, K. Lee, M.S. Oh, S. Im, Adv. Mater. **21**, 678 (2009)
22. D.H. Levy, D. Freeman, S.F. Nelson, P.J. Cowdery-Corvan, L.M. Irving, Appl. Phys. Lett. **92**, 192101 (2008)
23. E.M.C. Fortunato, P.M.C. Barquinha, A.C.M.B.G. Pimentel, A.M.F. Gonçalves, A.J.S. Marques, R.F.P. Martins, L.M.N. Pereira, Appl. Phys. Lett. **85**, 2541 (2004)

24. R.E. Presley, C.L. Munsee, C.-H. Park, D. Hong, J.F. Wager, D.A. Keszler, J. Phys. D. Appl. Phys. **37**, 2810 (2004)
25. G. Lavareda, C.N. de Carvalho, E. Fortunato, A.R. Ramos, E. Alves, O. Conde, A. Amaral, J. Non-Cryst. Solids **352**, 2311 (2006)
26. Y. Vygranenko, K. Wang, A. Nathan, Appl. Phys. Lett. **91**, 263508 (2007)
27. S.-S. Dhanajay, C.-Y. Cheng, C.-W. Yang, Y.-C. Ou, M.C. Chuang, C.-W. Wu, J. Chu, Phys. D. Appl. Phys. **41**, 092006 (2008)
28. M. Katayama, S. Ikesaka, J. Kuwano, Y. Yamamoto, H. Koinuma, Y. Matsumoto, Appl. Phys. Lett. **89**, 242103 (2006)
29. J.-W. Park, D. Lee, H. Kwon, S. Yoo, J. Huh, IEEE Electron. Devices Lett. **30**, 739 (2009)
30. K.-H. Choi, H.-K. Kim, Electrochem. Solid State Lett. **14**, H314 (2011)
31. J. Park, K.-C. Ok, B.D. Ahn, J.H. Lee, J.-W. Park, K.-B. Chung, J.-S. Park, Appl. Phys. Lett. **99**, 142104 (2011)
32. Y. Ye, R. Lim, J.M. Whiter, J. Appl. Phys. **106**, 074512 (2009)
33. S.J. Lim, S.-J. Kwon, H. Kim, J.-S. Park, Appl. Phys. Lett. **91**, 183517 (2007)
34. B. Yaglioglu, H.Y. Yeom, R. Beresford, D.C. Paine, Appl. Phys. Lett. **89**, 062103 (2006)
35. Y.-L. Wang, F. Ren, W. Lim, D.P. Norton, S.J. Pearton, I.I. Kravchenko, J.M. Zavada, Appl. Phys. Lett. **90**, 232103 (2007)
36. C.-J. Ku, Z. Duan, P.I. Reyes, Y. Lu, Y. Xu, C.-L. Hsueh, E. Garfunkel, Appl. Phys. Lett. **98**, 123511 (2011)
37. H.-S. Kim, S.H. Jeon, J.S. Park, T.S. Kim, K.S. Son, J.-B. Seon, S.-J. Seo, S.-J. Kim, E. Lee, J.G. Chung, H. Lee, S. Han, M. Ryu, S.Y. Lee, K. Kim, Sci. Rep. **3**, 1459 (2013)
38. M. Kim, J.H. Jeong, H.J. Lee, T.K. Ahn, H.S. Shin, J.-S. Park, J.K. Jeong, Y.-G. Mo, H.D. Kim, Appl. Phys. Lett. **90**, 212114 (2007)
39. H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, Appl. Phys. Lett. **89**, 112123 (2006)
40. J.-S. Park, K.-S. Kim, Y.-G. Park, Y.-G. Mo, H.D. Kim, J.K. Jeong, Adv. Mater. **21**, 329 (2009)
41. C.-J. Kim, S. Kim, J.-H. Lee, J.-S. Park, S. Kim, J. Park, E. Lee, J. Lee, Y. Park, J.H. Kim, S.T. Shin, U.-I. Chung, Appl. Phys. Lett. **95**, 252103 (2009)
42. M.K. Ryu, S. Yang, S.-H.K. Park, C.-S. Hwang, J.K. Jeong, Appl. Phys. Lett. **95**, 072104 (2009)
43. S. Yang, D.-H. Lee, M.K. Ryu, S.-H.K. Park, C.-S. Hwang, J. Jang, J.K. Jeong, Appl. Phys. Lett. **96**, 213511 (2010)
44. E. Chong, Y.S. Chun, S.Y. Lee, Appl. Phys. Lett. **97**, 102102 (2010)
45. H.Q. Chiang, J.F. Wager, R.L. Hoffman, J. Jeong, D.A. Keszler, Appl. Phys. Lett. **86**, 013503 (2005)
46. W.B. Jackson, R.L. Hoffman, G.S. Herman, Appl. Phys. Lett. **87**, 193503 (2005)
47. P. Görn, P. Hölzer, T. Riedl, W. Kowalsky, J. Wang, T. Weimann, P. Hinze, S. Kipp, Appl. Phys. Lett. **90**, 063502 (2007)
48. B.S. Yang, M.S. Huh, S. Oh, U.S. Lee, Y.J. Kim, M.S. Oh, J.K. Jeong, C.S. Hwang, H.J. Kim, Appl. Phys. Lett. **98**, 122110 (2011)
49. D.N. Kim, D.L. Kim, G.H. Kim, S.J. Kim, Y.S. Rim, W.H. Jeong, H.J. Kim, Appl. Phys. Lett. **97**, 192105 (2010)
50. G.H. Kim, W.H. Jeong, B.D. Ahn, H.S. Shin, H.J. Kim, H.J. Kim, M.K. Ryu, K.B. Park, J.B. Seon, S.Y. Lee, Appl. Phys. Lett. **96**, 163506 (2010)
51. D.-H. Cho, S. Yang, C. Byun, J. Shin, M.K. Ryu, S.-H.K. Park, C.-S. Hwang, S.M. Chung, W.-S. Cheong, S.M. Yoon, H.-Y. Chu, Appl. Phys. Lett. **93**, 142111 (2008)
52. E.M.C. Fortunato, L.M.N. Pereira, P.M.C. Barquinha, A.M.B. do Rego, G. Gonçalves, A. Vilà, J.R. Morante, R.F.P. Martins, Appl. Phys. Lett. **92**, 222103 (2008)
53. S.-Y. Han, D.-H. Lee, G.S. Herman, C.-H. Chang, J. Disp. Technol. **5**, 520 (2009)
54. B.J. Norris, J. Anderson, J.F. Wager, D.A. Keszler, J. Phys. D. Appl. Phys. **36**, L105 (2003)
55. B.S. Ong, C. Li, Y. Li, Y. Wu, R. Loutfy, J. Am. Chem. Soc. **129**, 2750 (2007)
56. Y.-J. Chang, D.-H. Lee, G.S. Herman, C.-H. Chang, Electrochem. Solid State Lett. **10**, H135 (2007)
57. D.-H. Lee, Y.-J. Chang, G.S. Herman, C.H. Chang, Adv. Mater. **19**, 843 (2007)
58. K.K. Banger, Y. Yamashita, K. Mori, R.L. Peterson, T. Leedham, J. Rickard, H. Sirringhaus, Nat. Mater. **10**, 45 (2011)
59. M.-G. Kim, M.G. Kanatzidis, A. Facchetti, T.J. Marks, Nat. Mater. **10**, 382 (2011)
60. Y.H. Hwang, J.-S. Seo, J.M. Yun, H. Park, S. Yang, S.-H.K. Park, B.-S. Bae, NPG Asia Mater. **5**, e45 (2013)
61. T. Jun, K. Song, Y. Jeong, K. Woo, D. Kim, C. Bae, J. Moon, J. Mater. Chem. **21**, 1102 (2011)
62. S.Y. Park, B.J. Kim, K. Kim, M.S. Kang, K.-H. Lim, T.I. Lee, J.M. Myoung, H.K. Baek, J.H. Cho, Y.S. Kim, Adv. Mater. **24**, 834 (2012)
63. Y.-H. Kim, J.-S. Heo, T.-H. Kim, S. Park, M.-H. Yoon, J. Kim, M.S. Oh, G.-R. Yi, Y.-Y. Noh, S.K. Park, Nature **489**, 128 (2012)
64. S.T. Meyers, J.T. Anderson, C.M. Hung, J. Thompson, J.F. Wager, D.A. Keszler, J. Am. Chem. Soc. **130**, 17603 (2008)
65. S.-C. Chang, C.-C. Yu, F.-W. Chang, S.-W. Liang, C.-H. Tsai, B.-C. Chuang, C.-Y. Tsay, SID Int. Symp. Dig. Tech. **39**, 1188 (2008)
66. C.G. Choi, S.-J. Seo, B.-S. Bae, Electrochem. Soild State Lett. **11**, H7 (2008)
67. G.H. Kim, B.D. Ahn, H.S. Shin, W.H. Jeong, H.J. Kim, H.J. Kim, Appl. Phys. Lett. **94**, 233501 (2009)
68. D.H. Lee, S.-Y. Han, G.S. Herman, C.-H. Chang, J. Mater. Chem. **19**, 3135 (2009)
69. Y.H. Hwang, J.H. Jeon, S.-J. Seo, B.-S. Bae, Electrochem. Soild State Lett. **12**(H336) (2009)
70. S.K. Park, Y.-H. Kim, H.-S. Kim, J.-I. Han, Electrochem. Solid State Lett. **12**, H256 (2009)
71. M.-K. Ryu, K.-B. Park, J.-B. Seon, S.Y. Lee, J. Soc. Inf. Display **18**, 734 (2010)
72. M.-G. Kim, H.S. Kim, Y.-G. Ha, J. He, M.G. Kanatzidis, A. Facchetti, T.J. Marks, J. Am. Chem. Soc. **132**, 10352 (2010)
73. Y.-H. Yang, S.S. Yang, C.-Y. Kao, K.-S. Chou, IEEE Electron. Device Lett. **31**, 329 (2010)
74. C.D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, J.M. Shaw, Science **283**, 822 (1999)
75. L.A. Majewski, R. Shreoder, M. Grell, Adv. Mater. **17**, 192 (2005)
76. M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schutz, S. Maisch, F. Effemberger, M. Brunnbauer, F. Stellacci, Nature **431**, 963 (2004)
77. S.M. Sze, K.K. Ng, *Physics of Semiconductor Devices* (John Wiley and Sons, New York, 2007), ISBN 9780–471143239
78. F. Fleischhaker, V. Wloka, I. Hennig, J. Mater. Chem. **20**, 6622 (2010)
79. D.H. Kim, S.-H. Choi, N.G. Cho, Y. Chang, H.-G. Kim, J.-M. Hong, I.-D. Kim, Electrochem. Solid State Lett. **12**, H296 (2009)
80. K. Kang, M.-H. Lim, H.-G. Kim, Y. Choi, H.L. Tuller, I.-D. Kim, J.-M. Hong, Appl. Phys. Lett. **87**, 242908 (2005)
81. I.-D. Kim, M.-H. Lim, K. Kang, H.-G. Kim, S.-Y. Choi, Appl. Phys. Lett. **89**, 022905 (2006)
82. J.-Y. Kwon, K.S. Son, J.S. Jung, K.-H. Lee, J.S. Park, T.S. Kim, K.H. Ji, R. Choi, J.K. Jeong, B. Koo, S. Lee, Electrochem. Solid State Lett. **13**, H213 (2010)
83. J.-S. Park, J. Electroceram. **25**, 145 (2010)
84. J.-S. Park, C.W. Lee, J.J. Yoon, K.-B. Chung, J. Electroceram. **26**, 63 (2011)
85. J.-S. Park, J. Electroceram. **28**, 74 (2012)
86. M.-H. Lim, K. Kang, H.-G. Kim, I.-D. Kim, Y. Choi, H.L. Tuller, Appl. Phys. Lett. **89**, 202908 (2006)
87. H.-S. Kim, J.S. Park, H.-K. Jeong, K.S. Son, T.S. Kim, J.-B. Seon, E. Lee, J.G. Chung, D.H. Kim, M. Ryu, S.Y. Lee, ACS Appl. Mater. Interfaces **4**, 5416 (2012)

88. Y.W. Choi, I.D. Kim, H.L. Tuller, A.I. Akinwande, IEEE Trans. Electron. Dev. **52**, 2819 (2005)

89. H. Kauk, H. Halik, F. Eder, G. Schmid, C. Dehm, U. Zschieschang, D. Rohde, R. Brederlow, S. Briole, S. Maisch, F. Effenberger, Tech. Digit. Int. Electron. Devices Meet. **2004**, 369 (2004)

90. S.A. DiBenedetto, A. Facchetti, M.A. Ratner, T.J. Marks, Adv. Mater. **21**, 1407 (2009)

91. T. Miyadera, T. Minari, S.D. Wang, K. Tsukagoshi, Appl. Phys. Lett. **93**, 213302 (2008)

92. L. Wang, M.-H. Yoon, G. Lu, Y. Yang, A. Facchetti, T.J. Marks, Nat. Mater. **5**, 893 (2006)

93. M.H. Yoon, H. Yan, A. Facchetti, T.J. Marks, J. Am. Chem. Soc. **127**, 10388 (2005)

94. G.W. Hyung, J. Park, J.R. Koo, K.M. Choi, S.J. Kwon, E.S. Cho, Y.S. Kim, Y.K. Kim, Solid State Electron. **69**, 27 (2012)

95. K. Lee, G. Ko, G.H. Lee, G. Han, M.M. Sung, T.W. Ha, J.H. Kim, S. Im, Appl. Phys. Lett. **97**, 082110 (2010)

96. P.K. Nayak, J. Kim, C. Lee, Y. Hong, Phys. Status Solidi A **207**, 1664 (2010)

97. J. Robertson, J. Vac. Sci. Technol. B. **18**, 1785 (2000)

98. R.K. Nahar, V. Singh, A. Sharma, J. Mater. Sci. Mater. Electron. **18**, 615 (2007)

99. G.D. Wilk, R.M. Wallace, J.M. Anthony, J. Appl. Phys. **87**, 484 (2000)

100. H. Takahashi, S. Toyoda, J. Okabayashi, H. Kumigashira, M. Oshima, Y. Sugita, G.L. Liu, Z. Liu, K. Usuda, Appl. Phys. Lett. **87**, 012903 (2005)

101. S.A. Campbell, D.C. Gilmer, X.C. Wang, M.T. Hsieh, H.S. Kim, W.L. Gladfelter, J.H. Yan, IEEE Trans. Electron. Devices **44**, 104 (1997)

102. J.P. Chang, Y.-S. Lin, K. Chu, J. Vac. Sci. Technol. B **19**, 1782 (2001)

103. A. Bahari, A. Anasari, Z. Rahmani, J. Eng. Technol. Res. **3**, 203 (2001)

104. I. Levin, D. Brandon, J. Am. Ceram. Soc. **81**, 1995 (1998)

105. J.H. Choi, Y. Mao, J.P. Chang, Mater. Sci. Eng. R **72**, 97 (2011)

106. M. Kadoshima, M. Hiratani, Y. Shimamoto, K. Torii, H. Miki, S. Kimura, T. Nabatame, Thin Solid Films **424**, 224 (2003)

107. D.K. Smith, C.F. Cline, J. Am. Ceram. Soc. **45**, 249 (1962)

108. C.T. Lynch, F.W. Vahldiek, L.B. Robinson, J. Am. Ceram. Soc. **44**, 147 (1961)

109. M.-H. Cho, D.-H. Ko, K. Jeong, S.W. Whangbo, C.N. Whang, S.C. Choi, S.J. Cho, Thin Solid Films **349**, 266 (1999)

110. J. Zabicky, *The Chemistry of Metal Enolates Part 1*, (John Wiley and Sons, New York 2009), ISBN 9780–470061688

111. Bansal, Narottam P., *Low Temperature Synthesis of Monolithic Transparent Ta₂O₅ Gels from Hydrolysis of Metal Alkoxide*, (National Aeronautics and Space Administration (NASA), Washington, DC, 1993), ISBN 9781234352011

112. A.P. Huang, Z.C. Yang, Paul K. Chu, in *Hafnium-based High-k Gate Dielectrics, Advances in Solid State Circuit Technologies*, ed. Paul K. Chu, (InTech, Shanghai, China, 2010) ISBN: 978-953-307-086-5, Available from: http://www.intechopen.com/books/advances-in-solid-state-circuit-technologies/hafnium-based-high-k-gatedielectrics

113. U. Diebold, Surf. Sci. Rep. **48**, 53 (2003)

114. M.-H. Cho, D.-H. Ko, Y.G. Choi, K. Jeong, I.W. Lyo, D.Y. Noh, H.J. Kim, C.N. Whang, J. Vac. Sci. Technol. A **19**, 192 (2001)

115. J. McPherson, J.Y. Kim, A. Shanware, H. Mogul, Appl. Phys. Lett. **82**, 2121 (2003)

116. S.C. Choi, M.H. Cho, S.W. Whangbo, C.N. Whang, J. Korean Phys. Soc. **31**, 144 (1997)

117. M. Gurvitch, L. Manchanda, J.M. Gibson, Appl. Phys. Lett. **51**, 919 (1987)

118. D.-H. Son, D.-H. Kim, J.H. Kim, S.-J. Sung, E.A. Jung, J.-K. Kang, Electrochem. Solid State Lett. **13**, H274 (2010)

119. J.-S. Park, J.K. Jeong, Y.-G. Mo, S. Kim, Appl. Phys. Lett. **94**, 042105 (2009)

120. J.S. Lee, S. Chang, S.-M. Koo, S.Y. Lee, IEEE Electron. Device Lett. **31**, 225 (2010)

121. Y.K. Moon, S. Lee, J.-W. Park, J. Korean Phys. Soc. **55**, 1906 (2009)

122. L. Zhang, J. Li, X.W. Zhang, X.Y. Jiang, Z.L. Zhang, Appl. Phys. Lett. **95**, 072112 (2009)

123. Z.L. Pei, L. Pereira, G. Gonçalves, P. Barquinha, N. Franco, E. Alves, A.M.B. Reqo, R. Martins, E. Fortunato, Electrochem. Solid State Lett. **12**, G65 (2009)

124. D.H. Kim, H. Seo, K.-B. Chung, N.G. Cho, H.-G. Kim, I.-D. Kim, J. Electrochem. Soc. **157**, H964 (2010)

125. J.-Y. Kwon, J.S. Jung, K.S. Son, K.-H. Lee, J.S. Park, T.S. Kim, J.-S. Park, R. Choi, J.K. Jeong, B. Koo, S.Y. Lee, Appl. Phys. Lett. **97**, 183503 (2010)

126. X. Zou, G. Fang, L. Yuan, X. Tong, X. Zhao, Semicond. Sci. Technol. **25**, 055006 (2010)

127. D. Yi, J. Yuan, H. Liu, Y. Shen, Y.-H. Lin, C.-W. Nan, X. Xi, J. He, J. Electroceram. **29**, 95 (2012)

128. M. Zhang, H. Wang, H. Yang, W. Liu, H. Zhou, X. Yao, J. Electroceram. **26**, 99 (2011)

129. X. Chou, J. Wang, Z. Zhao, W. Geng, W. Zhang, J. Zhai, J. Electroceram. **26**, 185 (2011)

130. H.-S. Kim, H.-G. Kim, I.-D. Kim, K.-B. Kim, J.-C. Lee, Appl. Phys. Lett. **87**, 212903 (2005)

131. H.-S. Kim, T.-S. Hyun, H.-G. Kim, I.-D. Kim, T.-S. Yun, J.-C. Lee, Appl. Phys. Lett. **89**, 052902 (2006)

132. Y.-S. Ham, S.W. Yun, J.-H. Koh, J. Electroceram. **26**, 32 (2011)

133. J.B. Kim, C. Fuentes-Hernandez, B. Kippelen, Appl. Phys. Lett. **93**, 242111 (2008)

134. K. Kang, M.-H. Lim, H.-G. Kim, I.-D. Kim, J.-M. Hong, Appl. Phys. Lett. **90**, 043502 (2007)

135. K. Kang, I.-D. Kim, M.-H. Lim, H.-G. Kim, J.-M. Hong, Thin Solid Films **516**, 1218 (2008)

136. Y.-B. Kim, J.-U. Kim, D.-K. Choi, J.-M. Hong, I.-D. Kim, J. Electroceram. **23**, 76 (2009)

137. D.-H. Kim, N.G. Cho, H.-G. Kim, H.-S. Kim, J.-M. Hong, I.-D. Kim, Appl. Phys. Lett. **93**, 032901 (2008)

138. D.-H. Kim, N.G. Cho, H.-G. Kim, I.-D. Kim, Electrochem. Solid State Lett. **13**, H370 (2010)

139. W. Li-Ping, L. Ai-Xia, D. Wei, W. Qing, Chin. Phys. Lett. **27**, 078502 (2010)

140. W. Fu, Z. Xu, K. Liu, W. Wang, X. Bai, E. Wang, Appl. Phys. Lett. **93**, 213107 (2008)

141. W. Liu, H. Wang, J. Electroceram. **27**, 209 (2011)

142. A.F. Qasrawi, B.H. Kmail, E.M. Nazzal, A. Mergen, J. Electroceram. (2013). doi:10.1007/s10832-013-9809-9

143. W. Liu, H. Wang, J. Electroceram. **29**, 183 (2012)

144. J. Lu, S. Stemmer, Appl. Phys. Lett. **83**, 2411 (2003)

145. I.-D. Kim, Y.W. Choi, H.L. Tuller, Appl. Phys. Lett. **87**, 043509 (2005)

146. N.G. Cho, D.H. Kim, H.-G. Kim, J.-M. Hong, I.-D. Kim, Thin Solid Films **518**, 2843 (2010)

147. G. Vasta, T.J. Jackson, A. Fronmmhold, J. Bowen, E.J. Tarte, J. Electroceram. **27**, 176 (2011)

148. M. Søgaard, A. Bieberle-Hütter, P.V. Hendriksen, M. Mogensen, H.L. Tuller, J. Electroceram. **27**, 134 (2011)

149. A.A. Al-Ghamdi, F. Al-Hazmi, F. Alnowaiser, R.M. Al-Tuwirqi, A.A. Al-Ghamdi, O.A. Alhartomy, F. El-Tantawy, F. Yakuphanoglu, J. Electroceram. **29**, 198 (2012)

150. T. Arai, T. Sasaoka, SID Symp. Dig. Tech. Pap. **42**, 710 (2011)

151. K. Ebata, S. Tomai, Y. Tsuruma, T. Litsuka, S. Matsuzaki, K. Yano, Appl. Phys. Express **5**, 011102 (2012)

152. S. Oh, B.S. Yang, Y.J. Kim, M.S. Oh, M. Jang, H. Yang, J.K. Jeong, C.S. Hwang, H.J. Kim, Appl. Phys. Lett. **101**, 092107 (2012)

153. S.Y. Park, K.H. Ji, H.Y. Jung, J.-I. Kim, R. Choi, K.S. Son, M.K. Ryu, S. Lee, J.K. Jeong, Appl. Phys. Lett. **100**, 162108 (2012)

154. S.-I. Kim, C.J. Kim, J.C. Park, I. Song, S.W. Kim, H. Yin, E. Lee, J.C. Lee, Y. Park, IEDM Tech. Dig. **73** (2008)

155. J.K. Jeong, H.W. Yang, J.H. Jeong, Y.G. Mo, H.D. Kim, Appl. Phys. Lett. **93**, 123508 (2008)

156. J.H. Shin, J.S. Lee, C.S. Hwang, S.H.K. Park, W.S. Cheong, C.W. Byun, J.I. Lee, H.Y. Chu, J. ETRI **31**, 62 (2009)

157. K.-H. Lee, J.S. Jung, K.S. Son, J.S. Park, T.S. Kim, R. Choi, J.K. Jeong, J.-Y. Kwon, B. Koo, S. Lee, Appl. Phys. Lett. **95**, 232106 (2009)

158. J.S. Jung, K.S. Son, K.-H. Lee, J.S. Park, T.S. Kim, J.-Y. Kwon, K.-B. Chung, J.-S. Park, B. Koo, S. Lee, Appl. Phys. Lett. **96**, 193506 (2010)

159. S.-I. Kim, S.W. Kim, C.J. Kim, J.-S. Park, J. Electrochem. Soc. **158**, H115 (2011)

160. H.-S. Kim, K.-B. Park, K.S. Son, J.S. Park, W.-J. Maeng, T.S. Kim, K.-H. Lee, E.S. Kim, J. Lee, J. Suh, J.-B. Seon, M.K. Ryu, S.Y. Lee, K. Lee, S. Im, Appl. Phys. Lett. **97**, 102103 (2010)

161. K.H. Ji, J.-I. Kim, H.Y. Jung, S.Y. Park, R. Choi, U.K. Kim, C.S. Hwang, D. Lee, H. Hwang, J.K. Jeong, Appl. Phys. Lett. **98**, 103509 (2011)