Optimized Cu-Sn Wafer-Level Bonding Using Intermetallic Phase Characterization

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The objective of this study is to optimize the Cu/Sn solid–liquid interdiffusion process for wafer-level bonding applications. To optimize the temperature profile of the bonding process, the formation of intermetallic compounds (IMCs) which takes place during the bonding process needs to be well understood and characterized. In this study, a simulation model for the development of IMCs and the unreacted remaining Sn thickness as a function of the bonding temperature profile was developed. With this accurate simulation model, we are able to predict the parameters which are critical for bonding process optimization. The initial characterization focuses on a kinetics model of the Cu₃Sn thickness growth and the amount of Sn thickness that reacts with Cu to form IMCs. As-plated Cu/Sn samples were annealed using different temperatures (150°C to 300°C) and durations (0 min to 320 min). The kinetics model is then extracted from the measured thickness of IMCs of the annealed samples.

Key words: Intermetallic formation, SLID bonding, Cu/Sn bonding, Pb-free solder

INTRODUCTION

Cu/Sn solid–liquid interdiffusion (SLID) waferlevel bonding is an attractive assembly technique for microelectromechanical systems (MEMS) encapsulation and interconnection due to its low cost, high temperature stability, high bond strength, and hermeticity.^{1,2} This bonding technique has been demonstrated for MEMS encapsulation, high-density interconnection, and simultaneous MEMS encapsulation and interconnection,^{3–5} but an optimized bonding process taking into account the aspects of wafer-level bonding has not yet been established. A typical bonding temperature profile and development of intermetallic compounds (IMCs) during the bonding process are described in Fig. 1.

As any SLID bonding technique, Cu/Sn SLID bonding is based on rapid formation of IMCs between two metal components: one low-melting component (Sn) and one high-melting component

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(Cu). The bonding is typically carried out at moderate temperatures between 250°C and 300°C,^{3,6} which is above the melting point of Sn. When the Sn melts, the IMCs solidify isothermally. For correctly designed layer thicknesses, the resulting bond-line will only consist of Cu and the intermetallic phases (Cu₆Sn₅ and Cu₃Sn), with melting temperatures of 415°C and 676°C, respectively. The overall goal of the wafer-level bonding process is to achieve a Cu/Cu₃Sn/Cu final bond-line, which is thermodynamically stable.

An important aspect of Cu/Sn SLID wafer-level bonding is the formation of Cu_6Sn_5 , the geometry of which has been shown to influence void formation in the bond-line. Voids would impact the bond strength and subsequently the hermeticity and overall reliability. The formation of Cu_6Sn_5 has been observed at room temperature.^{7,8} During a wafer-level bonding process where the temperature is increased following a defined profile, the Cu_6Sn_5 grains will grow. If Cu_6Sn_5 reaches the Sn surface while the temperature is still below the melting point of Sn, the Cu_6Sn_5 grains will act as spacers, and voids will later form.^{7,9}



Fig. 1. Typical Cu/Sn SLID wafer-level bonding temperature profile and formation of IMCs during the bonding process. Wafers are brought into contact at T_c , which is below the melting point of Sn, T_m . The temperature is kept at T_m for several minutes, then ramped to the bonding temperature, T_b . The IMCs formed during the bonding process are Cu₃Sn and Cu₆Sn₅.

For a Cu/Sn wafer-level bonding process with high yield, it is important to ensure that there remains unreacted Sn at the bond interface when the temperature of the wafer stack reaches the melting point of Sn (T_m) . The amount of Sn which remains at T_m depends on the initial Sn thickness and the amount of Sn that has reacted with Cu to form IMCs, which depends on the temperature profile. For an optimal bonding temperature profile and Cu/Sn layer thickness design, deeper understanding as well as a simulation model that can predict the IMC development during the bonding process are needed.

In this study, the intermetallic formation of electroplated Cu/Sn thin films is studied. Cu/Sn samples are annealed at different temperatures (150°C to 300°C), and then the IMCs are characterized by optical microscopy, scanning electron microscopy (SEM), and energy-dispersive x-ray spectroscopy (EDS). By measuring the growth rate of IMCs, thermal kinetics models for Cu₃Sn and the amount of Sn that is converted into IMCs are estimated. Based upon the characterization results, a simulation model which is suitable for understanding and predicting the IMC development during Cu/Sn wafer-level bonding is developed. The following parameters that are critical to bonding process optimization can thus be predicted:

• The unreacted remaining Sn thickness on each wafer at the contact temperature (T_c) when two wafers are brought into contact



Fig. 2. Schematic illustration of IMC formation during the Cu/Sn interdiffusion process. Cu_6Sn_5 is formed at the Cu_6Sn_5/Sn and Cu_6Sn_5/Cu_3Sn interface, while the Cu_3Sn phase is formed at the Cu/Cu_3Sn and Cu_6Sn_5/Cu_3Sn interface. The chemical reactions for Cu, Sn, and corresponding IMCs are listed in Table I.

- The unreacted remaining Sn thickness on each wafer when the melting point of Sn $(T_{\rm m})$ is reached
- The time required to convert all Sn into IMCs
- The time required to achieve the final Cu/Cu₃Sn/ Cu bond-line

EXPERIMENTAL PROCEDURES

IMC Characterization

Background

The general mechanism of IMC formation during a Cu/Sn interdiffusion process is in itself understood. The formation rate of IMCs depends on both the diffusion rate of the species and the actual chemical reaction kinetics. An illustration of the IMC formation process is shown in Fig. 2, with the chemical reactions given in Table I.

The kinetics model for the IMC thickness growth, or alternatively the thickness of Sn that reacts with Cu to form IMCs, can be expressed (assuming simplification to a one-dimensional diffusion problem) as^{10,11}

$$y_t^2 - y_0^2 = k_0 \exp\left(\frac{-Q}{RT}\right) t^{2n},\tag{1}$$

where y_t is the IMC thickness or the Sn thickness that has reacted with Cu to form IMCs after the annealing duration t, T is the temperature, Q is the activation energy, k_0 is the diffusion coefficient, y_0 is the initial IMC thickness or initial Sn thickness that has reacted with Cu to form IMCs, and n is an empirical exponent.

n = 1/2 corresponds to the analytical solution of the [one dimension (1D)] diffusion equation, implying that the diffusion rate dictates the IMC formation rate. For $n \neq 1/2$, other kinetics must also be considered. In particular, n < 1/2 can be interpreted as a situation where the reaction rate is limited,

Material Preparation

vel bonding process.

For full conversion to a $Cu/Cu_3Sn/Cu$ bond interface, the required minimum thickness ratio of Cu to Sn is

$$\frac{y_{\rm Cu}}{y_{\rm Sn}} = \frac{M_{\rm Cu}/\rho_{\rm Cu}}{M_{\rm Sn}/\rho_{\rm Sn}} = \frac{M_{\rm Cu}}{M_{\rm Sn}} \times \frac{\rho_{\rm Sn}}{\rho_{\rm Cu}} = \frac{61.63}{38.37} \times \frac{7.3}{8.9} = 1.32,$$
(2)

where $M_{\rm Cu}$ and $M_{\rm Sn}$ are the weight ratios of Cu and Sn in Cu₃Sn, and $y_{\rm Cu}$ and $y_{\rm Sn}$ are the thicknesses of Cu and Sn that are converted into Cu₃Sn. In this study, layer thicknesses of 5 μ m of Cu and 1.5 μ m of Sn were selected for characterization. Furthermore, a Cu/Sn thickness ratio greater than 1.32 was selected to ensure that there was an excess Cu layer in the final bond-line to isolate the IMC from the adhesion layer.

All the Cu/Sn films were deposited by electroplating on metallized Si wafers using Cu sulfateand Sn sulfate-based electrolytes. The wafers were thermally oxidized and sputter-coated with TiW (adhesion and barrier layer) and Au (seed layer). Photoresist was used as a mask for all electroplating. Before electroplating, the wafer was activated by Ar + O₂ plasma to ensure an organic-free surface of the Au seed layer. The electroplating procedure used a standard pulse plating process with current density of 10 mA/cm². A cross-section of an as-plated sample is shown in Fig. 3.

It is important to point out that, in our experiments, we observed an initial Cu_6Sn_5 layer of around 0.5 μ m thickness, as shown in Fig. 4. This

Table I. Chemical reactions during the Cu/Sn interdiffusion process

Layer	Interface	Chemical Reaction
Cu_3Sn	Cu/Cu ₃ Sn	$Sn_{diff} + 3Cu = Cu_3Sn_3$
CueSn5	Cu ₃ Sn-Cu ₆ Sn ₅ Cu ₂ Sn/Cu ₆ Sn ₅	$9Cu_{diff} + Cu_6Sn_5 = 5Cu_3Sn_3Sn_{diff} + 2Cu_2Sn = Cu_6Sn_5$
0 460115	Cu_6Sn_5 -Sn	$6Cu_{diff} + 5Sn = Cu_6Sn_5$



Fig. 3. As-plated Cu/Sn sample.

phase forms during and immediately after the plating process of Sn on Cu is completed, possibly induced by the electric fields in the electroplating process.

Annealing

Based on earlier experiments^{3,4,12} with Cu/Sn SLID bonding, a contact temperature (Fig. 1) of 150° C to 200° C and a bonding temperature of 250° C to 300° C result in high bond strength and high yield. Annealing temperatures from 150° C to 300° C and durations of 0 min to 320 min were selected (Table II). To minimize the thickness of IMC formed before the annealing temperature was reached, a high temperature ramping rate of 50° C/min was selected.

Characterization

The annealed samples were cross-sectioned by molding individual dies in epoxy, grinding with SiC paper, and polishing with diamond powder (Ø3 μ m and Ø1 μ m). Scanning electron microscopy (SEM) and energy-dispersive x-ray spectroscopy (EDS) were used to identify the IMC phases in the bondline. IMC thickness was measured by optical microscopy, as the phases were clearly distinguishable by color appearance in optical microscopy, as verified by EDS. Magnification of 1000× was used for optical microscopy. Since the cross-sectioned samples were flat-polished, the optical depth of focus did not affect the image quality, and high measurement accuracy could be obtained.

To determine the amount of Sn that had reacted with Cu to form IMCs, any unreacted remaining Sn on the annealed samples was removed by wet etching using 30% HCl solution. Since this etch is selective for pure Sn, the cross-sections of the etched samples only consist of Cu and IMCs (Cu₃Sn and Cu₆Sn₅). The amount of Sn that had reacted with Cu to form IMCs was calculated as



Fig. 4. As-plated Cu/Sn sample after Sn etching. The cross-section shows an initial Cu₆Sn₅ layer of 0.5 μm which forms immediately after plating.

Table	II.	Annealing	parameters	for	IMC	charac-
terizat	tion	(temperatu	are ramping	rate	50°C /	'min)

(°C) Annealing Time (min)
0, 10, 20, 40, 80
0, 10, 20, 40, 80, 160, 320
0, 10, 20, 40
0, 5, 10, 20

$$\begin{split} y_{\rm Sn} &= y_{\rm Sn}({\rm Cu}_3{\rm Sn}) + y_{\rm Sn}({\rm Cu}_6{\rm Sn}_5) \\ &= \frac{M_{\rm Sn}({\rm Cu}_3{\rm Sn})}{\rho_{({\rm Cu}_3{\rm Sn})}/\rho_{\rm Sn}} \times y_{{\rm Cu}_3{\rm Sn}} + \frac{M_{\rm Sn}({\rm Cu}_6{\rm Sn}_5)}{\rho_{({\rm Cu}_6{\rm Sn}_5)}/\rho_{\rm Sn}} \times y_{{\rm Cu}_6{\rm Sn}_5} \\ &= \frac{y_{\rm Cu}_3{\rm Sn}}{2.1} + \frac{y_{\rm Cu}_6{\rm Sn}_5}{1.4} \end{split}$$

$$(3)$$

where y_{Cu3Sn} and y_{Cu3Sn5} are the measured IMC thicknesses, $M_{\text{Sn}}(\text{Cu}_3\text{Sn})$ and $M_{\text{Sn}}(\text{Cu}_6\text{Sn}_5)$ are the weight ratios of Sn in Cu₃Sn and Cu₆Sn₅, and $y_{\text{Sn}}(\text{Cu}_3\text{Sn})$ and $y_{\text{Sn}}(\text{Cu}_6\text{Sn}_5)$ are the estimated Sn thicknesses that reacted with Cu to form Cu₃Sn and Cu₆Sn₅.

Kinetic Model Estimation

A simple linear regression model was used to extract the diffusion rate k and the empirical exponent n based upon the measured IMC thicknesses and the model derived from Eq. (1):

$$\ln(y_t^2 - y_0^2) = \ln(k) + 2n \times \ln(t).$$
(4)

The diffusion coefficient k_0 and activation energy Q could further be obtained from the extracted diffusion rate k by

$$\ln(k) = \ln(k_0) - \frac{Q}{R} \times \frac{1}{T}.$$
(5)

IMC Simulation Model

Model Setup

The simulation model for IMC development and estimation of unreacted remaining Sn thickness was based on the extracted kinetic coefficients of Cu₃Sn thickness growth and the amount of Sn that reacted with Cu to form IMCs. The unreacted remaining Sn thickness was calculated from the amount of Sn that reacted with Cu to form IMCs subtracted from the initial Sn thickness. At any given time t, the thickness of the Cu₃Sn layer or the amount of Sn that had reacted with Cu to form IMCs is y_t and the temperature is T_t . Assuming further that $y_0 = 0$, the estimated time required to obtain a given thickness y_t at annealing temperature T_t is

$$t_{\rm est} = \left(\frac{y_t^2}{k_0 \exp\left(\frac{-Q}{RT_t}\right)}\right)^{\frac{1}{2n_t}},\tag{6}$$

$$y_{t+\mathrm{d}t}^2 = k_0 \exp\left(\frac{-Q}{RT_t}\right) \cdot \left[\left(t_{\mathrm{est}} + \mathrm{d}t\right)^{2n_t} \right]. \tag{7}$$

The simulation model for IMC formation was implemented using MATLAB. For any given

wafer-bonding temperature profile and initial metal thicknesses, the model calculates the corresponding IMC thickness and the remaining Sn thickness. Figure 5 shows an example of a simulation result. Note that an initial Cu_6Sn_5 thickness of 0.5 μ m is taken into account in the simulation model.

Prediction of Bonding Parameters and Sn Thickness

With the simulation model shown in Fig. 5, we can predict $t_{\rm Sn}$, the required time that wafers need to be kept at the bonding temperature $T_{\rm b}$ to convert all Sn into IMCs, and $t_{\rm Cu3Sn}$, the time that wafers need to be kept at $T_{\rm b}$ to achieve a final Cu/Cu₃Sn/Cu bond-line. The effect of the initial Sn thickness and bond parameters (contact temperature, bonding temperature, and ramping rate) on $t_{\rm Sn}$ and $t_{\rm Cu3Sn}$ can then be analyzed.

Wafer-Level Bonding

Earlier studies reported Cu/Sn bonding using a Sn thickness between 2.5 μ m and 6 μ m.^{6,13–16} Successful bonding with Sn thickness of 1.5 μ m was also reported for symmetric bonding (1.5 μ m at both bonding surfaces).^{3,12,17} To optimize the wafer-level bonding process further, and in particular to reduce the time spent in the wafer bonder, it is important to select an initial Sn thickness that can accommodate any Cu thickness variation across the wafer, while at the same time ensuring that pure Sn remains at the surface when the two wafers make contact. To reduce the overall bonding time, a thin Sn layer should be used. In this study, an initial Sn thickness of 1.5 μ m was selected for wafer bonding experiments.

To examine the simulation model, two actual bonding experiments were carried out with two



Fig. 5. Results of a typical simulation scenario where the inputs are temperature profile and initial Sn thickness. For this practical simulation, the initial Sn thickness is 1.5 μ m. An initial Cu₆Sn₅ layer thickness of 0.5 μ m is assumed. For this case, the model predicts that all available Sn will be converted after 26 min; furthermore, the Cu₆Sn₅ phase will be converted to Cu₃Sn after 68 min in the wafer bonder.

different bonding temperature profiles. The wafers were bonded in an EVG 501 wafer bonder with the wafer-level bonding temperature profile given in Fig. 1. Details of bond parameters are given in Table III.

Cu/Sn bond frames were prepared by a Cu/Sn electroplating process with layer thicknesses of 5 μ m of Cu and 1.5 μ m of Sn. After electroplating, the Au seed and TiW adhesion layers were etched by KI solution and H₂O₂ solution. Wafers were aligned using an EVG 620 mask-bond aligner and then loaded into the bond chamber. To obtain a vacuum inside the package, the chamber was evacuated and purged. The pressure was reduced to 10^{-3} mbar, and the temperature was ramped to the contact temperature $T_{\rm c}$ (150°C) before the wafers were brought into contact and the bond pressure was applied. The temperature was kept at $T_{\rm c}$ for 5 min and then ramped to the bonding temperature, $T_{\rm b}$ (270°C) . The temperature was kept at T_{b} for 15 min (profile a) or 30 min (profile b). During the bonding process, Cu and Sn react to form solid IMCs. When the bond is finished at t_3 , a final bond-line consisting of only Cu and IMCs is obtained. The bond pressure is then released and the temperature is ramped down.

RESULTS AND DISCUSSION

IMC Characterization

Figure 6 shows the typical development of IMCs after annealing, where the Cu_3Sn and Cu_6Sn_5 phases can be observed. The IMC phases were confirmed by EDS analysis. As seen in Fig. 6b, for the sample annealed at low temperature (150°C), only a thin Cu_3Sn layer is visible, even though a relatively long annealing duration of 80 min was used. At higher temperatures, as shown in Fig. 6c, the IMC growth is accelerated and Sn reacts faster with Cu to form IMCs. For the particular sample shown, no pure Sn remained after annealing. For this reason, only samples annealed between 150°C and 200°C were used for characterizing the remaining Sn on the samples.

Kinetics Model Estimation

Figure 7 shows the resulting measurements and data for estimation of the diffusion rate k and the empirical exponent n from the Cu₃Sn thickness growth and the amount of Sn thickness converted

Table bondir	III. ng te	Bonding mperature	parameters e profiles	for	two	actual

	Profile a	Profile b
Contact temperature	150°C	150°C
Bonding temperature	$270^{\circ}\mathrm{C}$	$270^{\circ}\mathrm{C}$
Bonding time at $T_{\rm b}$	15 min	30 min

into IMCs at different temperatures. The estimated values are extracted using Eq. 4. The diffusion rate k as a function of temperature is shown in Fig. 8. The diffusion coefficient k_0 and activation energy Q were then further extracted from k, based on Eq. 5.

The extracted empirical exponent n for the Cu₃Sn thickness growth and the amount of Sn that reacted with Cu to form IMCs as a function of temperature is shown in Fig. 9. Here we clearly observe different values of n for Cu₃Sn and the amount of Sn thickness that reacted with Cu to form IMCs obtained at different temperatures. For the Cu₃Sn phase at temperatures above the melting point of Sn, n is equal to 1/2. At temperatures lower than the melting point of Sn, a smaller value for *n* is obtained for Cu_3Sn . The same trend with different values of *n* for different annealing temperatures was also observed for Sn. The extracted kinetic coefficients for Cu₃Sn thickness growth and the amount of Sn thickness that reacted with Cu to form IMCs are provided in Table IV.

With the kinetic coefficients listed in Table IV, simulations of the Cu_3Sn growth and the remaining Sn thickness during the annealing process were carried out. Figure 10 shows a comparison between the experimental and simulated data. The remaining Sn thickness was extracted from the amount of Sn that reacted with Cu to form IMCs and the initial Sn thickness.

As shown in Table IV, different empirical exponents n for the Cu₃Sn thickness growth model were obtained below and above the melting point of Sn. This differs from earlier published work, which considered IMC formation to be fully diffusion controlled,^{18–22} with an analytical solution of the diffusion equation of n = 1/2. However, several studies have presented values of n that vary with



Fig. 6. Formation of intermetallic phases during the Cu/Sn annealing process. Both phases of Cu₃Sn and Cu₆Sn₅ can be distinguished from Cu. Formation of Cu₃Sn dominates at high annealing temperatures.



Fig. 7. Extracted diffusion rate k and empirical exponent n from the measured thicknesses. The linear trend represents the empirical exponent n, and the intercept represents the diffusion rate k. Discrete points represent experimental data.



Fig. 8. Diffusion coefficient k_0 and activation energy Q extracted from the diffusion rate k as a function of temperature. The linear trend represents the activation energy, whereas the intercept represents the diffusion coefficient.



Fig. 9. Extracted empirical exponent *n* as a function of temperature for Cu₃Sn and Sn. Note that n = 1/2 (within the measurement accuracy) for $T > T_m$, whereas n < 1/2 for $T < T_m$.

temperature.^{11,23–25} Vianco et al.¹¹ also obtained n = 0.4 for an annealing temperature range below the melting point of Sn (70°C to 205°C). Our present work shows an exponent n < 1/2 for $T < T_m$, implying that the IMC growth rate is slower than can be explained by diffusion rates, showing that the chemical reaction kinetics is slow in this temperature regime. We observe n = 1/2 for $T > T_m$,

consistent with a faster chemical reaction rate and an IMC growth rate limited by diffusion alone. Thus, the diffusion mechanism is the dominating factor for IMC formation in the wafer-bonding process between $T_{\rm m}$ and $T_{\rm b}$.

To characterize the amount of Sn that is converted into IMCs in the bonding process, annealing temperatures below the melting point of Sn were

	Cu_3Sn	Reacted Sn
Diffusion coefficient, $k_0 \ (\mu m^2/\min^{2n})$	$7.9 imes10^{6}$	$2.8 imes10^4$
Activation energy, Q (kJ/mol K)	78	52
Empirical exponent, <i>n</i>	0.5 for $T \ge 232^{\circ}$ C	0.45 for $T \ge 180^{\circ}$ C
	$0.4 \text{ for } T < 232^{\circ} \text{C}$	$0.3 \text{ for } T < 180^{\circ}\text{C}$

Table IV. Estimated kinetic coefficients for Cu_3Sn and the amount of Sn thickness that reacted with Cu to form IMCs



Fig. 10. Comparison between simulation results and estimated values for both Cu_3Sn thickness and remaining Sn. The continuous line represents simulation, and the discrete points represent measured and extracted thickness values from the experimental data, with standard deviation. For this simulation, the initial Sn thickness was assumed to be 2.3 μ m.

used. Above the melting point of Sn, no pure Sn will remain on the Cu surface, however to obtain high bonding yield, pure and ductile Sn should remain at the interface of the two bonding partners when reaching the melting point of Sn.⁹ Therefore, the thickness of unreacted remaining Sn between the bonding surfaces of the two wafers at the contact point, $T_{\rm c}$, as well as at the melting point of Sn ($T_{\rm m}$) are two of the most critical parameters for a high-yield wafer-level bonding process.

Figure 11 shows a comparison of diffusion constants k collected from literature in addition to our study. The lines, which represent the activation energy (-Q/R), all have a similar slope, corresponding to Q = 50 kJ/mol(mol K) to 80 kJ/mol (mol K).^{10,19,26} However, the intercepts [which represent the diffusion coefficient, ln (k_0)] vary significantly between the studies. Liu et al.²⁵ suggested that the Cu grain size has a significant effect on the growth rate and thickness of IMC formation. With a smaller Cu grain size, the IMC growth rate will increase.

IMC Simulation Model

Predicting the Effect of Bonding Parameters

Since the IMC formation is not accelerated at temperatures below the melting point of Sn, the effects of $T_{\rm c}$ and the ramping rate of the first ramp

step to $T_{\rm c}$ are not critical for $t_{\rm Sn}$ (required time that wafers should be kept at $T_{\rm b}$ to consume all Sn into IMCs) and $t_{\rm Cu3Sn}$ (required time that wafers should be kept at $T_{\rm b}$ to achieve a final Cu/Cu₃Sn/Cu bondline). In addition, as the time that the wafers are kept at the contact temperature is short (several minutes), the effect of the contact temperature can be neglected.

Effect of Initial Sn Thickness

Typically in wafer-level bonding, the Sn thickness varies between 1 μ m and 3 μ m.^{3,4,12} Figure 12 shows simulation results for t_{Cu3Sn} and t_{Sn} as functions of initial Sn thickness.

Effect of Temperature

The bonding temperature plays an important role in the wafer-bonding process. Different bonding temperatures (240°C to 300°C) were simulated. Figure 13 shows the simulated results for $t_{\rm Sn}$ and $t_{\rm Cu3Sn}$ as functions of bonding temperature.

Effect of Ramping Rate

The effect of ramping rate on IMC formation is important to characterize. If the ramping rate is low, more Sn reacts with Cu to form IMCs before the melting point of Sn (T_m) is reached. In the case that all the Sn reacts with Cu to form IMCs before T_m , successful bonding is not obtained.



Fig. 11. Comparison of diffusion constants k collected from literature and this study. The relatively similar slope indicates that the activation energy Q is similar; however the spread of data means that the diffusion coefficient k_0 varies, showing dependence on the material properties of Cu.



Fig. 12. t_{Sn} and t_{Cu3Sn} as functions of initial Sn thickness; bonding temperature, 270°C; contact temperature, 150°C; first and second step ramp rates, 10°C/min and 5°C/min.

Different bonding temperature profiles with different second step ramp rates of 5°C/min to 30°C/ min were selected for simulation. For these temperature ramping rates, the contact temperature was maintained at 150°C, the bonding temperature was kept at 270°C, and the initial Sn thickness was set to 1.5 μ m. Figure 14 shows the simulated results for $t_{\rm Sn}$ and $t_{\rm Cu3Sn}$ as functions of the second step ramp rate.

The simulation results for t_{Cu3Sn} and t_{Sn} as functions of initial Sn thickness, bonding temperature, and ramping rate show that the initial Sn thickness



Fig. 13. t_{Cu3Sn} and t_{Sn} as functions of bonding temperature; contact temperature, 150°C; first ramp rate, 10°C/min; second ramp rate, 5°C/min; initial Sn thickness, 1.5 μ m.

and bonding temperature are the most critical parameters that affect the bonding time. Therefore, to reduce the overall processing time in the wafer bonder, an effective solution is to reduce the initial Sn thickness or to increase the bonding temperature. For MEMS devices which are sensitive to temperature, the bonding temperature may be limited. For thin initial Sn layer thickness, optimization of the temperature profile, in particular the contact temperature and ramping rate, is important to ensure that there remains unreacted Sn at the bond interface when the melting point of Sn is reached.

Comparison of Simulated and Experimental Results

Figure 15a shows a cross-section of a bond-line that consists of both Cu₃Sn and Cu₆Sn₅. We observe matching of the simulated and experimental thickness of the Cu₃Sn layer. From the simulation, the thickness of the Cu₆Sn₅ layer should be $2 \times 0.5 \ \mu\text{m} = 1 \ \mu\text{m}$. This thickness matches quite well with the measured Cu₆Sn₅ thickness (0.7 μ m). The observed deviation can be explained by the fact that the initial Sn thickness of this actual frame may be less than 1.5 μ m. Furthermore, liquid Sn



Fig. 14. t_{Cu3Sn} and t_{Sn} as functions of the second ramping rate; bonding temperature, 270°C; contact temperature, 150°C; first step ramp rate 10°C/min; initial Sn thickness, 1.5 μ m.

flows and may be squeezed out during the bonding process, leading to somewhat reduced Cu_6Sn_5 layer thickness compared with the simulated results from our 1D model.

To achieve a final Cu/Cu₃Sn/Cu bond-line, the time that the wafers need to be kept at the bonding temperature should be longer—30 min in this case, as shown in Fig. 15b. Here, the predicted result that all IMC is converted to Cu₃Sn is confirmed by experiment. With this bonding method, we obtained dicing yield of 100% (the percentage of dies that remained after dicing) and sealing yield of 80% (the percentage of dies that retained vacuum inside after dicing).

The reactions of Cu and Sn to form IMCs induce a volumetric change, due to differences in mass density (Table V). For the layer thicknesses in our experiments, complete conversion of all Sn to Cu_6Sn_5 corresponds to an overall volume reduction of 2%. Complete conversion to Cu_3Sn corresponds to a further 2% volume reduction. To accommodate this volume reduction, it is important that the design does not impose restrictions on the bond-line to accommodate this volumetric change. In wafer bonding, the applied pressure will ensure that this volumetric change is accommodated.

Table V. Cu, Sn, and IMC mass densities

	Cu	Sn	Cu ₃ Sn	Cu ₆ Sn ₅
Mass density (g/cm ³)	8.9	7.3	8.9	8.3



Fig. 15. Different designed bonding profiles for Cu/Sn SLID wafer-level bonding. The first ramping rate is 10° C/min; the second ramping rate is 4° C/min. Wafers are kept at contact temperature of 150° C for 5 min. For profile a: the bonding time at 270° C is 10 min, and the final bond interface consists of Cu₃Sn and Cu₆Sn₅. For profile b: the bonding time at 270° C is 30 min, and a final Cu₃Sn bond interface is achieved.

Turther annealing time t_{anneal} to convert an the Cu ₆ Sn ₅ into Cu ₃ Sn							
<i>T</i> _b (°C)	240	250	260	270	280	290	300
$t_{ m bond} \ ({ m min}) \ t_{ m anneal} \ ({ m min})$	11 96	7 67	4 47	$\frac{1}{34}$	$0 \\ 24$	0 16	0 10

Table VI. Required bonding time t_{bond} to achieve a final Cu/Cu₃Sn/Cu₆Sn₅/Cu₃Sn/Cu bond-line and required further annealing time t_{anneal} to convert all the Cu₆Sn₅ into Cu₃Sn

The initial Sn thickness is $1.5 \ \mu\text{m}$. The ramping rates of the first and second ramp steps are 10° C/min and 5° C/min. The contact temperature is 150° C. The time that the wafers are kept at the contact temperature is 5 min

Bonding Temperature Profile Optimization

The experiment shown in Fig. 15 and the simulation results for t_{Sn} and t_{Cu3Sn} shown in Figs. 12–14 show that the overall process time in the wafer bonder can be reduced by allowing the final bond-line to consist of Cu/Cu₃Sn/Cu₆Sn₅/ Cu₃Sn/Cu with further annealing of a larger batch of wafers to convert all the Cu₆Sn₅ into Cu₃Sn. The simulation results for t_{bond} and t_{anneal} at different selected temperatures are presented in Table VI, where t_{bond} is the required time that wafers need to be kept at the bonding temperature to achieve a Cu/ $Cu_3Sn/Cu_6Sn_5/Cu_3Sn/Cu$ bond interface, and t_{anneal} is the required annealing time to convert all the Cu_6Sn_5 into Cu_3Sn . Since the bond is left with a final Cu/Cu₃Sn/Cu₆Sn₅/Cu₃Sn/Cu interface, the effect of bonding temperature on the processing time in the wafer bonder can be minimized.

Another effective solution to reduce the overall bonding time is to increase the temperature ramping rate. Since a high ramping rate is used, the initial Sn thickness is also reduced.⁹ The challenge is that a high ramping rate can cause delamination of bond frames (between the adhesion layer and silicon dioxide) due to thermal stress. In addition, for a vacuum wafer-level encapsulation process, a pump/purge process is required to obtain a lower pressure, and this pressure should be achieved before the wafers are brought into contact. The pumping process requires time, thus a slow ramping rate may be required. However, if a slow ramping rate is used, all Sn may be converted into IMCs before the melting point of Sn is reached. Therefore, there is a tradeoff between process time, pumping time, and contact temperature.

CONCLUSIONS

The formation of IMCs which takes place during the Cu/Sn SLID wafer-level bonding process was successfully characterized. Thermal kinetics models of the Cu₃Sn thickness and the amount of Sn that is converted into IMCs were developed. One of the major findings of our study is that the empirical coefficient n depends on temperature. Above the melting point of Sn, n is equal to 1/2, as expected from the analytical solution of the diffusion equation, corresponding to a diffusion-controlled process. For temperatures below the melting point of Sn, a value of n below 1/2 is obtained, indicating that slower chemical reaction limits the IMC growth rate.

Based on this knowledge of IMC formation during the annealing process, a MATLAB model was created to simulate the IMC development during the bonding process. Using this simulation model, we can predict the parameters that are important for bonding temperature profile optimization: unreacted remaining Sn thickness on each wafer at the contact temperature and bonding temperature, and required bonding times to achieve Cu/Cu₃Sn/ Cu₆Sn₅/Cu₃Sn/Cu and Cu/Cu₃Sn/Cu final bondlines. Experiments show that the simulation model accurately predicts the IMC formation during the bonding process. The experimental and simulation results show that an effective solution to reduce the bonding time is to leave the final bond-line as Cu/ Cu₃Sn/Cu₆Sn₅/Cu₃Sn/Cu, with further annealing performed outside the wafer bonder to convert all the Cu_6Sn_5 into Cu_3Sn .

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REFERENCES

- N. Hoivik and K. Aasmundtveit, Handbook of Wafer Bonding (Wiley-VCH Verlag, 2012), pp. 181–214.
 N. Hoivik, H. Liu, K. Wang, G. Salomonsen, and K. Aas-
- N. Hoivik, H. Liu, K. Wang, G. Salomonsen, and K. Aasmundtveit, Advanced Materials and Technologies for Micro/Nano-Devices, Sensors and Actuators, ed. E. Gusev, E. Garfunkel, and A. Dideikin (Springer: Netherlands, 2010), pp. 179–190.

- A. Lapadatu, T.I. Simonsen, G. Kittilsland, B. Stark, N. Hoivik, V. Dalsrud, and G. Salomonsen, *ECS Trans.* 33, 73 (2010).
- H. Liu, G. Salomonsen, K. Wang, K.E. Aasmundtveit, and N. Hoivik, *IEEE Trans. Compon. Packag. Manuf. Technol.* 1, 1350 (2011).
- Y. Cao, W. Ning, and L. Luo, *IEEE Trans. Electron. Packag.* Manuf. 32, 125 (2009).
- R. Yibo et al., International Conference on Electronic Packaging Technology and High Density Packaging (ICEPT-HDP'09) (2009).
- 7. H.J. van de Wiel et al., 4th Electronic System-Integration Technology Conference (ESTC), Amsterdam (2012).
- 8. H. Etschmaier, et al., J. Mater. Eng. Perform. 21, 1724 (2012).
- 9. N.S. Bosco and F.W. Zok, Acta Mater. 52, 2965 (2004).
- 10. W. Peng, E. Monlevade, and M.E. Marques, *Microelectron. Reliab.* 47, 2161 (2007).
- P. Vianco, J. Rejent, and P. Hlava, J. Electron. Mater. 33, 991 (2004).
- 12. A. Duan et al., 4th Electronic System-Integration Technology Conference (ESTC), Netherland (2012).
- 13. C. Yuhan and L. Le, J. Semicond. 30, 086001 (2009).
- 14. D.Q. Yu and M.L. Thew, 3rd Electronic System-Integration Technology Conference (ESTC) (2010).

- 15. H. Zhihong et al., 58th Electronic Components and Technology Conference (ECTC 2008) (2008).
- 16. R. Labie, et al., 3rd Electronic System-Integration Technology Conference (ESTC) (2010).
- 17. T.T. Luu et al., 4th Electronic System-Integration Technology Conference (ESTC), Amsterdam (2012).
- Y.C. Chan, A.C.K. So, and J.K.L. Lai, *Mater. Sci. Eng. B* 55, 5 (1998).
- W.-M. Tang, et al., Trans. Nonferr. Met. Soc. China. 20, 90 (2010).
- P.J. Shang, Z.Q. Liu, D.X. Li, and J.K. Shang, J. Electron. Mater. 38, 2579 (2009).
- H.F. Zou, H.J. Yang, and Z.F. Zhang, Acta Mater. 56, 2649 (2008).
- 22. G.-T. Lim, B.-J. Kim, K. Lee, and J. Kim, *J. Electron. Mater.* 38, 2228 (2009).
- 23. T. Takenaka, et al., Mater. Sci. Eng. A 396, 115 (2005).
- 24. R. Gagliano and M. Fine, J. Electron. Mater. 32, 1441 (2003).
- H. Liu, K. Wang, K.E. Aasmundtveit, and N. Hoivik, J. Electron. Mater. 41, 2453 (2012).
- S. Mattafirri, et al., *IEEE Trans. Appl. Supercond.* 13, 3418 (2003).