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Low Capacitive Inductors for Fast Switching Devices in Active Power Factor Correction Applications

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***Abstract*-This paper examines different winding strategies for reduced capacitance inductors in active power factor correction circuits (PFC). The effect of the parasitic capacitance is analyzed from an electro magnetic compatibility (EMI) and efficiency point of views. The purpose of this work is to investigate different winding approaches and identify suitable solutions for high switching frequency/high speed transition PFC designs. A low parasitic capacitance PCB based inductor design is proposed to address the challenges imposed by high switching frequency PFC Boost converters**

Keywords— Parasitic capacitance, PFC, boundary conduction mode (BCM), high frequency.

I. Introduction

Increased switching frequency operation in power electronics converters permit achieving high power densities due to the size reduction of the energy storage elements in the circuit. Resonant converters have been a common approach to overcome the reduced switching speeds in the active devices, making possible to mitigate or completely eliminate the switching losses present in hard switching topologies. On the other hand, a new era in power electronics is approaching and starting to be a reality with the introduction of wide bandgap devices based on silicon carbide (SiC) and gallium nitride (GaN) materials. The increased electrical strength and electrical conductivity in these materials allows for a reduction of the switch die size, consequently reducing the device parasitic capacitance, which directly increases the achievable switching speed of these devices. Previous works have proven the advantages of the utilization of wide bandgap devices, [1], [2]. However, increased hard switched converter operating switching frequencies requires more attention to be put into the printed circuit board (PCB) and magnetic components design in order to minimize the introduction of parasitic inductances and capacitances into the circuit.

The work presented in this paper focuses on the reduction of the parasitic capacitances of the PFC input inductor. Some research has already been performed on parasitic capacitance calculations based on analytical models [3], [4], [5] and finite element analysis [6]. The solution presented in [7] and [8] proposes a new winding strategy for reduction of inductors self-capacitance for SiC based power converters. A model for calculating the parasitic capacitance is addressed, and finally the effect of the reduction of this parasitic component is analyzed based on several measurements performed with different SiC devices. Some research has already been performed on the inductor self-capacitance effect on boost PFC's EMI performance. This work is part of a larger research project where the goal is to successfully introduce and take advantage of wide band gap devices for single phase PFC converters. It is the authors' opinion that this implicit means that the switching frequency must be increased in order to fully take advantage of these new devices. The justification of this paper is the work done on comparing different winding strategies in terms of EMI, switching and conduction loss. Furthermore, a novel winding strategy based on PCB manufacturing for reduced cost inductors with low ac resistance and self-capacitance is proposed. The proposed solution addresses the requirements for inductor designs in high frequency boost derived PFC circuits.

II. Inductor Parallel Capacitance

The inductor behavior at very high frequencies is clearly dominated by the parasitic capacitance effect and other non-ideal behavior. The component impedance can be approximated based on lumped parasitic models, which can be simplified to the model shown in Fig. 1.

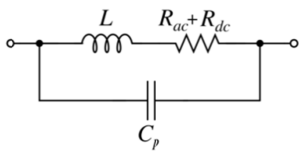

Fig. 1 Inductor equivalent simplified model

This model, presented in [9], includes the windings dc and ac resistances, which will effectively affect impedance curve quality factor at the component resonant frequencies. A parallel resistor, modeling the inductor core loss, is included in [10]. A more complex model based on impedance measurement fitting is presented in [11] and [12], in order to take into account very high frequency parasitic effects.

As presented in [7] and [8], if the capacitance has to be minimized, the layer to layer, the first turn to last turn and the turn to core capacitances represent the mayor contribution to the final capacitance of the inductor. This is due to the fact that even if the turn to turn capacitance is larger than the last ones, they will be interconnected in series minimizing its effect.

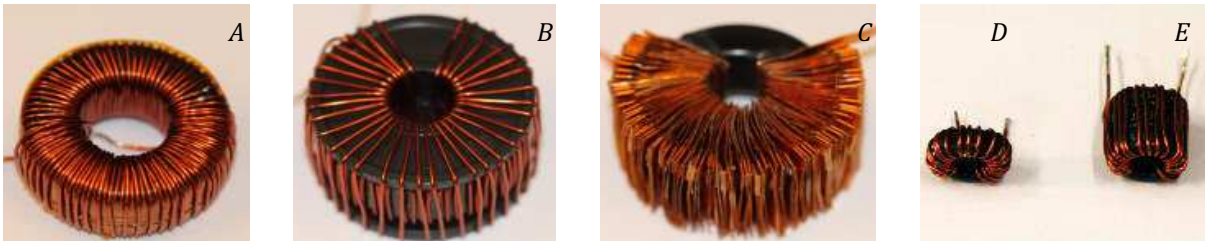

Fig. 2. Implemented inductor prototypes. A-Conventional double layer, B-Double layer with separator, C-Copper foil, Small size low capacitance inductors D-25 μH and E-69 μH.

III. Prototype Implementation

In order to compare the performance of different winding strategies, a toroidal Kool Mu core from Magnetics is selected. The same copper cross section and number of turns is used in all the implemented prototypes, to perform a fair comparison between the different winding structures. Toroidal cores are selected because they provide a large winding area compared to the core volume and represent a low cost solution in PFC inductor implementation. A first prototype is implemented using a conventional two layer structure that will present very large capacitance due to the layer-to- layer capacitance contribution. The selected core is 0077439A7 Kool Mμ 60 from Magnetics®. The winding is implemented using 94 turns of AWG 18 coated cable obtaining an inductance value of 1.2 mH. The well-known progressive winding or sectioned bobbin techniques [13] for reducing self-capacitance are not considered because of the difficulty of implementation in toroidal shaped cores. Instead, based on the work presented in [7] and [8], a two layer toroidal core with a layer to layer separator is implemented for layer-to-layer capacitance reduction. Moreover, a gap is introduced from first to last turn in each of the layers for reduction of the parasitic capacitance. Finally, in order to evaluate the feasibility of introducing PCB windings for this design, a copper foil implementation is selected where the copper cross section is adjusted to match the AWG18 cross section. This structure will present a relatively large turn-to-turn capacitance due to the increased area of the equivalent capacitance plates as shown in (1). Where ε_r is the relative permittivity, A is the plate area and d is the distance between plates.

$$C = \varepsilon_r \cdot \varepsilon_0 \cdot \frac{A}{d} \tag{1}$$

However this structure will not present any of the critical layer-to-layer or first turn to last turn contribution due to the fact that the increased fill factor will allow implementing the same amount of turns in a single layer structure with a large gap between first and last turn. Moreover, this structure presents a reduced turn to core capacitance contribution respect to the conventional windings because of the reduced A/d ratio. To finalize the comparison, as suggested in [14], the effect of adding a small inductor with very low capacitance in series with a multilayer high capacitance design is analyzed by constructing two single layer toroids using one core and three stacked cores Magnetics® Kool Mμ 125 0077350A7 with an inductance value of 25.9 and 69.9 μH respectively. The implemented prototypes are presented in Fig. 2 and the impedance measurements results are shown in Fig. 3 and Fig. 4.

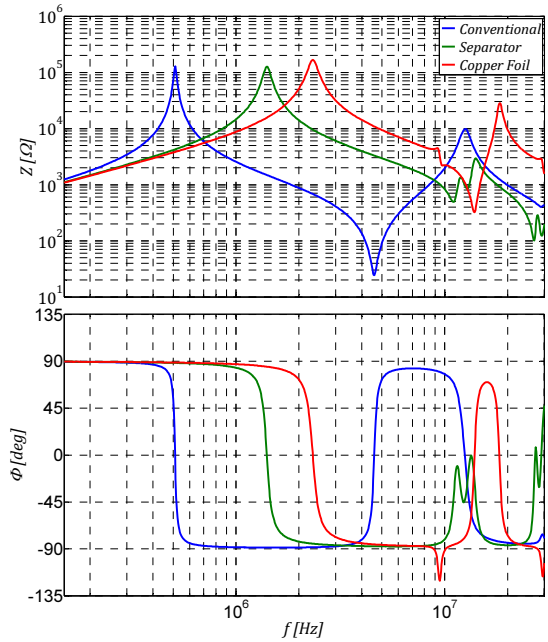

Fig. 3. Impedance and phase magnitudes in the conducted EMI frequency range ($150\,kHz - 30MHz$) for the conventional (blue), separator (green) and copper foil (red) inductors.

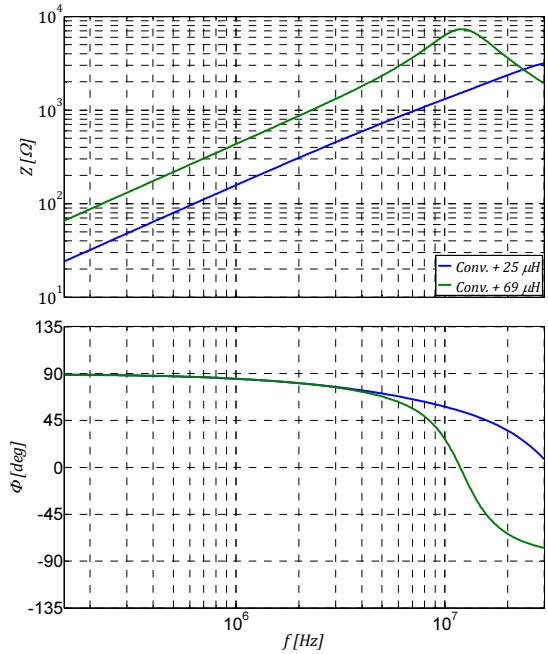

Fig. 4. Impedance and phase magnitudes in the conducted EMI frequency range ($150\,kHz - 30MHz$) for the small size inductors 25 μH (blue), 69 μH (green).

The parallel capacitance is calculated from the measured parallel resonant frequency and inductance value. The obtained values are shown in Table I.

TABLE I
PROTOTYPES' INDUCTANCE AND CAPACITANCE VALUES

Prototype	$L\ [mH]$	$f_0\ [MHz]$	$C_p\ [pF]$
Conventional	1.21	0.51	80.5
Separator	1.16	1.41	11
Copper Foil	1.15	2.34	4
25 μH	0.0259	32.5	1
69 μH	0.0698	11.8	2.7

As it can be observed form Table I, the two layer structure with separator has seven times lower capacitance than the conventional structure due to the reduced layer to layer capacitance and the inserted gap between the first and last turn in each of the layers. The copper foil implementation reaches a capacitance level twenty times lower than the conventional structure. Even with a much larger turn to turn capacitance this structure achieves the smallest parasitic capacitance value. Finally, the low size implemented inductors present a quasi-ideal behavior up to 30 MHz with a parasitic capacitance of 1 and 2.7 pF respectively.

IV. CONDUCTED EMI MEASUREMENTS

The EMI performance of the different implemented prototypes is analyzed using an ac-dc converter evaluation board from Texas Instruments PMP669 (Fig. 5) where the dc-dc conversion power stage has been disabled and the input EMI filter completely removed.

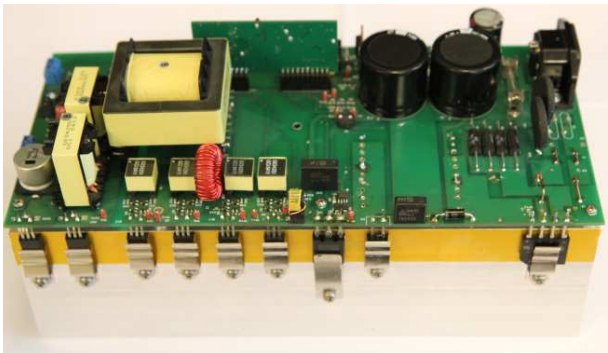

Fig. 5. AC-DC converter with conventional PFC. Evaluation board from Texas Instruments PMP669 MB

The EMI measurement is performed using a Two-line V-Network (LISN) with the converter operating @ $f_{sw} = 98\ kHz$ $V_{ac} = 230\ V_{rms}$ and $P_o = 200\ W$. Fig. 6 shows the measurement result for the three main different prototypes. Fig. 7 shows the effect of adding the small inductor in series with the conventional two layer inductor.

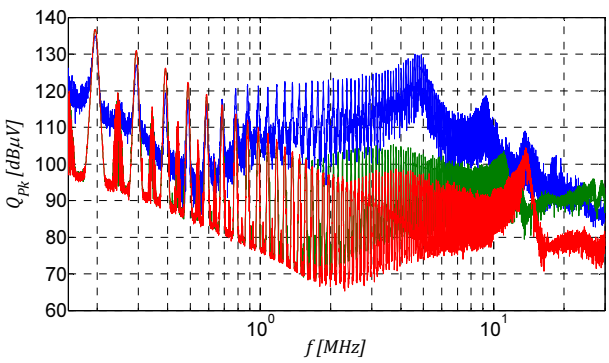

Fig. 6. EMI measurement using LISN network from 150 kHz to 30 MHz @ 230 V_{rms} and 200 W for the conventional (blue), separator (green) and copper foil (red) implemented inductors.

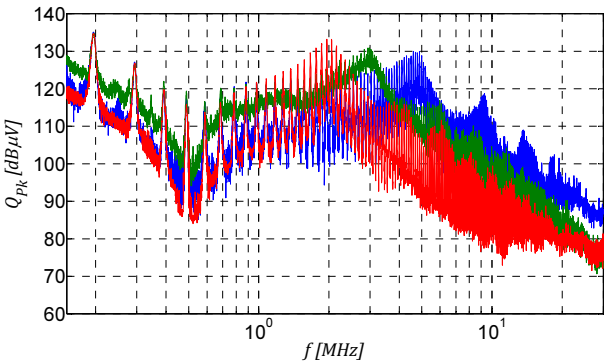

Fig. 7. EMI measurement using LISN network from 150 kHz to 30 MHz @ 230 V_{rms} and 200 W .Conventional (blue), conventional+ 25 μH (green), and conventional+ 68 μH (red).

The capacitance reduction obtained in the two layers with separator and the copper foil implementations provide a significant reduction in conducted EMI ss it can be observed in Fig. 6. The conventional structure shows high amplitude harmonics around 5.5 MHz which corresponds to the location of the minimum impedance measured for this prototype (Fig. 3). Fig. 7 shows the small effect of adding a small series inductance in series with the conventional two layer inductor. In fact, as it can be observed, the high frequency noise will be reduced due to the increased impedance in this area. On the other hand, at low frequencies, the introduction of this inductance will reduce the frequency of the minimum inductor impedance, increasing the propagated noise due to the higher amplitude of the switching frequency harmonics and the increased quality factor at this resonant frequency due to the reduced ac resistance.

V. EVALUATION OF THE IMPACT ON THE SWITCHING AND CONDUCTION LOSS

After comparing the different configurations in terms of conducted EMI, an efficiency related comparison is performed using a low inductive double pulse tester (DPT) shown in Fig. 8. A small die size 600V super-junction device FCD9N60N from Fairchild Semiconductor is used in combination with a 600V SiC diode IDD10SSG60C from Infineon Technologies.

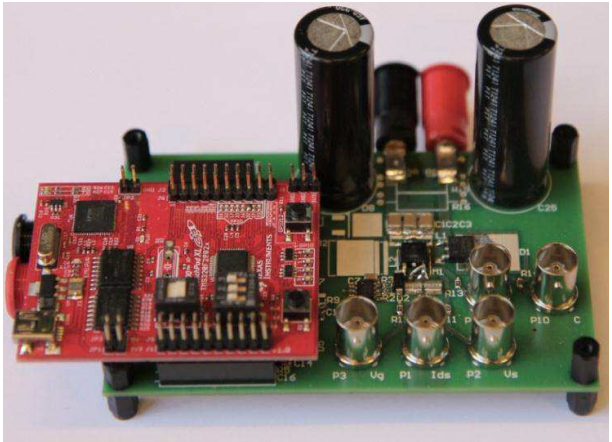

Fig. 8. Implemented double pulse tester prototype.

Fig. 9 shows the DPT switching waveforms for the conventional inductor (green current) and the copper foil prototypes for an inductor current level of 6A and a bus voltage of 400V. Fig. 10 shows the switching waveforms for the conventional two layer inductor (green current) in series with the 25 μH (purple) and the 69 μH (blue) prototypes.

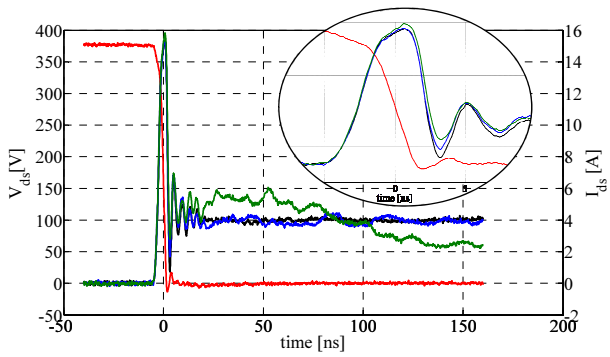

Fig. 9. Switching waveform comparison between the conventional (green current waveform) and the copper foil (blue current waveform) inductor prototypes.

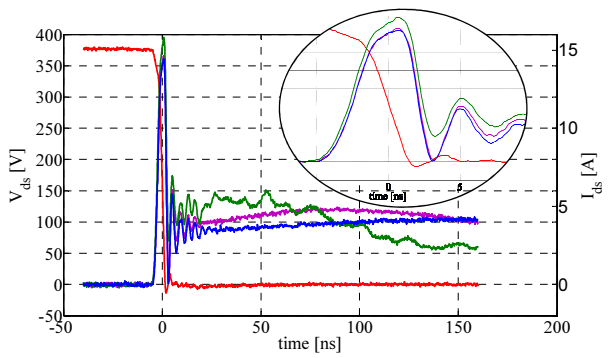

Fig. 10. Switching waveform comparison between the conventional (green current waveform) and conventional with series 25 μH (purple) and 69 μH (blue) inductor prototypes.

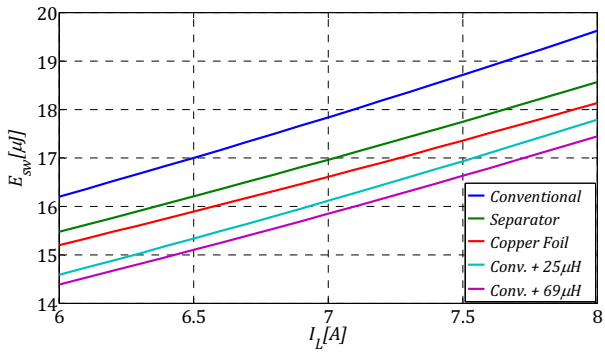

Fig. 11. MOSFET switching energy as a function of the inductor current level for the different inductor prototypes.

After performing a switching energy loss extraction, the turn on energy dissipated in the MOSFET is plotted as a function of the inductor current level (Fig. 11). As it can be observed, a small difference is obtained in the MOSFET turn on loss due to the inductor parasitic capacitance effect. Acording to the difference in calculated capacitance value and according to (2), the difference in energy loss from the standard double layer and the copper foil inductors should be at least 6 μJ

$$E = \frac{1}{2} \cdot C \cdot V^2 \tag{2}$$

However, this difference from the measurement to the calculation can be easily explained by looking at Fig. 9 and Fig. 10. As it can be observed the dissipated energy in the MOSFET before the drain to source voltage collapses to zero varies very little between the different measurements. This is due to the fact that the parasitic capacitance will not be charged on this small subinterval. Instead this capacitance will resonate with the parasitic inductance formed by the inductor interconnection and will finalize the charge long time after the switch has completed the switching transition. It can be concluded that the charge of the parasitic capacitance will not create a large increment in the MOSFET switching loss but it will increase the conduction losses in the inductor because of the presence of a high frequency resonant current that will be damped by the component ac resistance. Furthermore, there is also a risk that these resonances can couple through parasitic capacitances to the converter structure and generate common mode noise source further challenging the input EMI filter. Finally, as it can be observed in Fig. 10 the inclusion of the small size inductors in series with the standard double layer inductor will effectively reduce the frequency of this resonance minimizing the joule losses in the circuit because of the reduced ac resistance effect at lower frequencies.

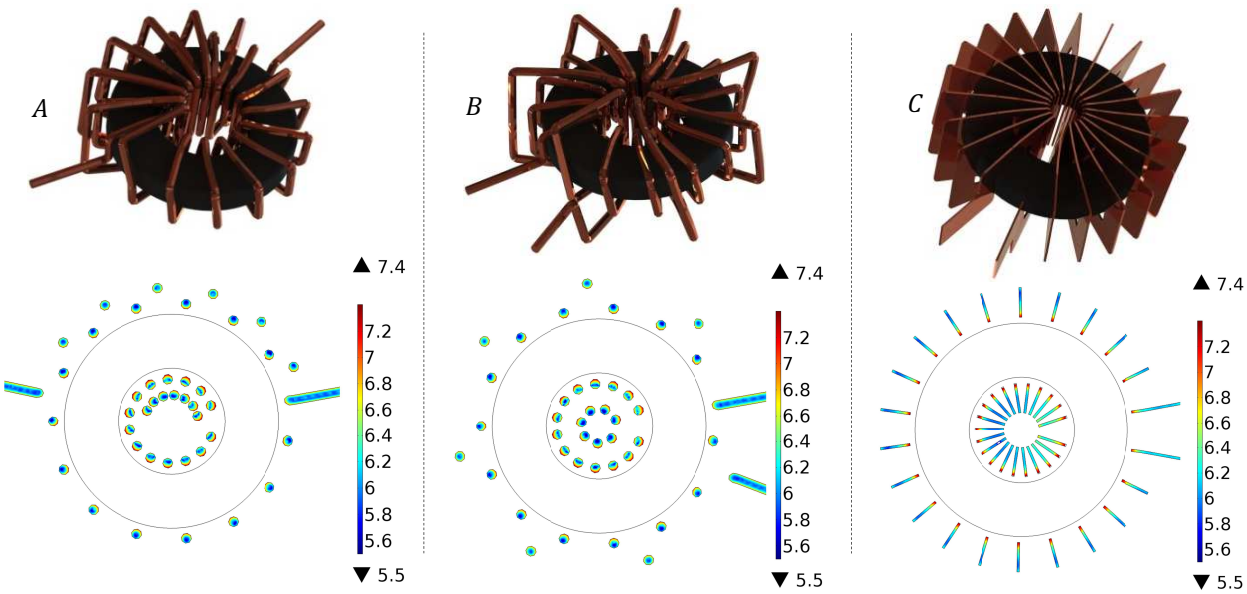

Fig. 12. Simulated inductor structures and 2d plots of the windings current density. A-Conventional double layer, B-Double layer with separator, C-Copper foil.

In order to complete the analysis of the different designs is important to evaluate the ac resistance of the different structures. This is a very important parameter in PFC applications with boundary conduction mode (BCM) operation where the inductor current presents a large high frequency component. Ac resistance measurement of inductors is a difficult task because when the measurement is performed, the magnetic material losses are included in the measurement and they are difficult to separate from each other. Another possibility is to perform an analytical calculation based on Dowell equations (3) where h is the copper thickness amd δ is the skin depth.

$$\frac{R_{ac,m}}{R_{dc,m}} = \frac{\xi}{2}\left[\frac{\sinh\xi + \sin\xi}{\cosh\xi - \cos\xi} + (2m-1)^2\frac{\sinh\xi - \sin\xi}{\cosh\xi + \cos\xi}\right]$$

$$\xi = \frac{h}{\delta} \qquad \delta = \frac{7.5}{\sqrt{f}} \quad [cm] \qquad (3)$$

However even considering that this work takes into account skin and proximity effects, it will not provide a correct solution in this specific problem where a 3d structure is evaluated with a variable distance between turns and layers. Instead, a finite element analysis (FEA) is performed by constructing a 3d model of the different analyzed winding strategies. The size of the simulated inductors is reduced to minimize the complexity of the solution. The same copper cross section $A = 0.56\ mm^2$ is used in the simulated structures. The three implemented models are shown in Fig. 12. A simulation is performed where the ac resistance is calculated for different frequencies up to $400\ kHz$. The windings are meshed to take into account the skin effect. Fig. 12 shows a current density plot of the three different structures at a frequency of $400\ kHz$ represented with a logarithmic colorbar. The skin effect can be easily appreciated in the inductor terminals in the conventional and the separator structures. All the structures present a higher current density near the core due to the high concentration of flux lines in the core proximity. The proximity effect of the second layer can be seen in the inner part of the toroid in the conventional structure where the first layer presents a high current density area in the close proximity to the second layer windings.

The obtained ac resistance for the different structures is shown in Fig. 13. All the structures present a similar ac resistance value at $100\ Hz$ of around $18\ m\Omega$. The conventional structure ac resistance value increases up to $1.54\ \Omega$ compared with $1.07\ \Omega$ and $0.63\ \Omega$ for the separator and copper foil structures respectively.

Finally, the effect of the parasitic capacitance in the converter efficiency is analyzed by testing the copper foil and the conventional implemented inductor prototypes in a PFC stage operating in BCM. The power stage is a modular PFC design operated with a superjunction 600V MOSFET 65R230C7 and a SiC 600V diode IDD04SG60C. The MOSFET is driven by a high current 9A driver FAN3122 and controlled by a BCM controller FAN7930B. Fig. 14 shows the implemented PFC power stage and Fig. 15 shows the measured converter efficiency as a function of the converter output power for a constant dc input voltage $V_{in} = 200V$ and an output voltage $V_{out} = 375V$.

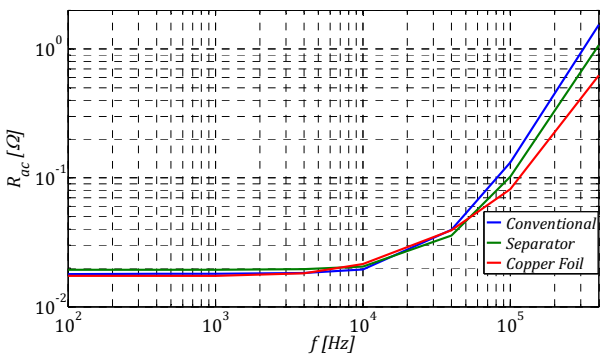

Fig. 13 Simulated ac resistances of the different analyzed structures

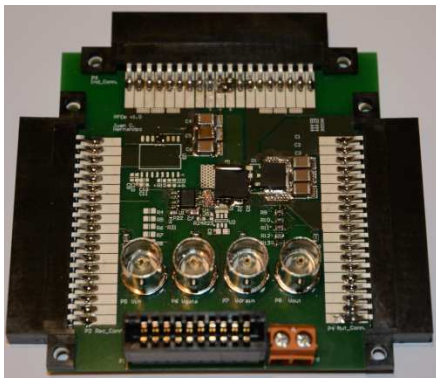

Fig. 14 Implemented modular PFC power stage

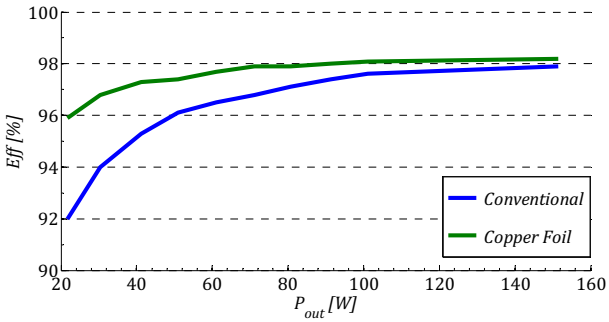

Fig. 15 Measured efficiency as a function of the converter output power for $V_{in} = 200\ V$ and $V_{out} = 375\ V$.

The effect of the capacitance can be appreciated at very low power levels. Under this situation, the converter switching frequency is increased up to $215\ kHz$. The difference in power loss between the two solutions is $0.96W$. With the operating voltage levels, the inductor parasitic capacitor changes its voltage from $200V$ to $-175V$. Taking into account the measured capacitance for the two prototypes, this change in voltage corresponds to a dissipated energy difference of $2.7148\ \mu J$ which corresponds to a power loss difference of $0.58\ W$. Therefore the remaining power loss difference is attributed to ac resistance difference between the two structures. As it can be seen, as the converter output power increases the two efficiency measurements get closer because the converter switching frequency is reduced down to $48\ kHz$ at $150\ W$ output power, minimizing the ac resistance difference between the prototypes.

VI. Conclusions

This paper analyzes different inductor winding structures focusing on parasitic capacitance reduction of the component. The parasitic capacitance effects are analyzed from conducted EMI and efficiency point of views. Different solutions for reduced capacitance effects are evaluated. The ac resistance of the different structures is evaluated together with the capacitance because it has a large impact on PFC converters efficiency operating in BCM mode. A copper foil winding structure is proposed with very low parasitic capacitance and ac resistance compared to the conventional structures. This foil winding structure is similar to using PCB windings in a U core or E core structure. Using a single layer configuration can be very effective in reducing the parasitic capacitance mitigating EMI conducted and radiated problems and improving the converter efficiency. Moreover high frequency PFC converters operating in BCM will benefit from a reduced winding ac resistance

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