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HIGH-PERFORMANCE DIGITAL FILTER IN FPGA

SITI SUHAILA MOHD YUSOF

UNIVERSITI TEKNOLOGI MALAYSIA

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SITI SUHAILA MOHD YUSOF

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requirements for the award of the degree of
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Specially dedicated to my beloved family, lecturers and friends
for the guidance, encouragement and inspiration throughout my journey of education

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ABSTRACT

Digital filtering algorithms are most commonly implemented using general purpose digital signal processing chips for audio applications, or special purpose digital filtering chips and application- specific integrated circuits (ASICs) for higher rates. Based on the study digital filter which is Infinite Impulse Response (IIR) filter, the filter is generally used in the lower sample rates, that is less than 200 kHz (2009) [2]. These filters are used over a wide range of sample rates and are well supported in terms of tools, software, and IP cores. In this research, a high performance and area optimized infinite impulse response (IIR) filter realization in field programmable gate arrays (FPGAs) is proposed. The advantages of the FPGA approach to digital filter implementation include higher sampling rates than are available from traditional DSP chips, lower costs than an ASIC for moderate volume applications, and more flexibility than the alternate approaches. Since many current FPGA architectures are in-system programmable, the configuration of the device may be changed to implement different functionality if required. The main goal of this project is to mapping data flow graphs (DFGs) from the BiQuad architecture direct form II of Infinite Impulse Response filtering algorithms into application specific structure is considered. This filter realizes BiQuad Methods was structured with the high throughput, high clock frequency (Fmax), low Critical Path Delay (CPD), and low Latency (L). Optimization method is proposed which provides designing pipelined structures, concurrent, minimal resource utilization and minimized sensitivity to truncation errors. A digital filter which is compatible with simulation tool (software) Verilog HDL Quartus II and Matlab presented in preliminary results chapter 5.

Keywords – Digital IIR filter, FPGA, Verilog HDL, MATLAB, and Quartus II.

ABSTRAK

Digital penapisan algoritma adalah yang paling biasa dilaksanakan dengan menggunakan tujuan umum digital cip pemprosesan isyarat untuk aplikasi audio, atau tujuan digital cip penapisan khas dan litar bersepadu khusus aplikasi (ASIC) untuk kadar yang lebih tinggi. Berdasarkan kajian penapis digital yang mana Impulse Response Infinite (IIR) biasanya digunakan dalam kadar sampel yang lebih rendah, dan kurang daripada 200 kHz (2009) [2]. Penapis ini digunakan dalam pelbagai kadar sampel dan disokong dari segi alat, perisian, dan teras IP. Dalam kajian ini, infinite impulse response (IIR) dioptimumkan menggunakan field programmable gate arrays (FPGAs) dicadangkan. Kelebihan pendekatan FPGA untuk pelaksanaan penapis digital termasuk kadar sampel yang lebih tinggi daripada yang boleh didapati dari tradisional cip DSP, kos yang lebih rendah daripada satu ASIC untuk aplikasi jumlah yang sederhana, dan lebih fleksibel daripada pendekatan alternatif. FPGA memang telah banyak digunakan dalam sistem diprogramkan, konfigurasi peranti ini boleh diubah untuk melaksanakan fungsi yang berbeza jika diperlukan. Matlamat utama projek ini adalah untuk pemetaan graf aliran data (DFGs) daripada BiQuad bentuk langsung II. Menyedari Kaedah BiQuad telah distrukturkan dengan pemprosesan yang tinggi, dan frekuensi yang tinggi (Fmax), tempoh masa yang rendah (CPD), dan Latency yang rendah (L). Kaedah pengoptimuman adalah dicadangkan yang menyediakan bentuk struktur saluran maklumat, serentak, penggunaan sumber yang minimum dan sensitiviti dikurangkan kepada kesilapan pemangkasan. Satu penapis digital yang serasi dengan simulasi alat (perisian) Verilog HDL Quartus II dan Matlab dibentangkan dalam keputusan awal bab 5.

Kata Kunci – Penapis IIR , FPGA, Verilog HDL, MATLAB, dan Quartus II.