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Baseband Processor for IEEE 802.11a Standard with Embedded BIST

This paper is dedicated to dear friend of my familly Prof. K. Tröndle on the occasion of his retirement

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Abstract: In this paper results of an IEEE 802.11a compliant low-power baseband processor implementation are presented. The detailed structure of the baseband processor and its constituent blocks is given. A design for testability strategy based on Built-In Self-Test (BIST) is proposed. Finally, implementational results and power estimation are reported.

Keywords: IEEE 802.11a, Baseband processor, Low power, BIST.

1 Introduction

Fourth generation (4G) wireless and mobile systems are today very attractive for research and development. New types of services will be universally available to consumers and for industrial applications with the use of 4G devices. Broadband wireless networks will enable packet based high-speed data transfer suitable for video transmission and mobile Internet applications.

This paper is based on the outcomes of a project that aims to develop a wireless broadband communication system in the 5 GHz band, compliant with the IEEE 802.11a standard [1]. This standard specifies broadband communication systems using OFDM (Orthogonal Frequency Division Multiplexing) with data rates ranging from 6 - 54 Mbit/s. According to the standard, physical layer computational

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requirements can be achieved by adequate digital baseband processing. A practical implementation of the IEEE 802.11a compliant baseband processor can be done in several ways. In general, software based baseband processing can be done using either a multiprocessor system or a single DSP processor with a number of hardware accelerators. The standard defines very intensive computational activities, and possible software solutions lead to increased power dissipation.

Therefore, we have decided to use a dedicated ASIC (Application Specific Integrated Circuit) for baseband processing. The processing algorithm defined by the standard corresponds to a datapath architecture of transmitter and receiver. To decentralize some timing critical control functions a token-flow approach was adopted [2]. Every block in the baseband processor has an input signal, which indicates that valid data is ready for processing. A similar signal is generated by every block upon output, to indicate that the subsequent block can process data. The token-flow approach can easily be expanded with clock gating. In this way an efficient power saving mechanism is implemented.

In the following sections, first the architecture of the processor will be described. Then power saving mechanism of the baseband processor will be discussed, as well as the testing strategy. Finally, implementational results and some conclusions will be presented.

2 Architecture of the Baseband Processor

A block diagram of the Baseband processor is shown in Fig. 1. In order to achieve low power dissipation and to optimize silicon usage, the architecture is divided in two principle blocks: Transmitter and Receiver. According to this division, the baseband processing can provide two almost independent dataflow directions: transmit and receive.

The transmitter block consists of an input buffer, scrambler, signal field generator, encoder, interleaver, mapper, 64-point IFFT/FFT (Inverse Fast Fourier Transform / Fast Fourier Transform) and circuitry for pilot insertion (with pilot scrambler), guard interval insertion, and preamble insertion. The IFFT/FFT is a single block used in both, receive and transmit direction in order to optimize the baseband processor structure. On the other hand, this solution is more complex for implementation, because of incomplete decoupling between the transmitter and receiver datapath.

The standard [1] defines the procedure for the receiver and transmitter datapath processing. A fundamental issue, not tackled by the standard, is the mechanism of the synchronization and the channel estimation. The solution for this problem is one of the most important outcomes of our work. The synchronizer has to ful-

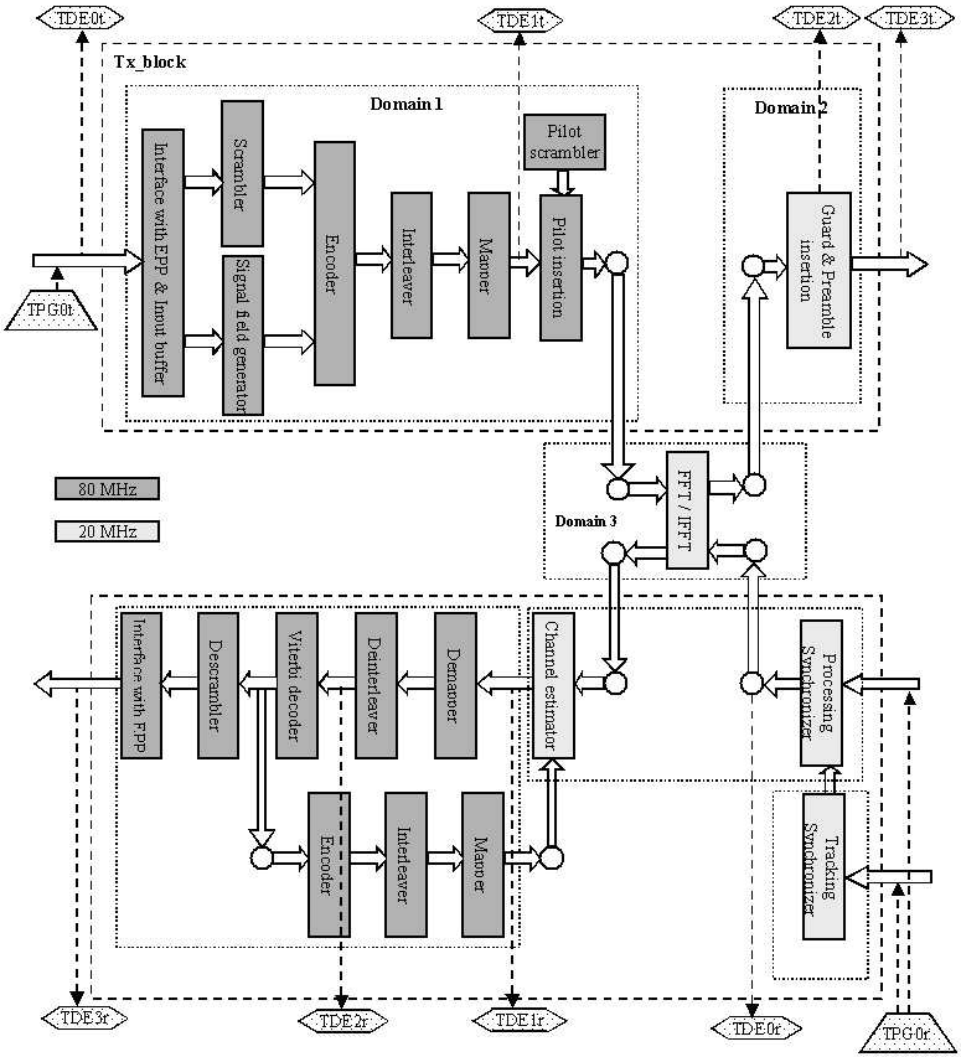

Fig. 1. Block diagram of the Baseband processor with embedded BIST.

fill the following operations: frame detection, carrier frequency offset estimation, symbol timing estimation, extraction of the reference channel and data reordering. A block scheme of the synchronizer is given in Fig. 3. In order to obtain a power efficient design, the synchronizer structure was split into two mutually exclusive paths: tracking data path and processing data path [3]. The main function of the tracking data path is to detect an incoming frame by searching for the periodic structure of the preamble symbols and to estimate the carrier frequency offset. In

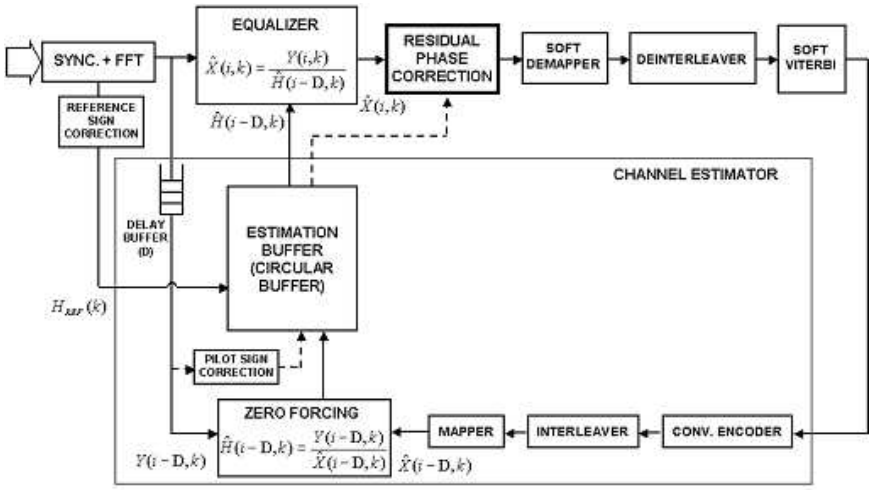

Fig. 2. Block diagram of the proposed Channel Estimator.

our design, a wide range of frequency offsets can be estimated ($\pm$80 ppm) using only two autocorrelators. The output of one of those is also used in the frame detection mechanism. This provides a significant core area reduction in comparison with other proposed solutions, as in [4]. Here, the range of estimated frequency offsets is $\pm$40 ppm and three autocorrelators are used for the frame detection, but only two of them for the frequency offset estimation. In our design, frame detection is performed by a plateau detector, which has to detect a specific plateau shape in the incoming preamble symbols. The activity of the processing datapath starts after the frame is detected and the estimated value for frequency offset is available.

This part of the synchronizer performs the carrier frequency error correction, estimates the symbol timing and obtains the reference channel estimation. It consists of an NCO (Numerically Controlled Oscillator, in this case a CORDIC processor operating in rotational mode), FFT processor and a simplified crosscorrelator based on XNOR gates [3].

Channel estimation is based on a decision-directed method [5] with simplified residual phase estimation and correction mechanism. This type of channel estimation is based on a feedback loop. Therefore our receiver involves additional encoding, interleaving and mapping (Fig. 2). The interesting point in this concept is that it makes use of a division unit to correct the data samples (equalizer). The estimator is designed in such a way that the samples of symbol i are used to calculate an estimation of the channel, which will be used to correct the symbol $i+D$, where D is the delay introduced by the feedback loop.

Other blocks on the receiving path, mainly defined by the standard, are demap-

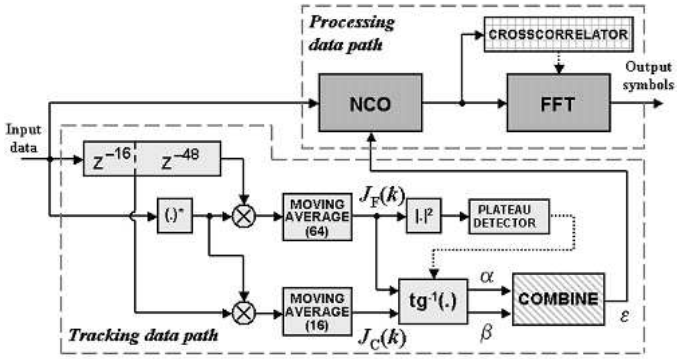

Fig. 3. General scheme of the Synchronizer.

per, deinterleaver, descrambler, Viterbi decoder, and additional buffers.

In order to simplify processing of the data and optimize power consumption to the maximal extent, the complete structure was divided into two clock domains. Computationally complex blocks without high data throughput requirements were designed for 20 MHz and high data throughput demanding circuits were designed for 80 MHz.

3 Power Saving Issues in the Baseband Processor

In order to avoid unnecessary waste of energy, clock gating is introduced as a power saving technique in the baseband processor. This circuit is divided into the transmitter (Tx) and the receiver (Rx) section, and accordingly, for the power saving purpose, blocks from Tx and Rx will not be in the same clock domain. The FFT/IFFT block is used both in the receiver and transmitter and it is defined as an independent clock domain. This block will be triggered whenever the transmitter is active. Additionally, this block will be used in the receiving phase when coarse synchronization is reached and data should be processed in the FFT. Our transmitter consists of two clock domains: one that assembles 80 MHz blocks and other for 20 MHz blocks. Clocks for this both blocks will be enabled only when the baseband processor is in transmit mode. In the receiver, the tracking synchronizer block is a stand-alone domain. This block will be active most of the processing time, because the baseband processor is always in receive mode, except for the time when it transmits. Also, in receive mode for most of the time the baseband processor will search for coarse synchronization. With this domain separation we can save a significant amount of energy. Other domains in the receiver are 20 MHz domains for synchronizer and channel estimator and 80 MHz domain for blocks as Viterbi decoder and deinterleaver. Those blocks will be activated only when coarse synchronization is

reached and there is data to be processed. After processing all data from one frame, the processing domains will be deactivated and the tracking synchronizer will again start toggling.

4 Baseband chip design for testability

The baseband processor has very complex datapath architecture. In order to guarantee reliable operation it is necessary to provide a certain level of testability. A standard procedure in the synchronous world is to apply scan- based testing. In the case of the baseband processor we have decided not to use that approach. Scan testing could decrease performances of our system, and requires expensive hardware testers. Additionally, for datapath architectures Built-in Self-Test (BIST) could be designed in such way, that it tests most of the system functionality with very low cost in additional hardware and decreased performance.

It would be ideal if we could just in one run, perform testing of the complete baseband processor. Unfortunately, this baseband processor implementation does not allow that. The critical part is FFT/IFFT, which is a single block and can be either in transmit or receive mode and not both in the same time. All other parts in receiving and transmitting datapath are completely decoupled.

For that reason, we decided to create two separate BIST paths (domains). One is for testing the receiver and the other for testing the transmitter. In both cases we have designed Test Pattern Generators (TPG). Generally, a TPG consists of a Linear Feedback Shift Register (LFSR). In the receiver direction, to activate deeper pipeline stages, it was necessary to add to the TPG also a preamble and signal field generator. Otherwise our testing sequence would never go out from the synchronizer. In the transmitter stage TPG also has to include a starting sequence that enables transmission of data. In both BISTs, four Test Data Extractors (TDE) are implemented. A TDE is essentially also a LFSR. The idea behind that is to have more information about the results of testing. Generally, validity of the test is signaled with the TDEs at the output stages of transmitter and receiver. Additionally at three positions inside the transmitter and receiver datapath, additional TDEs are connected. They could provide information about some errors that could be masked in the following dataflow. Additionally, when the final TDE gives an erroneous result, we could isolate the errors and find erroneous blocks inside the receiver and transmitter. Only one-bit information is used for BIST test result collection. When the test is finished, pulses at the Bist_ok line should indicate validity of the internal test and the level of the final value will indicate correctness of the output data.

5 Implementation

The complete baseband processor was modeled in VHDL and synthesized using our in-house 0.25 μm standard cell library. It's drawing cell area, including all blocks from Fig. 1, is 32,85 mm^2 (equivalent transistor count is around 1 Million). In Table 1 some synthesis results for our technology are given, where $Tx\_^*$ indicates transmitter components and $Rx\_^*$ stands for receiver components. From Table 1 it can be noticed that the dominant hardware part is the receiver. It uses 67.6% of the chip cell area. Generally, the most silicon consuming components are synchronizer, channel estimator, Viterbi decoder and FFT/IFFT. Based on the result of the synthesis, the layout of the baseband chip is performed. According to after-layout power estimation with Synopsys Prime Power [6], the expected power consumption is 393 mW for the scenario of a real transceiver application. This application consists of the reception of 43 bytes and subsequent transmission of the standard acknowledge of 14 bytes. From this point of view most of the power is spent in the Viterbi processor (13.5%), FFT/IFFT (10.4%) and Transmitter in general (13%). One could observe that the total power spent in receiver is around 63.3 %. Remaining power is utilized by the clock tree, which impact is analyzed separately.

Table 1. Baseband processor synthesis results

Hardware part		Cell area (mm^2)	Cell area (%)	Power (mW)	Power (%)
Tx		**3.064**	**9.3**	**63**	**16**
	Interleaver	0.501	1.5	13	3.3
	Pilot_insert	0.820	2.5	31	7.9
	Guard_insert	1.011	3.1	4	1
	Inputbuffer	0.201	0.6	1	0.2
	Tx_BIST	0.130	0.4	1	0.2
Rx		**22.201**	**67.6**	**145**	**36.9**
	Synchronizer	6.183	18.8	25	6.4
	Chanel_est.	5.297	16.1	15	3.8
	Viterbi_dec	5.910	18.0	53	13.5
	CE_buffer	1.446	4.4	13	3.3
	Deinterleaver	1.786	5.4	21	5.3
	Demapper	0.422	1.3	1	0.2
	Interleaver	0.630	1.9	7	1.8
	Rx_BIST	0.247	0.8	1	0.2
FFT/IFFT		**7.556**	**32.0**	**41**	**10.4**
Total		**32.851**	**100**	**393**	**100**

Die photo of the produced Baseband chip is given in Fig. 4. After layout, the silicon area for this design is 34 mm^2, including pads. The number of pins is 124.

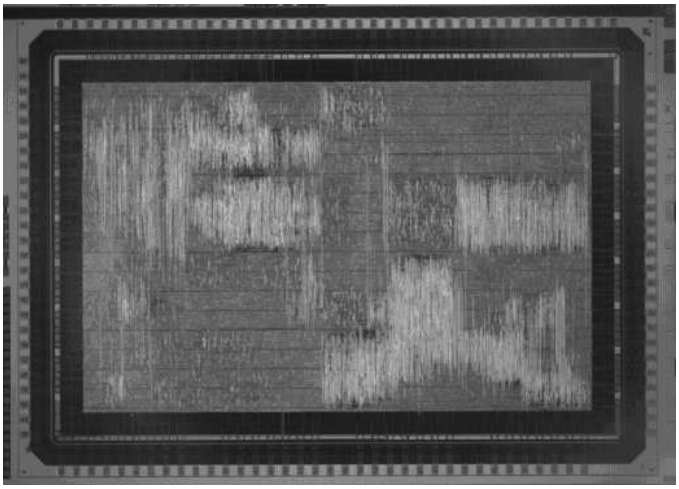

Fig. 4. Die photo of the Baseband chip.

6 Conclusions

This paper summarizes some research results from our Wireless Broadband Networks project over the last five years. The implementation of the Baseband processor compliant with the IEEE 802.11a standard was a major task. In order to fulfill it, several innovative techniques were applied. In this paper the final structure of the designed Baseband processor chip is described. The general scheme is explained and synthesis and layout results are presented. The circuitry, described here, is fabricated in IHP in-house 0.25 μm CMOS technology.

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