Research Article

Processing Chip for Thin Film Bulk Acoustic Resonator Mass Sensor

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Aimed at portable application, a new integrated process chip for thin film bulk acoustic resonator (FBAR) mass sensor is proposed and verified with 0.18 um CMOS processing in this paper. The longitudinal mode FBAR with back-etched structure is fabricated, which has resonant frequency 1.878 GHz and Q factor 1200. The FBAR oscillator, based on the current-reuse structure, is designed with Modified Butterworth Van Dyke (MBVD) model. The result shows that the FBAR oscillator operates at 1.878 GHz with a phase noise of -107 dBc/Hz and -135 dBc/Hz at 10 KHz and 100 KHz frequency offset, respectively. The whole process chip size with pads is $1300\,\mu$m $\times$ $950\,\mu$m. The FBAR and process chip are bonded together to sense tiny mass. The measurement results show that this chip precision is 1 KHz with the FBAR frequency gap from 25 kHz to 25 MHz.

1. Introduction

In recent years, mass sensor based on FBAR technology has a rapid development due to its high mass sensitivity and integrated potential [1]. FBAR mass sensor is considered as an excellent portable healthcare sensor resolution [2, 3]. Recent researches mainly focus on relative humidity sensor [4], glycerol detector [5], gravimetric sensing [6], ultraviolet sensor [7], DNA and protein detection [8], microfluidic system [9], and so on. However, by now FBAR mass sensors are handled with network analyzer and RF probe station, which is massive and various with testing environment. It is not fit to portable application. There is no paper to report FBAR sensor signal processing chip and its FBAR oscillator. In this paper, we presented an integrated chip, which can be connected with FBAR to process its RF sensor signal and show mass change value directly.

2. FBAR Sensor Design

2.1. System Scheme. FBAR structure is shown in Figure 1. It consists of an AlN thin piezoelectric film sandwiched by two Al metal electrodes with back-etched structure and an adsorption layer which is used to adsorb a particular material

for sensor. The adsorption layer should be selected according to the different detected target materials. The resonant frequency will change due to the change of mass of the target material. Conversion between frequency change and the mass loading is described by the Sauerbrey equation [10]:

$$\Delta f_s = -2\Delta m \cdot f_s^2 A^{-1} \mu_q^{-1/2} \rho_q^{-1/2}, \tag{1}$$

in which Δf_s is the frequency change, f_s is the fundamental resonant frequency, Δm is the mass change, A is the active area, ρ_q is the density, and μ_q is the shear modulus.

The sensor process system should be designed to obtain FBAR resonant frequency changes due to tiny mass. Usually, the system is based on dual-path structure, shown in Figure 2, one path for sensor signal and the other for reference signal to deembed testing environment effects change, such as pressure, temperature, and humidity, due to the two paths that are neighbor in one chip. Because the signals of FBAR are always weak, an oscillator network is designed to active FBAR signals to obtain 3 V output to drive the following processing circuit. The FBAR resonant frequency is usual about 2-3 GHz. It is too high to be processed with normal high speed counter. Mixture frequency approach is also not fit to FBAR sensor owing it IP3 and complex
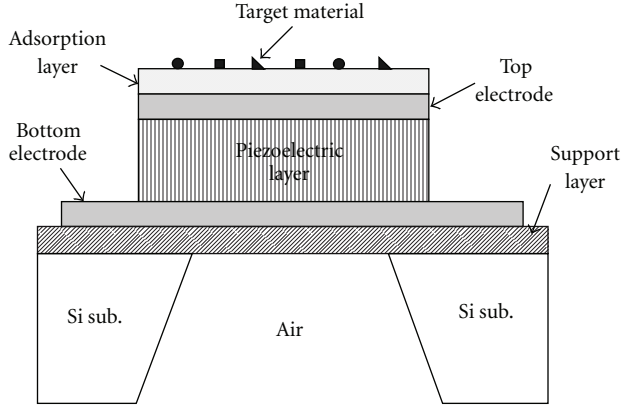
FIGURE 1: Cross-section structure of FBAR.

structure. The designed new chip employs two divide-by-256 dividers to lower FBAR resonant frequencies to about 10 MHz, then it counted them by two high speed counters. The frequency difference is obtained by the subtractor. According to this counting difference, the change of mass load can be obtained from the following calculation:

$$\Delta m \approx -\frac{M}{f_s} \cdot \Delta f = -\frac{M \cdot N}{f_s \cdot T} \cdot S, \qquad (2)$$

where M is the quality of the work area of FBAR piezoelectric, N is the division ratio of divider, T is the counting cycle of counter, and S is the frequency counting difference. The whole chip schematic also includes self-calibration and UART interface.

2.2. FBAR and Its Oscillator. Back-etched structure is used to manufacture FBAR, because it is relatively easy to fabricate and has better performance compared to solid-mounted structure (SMR). Figure 3(a) is the top view of the FBAR, and the measured S parameter is shown in Figure 3(b). It shows that the measured Q factor of FBAR is above 1200, and the resonant frequency is 1.878 GHz. The FBAR oscillator is composed of a FBAR, a pair of NMOS and PMOS, and some resistors and capacitors to form the current-reuse structure, in which the negative conductance is supplied by the pair of MOS transistors, as shown in Figure 4. Compared to the traditional cross-couple structure, this configuration consumes less power since the pair of NMOS and PMOS switches simultaneously, while the pair of NMOSs or PMOSs in the conventional structure converts alternately. FBAR oscillators designed and fabricated with 0.18 μm RF/mixed-signal CMOS process and the MBVD model are employed [11]. The simulation result of phase noise of the FBAR oscillator is shown in Figure 5, and the result shows that the oscillator operates at 1.878 GHz with a phase noise of −107 dBc/Hz and −135 dBc/Hz at 10 KHz and 100 KHz frequency offset, respectively.

2.3. Sensor Signal Processing Circuit. According to the operation of FBAR oscillators, we get the output frequency between 1.5 GHz and 2.0 GHz. In order to meet the digital

signal processing requirements, two divide-by-256 dividers are designed to reduce the frequencies down to 10 MHz. Owing to the high frequency, the front-end of dividers should adopt high speed circuits. Hence, signal-coupled logic (SCL) structure which is the evolution of emitter-coupled logic (ECL) is used due to its high speed, low power, and low noise [12]. The divide-by-256 divider consists of a single-ended to differential converter, three cascaded divide-by-2 SCL dividers, and five cascaded divide-by-2 D-flip-flop (DFF) dividers. The reason why it does not implement with all SCL dividers is that the layout area of SCL is larger than DFF structure. The main structure of SCL divider is master-slaver D flip-flop consisting of two D-latches. Figures 6(a) and 6(b) show the block diagram of the divide-by-2 SCL divider and the circuit schematic of the D-latch, respectively. M1 and M4 constitute the sampling circuit, and the cross-coupled pair M2 and M3 constitutes the holding circuit. When the clock signal (CK) is at high state, D-Latch works like a buffer; when the clock signal is low, the cross-coupled pair holds the existing state through positive feedback principle. Additionally, five stages of divide-by-2 DFF divider are implemented based on the traditional master-slaver structure.

The signal after divide-by-256 will be sent into standard digital signal processing circuit. In this paper, 40 MHz temperature compensate X'tal (crystal) oscillator (TCXO) is used as the high precision clock due to its high frequency stability, wide frequency range, and high frequency accuracy. Taking into account the power consumption, the sampling period of this system is set to 500 ms, and the counting period is set to 256 ms. The word length of the count difference is 24 bits. Figure 7 gives the top block diagram of the digital processing circuit generated by Verdi. It consists of timing module, counter module, subtracter module, encoding module, UART clock module, and sending module.

3. Measurement Results

The whole FBAR signal processing circuit is verified in 0.18 μm RF/mixed-signal CMOS process, and the dimension of the chip with pads is 1300 μm × 950 μm. Figure 8 shows the chip micrograph. The chip is banded with FBAR by gold wire, and the whole sensor system is tested. The measurement results are listed in Table 1, where the frequency difference ranges from 25 kHz–25 MHz. This tiny mass sensor signal processing circuit has high accuracy, but sometimes there is an accidental error of ±1000 Hz, which is related to the synchronization of high speed counter trigger. For example, when the signal frequency difference is 100 kHz, the measured difference is 100 kHz in most case, but sometimes it is 99 kHz or 101 kHz.

4. Conclusion

An integrated tiny mass sensor based on FBAR and CMOS technology is proposed and verified in this paper. The system of FBAR sensor is designed with dual-path structure. One path is used for sensor signal, and the other for reference signal to diminish the effect of environment change. FBAR
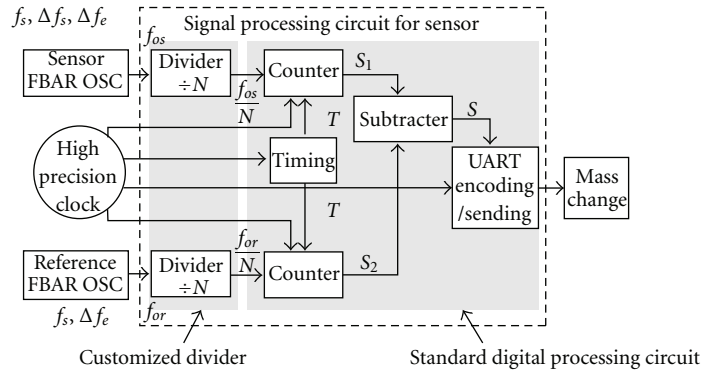
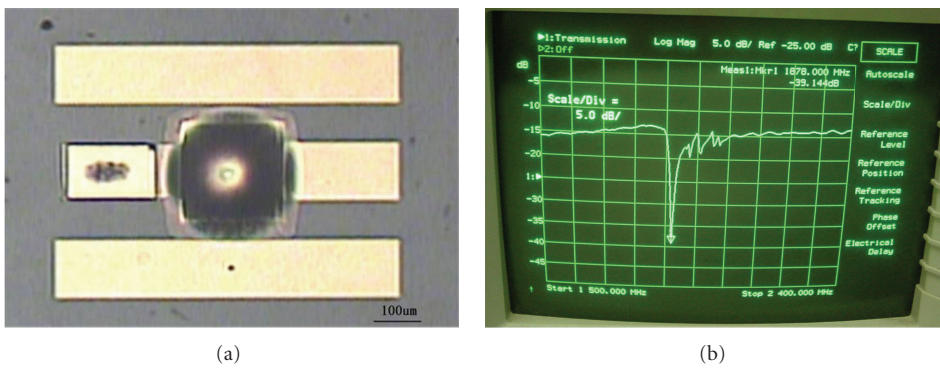FIGURE 2: Scheme of FBAR tiny sensor.

(a)   (b)

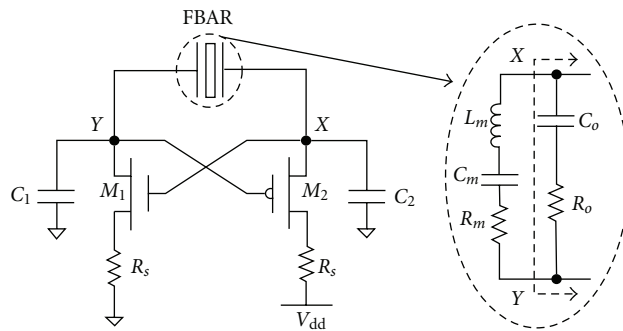FIGURE 3: (a) Chip photo of the fabricated FBAR, (b) measured resonant frequency of FBAR.

FIGURE 4: Schematic of the FBAR oscillator and equivalent circuit of FBAR.
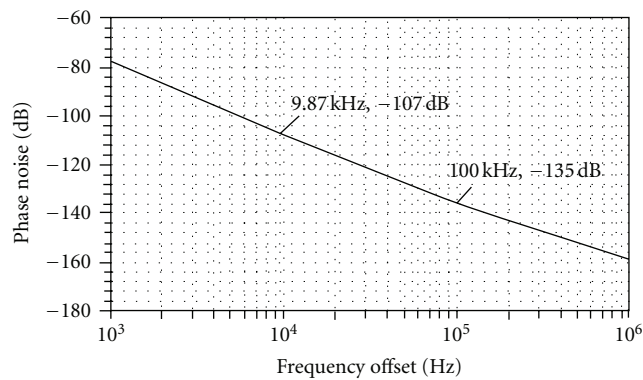

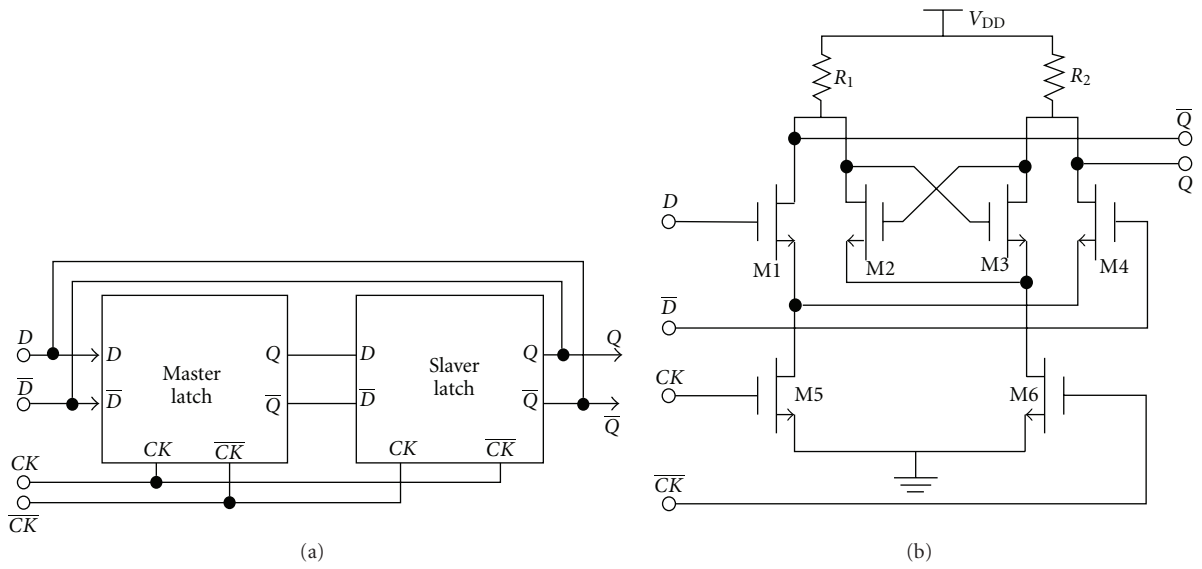FIGURE 5: Phase noise of the FBAR oscillator from postlayout simulation.

(a)

(b)

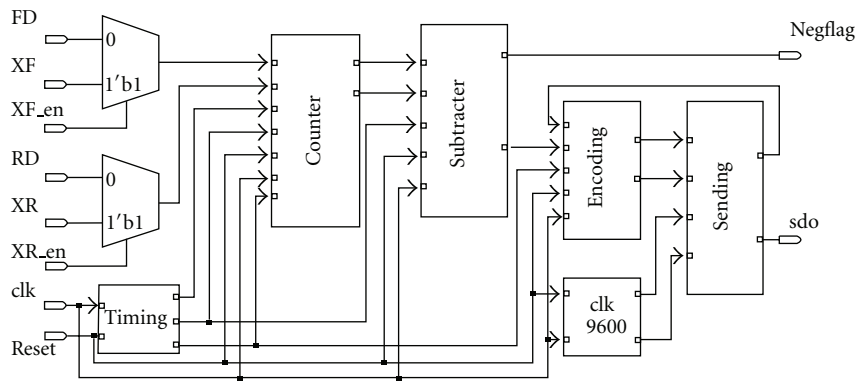FIGURE 6: (a) Block diagram of divide-by-2 SCL divider, (b) circuit schematic of D-latch.

FIGURE 7: Block diagram of the digital processing circuit generated by Verdi.
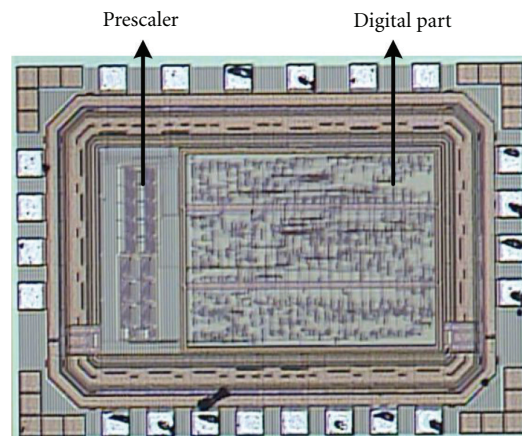

FIGURE 8: Chip micrograph.

TABLE 1: Measurement results of sensor signal processing circuit.

Reference signal/Hz	Sensor signal/Hz	Measured difference/Hz	Accidental error/Hz
1 899 000 000	1 898 975 000	25 000	±1 000
1 899 000 000	1 898 900 000	100 000	±1 000
1 899 000 000	1 889 000 000	10 000 000	±1 000
1 899 000 000	1 874 000 000	25 000 000	±1 000

operates in longitudinal mode, and its resonant frequency is 1.878 GHz with Q factor above 1200. Two FBAR signals are activated by oscillators based on current-reuse differential configuration to promote their output signals. Subsequently, these two FBAR oscillator signals are divided by 256 and then sent to digital signal processing circuit to obtain the frequency difference. Finally, this frequency offset is used to evaluate the tiny mass loading change. The whole FBAR signal processing circuit is verified in 0.18 μm RF/mixed-signal CMOS process.

Acknowledgment

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