

Research Article

Space Vector Modulation Technique for 3-Level NPC Converter with Constant Switching Frequency

Imen Ouerdani,¹ Hamed Ben Abdelghani,¹ Afef Bennani Ben Abdelghani,^{1,2} Daniel Montesinos-Miracle,³ and Ilhem Slama-Belkhodja¹

¹*Ecole Nationale d'Ingénieurs de Tunis, LRIIES15 Laboratoire de Systèmes Electriques, Université de Tunis El Manar, 1002 Tunis, Tunisia*

²*Institut National des Sciences Appliquées et de Technologie (INSAT), Université Tunis Carthage, Centre Urbain Nord, BP 676, 1080 Tunis, Tunisia*

³*Centre d'Innovació Tecnològica en Convertidors Estàtics i Accionaments (CITCEA-UPC), Departament d'Enginyeria Elèctrica, Universitat Politècnica de Catalunya, ETS d'Enginyeria Industrial de Barcelona, Avenida Diagonal 647, Pl. 2, 08028 Barcelona, Spain*

Correspondence should be addressed to Imen Ouerdani; imen.wardani@gmail.com

Received 23 April 2016; Accepted 25 May 2016

Academic Editor: Francesco Profumo

Copyright © 2016 Imen Ouerdani et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

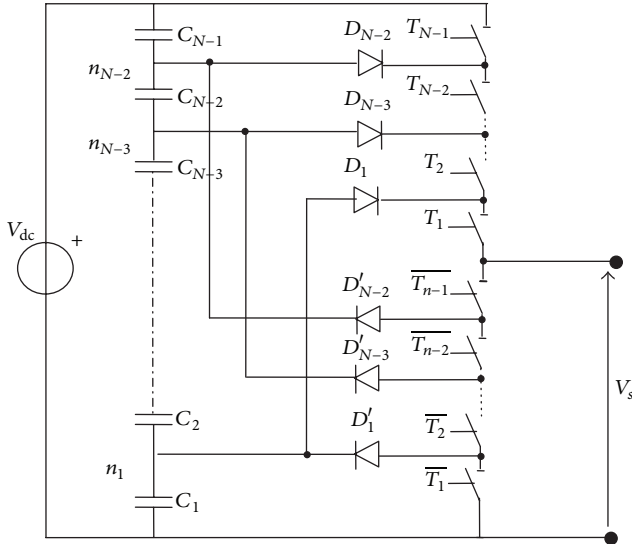
This paper presents a simple Space Vector Modulation (SVM) methodology for a three-level NPC converter. Nearest three vectors (NTV) and corresponding duty cycles are deduced through simple generic mathematical expressions. Extra degrees of freedom of NPC converter are used to fully benefit from SVM advantages and to control the switching frequency. Simulation and experimental results are presented and discussed to validate the proposed methodology.

1. Introduction

Power conversion investigation attracted attention particularly in Medium Voltage/High Power ranges [1, 2]. During the three last decades, advancements in power electronics fields have led to innovative converter topologies, called multilevel converters [3, 4]. In fact, compared to classical two-level converters, multilevel converters are an attractive solution since they support higher operation voltages, reduce common mode voltages, minimize output current and voltage distortions, and optimize output filter size and cost. One of the most widely used and investigated multilevel topologies is the neutral point clamped converter. This topology was firstly introduced by Richard Baker in the early eighties [5]. Later on, several converters based on the NPC were proposed such as the Active NPC [6–9] and the Optimized NPC [10–12]. These converters are classified as the Diode Clamped Converters [13]. The three-phase N -level NPC converter uses $(N - 1)$ series-connected capacitors to divide the DC bus into a set of intermediary voltage levels as presented in Figure 1.

Simultaneously, classical modulation algorithms proposed for two-level converters such as Pulse Width Modulation (PWM) [14], hysteresis current control [15], and selective harmonic elimination [16] have been extended to multilevel topologies. Among the proposed algorithms, the Space Vector Modulation (SVM) is the most widely used due to its better utilization of the DC bus [9] and higher harmonic performances in linear and nonlinear operating zones [17, 18] compared to conventional PWM strategies. Detecting the nearest three vectors (NTV) among the numerous available ones, selecting and fully defining the corresponding switches duty cycles with respect to possible additional criteria are the main issues of SVM technique in multilevel converter context.

In this paper, a simple approach for a 3-level Space Vector Modulation technique available for the NPC converter is presented. In the proposed method, the nearest three vectors and their corresponding on-times application are simply expressed using generic mathematical expressions. The choice of the Phase Level Sequence (PLS) is used as

FIGURE 1: N -level neutral point clamped inverter leg.

an extra degree of freedom in order to control the switching frequency. Simulation and experimental results are presented to verify the effectiveness of the proposed SVM strategy.

2. NPC Converter and Space Vector Modulation (SVM)

2.1. Neutral Point Clamped Converter. One phase of an n -level neutral point clamped inverter consists of $(n - 1)$ capacitors, $6 \times (n - 1)$ power switches, and $6 \times (n - 2)$ clamping diodes and is able to generate $(n - 2)$ capacitive midpoints. The output voltage V_s is equal to the voltage of the capacitive midpoint connected to it. Hence, V_s can take $(n - 2)$ values as

$$\frac{V_{dc}}{n-1}, \frac{2V_{dc}}{n-1} \dots \frac{j \cdot V_{dc}}{n-1} \dots \frac{(n-2)V_{dc}}{n-1}. \quad (1)$$

In order to generate the output voltage V_s , the IGBTs T_1 to T_k and $\overline{T_{k+1}}$ to $\overline{T_{n-1}}$ must be ON. The current is then flowing from the diodes D_k through the switches T_1 to T_k to the output V_s . It is to note that any other configuration is not permitted and each voltage level is realized by an only one configuration [19, 20]. In this paper, the triplet (X, Y, Z) , called Phase Level Sequence (PLS), is introduced for a three-phase multilevel neutral point clamped inverters, where X (Y and Z , resp.) is the phase level of phase a (phase b and phase c, resp.). Three-phase n -level NPC converters are able to generate n^3 PLS and $(3n(n-1) + 1)$ space vectors.

Hence, 3-phase 3-level NPC converter presented in Figure 2 is able to generate 27 PLS and 19 space vectors.

For a single phase, phase level is equal to 0 when both commutation cells are OFF-switched and is equal to 2 when both commutation cells are ON-switched. The corresponding output voltage for phase level 0 is $-V_{dc}/2$ whereas the corresponding output voltage for phase level 2 is equal to $V_{dc}/2$. Intermediate level is equal to 1 and is obtained when

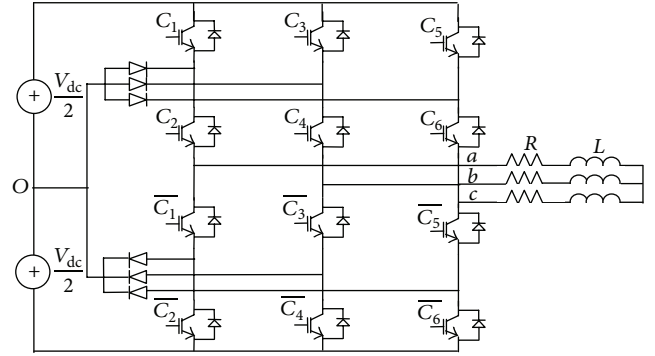


FIGURE 2: Three-phase 3-level NPC converter.

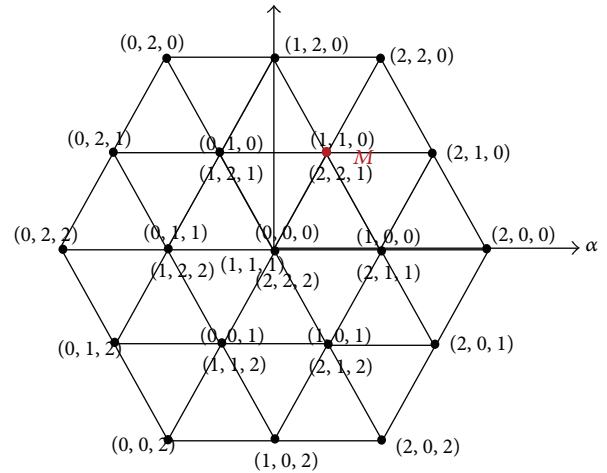


FIGURE 3: Three-level inverter space vector diagram.

only one commutation cell is ON-switched, in which case the output voltage is equal to 0.

Figure 3 shows the (α, β) frame of a 3-phase NPC 3-level converter.

2.2. Space Vector Modulation (SVM). For a three-phase two-level converter, the aim of the Space Vector Modulation is to select the appropriate space vectors to apply and their respective application times [21, 22]. Given a voltage reference vector V_s^* , the SVM strategy selects the two nearest active vectors (V_k and V_{k+1}) and the zero vectors $(0, 0, 0)$ and $(1, 1, 1)$ as shown in Figure 4(a). The application times for these 4 vectors are calculated using the volt-second balance as

$$\begin{aligned} T_{k+1}V_{k+1} + T_kV_k + (T_{SVM} - (T_{k+1} + T_k)) \cdot V_0 \\ = T_{SVM} \cdot V_s^*, \end{aligned} \quad (2)$$

where V_k , V_{k+1} , and V_0 are space vectors, T_k and T_{k+1} are the application times corresponding to V_k and V_{k+1} , respectively, and T_{SVM} is the SVM period. $T_{SVM} - (T_{k+1} + T_k)$ is the application time of zero voltages: during the first half of this time slot $(0, 0, 0)$ is applied and during the second half $(1, 1, 1)$ is applied if symmetrical SVPWM technique is used.

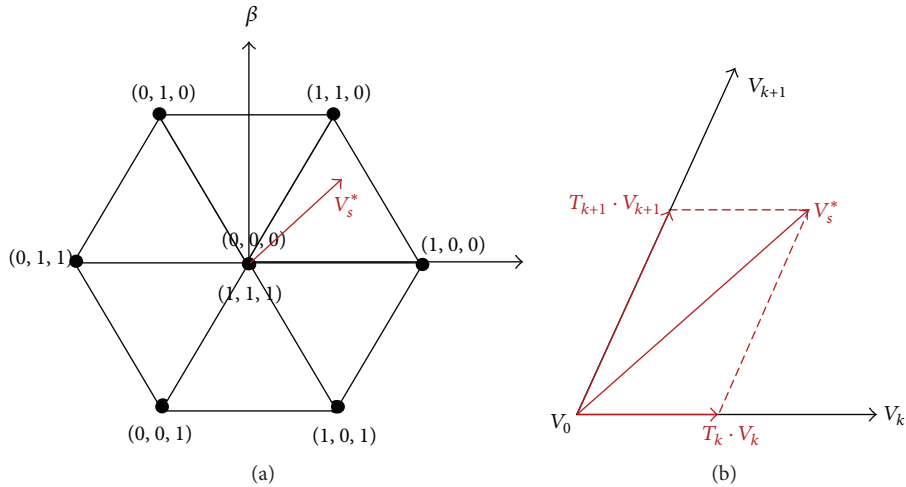


FIGURE 4: (a) Two-level inverter space vector diagram; (b) SVM for a two-level inverter.

Compared to conventional PWM strategies, the Space Vector Modulation leads to better dynamic performances and a higher modulation index even if the calculation complexity is comparatively increased.

For an n -level converter, the increased number of space vectors and switching states further enhances the dynamic performances but needs additional calculation capabilities and introduces considerable implementation complexity.

In this paper, a simple approach to implement a three-level SVM algorithm using mathematical analysis of the obtained (α, β) frame is proposed. Active vectors to be applied, switching states, and IGBT on-times calculation are easily deduced using the proposed method.

3. Proposed Algorithm

Figure 5 shows the block diagram of the proposed method, where the main task of each step is written in bold and criterion for each task is written in *italic* in the neighboring box.

3.1. Step 1: Localization of V_s^* . The aim of V_s^* Localization block is to identify the appropriate three vectors V_i , $i = 1, 2, 3$, to apply and consequently their corresponding PLS in order to generate an output voltage with a mean value on the switching period equal to the reference voltage. The space vectors needed for the SVM are the nearest three vectors to V_s^* .

In order to localize the reference voltage vector, its module and phase, noted, respectively, as $\|V_s^*\|$ and θ_s , are used. They are calculated using basic $(abc-\alpha\beta)$ transformation.

The (α, β) frame is divided into 6 sectors and 4 quadrants according to Figure 6. This sectorization represents the first step to deduce to which triangle (among the available 24 ones) the reference voltage vector belongs. Once this triangle selected, a lookup table gives the three nearest voltage vectors the inverter must generate.

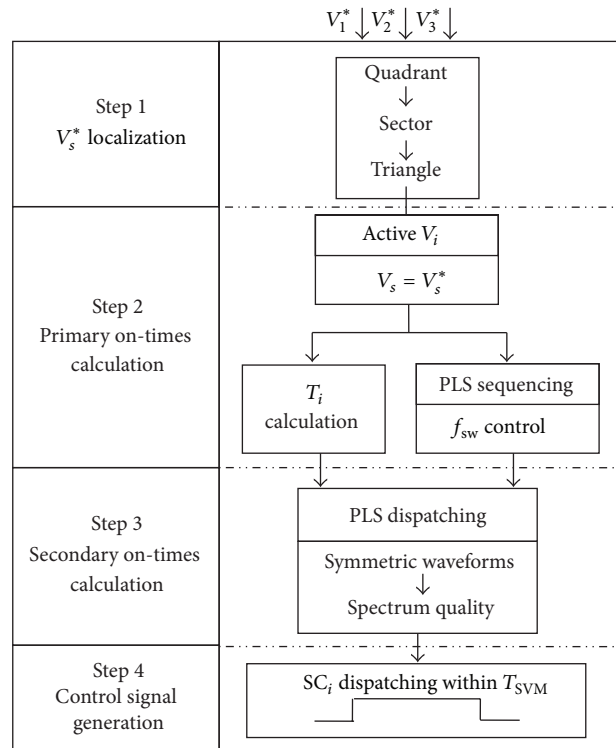


FIGURE 5: Block diagram of the proposed scheme.

Depending on the modulation depth m , specific triangles are used: if $0 < m < 0.75$, space vector V_s crosses triangles T1, T5, T9, T13, T17, and T21 and if $0.75 < m < 1.15$, the remaining triangles (T2, T3, T4, T6, T7, T8, T10, T11, T12, T14, T15, T16, T18, T19, T20, T22, T23, and T24) are used. It is to be noted that the modulation index $m = \|V_s^*\|/V_{dc}$ and the maximum modulation index $m = 1.15$ is obtained when $\|V_s^*\| = V_{dc}/\sqrt{3}$.

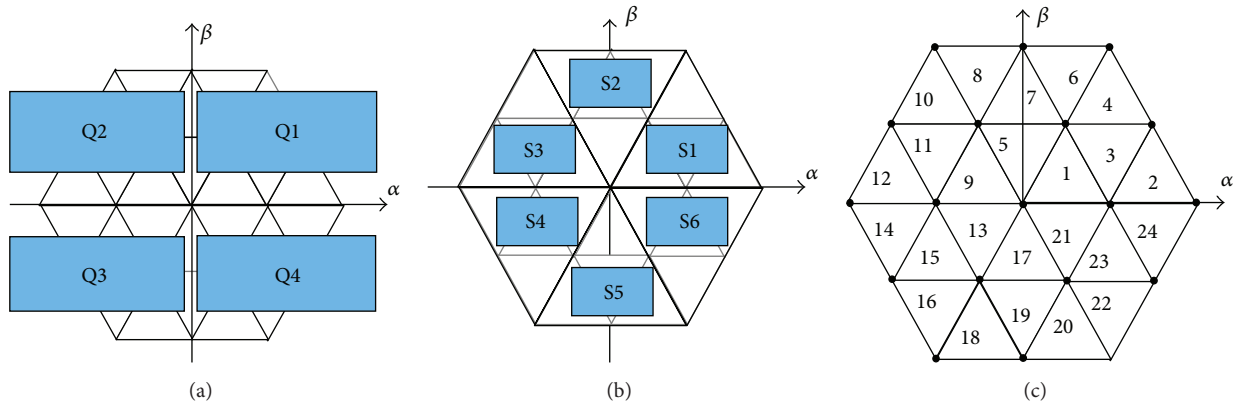


FIGURE 6: (α, β) frame sectorization: (a) 4 quadrants; (b) 6 sectors; (c) 24 triangles.

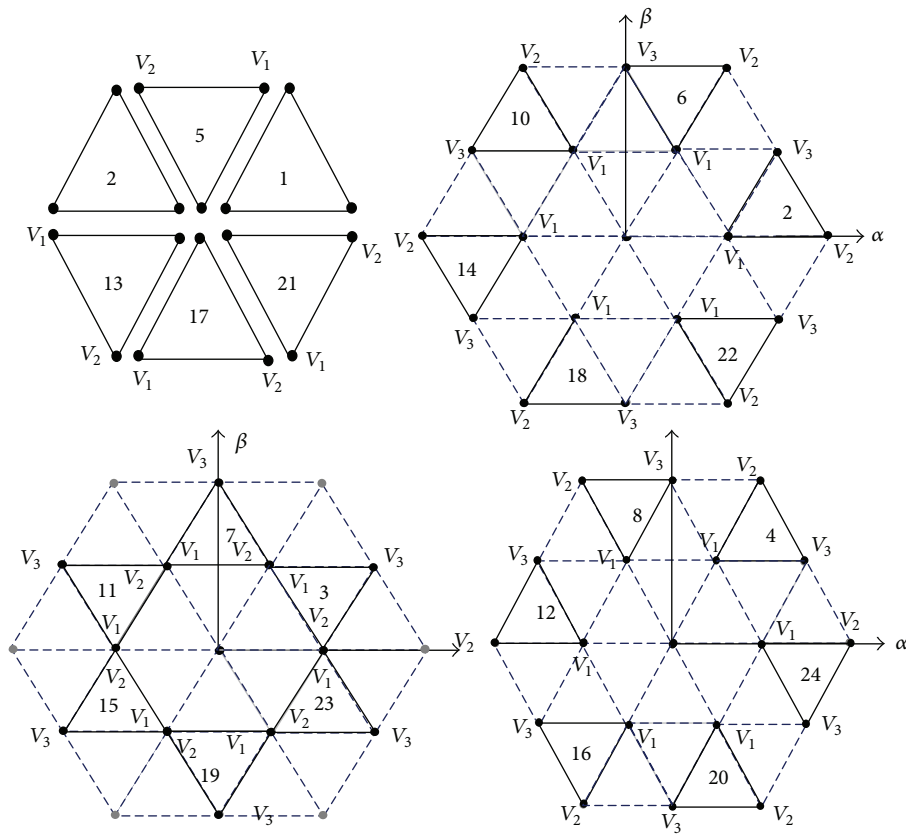


FIGURE 7: Triangles division into 4 families.

3.2. Step 2: Primary ON-Times Calculation. The “Primary ON-Times Calculation” block aims to determine the on-time for each of the three vectors V_i , $i = 1, 2, 3$, that is, the activation time over switching period T_{SVM} . Step 2 outputs are as follows:

- (i) The corresponding on-time T_i , $i = 1, \dots, 3$, for the three needed vectors the converter has to perform on the next T_{SVM} .

These vectors V_i , $i = 1, \dots, 3$, correspond to the localized triangle’s vertices.

- (ii) The PLS leading to the specified space vectors. The PLS choice affects the converter switching frequency.

To perform a rigorous on-times calculation, fine modeling of the three-level converter voltage vectors is needed. The proposed algorithm divides the 24 triangles among 4 families given by Figure 7. In fact, the 3 vectors of all the triangles belonging to the same family can be expressed using a unique generic form. Thus, on times are deduced as generic forms depending on the selected family.

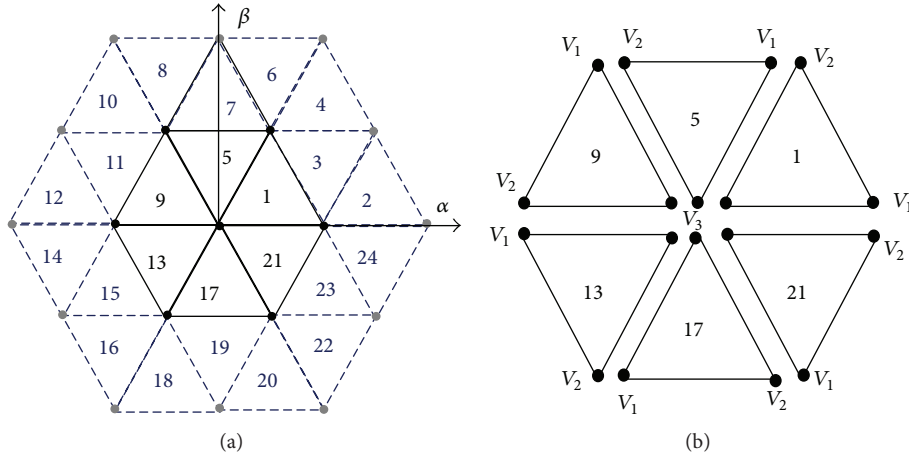


FIGURE 8: Family 1: (a) triangles; (b) zoom on family 1 space vectors.

3.2.1. V_i Generic Expressions. Family 1 is formed by triangles 1, 5, 9, 13, 17, and 21 as shown in Figure 8. V_1 , V_2 , and V_3 are represented for each triangle belonging to this family and their expressions are

$$V_1 = \frac{V_{dc}}{3} e^{j(k-1)(\pi/3)} = \frac{V_{dc}}{3} \begin{pmatrix} \cos(k-1) \frac{\pi}{3} \\ \sin(k-1) \frac{\pi}{3} \end{pmatrix},$$

$$V_2 = \frac{V_{dc}}{3} e^{j(k)(\pi/3)} = \frac{V_{dc}}{3} \begin{pmatrix} \cos\left(k \frac{\pi}{3}\right) \\ \sin\left(k \frac{\pi}{3}\right) \end{pmatrix}, \quad (3)$$

$$V_3 = 0,$$

where k is the sector's index corresponding to each triangle.

Family 2 is formed by triangles 2, 6, 10, 14, 18, and 22, as shown in Figure 9.

V_1 , V_2 , and V_3 corresponding to this family are given by

$$V_1 = \frac{V_{dc}}{3} e^{j(k-1)(\pi/3)} = \frac{V_{dc}}{3} \begin{pmatrix} \cos(k-1) \frac{\pi}{3} \\ \sin(k-1) \frac{\pi}{3} \end{pmatrix},$$

$$V_2 = \frac{2V_{dc}}{3} e^{j(k-1)(\pi/3)} = \frac{2V_{dc}}{3} \begin{pmatrix} \cos(k-1) \frac{\pi}{3} \\ \sin(k-1) \frac{\pi}{3} \end{pmatrix}, \quad (4)$$

$$V_3 = \frac{V_{dc}}{\sqrt{3}} e^{j(k-0.5)(\pi/3)} = \frac{V_{dc}}{\sqrt{3}} \begin{pmatrix} \cos(k-0.5) \frac{\pi}{3} \\ \sin(k-0.5) \frac{\pi}{3} \end{pmatrix}.$$

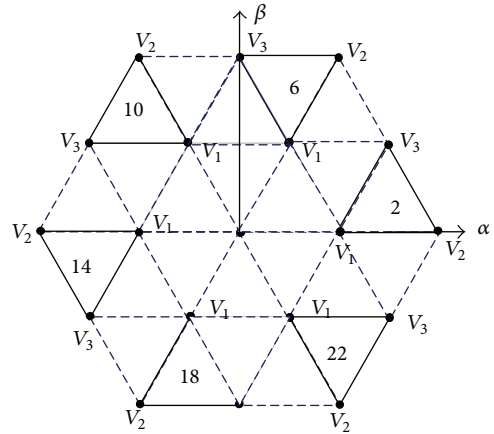


FIGURE 9: Family 2 space vectors.

Family 3 is formed by triangles 3, 7, 11, 15, 19, and 23 as shown in Figure 10, and associated space vectors are given by

$$V_1 = \frac{V_{dc}}{3} e^{j(k-1)(\pi/3)} = \frac{V_{dc}}{3} \begin{pmatrix} \cos(k-1) \frac{\pi}{3} \\ \sin(k-1) \frac{\pi}{3} \end{pmatrix},$$

$$V_2 = \frac{V_{dc}}{3} e^{j(k)(\pi/3)} = \frac{V_{dc}}{3} \begin{pmatrix} \cos\left(k \frac{\pi}{3}\right) \\ \sin\left(k \frac{\pi}{3}\right) \end{pmatrix}, \quad (5)$$

$$V_3 = \frac{V_{dc}}{\sqrt{3}} e^{j(k-0.5)(\pi/3)} = \frac{V_{dc}}{\sqrt{3}} \begin{pmatrix} \cos(k-0.5) \frac{\pi}{3} \\ \sin(k-0.5) \frac{\pi}{3} \end{pmatrix}.$$

The remaining triangles labeled 4, 8, 12, 16, 20, and 24 form family 4, as shown in Figure 11.

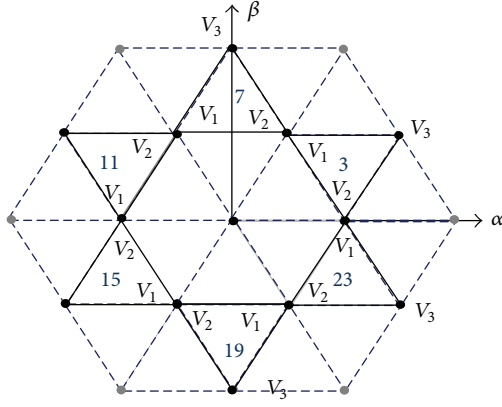


FIGURE 10: Family 3 space vectors.

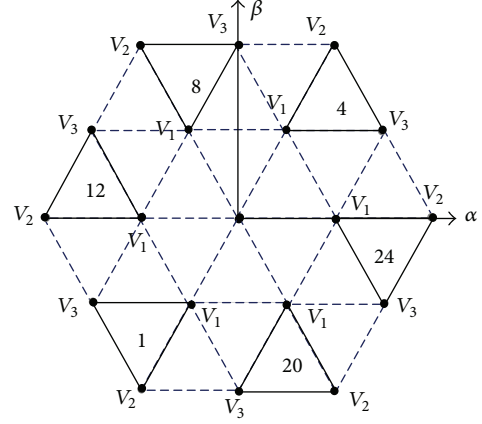


FIGURE 11: Family 4 space vectors.

Family 4 V_i expressions are

$$\begin{aligned} V_1 &= \frac{V_{dc}}{3} e^{jk(\pi/3)} = \frac{V_{dc}}{3} \begin{pmatrix} \cos k \frac{\pi}{3} \\ \sin k \frac{\pi}{3} \end{pmatrix}, \\ V_2 &= \frac{2V_{dc}}{3} e^{jk(\pi/3)} = \frac{2V_{dc}}{3} \begin{pmatrix} \cos k \frac{\pi}{3} \\ \sin k \frac{\pi}{3} \end{pmatrix}, \\ V_3 &= \frac{V_{dc}}{\sqrt{3}} e^{j(k-0.5)(\pi/3)} = \frac{V_{dc}}{\sqrt{3}} \begin{pmatrix} \cos(k-0.5) \frac{\pi}{3} \\ \sin(k-0.5) \frac{\pi}{3} \end{pmatrix}. \end{aligned} \quad (6)$$

3.2.2. T_i Calculation. T_i correspond to the application time of V_i , $i = 1, 2, 3$. They are the solutions of the three-level volt-second balance given by

$$T_1 \cdot V_1 + T_2 \cdot V_2 + T_3 \cdot V_3 = T_{SVM} \cdot V_s^* \quad (7)$$

and verifying

$$T_1 + T_2 + T_3 = T_{SVM}. \quad (8)$$

The resolution of (7) and (8) for given V_1 , V_2 , and V_3 can lead to a potentially complex calculation. But, thanks to the proposed families repartition described above, T_i calculation can be easily performed. As an example, we detail this step for family 2.

The substitution of (4) in (7) leads to

$$\begin{aligned} T_{SVM} \cdot V_{sm} \begin{pmatrix} \cos \theta_s \\ \sin \theta_s \end{pmatrix} &= \left[\frac{V_{dc}}{3} \begin{pmatrix} \cos(k-1) \frac{\pi}{3} \\ \sin(k-1) \frac{\pi}{3} \end{pmatrix} \cdot T_1 \right. \\ &+ \frac{2V_{dc}}{3} \begin{pmatrix} \cos(k-1) \frac{\pi}{3} \\ \sin(k-1) \frac{\pi}{3} \end{pmatrix} \cdot T_2 \\ &\left. + \frac{V_{dc}}{\sqrt{3}} \begin{pmatrix} \cos(k-0.5) \frac{\pi}{3} \\ \sin(k-0.5) \frac{\pi}{3} \end{pmatrix} \cdot T_3 \right]. \end{aligned} \quad (9)$$

Consequently,

$$\begin{pmatrix} \cos \theta_s \\ \sin \theta_s \end{pmatrix} = \frac{V_{dc}}{3T_{SVM} \cdot V_{sm}} \cdot B \cdot \begin{pmatrix} T_1 + 2T_2 \\ \sqrt{3} \cdot T_3 \end{pmatrix}, \quad (10)$$

where

$$\begin{aligned} B &= \begin{pmatrix} \cos(k-1) \frac{\pi}{3} & \cos(k-0.5) \frac{\pi}{3} \\ \sin(k-1) \frac{\pi}{3} & \sin(k-0.5) \frac{\pi}{3} \end{pmatrix}, \\ B^{-1} &= 2 \cdot \begin{pmatrix} \sin(k-0.5) \frac{\pi}{3} & -\cos(k-0.5) \frac{\pi}{3} \\ -\sin(k-1) \frac{\pi}{3} & \cos(k-1) \frac{\pi}{3} \end{pmatrix}. \end{aligned} \quad (11)$$

From (10) and (11) it can be deduced that

$$\begin{aligned} T_1 + 2T_2 &= \frac{6T_{SVM} \cdot V_{sm}}{V_{dc}} \left[\sin\left((k-0.5) \frac{\pi}{3}\right) \cos \theta_s \right. \\ &\left. - \cos\left((k-0.5) \frac{\pi}{3}\right) \sin \theta_s \right], \end{aligned} \quad (12)$$

$$\begin{aligned} T_3 &= \frac{2\sqrt{3}T_{SVM} \cdot V_{sm}}{V_{dc}} \left[\cos\left((k-1) \frac{\pi}{3}\right) \sin \theta_s \right. \\ &\left. - \sin\left((k-1) \frac{\pi}{3}\right) \cos \theta_s \right]. \end{aligned} \quad (13)$$

Equation (13) gives

$$T_3 = \frac{2\sqrt{3}T_{SVM} \cdot V_{sm}}{V_{dc}} \sin\left(\theta_s - (k-1) \frac{\pi}{3}\right). \quad (14)$$

To simplify T_i expressions, we introduce θ_i defined as

$$\theta_i = \theta_s - (k-1) \frac{\pi}{3}. \quad (15)$$

Considering (15), T_3 final expression is

$$T_3 = \frac{2\sqrt{3}T_{SVM} \cdot V_{sm}}{V_{dc}} \sin(\theta_i). \quad (16)$$

TABLE 1: On-times calculation.

Family	1	2	3	4
T_1	T_{k1}	$T_{SVM} - T_3 - T_2$	$T_{SVM} - T_{k2}$	$T_{SVM} - T_2 - T_3$
T_2	T_{k2}	$-T_{SVM} + T_{k1}$	$T_{SVM} - T_{k1}$	$-T_{SVM} + T_{k2}$
T_3	$T_{SVM} - T_1 - T_2$	T_{k2}	$T_{SVM} - T_1 - T_2$	T_{k1}

After substituting (15) in (12) one can write

$$T_1 + 2T_2 = \frac{6T_{SVM} \cdot V_{sm}}{V_{dc}} \sin\left(\frac{\pi}{6} - \theta_i\right). \quad (17)$$

Comparing (7) and (17) gives

$$\begin{aligned} T_1 &= \frac{6T_{SVM} \cdot V_{sm}}{V_{dc}} \sin\left(\frac{\pi}{6} - \theta_i\right) - 2T_2 \\ &= T_{SVM} - T_3 - T_2. \end{aligned} \quad (18)$$

Consequently

$$T_2 = \frac{6T_{SVM} \cdot V_{sm}}{V_{dc}} \sin\left(\frac{\pi}{6} - \theta_i\right) - T_{SVM} + T_3. \quad (19)$$

The final T_i expressions for family 2 are as follows:

$$\begin{aligned} T_1 &= T_{SVM} - T_3 - T_2, \\ T_2 &= \frac{6T_{SVM} \cdot V_{sm}}{V_{dc}} \sin\left(\frac{\pi}{6} - \theta_i\right) - T_{SVM} + T_3, \\ T_3 &= \frac{2\sqrt{3} \cdot T_{SVM} \cdot V_{sm}}{V_{dc}} \sin(\theta_i). \end{aligned} \quad (20)$$

The same computation method is applied for the remaining 3 families. Consequently, the obtained on-times vectors applications for the 4 families are summarized in Table 1, where

$$\begin{aligned} A &= \frac{2 \cdot \sqrt{3} \cdot V_{sm} \cdot T_{SVM}}{V_{dc}}, \\ T_{k1} &= A \sin\left(\frac{\pi}{3} - \theta_i\right), \\ T_{k2} &= A \sin \theta_i. \end{aligned} \quad (21)$$

3.3. Step 3: Secondary ON-Times Calculation. As explained in Section 1, each vector can be reached by multiple PLS. The aim of Step 3 is to choose which PLS has to be activated over its corresponding on-time. Obviously, the inverter performance significantly depends on this PLS management.

The aim of the PLS management is to operate with fixed switching frequency: this is easily reachable when each IGBT switches once during a switching period. In fact, for a selected triangle, the available PLS are applied, so they are all used during a switching period and the transition from one PLS to the other requires only one commutation. For example, if V_s^* is localized in triangle 4, the order of application of PLS is

$$\begin{aligned} (1, 1, 0) &\rightarrow (2, 1, 0) \rightarrow (2, 2, 0) \rightarrow (2, 2, 1) \\ &\rightarrow (2, 2, 0) \rightarrow (2, 1, 0) \rightarrow (1, 1, 0). \end{aligned} \quad (22)$$

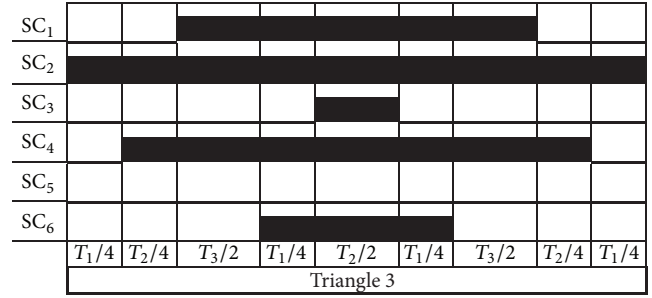


FIGURE 12: Switching signals for triangle 3.

3.4. Step 4: Dispatching within T_{SVM} . According to the described PLS management strategy, each PLS is realized first by defining the appropriate space vector (V_1 , V_2 , or V_3). Since the previously calculated on-times T_i are the total application time for the space vector V_i within T_{SVM} , they are evenly spread over the switching period. For example, if V_s^* is localized in triangle 4, V_1 (of family 4) is applied 3 times during T_{SVM} , and V_2 and V_3 must be applied twice. Therefore, T_1 is equally divided into 3 time slots: each PLS that generates V_1 is applied during $T_1/3$. T_2 and T_3 are also divided into 2 time slots equal to $T_2/2$ and $T_3/2$, respectively. The resulting control signals of triangle 3 are shown in Figure 12.

4. Simulation Results

The three-level NPC converter is simulated using PSIM software, where the converter is connected to an RL load, as shown in Figure 13. Simulation parameters are presented in Table 2.

As mentioned in Section 3.1, the triangles covered by the space vector reference depend on the modulation depth m . Figure 13 shows the sectors and triangles covered by the space vector for a reference magnitude equal to 100 V. Thus, modulation depth m is equal to $m = 100/270 = 0.37$.

For $m = 0.37$, when the space vector is circulating in sector 1 (2, 3, 4, 5, and 6, resp.), the triangle containing the space vector is T1 (T5, T9, T13, T17, and T21, resp.). It is to be noted that all of the 6 triangles are covered during 20 ms, corresponding to the reference voltage's frequency of 50 Hz.

Similarly, Figure 14 presents the sectors and triangles covered by the space vector when the reference magnitude is equal to 250; that is, $m = 0.92$.

The lookup table implemented on PSIM generates the appropriate control signals depending on the selected sector and triangle. Figure 15 presents the converter's control signals when the reference space vector is in triangle 3 and the resulting phase voltage. It is seen in Figure 15(b) that the

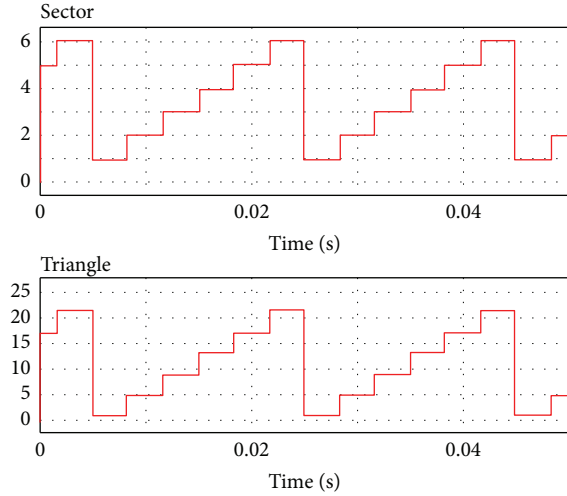
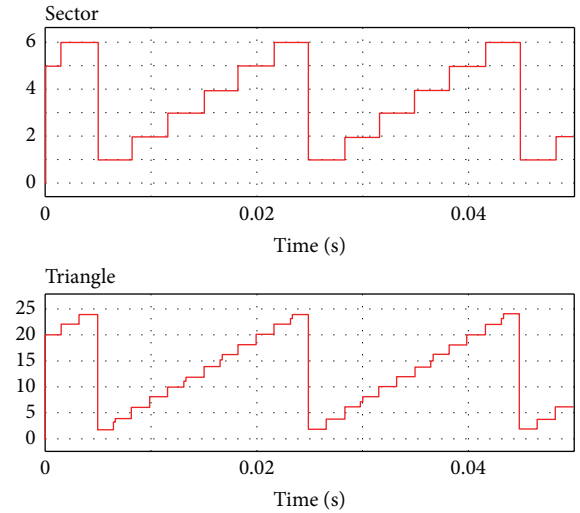
FIGURE 13: Space vector's sector and triangle for $m = 0.37$.FIGURE 14: Space vector's sector and triangle for $m = 0.92$.

TABLE 2: Simulation parameters.

Item	Value
Switching frequency T_{SVM}	50 μ s
DC link voltage	540 V
Line frequency	50 Hz
Load resistor R	10 Ω
Load inductor L	2 mH

proposed sequencing of the PLS ensures that the phase level (consequently voltage level) changes only once per commutation cell.

In order to validate the converter performances of the proposed scheme, the output line currents are presented in Figure 16. Maximum magnitude is equal to 28 A. Line-to-line and phase leg voltages are shown in Figure 17. The expected multilevel waveforms insure the power quality improvement. This is illustrated by line a current spectrum given in Figure 18. THD value is estimated to be 0.69%. On this spectrum, the main harmonic is equal to 20 kHz which corresponds to the switching frequency f_{sw} .

It is to be noted that, thanks to the proposed SVM strategy, the converter's switching frequency f_c is constant. Moreover, when the modulation depth m is greater than 0.575, f_c is almost equal to 50% of f_{sw} . Thus, the analysis of the whole switching signals proves that each IGBT switches once per T_{sw} , during almost half of the reference period. For example, for switching signal SC1, it switches once per T_{sw} , if the vector V_s belongs to triangles T2, T3, T4, T6, T7, T19, T20, T22, T23, and T24. When V_s belongs to T8, T10, T11, T12, T14, T15, T16, and T18, SC1 does not switch.

This leads to a mean switching frequency of $T_{sw}/2$. Figure 19 gives the simulated switching frequency of the three converter legs. A 20 ms window is used to perform the switching frequency calculation.

Switching frequency f_{sw} of one leg is presented as the average of f_{sw} of the IGBTs in the same leg. They are calculated as

$$\begin{aligned}
 f_{sw-a} &= \frac{f_{sw1} + f_{sw2}}{2}, \\
 f_{sw-b} &= \frac{f_{sw3} + f_{sw4}}{2}, \\
 f_{sw-c} &= \frac{f_{sw5} + f_{sw6}}{2},
 \end{aligned} \tag{23}$$

where f_{swi} is the switching frequency of IGBTi. f_{sw-a} (f_{sw-b} and f_{sw-c} , resp.) is leg a (leg b and leg c, resp.) switching frequency.

It is shown in Figure 18 that f_{sw} for each leg is a constant equal to 10.4 kHz. The additional 400 Hz compared to the SVM design (one commutation per IGBT within one T_{SVM}) is due to the V_s transition from one triangle to another.

5. Experimental Results

The proposed algorithm is experimentally tested. A 4 kW three-phase three-level NPC converter laboratory prototype was conceived as shown in Figure 20. The setup parameters are listed in Table 3. The power devices are the F3L150R07W2E3_B11 from Infineon. The proposed modulation method is implemented with a TI TMS320F2809 DSP.

Figure 21 shows the triangles crossed by V_s for different modulation depths. When $m < 0.5$, V_s crosses 6 triangles which are T1, T5, T9, T13, T17, and T21 (Figure 21(a)). When $m > 0.5$, V_s crosses the remaining triangles (Figure 21(b)).

Figure 22 shows the steady state waveforms of the line-to-line voltages and line a current.

The spectral analysis of the line current given in Figure 23 shows that first carrier harmonics appear at 20 kHz and then 40 kHz according to theoretical and simulation investigations.

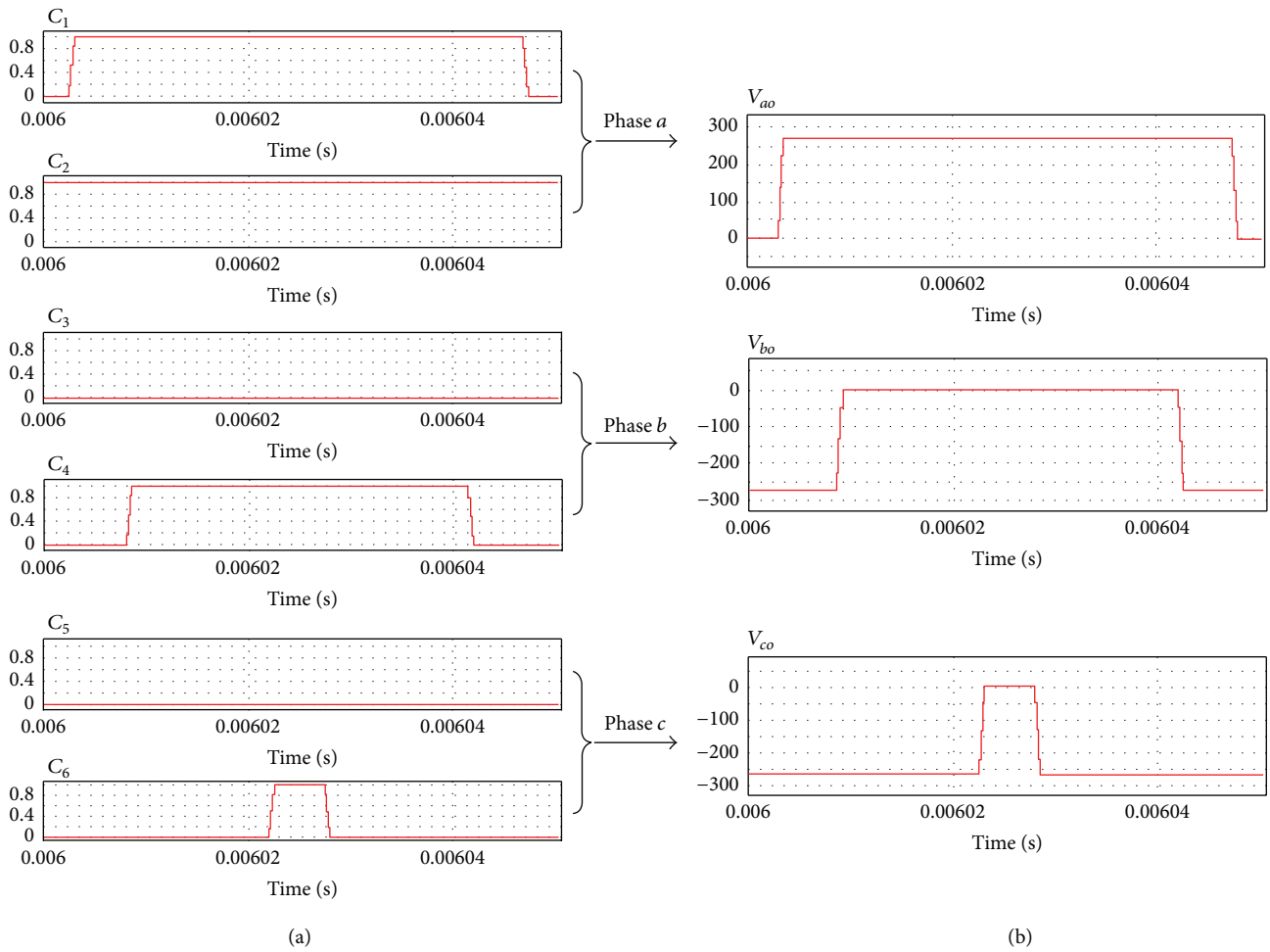


FIGURE 15: Triangle 3 simulation results: (a) control signals; (b) 3 phases output voltages.

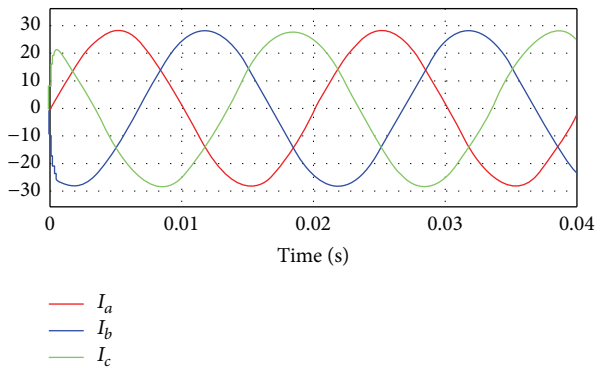


FIGURE 16: Output line currents.

Figure 24 shows the control signals of one commutation cell of leg a during two switching periods. The control signals are complementary, and the IGBTs switch once per period.

TABLE 3: Parameters of the 3-phase 3-level NPC converter.

Item	Value
Rated active power	4 kW
Switching frequency	20 kHz
Line frequency	50 Hz
DC link voltage	400 V
Line current amplitude	10 A

6. Conclusion

This paper proposes a Space Vector Modulation (SVM) technique for a three-level NPC converter. The proposed method consists in dividing the space vector diagram into four categories leading to a simple nearest three-vector detection and on-times calculation. Moreover, the choice of the converter Phase Level Sequence is used as an extra degree of freedom in order to control the converter's switching frequency. In fact, once the vectors to apply are detected, their corresponding Phase Level Sequences are dispatched

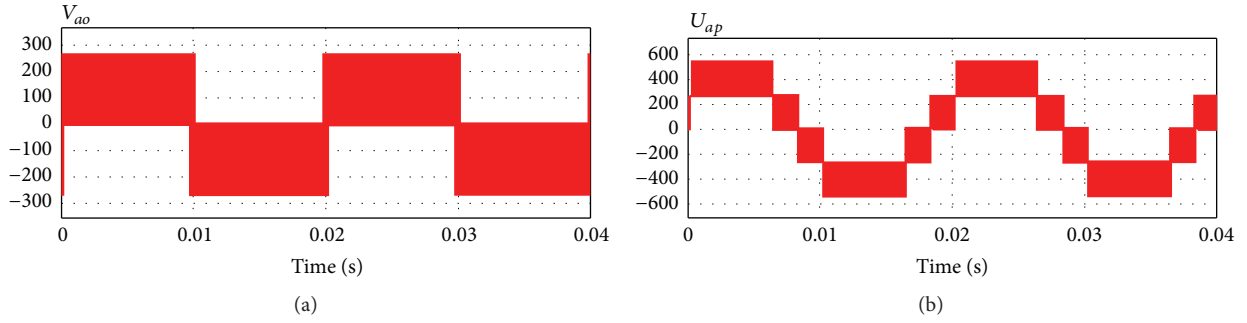


FIGURE 17: NPC voltages: (a) simple phase voltage; (b) line-to-line voltage.

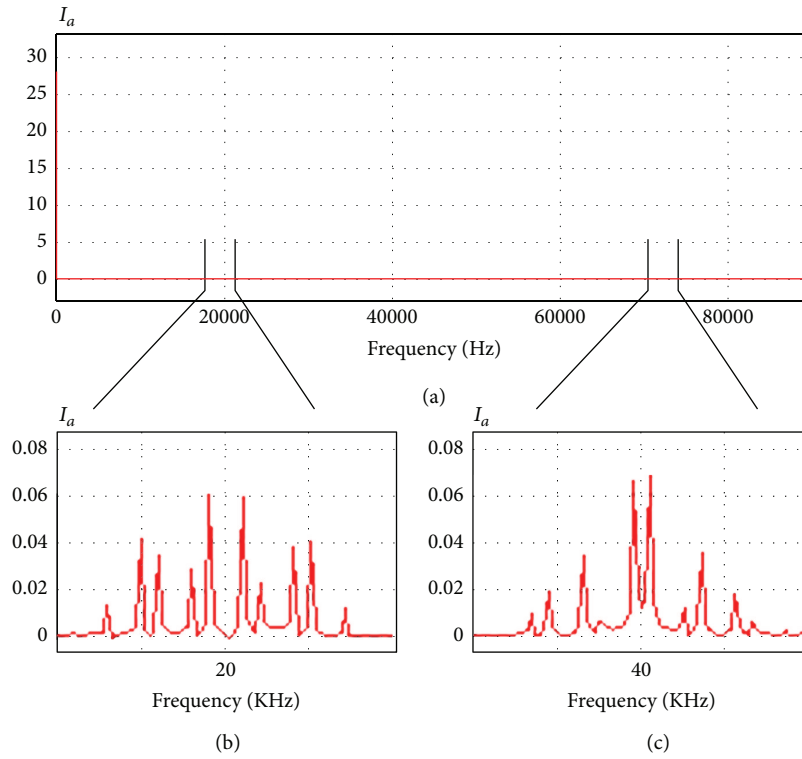


FIGURE 18: (a) Line a current spectral analysis; (b) zoom around 20 kHz; (c) zoom around 40 kHz.

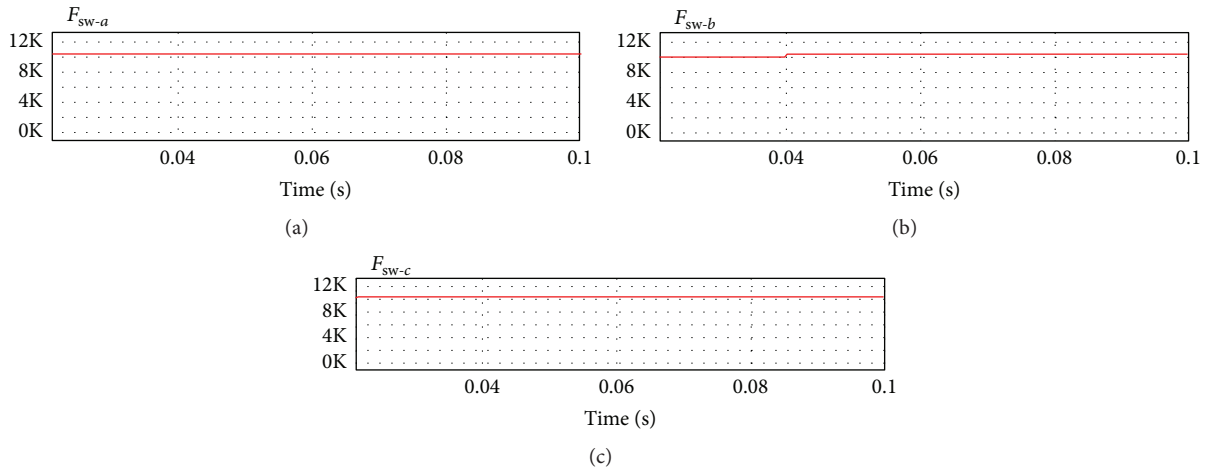


FIGURE 19: NPC legs switching frequencies: (a) leg a; (b) leg b; (c) leg c.

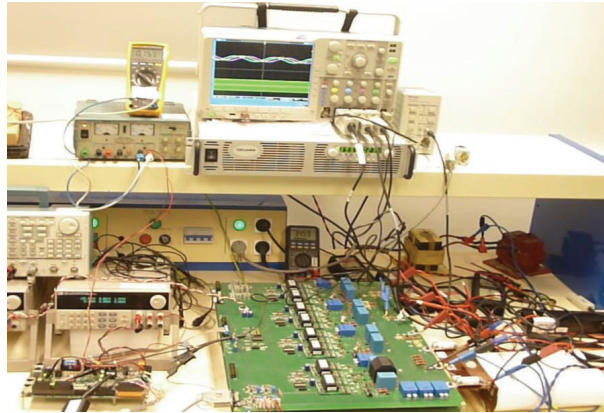


FIGURE 20: The experimental setup.

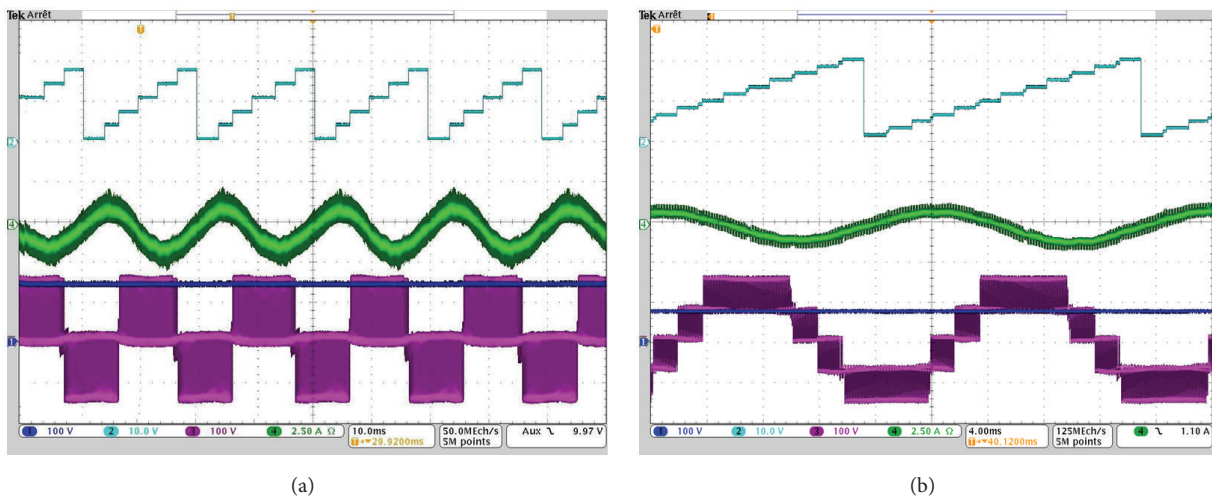


FIGURE 21: SVM triangles when (a) $m < 0.5$ and (b) $m > 0.5$.

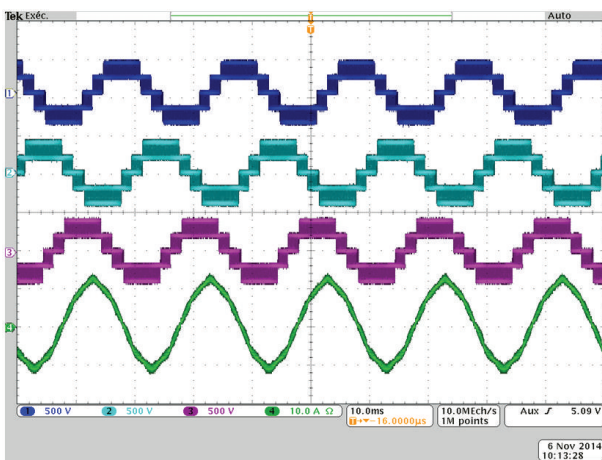


FIGURE 22: Line-to-line voltages and line a current.

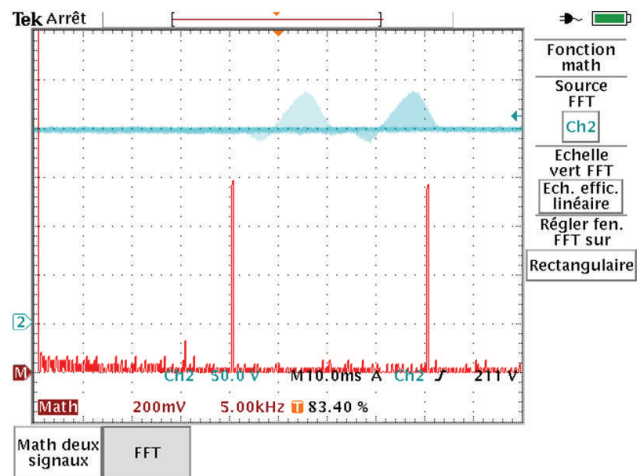


FIGURE 23: Spectral analysis of line a current.

among the SVM period such that they are all applied and the transition from one PLS to the following requires only one commutation. This SVM can be extended to higher levels if

the space vector diagram available triangles are appropriately defined.

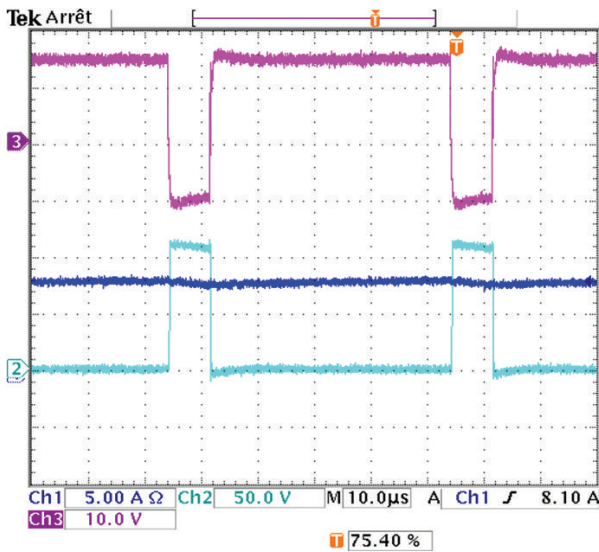


FIGURE 24: Leg a commutation cell control signals.

The proposed methodology is verified by simulation and through a 4 kW experimental test bed: the resulting output currents show a constant switching frequency and a reduced current THD. For applications such as renewable energies, this is a valuable improvement since it reduces the commutation power losses and lowers the output and grid connection filters size.

Nomenclature

NPC:	Neutral point clamped
SVM:	Space Vector Modulation
V_{dc} :	DC bus voltage
V_s :	Space vector output voltage
THD:	Total Harmonic Distortion
SC_i :	i th cell control signal
X, Y, Z:	Phase level related to phase a, b, and c, respectively
PLS:	Phase Level Sequence
V_s^* :	Reference voltage vector
V_k :	Nonzero voltage space vector in the (α, β) frame
T_k :	Application time related to V_k
T_{SVM} :	SVM period
PWM:	Pulse Width Modulation
θ_s :	Phase of the reference voltage vector
f_{sw} :	Switching frequency.

Competing Interests

The authors declare that there are no competing interests related to this paper.

Acknowledgments

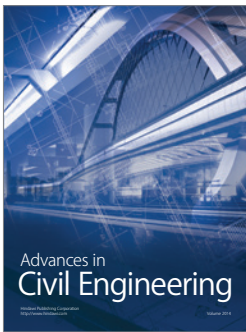
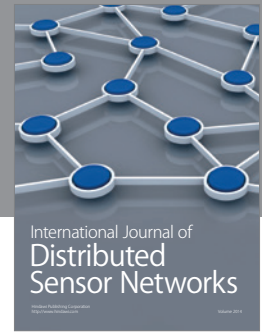
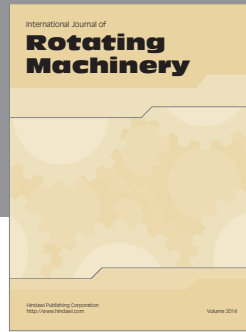
This work was partially supported by Tunisian-French Cooperation project CMCU 12G 1120, LAPLACE (University of

Toulouse), and LSE (University of Tunis El Manar). Particularly, the authors gratefully acknowledge Professor Frédéric Richardeau, Professor Maria David-Pietrzak, and Engineer Jean-Marc Blaquièrre from LAPLACE-University of Toulouse for their support for the experimental validation.

References

- [1] M. Amirabadi, "A new class of high-power-density universal power converters," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE '15)*, pp. 2596–2602, Montreal, Canada, September 2015.
- [2] S. Soumiah, R. P. Vengatesh, and S. E. Rajan, "Performance evaluation of single switch high frequency resonant power converter for alternative energy sources," in *Proceedings of the IEEE International Conference on Circuit, Power and Computing Technologies (ICCPCT '15)*, pp. 1–10, Nagercoil, India, March 2015.
- [3] N. Mittal, B. Singh, S. P. Singh, R. Dixit, and D. Kumar, "Multilevel inverters: a literature survey on topologies and control strategies," in *Proceedings of the 2nd International Conference on Power, Control and Embedded Systems (ICPCES '12)*, pp. 1–11, Allahabad, India, December 2012.
- [4] A. Christe and D. Dujić, "State-space modeling of modular multilevel converters including line frequency transformer," in *Proceedings of the 17th European Conference on Power Electronics and Applications (EPE '15)*, pp. 1–10, Geneva, Switzerland, September 2015.
- [5] R. H. Baker, "Bridge converter circuit," US4270163 A, 1981.
- [6] L. Ma, X. Jin, T. Kerekes, M. Liserre, R. Teodorescu, and P. Rodriguez, "The PWM strategies of grid-connected distributed generation active NPC inverters," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE '09)*, pp. 920–927, September 2009.
- [7] S. Saridakis, E. Koutroulis, and F. Blaabjerg, "Optimal design of NPC and active-NPC transformerless PV inverters," in *Proceedings of the 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG '12)*, pp. 106–113, Aalborg, Denmark, June 2012.
- [8] J. Li, S. Bhattacharya, and A. Q. Huang, "A new nine-level active NPC (ANPC) converter for grid connection of large wind turbines for distributed generation," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 961–972, 2011.
- [9] O. Bouhali, N. Rizoug, T. Mesbahi, and B. Francois, "Modeling and control of the three-phase NPC multilevel converter using an equivalent matrix structure," in *Proceedings of the 7th IET International Conference on Power Electronics, Machines and Drives (PEMD '14)*, pp. 1–6, April 2014.
- [10] C. Wang and Y. Li, "A new balancing algorithm of neutral-point potential in the three-level NPC converters," in *Proceedings of the IEEE Industry Applications Society Annual Meeting (IAS '08)*, pp. 1–5, Edmonton, Canada, October 2008.
- [11] K. Komatsu, M. Yatsu, S. Miyashita et al., "New IGBT modules for advanced neutral-point-clamped 3-level power converters," in *Proceedings of the International Power Electronics Conference-ECCE Asia (IPEC '10)*, pp. 523–527, Sapporo, Japan, June 2010.
- [12] T. B. Soeiro and J. W. Kolar, "The new high-efficiency hybrid neutral-point-clamped converter," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 1919–1935, 2013.
- [13] N. Celanovic and D. Boroyevich, "A fast space vector modulation algorithm for multilevel three-phase converters," in

- Proceedings of the Conference Record of the IEEE Industry Applications Conference, 34th IAS Annual Meeting*, vol. 2, pp. 1173–1177, Phoenix, Ariz, USA, October 1999.
- [14] B. Zhang, Q. Ge, L. Tan, X. Wang, Q. Chang, and J. Liu, “A new PWM strategy for three-level Active NPC converter,” in *Proceedings of the International Conference on Electrical Machines and Systems (ICEMS '13)*, pp. 1792–1795, Busan, Republic of Korea, October 2013.
- [15] H. Yi, F. Zhuo, F. Wang, and Z. Wang, “A digital hysteresis current controller for three-level neutral-point-clamped inverter with mixed-levels and prediction-based sampling,” *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3945–3957, 2016.
- [16] M. Sharifzadeh, A. Sheikholeslami, H. Vahedi, H. Ghoreishy, P. Labbé, and K. Al-Haddad, “Optimised harmonic elimination modulation extended to four-leg neutral-point-clamped inverter,” *IET Power Electronics*, vol. 9, no. 3, pp. 441–448, 2016.
- [17] Z.-B. Yuan, J.-J. Zhang, J. Hao, and D.-Y. Lu, “Phase-shift selective harmonic elimination pulse width modulation for multilevel converter,” in *Proceedings of the 34th Chinese Control Conference (CCC '15)*, pp. 8981–8985, Hangzhou, China, July 2015.
- [18] V. Dargahi, A. K. Sadigh, and K. Corzine, “Selective harmonic elimination for extended cascaded multicell multilevel power converters,” in *Proceedings of the Clemson University Power Systems Conference (PSC '15)*, pp. 1–8, Clemson University, March 2015.
- [19] A. Nabae, I. Takahashi, and H. Akagi, “A new neutral-point-clamped PWM inverter,” *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, 1981.
- [20] Y.-H. Yu, N.-J. Ku, and D.-S. Hyun, “The control algorithm of three-level NPC inverter under unbalanced input voltage conditions,” in *Proceedings of the IEEE Vehicle Power and Propulsion Conference (VPPC '14)*, IEEE, Coimbra, Portugal, October 2014.
- [21] V. Dargahi, A. K. Sadigh, and K. Corzine, “Selective harmonic elimination for extended cascaded multicell multilevel power converters,” in *Proceedings of the Clemson University Power Systems Conference (PSC '15)*, Clemson, SC, USA, March 2015.
- [22] Y. Deng, Y. Wang, K. H. Teo, and R. G. Harley, “A simplified space vector modulation scheme for multilevel converters,” *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 1873–1886, 2016.



Hindawi

Submit your manuscripts at
<http://www.hindawi.com>

