

**CHARACTERIZING AND MODELING OF TRANSIENT BEHAVIOR IN POWER
ELECTRONIC CIRCUITS WITH WIDE BANDGAP SEMICONDUCTORS AND IN
MAXIMUM POWER POINT TRACKING FOR PHOTOVOLTAIC SYSTEMS**

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This dissertation examines the transient characteristics in next generation power electronic circuits at both the device-level and the systems-level. At the device-level, the effect of the parasitic capacitances on the switching performance of emerging wide bandgap semiconductors (WBG) is evaluated. Equivalent device models based on gallium nitride (GaN) and silicon carbide (SiC) are implemented in SaberRD and MATLAB, and transient switching characteristics are analyzed in great detail. The effects of the parasitic capacitances on detrimental circuit behavior such as “overshoot,” “ringing,” and “false turn-on” are investigated. The modeled results are supplemented and validated with experimental characterization of the devices in various power conversion circuits. The models can be used to aid in the design of next generation WBG devices so that the undesirable transient effects displayed by contemporary versions of these devices can be mitigated.

At the systems-level, the transient overshoot demonstrated by conventional maximum power point tracking algorithms for photovoltaic power conversion systems is investigated. An adaptive controller is implemented so that the operating point can converge to the optimal power point rapidly with minimal overshoot. This new controller overcomes the parasitic components

inherent to the power converter which limit its ability to deliver maximum power rapidly. It will be shown that with the new controller, the maximum power point is attainable in 4 milliseconds.

The work accomplished in this dissertation lays a foundation for power electronic engineers to integrate semiconductor device theory with control theory to optimize the performance of next generation power conversion systems.

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PREFACE

First and foremost I would like to thank my honorable, esteemed and ever so humble adviser, Dr. William Stanchina. When working with Dr. Stanchina, you would have a hard time believing how successful and accomplished he is – given his down to earth and modest demeanor. He shows the rare combination of patience, decency and success. In addition to being my PhD adviser, Dr. Stanchina has been the chairperson in the ECE Dept. at Pitt, and even such has always held an “open door” policy for me (and others). Being a PhD student is at many times a stressful, emergency prone endeavor. I am the type of person that always likes to solicit advice before making a hard decision. Dr. Stanchina was always there for me when I needed his valued opinions, in spite of his very busy schedule. I will never forget the first year of my PhD, where Dr. Stanchina showed me how to review and interpret the literature. It was because of that pivotal first year “growing experience” that bolstered me to eventually learn how to follow my own light, down the long tunnel of a PhD. Dr. Stanchina has also instilled in me the value of presentation. As an example, prior to my leaving for a conference in California to present research results, Dr. Stanchina asked me to practice my presentation many times as he spent his precious time watching and critiquing. Because of this, I was able to win a presentation award at the conference. Throughout the hundreds of one on one meetings I have had with him over the past 6 years, I will always be grateful for our conversations about life. We could talk about anything: sports, the news, family, etc etc. I learned so much from these conversations and it

relieved me to have a real-life example in front of me of someone who could be such a successful person in both his personal life and his career. I made many mistakes throughout the course of graduate school, and while most other advisers would show frustration to these mistakes, Dr. Stanchina showed patience. He always believed in me, and if he had not, I would not be here today. For these reasons, and many more, I am grateful to him. It is my sincerest wish that he and I will continue to work together, and more importantly maintain our relationship together. I have met Dr. Stanchina's family on many occasions and it is also clear to me what a wonderful family man he is as well. His ability to balance family, work and fun so magnanimously is truly inspiring.

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From the beginning, Dr. Reed envisioned a power program that spanned the entire scale of power systems, from large scale to small scale. Dr. Reed's expertise is in large scale power systems. However he still supported my research in semiconductor device modeling. I am truly grateful to Dr. Reed for always believing in me, and supporting me to work on something outside his broad spectrum of expertise. Also, because of Dr. Reed's incredible ability to spread the word about our program at Pitt, I have become involved with many of the power industries, not only in Pittsburgh, but also at national labs in the Washington DC area. This is all due to Dr. Reed's amazing ability to promote and advertise our power program.

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I would like to thank my Aunt and Uncle, Dr. Dolly Luthra and Dr. Juginder Luthra. Your inspiring family filled with love is truly a blessing. When my immediate family could not be there, you were always there, right from the beginning of my life. Thank you.

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1.0 INTRODUCTION

This dissertation explores technical approaches for analyzing and characterizing the dynamic behavior of power electronic converters as influenced by the semiconductor device utilized in power conversion circuits and maximum power point tracking (MPPT) in photovoltaic systems. The dynamic behavior of electronic power converters has a significant impact on the efficiency of the entire system. The research accomplished here examines the dynamic performance of power conversion circuits at two levels. First, the effects of the parasitic components the switching performance of emerging wide bandgap semiconductor devices is analyzed. Second, the parasitic effects of DC-DC converters using MPPT control algorithms will be explored. This two level approach can facilitate a unique integration of wide bandgap device model development and innovative MPPT algorithm design in order to maximize the efficiency of the power converters utilized in photovoltaic systems.

The accomplished work will lay a foundation for optimizing power conversion at both the small scale device level, through understanding the impact of device capacitances and at the larger-scale sub-systems level through analyzing the impacts of DC-DC converter parasitics on the performance of MPPT control algorithms. To achieve this first requires independently analyzing the dynamic influence of both the semiconductor device and the MPPT control algorithm.

This introductory section of the dissertation provides the project's objective in section 1.1 and the project's motivation/impact in section 1.2. Finally, the organization for the rest of this dissertation is given in section 1.3.

1.1 OBJECTIVE

Wide bandgap semiconductors like Gallium Nitride (GaN) and Silicon Carbide (SiC) are attractive candidates to replace Silicon (Si) as the primary switching device in future power converters of photovoltaic systems. Relative to Si Field Effect Transistors (FETs), GaN and SiC FETs can operate in higher switching frequency and higher temperature applications. This facilitates the implementation of power converters in a smaller operating area/footprint with minimal loss. This attribute is essential for the application of renewable energy sources as well as electric vehicles where high power density (high efficiency and low operating area) is of primary interest [1, 2]. The impact of the wide bandgap semiconductor's parasitic components (capacitances, inductances) on the performance of power conversion systems is not fully understood. Although the fast switching capability of WBGs is generally considered a beneficial feature, undesirable and detrimental high dv/dt transient effects such as "high overshoot," "ringing loss," and "false turn-on" can also arise. The cause of these effects, as well as potential design modifications for these effects is explored in this dissertation. Furthermore, many MPPT control algorithms reported in the literature for PV systems have promised to increase the efficiency of photovoltaic systems by regulating the system about its theoretical optimal power point; however, several limitations with these current MPPT algorithms have hindered their ability to consistently extract maximum allowable power from photovoltaic systems [3].

Demonstrated here is a method for characterizing the dynamic responses of power converter systems as influenced by emerging wide bandgap semiconductors and more sophisticated MPPT control algorithms. The accomplished work will therefore address parasitic power conversion effects at the small-scale power switching device level and at the larger-scale converter level. Such an analysis will enable the eventual integration of wide bandgap semiconductor device models with a novel MPPT control algorithm in order to maximize the efficiency of next generation photovoltaic power conversion systems.

The development of novel device models for emerging wide bandgap semiconductor transistors allows for a benchmark analysis against today's Si devices, which is the current state of the art technology for power switching [4]. Consequently, the potential advantages of wide bandgap devices for future generation power converters in photovoltaic systems will be demonstrated in this work. In addition to device model development for existing devices, methodologies will be demonstrated that enable future scaled device structures to be transformed into potential building blocks for new electric power transmission and distribution systems.

Due to the ability of GaN/SiC transistors to adequately sustain high switching frequency applications, the filter sizes required for GaN/SiC based power converters can be significantly decreased which should lead to optimized power density within the converter [5]. Thus, the integration of the wide bandgap device model with the novel MPPT controller would demonstrate the feasibility of an enhanced power optimization system that reduces power converter inefficiencies and sizes while extracting optimal power from photovoltaic installations.

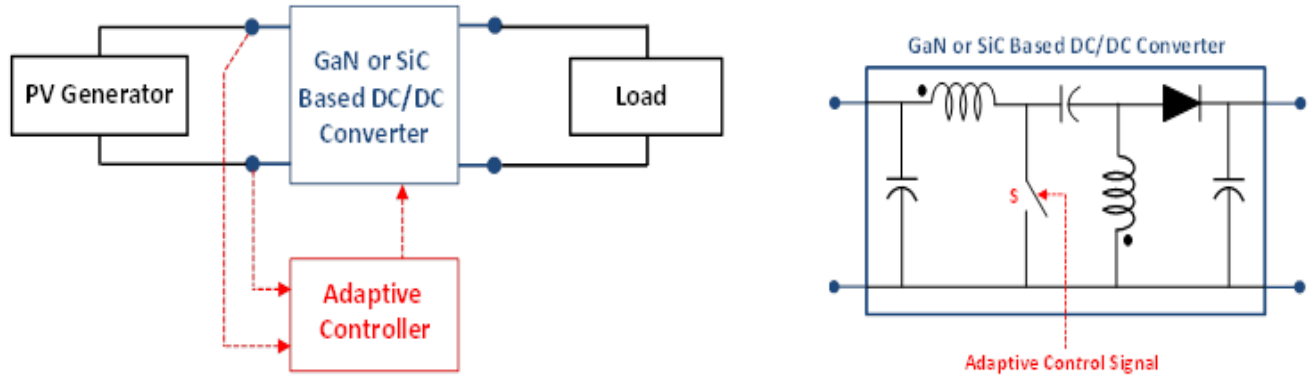


Figure 1: GaN/SiC based PV converter with adaptive control.

Figure 1 (left) depicts a schematic of the power conversion system under study. A solar array feeds the input of a DC/DC converter. This DC/DC converter is used to regulate and condition the power coming out of the solar array for grid-level integration. An adaptive control system senses the photovoltaic output and produces a new duty cycle to control the switching of the novel wide bandgap transistor model, denoted “S” in Figure 1 (right). Thus, as solar insolation and temperature vary, the control system regularly updates the duty cycle for the transistor in order to deliver maximum available power for that operating point. In addition, the entire system envisioned here would reduce switching and conduction losses as well as filter sizes within the converter thereby maximizing power density. A full theoretical model of the system in Figure 1 is a long range vision but is beyond the scope of this dissertation. However, characterizing the parasitic components of the devices that influence the switching losses, as well as analyzing the parasitic effects in various MPPT control schemes is what is proposed for this dissertation. Specifically, the proposed work will address optimizing the performance of next generation power electronic converters both at the switching transistor level and the converter

level. Thus, this dissertation will serve as a basis for future work where device models can be integrated with an MPPT controller.

To develop the GaN/SiC FET models, commercial devices of differing sizes and power ratings along with their respective data sheets will be used as the basis for simulating the devices' performance. Behavioral models which simulate the current-voltage (I-V) and capacitance-voltage (C-V) characteristics of the devices will be developed in SaberRD™ (Synopsys) [6]. In addition, analytical equivalent circuit models will be developed for time-domain analysis using MATLAB. The behavioral and analytical model results will be compared to experimental results obtained from the using these wide bandgap devices in experimentally constructed switching test circuits. These switching-loss analyses of GaN/SiC devices of various sizes and power ratings may enable the development of “scaling-rules” which could be used to project to the performance of future larger voltage/current GaN/SiC devices.

One particular topic of interest in this dissertation will be characterizing the effects of the parasitic device components on the switching behavior of the device. As a result, this dissertation will explore the dynamic behavior of power electronic converters, and how the parasitic components of the device can be optimized in order to ensure more efficient converter operation. This is an essential study, as the parasitic components of WBGs have led to detrimental undesirable phenomena such as false turn-on, overshoot and ringing. These harmful effects are hindering WBGs from attaining their full potential of enhancing the performance of next generation power electronic systems. This dissertation models these behaviors in WBGs, so that future generations of these devices can be designed with more optimal performance. In addition, photovoltaic power conversion systems have parasitic components inherent to them which adversely impact the performance of MPPT control algorithms. A new adaptive controller that

accounts for these system parasitics is developed which enables the system to converge to the theoretical MPP with minimal oscillation. Thus, the dynamic behavior of MPPT control algorithms in power conversion circuits will also be investigated.

Resulting from this two-level study is the ability to integrate the emerging wide bandgap semiconductor device models with the MPPT controller, to enable a new generation of photovoltaic system DC-DC converters which minimize losses while delivering optimal power to the load.

1.2 MOTIVATION AND IMPACT

The emerging global energy crisis has led to national mandates of promoting efficient green energy usage while reducing both carbon emissions and overall energy consumption. The US Congress has recently attempted to fulfill these national mandates by enacting several key pieces of legislation. For instance, the Energy Policy Act of 2005 sought to increase domestic energy production by providing loan guarantees and tax incentives to renewable energy producers [7]. The Energy Independence and Security Act of 2007 had the stated purpose “to move the United States toward greater energy independence and security, to increase the production of clean renewable fuels, to protect consumers, to increase the efficiency of products, buildings, and vehicles, to promote research on and deploy greenhouse gas capture and storage options, and to improve the energy performance of the Federal Government [8].” Finally, the American Recovery and Reinvestment Act of 2009 made \$27.2 billion available for research in energy

efficiency and renewable energy, including \$115 million specifically for the development of solar power technologies [9].

As one approach to properly address the afore mentioned issues, the prospect of integrating direct current (DC) power grids with renewable energy systems is being heavily researched for more efficient power transmission. The current US grid-infrastructure is comprised of alternating current (AC) technology and is becoming progressively untenable for increased levels of solar energy integration [10]. DC power is becoming an attractive candidate for large scale power systems and loads at both high and low voltage levels. This would mitigate the need for loss-intensive inverter conversion systems required today for converting the DC generated solar power into grid-compatible AC power [11, 12]. Furthermore, in applications requiring high voltage transmission, the AC infrastructure is more susceptible to distribution losses than the high voltage DC counterpart. In [12], a comparison between traditional AC and DC systems reveals that the DC system contains 0.5% higher losses than the AC system. However, if the semiconductor losses in the power converters are reduced by 50%, the DC system becomes more efficient than the AC system. These observations point to the promise of GaN and SiC switching devices to significantly improve the efficiency of DC systems and photovoltaic power converter systems.

However, many factors have prevented DC solar power from becoming a major component of US domestic electrical production. These factors include low photovoltaic cell efficiencies, high capital costs, low capacity factors, and limitations in the components of the power electronics converters utilized in distributing solar energy [13]. For instance, the National Renewable Energy Laboratory recently reported that the reliability of the Si based switching device is one of the most significant barriers to integrating solar energy to the power grids at a

high efficiency [14]. This is due in part to the fact that 80% of photovoltaic power converter system down time has been attributed to the Si component's intolerance to harsh operating environmental conditions such as high operating temperatures [15]. Both GaN and SiC have been demonstrated to adequately sustain high temperature applications and would therefore increase operating reliability of solar farms implemented in deserts and other extremely warm areas [16].

In order to avoid other inefficiencies of photovoltaic systems, MPPT algorithms have been introduced to increase utilization and capacity factors. However many of the algorithms reported in the literature have significant drawbacks which hinder their ability to adapt to rapidly changing environmental conditions. Additionally, many MPPT algorithms require complex control architectures making it difficult to implement the controller on the solar panel ("modular-level" MPPT controllers) which is more efficient than centralized grid-tie controllers [17]. This work proposes a novel adaptive control algorithm suitable for integration with GaN and SiC devices and modular-level MPPT control architectures thus providing the possibility of an even more efficient power converter system.

Recently, the prospect of GaN FETs in MPPT schemes of photovoltaic systems was described in [18]. It was reported that GaN based converters can enable improved "module-level" MPPT, where the controller is implemented on the back of the photovoltaic panel as opposed to a centralized grid-level controller which regulates the output voltages of numerous photovoltaic modules, collectively. Module-level MPPT can be achievable in GaN based converters due to the high switching frequency capability of GaN devices which allows for smaller sized filters within the converter. Thus, the size of a GaN based converter can be relatively smaller thereby permitting more room for control architectures on the back of the

photovoltaic panel. The benefits of a module-level MPPT controller include faster and more optimal tracking in contrast to its grid-level counterpart. This allows the module-level MPPT controller to more efficiently respond to rapid changes in solar insolation and ambient temperature [18]. Furthermore in [19], “Ripple Correlation Control” (RCC) is discussed as a potentially advantageous MPPT control algorithm in high switching frequency applications. It was reported that the convergence rate of RCC based algorithms is dependent on the switching frequency of the power converter. That is, at high switching frequencies the controller converges to the optimal power point at a faster speed. In addition, as described in [19], RCC based algorithms are more appropriate for “modular application, which would use many smaller converters.” Thus, GaN based converter systems would be a suitable candidate for MPPT control algorithms employing RCC.

It is the purpose of this work to develop GaN/SiC models and characterize the effects of their parasitic components on their dynamic performance in power electronic systems. In parallel, the parasitic effects of DC-DC converters on the dynamic performance of MPPT control algorithms will also be studied. A novel MPPT control algorithm will be developed that enables the system to rapidly converge to the MPP with minimal oscillation. This will permit the first integration between switching transistor models and control systems that could significantly increase the efficiency of photovoltaic systems.

1.3 DISSERTATION ORGANIZATION

The rest of this dissertation is organized as follows: Section 2.0 presents the literature review for both modeling Si based FETs and wide bandgap semiconductors next generation power electronics. Section 3.0 presents the current limitations with WBG devices which are preventing them from realizing their full potential. A research plan for modeling WBG devices is also given in Section 3.0.

Results from the research plan begin in Section 4.0 where the effect of the parasitic capacitances on the switching performance of GaN FETs is analyzed. Next, in Section 5.0 a high dv/dt test circuit is developed both experimentally and analytically to characterize phenomena known as “overshoot,” “ringing,” and “false turn-on” in SiC MOSFETs. In Section 6.0 a full synchronous buck converter is implemented. The interactions between the two FETs of synchronous buck converters are extensively investigated. False turn-on effects in SiC MOSFETs are further characterized analytically and experimentally in Section 6.0.

In Section 7.0 is a comprehensive literature review for state of the art techniques in MPPT control, as well as the research plan for implementing a faster more robust MPPT controller. Section 8.0 presents a new MPPT controller which can enable the photovoltaic power conversion system to converge to the MPP rapidly. Such a system minimizes “power wasting” where the operating point oscillates above and below the MPP for significant amounts of time before finally settling at the actual MPP. Concluding remarks for this dissertation are given in Section 9.0.

2.0 LITERATURE REVIEW ON WIDE BANDGAP SEMICONDUCTORS

This chapter of the dissertation discusses the unique properties of the wide bandgap semiconductors which potentially make them a superior device to Si in next generation power electronics. In addition to the wide bandgap property, other properties to be discussed include the body diode feature and several Figures of Merit (FOMs). These FOMs serve as metrics to benchmark current state of the art technologies against future generation devices in power electronics. The FOMs to be discussed are listed below:

- breakdown voltage versus cutoff frequency technology comparison using Johnson's FOM (JFOM)
- specific on resistance versus breakdown voltage FOM
- gate charge multiplied by specific on resistance FOM

Furthermore, approaches for modeling of power semiconductor devices will be discussed. In order for designers to completely understand the potential benefits and possible limitations of wide bandgap semiconductors, as well as project their performance in future generation power electronics, circuit simulation models of power electronics devices are becoming increasingly crucial. Continued improvement on SiC power devices has led to the development of several circuit simulation models [20, 21]. In [22] a parameter extraction procedure is given for SiC power MOSFETs using circuit simulation to model the device's behavior in both the linear and

saturation regions of operation. The approach used in [22] combines elements of physics-based and behavioral device models to accurately reproduce the I-V characteristics of the SiC MOSFET in both regions of operation. Bridging the gap between physics-based models and behavioral models was demonstrated in [23] where TCAD tools from Synopsys were used to optimize the performance of a virtual Si based power MOSFET. Using DESSIS (Synopsys) software, the authors of [23] were able to assess the impact of the output capacitance, C_{oss} on the switching performance of the virtual MOSFET. As will be demonstrated in subsequent chapters, an assessment of the effect that the parasitic capacitances have on the switching performance of both SiC and GaN devices will be presented with this work. Since the parasitic capacitances are a direct consequence of the area/layout of a device, such an investigation enables design engineers to optimize the size of their intended wide bandgap switching transistors, particularly as the number of applications requiring higher power devices continues to grow.

Circuit simulation models for GaN FETs have been reported in the literature [24, 25], however these models are still relatively immature in comparison to the advanced and well developed Si models. As a result, it is imperative for next generation power engineers to understand device modeling approaches for the current state of the art, so that potential improvements can be made on forth-coming technologies. This will enable one to analyze the potential benefits of the device both at the small-scale device level and at the large-scale systems level. Therefore, in order to develop a new wide bandgap device model, techniques for modeling the state of the art transistors at the small-scale device level as well as the large-scale systems level must be reviewed. The former is described in section 2.5 while the latter is discussed in section 2.6. A summary of chapter 2.0 is given in section 2.7.

2.1 WIDE BANDGAP

GaN and SiC belong to the class of wide bandgap semiconductors, which is defined as materials having a conduction-valence band difference (bandgap) of greater than 1.7eV. The bandgap for GaN and SiC is 3.4eV and 3.2eV respectively, in contrast to Si which has a bandgap of 1.12eV [26]. The high electron mobility of wide bandgap devices yields a smaller device specific on resistance than narrow bandgap devices. The small on resistance exhibited by wide bandgap devices leads to a significant reduction in the conduction losses in the power converters in which the wide bandgap device may be implemented. A wide bandgap device also has a comparatively stronger electric field which leads to a high device breakdown voltage thus making the device suitable for high power converters [27]. Also, the enhanced thermal conductivity of wide bandgap devices enables the device to cool down in a shorter amount of time after use in high power and high temperature applications. Furthermore, a wide bandgap material has smaller intrinsic carrier concentrations (n_i) than a narrow bandgap material at the same operating temperature. For example, GaN has an n_i value of 10^{-11} cm^{-3} whereas the n_i value for Si is approximately 10^{10} cm^{-3} . This allows the wide bandgap device to adequately sustain high temperature applications that which Si cannot [16, 27, 28]. For instance, in [29], a normally-off GaN FET was reported with operation at 250 degrees Celsius. In [30], a GaN FET was demonstrated to be operational in a 1000 deg. C vacuum. SiC transistors can withstand even higher temperatures than GaN. Silicon based FETs on the other hand degrade at temperatures beyond 150 degrees Celsius [29]. These observations make GaN FETs an excellent candidate to

be the primary switching device in power converters of photovoltaic systems where hazardous operating conditions are often observed.

2.2 BODY DIODE

Both GaN and SiC transistors have internal “body diodes” which can aid in their switching performance. For instance, in the fabricated GaN FET seen in Figure 2, there are no parasitic pn junctions which are commonly observed in traditional Si FETs. Due to the absence of parasitic pn junctions within the GaN FET, minority carrier (holes) conduction in devices is insignificant. Thus, in effect there is a body diode between the drain and source terminal of wide bandgap devices which inhibits the flow of hole-current from drain to source during the transistor’s off-state. The body diode of GaN FETs is shown in Figure 3 [31].

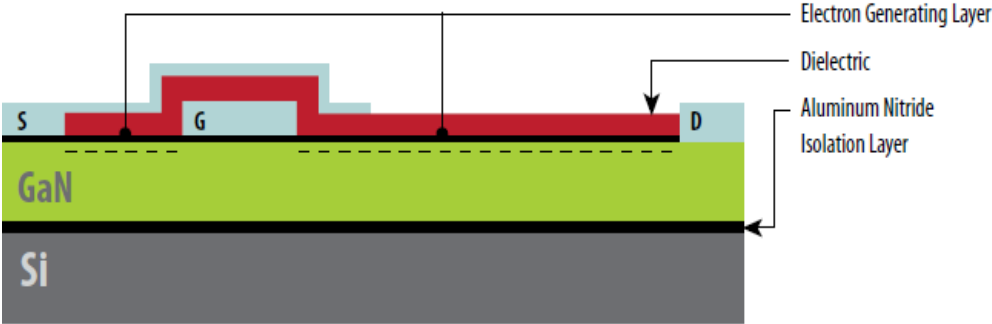


Figure 2: Structure of GaN power transistor [31].

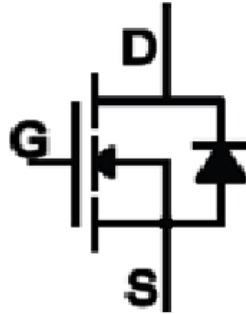


Figure 3: GaN body diode [31].

The lack of minority carrier conduction in GaN devices leads to nearly zero reverse recovery losses in power switching applications. Reverse recovery characteristics of diodes are illustrated in Figure 4. After the voltage switch occurs at -50 nanoseconds, the diode begins to gradually turn off as the current starts to fall. The diode current continues to decrease in the negative direction past zero, before ultimately reaching its “peak inverse” value. As seen in Figure 4, the peak inverse current for the Si device (black line in Figure 4) is approximately -5 amps at 25 nanoseconds. After reaching its peak inverse value, the current gradually climbs in the positive direction and reaches its steady state value of zero amps thus rendering the device completely off. From Figure 4, it is evident that the Si diode turns completely off more than 100 nanoseconds after the voltage switching occurred. On the other hand, as seen in Figure 4, both the GaN diode and SiC diode (red and blue lines respectively) turn completely off well with 100 nanoseconds of the voltage switch [32].

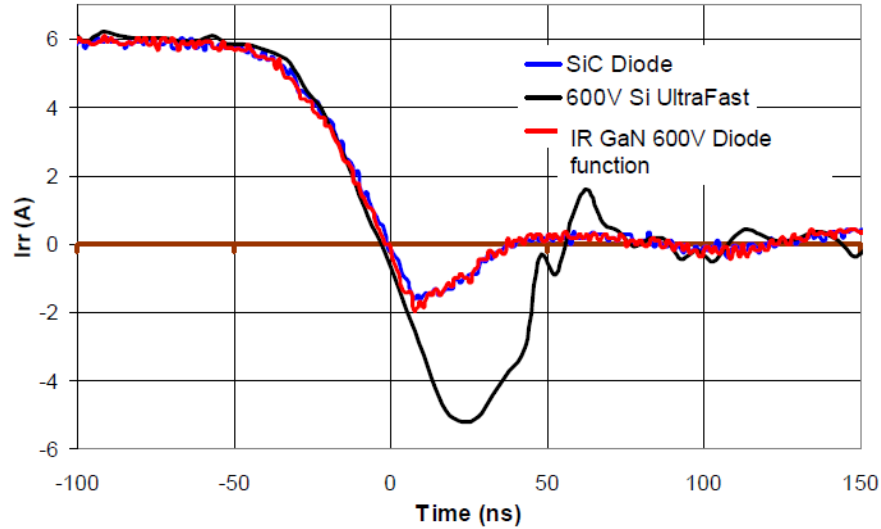


Figure 4: Reverse recovery comparison of GaN, SiC and Si diodes [32].

The time duration for the above described transitions should be ideally zero seconds. However in the case of the Si FET, a few nanoseconds are required for the minority carriers to return to the p-type material of the diode after the turn-off transition begins. Thus, Si FETs suffer from substantial reverse recovery losses. Since GaN/SiC devices have negligible minority carrier conduction, they suffer from insignificant reverse recovery losses [31-33]. This is potentially evident in Figure 4 by performing a calculus based integration of the area underneath the curve for each material's reverse recovery diode characteristic. By multiplying the result of this calculation by the applied diode voltage, the reverse recovery losses can be calculated. From Figure 4, it is given that the GaN, SiC and Si diodes are all 600V devices and therefore any disparity in reverse recovery losses between the materials is attributable to the difference in the area underneath the curve for each material's reverse recovery diode characteristic. Clearly, from Figure 4, there is considerably more area underneath the curve for the Si diode characteristic, which would thus exhibit significantly greater reverse recovery losses.

2.3 FIGURES OF MERIT

This sub-section of chapter 2 provides several FOM analyses which serve to benchmark current Si technology with next generation devices like GaN and SiC. The first FOM to be discussed is the derivation of the breakdown voltage versus cutoff frequency characteristic of recently reported and similarly rated GaN, SiC and Si devices. This characteristic gives an indication of each material's ability to sustain high frequency and high power switching applications. Next, the on resistance versus breakdown voltage FOM is discussed for GaN, SiC and Si. This FOM enables one to assess the potential conduction losses offered by each material in high power applications. The final FOM to be discussed is the on-resistance multiplied by gate charge characteristic. This FOM serves to balance the tradeoff for devices requiring smaller on-resistance and thus larger area, for which the consequence is higher parasitic capacitances and thus higher switching losses.

2.3.1 Breakdown Voltage vs. Cutoff Frequency Derivation

In the technology progression of GaN based microelectronics, the need for optimized high power radio frequency devices has been a pace-setter due to the funding available from the Dept. of Defense and the ability to rely on smaller area devices. A crucial attribute of radio frequency power devices is their breakdown voltage (V_{BD}) as a function of the associated cutoff frequency (f_T). In the following analysis, this characteristic was derived for recently reported and similarly rated GaN, SiC and Si devices. In each case, the reported data provided the transistor cutoff frequency versus the transistor gate length (L_G) characteristic. By utilizing the known JFOM for each material as well as other known device equations, the reported data was mathematically

manipulated in order to derive the breakdown voltage versus cutoff frequency characteristic. The forthcoming analysis demonstrates the mathematical manipulations required to obtain the breakdown voltage/cutoff frequency characteristic for devices with reported cutoff frequency /gate length characteristics.

The derivation begins with the JFOM – a key metric used to assess the high frequency performance of semiconductor materials. The JFOM is given in (2.0 -1) by: [34]

$$JFOM = \frac{v_{SAT} E_{BD}}{2\pi} \quad (2.0 -1)$$

Where V_{SAT} is the electron velocity in saturation and E_{BD} is the electric field at breakdown. A related equation from [34] stipulates that the breakdown voltage is related to the electric field at breakdown and the transistor gate length by (2.0 -2):

$$V_{BD} = \alpha \frac{L_G E_{BD}}{2} \quad (2.0 -2)$$

Where α is close to unity. Solving (2.0 -1) for E_{BD} and substituting in (2.0 -2) yields (2.0 -3):

$$V_{BD} = \alpha \pi \frac{L_G JFOM}{v_{SAT}} \quad (2.0 -3)$$

Also of relevance is that the transistor cutoff frequency is related to the above parameters through (2.0 -4) [34]:

$$L_G = \frac{V_{SAT}}{2\pi f_t} \quad (2.0 -4)$$

Combining (2.0 -3) and (2.0 -4) leads to (2.0 -5):

$$V_{BD} = \alpha \frac{JFOM}{2f_t} \quad (2.0 -5)$$

The relation in (2.0 -5) shows the inverse relationship between cutoff frequency and breakdown voltage as would be expected. In [35] and [36], the cutoff frequency/gate length characteristic is reported for two similarly rated Si and SiC devices, respectively. Using the derivation above, and the known JFOM for each material, the data reported in [35] and [36] can be mathematically manipulated to obtain the breakdown voltage/cutoff frequency for the two devices. This data can be compared with the data reported in [37] which depicts the breakdown voltage/cutoff frequency characteristic for a similarly rated GaN FET. The result of this analysis is given in Figure 5. The lines in Figure 5 include measured (solid) and extrapolated (dotted) characteristics for the three devices. As can be seen from Figure 5, at a cutoff frequency of 1 GHz, GaN has the potential of roughly 30 times greater operating voltage than Si with the advantage over SiC growing wider at lower frequencies. Here cutoff frequency is an indication of the maximum switching frequency that a transistor of a given size can operate at while

breakdown voltage is indicative of the maximum potential output voltage available from the transistor of that same size. Thus in general transistors with smaller breakdown regions have shorter distances for the electrons to travel thereby resulting in higher cutoff frequencies. While the cutoff frequency is a small signal parameter applicable to RF power amplifiers, the results in Figure 5 still offer a relative measure of how a particular material will perform in large signal power conversion schemes where operational frequency may be a fraction of the cutoff frequency.

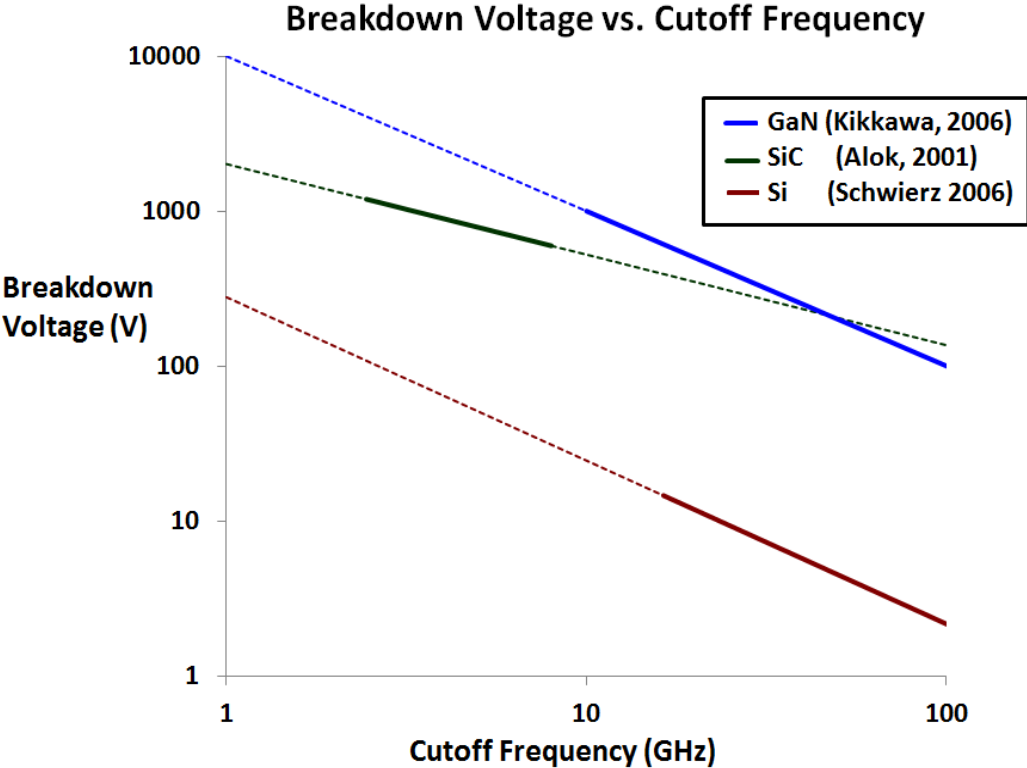


Figure 5: Breakdown Voltage vs. cutoff frequency for GaN, SiC, and Si

2.3.2 Specific On Resistance vs. Breakdown Voltage

Another standard FOM of importance is the specific on resistance (R_{on}) as a function of the device breakdown voltage. This FOM assesses the device's capability to maintain satisfactory conduction losses in high power applications. The current and projected on-resistance/breakdown voltage characteristics for the materials of interest are illustrated in Figure 6. As seen in Figure 6, the measured data points for GaN (red points) and SiC (maroon points) devices demonstrate significantly higher breakdown voltage than Si (blue points) at lower values of R_{on} [38].

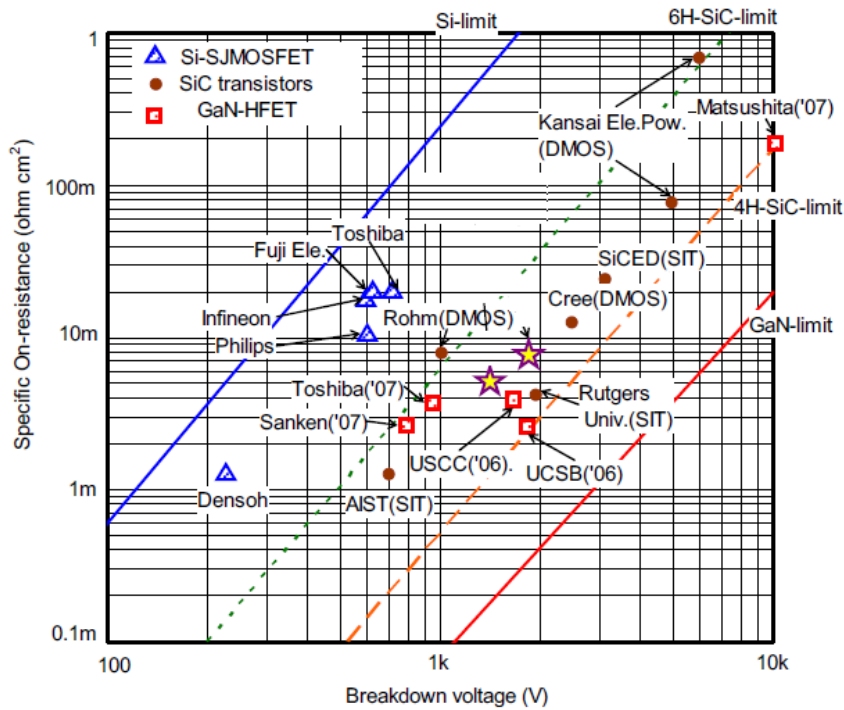


Figure 6: On resistance versus breakdown voltage for GaN, SiC and Si [38]

Also it is apparent from Figure 6 that the existing data points for SiC are approaching their physical theoretical limit (dotted red line). GaN devices, on the other hand have not yet reached their theoretical limit (solid red line). This demonstrates that GaN technology still has a significant upside potential with further device development to yield optimal device performance and hence enhanced power distribution in the future.

2.3.3 Product of Specific On-Resistance and Gate Charge

In power devices, it is important to balance the tradeoff between increasing (decreasing) the device width and consequently decreasing (increasing) the on-resistance and increasing (decreasing) the total device capacitance. The on-resistance plays a significant role in the conduction losses of the device in power converters, while the switching losses of the device in power converters can be mainly attributed to the device's capacitance [39, 40]. From this observation arises the following FOM which is the product of the device's on-resistance and its total gate charge. Essentially, this FOM assesses the optimal size of a device which can lead to switching and conduction losses that are as low as possible. Shown in Figure 7 is a comparison of this FOM for recently reported GaN and Si FET devices. Since the effects of both the on-resistance and device capacitance are to be mitigated as much as possible, a smaller FOM in this case is indicative of a superior device. As seen in Figure 7, the GaN FET is at least four times more superior than the best in class Si FET devices [40].

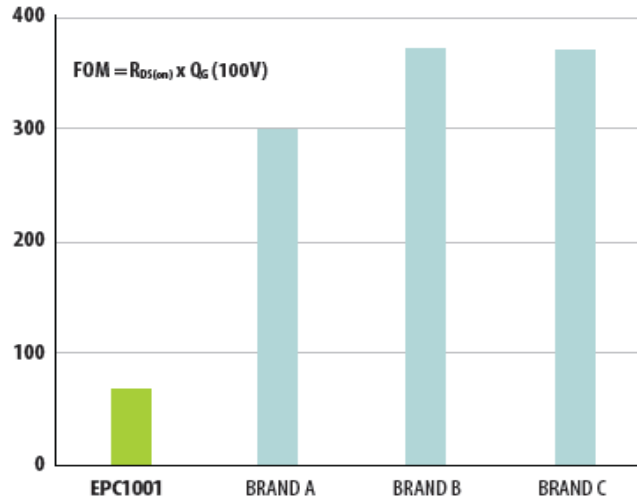


Figure 7: Product of R_{ON} and Q_G for GaN and best Si FET devices [40].

2.4 GALLIUM NITRIDE VS SILICON CARBIDE

While many of the metrics described above demonstrate a clear theoretical advantage for GaN over not only Si, but also SiC, there are still limitations that are preventing GaN from realizing its full potential. From the stand point of “technology readiness level”, SiC is in fact ahead of GaN, particularly for larger voltage devices. GaN transistors have been shown to suffer from the “punch-through” effect where electrons are traverse through the channel under the influence of high drain-source bias (transistor off-time) [41]. This can cause device failure. Additionally, GaN FETs are often grown on Si substrates for cost-effective reasons. The lattice mismatch between the two dissimilar materials can result in certain material defects. These material defects have been shown to create electron traps and thus degrade the performance of the device at high voltage [42]. SiC on the other hand suffers from this phenomenon less so, due to the fact that SiC

can be grown on SiC substrates. As a result, high voltage SiC devices are more advanced than high voltage GaN devices.

Furthermore, for applications requiring high temperature SiC has an advantage over GaN. This is because SiC has a higher thermal conductivity ($3.7 \text{ W/cm}^*\text{K}$) than GaN ($2.3 \text{ W/cm}^*\text{K}$). As a result, the SiC transistors can dissipate heat to the atmosphere better than GaN transistors.

Lastly, both GaN and SiC have smaller parasitic capacitances than Si. In general, smaller parasitic capacitances are an advantage since transistor switching times are reduced. However, smaller capacitances can induce certain dv/dt issues within the power converter. These issues will be explored for both GaN and SiC in the proposed dissertation. Thus, the proposed dissertation will include analysis of both GaN and SiC so that projections can be made for future larger generations of wide bandgap semiconductors.

2.5 DEVICE MODELING IN SABERRD

In [43], a 24 kW SiC power MOSFET from CREE is modeled in SaberRD. The device is a TO-247 packaged device, which permits DC parameter extraction from curve tracers and impedance analyses. As described in [43], in order to adequately simulate a device's switching performance in SaberRD, three essential characteristics must first be modeled: the I_D - V_{DS} output characteristic, the I_D - V_{GS} transfer characteristic and finally the nonlinear junction capacitances as a function of the drain to source voltage. The nonlinear junction capacitances are comprised of the input capacitances, C_{iss} , the output capacitance, C_{oss} and the reverse transfer capacitance, C_{rfs} .

These three capacitances are functions of the device's interelectrode capacitances, C_{GD} , C_{GS} and C_{DS} . Once these I-V and C-V characteristics of the SiC FET were obtained from a curve tracer and impedance analyzer, the following device parameters were extracted from the measured characteristics:

- specific on resistance, R_{on}
- the threshold voltage, V_{th}
- the channel length modulation parameter, LAMBDA
- the three interelectrode capacitances, C_{GD} , C_{GS} and C_{DS}

The experimentally measured data and the extracted parameters were then used to implement an equivalent SiC device model in the power semiconductor tool of SaberRD. Shown in Figure 8 is a comparison between the experimentally measured I_D - V_{DS} output characteristic and the modeled I_D - V_{DS} output characteristic of the SiC FET [43].

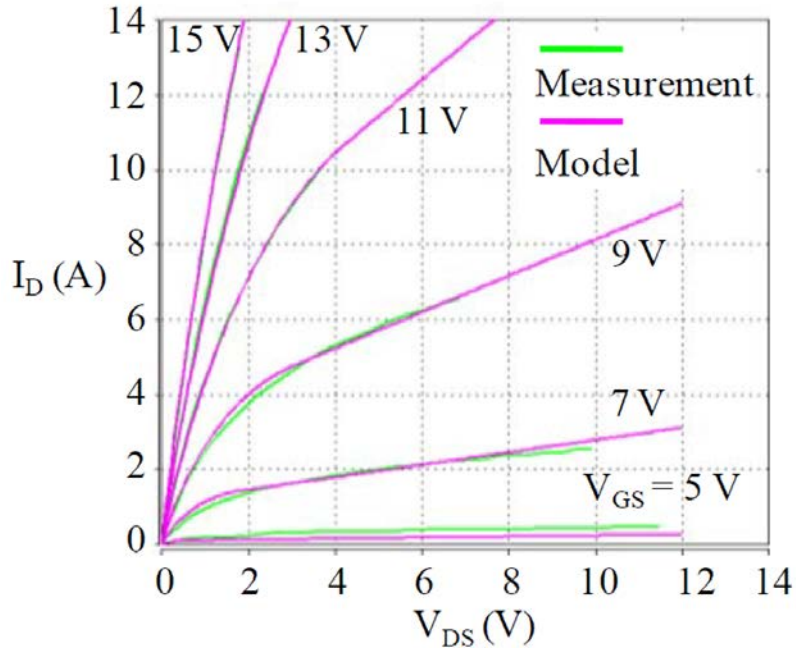


Figure 8: Measured and modeled I-V output characteristics of SiC MOSFET [43].

As can be seen from Figure 8, the measured and modeled I-V output characteristics show adequate agreement. In addition, the measured and modeled I_D - V_{GS} transfer characteristics were also compared and good agreement was obtained. Finally, the C-V measurements were also modeled and a comparison between the experimental results and the modeled results is shown in Figure 9 [43].

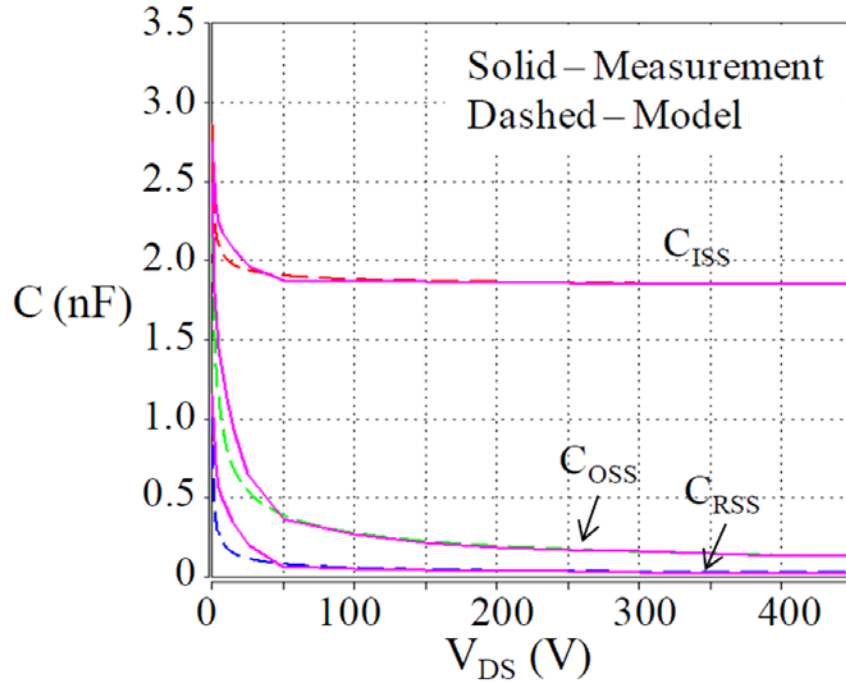


Figure 9: Comparison of measured and modeled C-V characteristics for SiC MOSFET [43].

In Figure 9, the solid lines are the measured data and the dashed lines are modeled data. Again, as can be seen from Figure 9, the measured and modeled results show relatively adequate agreement. These observations ensured the validity of the model. After the model was demonstrated to be valid, the actual test device and model were implemented and simulated in a standard switching test circuit known as the double-pulse tester shown in Figure 10. This circuit employs an inductor in parallel with a freewheeling diode at the drain terminal of the device. The inductance is specifically chosen so that the resulting time constant of the circuit enables the switching current and voltages to be captured on the oscilloscope [43].

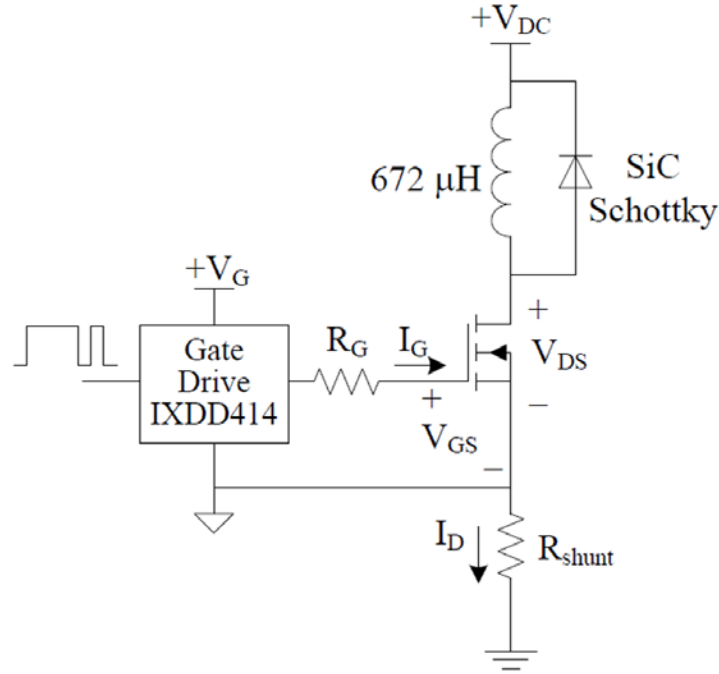


Figure 10: Standard switching test circuit, the double-pulse tester [43].

The freewheeling diode is implemented to eliminate the “reverse recovery effect” of inductive load circuits. When the FET turns off, the current through the inductor cannot instantaneously drop to zero. By employing the freewheeling diode in parallel with the inductor, an effective loop is created between the drain power supply, the inductor and the diode. Thus, when the FET turns off, the inductor current is dissipated through the drain power supply via the freewheeling diode which is forward biased when the FET is off. In effect, this eliminates the reverse recovery effect of inductive load circuits where large current spikes are often observed which hinders one’s ability to analyze the switching characteristics of the device only [43].

A comparison between the experimentally measured device turn-on switching characteristic and the simulated turn-on switching characteristic from SaberRD is shown in Figure 11. In Figure 11, the experimentally measured switching data is shown in black and the

simulated switching data is in color. As can be seen from Figure 11, good agreement is obtained in using SaberRD to simulate the switching behavior of the SiC device. Again, this agreement is obtained due to the accurate modeling of the device's I-V output and transfer characteristics in addition to modeling the device's C-V characteristics. The turn-off switching behavior was also simulated and compared with the experimentally measured data and again adequate agreement was obtained.

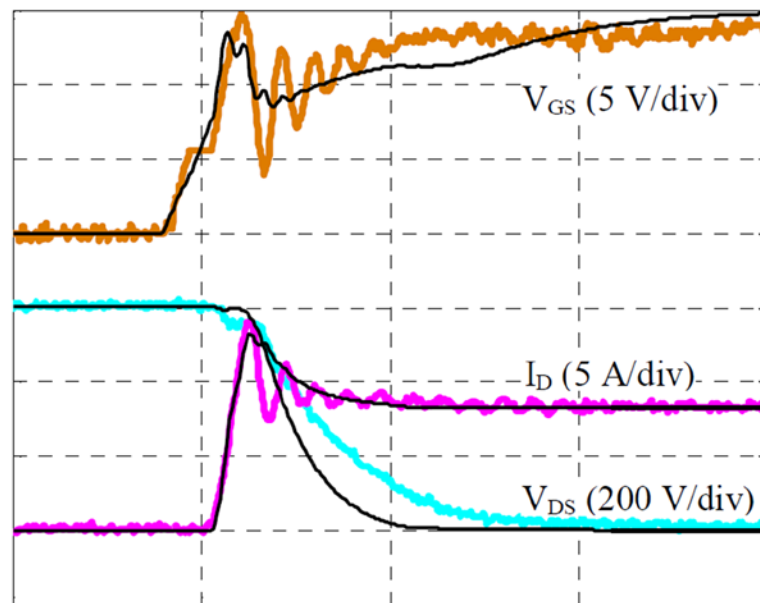


Figure 11: Measured (black) and simulated turn-on characteristics for SiC FET [43].

The observations from [43] indicate that SaberRD is a valid simulation tool for assessing the performance of power device models once the experimental characterization of the device is obtained. The authors of [43] reported similar modeling of SiC power devices in SaberRD [44, 45]. In addition, SaberRD has been used to model and simulate power semiconductors in various other references [46-48]. In [49], Shenai et al. used existing GaN and Si device data sheets to develop equivalent device models in SaberRD. To develop their models, the authors in [49] used

datasheets of GaN devices reported by Efficient Power Corporation (EPC) [50]. In addition, the authors of [49] proposed a novel enhancement mode GaN device model for benchmark analysis in SaberRD. Similar to the work previously described in [43], the on-resistance and parasitic nonlinear junction capacitors were among the pertinent parameters that were modeled in SaberRD in order to accurately reproduce the behavior of the devices [49]. The tabulated datasheet parameters used to create the model are seen in Figure 12. However, in [49] the authors did not use the power semiconductor device tool in SaberRD but rather the LEVEL 3 circuit simulation model in SaberRD. Once the GaN and Si models were created, they were simulated in a simple buck converter shown in Figure 13.

Device	V_{BR} (V)	V_T (V)	R_{ON} (m Ω)	C_{ISS} (nF)	C_{OSS} (nF)	C_{RSS} (pF)	Q_G (nC)
Best Commercial Silicon MOSFET	30	1.6	6	2.3	2	300	40
Best Commercial GaN E-Mode FET	40	1.4	4	1.3	1.2	200	30
Proposed GaN E-Mode FET	25	1	5	0.15	15	15	20

Figure 12: Datasheet parameters used to create circuit simulation models in SaberRD [49].

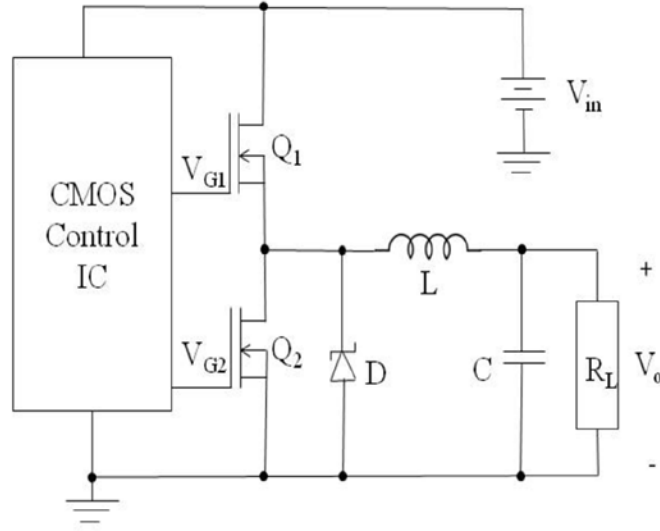


Figure 13: Buck converter benchmark analysis of datasheet driven GaN and Si models [49].

The frequency dependent-efficiency of the buck converter was then simulated for the GaN and Si models with the results shown in Figure 14. As can be seen in Figure 14, the efficiency of the GaN based buck converter is significantly greater than that of the Si based buck converter. This observation is noted when using either the proposed GaN FET model of [49] or the datasheet driven GaN FET model which was developed using datasheets from EPC. In the next section, previously reported approaches for system level simulations of device models are reviewed.

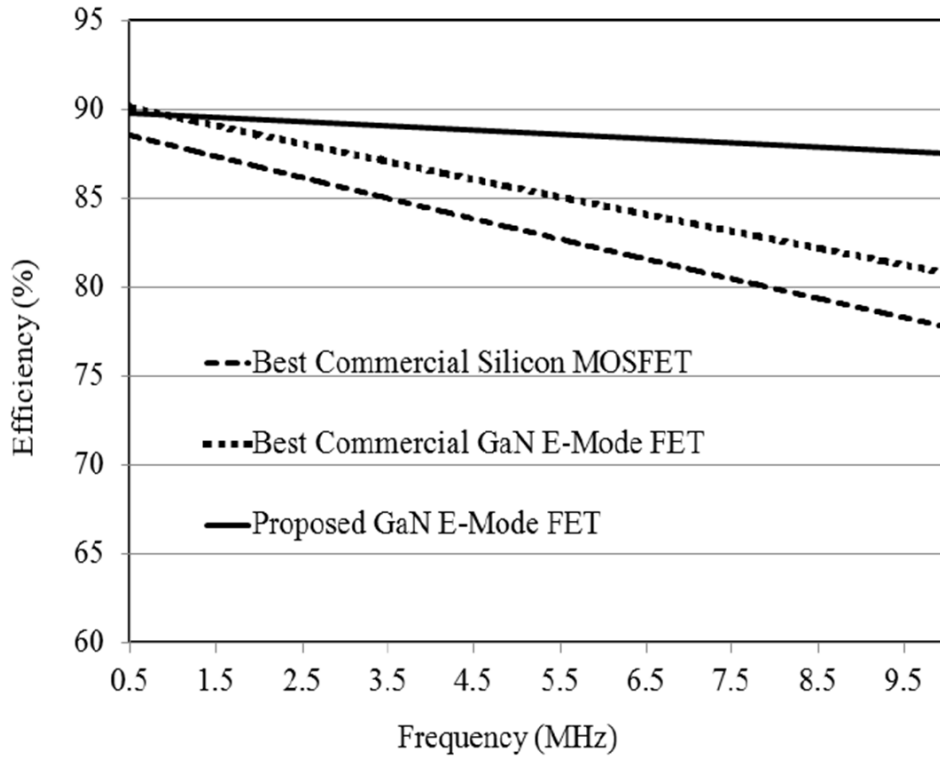


Figure 14: Frequency dependent efficiency of GaN/Si based buck converter in SaberRD [49].

2.6 SYSTEM LEVEL DEVICE MODEL IMPLEMENTATION

In the benchmark analysis of power device models, it is not only imperative to demonstrate the device’s benefits at the small scale “device level” but also at the large scale “systems level”. The system-based benchmark analysis previously described in [49] (see section 2.5) is quite simplistic. A buck converter is not indicative of the large and complex power systems that power devices are typically implemented in. Since significant losses at the system level can be attributed to the device, accurate device simulation in larger and more complex power systems is becoming a rapidly growing challenge [51-53].

While SaberRD is often used for modeling at the device level, electromagnetic transient programs like PSCAD are suitable for analyzing transient grid-level behavior of large and complex power systems. Furthermore, since the semiconductor device models in SaberRD can be physics based, large and undesirable CPU times are required for complex system level simulations of power electronics modules in SaberRD. In addition, PSCAD is appropriate for modeling and simulation of renewable energy systems like wind and solar power [54-56]. Recently, Rajapakse et al, reported on the limitations of PSCAD for modeling the switching losses in power semiconductor devices of power systems in [51] and [52]. These limitations arise due to the fact that switching events of power devices in power conversion schemes typically take a few hundred nanoseconds to complete. However, PSCAD uses a time-step in the tens of microseconds making it nearly impossible for the software to capture all the relevant switching data at the device level. In order to circumvent this apparent problem, Rajapakse et al. developed algebraic equations to “model” the current and voltage characteristics of the device during switching events. These equations were used to “fill-in” the missing data that PSCAD is unable to capture due to its large time-step. The equations were developed by measuring the switching current and voltage characteristic of an Insulated Gate Bipolar Transistor (IGBT) which was experimentally implemented in a physical switching test circuit. Shown in Figure 15 is a comparison between the measured turn-on of the device and the modeled turn-on using the developed equations for representing the current and voltage waveforms during the switching event [52]. The equations were developed by using linear approximations of the experimentally measured switching events depicted in Figure 15 (left). It should be noted that originally in [51], the developed equations matched the experimental data more precisely. However, this required

extremely complex equations and thus the work in [52] was developed in order to simplify the problem by using simple linear equations at the expense of precision.

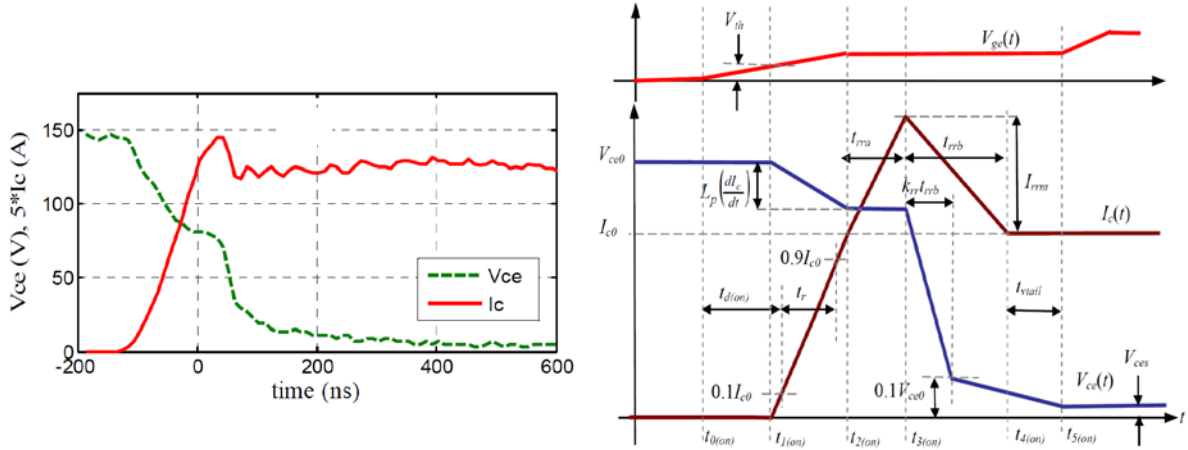


Figure 15: (Left). Measured IGBT turn-on [52]. (Right). Modeled IGBT turn-on [52].

As seen in Figure 15, the estimated turn-on (right) waveforms show reasonable agreement with the measured turn-on characteristic (left). The energy lost during the switching event is obtained by a calculus-based integration of the area underneath the curve where the modeled current and voltage waveforms overlap. Since the equations that represent the current and voltage transitions had already been derived, the afore-mentioned calculation is fairly straight forward. The calculus-based integration of the area-overlap between the current and voltage waveforms was then implemented into a loss estimation module which is compiled into PSCAD where the device is modeled mathematically in power conversion schemes. This process evades the previously described issue of PSCAD having too large of a time-step to capture relevant switching data at the device level. The loss-estimation module is depicted in Figure 16. As seen in Figure 16, the calculated “device loss model” is appended to the generic switch model that already exists in PSCAD. The flow-diagram method for device modeling in large scale

power systems seen in Figure 16 is not uncommon and has been used in various other references as will be demonstrated later. The flow type diagram allows the device to be interfaced with the rest of the electrical network which enables device models to be benchmarked against each other in larger and more complex power systems.

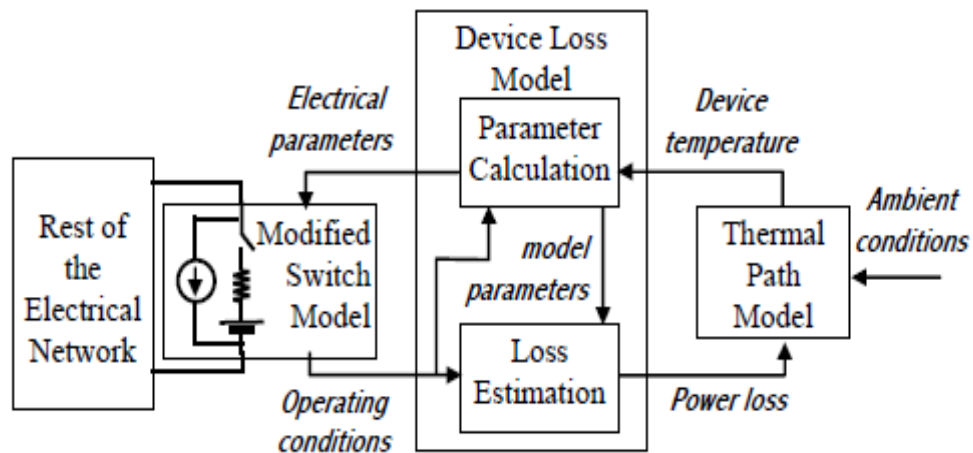


Figure 16: Loss estimation module implemented in PSCAD [52].

In [57] and [58] a slightly different approach was used for system level implementation of device models. In both works, a benchmark analysis is presented which compares SiC device models with Si device models in large wind farm systems. The wind farm and power conversion system used in [57] and [58] is shown in Figure 17.

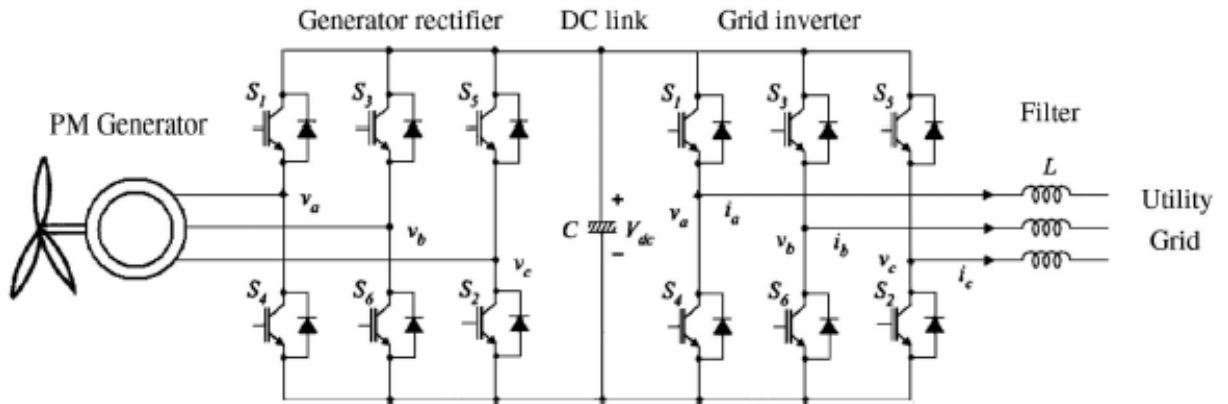


Figure 17: Wind farm power conversion system used in [57] and [58].

Each switch model seen in Figure 17 is a SiC “Device Model” characterized in the flow-type diagram seen in Figure 18. The device model is similar to the loss estimation module previously described in in [51] and [52] (see Figure 16 on page 35). However, this device model uses lookup tables to refer to the appropriate amount of switching and conduction losses as wind and environmental conditions vary.

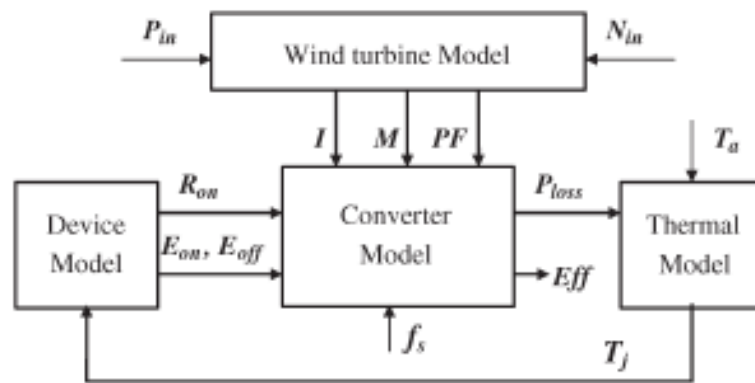


Figure 18: Flow diagram system used for modeling SiC and Si FETs [57, 58].

In Figure 18, the inputs to the system are the ambient temperature, the converter switching frequency and the input power which is dependent on the wind intensity of the

environment. The device model in Figure 18 is able to utilize these inputs to refer to previously programmed lookup tables in order to extract the appropriate switching loss and the on-resistance at the specified conditions. The lookup tables were implemented by measuring both the on-resistance of the device at varying temperatures as well as the switching losses at varying currents. For the on-resistance lookup table, the I_D - V_{DS} output characteristics were experimentally measured at varying temperatures as shown in Figure 19.

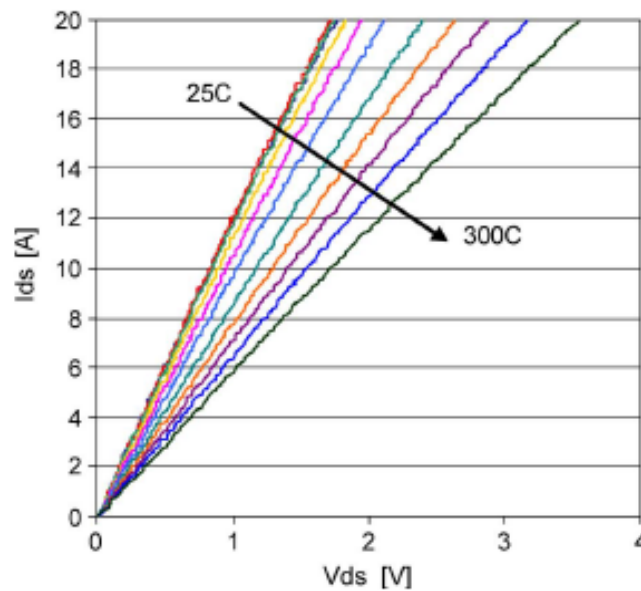


Figure 19: I_D - V_{DS} characteristic of SiC FET at varying temperatures [57, 58].

As can be seen from Figure 19, the slope of the I_D - V_{DS} output characteristic decreases with increasing temperature. Since the specific on-resistance of the SiC FET is inversely proportional to the slope of the I_D - V_{DS} output characteristic, the on-resistance increases with increasing temperature as seen in Figure 20.

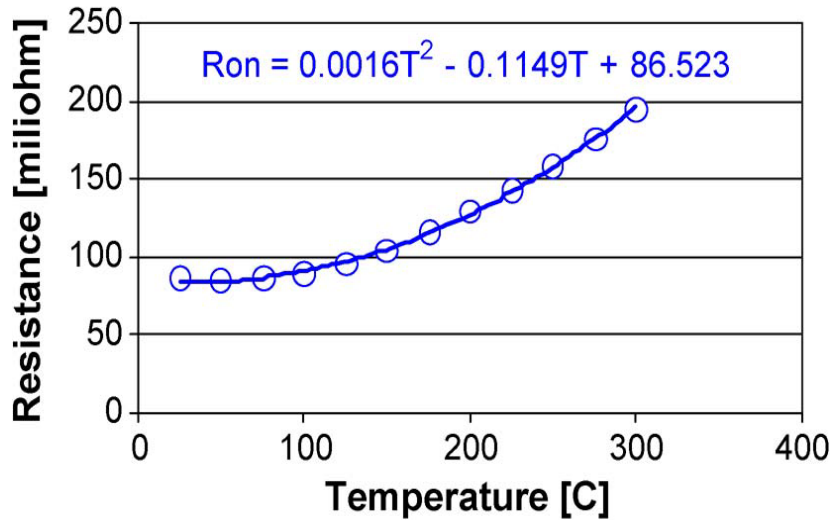


Figure 20: Change in on-resistance with changing temperature [57, 58].

From the data in Figure 20, a curve fitting algorithm was developed for implementation of the lookup table used in the device model of Figure 18 (page 36). In this manner, the appropriate on-resistance can be extracted from the lookup table as temperature varies. The on-resistance can then be used to calculate the conduction losses of the converter at the specified input power and temperature. The switching losses were also tabulated into the device model in a similar method. The switching losses of the SiC FET were experimentally measured at varying drain current levels as shown in Figure 21. The drain current of the SiC FET is dependent on the varying environmental wind speeds. As the wind intensity of the environment varies, the input power to the converter varies accordingly thus leading to different levels in drain current for the SiC FET. Thus, using the data from Figure 21, the lookup table is able to extract the appropriate amount of switching loss from the device model at the measured current.

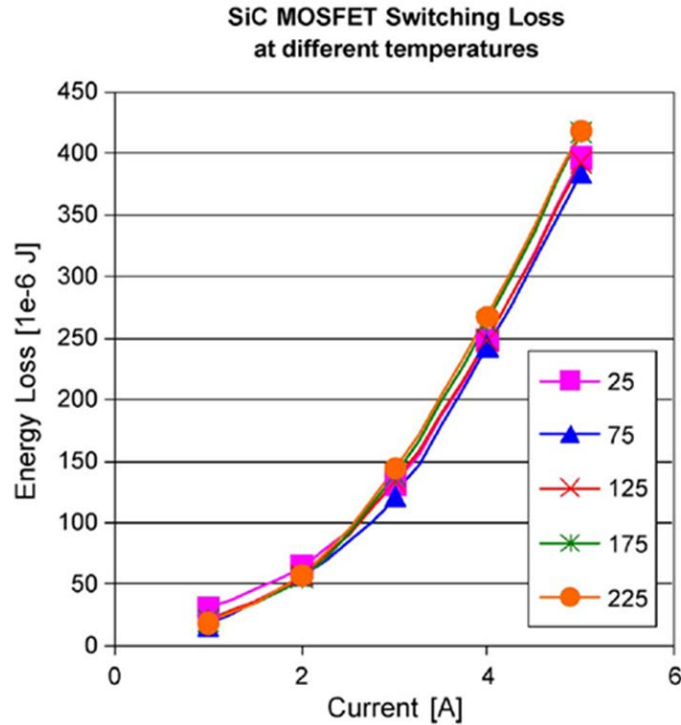


Figure 21: Change in switching losses with varying drain-current of SiC FET [57, 58].

2.7 SUMMARY OF CHAPTER 2

This chapter discussed the properties of GaN and SiC devices that make them an attractive alternative to Si switching devices in next generation power electronics. In section 2.1 the advantages of wide bandgap devices were discussed. These merits include, amongst others, the higher breakdown voltage of GaN/SiC devices, as well as their enhanced performance at high switching frequencies. In section 2.2, the body diode effects of GaN/SiC devices were discussed. The body diode effect of GaN/SiC devices is created due to the fact that GaN/SiC FETs are majority carrier devices. This quality of GaN/SiC devices allows them to demonstrate significantly lower reverse recovery losses than Si devices in power switching applications. In section 2.3 a comparative FOM analysis was given. These FOMs serve to assess and benchmark

the performance of GaN/SiC devices against Si in high switching frequency and high power applications. It was also demonstrated that SiC is ahead of GaN in terms of technological readiness. As a result, the proposed dissertation will analyze both SiC and GaN as potential alternatives to Si for next generation power electronics. Specifically, the stability of GaN and SiC in power electronic systems will be analyzed, due to the fact that both materials possess smaller parasitic capacitances.

Furthermore, in this chapter, a review of the literature for device model development and simulation at both the device and systems level was presented. At the device level, SaberRD has been used to accurately model the switching performance of SiC power MOSFETs. This required the modeling of the device's I-V and C-V characteristics. The device could then be simulated in switching test circuits and the simulation results were validated with experimental data [43]. System level simulation of devices in PSCAD requires the development of loss estimation modules based on experimental switching tests. These loss estimation modules allow the simulator to faithfully represent the switching loss of the device in large scale power systems, despite that PSCAD has too large of a time-step to capture switching events at the device level [51, 52]. Furthermore, a method for estimating the device's switching losses at varying environmental conditions was demonstrated. In the example given, a lookup table was used to extract the appropriate amount of switching loss from a SiC based power conversion system integrated with a windmill [57, 58].

3.0 RESEARCH PLAN FOR WBG DEVICES

This section of the dissertation outlines the statement of work to be accomplished for my PhD research. In the first section of this chapter, certain limitations associated with wide bandgap semiconductors are discussed. These limitations at the circuit level are what are currently preventing GaN and SiC from achieving their full potential for enhancing the performance of next generation power electronic systems. For example, the high dv/dt capability of GaN and SiC, though usually a beneficial aspect, can lead to certain undesirable transient phenomena such as “overshoot,” “ringing” and “false turn-on.” In the second section of this chapter, an outline of the modeling and characterization work that will diagnose and evaluate the impact of the aforementioned phenomena is presented. Behavioral and analytical models are proposed and subsequently developed to model some of these phenomena, so that design considerations can be made to mitigate their undesirable effects. In the next chapter, the current limitations with wide bandgap semiconductors are discussed. These are the limitations to be addressed in this dissertation.

3.1 LIMITATIONS WITH WBG DEVICES

3.1.1 Overshoot

Recently reported 100-volt and 200-volt GaN FETs [59, 60] from *Efficient Power Conversion*® (EPC) are typically operated at a steady-state gate-source voltage of 5 volts, which during device conduction yields a low on-resistance. This characteristic is shown in Figure 22, where it can be seen that at a gate-source voltage of 5 V, an on-resistance of just over 20 mΩ is obtained. Therefore, with 5 V applied to the gate of the transistor, the conduction losses of the power electronic converter can be significantly small.

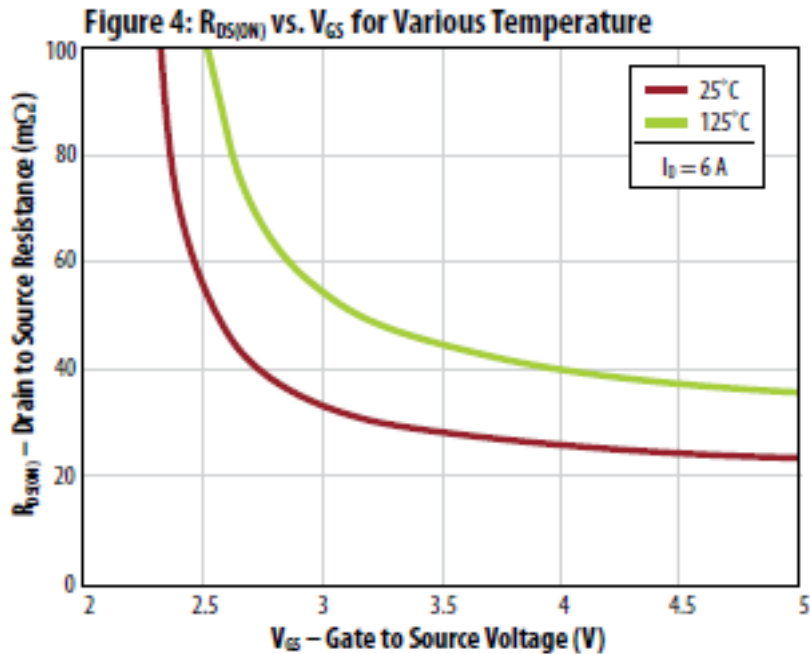


Figure 22: On resistance vs gate-source voltage for EPC2007 [59].

However, these devices have a maximum gate-source voltage of 6 V. Therefore, the safety margin for transient overshoot is a mere 1 volt. If the voltage on the gate exceeds 6 V, the device will fail, causing interruption in energy delivery. The very fast switching capability of GaN can often lead to excessive overshoot, which can be “damped” with external gate resistance. To illustrate this, consider the “gate-charging” circuit shown in Figure 23. This is the equivalent circuit of the GaN transistor while charging to conduction prior to reaching the threshold voltage. In Figure 23, v_{drive} represents the pulse width modulation source for turning the transistor on and off, L_{eq} is the equivalent loop inductance of the printed circuit board and device package (if applicable), and C_{eq} is the parallel combination of C_{gs} and C_{gd} , the gate-source and gate-drain capacitances, respectively.

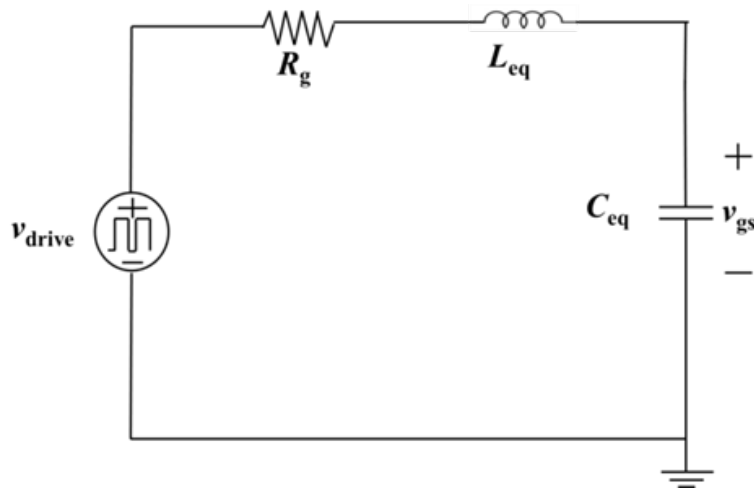


Figure 23: Gate charging circuit.

To understand the effects of the circuit parameters on transient characteristics such as overshoot, the transfer function from v_{drive} to v_{gs} can be considered:

$$\frac{v_{gs}(s)}{v_{drive}(s)} = \left[\frac{\frac{1}{C_{eq}L_{eq}}}{s^2 + \frac{R_g}{L_{eq}}s + \frac{1}{C_{eq}L_{eq}}} \right]. \quad (3.0 -1)$$

The denominator of the transfer function can be compared to the canonical form of a second order system:

$$s^2 + 2\zeta\omega_n s + \omega_n^2. \quad (3.0 -2)$$

Where ζ is the damping ratio and ω_n is the natural frequency: From inspection of the two expressions, it can be inferred that:

$$\zeta = \frac{R_{g1}}{2} \sqrt{\frac{C_{eq}}{L_{eq}}} \text{ and } \omega_n = \frac{1}{\sqrt{C_{eq}L_{eq}}}. \quad (3.0 -3)$$

The damping ratio provides information about how much the system overshoots its steady-state value before it finally settles, while the natural frequency determines the rate at which the system oscillates before it finally settles. When the damping ratio is less than 1, the system is underdamped and exhibits dramatic overshoot in its step responses. When the damping ratio is greater than 1, the system is overdamped and exhibits no overshoot, however with very slow convergence. When the damping ratio is equal to 1, the system is critically damped and exhibits optimized convergence time with no oscillation. The rate at which the system rises to its steady-state value is determined by the time constant, $R_g C_{eq}$. Thus a lower gate resistance leads to a faster rise-time, which can save the device from excessive switching loss. However, a lower gate resistance will lead to significant overshoot, which can damage the GaN device (recall the

small gate voltage safety margin). To damp the overshoot, a high gate resistance can be used, at the cost of slow convergence time and increased switching/gate-drive losses. To illustrate this, the circuit in Figure 23 was simulated using practical capacitance and inductance values for the EPC 2007 GaN device. The results are shown in Figure 24, where the gate-voltage is plotted as a function of time during turn-on. As can be seen in Figure 24, when R_g is 0.5Ω , there is significant overshoot above the maximum 6 V rating, thus likely causing harm to the device. However, the transistor channel (2-dimensional electron gas) is fully formed (“enhanced”) after approximately 0.6 nanoseconds – the time when the voltage reaches 5 V. At this gate-source voltage, channel conduction is maximum with minimum on-resistance as seen in Figure 22. When R_g is 1Ω , there is negligible overshoot, but the transistor is fully formed after 1 nanosecond. Finally, when R_g is 1.5Ω , there is no overshoot, and the transistor channel is fully enhanced after 1.75 nanoseconds. It is clear then, that a higher value of R_g is required to damp the overshoot on the GaN transistor, at the expense of slower convergence times, which can lead to higher gate-drive losses [61].

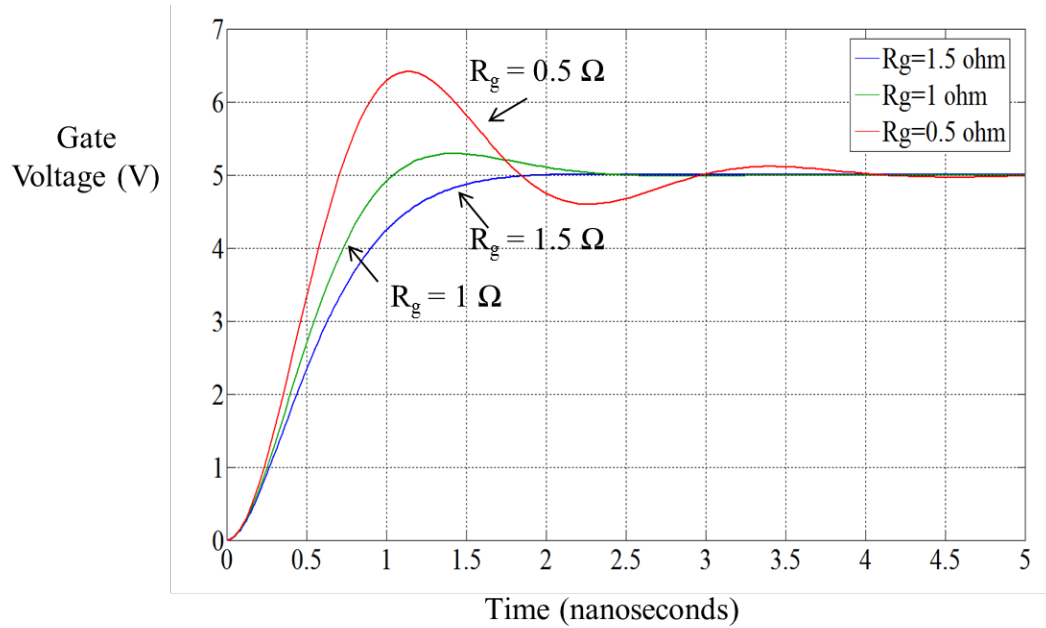


Figure 24: Gate voltage versus time at varying gate resistance.

In light of these observations, EPC devices are implemented with a chip-scale Land Grid Array (LGA) package, which reduces stray inductance and parasitic resistance [62]. This is because the lead-terminals of typical packages introduce significant inductance. From inspection of (3.0 -3), additional inductance would reduce the damping ratio, thereby leading to larger overshoot and thus damage the device. The disadvantage of the LGA device is that it is harder to implement in test circuits, often requiring a skilled professional for alignment bonding. The advantage of the EPC device is that it is a “normally-off” transistor, where a positive gate voltage is required to turn it on. This is a preference in power electronic applications because “normally-on” devices require external protection circuits to prevent device failure.

Another solution to the overshoot problem is to employ the GaN transistor in a “cascode” configuration, which was developed by *Transphorm* ®. The cascode configuration package is seen in Figure 25, while the cascode circuit is shown in Figure 26. In the cascode configuration,

a low voltage normally-off Si MOSFET is connected to the gate of a normally-on GaN HEMT as seen in Figure 26. The two transistor integration is treated as one overall normally-off device. In this configuration, the absolute maximum gate-source voltage is significantly higher than the preferred steady-state operating gate voltage, and thus overshoot does not harm the device. The *Transphorm* HEMT can thus be implemented in the classic TO-220 package, which is easy to use in test circuits. The disadvantage of this particular configuration is the added capacitance of the Si MOSFET, which makes the device slower, thus increasing switching losses.

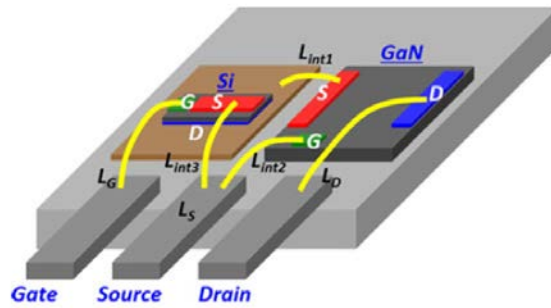


Figure 25: Package cascade configuration of Transphorm GaN FET [63].

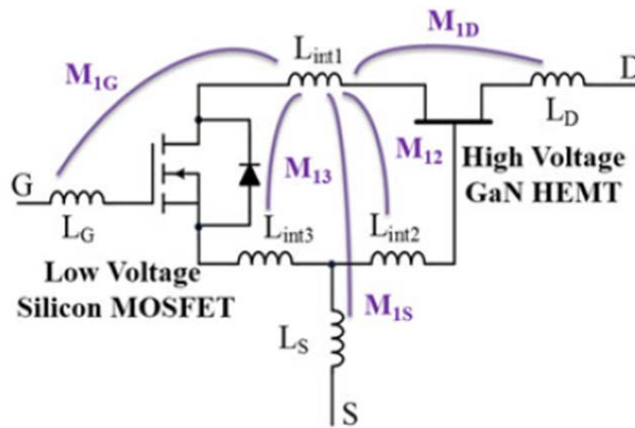


Figure 26: Circuit model for cascode configuration of Transphorm GaN FET [63].

It should be noted that the overshoot problem is specific more to WBG devices than Si devices. The reason for this is two-fold. First, WBG devices have a lower capacitance to inductance ratio, therefore resulting in more overshoot as can be inferred from inspection of (3.0-3). In Si devices, this ratio is higher, and therefore overshoot is rarely observed. While a low capacitance to inductance ratio is typically a beneficial aspect, it is demonstrated here that it can have certain disadvantages as well. Second, the oxide layer in the gate of the Si structure does not breakdown as easily as the dielectric material in WBG devices, and therefore the absolute maximum ratings for Si devices are higher. Consequently, even if overshoot is observed in an Si device, minimal damage would occur.

3.1.2 Ringing

Another potential problem affecting wide bandgap semiconductors is the loss associated with “ringing.” This phenomena is observed when the various signals throughout the transistor continue to fluctuate at steady-state, which can cause switching and conduction loss. An example of excessive ringing is shown in Figure 27, taken from [64]. It was shown in [64] that a SiC MOSFET in a half-bridge power conversion circuit will exhibit significant ringing. As seen in Figure 27, during device turn-off, the drain-source voltage (V_{DS}) rises as the drain-current (I_D) falls, and both signals oscillate or “ring” for 9.4 μ s. Typically, the time required for voltages and currents to reach steady-state values are typically tens of ns. However, due to the low capacitance of the SiC MOSFET in [64], a resonant frequency is excited thus leading to the observed oscillations in Figure 27. Again, from inspection of (3.0-3), the natural frequency, ω_n of WBG based power conversion circuits will tend to be higher than Si based circuits, due to the low capacitance of WBG devices. This is why ringing can be observed more often in WBG

devices. The type of oscillatory modes seen in Figure 27 can cause unstable behavior in the power converter, and potentially damage the device. These oscillatory modes have been shown to self-excite in SiC based power conversion circuits [64].

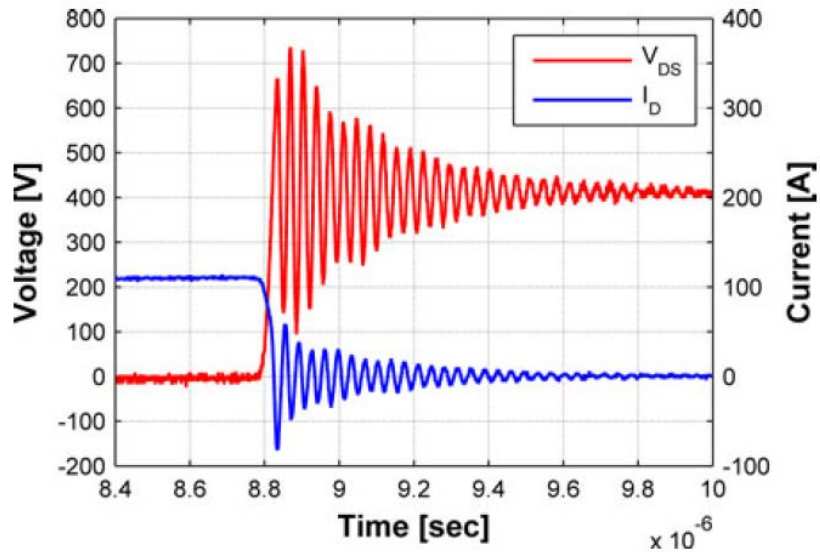


Figure 27: Ringing in SiC MOSFET [64]

3.1.3 False Turn-On

Finally, due to the very fast switching capability of WBG devices, high dv/dt is often observed in power conversion circuits using GaN or SiC FETs. When the dv/dt becomes too high, transistors have been shown to turn-on spuriously during the expected off-time in circuits containing multiple switching devices. To illustrate this, consider the off-state model of a transistor shown in Figure 28. Since the transistor is off, there is no channel between its drain and source terminals. If a high dv/dt is imposed on the drain terminal of the circuit in Figure 28 (due to the rapid turn-on/off of another transistor in the power conversion circuit), a large current would be injected through the gate-drain capacitance, C_{GD2} . Consequently, a current would flow across the external gate-resistance of the transistor, R_{G2} . The resulting voltage across the gate and source

terminals could force the device to turn-on, despite that the driving signal on the device is effectively at ground potential. This is called “false turn-on,” where the device turns on when it was not supposed to. False turn-on can lead to significant switching losses throughout the power conversion circuit. This is again a problem potentially seen more in WBG power conversion circuits, where fast switching times and high dv/dt are often observed.

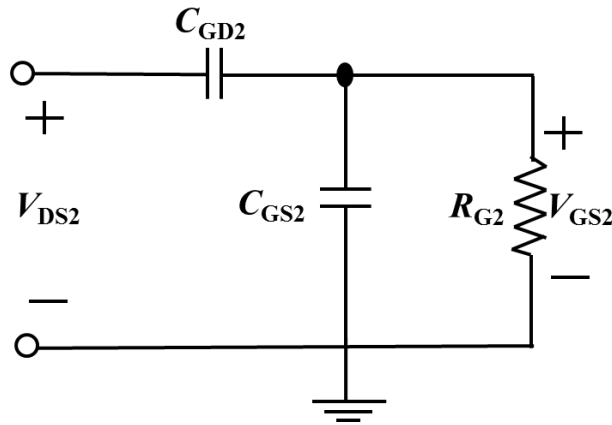


Figure 28: Off-state transistor model.

3.2 RESEARCH PLAN OUTLINE FOR WBG DEVICES

The goal then of this dissertation is to develop models which can characterize the phenomena affecting WBG devices described above. These models will enable design engineers to develop modification techniques in the design and fabrication of next generation power semiconductor devices. In Chapter 4.0 behavioral GaN device models are developed using SaberRD (*Synopsys*). The models are validated against existing experimental data, published by *EPC*. The device models are then implemented in a switching test circuit under the influence of varying parasitic capacitance conditions. The switching losses are measured in simulation under all these variable conditions. This analysis enables one to determine which parasitic capacitance has the most

detrimental impact on the switching performance of GaN FETs. The models developed in Chapter 4.0 are based on 100 V and 200 V GaN devices. As such, certain trends in the results seen in Chapter 4.0 can be used to project the performance of a 600 V GaN device that EPC may develop in the near future. The research in Chapter 4.0 was presented at the *2012 IEEE Energy Conversion Congress and Exposition* in Raleigh, North Carolina [65].

In Chapter 5.0 a test power conversion circuit is used to characterize the overshoot, ringing and false turn-on behavior in a SiC MOSFET. The effect that each parasitic capacitance has on the damping of the drain-source voltage is investigated extensively, both analytically and experimentally. In addition, the effect that each capacitance has on the magnitude of the induced gate-source voltage during false turn-on is also studied both analytically and experimentally. The research in Chapter 5.0 was presented at the *2013 IEEE Applied Power Electronics Conference* in Long Beach, California [66].

Chapter 6.0 presents new insights on false turn-on in synchronous buck converters using a SiC MOSFET. An analytical state space model is developed, which consists of equivalent circuits for the two MOSFETs in the converter. The output of the model is shown to closely predict experimental waveforms for various signals in the converter during the instance of false turn-on. The complex interactions between both devices are modeled in detail, showing how the impedance of one MOSFET can affect the switching behavior of the other. As the adoption of faster wide bandgap semiconductors becomes more pervasive, the model presented in Chapter 6.0 can be used by design engineers to mitigate the detrimental transient high dv/dt effects often demonstrated by next generation power electronic devices.

The models presented in this dissertation provide a foundation for design engineers to utilize in order to mitigate the current detrimental behavior of WBG devices. This will allow WBG devices to realize their full potential of enhancing next generation power electronic systems.

4.0 EFFECTS OF PARASITIC CAPACITANCES ON GAN HFETS

Resulting from the review of the limitations with WBG devices discussed in Chapter 3.0 , was the need to understand the effects of the parasitic device capacitances on the switching performance of next generation wide bandgap devices. Understanding the effects of the parasitic capacitances enables one to determine their influence on the dynamic behavior of power electronic circuits. In this chapter, the parasitic capacitances of GaN have been evaluated in order to assess the impact that each capacitance has on the switching losses of GaN devices. This required developing and validating equivalent GaN HFET device models in SaberRD and implementing the models in a switching test circuit under variable parasitic capacitance conditions. The data presented here can facilitate optimizing the area and hence capacitance of GaN devices for future generation power electronics.

4.1 INTRODUCTION

The Gallium Nitride (GaN) Heterostructure Field Effect Transistor (HFET) poses as a potential improvement to the current technological limitations associated with switching devices for power

electronics. Due to its wide bandgap of 3.4eV, GaN devices can sustain relatively adequate performance under high switching frequency and high temperature applications [1]. Despite its promising future, GaN technology is still relatively immature in terms of its technological readiness level, particularly for larger high voltage devices. Further development work is required on GaN in order for it to achieve its full array of capabilities for enhancing future generation power electronics [2]. In this work, the effect of the parasitic capacitances on the switching performance of GaN devices is evaluated. Since the parasitic capacitances arise from the area/layout of a device, this investigation will aid design engineers in optimizing GaN devices for applications requiring larger operating voltage and higher current devices.

In power conversion applications, the semiconductor device serves as a switch of considerable current and voltage. Thus, the transient switching behavior of these devices is an important parameter that affects their high power performance, specifically power conversion efficiency. The parasitic nonlinear junction capacitances substantially influence the transient turn-on and turn-off behavior of a power switching device. The critical capacitances include the input capacitance C_{ISS} , the output capacitance C_{OSS} , and the reverse transfer capacitance C_{RSS} . For the FET devices under consideration, these capacitances are related to the device's internal physical capacitances as shown in (4.0 -1)-(4.0 -3) [44]:

$$C_{ISS} = C_{GS} + C_{GD} \quad (4.0 -1)$$

$$C_{OSS} = C_{DS} + C_{GD} \quad (4.0 -2)$$

$$C_{RSS} = C_{GD} \quad (4.0 -3)$$

Here C_{GS} , C_{GD} , and C_{DS} are the gate-source, gate-drain, and drain-source capacitances respectively. Several reports from the literature have proposed various methods of analyzing the effects of these capacitances on the switching performance of power devices. In [23], Xiong et al. developed a novel methodology for assessing the dependence of C_{OSS} on the switching losses of a virtual Silicon (Si) MOSFET using circuit simulation. In [5], a gate drive circuit was proposed to evaluate the dependence of C_{ISS} on a GaN power MOSHFET's switching losses. In [49], Shenai et al. developed datasheet driven GaN and Si models in SaberRD (Synopsys) [6] to benchmark device model performance in a buck converter. The parasitic capacitances were amongst the pertinent datasheet parameters used to develop the models. In addition, SaberRD has been used to develop and simulate power semiconductor device models in various other references [45-48]. For this work, SaberRD has been utilized to develop GaN models in order to present a graphical depiction between all the parasitic capacitances and their individual relative effects on the turn-on and turn-off losses of GaN HFETs. Furthermore, a discussion on the physical location of the GaN capacitances within the GaN HFET structure is provided here, in conjunction with a theoretical discussion on the potential beneficial/parasitic tradeoffs that each capacitance may contribute in power conversion applications.

Due to their available datasheets, two commercially available eGaN® HFETs from Efficient Power Conversion Corporation (EPC) [50] were chosen in order to evaluate the individual effect of all the parasitic capacitances on the GaN HFET's turn-on and turn-off switching performance. This analysis required developing equivalent device models of the EPC GaN HFETs in SaberRD and comparing the simulated behavior of the device models with EPC's published datasheets [59, 60]. To develop the models, an approach was used similar to the one reported by Z.Chen et al. in [43] where a 24kW Silicon Carbide (SiC) MOSFET was modeled

using SaberRD. The analysis of the modeled results to be presented here suggests which capacitances are most critical in the optimization of future higher power GaN devices.

The rest of this chapter is organized as follows: Section 4.2 provides a background discussion on the parasitic capacitances of GaN HFETs as well as their location within the GaN HFET structure. Section 4.3 describes the methods used for developing and validating GaN HFET models in SaberRD in order to evaluate the effect of each parasitic capacitance on the switching performance of GaN devices. Results and discussion are given in Section 4.4 followed by concluding remarks in Section 4.5.

4.2 GAN CAPACITANCE CHARACTERISTICS

Figure 29 shows the EPC GaN HFET structure and the locations of the terminal capacitances within the device structure. The lateral (effectively planar) device structure seen in Figure 29 has the effect of lowering the spatial charge of the GaN HFET. This enables the device to operate with higher switching frequencies often in the megahertz range. As depicted in Figure 29, C_{GS} is the effective capacitance of the device seen from the “channel” (formed by two-dimensional electron gas) to the field plate on top of the gate terminal, while C_{DS} is the effective capacitance between the drain terminal (continuation of source contact across gate) and the field plate. Finally, C_{GD} is located in a small portion of the gate terminal and is also smaller in size relative to C_{GS} and C_{DS} [31].

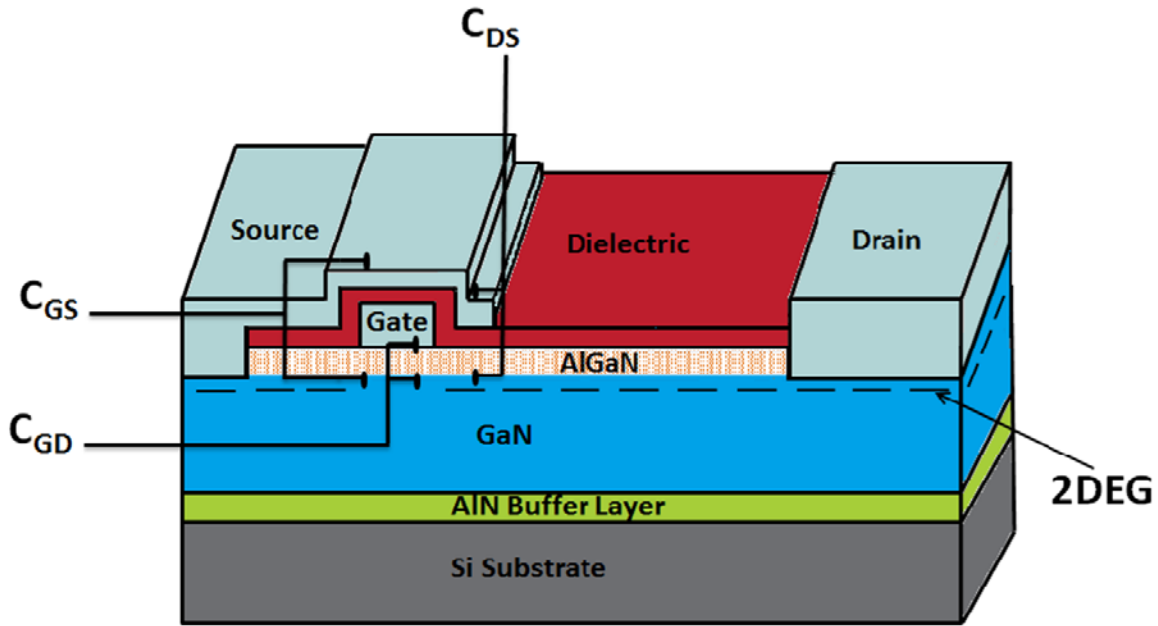


Figure 29: Cross section of EPC GaN HFET.

As described in [31], since C_{GS} is larger than C_{GD} in the GaN HFET, the device is relatively less susceptible to undesired transient dv/dt voltage spikes on the transistor's gate terminal. These transient voltage spikes have been demonstrated to induce false turn-on for devices of other materials. The issue of large dv/dt induced false turn-on for power devices has been discussed in various references from the literature [21, 67, 68]. In synchronous buck converters as well as other power converters containing multiple switching devices, a second FET Q_2 , is used to replace the conventionally used diode in order to reduce the overall conduction losses of the converter. However, if Q_2 suffers from false turn-on due to large dv/dt , the switching losses of the converter can increase significantly.

To illustrate the mechanism of false turn-on, a synchronous buck converter is shown in Figure 30. False turn-on of Q_2 can occur when Q_1 is switched on which leads to a large dv/dt on C_{GD} of Q_2 (C_{GD2}). For illustrative purposes, the physical capacitances, C_{GD2} and C_{GS2} are shown in Figure 30 for Q_2 , but not for Q_1 . The large dv/dt on C_{GD2} induces a current through C_{GD2} which in

turn leads to a current through the gate resistor, R_{G2} . It should be noted that during these transitions the gate voltage on Q_2 should be zero because Q_2 is supposed to be off, however the induced current through R_{G2} forces a positive gate voltage on Q_2 . If this induced gate voltage exceeds the threshold voltage of Q_2 , the device is forced into conduction spuriously, leading to significant power losses. False turn-on of Q_2 can be avoided if one considers the circuit shown in Figure 31, which is the equivalent circuit for Q_2 when Q_1 is turning on and therefore the gate-pulse on Q_2 is zero or effectively grounded [69].

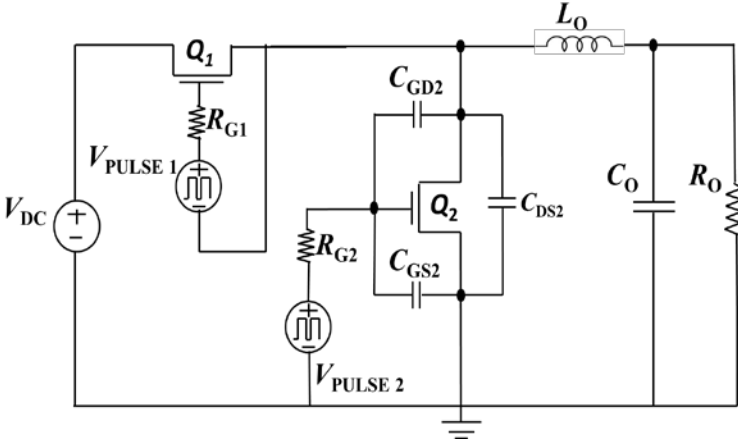


Figure 30: Synchronous buck converter.

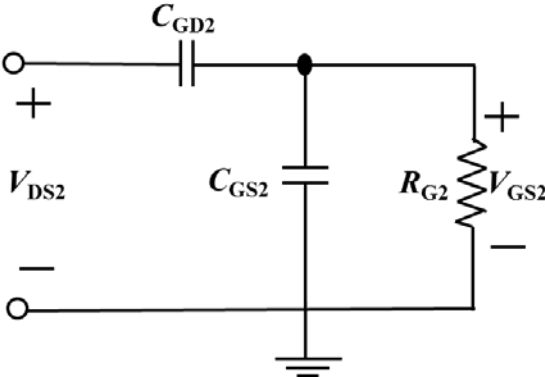


Figure 31: Q_2 in its off-state.

The transfer function for the circuit shown in Figure 31 is given in (4.0 -4) below:

$$\frac{V_{GS2}}{V_{GS2}} = \frac{sR_{G2}C_{GD2}}{1 + sR_{G2}(C_{GD2} + C_{GS2})} \quad (4.0 -4)$$

Where $s = j2\pi f$, and f is the frequency associated with rise times. In order to avoid false turn-on of Q_2 , the left hand side of (4.0 -4) should be as small as possible so that the value of V_{GS2} does not exceed the threshold voltage of Q_2 , a normally off device. In analyzing (4.0 -4), it is clear that low values of C_{GD2} make the left hand side of (4.0 -4) smaller. It can also be deduced from (4.0 -4) that high rise time frequency operation (hundreds of kilohertz) may increase the possibility of false turn-on unless C_{GS2} is designed to be sufficiently large enough.

This observation points to the crucial need to optimize the value of C_{GS} in GaN power HFETs. Since GaN devices are faster than Si based FETs due to their smaller intrinsic capacitances, it follows that GaN devices must be designed so that C_{GS} is large enough to avoid false turn-on in high rise-time frequency synchronous buck converters, and yet small enough so as to not adversely affect the switching speed of the converter (the authors are currently investigating this topic). Indeed as reported in [31], C_{GS} for GaN is larger than C_{GD} , however C_{GS} for GaN is still smaller relative to Si MOSFETs, which allows GaN power switching devices to exhibit shorter delay times in power switching applications.

In the next section, the methodology used for developing and validating GaN device models in SaberRD is described. These models are used to assess the impact that the above described capacitances have on the switching performance of 100V and 200V GaN HFETs. Such an analysis could aid in projecting the performance of larger area and higher voltage GaN devices,

while also providing further insight on the individual effect of each capacitance on the switching performance of GaN HFETs.

4.3 METHODOLOGY FOR MODEL DEVELOPMENT AND VALIDATION

Shown in Figure 32 is the circuit model for the power semiconductor tool in SaberRD which was used to simulate the performance of the GaN HFETs. The model in Figure 32 shows reasonable agreement with other equivalent circuit GaN models recently reported for power conversion [24, 42].

To develop the GaN device models, two commercially available GaN HFETs were chosen, the EPC2007 and the EPC2010 which are 100V and 200V devices respectively [59, 60]. The forthcoming analysis demonstrates the method used for developing the EPC2007 model as an example. The same development was undertaken for the EPC2010 which enabled a comparative analysis between the two devices. As described by Z. Chen et al. in [43] for SiC MOSFETs, in order to accurately simulate a device's switching performance, four essential characteristics must be modeled: the I_D - V_{DS} output characteristic, the I_D - V_{GS} transfer characteristic, the body diode characteristic and finally the nonlinear junction capacitances as a function of the drain-source voltage. Using the power semiconductor tool in SaberRD, the output and transfer characteristics of the EPC2007 were modeled. Shown in Figure 33 are comparisons between the datasheet reported I-V output and transfer characteristics of the EPC2007 and the modeled versions at 25 degrees Celsius. As seen in Figure 33, adequate agreement was obtained for modeling the I-V output and transfer characteristics of the EPC2007. Distinct areas of commonality between the datasheet and models are highlighted with circles for ease of comparison.

Next, the dependence of the drain-source voltage on the parasitic nonlinear junction capacitances was modeled as well as the body diode characteristic. A comparison between the capacitance-voltage characteristics and body diode characteristic of the device's datasheet and the modeled versions are shown in Figure 34. Again, good agreement was obtained for modeling these characteristics.

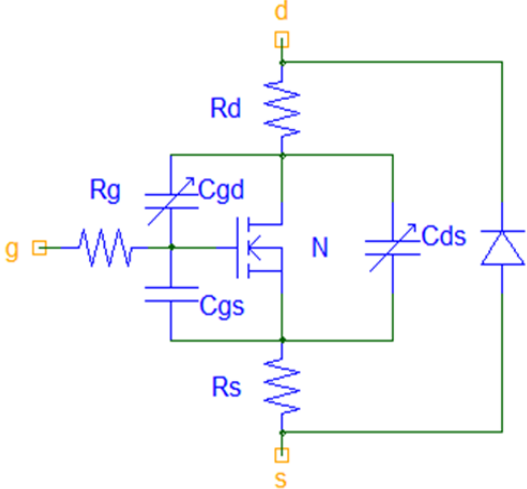


Figure 32: SaberRD semiconductor model.

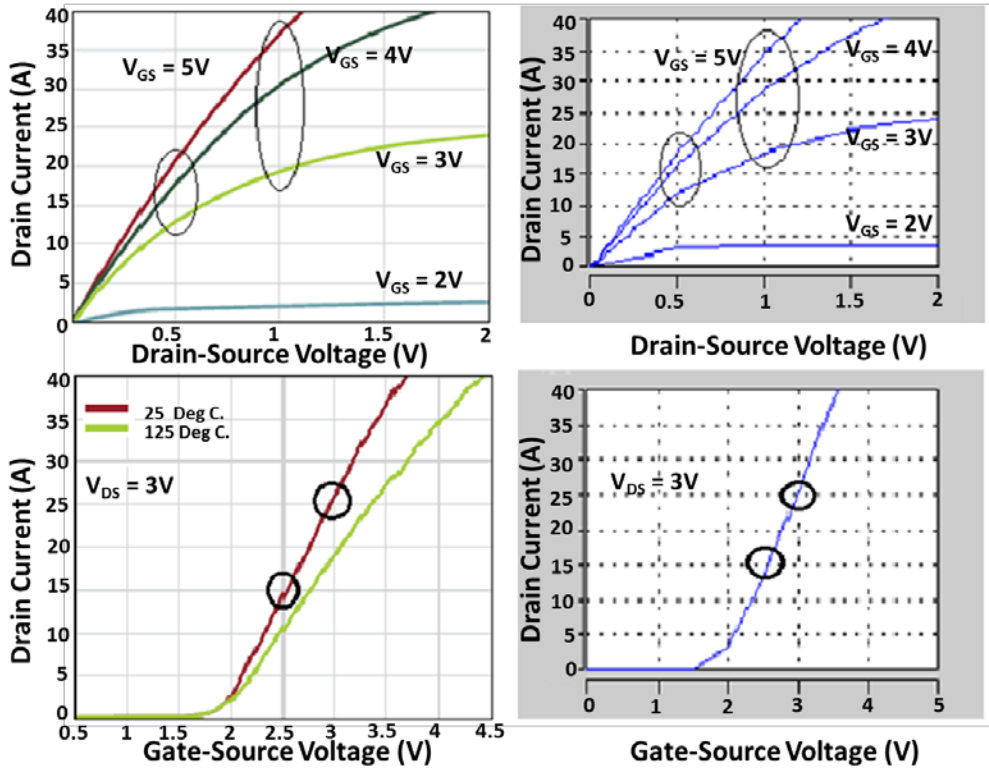


Figure 33: IV comparison between datasheet (left) and model (right).

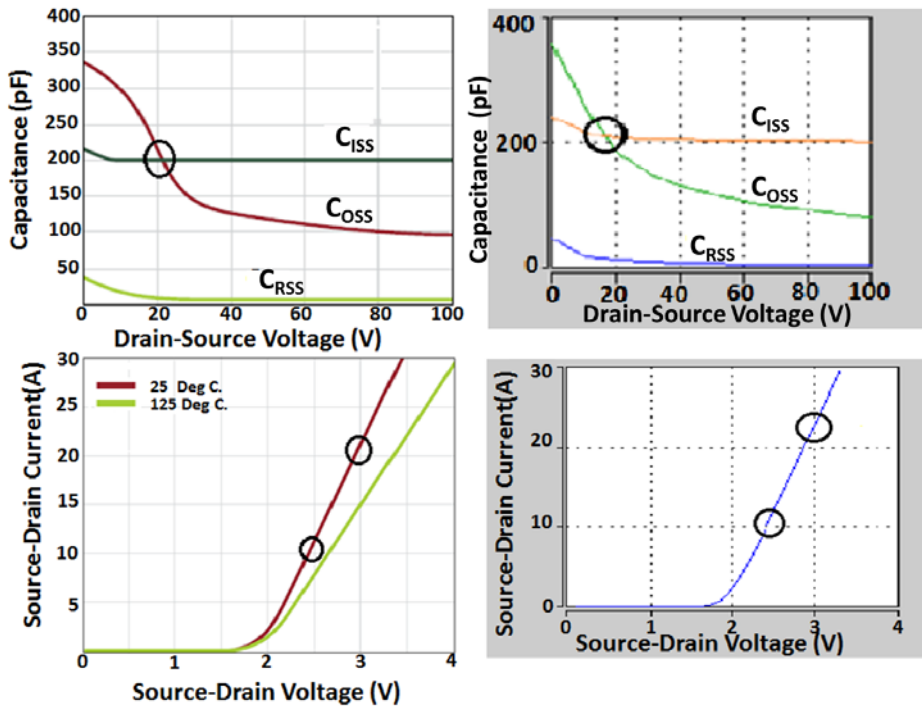


Figure 34: (Top). C-V characteristics comparison. Body diode characteristics (bottom).

Having modeled the appropriate I-V and C-V characteristics for the EPC2007, the validity of the model was ensured in two manners. First, the gate charge characteristics of the device model were simulated and compared against the published experimental gate charge characteristic shown on the datasheet [59]. This comparison is shown in Figure 35. As can be seen from Figure 35, at the proper test condition of $I_D = 6A$ and $V_{DS} = 50V$, the simulation of the gate charge characteristics of the EPC2007 model show good agreement with the experimentally measured gate charge characteristics as reported on the datasheet. Further model validation can be obtained by cross-checking the values of the extracted device parameters from the model development against the device parameters reported on the datasheet. Shown in Figure 36 is a tabulation of the extracted device parameters from the SaberRD model development. As seen in Figure 36, the extracted on-resistance, “rds0” from the model development was $22.3m\Omega$. This value compares well with the typical value of $24m\Omega$ as reported on the EPC2007 datasheet. Also from Figure 36, it can be seen that the extracted threshold voltage from the model development, shown as “vt” is given to be $1.62V$. This value falls within the acceptable range of threshold voltages for this device which is between $0.7V$ and $2.5V$ as reported on the datasheet [59].

In the next section, the results of implementing the EPC2007 and the EPC2010 in a standard switching test circuit are discussed. These simulations were performed repeatedly after individually varying each parasitic capacitance in order to assess the effect that each capacitance has on the switching performance of GaN devices.

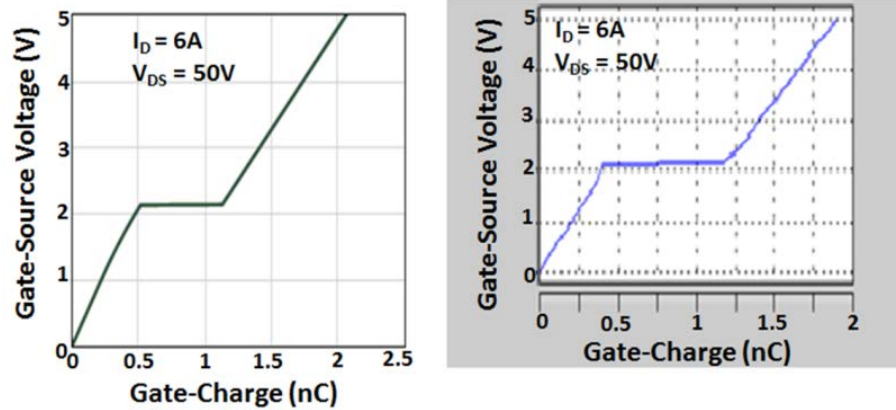


Figure 35: Gate charge characteristics comparison between datasheet (left) and model (right).

tempj	25
vt	1.62
vgs0	3.0
vds0	3
ids0	25.5
rds0	0.0223
rd	145n
rs	0.022
rg	5
lambda	0.022

Figure 36: Table showing extracted device parameters from SaberRD.

4.4 RESULTS AND DISCUSSION

Having developed the equivalent device models for the EPC2007 (100V device) and EPC2010 (200V device) and ensured the relative validity of the models, the turn-on and turn-off switching

losses of the models were simulated using a standard resistive load switching circuit seen in Figure 37. The results of these switching simulations are shown in Figure 38 for the EPC2007 and Figure 39 for the EPC2010 and tabulated in Table 1.

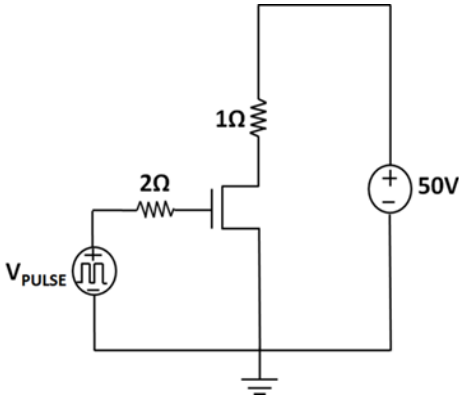


Figure 37: Resistive load switching test circuit.

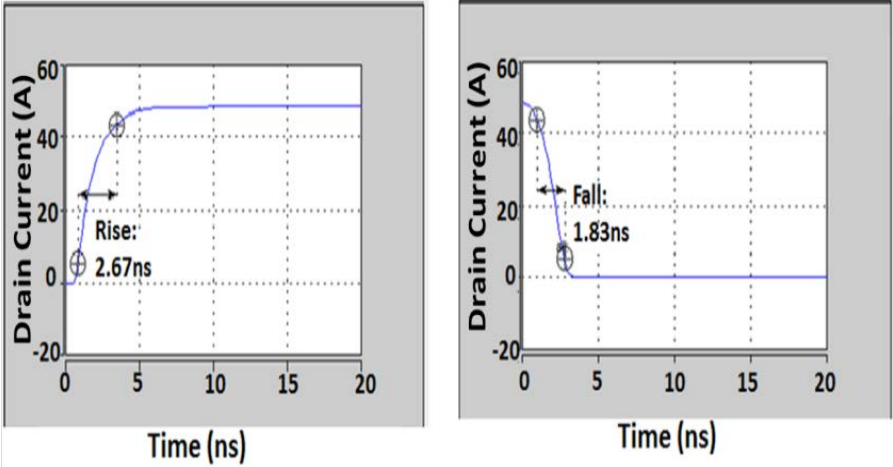


Figure 38: Results from nominal switching simulation for EPC 2007.

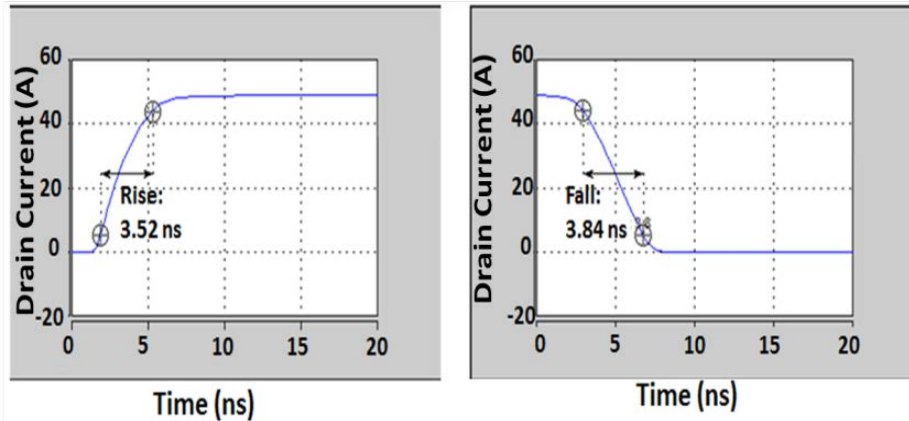


Figure 39: Results from nominal switching simulation for EPC 2010.

In both Figure 38 and Figure 39, the figure on the left shows the rise in device current for device turn-on while the figure on the right shows the fall in device current for device turn-off. From Table 1, it can be seen that for the EPC2007, the turn-on accounts for 2.91 microjoules (μJ) in loss while turn-off accounts for 824 nanojoules (nJ). For the EPC2010, the turn-on accounts for 3.16 μJ in loss while turn-off accounts for 1.72 μJ . Furthermore, as seen in Table 1 the rise and fall times for the EPC2010 are between 3 and 4 nanoseconds (ns). For experimental benchmark purposes, these data for the EPC2010 can be compared to the observations reported previously by M. Danilovic et al. in [70], where the switching performance of a EPC GaN device (EPC1010) with identically similar voltage, current and resistive ratings (200V, 12A, 25m Ω) was experimentally characterized. In [70], rise and fall times for the EPC1010 were reported between 2 and 3ns with switching losses varying throughout the microjoule range depending on the type of switching circuit used. These values are comparable with the simulation data presented here for the EPC2010 which again has identical power ratings to the EPC1010 characterized in [70].

Table 1: Comparison between EPC2007 and EPC2010.

Device	Turn-on Loss	Turn-off Loss	Turn-on Rise Time	Turn-off Fall Time
EPC2007	2.91 μ J	824 nJ	2.67 ns	1.83 ns
EPC2010	3.16 μ J	1.72 μ J	3.52 ns	3.84 ns

After simulating the switching losses for the nominal GaN HFET device models under consideration, identical switching simulations were performed after individually varying each high voltage parasitic capacitance. After each increment, the turn-on and turn-off switching losses were simulated and documented. This analysis allows one to assess the effect of each individual parasitic capacitance on the switching performance of the GaN devices. In order to isolate the impact of each individual parasitic capacitance on the device switching losses from the influence of other circuit components, all other circuit parameters were held constant including the value of the gate resistor, R_G , which can significantly impact the gate drive switching losses of the device. The gate drive used for these simulations is a simple ideal pulse voltage source. Thus, any switching losses contributed by gate drive circuits are not under consideration for this work.

The comparison presented here between the 100V and 200V devices is intended to show trends in switching performance as device operation capabilities increase. This enables design engineers to project the performance of larger voltage and larger area GaN devices which may have not yet been developed. Shown in Figure 40 is a plot illustrating the turn-on losses versus parasitic capacitances for the EPC2007 and the EPC2010. The x-axis on each plot depicts a percentage change about each nominal high voltage parasitic capacitance value as reported in the datasheet. A similar analysis was done for simulating the turn-off losses of the two devices as

shown in Figure 41. In analyzing the relative slopes and trends of each curve from Figure 40 and Figure 41, many observations can be made. First, it can be seen that for both device turn-on and turn-off, the reverse transfer capacitance, C_{RSS} (C_{GD}) has the most influence on the switching losses when transitioning to the higher voltage device. For device turn-on, when the nominal value of C_{RSS} is increased by 400%, the switching losses for the EPC2010 (200V device) are 1.5 times greater than that of the EPC2007 (100V device). For device turn-off, when C_{RSS} is increased by 400%, the switching losses for the EPC2010 are more than double that of the EPC2007.

It is also evident from both Figure 40 and Figure 41 that the parasitic impact of C_{ISS} and C_{OSS} is less than that of C_{RSS} . Furthermore, for both device-turn on and device turn-off, it appears that C_{OSS} has the least parasitic effect on the switching performance of the GaN devices. In addition, the potential beneficial aspects of C_{OSS} in GaN HFETs can be inferred from Figure 41. As seen in Figure 41, the turn-off switching losses for both devices decrease as C_{OSS} increases. In analyzing (4.0 -2) and (4.0 -3), this shows that the beneficial aspects of C_{DS} play an even greater role than the already parasitic effects of C_{GD} in the turn-off cycle of the GaN devices. This analysis is presented in order to aid in projecting the performance of future larger devices. For example, these data could aid in the design of a 600V to 1kV GaN HFET and in assessing the potential applicability of such a device.

As described earlier, the beneficial aspects of each capacitance must be considered thoroughly in device design. For instance, these data show that increasing C_{DS} reduces the parasitic effects of C_{GD} for device turn-off, however if C_{DS} is increased too significantly, the device could become substantially slower and potentially less efficient. Similarly, as mentioned before, high values of C_{GS} can reduce the possibility of false turn-on of GaN devices in high

frequency synchronous buck converters. However, if C_{GS} is designed to be too large, the device's switching losses (due to C_{ISS}) as well as the turn-on time could become undesirable.

Turn On Loss vs Parasitic Capacitances

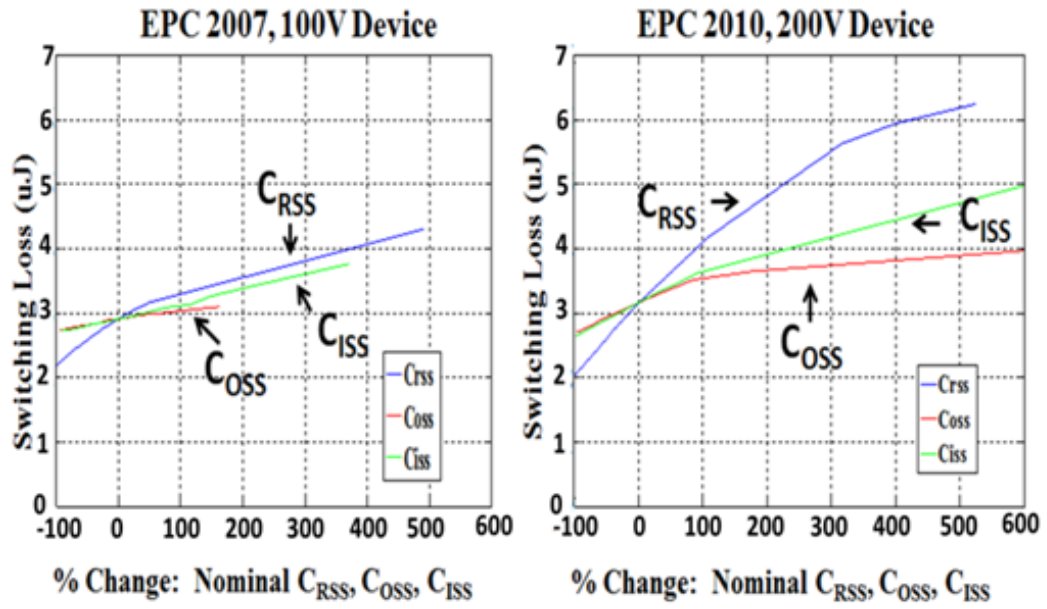


Figure 40: Turn-on losses for EPC2007 and EPC2010 versus parasitic capacitances.

Turn Off Loss vs Parasitic Capacitances

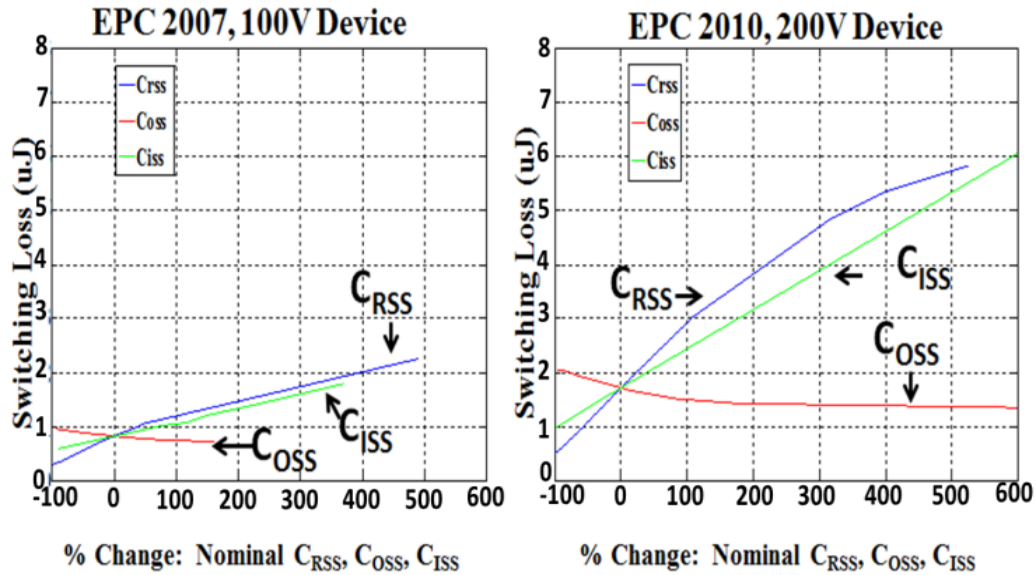


Figure 41: Turn-off losses for EPC2007 and EPC2010 versus parasitic capacitances.

4.5 SUMMARY OF CHAPTER 4.0

Equivalent device models for GaN HFETs have been developed in SaberRD in order to assess the effect of the parasitic capacitances on these devices. The methods used for this study followed model development algorithms similar to those previously reported in the literature. The models were validated by comparing simulated gate charge characteristics from the model with the experimental gate charge results as reported on the datasheets and good agreement has been obtained. The models were further validated by comparing extracted device model parameters with device parameters reported on the manufacturer’s datasheets, again with adequate agreement. The device models were simulated in standard switching test circuits, from which the results are

comparable with experimental results also reported in the literature for devices of similar ratings and sizes.

The results from the analysis presented here support the remarks made in [31], where the manufacturers of the GaN devices reported that C_{GD} is most crucial in device switching. Clearly, the data reported in this chapter substantiate this claim. Also, it has been concluded that the optimization of both C_{GS} and C_{DS} is crucial for GaN power device switching applications. For C_{GS} , an optimal value must be found so that the device is capable of fast turn-on and so that the device is not forced into conduction spuriously in synchronous buck converters and other multi-device converters. For C_{DS} , further optimization could significantly reduce the turn-off losses of the device while still allowing the device to retain its fast switching behavior. As the demand for faster, more efficient and more robust power switching devices continues to increase, designers of GaN power devices must consider the area of their intended device and how the resulting capacitance could affect the switching performance of the device. The data presented here illustrates the effect that each parasitic capacitance can have on the switching performance of GaN power devices as well as the role each capacitance could play in GaN devices of higher voltage.

5.0 HIGH DV/DT TEST CIRCUIT

In this chapter, a Cdv/dt test circuit is utilized to characterize the overshoot, ringing and false turn-on behavior in a SiC MOSFET. The effect that each parasitic capacitance has on the damping of the drain-source voltage is investigated extensively, both analytically and experimentally. In addition, the effect that each capacitance has on the magnitude of the induced gate-source voltage during false turn-on is also studied both analytically and experimentally.

5.1 PROPOSED HIGH DV/DT TEST CIRCUIT

Shown in Figure 42 is the Cdv/dt test circuit utilized here to study the false turn-on of the SiC MOSFET, both analytically and experimentally. In Figure 42(a), a pulse-width modulated signal is used to drive the drain terminal of the transistor, via an external test resistance, R_1 . The value of R_1 was varied throughout the analysis in order to vary the dv/dt seen at the drain terminal of the SiC MOSFET. The gate terminal of the MOSFET is grounded via an external gate resistor, R_{G2} . By varying the dv/dt seen at the drain terminal of the MOSFET, one can then analyze the induced gate-source voltage, V_{GS2} on the MOSFET, and determine the maximum allowable dv/dt that does not force the device into conduction. Shown in Figure 42 (b) is the complete circuit model for Figure 42(a), which includes all the parasitic components of the MOSFET as well as the parasitic inductance of R_1 , depicted as L_{R1} .

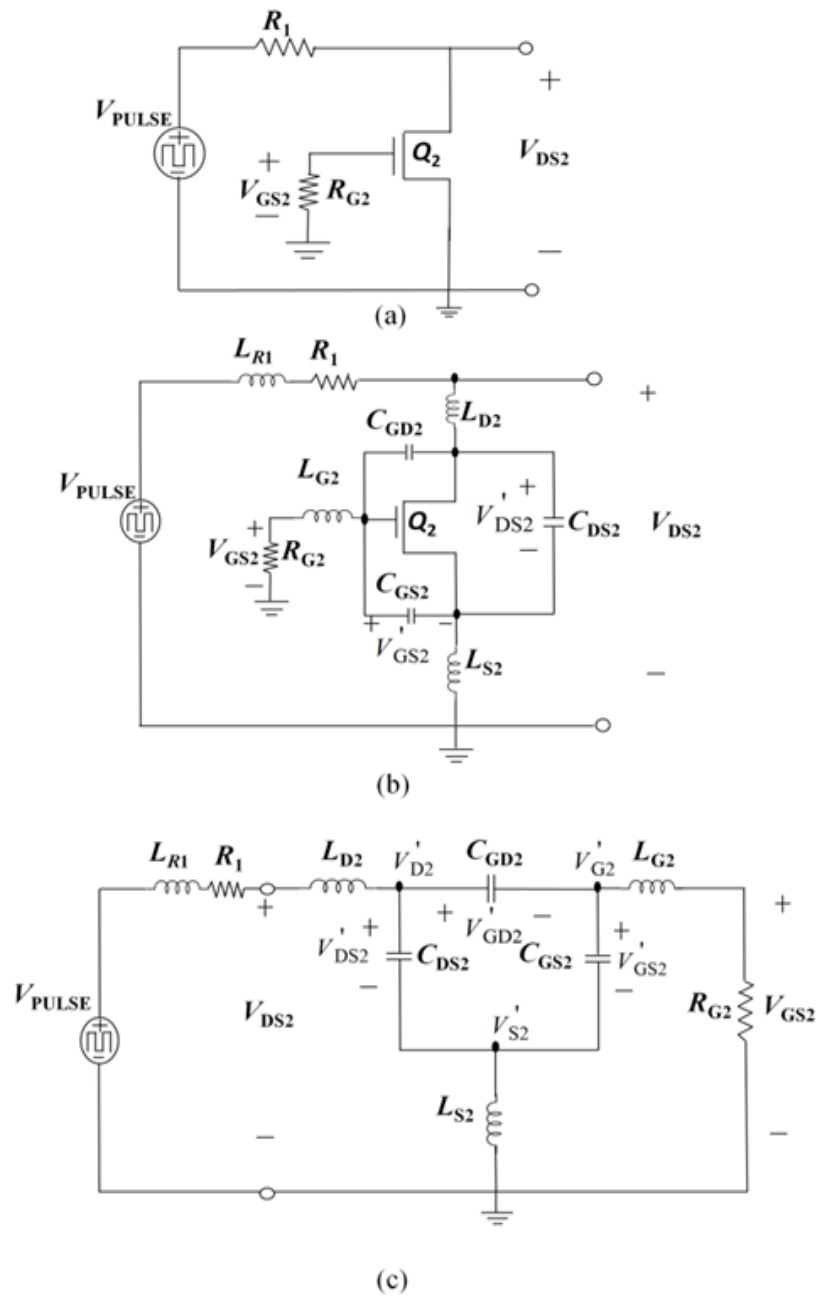


Figure 42: (a). C_{dv}/dt test circuit. (b) Test circuit with parasitics. (c) Equivalent circuit for Q_2 .

A rearrangement of the elements in Figure 42(b) is shown in Figure 42(c) where Q₂ is in its off-state and therefore there is no channel between its drain and source terminals. It is desired to derive transfer functions for V_{GS2} and V_{DS2}, where the input to the system is considered to be a unit step function. From analyzing the node currents in Figure 42(c), the following expressions can be obtained:

$$\frac{V_{\text{PULSE}} - V_{\text{DS2}}}{sL_{R1} + R_1} = \frac{V_{\text{DS2}} - V'_{\text{D2}}}{sL_{\text{D2}}} \quad (5.0 -1)$$

$$\frac{V_{\text{DS2}} - V'_{\text{D2}}}{sL_{\text{D2}}} = (V'_{\text{DS2}})sC_{\text{DS2}} + (V'_{\text{GD2}})sC_{\text{GD2}} \quad (5.0 -2)$$

$$(V'_{\text{GD2}})sC_{\text{GD2}} = (V'_{\text{GS2}})sC_{\text{GS2}} + \frac{V'_{\text{G2}}}{sL_{\text{G2}} + R_2} \quad (5.0 -3)$$

$$\frac{V'_{\text{S2}}}{sL_{\text{S2}}} = (V'_{\text{DS2}})sC_{\text{DS2}} + (V'_{\text{GS2}})sC_{\text{GS2}} \quad (5.0 -4)$$

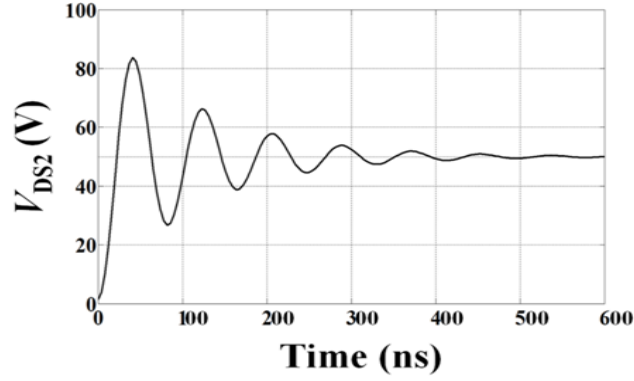
$$\frac{V'_{\text{G2}} - V_{\text{GS2}}}{sL_{\text{G2}}} = \frac{V_{\text{GS2}}}{R_{\text{G2}}} \quad (5.0 -5)$$

Shown in Table 2 are the nominal parameter values used for the model. The parasitic capacitance values are obtained from the datasheet of the SiC MOSFET [71]. The parasitic inductances are estimated from experimental measurement using $V=Ldi/dt$. In solving (5.0 -1)-(5.0 -5) simultaneously, and considering the input to be a unit step function, the transfer functions for V_{DS2} and V_{GS2} are then obtained and their step responses are plotted in Figure 43(a) and Figure 43(b) respectively. As seen in Figure 43(a), the drain-source voltage rises and oscillates for 300 nanoseconds (ns) before reaching its final steady state value of 50 V at 500 ns. From Figure 43 (b), the gate-source voltage rises rapidly to approximately 3 V during the false turn-on, but

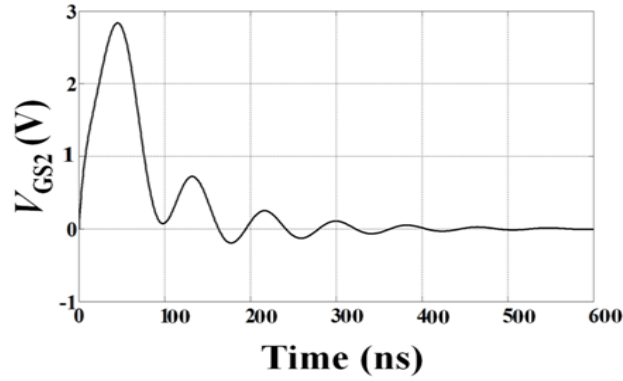
eventually goes to zero after 300 ns. As will be shown in the Section 5.3, both responses seen in Figure 43 show adequate agreement with the experimentally measured data. Next it is desired to evaluate the influence of each parasitic parameter on both the damping of the drain-source voltage and the magnitude of the induced gate-source voltage.

Table 2: Nominal parameter values for test circuit

Parameter	Value
C_{DS2}	2.75 nF
C_{GD2}	0.25 nF
C_{GS2}	11 nF
L_{D2}	15 nH
L_{G2}	15 nH
L_{S2}	1 nH
R_{G2}	5 Ω
R_1	5 Ω
L_{R1}	50 nH



(a)



(b)

Figure 43: Analytical step response for V_{DS2} and V_{GS2} .

5.2 ANALYTICAL RESULTS

5.2.1 Damping and Natural Frequency Sensitivity Analysis

In the proposed model, the Laplace transform for the drain-source voltage has a general form,

$$V_{DS2}(s) = \frac{(s + z_1)(s + z_2)(s^2 + 2\alpha s + \beta)}{s(s + p_1)(s + p_2)(s^2 + 2\zeta\omega_n s + \omega_n^2)} \quad (5.0 -6)$$

where p_1 , p_2 and z_1 , z_2 are the poles and zeros of the system, respectively and α and β are constants. Also in (5.0 -6), ζ and ω_n represent the damping ratio and natural frequency of the system's oscillatory mode, respectively. These two parameters provide information about the

speed at which a system converges to its steady state value as well as how violently it oscillates. The damping ratio and natural frequency are highly dependent on the parasitic components of the SiC MOSFET. To characterize the sensitivity of the damping ratio and natural frequency on the device's capacitances and inductances, each parasitic element was individually varied after which the resulting Laplace transform in (5.0 -6) was re-analyzed to find the system's new parameters. This enables one to assess how the change in each individual parasitic component affects the change in damping ratio and natural frequency.

Shown in Figure 44 is a plot of the damping ratio versus the parasitic device capacitances. Since Figure 44 depicts a sensitivity analysis, the slope of each curve is more meaningful than the absolute magnitude of each curve. In Figure 44 it can be seen that the slopes for C_{GD2} and C_{DS2} are approximately equal and significantly positive. This means that increasing C_{GD2} and C_{DS2} can reduce the oscillations in the drain-source voltage during the false turn-on of the device. However, the slope for the curve of C_{GS2} is relatively constant, indicating that C_{GS2} has insignificant influence on the oscillations of the drain-source voltage. For fair comparison, several extra data points beyond 10 nF were taken for C_{GS2} , since it is an order of magnitude greater than C_{GD2} . As seen in Figure 44, when C_{GS2} is 30 nF or approximately three times its nominal value, it still has no effect on the damping ratio of the drain-source voltage. It should be noted that the observations reported here are specific to the particular circuit topology in Figure 42. However, the methods reported here can be expanded to more commonly observed high dv/dt circuits like the synchronous buck converter.

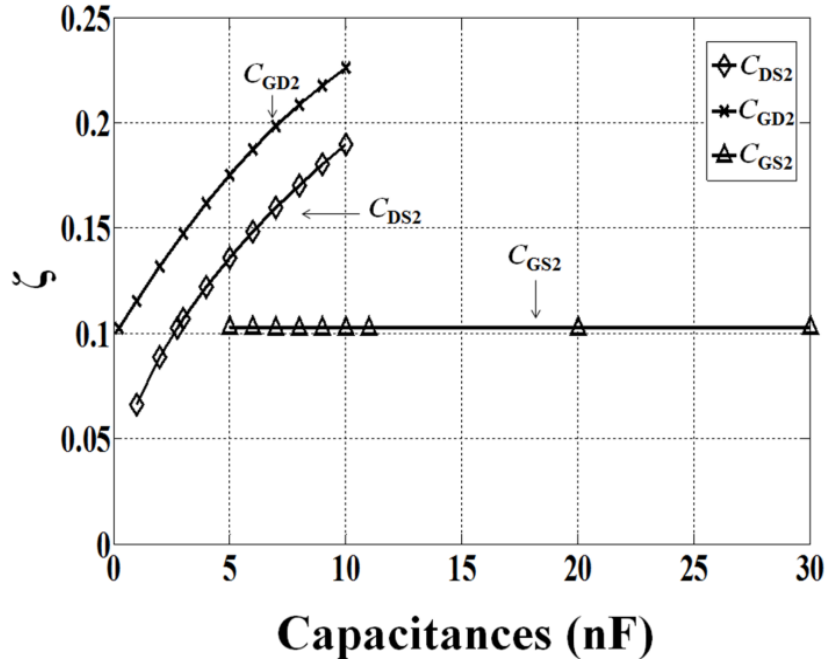


Figure 44: Damping ratio versus parasitic device capacitances.

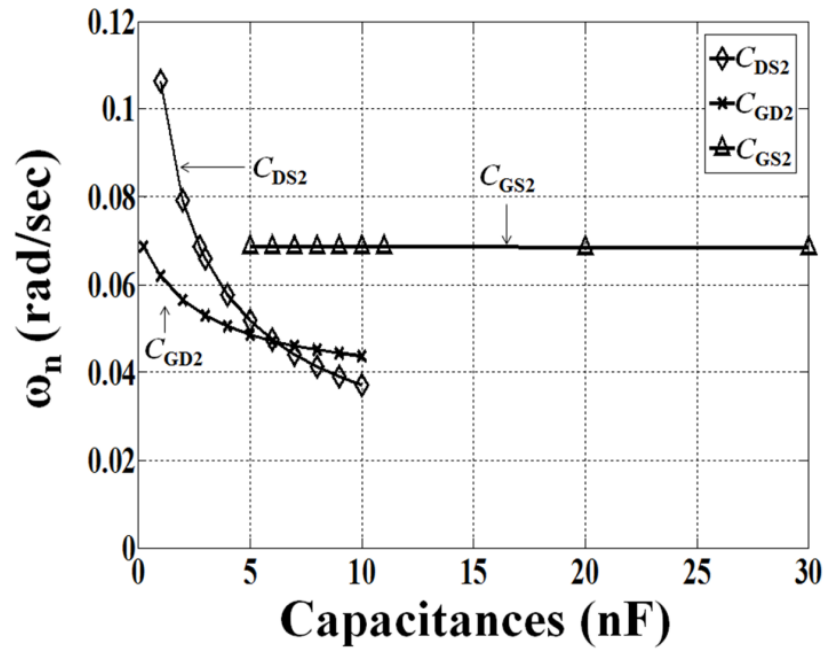


Figure 45: Natural frequency versus parasitic device capacitances.

Shown in Figure 45 is a plot of the natural frequency versus the parasitic device capacitances. Both C_{DS2} and C_{GD2} have a significant effect on the natural frequency, however the influence of C_{DS2} is greater. Both curves show a negative trend, indicating that increasing either C_{DS2} or C_{GD2} will decrease the frequency of oscillations in the drain-source voltage. Increasing C_{GS2} on the other hand has little effect on the natural frequency of the drain-source voltage.

To illustrate these findings, Figure 46 shows the model's predicted drain-source voltage when the value of C_{GD2} is increased to 10 nF. When comparing Figure 46 with the nominal condition in Figure 43(a), it is clear that the response in Figure 46 shows smaller overshoot with less oscillatory frequency. Since the damping ratio varies inversely with overshoot, the observations in Figure 46 are consistent with the data in Figure 44 and Figure 45 which show that increasing C_{GD2} will increase the damping ratio while decreasing the natural frequency.

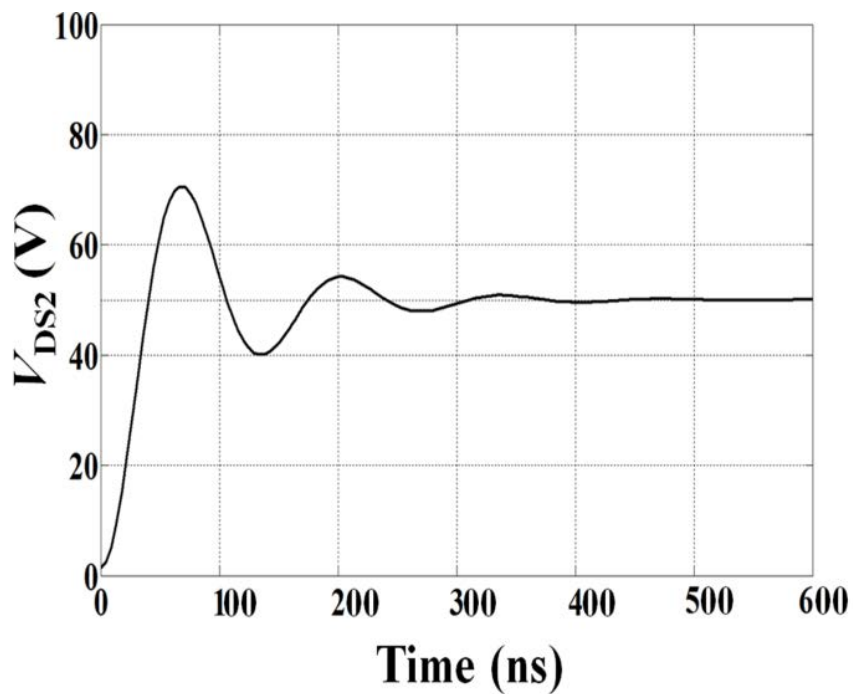


Figure 46: Step response for V_{DS2} after C_{GD2} is increased to 10 nF.

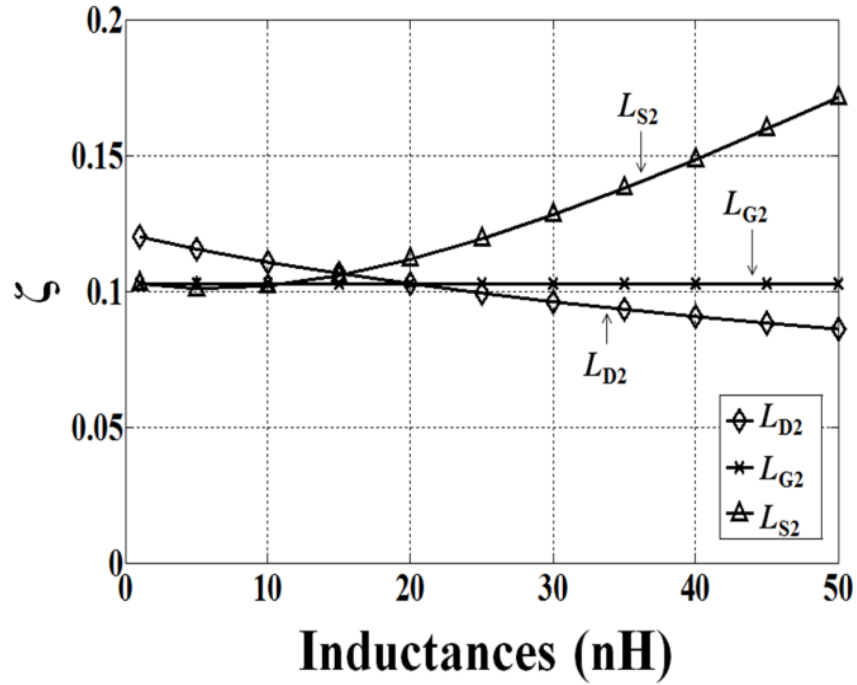


Figure 47: Damping ratio versus parasitic inductances.

Figure 47 shows the dependence of the parasitic device inductors on the damping ratio of the drain-source voltage, while Figure 48 shows the dependence of the parasitic device inductors on the natural frequency of the drain-source voltage. As seen in Figure 47 the damping ratio decreases with increasing drain inductance, L_{D2} . However, the damping ratio increases with increasing source inductance, L_{S2} . This observation points to the potential beneficial aspects of the source inductance during the false turn-on of SiC MOSFETs. On the other hand, the gate inductance, L_{G2} has very little influence on the damping ratio of the drain-source voltage. From Figure 48, it is evident that increasing L_{D2} and L_{S2} will decrease the natural frequency of the drain-source voltage while again L_{G2} has no effect.

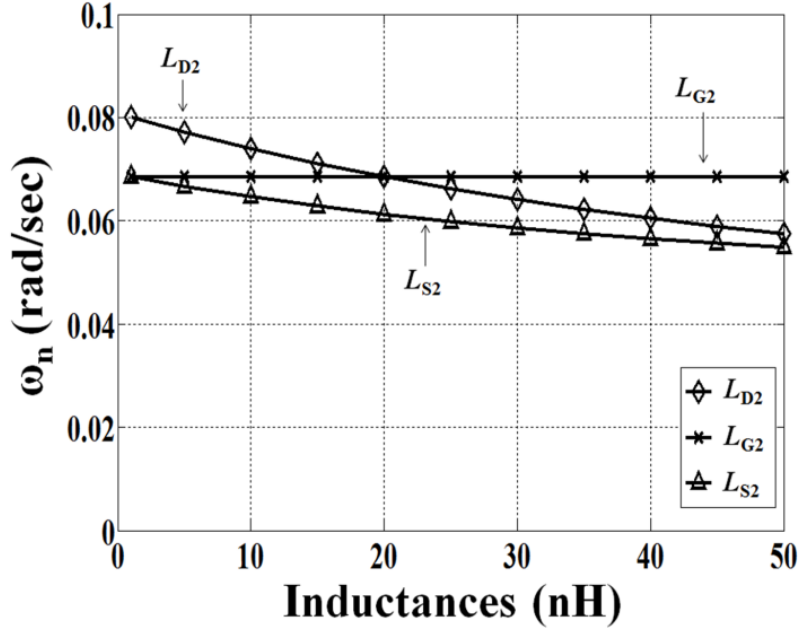


Figure 48: Natural frequency versus inductances.

5.2.2 Dependence of Parasitic Capacitances on Induced V_{GS2}

Next the influence of the parasitic capacitances on the induced gate-source voltage was analyzed. Figure 49 shows the analytical results obtained for this analysis. As seen in Figure 49, C_{GD2} has a significant impact on the induced gate-source voltage during false turn-on. The relationship between the gate-source voltage and C_{GD2} is nearly piecewise linear during false turn-on. It should be noted that the nominal value of C_{GD2} is 0.25 nF, and this analysis extrapolated the value of C_{GD2} to 10 nF, which is impractical for SiC. However, this analysis does provide a relative measure of how substantial the effect of C_{GD2} could be even on a smaller scale. Further analysis of Figure 49 shows that increasing C_{GS2} will decrease the magnitude of the induced gate-source voltage during false turn-on.

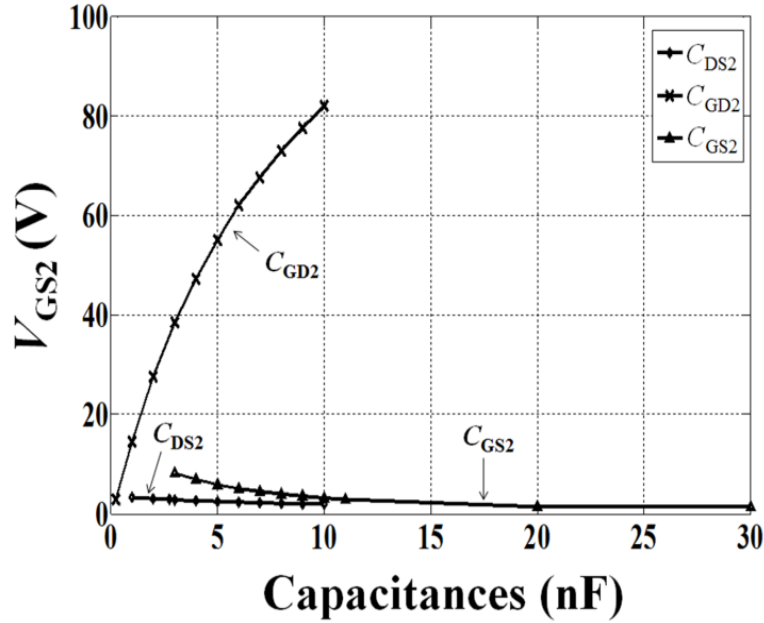


Figure 49: Magnitude of induced gate-source voltage versus parasitic capacitances .

To illustrate the effect of C_{GS2} on the gate-source voltage, Figure 50 shows the analytical measurement of the gate-source voltage after C_{GS2} has been increased to 30 nF. As seen in Figure 50, the magnitude of the gate-source voltage is approximately 1 V, which is almost three times less than its nominal false turn-on value as shown in Figure 43(b).

In order to assess the impact of C_{DS2} on the induced gate-source voltage, Figure 51 depicts a magnified portion of Figure 49 where only C_{DS2} is shown. As seen in Figure 51, increasing C_{DS2} will also decrease the induced gate-source voltage. While the beneficial effect of C_{DS2} for false turn-on is not as substantial as C_{GS2} , it is still measurable and should not be neglected. It should be noted that increasing capacitance in general will increase switching losses during the *intended* turn-off and turn-on of the device. Thus in order to minimize total switching losses in high dv/dt circuits, the values of C_{GS2} and C_{DS2} need to be optimized so that their beneficial aspects during false turn-on are not completely offset by their parasitic effects during

intended turn-on and turn-off. In the next section, experimental studies are provided to validate the analytical results reported here.

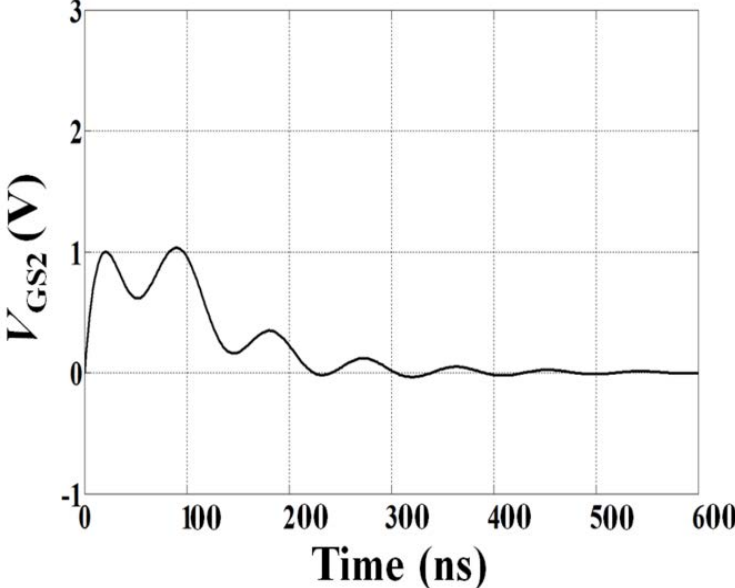


Figure 50: Induced V_{GS2} after C_{GS2} was increased to 30 nF.

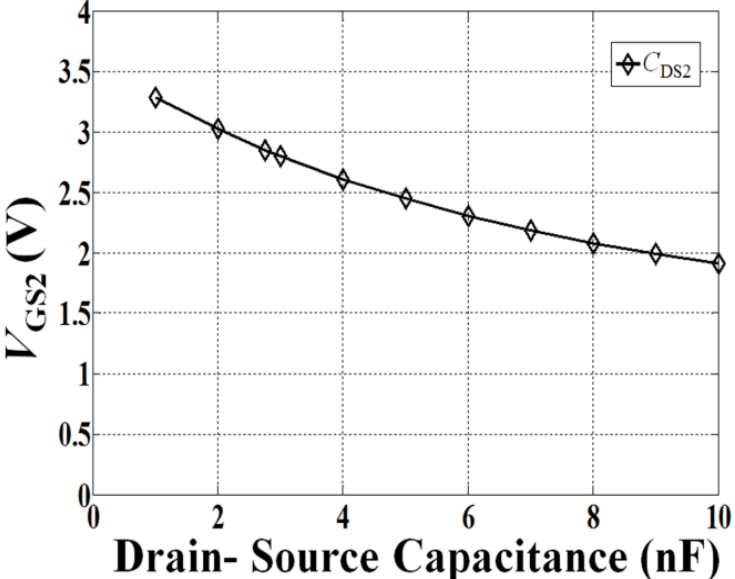


Figure 51: Induced V_{GS2} versus C_{DS2} .

5.3 EXPERIMENTAL RESULTS

5.3.1 Nominal Comparison

The circuit in Figure 42 was then experimentally tested using the SiC MOSFET in order to validate the results of the analytical model. Figure 52 shows the experimentally measured drain-source voltage and gate-source voltage during false turn-on under the nominal conditions seen in Table 2. The data in Figure 52 can be compared with the analytical results for the drain-source voltage and gate-source voltage seen in Figure 43. Reasonable agreement is obtained. The final steady state value for the drain-source voltage both analytically and experimentally is 50 V. The overshoot in the drain-source voltage is higher for the analytical model, while the time required to reach the steady state value is slightly longer for the experimental measurements. This indicates that the damping ratio for the experimental data is higher than in the analytical model, while the natural frequency for the experiment is lower than the analytical model. The reason for this discrepancy can most likely be attributed to experimental circuit parasitics not accounted for in the analytical model. For the gate-source voltage, the peak value in both the experimental result and analytical result is approximately 2.75 V. In the model, the gate-source voltage reaches its first minimum value at 100 ns, while experimentally this point occurs at 120 ns again indicating the experimental result is somewhat slower than the analytical result, due to circuit parasitics. However, the trends and shapes of the experimental waveforms show reasonably adequate agreement with the analytical results.

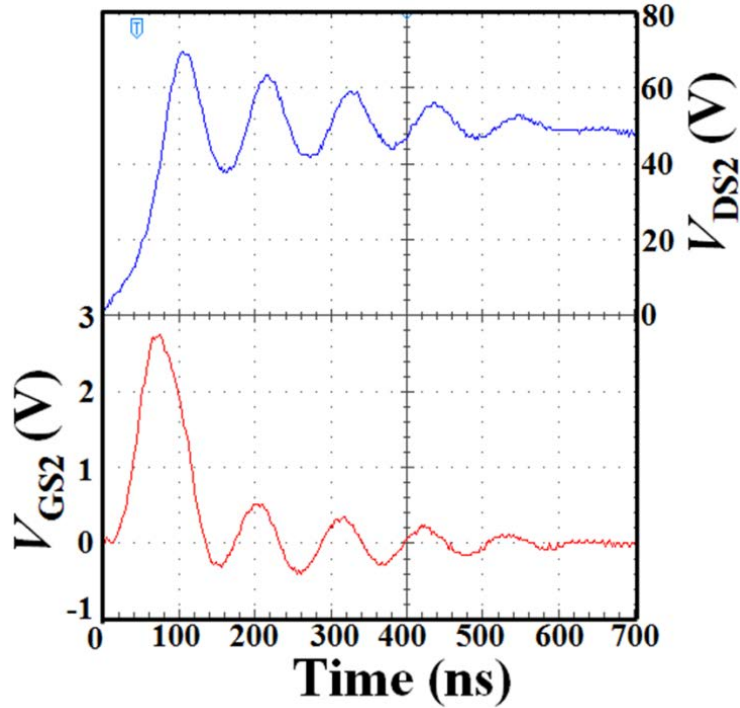


Figure 52. Experimental drain-source and gate-source voltage.

5.3.2 Effects of C_{GS2}

Shown in Figure 53 is a plot of the experimental drain-source and gate-source voltage after C_{GS2} is increased to 30 nF by connecting a 19 nF capacitor across the device's internal 11 nF nominal C_{GS2} . The result in Figure 53 verifies two analytical observations obtained in the previous section. First, increasing the value of C_{GS2} did not noticeably affect the damping ratio or natural frequency of the drain-source voltage. This is observable by comparing the drain-source voltage under the nominal condition, seen in Figure 52 versus the drain-source voltage with increased C_{GS2} seen in Figure 53. In comparing the speed, overshoot and oscillatory frequency of the two figures, they are nearly identical. Indeed as illustrated in Figure 44 and Figure 45, for this particular circuit C_{GS2} has no influence on the damping ratio or the natural frequency of the drain-source voltage. Secondly, the experimentally measured gate-source voltage after C_{GS2} is

increased to 30 nF in Figure 53 is in good agreement with its analytical counterpart seen in Figure 50. Both figures show two peaks at approximately 1 V, however again the analytical result is faster. These observations further confirm the validity of the proposed model.

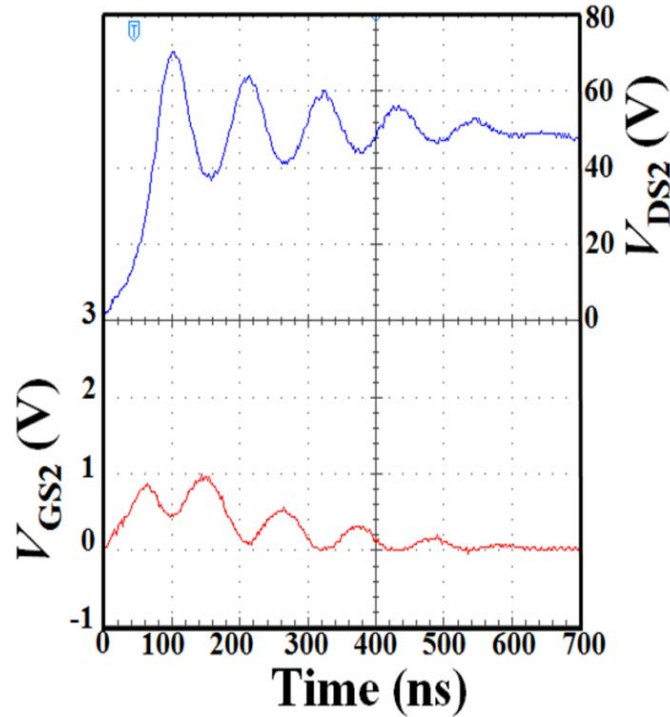
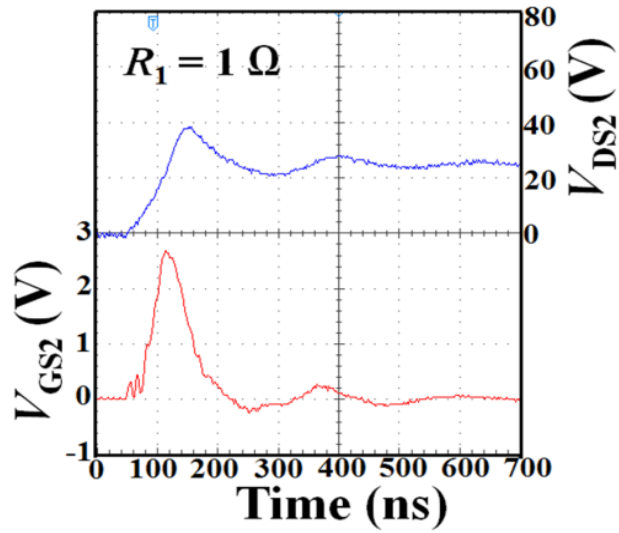


Figure 53: Experimental results after gate-source capacitance was increased to 30 nF.

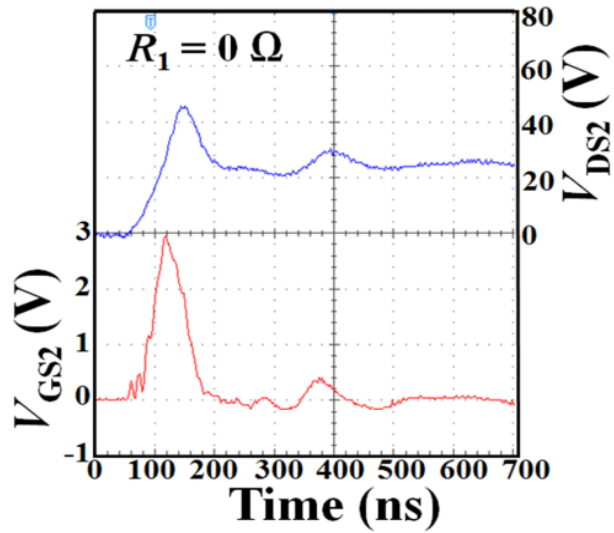
5.3.3 Maximum Allowable dv/dt

It is also desired to experimentally evaluate how the magnitude of dv/dt affects the induced gate-source voltage. By changing the value of R_1 in Figure 42, the effective RC time constant of the circuit is changed, thereby varying the dv/dt seen at the drain terminal of the MOSFET. Such an analysis enables one to determine the maximum allowable dv/dt that does not force the device into conduction.

Figure 54 shows a comparison between the device voltages when R_1 is changed from 1 Ω to 0 Ω . In this experiment, the magnitude of the pulse width modulated signal is half of that from previous experiments, so that changing R_1 can have more effect on the dv/dt . As can be seen in Figure 54, after the value of R_1 is changed from 1 Ω to 0 Ω , the overshoot in the drain-source voltage is higher, while the induced gate-source voltage increases from 2.75 V to 3 V. This undesired observation occurs because decreasing R_1 increases the dv/dt seen at the drain terminal, thus inducing a higher gate-source voltage. To allay this effect, C_{GS2} can be increased so that the gate-source voltage is reduced even at high values of dv/dt . Figure 55 shows the measured gate-source voltages at varying values of C_{GS2} as well as varying values of dv/dt (R_1). From the datasheet of the MOSFET, the minimum threshold voltage of the device (V_{TH}) is 1.5 V. The results from Figure 55 show that for the nominal capacitance values, a dv/dt of 0.15 V/ns will force the device into conduction. As seen in Figure 55 if the total value of C_{GS2} is increased to 20 nF, false conduction can be avoided at 0.15 V/ns. For a higher dv/dt of 0.63 V/ns, a total C_{GS2} of 40 nF is required to avoid false turn-on. For a low dv/dt of 0.015 V/ns, there is no possibility of false turn-on. The general trend of Figure 55 confirms the analytical trend seen in Figure 49 where it was shown that increasing the value of C_{GS2} will decrease the induced gate-source voltage during false turn-on.



(a)



(b)

Figure 54: Experimental result with (a) $R_1 = 1$ ohm and (b) $R_1 = 0$ ohms.

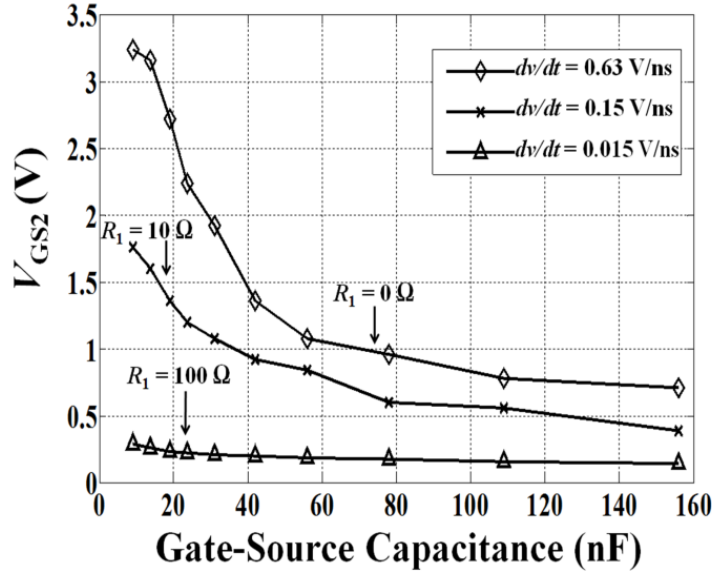


Figure 55: Experimental V_{GS2} versus C_{GS2} at varying dv/dt .

5.4 SUMMARY OF CHAPTER 5.0

An analytical methodology for evaluating the Cdv/dt induced false turn-on in SiC MOSFETs has been presented. The model presented here enables one to assess the influence of the parasitic device parameters on the damping ratio and natural frequency of the drain-source voltage. In addition, the influence of the parasitic capacitances on the induced gate-source voltage has been investigated. The analytical results presented here have been validated with experimental data and adequate agreement has been obtained. As device performance capabilities increase, the methods reported here can be beneficial in the design of high voltage synchronous buck converters, or other power conversion circuits containing multiple switching devices and high dv/dt . Again, it should be noted that the findings in this chapter are unique to the particular circuit topology used, however this work still provides a method for modeling Cdv/dt false turn-on which can be extrapolated to other desired circuits. The next objective for this work is to

expand the analysis of this chapter to a full synchronous buck converter so the work can be utilized in a more practical fashion.

6.0 FALSE TURN-ON BEHAVIOR IN SYNCHRONOUS BUCK CONVERTERS

This work presents new insights on false turn-on in synchronous buck converters using a SiC MOSFET. An analytical state space model is developed, which consists of equivalent circuits for the two MOSFETs in the converter. The output of the model is shown to closely predict experimental waveforms for various signals in the converter during the instance of false turn-on. The complex interactions between both devices are modeled in detail, showing how the impedance of one MOSFET can affect the switching behavior of the other. As the adoption of faster wide bandgap semiconductors becomes more pervasive, the model presented here can be used by design engineers to mitigate the detrimental transient high dv/dt effects often demonstrated by next generation power electronic devices.

6.1 INTRODUCTION

Mathematical semiconductor device models are becoming increasingly beneficial for evaluating the performance of dynamic power electronic systems. As device operating capabilities continue to progress, mathematical models can be used to project the efficiency of higher voltage power converters. Two types of mathematical semiconductor models have been proposed in order to assess device performance. The first type is the physics-based approach where the physical parameters of the device serve as inputs to the model [22], [72]. In [23], a physics-based model

for a virtual Field Effect Transistor (FET) was created to measure the effect of the device's output capacitance on its switching losses. The results from the virtual model were confirmed by experimentally varying the output capacitance of the device and measuring the resulting switching losses. The merit of the physics-based approach has been further demonstrated in emerging faster wide bandgap semiconductor technologies like gallium nitride (GaN) [39]. In general, the results obtained from physics-based models match the experimental results very well, but at the expense of increased computation times [43].

The second type of mathematical model is the equivalent circuit model. Here, equivalent circuits are derived to model the behavior and efficiency of the device during various sub-stages of the switching period. In [73] and [74], comprehensive analytical circuit models for a FET which included the parasitic inductances of the device package were presented. The various circuit models for the FET during different sub-stages of the switching period in a generic circuit topology were analyzed in great detail. However, to date a full converter model consisting of detailed analytical device models within the converter topology has not been offered. While such an analysis would be extremely complex for all of the sub-stages of the converter's switching period, focusing on one sub-stage of converter operation, particularly one where significant losses occur is more practical and beneficial. In particular, power electronic circuits which contain multiple switching devices are of considerable interest since the efficiency of these converters is significantly influenced by the devices' switching losses [58], [75].

This work presents new insights on one sub-stage of the switching period in the synchronous buck converter, specifically that of "false turn-on." An analytical state-space model of the synchronous buck converter is established, which contains the circuit models for each of the converter's FETs during false turn-on. The results obtained from the analytical model will be

shown to match experimental data. The model presented in this paper is particularly useful as the adoption of faster wide bandgap semiconductors becomes more widespread in next generation power electronic systems, such as renewable energy implementations. Although the fast switching capability of wide bandgap semiconductors is generally considered a beneficial feature, undesirable and detrimental high dv/dt transient effects such as “high overshoot,” “ringing loss,” and false turn-on can also arise [61, 63, 64, 66, 76]. As such, the device utilized for this study is a high voltage silicon carbide (SiC) MOSFET. The issue of false turn-on was discussed extensively in [67], where it was demonstrated that several design optimization considerations must be made in order to mitigate the detrimental effects of high dv/dt circuits. The purpose of this work is to supplement the experimental work shown in [67] with an analytical circuit model, which will aid in the design optimization process. The methods in this paper can be extrapolated to other converters containing wide bandgap semiconductors and potential high dv/dt effects.

The remainder of this chapter is organized as follows: Section 6.2 discusses the inherent cause of false turn-on in synchronous buck converters and also provides experimental waveforms for the various signals in a synchronous buck converter. Section 6.3 presents the analytical model which can reproduce the experimental waveforms seen in Section 6.2 while also offering new insights on the oscillations observed in the various signals of the converter. A sensitivity analysis is given in Section 6.5. Concluding remarks are given in Section 6.6.

6.2 PROBLEM CONTEXT

6.2.1 False Turn-on in Synchronous Buck Converters

The synchronous buck converter shown in Figure 56 is becoming the preferred circuit topology for low voltage power electronic applications requiring attenuation of the input signal [77]. This converter offers several advantages for renewable energy integration applications, where size, cost and efficiency are of considerable importance. Further, the converter is a suitable topology for utility-based photovoltaic installations, where a sufficient number of panels can be cascaded in series, therefore negating the need for the “step-up” or boost converter [78].

The synchronous buck converter contains a high side FET, Q_1 , and a low side FET, Q_2 . Relative to the conventional buck converter which uses a diode instead of Q_2 , the synchronous buck converter has the advantage of significantly reducing the conduction losses observed in the conventional buck converter. However, if Q_2 suffers from high dv/dt induced false turn-on during its off-state, the switching losses of the synchronous buck converter can become undesirably high.

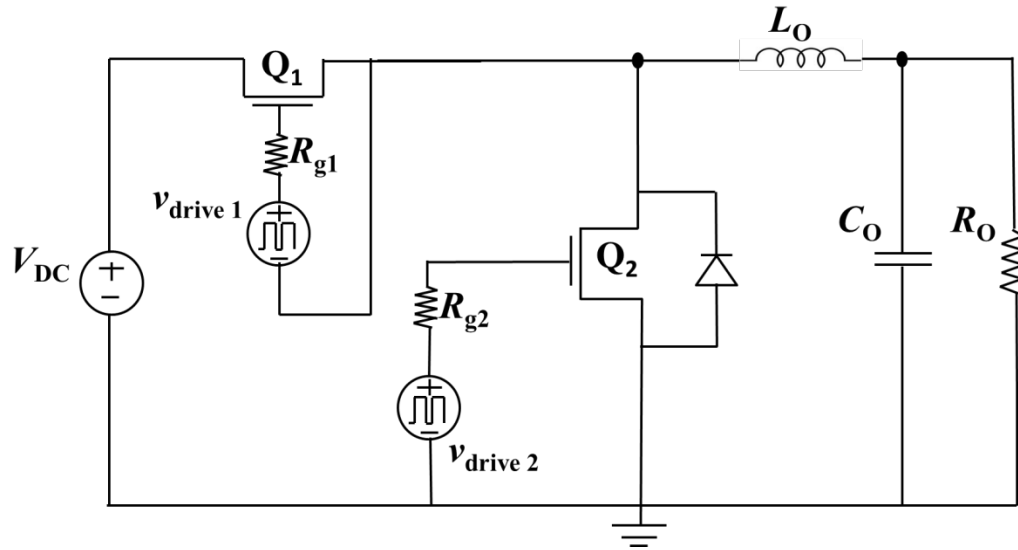


Figure 56: Synchronous buck converter.

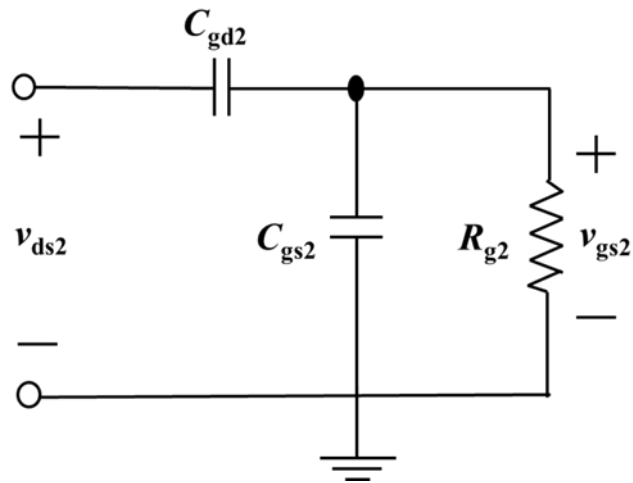


Figure 57: First order circuit model for Q_2 in its off state [69].

To illustrate the mechanism of false turn-on, a first order circuit model for Q_2 in its off-state is shown in Figure 57 [69]. Since Q_2 is in its off-state, there is no channel between its drain and source terminals, and the input gate signal is effectively at ground potential. During the rapid turn-on of Q_1 , a high dv/dt is induced on the drain terminal of Q_2 leading to a current through the gate-drain capacitance, C_{gd2} . In turn, a current flows out of the gate of Q_2 and across the external gate resistor, R_{g2} . If the resulting voltage across R_{g2} exceeds the threshold voltage V_{TH2} , of Q_2 , the device is forced into conduction spuriously leading to significant switching losses. To understand how each of the parameters in Fig. 2 affect the false turn-on behavior of Q_2 , the frequency response function shown in (6.0 -1) can be utilized

$$\frac{v_{gs2}(j\omega)}{v_{ds2}(j\omega)} = \frac{j\omega R_{g2} C_{gd2}}{1 + j\omega R_{g2} (C_{gd2} + C_{gs2})}. \quad (6.0 -1)$$

To reduce (increase) the possibility of false turn-on, the magnitude of the left hand side of (6.0 -1) should be small (large) so that v_{gs2} does not exceed the threshold voltage. In analyzing (6.0 -1), it can be inferred that low values of R_{g2} and C_{gd2} can decrease the possibility of false turn-on. It can also be seen that high values of C_{gs2} will decrease the possibility of false turn-on at sufficiently high rise-time frequencies. However, the value of C_{gs2} should not be designed to be too large, otherwise the switching losses during the intended turn-on of Q_2 will become undesirably high.

The speed at which Q_1 turns-on can also affect the magnitude of the spuriously induced gate-source voltage on Q_2 . Typically, a higher charge device, with higher parasitic capacitance, is used for Q_1 , in order to reduce the dv/dt seen at the drain terminal of Q_2 . This comes at the expense of increased switching losses through Q_1 during its turn-on and turn-off cycles. If a wide bandgap semiconductor (with relatively low parasitic capacitances) is used for Q_1 , the turn-on

rate can be slowed by increasing the value of the external gate resistor, R_{g1} . This also comes with the cost of increased switching losses through Q_1 .

It is clear then, that several design optimization considerations must be made for synchronous buck converters and other high dv/dt circuits which exhibit false turn-on behavior. As a necessity for optimization, an analytical model which can accurately model the experimental waveforms of the converter is needed. The goal of this paper then is to present a comprehensive analytical converter model which includes all the parasitic components of both Q_1 and Q_2 and closely approximates the experimental waveforms of the converter during false turn-on. Once the waveforms can be reproduced and the model is proven to be valid, optimization of each circuit parameter can occur so that switching losses in both Q_1 and Q_2 can be minimized. Analytically reproducing experimental waveforms in order to gain more insight into false turn-on behavior is the subject of this paper, while optimization of the analytical model will be the subject of our future work.

6.2.2 Experimental Waveforms

In order to understand the phenomenon of false turn-on in Q_2 , the synchronous buck converter in Figure 56 was experimentally constructed and tested. An analytical model would then be developed around the measured data from the circuit. The nominal parameter values and testing conditions used in the circuit are seen in Table 3. An ideal scenario for avoiding false turn-on was created, where a high charge device served as Q_1 . Therefore, for the purpose of minimizing false turn-on, little attention was paid to the increase in switching losses through Q_1 . As previously described, using a higher charge and resultantly slower device for Q_1 reduces the dv/dt seen at the drain terminal of Q_2 , thus decreasing the possibility of false turn. Therefore, a

Silicon (Si) based MOSFET served as Q_1 . Also, from (6.0 -1) it is clear that devices with lower values of C_{gd} should be used as Q_2 in order to avoid false turn-on in synchronous buck converters. Wide bandgap devices offer low parasitic capacitances and therefore a SiC MOSFET served as Q_2 . To even further reduce the possibility of false turn-on occurring, a 100Ω external resistor was applied to the gate of Q_1 , thereby slowing its turn-on speed. Thus, in this case study, any observed false turn-on in Q_2 implies that even more false turn-on would occur if a faster wide bandgap semiconductor would be used for Q_1 (with similar voltage and current ratings) and/or if a Si based FET would be used for Q_2 (with similar voltage and current ratings). This is an essential study particularly as the adoption of faster wide bandgap semiconductors becomes more widespread for enhancing the performance of next generation power electronic systems.

During the interval where Q_1 is at the point of turn-on, voltage measurements were then taken for v_{gs1} , v_{ds2} , and v_{gs2} , which can be seen in Figure 58. In order to account for extraneous experimental parasitics both from instrumentation and circuit wiring, the insight and observations presented in [79] were taken into consideration.

Table 3: Nominal Circuit parameters used to construct synchronous buck converter

Parameter	Value
R_{g1}	100 Ω
R_{g2}	5 Ω
L_O	2.5 mH
C_O	10 mF
R_O	10 Ω
V_{DC}	50 V
v_{drive1}	20 V
v_{drive2}	20 V
f_{sw}	10 kHz

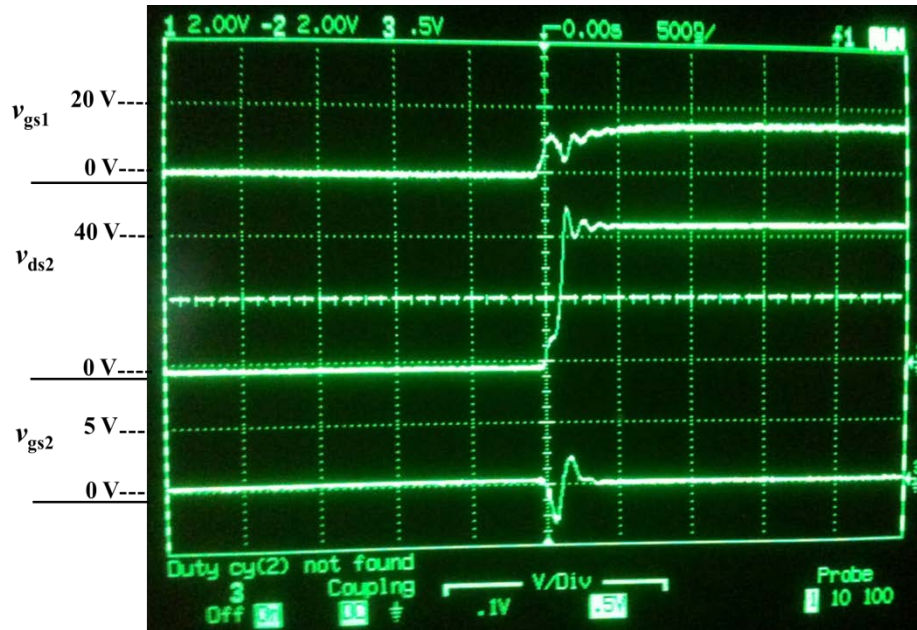


Figure 58: Experimental waveforms for false turn-on.

As observed in Figure 58, v_{gs1} initially increases towards its steady-state value with no oscillation. However, as the channel completely forms in Q_1 , the impedance of Q_2 becomes apparent to Q_1 . This can be observed as the drop and subsequent transient recovery of v_{gs1} and corresponding dramatic rise of v_{ds2} . Both of these phenomena can be seen clearly within the first 250 nanoseconds in the plots for v_{gs1} and v_{ds2} . Furthermore, the quick rise in v_{ds2} corresponds to a rapid transient response in v_{gs2} , one that is sufficiently large enough to produce false turn-on in Q_2 . As seen in the waveform for v_{gs2} , its induced magnitude is approximately 2.5 V, which is higher than the SiC MOSFET's minimum threshold voltage of 1.5 V, therefore resulting in false turn-on.

From inspection of the converter in Figure 56, the waveform for v_{ds1} can be surmised as the difference between a constant DC voltage source and the given waveform for v_{ds2} seen in Figure 58. Therefore, any oscillations in v_{ds2} can be inferred to occur in v_{ds1} but opposite in

direction. Thus, the ability of the parasitic components of Q_2 to affect the behavior of v_{gs1} and v_{ds1} shows that the switching losses of Q_1 will depend not only on its own parasitic components, but also on the parasitic components of Q_2 . Consequently, a full circuit model for Q_1 during turn-on should include a model for Q_2 as well. The goal then becomes to model this phenomenon analytically in order to predict false turn-on and optimize system parasitics. The following section will therefore analytically detail the stages of false turn-on in the synchronous buck converter where the results will match the experimental waveforms given here, thereby providing a path towards system optimization.

6.3 STAGES OF FALSE TURN-ON

6.3.1 Substage I: Charging of Q_1 of Conduction

Just prior to false turn-on occurring, the converter is in its “dead-time” where both devices are non-conductive. During the dead-time, Q_1 is in its off state while the body diode of Q_2 conducts current in the upward direction. The equivalent circuit for this situation is shown in Figure 59, where v_{drive1} is effectively zero volts. Shown in Figure 60 is a simplified version of Figure 59, with the pertinent voltages clearly indicated and where Z_{eq} represents the equivalent impedance of the body diode and parasitic inductances of Q_2 in parallel with the output of the converter.

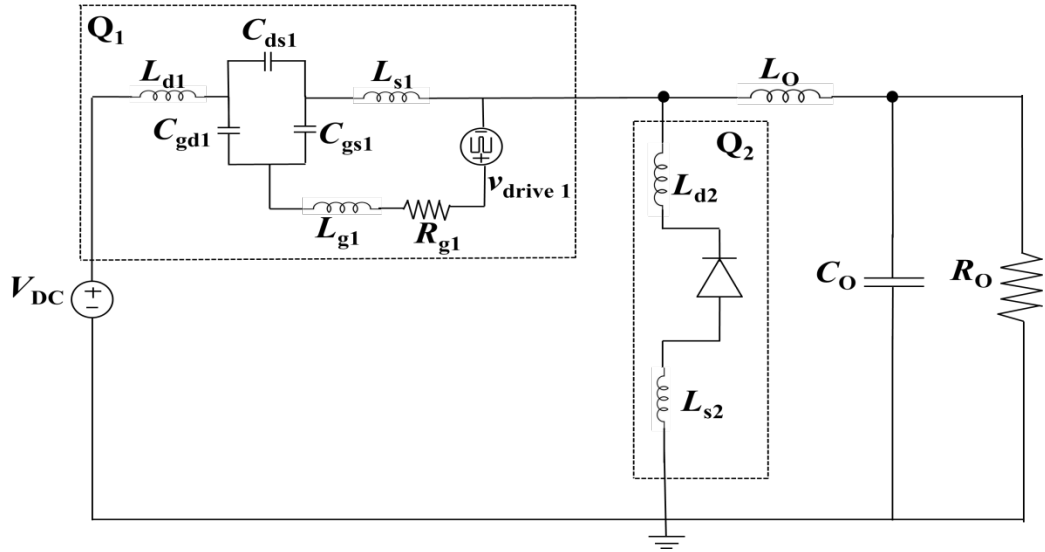


Figure 59: Synchronous buck converter during dead time interval.

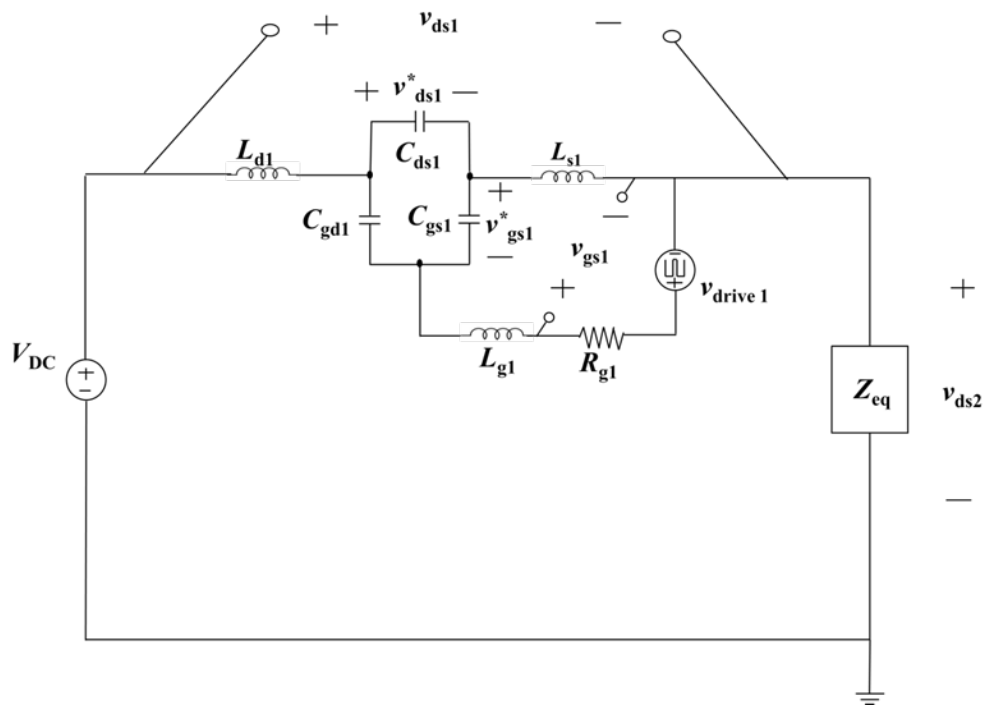


Figure 60: Simplified version of Figure 59, with voltage clearly indicated.

Then v_{drive1} begins to charge the gate of Q_1 so that v_{gs1}^* increases towards V_{TH1} . Before v_{gs1}^* reaches V_{TH1} , the MOSFET is open-circuited, and therefore v_{ds1} remains constant implying that C_{ds1} can be removed from the initial analysis. As the body diode of Q_2 has a very small voltage across it, the source-terminal of Q_1 is effectively at ground potential during this phase. The equivalent circuit for this sub-stage is shown in Figure 61.

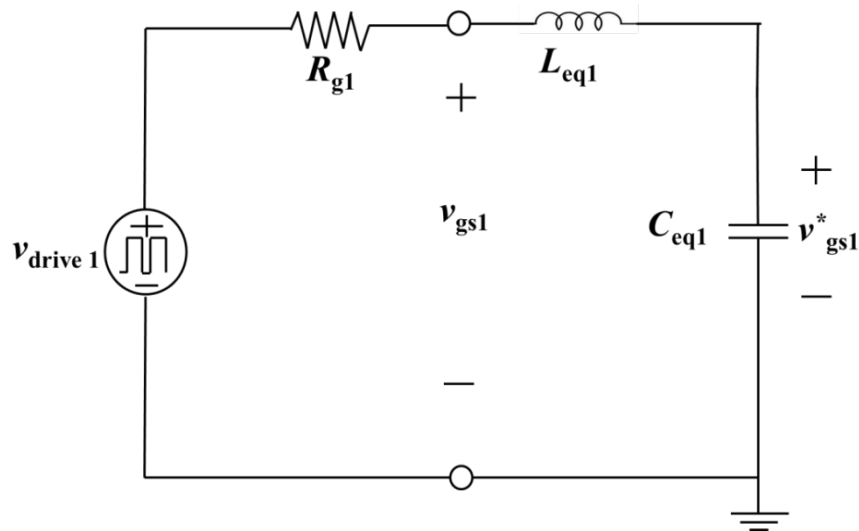


Figure 61: Synchronous buck converter during charging of Q_1 interval.

Using frequency domain analysis, the Laplace transform for v_{gs1} is

$$v_{gs1}(s) = \frac{1}{s} \left[\frac{\frac{1}{C_{eq1}L_{eq1}} + s^2}{s^2 + \frac{R_{g1}}{L_{eq1}}s + \frac{1}{C_{eq1}L_{eq1}}} \right] \quad (6.0 -2)$$

where $C_{eq1} = C_{gs1} + C_{gd1}$, $L_{eq1} = L_{g1} + \frac{L_{s1}L_{d1}}{L_{s1} + L_{d1}}$, and v_{drive1} is considered to be a unit-step

function. To understand the experimental oscillations of v_{gs1} in Figure 58, one can analyze the denominator of (6.0 -2) in canonical form of a second-order system:

$$s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (6.0 -3)$$

where ω_n is the natural frequency and ζ is the damping ratio. From inspection of (6.0 -2) and (6.0 -3), it can be seen that

$$\zeta = \frac{R_{g1}}{2} \sqrt{\frac{C_{eq}}{L_{eq}}}. \quad (6.0 -4)$$

It should be noted that the experimental oscillations of v_{gs1} in Figure 58 are indicative of a damping ratio significantly less than one. To demonstrate this, it should be recalled that in the experimental analysis that yielded the results shown in Figure 58, a 100 Ω resistor was used for

R_{g1} . For the damping ratio to be less than one, this then implies that the ratio $\sqrt{\frac{C_{eq}}{L_{eq}}}$ must be no

greater than 0.01, which is unreasonable. This observation implies that the oscillations in v_{gs1} are not contributed explicitly by the circuit parameters in Figure 61 and a more accurate model is required. In the next section, a more complete representation is presented in order to describe the above transitions.

6.3.2 Substage II: Formation of Q₁ Channel

As v_{drive1} charges the gate of Q₁, the circuit in Figure 61 is valid until v_{gs1}^* reaches V_{TH1} at which point a channel is gradually formed across the drain and source terminals of Q₁. As seen in Figure 58, the time required for v_{gs1}^* to reach its steady-state value is relatively slow, indicating a very gradual channel formation in Q₁. This observation is due to the use of both the large R_{g1} as well as the highly capacitive Si MOSFET. As the channel forms, v_{ds1} decreases. When the channel is completely formed, v_{ds1} reaches its minimum steady-state value (approximately zero, depending on the value of R_{ON1}) and remains constant. The equivalent circuit for the entire synchronous buck converter at this particular moment is shown in Figure 62. Since the entire circuit now feels the effect of V_{DC} , the body diode of Q₂ stops conducting and therefore Q₂ assumes its off-state model.

In order to plot step responses for the desired voltages, we adopt an analytical state-space model of the synchronous buck converter. The state-space model facilitates the definition of the circuit's initial conditions, which are constantly varying throughout the dynamic switching process. To obtain analytical waveforms for v_{gs1} , v_{ds2} , and v_{gs2} , state variables were assigned for inductor currents and capacitor voltages. As seen in Figure 62, symbols across inductors indicate current state variables, while symbols across capacitors denote voltage state variables. The definition of all state-variables is summarized in Table 4. Shown in Table 5 and Table 6 are the circuit and transistor parameter values that produced the analytical results given in this section and subsequent sections. Parasitic capacitance values were extracted from the datasheets of the MOSFETs, while package inductances were estimated using $V=Ldi/dt$.

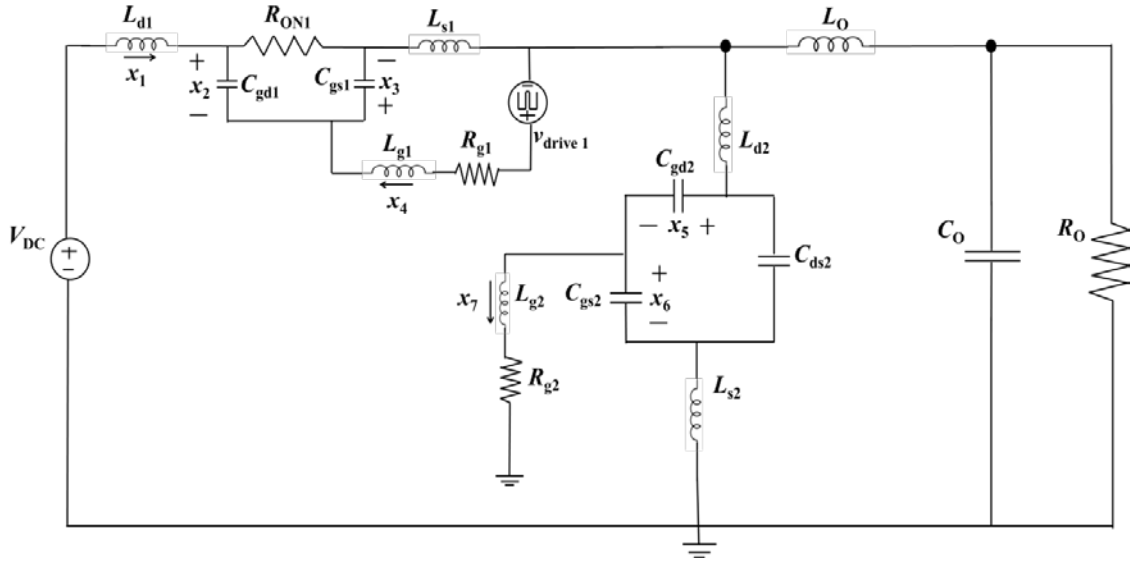


Figure 62: Synchronous buck converter after formation of Q_1 channel.

Table 4: State variable assignments.

Parameter	Element	State Variable
i_L	L_{d1}	x_1
v_C	C_{gd1}	x_2
v_C	C_{gs1}	x_3
i_L	L_{g1}	x_4
v_C	C_{gd2}	x_5
v_C	C_{gs2}	x_6
i_L	L_{g2}	x_7

From analysis of Figure 62, and the state variable assignments, the equations seen in (6.0 -5)-(6.0 -11) can be derived in order to plot the step responses for the desired outputs,

$$(L_{d1} + L_{s1} + L_{d2})\dot{x}_1 - R_{ON1}C_{gd1}\dot{x}_2 + L_{s1}\dot{x}_4 + L_{g2}\dot{x}_7 = -R_{ON1}x_1 - x_5 - R_{g2}x_7 + V_{DC} \quad (6.0 -5)$$

$$R_{ON1}C_{gd1}\dot{x}_2 = R_{ON1}x_1 - x_2 - x_3 \quad (6.0 -6)$$

$$L_{s1}\dot{x}_1 + (L_{g1} + L_{s1})\dot{x}_4 = -x_3 - R_{g1}x_4 + V_{drive1} \quad (6.0 -7)$$

$$-L_{s2}\dot{x}_1 + (L_{g2} + L_{s2})\dot{x}_7 = x_6 - R_{g2}x_7 \quad (6.0 -8)$$

$$C_{gd1}\dot{x}_2 - C_{gs1}\dot{x}_3 = -x_4 \quad (6.0 -9)$$

$$(C_{gd2} + C_{ds2})\dot{x}_5 + C_{ds2}\dot{x}_6 = x_1 \quad (6.0 -10)$$

$$C_{gd2}\dot{x}_5 - C_{gs2}\dot{x}_6 = x_7 \quad (6.0 -11)$$

The expressions seen in (6.0 -5)-(6.0 -11) can be transformed into matrix form and solved with linear algebra as seen in (6.0 -12),

$$E[\dot{x}] = F[x] + G[u]. \quad (6.0 -12)$$

Using (6.0 5)-(6.0 -11), the formulation of matrices $[E]$, $[F]$, and $[G]$ from (6.0-12), are given in (6.0 -13)-(6.0 -16),

$$E = \begin{bmatrix} L_{d1} + L_{s1} + L_{d2} & -R_{ON1}C_{gd1} & 0 & L_{s1} & 0 & 0 & L_{g2} \\ 0 & R_{ON1}C_{gd1} & 0 & 0 & 0 & 0 & 0 \\ L_{s1} & 0 & 0 & L_{g1} + L_{s1} & 0 & 0 & 0 \\ -L_{s2} & 0 & 0 & 0 & 0 & 0 & L_{g2} + L_{s2} \\ 0 & C_{gd1} & -C_{gs1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{gd2} + C_{ds2} & C_{ds2} & 0 \\ 0 & 0 & 0 & 0 & C_{gd2} & -C_{gs2} & 0 \end{bmatrix} \quad (6.0 -13)$$

$$F = \begin{bmatrix} -R_{ON1} & 0 & 0 & 0 & -1 & 0 & -R_{g2} \\ R_{ON1} & -1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & -R_{g1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & -R_{g2} \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \quad (6.0 -14)$$

$$G_{DC} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (6.0 -15)$$

$$G_{drive1} = \begin{bmatrix} 0 \\ 0 \\ 1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \cdot \quad (6.0 -16)$$

In (6.0 -16) and (6.0 -17), the variables $[G_{DC}]$ and $[G_{drive1}]$ represent matrices for the two enabled sources at the instance of false turn-on, V_{DC} and V_{drive1} . The system of equations can then be solved using (6.0 -17) and (6.0 -18),

$$[\dot{x}] = E^{-1}F[x] + E^{-1}G[u] \quad (6.0 -17)$$

$$[\dot{x}] = A[x] + B[u]. \quad (6.0 -18)$$

Table 5: Analytical model parameter values.

Parameter	Value
R_{ON1}	0.5 Ω
R_{g1}	100 Ω
R_{g2}	5 Ω
R_O	10 Ω
C_O	10 mF
C_{gd1}	0.0077 nF
C_{gs1}	1.022 nF
C_{gd2}	0.25 nF
C_{gs2}	10.75 nF
C_{ds2}	2.75 nF

Table 6: Analytical model parameter values.

Parameter	Value
L_O	2.5 mH
L_{d1}, L_{g1}	1 nH
L_{s1}	2 nH
L_{d2}, L_{g2}	15 nH
L_{s2}	30 nH
V_{DC}	50 V
v_{drive1}	20 V
v_{drive2}	20 V

In solving the state-space equations (6.0 -17) and (6.0 -18), the step response for v_{gs1} , seen in Figure 63, is obtained. Here, the step response for v_{gs1} is obtained by treating both V_{DC} and v_{drive1} as step-input voltages and thus invoking the superposition theorem. It should be noted that in practice V_{DC} is always on, and is therefore not a step function. However, modeling V_{DC} as a step function simulates the formation of the channel and the resulting near-instantaneous effect that V_{DC} has on the rest of the circuit.

When comparing the analytical step response for v_{gs1} seen in Figure 63 with the experimental result also superimposed in Figure 63, reasonable agreement is obtained. Both waveforms show significant oscillation, with no overshoot above the steady-state value of 14V. The trend and phase of the oscillations in both waveforms are similar as well. Using the proposed model, the oscillations in v_{gs1} can now be explained. Prior to v_{gs1}^* reaching V_{TH1} , the gate of Q_1 is charged by v_{drive1} and the circuit in Fig. 5 is valid. During this interval, v_{gs1} increases with no oscillation. When v_{gs1}^* reaches V_{TH1} , a channel is formed across Q_1 and v_{ds1} decreases to its steady-state value. When the channel is completely formed, the circuit in Figure 62 applies: current flows through Q_1 and charges the parasitic capacitances of Q_2 , forcing v_{ds2} to increase. As v_{ds2} increases and the parasitic capacitances of Q_2 continue to charge, the current through Q_2 decreases, thus decreasing the current through Q_1 . As a result, v_{ds1} decreases since now the product of i_1 and R_{ON1} will be lower. Due to capacitive coupling, the transient decrease in v_{ds1} leads to a transient decrease in v_{gs1} , which is the first oscillatory dip at 125 nanoseconds seen in both the analytical and experimental result in Figure 63. As v_{drive1} continues to charge the gate of Q_1 , v_{gs1} resumes its exponential increase towards its steady state value before settling at approximately 500 nanoseconds. It should be reiterated that in order to derive the proper response for v_{gs1} , the parasitic components of Q_2 needed to be included in the full circuit model. Only with the new proposed model are the oscillations in v_{gs1} fully accounted for. Thus, the switching losses of Q_1 depend not only on its own parasitic components, but also on the parasitic components of Q_2 .

It should be noted that the magnitude of the oscillations is greater for the experimental result as seen in Figure 63. The reason for this is likely due to the linear modeling of the parasitic device capacitances in the analytical model. In our previous work [66], it was shown that using

constant parasitic capacitances in an analytical device value can still result in good agreement. However, the circuit topology in this work is significantly more complex than the topology utilized in [66]. We therefore attribute the minor transient discrepancies shown in Figure 63 and subsequent results to the linear modeling of the parasitic capacitances. In our future work, we intend to develop a “switched analytical model” where the parasitic capacitance values dynamically change during the switching event.

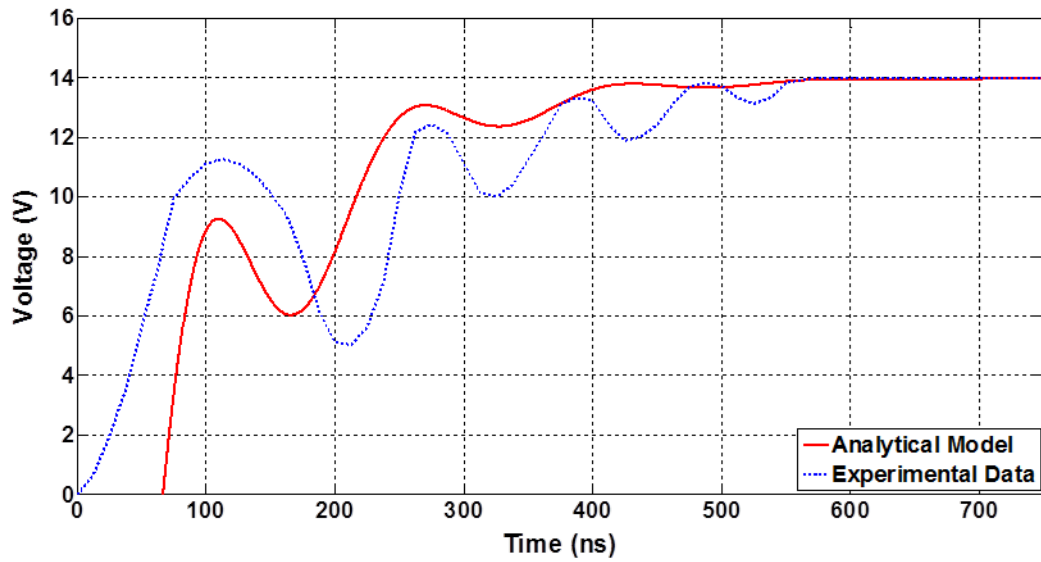


Figure 63: Step response for v_{gs1} .

6.3.3 Substage III: Rise in v_{ds2}

After the channel across the drain and source terminals of Q_1 forms, v_{ds2} increases approximately to the value of the input voltage, V_{DC} . The circuit in Fig. 6 still applies during these transitions. Therefore the relations seen in (6.0 -5)-(6.0-11) remain relatively unchanged, with the exception that v_{drive1} is no longer considered an input as it is assumed to have reached its steady-state value. Thus, to derive the proper response for v_{ds2} , only V_{DC} is considered as a step input voltage.

The step response for v_{ds2} can be obtained as seen in Figure 64. When comparing the analytical v_{ds2} in Fig. 8 with the experimental v_{ds2} also superimposed in Figure 64, adequate agreement is again obtained. As seen in both figures, immediately after the channel of Q_1 is formed, v_{ds2} rises, overshoots, and undershoots its steady state value three times, with each overshoot and undershoot becoming smaller in magnitude. Eventually v_{ds2} reaches its steady-state value at approximately 500 nanoseconds. As previously mentioned, the waveform for v_{ds1} can be assumed as the difference between V_{DC} and v_{ds2} . Therefore, the oscillations seen for v_{ds2} in Fig. 8 also occur in v_{ds1} but opposite in direction. In the previous section it was demonstrated that the parasitic components of Q_2 will affect the behavior of v_{gs1} during turn-on. Here, it is shown that the parasitic components of Q_2 will affect the behavior of v_{ds1} during turn-on as well. Thus, the parasitic components of Q_2 have an influence on the switching losses of Q_1 during turn-on and should not be excluded when analyzing the turn-on behavior of Q_1 .

In order to account for the gradual channel creation in Q_1 , due in part to the large 100 Ω external gate resistance, a 70 nanosecond delay was created for the analytical model that produced the result in Figure 64. This is a necessary analytical modeling measure, since the step response function cannot account for the gradual channel creation in Q_1 and the resulting effect on v_{ds2} . Our proposed future work of creating a switched analytical model will negate the need for the delay.

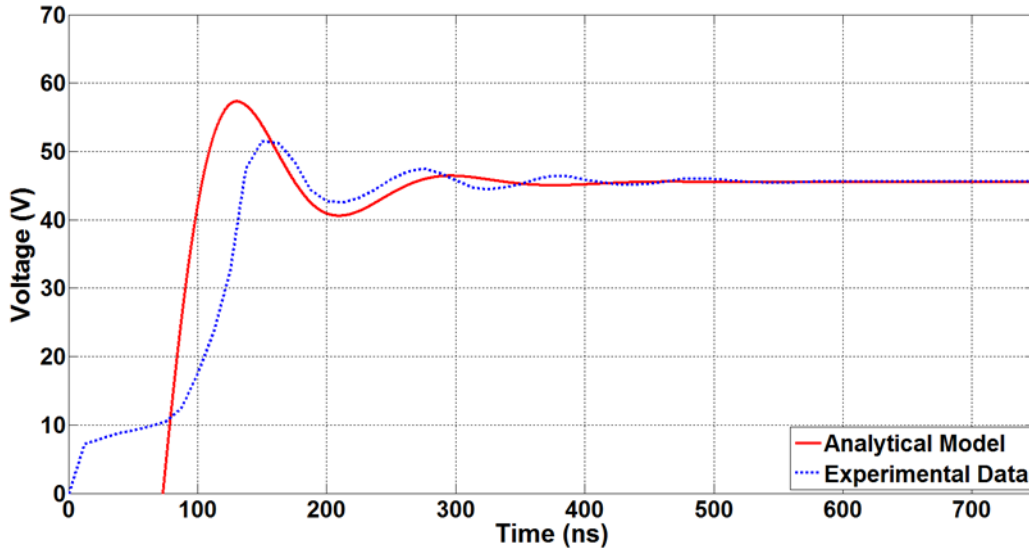


Figure 64: Step response for v_{ds2} .

6.3.4 Substage IV: Spike in v_{gs2}

When v_{ds2} increases rapidly, the dv/dt seen at the drain terminal of Q_2 is high, thus inducing a current through C_{gd2} as well as through C_{ds2} . Consequently, C_{gd2} current will cause a voltage to develop across R_{g2} despite that the driving signal of Q_2 is effectively at ground potential. If the voltage across R_{g2} exceeds V_{TH2} , the device is forced into conduction. To model these transitions, the state-space equations seen in (6.0 -17) and (6.0 -18) are utilized, resulting in the step response for v_{gs2} as seen in Figure 65, where again V_{DC} is the input and is considered to be a unit step function. When comparing the analytical result of Figure 65 with the experimental result also superimposed in Figure 65, reasonable agreement is obtained. Both waveforms oscillate above and below zero for 400 nanoseconds before settling at zero after 500 nanoseconds. Here again, the previously described 70 nanosecond delay was implemented.

Thus, it is clear from the model presented here that the switching losses of Q_1 depend not only on its own parasitic components, but also on the parasitic components of Q_2 . Therefore, any

model of Q_1 during turn-on should also contain a circuit model for Q_2 during the proper intervals, in order to fully account for the behavior of the various signals in the converter. Furthermore, the induced v_{gs2} during false turn-on is highly dependent on the rapid turn-on of Q_1 . That is, the faster that Q_1 turns on, the higher the dv/dt will be at the drain terminal of Q_2 thus leading to a higher current through C_{gd2} . Subsequently, the magnitude of the induced v_{gs2} will be larger. In order to optimize the various components of Q_1 and Q_2 to ensure more efficient converter operation, an analytical model such as the one presented above can be used.

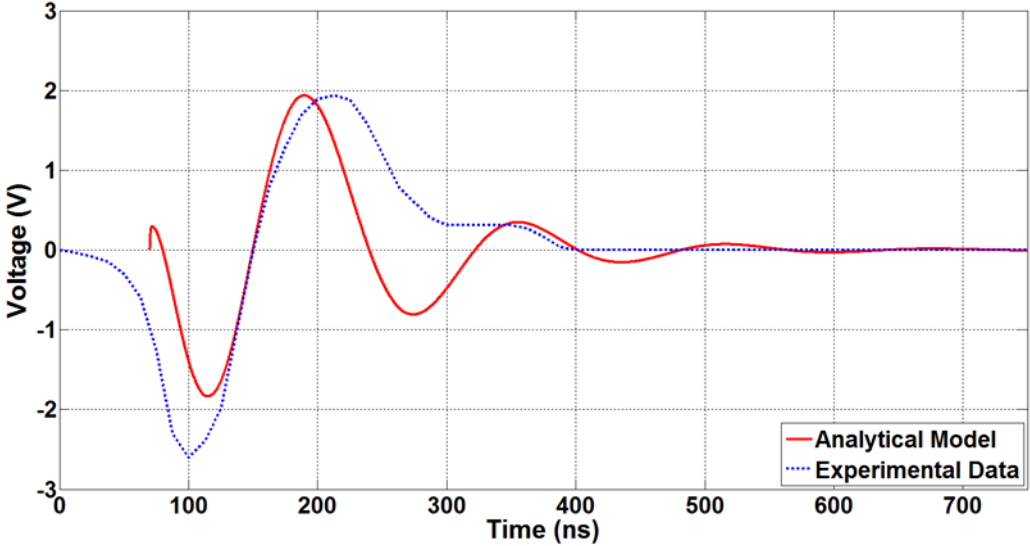


Figure 65: Step response for v_{gs2} .

6.4 FREQUENCY AND TIME DOMAIN COMPARISON

In the previous section, a state space model was used to model false turn-on in synchronous buck converters. Another approach is to use frequency domain analysis. The latter approach can be somewhat more straight forward at the cost of accuracy in the results. To illustrate this, consider the circuits shown in Figure 66, Figure 67, and Figure 68. Shown in Figure 66 is the equivalent circuit for the synchronous buck converter immediately after the channel in Q_1 is formed. A simplified version of Figure 66 is shown in Figure 67 where the node voltages are clearly indicated in order to facilitate frequency domain circuit analysis. Figure 68 shows the equivalent circuit for Z_{eq} in Figure 67, where again node voltages are clearly indicated.

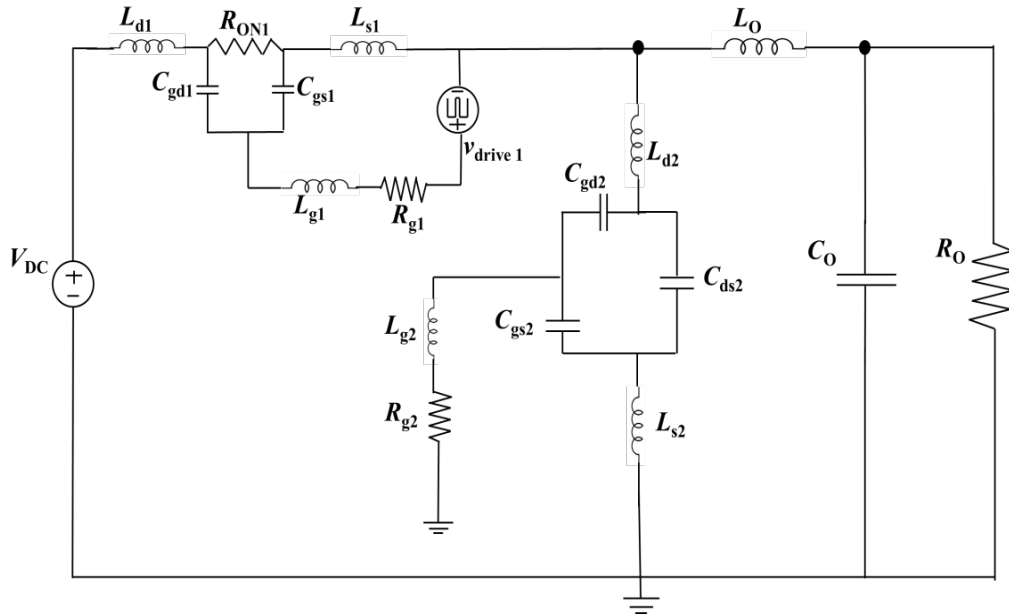


Figure 66: Synchronous buck converter after formation of Q_1 channel.

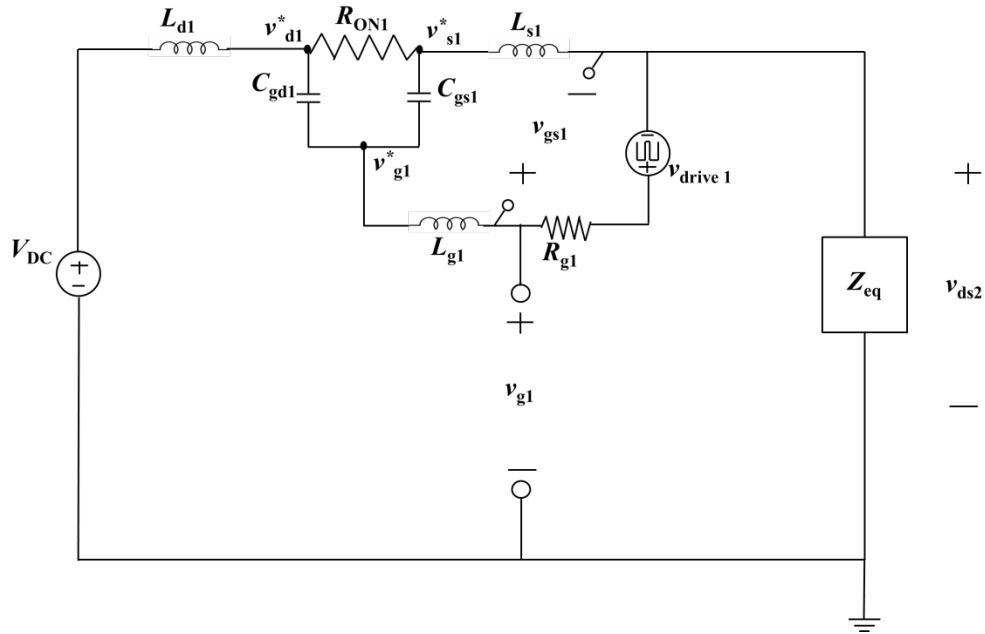


Figure 67: Simplified version of Figure 66.

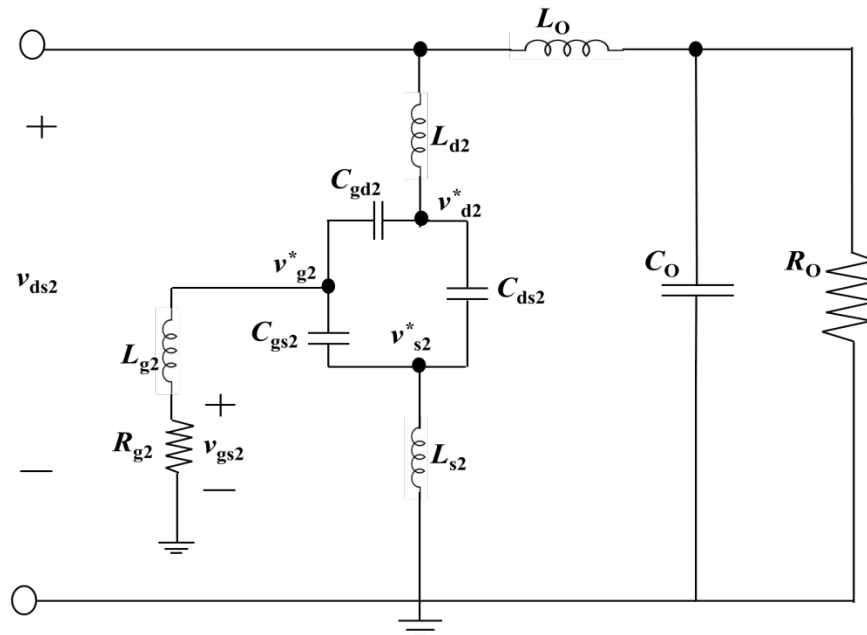


Figure 68: Equivalent circuit for Z_{eq} in Figure 67.

From analysis of Figure 67, the following frequency domain equations can be used in order to analytically create the waveform for v_{ds2} :

$$\frac{v_{ds2} - v_{g1}^*}{R_{g1} + sL_{g1}} + sC_{gd1}(v_{d1}^* - v_{g1}^*) = sC_{gs1}(v_{g1}^* - v_{s1}^*) \quad (6.0 -19)$$

$$\frac{v_{ds2} - v_{g1}}{R_{g1}} = \frac{v_{g1} - v_{g1}^*}{sL_{g1}} \quad (6.0 -20)$$

$$\frac{V_{DC} - v_{d1}^*}{sL_{d1}} = \frac{v_{d1}^* - v_{s1}^*}{R_{ON1}} + sC_{gd1}(v_{d1}^* - v_{g1}^*) \quad (6.0 -21)$$

$$\frac{v_{d1}^* - v_{s1}^*}{R_{ON1}} + sC_{gs1}(v_{g1}^* - v_{s1}^*) = \frac{v_{s1}^* - v_{ds2}}{sL_{s1}} \quad (6.0 -22)$$

$$\frac{v_{s1}^* - v_{ds2}}{sL_{s1}} = \frac{v_{ds2} + v_{gs1} - v_{g1}^*}{sL_{g1}} + \frac{v_{ds2}}{Z_{eq}} \quad (6.0 -23)$$

$$v_{gs1} = v_{g1} - v_{ds2} \cdot \quad (6.0 -24)$$

Upon solving the equations above simultaneously, the step response (using frequency domain analysis) for v_{ds2} can be obtained, as seen in Figure 69. As seen in Figure 69, the model and experimental data match fairly well at steady-state. However, the model is significantly inaccurate prior to 100 ns. This is due to the fact that the frequency domain model utilized here assumes zero initial conditions. While initial conditions can be set in the frequency domain, it is indeed a very tedious and complex process. In the state-space model presented in the previous section, the initial conditions could be set in a more straight-forward manner. As a result, the v_{ds2}

waveform obtained using the state-space model in Figure 64 is more accurate than the v_{ds2} waveform seen in Figure 69.

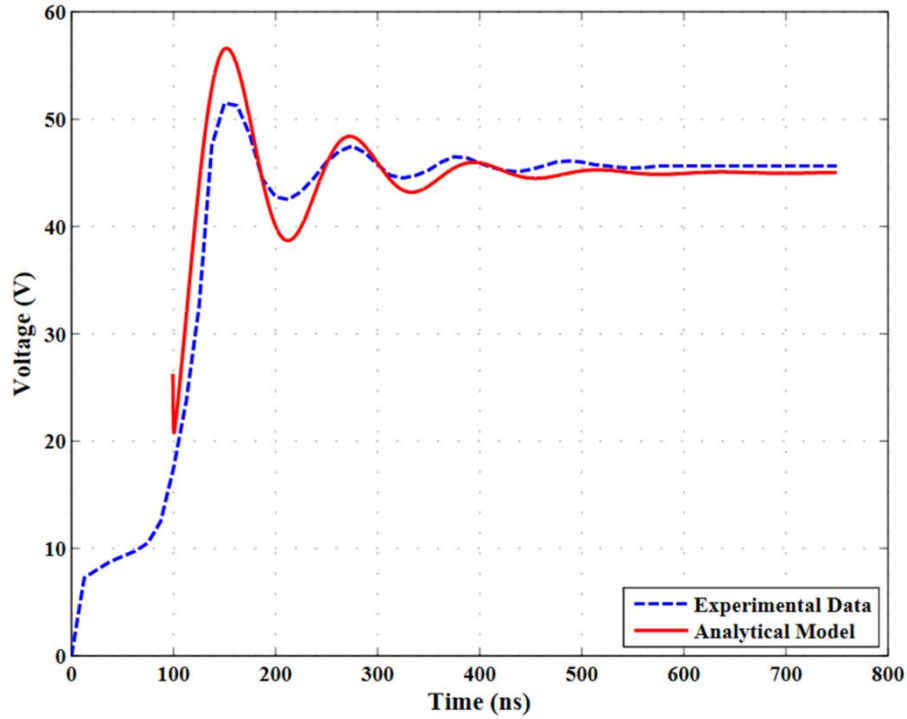


Figure 69: Step response for v_{ds2} using frequency domain analysis.

6.5 SYNCHRONOUS BUCK CONVERTER SENSITIVITY ANALYSIS

To further investigate the interactions between Q_1 and Q_2 in the synchronous buck converter and to validate the conclusions from previous section, the effects that false turn-on has on the oscillations in the various signals of the converter were experimentally measured. This required externally varying the circuit parameters that have the most influence on the false turn-on of Q_2 .

Figure 70 illustrates the experimental waveforms obtained for v_{gs1} , v_{ds2} , and v_{gs2} after the value of R_{g2} was increased to 45Ω . As seen in Figure 70, the magnitude of the induced v_{gs2} is now 5 V, twice the amount seen in the nominal condition of Figure 58. However, the oscillations in all three signals are significantly less after R_{g2} was increased. It is particularly intriguing to note that R_{g2} can have an effect on the oscillations in v_{gs1} , since R_{g2} is far away from v_{gs1} in the circuit. In addition, the change in oscillatory behavior observed in v_{ds2} will also occur in v_{ds1} . Thus the ability of R_{g2} to noticeably affect the behavior of v_{gs1} and v_{ds1} implies that R_{g2} will have an influence on the switching losses in Q_1 . Although a larger R_{g2} lowered the oscillations in the converter, the effect of increasing R_{g2} (and inducing more false turn-on) can also be detrimental to converter operation in many ways. First, as seen in Figure 70, by increasing R_{g2} to 45Ω , the induced v_{gs2} reaches an undesirably high value which would lead to significant switching losses in Q_2 . Furthermore, if the induced current through Q_2 is significantly large, the switching losses in Q_1 can be severely impacted since Q_1 and Q_2 share the same current during false turn-on. Ideally, an optimal R_{g2} can be found which would reduce oscillations in all three signals while not allowing the switching losses in both Q_1 and Q_2 to become undesirably high. In our future work, the analytical model presented in the previous section will be utilized to perform this optimization. It is further instructive to note that in this model/experiment, Q_2 is a 1200V device and therefore at the applied voltage of 50V the reduction in signal oscillation induced by false turn-on will have minimal beneficial effects. However, the observations presented here demonstrate that by inducing a certain amount of false turn-on to a transistor rated at a significantly smaller voltage, the resulting reduction in signal oscillation could be more advantageous.

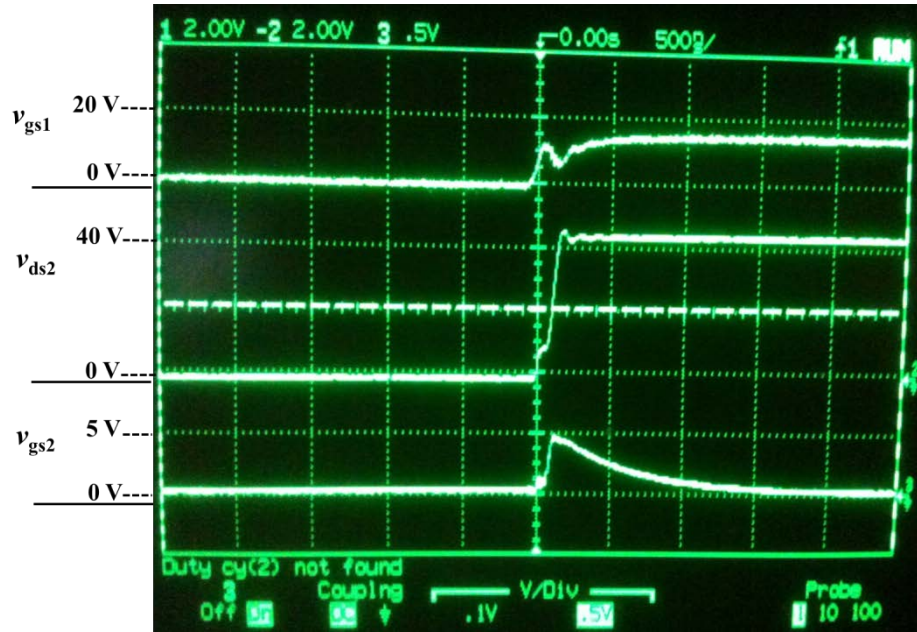


Figure 70: Experimental waveforms after R_{g2} is raised to 45Ω .

Shown in Figure 71 are the experimental results obtained for the three signals after C_{gd2} is increased to a total of 1.25 nF . This was done simply by connecting a 1 nF capacitor across the internal C_{gd2} of Q_2 . In this analysis, the value of R_{g2} was reduced to its nominal value of 5Ω . As seen in Figure 71, the magnitude of the induced v_{gs2} is 3.75 V , or 50% higher than in the nominal condition. Also, the oscillations in all three signals have been reduced compared to the nominal condition. As a result, C_{gd2} can have an effect on the switching losses in Q_1 as well. Again, the effect of increasing C_{gd2} and inducing more false turn-on may also lead to more switching losses in Q_1 , particularly if the shared current between Q_1 and Q_2 is large enough.

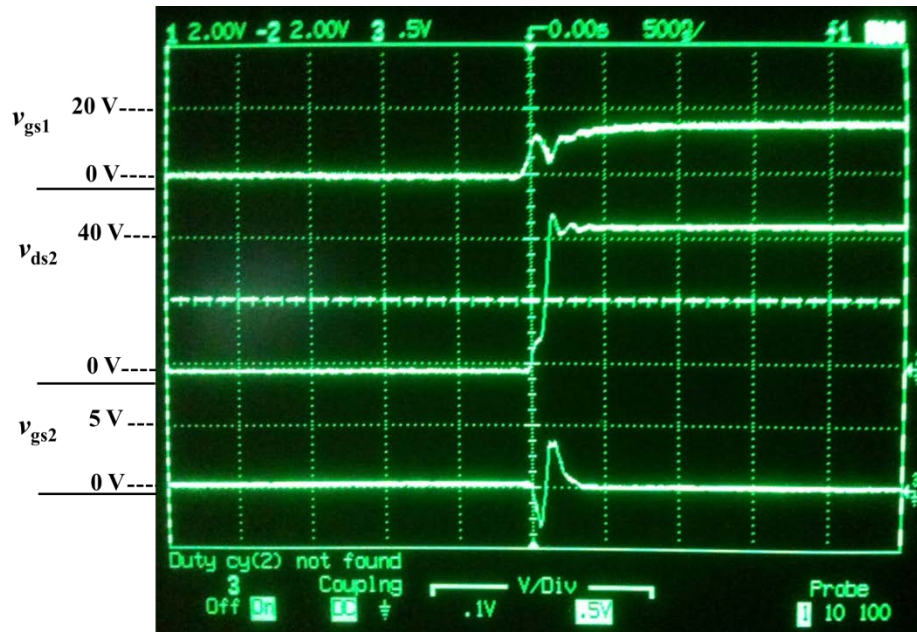


Figure 71: Experimental waveforms after C_{gd2} is raised to 1.25 nF.

Figure 72 depicts the experimental results obtained after a 10 nF capacitor was connected across C_{gs2} to obtain a total gate-source capacitance of 20.75 nF. The other circuit parameters were reduced to their nominal values. As seen in Figure 72, the magnitude of the induced v_{gs2} is now 1.25 V, half the voltage seen in the nominal condition. However, the oscillations in only v_{gs2} are slightly greater than in the nominal condition. The oscillations in v_{gs1} and v_{ds2} remain relatively unchanged. In the synchronous buck converter, C_{gs2} is an essential parameter to optimize. This is because larger values of C_{gs2} will increase switching losses during intended turn-on, but will reduce the magnitude of the induced gate-source voltage during false turn-on as shown here. As such the analytical model presented in the previous can be utilized to perform this crucial optimization.

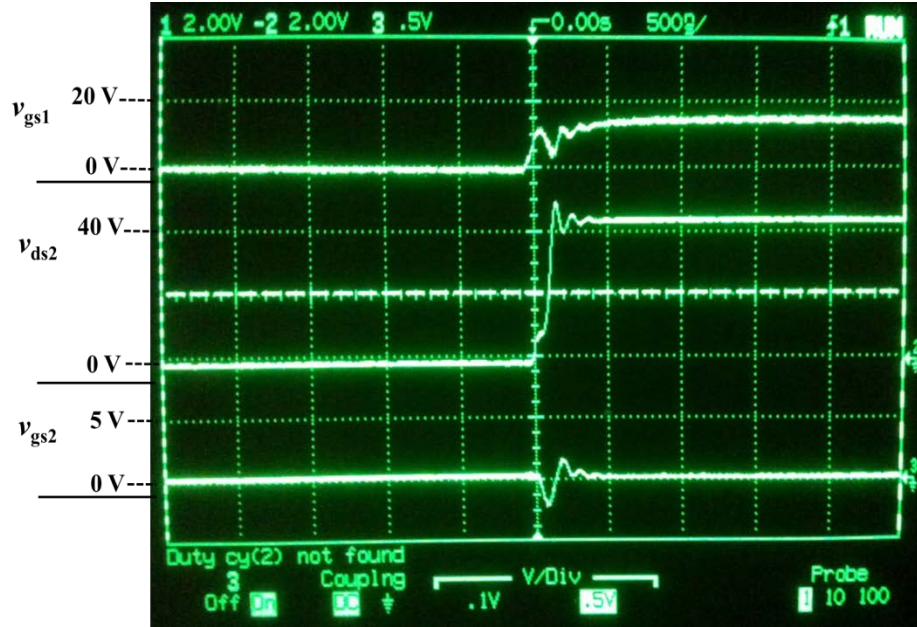


Figure 72: Experimental waveforms after C_{gs2} is raised to 20.75 nF.

The data in this section is in agreement with the results presented in our preliminary false turn-on test circuit, presented in [66] where experimental data showed that larger values of C_{gd2} will increase the damping ratio of v_{ds2} while also reducing the natural frequency of v_{ds2} . As a result, larger values of C_{gd2} will decrease the oscillations in v_{ds2} , as shown in this paper. Furthermore in [66], larger values of C_{gd2} were shown to reduce the magnitude of the induced v_{gs2} , as shown here. Finally, the data in [66] showed that larger values of C_{gs2} will have minimal effect on the oscillations of v_{ds2} while also reducing the magnitude of the induced v_{gs2} which is again consistent with the data demonstrated in this report.

Thus, the experimental data here confirms that the internal and external circuit parameters of Q_2 will affect the behavior of Q_1 during turn-on. Therefore, any model of Q_1 should contain the components of Q_2 during the proper intervals. As shown here, raising both R_{g2} and C_{gd2} will decrease the oscillations in the various signals of the converter but increase the

magnitude of the induced v_{gs2} . Conversely, raising C_{gs2} will decrease the magnitude of the induced v_{gs2} but with minimal effect on the voltage-oscillations of the converter. These observations point to the necessity of design optimization for next generation synchronous buck converters. Design optimization is made possible through the analytical model presented in the previous section.

It should be noted that in many power conversion circuits, two transistors are intentionally conducting simultaneously and it is therefore intuitive that the parasitic elements of one transistor may affect the behavior and oscillations in the signals of the other transistor. However, in the synchronous buck converter, Q_1 and Q_2 never intentionally conduct at the same time. It is thus logical to assume that when Q_2 turns on spuriously, the simultaneous cross conduction between Q_1 and Q_2 will lead to different signal oscillations and circuit behaviors than if Q_2 had not turned on falsely. The work presented here demonstrates this phenomenon both analytically and experimentally

6.6 SUMMARY OF CHAPTER 6.0

The occurrence of false turn-on in the synchronous buck converter was investigated, and the interaction between the two MOSFET devices was explored. It was shown that the interaction between the devices is non-trivial and cannot be predicted directly from the device characteristics. Rather, an analytical model was developed based on state-space analysis of the circuit during the moments after application of voltage to the gate of Q_1 . It was shown that an equivalent circuit can be created for the converter at the time of the formation of the channel in

Q_1 , allowing for analysis of the system without relying on complex physics models for the semiconductor devices. This model was shown to closely approximate the experimental response of the circuit during the turn-on of Q_1 , taking into account the impact of the parasitic components of Q_2 . As a result, it was concluded both analytically and experimentally that Q_2 should not be excluded from circuit models of Q_1 during turn-on. Furthermore, the voltages v_{gs1} , v_{ds2} , and v_{gs2} from the analytical model matched the experimental waveforms and clearly demonstrated the ability of the model to predict false turn-on in Q_2 . The ability to accurately model the false turn-on phenomenon will enable system designers to determine the optimal sizes of parasitic components for both Q_1 and Q_2 . This will allow for development of converters with parasitic components which have been optimized for their specific semiconductor devices, striking a balance between minimizing losses from intended switching and retaining enough capacitance to reduce transient high dv/dt effects like false turn-on in next generation faster wide bandgap semiconductor devices. An accurate analytical model is essential for such a process, reducing time and effort necessary to tune the converter to behave optimally. In developing such a model, it was shown that the complex interactions between devices can be accurately modeled and that false turn-on can be closely predicted. This model is intended to offer a better understanding of those interactions while also providing a path towards better design procedures for new generations of devices. Finally, the model and methods in this work can serve as a basis for design optimization techniques for other converters containing faster wide bandgap devices and high dv/dt effects.

7.0 MAXIMUM POWER POINT TRACKING LITERATURE REVIEW

In this chapter, the background and theory of MPPT is discussed. Several state of the art algorithms are discussed along with their advantages and disadvantages. The inherent parasitics of the DC-DC boost converter system which adversely affect the performance of the MPPT controller are also discussed. A potential solution to this problem is presented in the next chapter.

7.1 STATE OF THE ART MPPT CONTROLLERS

Photovoltaic systems are a critical component in addressing the national mandates of achieving energy independence and reducing the potentially harmful environmental effects caused by increased carbon emissions. Due to variations in solar insolation and environmental temperature, photovoltaic systems do not continually deliver their theoretical optimal power unless an adequate maximum power point tracking (MPPT) algorithm is used. Ideally, MPPT algorithms are designed in order for the photovoltaic system to adapt swiftly and precisely to environmental changes so that optimal power is delivered. Power electronic converter systems are typically integrated with the MPPT algorithms where the duty cycle of the converter is controlled in order to deliver maximum available power to the load [80, 81].

Many MPPT control algorithms have already been extensively reported in the literature. The most common of these algorithms is the perturb and observe (P&O) method [82-84]. This control strategy requires external circuitry to repeatedly perturb the array voltage and subsequently measure the resulting change in output power. If the voltage perturbation produces a positive change in power, the direction of the perturbation is continued for the next cycle. If however, the voltage perturbation produces a negative change in output power, the direction of the perturbation is reversed. While P&O is inexpensive and relatively simple, the algorithm is inefficient at steady state because it forces the system to oscillate around the MPP instead of continually tracking it. Furthermore, the P&O algorithm fails under rapidly changing environmental conditions because it cannot discern the difference between changes in power due to environmental effects versus changes in power due to the inherent perturbation of the algorithm [85]. The incremental conductance (INC) method uses the fact that the derivative of the array power with respect to the voltage (Figure 73) is ideally zero at the MPP, positive to the left of the MPP, and negative to the right of the MPP. The INC method has been shown to perform well under rapidly changing environmental conditions, however at the expense of increased response times due to complex hardware and software requirements [86]. The fractional open circuit voltage (FOCV) method uses an approximate relationship between the open circuit voltage of the array, V_{OC} and the array voltage at which maximum power is obtained, V_M , in order to track the MPP [87]. Like P&O, the FOCV algorithm is inexpensive and can be implemented in a fairly straight-forward manner. However, the FOCV method is not a true MPP tracker since the assumed relationship between V_{OC} and V_M is only an approximation. Fuzzy logic and neural network-based algorithms have demonstrated fast convergence and high performance under varying environmental conditions, however the implementation of these

algorithms can be undesirably complex [17, 88]. To this end, a general problem associated with MPPT control algorithms is the transient oscillations in the system's output voltage after the duty cycle is rapidly changed in order to track the MPP [86]. Thus, the ideal MPPT control algorithm would be simple and inexpensive, and would demonstrate rapid convergence to the MPP with minimal oscillation in the output voltage. Shown in Figure 73 are the power-voltage characteristics of a photovoltaic system. The ultimate goal is to force V_{PV} to track V_M .

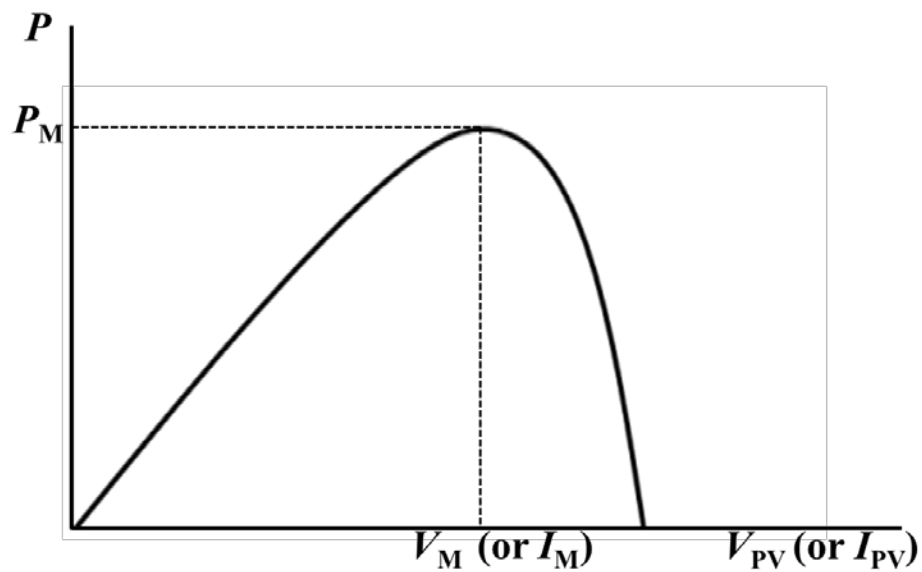


Figure 73: PV characteristics

7.2 PV SYSTEM DESCRIPTION

7.2.1 PV Characteristics

The current-voltage (I-V) characteristics of photovoltaic systems under varying levels of solar insolation are seen in Figure 74. The MPP occurs at the so-called “knee” of the I-V curve, (V_M , I_M) so that when either V_M or I_M is achieved, the maximum available power, P_M is obtained.

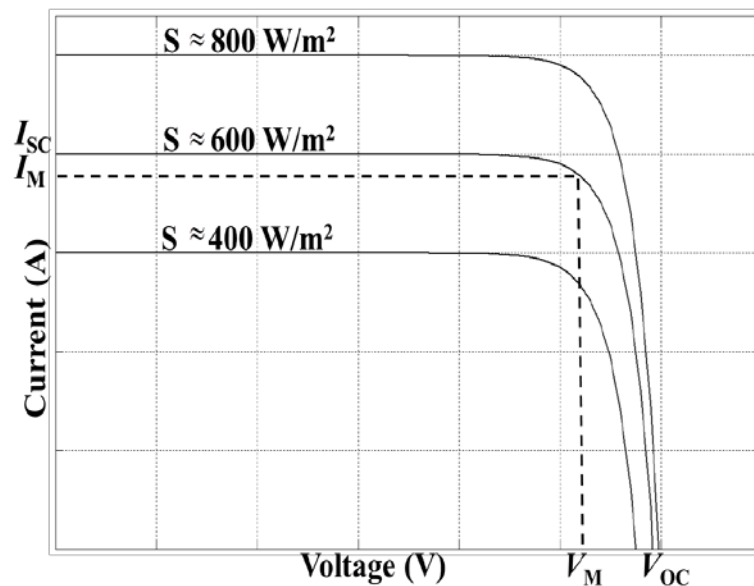


Figure 74: Current-voltage characteristics of PV systems.

By implementing the photovoltaic system with a DC-DC converter interfaced with an MPPT controller, the voltage or current of the solar panel can be regulated so that maximum allowable power is delivered [89, 90]. Shown in Figure 75 is the integration of such a system where a boost converter is utilized to deliver optimal power to the load. Depending on the application, other power converter topologies may be used in place of the boost converter in Figure 75.

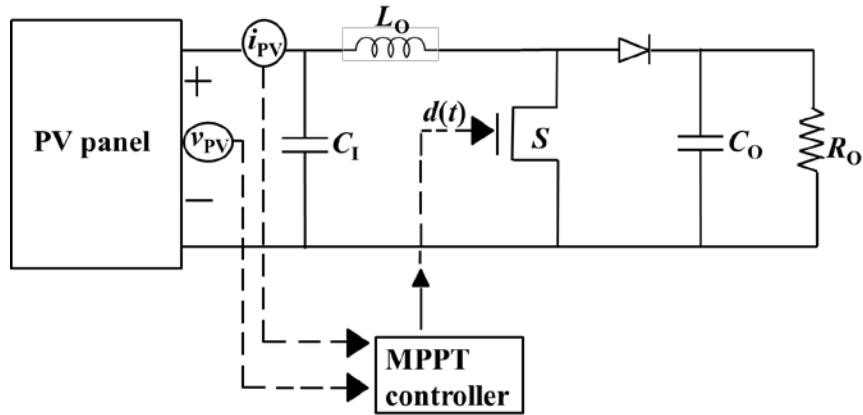


Figure 75: PV boost converter system.

As can be seen from Figure 75, the MPPT controller senses the voltage and current of the solar panel and thus yields a new duty cycle, $d(t)$ to the switching transistor, S of the converter so that maximum power is obtained. In order to analyze the dependence of the array voltage on the duty cycle, it is initially assumed that the input capacitance to the boost converter in Figure 75, C_1 is equal to zero. Thus for boost converters, the duty cycle of the transistor is related to the array voltage through (7.0 -1):

$$v_{pv} = i_{pv} R_O (1-d)^2 \quad (7.0 -1)$$

where v_{pv} and i_{pv} are the array voltage and current respectively, and R_O is the load resistance.

Both the array voltage and current consist of DC terms, V_{PV} and I_{PV} as well as ripple terms, \tilde{v}_{pv} and \tilde{i}_{pv} . The goal then is to design a controller that continually calculates the optimal value of the duty cycle so that V_{PV} tracks V_M or (I_{PV} tracks I_M) thus delivering maximum power.

7.2.2 Converter Dynamics

The relationship given in (7.0 -1) provides the foundation for conventional MPPT algorithms so that the converter's duty cycle can be controlled in order for V_{PV} to track V_M at steady state. Next, it is necessary to consider the dynamics between the duty cycle and array voltage so as to eliminate any transient oscillations in the array voltage after the duty cycle has been updated to account for rapidly changing environmental conditions. Transient oscillations are undesired and can lead to inefficient operation of the system. In order to analyze the transient response of the system, the small signal equivalent circuit of the photovoltaic power conversion system seen in is Figure 76 considered [86].

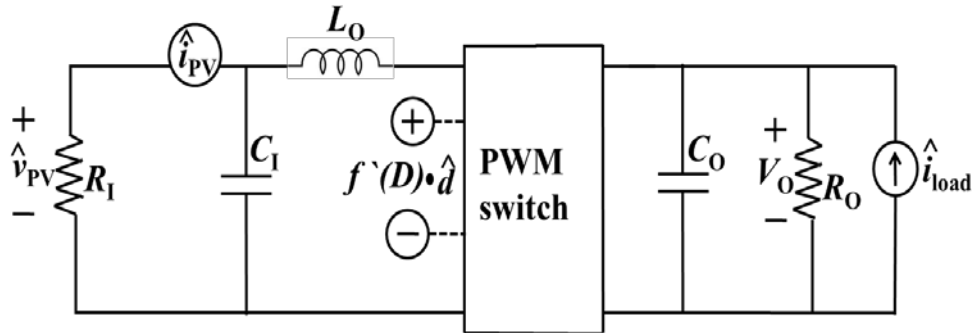


Figure 76: Small signal equivalent circuit for boost converter.

For small signal operation around a single operating point, a resistor R_1 is used to model the solar array with a small signal array voltage \hat{v}_{pv} and small signal array current \hat{i}_{pv} across its terminals. It is necessary to derive the small signal control to array voltage transfer function, G_{vp} so that the dynamics of the system can be studied. In analyzing Figure 76, one can use circuit analysis to express the relationship seen in (7.0 -2):

$$\frac{\hat{v}_{pv}}{R_I} + s \hat{v}_{pv} C_I = \frac{f'(D) \cdot \hat{d} - \hat{v}_{pv}}{sL_O} \quad (7.0 -2)$$

where \hat{d} represents the small signal variation around the converter's duty cycle, and $f'(D)$ is the derivative (with respect to the duty cycle) of the DC steady state relationship between the input and output of a boost converter, $f(D)$. From (7.0 -2), one can then obtain the small signal control to array voltage transfer function G_{vp} as seen in (7.0 -3):

$$G_{vp} = \frac{\hat{v}_{pv}}{\hat{d}} = \frac{f'(D)}{L_O C_I s^2 + \frac{L_O}{R_I} s + 1} \quad (7.0 -3)$$

The known DC steady state relationship between the input and output of a boost converter is given in (7.0 -4).

$$f(D) = V_{PV} = (1 - D)V_O \quad (7.0 -4)$$

In (7.0 -4), V_{PV} and V_O are the steady state DC input and output voltages of the boost converter respectively, and D is the DC component of the duty cycle. The relationship in (7.0 -4) assumes the average values of $f(D)$ and V_{PV} are equivalent and that the DC steady state relation between

$f(D)$ and V_o is un-affected by the transient switching action. From (7.0 -4), the derivative of $f(D)$ with respect to the duty cycle is given in (7.0 -5).

$$f'(D) = -V_o \quad (7.0 -5)$$

Thus, substituting (7.0 -5) into (7.0 -3) and with some rearrangement, the relationship seen in (8.0 -6) is obtained.

$$G_{vp} = \frac{\frac{-V_o}{L_o C_I}}{s^2 + \frac{1}{R_I C_I} s + \frac{1}{L_o C_I}} \quad (7.0 -6)$$

The transfer function in (7.0 -6) is derived from a linearized version of the highly non-linear system seen in Figure 75, around a single operating point. As solar insolation varies, the operating point of the system will vary thereby changing the effective values of the parameters seen in (7.0 -6), specifically R_I . To illustrate the effect of R_I on the system, one can analyze the general form of (7.0 -6) as seen in (7.0 -7).

$$G_{vp} = \frac{\mu \omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \quad (8.0 -7)$$

From inspection of (7.0 -6) and (8.0 -7), the damping ratio, ζ can be calculated as seen in (8.0 -8).

$$\zeta = \frac{1}{2R_I} \sqrt{\frac{L_O}{C_I}} \quad (7.0 -8)$$

For a critically damped system, the value of the damping ratio must approach one. While it is possible to tune the value of R_I to yield a critically damped system for a single operating point, it is not guaranteed that a fixed R_I will produce a critically damped system for varying operating points. This observation leads to the conclusion that an adaptive controller is required to force the value of the damping ratio to one, irrespective of any changes in solar insolation. Using an MRAC controller to optimize the dynamics in (7.0 -6) is the subject of the proposed MPPT algorithm discussed in the next chapter.

7.3 SUMMARY OF CHAPTER 7.0

In order to improve the efficiency of photovoltaic systems, MPPT algorithms are used to deliver maximum available power from the solar array to the load. Critical issues to be considered in MPPT algorithms include system complexity, uncertainty, and dynamic performance. It has been shown that state of the art MPPT control algorithms are unable to compensate for the parasitic effects of the DC-DC boost converter so that the system can converge rapidly to the optimal point.

8.0 MPPT USING RCC AND MODEL REFERENCE ADAPTIVE CONTROL

In this chapter, the proposed implementation of a two-level maximum power point tracking algorithm which consists of ripple correlation control in the first level and model reference adaptive control in the second level is discussed. This unique integration enables the controller to optimize the convergence of the algorithm so that the maximum power point is obtained rapidly with minimal oscillation in the system's output voltage. The objective here is consistent with the objectives in previous chapters - which is to understand how the various parasitic components of power electronic systems influence their dynamic performance. In previous sections, the goal was investigate the effect of the parasitic device components on the performance of power electronic systems. In this section, the circuit parameters of DC-DC boost converters are analyzed in order to assess their influence on the convergence time of MPPT control algorithms.

Proposed here is the development of a two-level MPPT control algorithm which consists of ripple correlation control (RCC) [19, 91, 92] in the first level and model reference adaptive control (MRAC) [93] in the second level. As seen in Figure 77, in the first control level the array voltage, v_{pv} and power p_{pv} serve as the inputs to the RCC unit. The RCC unit then calculates the duty cycle of the system, $d(t)$ so as to deliver the maximum power to the load at steady state. In the second control level, the new duty cycle calculated from the RCC unit is routed into an MRAC architecture, where the dynamics of the entire photovoltaic power conversion system, or equivalently the plant, are improved to eliminate any potential transient oscillations in the

system's output voltage. Transient oscillations in the system's output voltage can result after the duty cycle has been updated to account for rapidly changing environmental conditions. To prevent the plant from displaying such oscillations, a critically damped system is implemented as the reference model in Figure 77. During adaptation, the error between the plant and reference model is utilized to tune the system's adjustment parameters, which are contained in the feedforward and feedback controllers, C_f and C_b , respectively. Properly tuning the adjustment parameters enables the output of the plant to match the output of the reference model, at which point the error converges to zero and maximum power is obtained. Analysis of both the analytical and modeled results to be presented here demonstrates fast convergence to the optimal power point with complete elimination of underdamped responses, which are often observed in photovoltaic power converter systems.

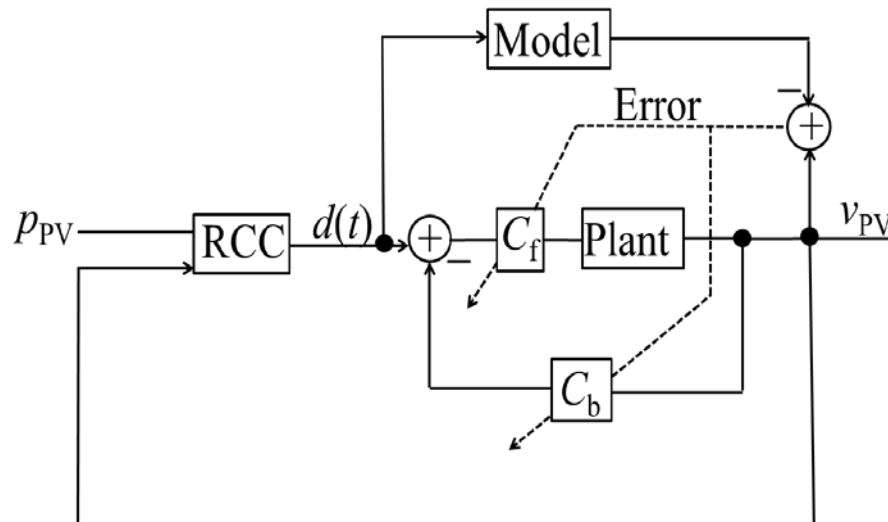


Figure 77: Proposed control algorithm.

It is instructive to note that the previous literature has proven the independent stability of both RCC and MRAC, however it is not necessarily guaranteed that coupling two independently stable algorithms will lead to an overall system that is stable. On the contrary, because the time constants of the two control algorithms used here are significantly disparate, one can effectively decouple the two algorithms so that the system is entirely stable.

8.1 RCC AND MRAC

8.1.1 Ripple Correlation Control

For convenience, the previously derived relationship for a boost converter (7.0 -1), is shown here as (8.0 -1).

$$v_{pv} = i_{pv} R_O (1-d)^2 \quad (8.0 -1)$$

To calculate the duty cycle which delivers maximum power to the load at steady state, RCC is utilized. Recently, RCC was reported in [19], where it was shown that the switching ripple inherent to the converter can be utilized to perturb the system and thus track the MPP. The RCC method is essentially an improved version of P&O, with the exception that the perturbation is already inherent to the converter. Such a methodology is advantageous because it negates the necessity for external circuitry to inject the perturbation. In addition, RCC has been proven to converge asymptotically to the MPP with minimal controller complexity and straight-forward

circuit implementation [19]. The method of RCC is based on the observation that the product of the time-based derivatives of the array voltage and power will be greater than zero to the left of the MPP (from inspection of Figure 73), and less than zero to the right of the MPP and exactly zero at the MPP. This can be illustrated quantitatively in (8.0 -2) – (8.0 -3).

When V_{PV} is less than V_M :

$$\tilde{p}_{pv} \cdot \tilde{v}_{pv} > 0 \quad (8.0 -2)$$

For V_{PV} greater than V_M :

$$\tilde{p}_{pv} \cdot \tilde{v}_{pv} < 0 \quad (8.0 -3)$$

and when V_{PV} is equal to V_M :

$$\tilde{p}_{pv} \cdot \tilde{v}_{pv} = 0. \quad (8.0 -4)$$

These observations lead to the control law derived in [19] as seen in (8.0 -5):

$$d = k \int (\tilde{p}_{pv} \cdot \tilde{v}_{pv}) dt \quad (8.0 -5)$$

where \hat{p}_{pv} and \hat{v}_{pv} are the ripple components of the array power and voltage, respectively and k is a constant of negative gain. From (8.0 -1) in, it is clear v_{pv} is a monotonic decreasing function of d and therefore using a negative k reverses the direction of the system. As a result, (8.0 -5) can

be qualitatively described as follows: if v_{pv} increases and there is a resulting increase in p_{pv} , the system's operating point is to the left of the MPP (Figure 73) and therefore d decreases according to (8.0 -1) in. If p_{pv} decreases after an increase in v_{pv} , then d should increase. From inspection of (8.0 -4) and (8.0 -5), the goal then is to drive the time-based derivative of d to zero so that maximum power is obtained. As established in [19], RCC has a well-developed theoretical basis and has been mathematically proven to yield the optimal value of the duty cycle in order to deliver maximum power at steady state. The advantage of RCC over conventional algorithms such as P&O, is that at steady state RCC converges to the MPP while P&O oscillates around the MPP. Relative to fuzzy logic and neural networks, RCC is advantageous due to its simple implementation as well as its low cost. In [19], it was demonstrated that RCC can be implemented using inexpensive analog circuitry for less than \$10.00.

In addition to steady state analysis, one must also consider the transient response of the photovoltaic boost converter power conversion system shown in Figure 75 so that the controller can rapidly converge to the theoretical MPP with minimal oscillation. In the next section, an adaptive control algorithm is proposed in order to prevent the array voltage from exhibiting an underdamped response.

8.1.2 Proposed MRAC Method

In the previous section, RCC was used to calculate the duty cycle which delivers the maximum available power at steady state. It is also desired that the system converges to the MPP swiftly during rapid changes in solar insolation. As shown in (7.0 -6) in Section 7.2.2 which is copied below for convenience as (8.0 -6), the relationship between the array voltage and the converter

duty cycle is a highly dynamic process. Please refer back to Section 7.2.2 for a detailed analysis of the derivation of (8.0 -6).

$$G_{vp} = \frac{\frac{-V_o}{L_o C_I}}{s^2 + \frac{1}{R_I C_I} s + \frac{1}{L_o C_I}} \quad (8.0 -6)$$

Since the operating point will vary as solar insolation varies, it is never guaranteed that the array voltage exhibits critically damped behavior without adaptive control. The MRAC architecture shown in Figure 77 is proposed so that the array voltage demonstrates critically damped behavior. The input to the overall system, d is the duty cycle calculated in the previous section using RCC. The plant model in Figure 77 corresponds to the small signal control to array transfer function seen in (8.0 -6).

The fundamental objective of MRAC is to design an adaptive controller so that the response of the controlled plant remains close to the response of a reference model with desired dynamics, despite uncertainties or variations in the plant parameters. The proposed architecture of MRAC is shown in Figure 78 and Figure 79.

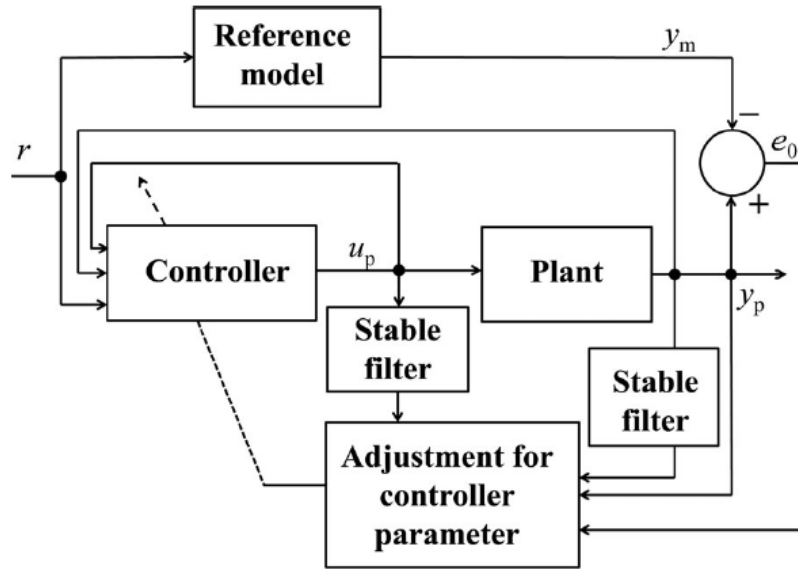


Figure 78: MRAC structure.

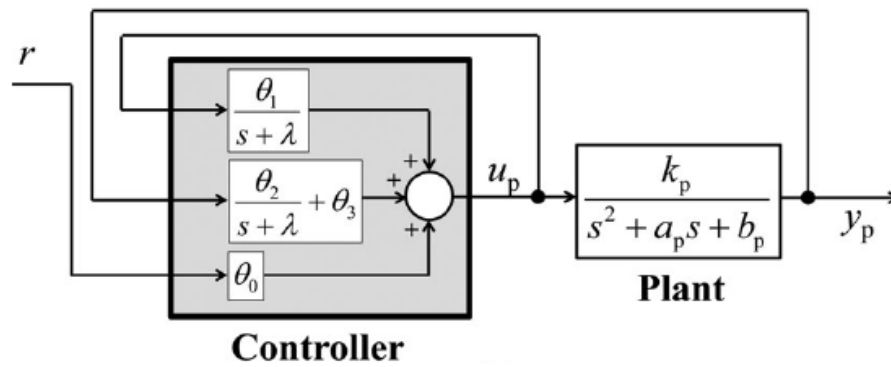


Figure 79: Controller structure in the proposed MRAC.

The input to the overall system, $r(t)$, is the change in duty cycle calculated in by the RCC unit in Section 8.1.1. The plant model in Figure 78 corresponds to the transfer function in (8.0 - 6). However, for convenience, we change its sign (by multiplying -1 to it) so that the plant model has only positive coefficients. We use $u_p(t)$ and $y_p(t)$ to reproduce the input and output of the plant, respectively, and re-express the plant model as

$$G_{vp} = \frac{y_p(s)}{u_p(s)} = \frac{k_p}{s^2 + a_p s + b_p}. \quad (8.0 -7a)$$

Where the values and meanings of k_p , a_p , and b_p can be implied from (8.0 -7a). The reference model is chosen to exhibit desired output $y_m(t)$ and input $r(t)$

$$G_m = \frac{y_m(s)}{r(s)} = \frac{k_m}{s^2 + a_m s + b_m} \quad (8.0 -7b)$$

Where k_m is a positive gain, and a_m and b_m are determined so that the reference model delivers a critically damped step response. The control objective is to design $u_p(t)$ so that $y_p(t)$ asymptotically tracks $y_m(t)$.

In the following, we take four steps to derive the adaptation law for controller parameters in MRAC: 1) choosing the controller structure; 2) finding state-space expressions for the controlled plant and the reference models; 3) constructing error equations; and 4) deriving an adaptation law for MRAC using the Lyapunov method.

A. Controller Structure: To achieve the control objective, we use the controller structure shown in Figure 79. The expression for the controller is

$$\begin{aligned}
u_p &= \theta_0 r + \theta_1 \frac{1}{s + \lambda} u_p + \theta_2 \frac{1}{s + \lambda} y_p + \theta_3 y_p \quad (8.0-8) \\
&= \theta_0 r + \theta_1 \omega_1 + \theta_2 \omega_2 + \theta_3 y_p = \theta^T \omega
\end{aligned}$$

Where $\theta = [\theta_0, \theta_1, \theta_2, \theta_3]^T$ is the parameter vector of the controller, ω is defined as

$\theta = [r, \omega_1, \omega_2, y_p]^T$ with $\omega_1 = \frac{1}{s + \lambda} u_p$ and $\omega_2 = \frac{1}{s + \lambda} y_p$, and $\frac{1}{s + \lambda}$ is a stable filter with an

arbitrarily chosen $\lambda > 0$. Equivalently, ω_1 and ω_2 are determined by

$$\begin{aligned}
\dot{\omega}_1 &= -\lambda \omega_1 + u_p \\
\dot{\omega}_2 &= -\lambda \omega_2 + y_p
\end{aligned} \quad (8.0-9)$$

It has been shown in previous adaptive control references that the controller shown in (8.0-8) is adequate to achieve the control objective: it is possible to make the transfer function from r to y_p equal to the transfer function shown in (8.0-7). Specifically, $y_p(s)/r(s)$ equals

$y_m(s)/r(s)$ when θ equals $\theta^* = [\theta_0^*, \theta_1^*, \theta_2^*, \theta_3^*]^T$ with

$$\theta_0^* = \frac{k_m}{k_p}$$

$$\theta_1^* = a_p - a_m$$

$$\theta_2^* = \frac{(a_p - a_m)(-\lambda^2 + \lambda a_p - b_p)}{k_p}$$

$$\theta_3^* = \frac{(b_p - b_m) + (a_p - a_m)(\lambda - a_p)}{k_p} \quad (8.0 -10)$$

B. State-Space Expressions of the Controlled Plant and the Reference Model: Let $\{A_p, B_p, C_p\}$ be a minimal realization of the plant $G_p(s)$

$$\dot{x}_p = A_p x_p + B_p u_p$$

$$y_p = C_p x_p \quad (8.0 -11)$$

Where x_p is a 2-D state vector. Consider the dynamics of the controller, i.e., (8.0 -8) and (8.0 -9), the closed-loop system with the plant and controller in the loop can be described by the following state-space expression:

$$\dot{x}_{pe} = A_{pe} x_{pe} + B_{pe} \theta_0^* r + B_{pe} (u_p - \theta^{*T} \omega)$$

$$y_p = C_{pe} x_{pe} \quad (8.0 -12)$$

Where x_{pe} is an extended vector defined by $[x_p^T, \omega_1, \omega_2]^T$, θ^* is determined by (8.0 -10), and matrices A_{pe} , B_{pe} , and C_{pe} are defined by

$$A_{pe} = \begin{bmatrix} A_p + \theta_3^* B_p C_p & \theta_1^* B_p & \theta_2^* B_p \\ \theta_3^* C_p & -\lambda + \theta_1^* & \theta_2^* \\ C_p & 0 & -\lambda \end{bmatrix}$$

$$B_{pe} = \begin{bmatrix} B_p \\ 1 \\ 0 \end{bmatrix}$$

$$C_{pe} = [C_p \quad 0 \quad 0] \quad (8.0 -13)$$

Note that, when $u_p = \theta^{*T} \omega$, (8.0 -12) becomes

$$\dot{x}_{pe} = A_{pe} x_{pe} + \theta_0^* B_{pe} r$$

$$y_p = C_{pe} x_{pe} \quad (8.0 -14)$$

Meanwhile $u_p = \theta^{*T} \omega$ also implies $y_p(s)/r(s) = y_m(s)/r(s)$. Therefore, $\{A_p, \theta_0^* B_{pe}, C_p\}$ should be a realization of the reference model. In other words, the reference model can be realized by the following state-space expression:

$$\dot{x}_{me} = A_{pe} x_{me} + \theta_0^* B_{pe} r$$

$$y_m = C_{pe} x_{me} \quad (8.0 -15)$$

Where x_{me} is the four dimensional state vector of the aforementioned realization. It can be verified that A_{pe} is asymptotically stable.

C. *Error Equations:* By subtracting the reference model's state-space equation (8.0 -15) from the plant's state-space equation (8.0 -12), the state-space equations for the state error, controller parameter error, and the tracking error are obtained as follows:

$$\dot{e} = A_{pe} e + B_{pe} (u_p - \theta^{*T} \omega) = A_{pe} e + B_{pe} \tilde{\theta}^T \omega$$

$$e_0 = C_{pe} \cdot \quad (8.0 -16)$$

Where e , e_0 , and $\tilde{\theta}$ represent the state error, tracking error (output error), and controller-parameter error, respectively

$$e = x_{pe} - x_{me}$$

$$e_0 = y_p - y_m$$

$$\tilde{\theta} = \theta - \theta^*. \quad (8.0 -17)$$

In finding the adaptation law for the controller by means of the Lyapunov function, the input-output transfer function of a state error-equation should be strictly positive and real (SPR). However, the transfer function of the realization $\{A_p, B_{pe}, C_p\}$ in (8.0 -16) is not SPR, because $C_{pe}(sI - A_{pe})^{-1}B_{pe}$ equals $G_m(s)/\theta_0^*$ according to (8.0 -15) and the relative degree of $G_m(s)$ is two, which implies that $G_m(s)/\theta_0^*$ is not SPR.

To overcome the aforementioned difficulty, we use the identity $(s+g)(s+g)^{-1} = 1$ for some $g > 0$ and thus (8.0 -16) can be rewritten as

$$\dot{e} = A_{pe}e + B_{pe} \left\{ (s+g)(u_g - \theta^{*T} \phi) \right\} = A_{pe}e + B_{pe} \left\{ (s+g) \tilde{\theta}^T \phi \right\}$$

$$e_0 = C_{pe}e. \quad (8.0 -18)$$

Where $u_g = \frac{1}{s+g}u_p$ and $\phi = \frac{1}{s+g}\omega$. The term $s+g$ will increase the degree of the numerator to

make the relative degree of the transfer function equal to one. Since $u_g = \theta^T \phi$, the controller can

be expressed as $u_p = (s+g)u_g = \dot{\theta}^T \phi + \theta^T \dot{\phi} + g\theta^T \phi = \dot{\theta}^T \phi + \theta^T (\dot{\phi} + g\phi) = \dot{\theta}^T \phi + \theta^T \omega$

Now introduce

$$\bar{e} = e - B_{pe} \tilde{\theta}^T \phi \quad (8.0-19)$$

Then, we can derive

$$\frac{d}{dt} \bar{e} = A_{pe} \bar{e} + (A_{pe} B_{pe} + gB_{pe}) \tilde{\theta}^T \phi$$

$$e_0 = C_{pe} \bar{e} + C_{pe} B_{pe} \tilde{\theta}^T \phi \quad (8.0-20)$$

Denoting $B_1 = A_{pe} B_{pe} + gB_{pe}$ and noting that $C_{pe} B_{pe}$ equals 0 (because the relative degree of the reference model is two), we have

$$\frac{d}{dt} \bar{e} = A_{pe} \bar{e} + B_1 \tilde{\theta}^T \phi$$

$$e_0 = C_{pe} \bar{e}. \quad (8.0-21)$$

For the new state-error equation (8.0 -21), its transfer function from $\tilde{\theta}^T \phi$ to e_0 should be the same as the transfer function from $\tilde{\theta}^T \phi$ to e_0 in (8.0 -18) because (8.0 -21) is equivalently transformed from (8.0 -18). Therefore the realization $\{A_p, B_1, C_p\}$ has the following transfer function:

$$\begin{aligned}
 C_{pe}(sI - A_{pe})^{-1}B_1 &= C_{pe}(sI - A_{pe})^{-1}B_{pe}(s + g) \\
 &= (s + g)\frac{G_m}{\theta_0^*} \\
 &= \frac{k_m}{\theta_0^*} \cdot \frac{s + g}{s^2 + a_m s + b_m}. \tag{8.0 -22}
 \end{aligned}$$

Where the positive constant g is chosen to be less than a_m . It can be shown that (8.0 -22) is SPR for any g satisfying $0 < g < a_m$.

D. *Derivation of the Adaptation Law:* To derive the adaptation law for controller parameters, we construct a Lyapunov function that has two error vectors – the controller parameter error $\tilde{\theta}$ and the state error \bar{e}

$$V(\tilde{\theta}, \bar{e}) = \frac{\bar{e}^T P \bar{e}}{2} + \frac{\tilde{\theta}^T \Gamma^{-1} \tilde{\theta}}{2} \tag{8.0 -23}$$

Where Γ is an arbitrary symmetric positive definite matrix and P is a symmetric positive definite matrix determined using Meyer-Kalman-Yakubovic (MKY) Lemma. According to MKY Lemma, since A_{pe} is stable and $\{A_{pe}, B_1, C_{pe}\}$ is a realization of the SPR transfer function (8.0 - 22), there exists a symmetric positive definite matrix P , a vector q , and a scalar $\nu > 0$ such that the following is true for any given matrix.

$$\begin{aligned} PA_{pe} + A_{pe}^T P_1 &= -qq^T - \nu L \\ PB_1 &= C_{pe}^T \end{aligned} \quad (8.0 -24)$$

Matrix P in (8.0 -23) satisfies (8.0 -24). The time-derivative of the Lyapunov function (8.0 -23) along the solution of (8.0 -21) can be calculated as

$$\dot{V}(\tilde{\theta}, \bar{e}) = -\frac{\bar{e}^T qq^T \bar{e}}{2} - \frac{\nu \bar{e}^T L \bar{e}}{2} + \bar{e}^T PB_1 \tilde{\theta}^T \phi + \tilde{\theta}^T \Gamma^{-1} \frac{d}{dt} \tilde{\theta}. \quad (8.0 -25)$$

Since $\bar{e}^T PB_1 = \bar{e}^T C_{pe}^T = e_0$, we can choose

$$\dot{\tilde{\theta}} = \frac{d}{dt} \tilde{\theta} = -\Gamma e_0 \phi. \quad (8.0 -26)$$

Therefore, we arrive at the expression seen in (8.0 -27).

$$\dot{V}(\tilde{\theta}, \bar{e}) = -\frac{\bar{e}^T qq^T \bar{e}}{2} - \frac{\nu \bar{e}^T L \bar{e}}{2} \leq 0. \quad (8.0 -27)$$

Under the adaptation law (8.0 -26), the conditions shown in (8.0 -27) will always be satisfied, which guarantees that the tracking error and control parameter error are both stable and bounded. According to the derivations above, the overall MRAC rules can be concluded as follows:

$$\dot{\omega}_1 = -\lambda\omega_1 + u_p$$

$$\dot{\omega}_2 = -\lambda\omega_2 + y_p$$

$$\dot{\phi} = -g\phi + \omega, \quad \omega = [r, \omega_1, \omega_2, y_p]^T \quad (8.0-28)$$

$$u_p = \theta^T \omega + \dot{\theta}^T \phi = \theta^T \omega - \phi^T \Gamma e_0 \dot{\phi}$$

$$\dot{\theta} = -\Gamma e_0 \dot{\phi}$$

8.2 RESULTS AND DISCUSSION

The adaptive controller presented in the previous section was then simulated for verification. The values of the boost converter parameters which yield an underdamped system are shown in Table 7. The plant and controller parameters are listed in Table 8. The plant model was chosen to deliver an actual array voltage with an underdamped step response. The reference model was designed to deliver a theoretical MPP voltage with a critically damped step response. Its damping ratio which equals $\frac{a_m}{2\sqrt{b_m}}$ is the determining factor as inferred from (8.0 -8).

Table 7: Boost Converter Parameter Values

Circuit Parameter	Value
R_1	45 Ω
L_0	600 μH
C_1	100 μF
V_0	350 V

Table 8: Parameters used for adaptive controller

Parameter	Value
$k_p = \frac{V_o}{L_o C_o}$	$5.83 \times 10^9 V (rad / s)^2$
$a_p = \frac{1}{R_l C_l}$	$222 rad/s$
$b_p = \frac{1}{L_o C_l}$	$1.67 \times 10^7 (rad / s)^2$
k_m	$5.83 \times 10^9 V (rad / s)^2$
a_m	$8.17 \times 10^3 rad / s$
b_m	$1.67 \times 10^7 (rad / s)^2$
λ	1
g	1
Γ	$5 \times$ identity matrix

Normally, the ratio is chosen to be either exactly 1 or slightly less than 1. In the latter case, the step response rises faster at the cost of slight overshoot. The desired outcome of simulation would be that after the plant has undergone the adaptation phase, the parameters of the controlled plant would converge to the parameters of the reference model and thus the adapted array voltage would show critically damped behavior.

Shown in Figure 80 and Figure 81 is a comparison between the actual adapted array voltage (using MRAC) and the theoretical MPP voltage, where a square pulse width modulated signal is used to simulate the continued update of the duty cycle due to the variance in solar insolation. For comparison purpose, both Figure 80 and Figure 81 show the un-adapted array

voltage (without using MRAC). The scale in both Figure 80 and Figure 81 and subsequent figures has been normalized to an interval between 0 and 1 V. The control intervals are divided into three sub-stages. In the early stage shown in Figure 80, the adapted array voltage oscillates considerably more than both the theoretical MPP voltage as well as the un-adapted array voltage. However, within 4 ms, the plant starts to learn and the adapted array voltage begins to dampen while the un-adapted array voltage continues to oscillate. Eventually, both the adapted array voltage and the un-adapted array voltage reach the theoretical steady-state MPP voltage. This demonstrates the accuracy of RCC and its ability to calculate the correct optimal duty cycle which can deliver maximum available power in the steady state. Then at 12 ms, the solar insolation changes and the un-adapted voltage shows an underdamped response. At this point, the adapted voltage also diverges slightly away from the theoretical MPP. This change in solar insolation represents the first time the ambient conditions have altered after the adapted array voltage has reached a steady-state value. Thus, the plant must learn to adapt to such a change in solar insolation. However, the adapted array voltage in Figure 80 shows no oscillatory response

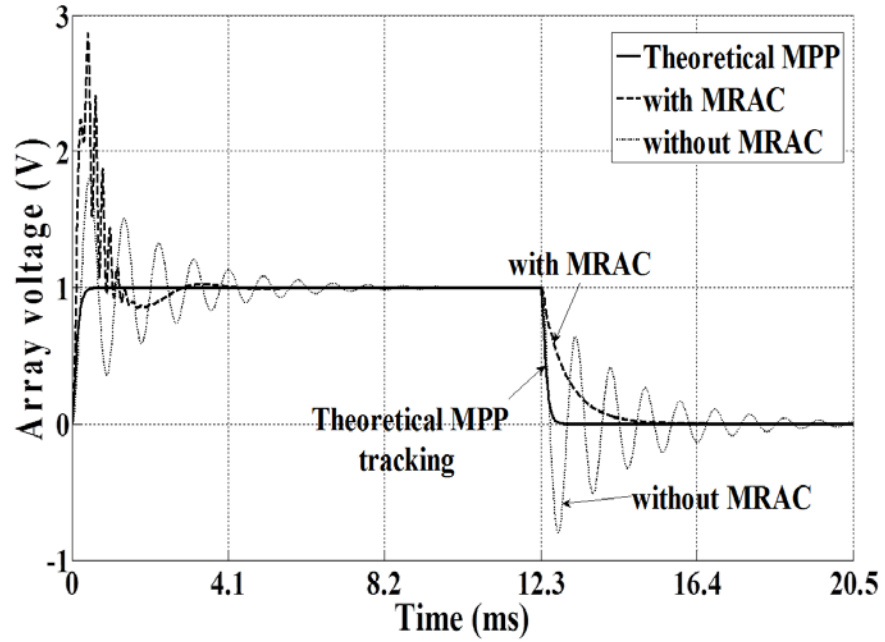


Figure 80: Early adaptation stage, with MRAC vs without MRAC.

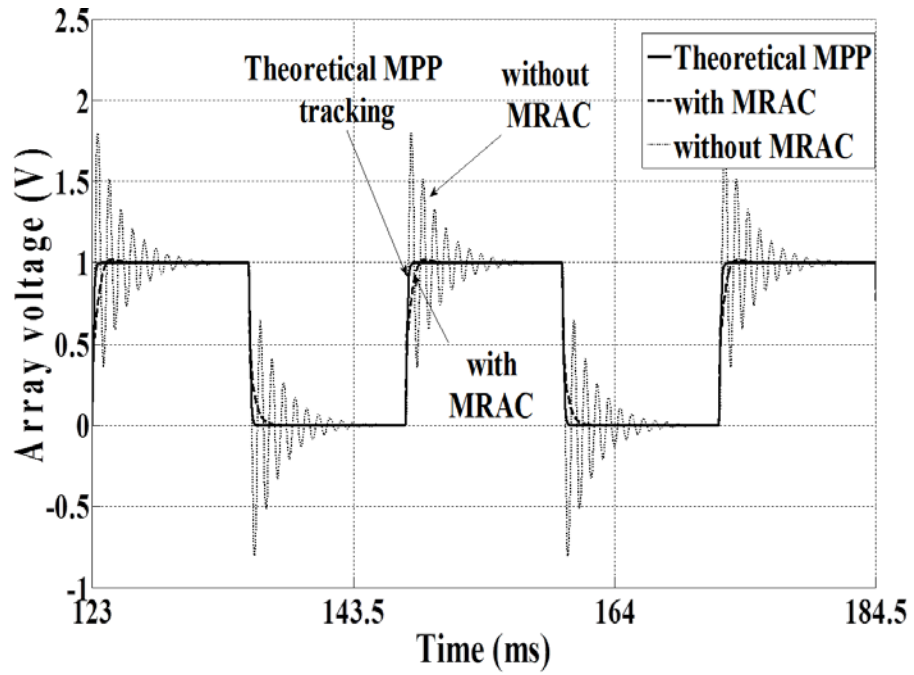


Figure 81: Middle adaptation stage, with MRAC vs without MRAC.

even after the first change in sunlight at 12 ms. That is one of the goals of this study, which is to eliminate any potential underdamped response by the plant due to rapid changes in solar insolation. Next, the adapted array voltage should continue to learn, and converge to the theoretical MPP during the transient changes in solar insolation as shown in Figure 81. In the middle stage of adaptation shown in Figure 81, the adapted array voltage has almost completely converged to the theoretical MPP after only 120 ms, even during changes in solar insolation. Conversely, the un-adapted array voltage continues to oscillate at each change in solar insolation. In observing the parabolic-like solar array characteristic in Figure 73, it can be inferred that during changes in solar insolation, the un-adapted array voltage fluctuates to the left and right of the MPP, before finally reaching the MPP. On the other hand, the adapted array voltage converges directly to the theoretical MPP with no fluctuation.

The observations from both Figure 80 and Figure 81 are supplemented in Figure 82 and Figure 83, where the error between the actual adapted array voltage and the theoretical MPP is shown. The error between the un-adapted and theoretical MPP is also shown in both Figure 82 and Figure 83. As seen in Figure 82, in the early control stage the error for the adapted array voltage is significant. This is consistent with the violent oscillations observed in the adapted array voltage seen in Figure 80. However, after the initial learning phase, the error in both the adapted array voltage and theoretical MPP voltage converges to zero in the steady state. As previously stated, the solar insolation changes at 12 ms, and there is a transient error in both the adapted array voltage as well as the un-adapted array voltage. Comparatively, the error for the adapted array voltage is smaller in magnitude and time duration.

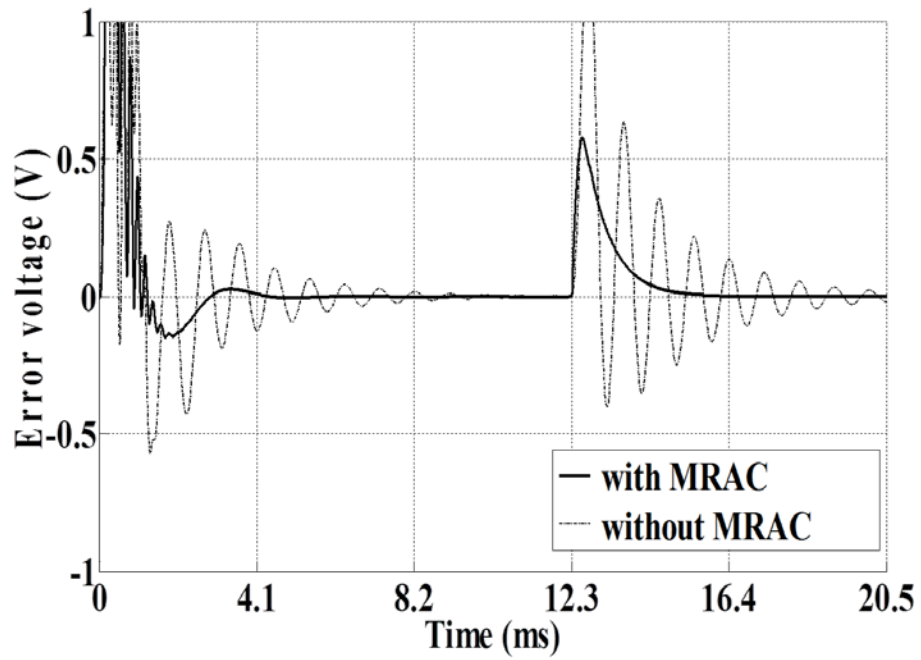


Figure 82: Error signal. Early adaptation stage, with MRAC vs without MRAC.

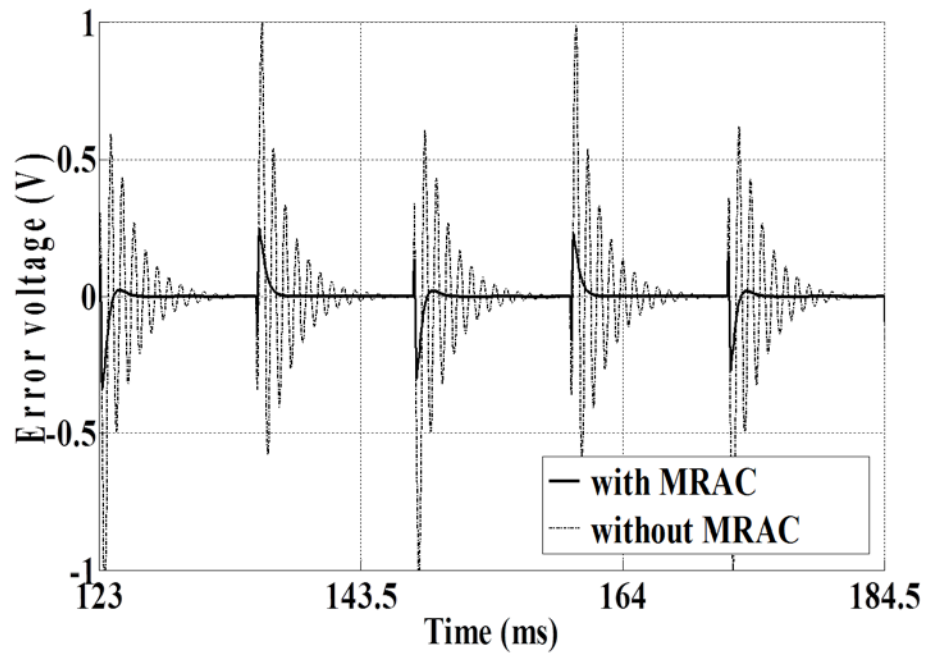


Figure 83: Error signal. Middle adaptation stage, with MRAC vs without MRAC.

Then in the middle stage of adaptation shown in Figure 83, the adapted array voltage error during each transient change in solar insolation is significantly smaller than seen in the initial phase. Conversely, the un-adapted array voltage error continues to oscillate with a larger magnitude and time-duration than the adapted array voltage.

Shown in Figure 84 is a comparison between the three systems in the late adaptation stage. As seen in Figure 84, the adapted array voltage has completely converged to the theoretical MPP voltage. The frequency response of the MRAC-adapted system and un-adapted system is shown in Figure 85. For ease of comparison, both the adapted and un-adapted systems are normalized to have unity DC gains. Clearly, the un-adapted system attains its peak value of magnitude at about its natural frequency. The amplified magnitudes near the natural frequency indicate resonant behaviors when the system is excited at frequencies close to the natural frequency. The peak also implies that the system has underdamped transient responses. In contrast, the adapted system exhibits no “hump” in the range of higher frequencies including the natural frequency - the MRAC regulation is able to remove the underdamped modes and correct the resonant behavior of the original plant. Therefore Figure 85 illustrates the robust ability of the controller to eliminate potential transient oscillations. A comparison between the nominal controller’s parameters and the updated controller’s parameters is shown in Table 9. Reasonable agreement is obtained thereby demonstrating that the controller parameters will converge to the ideal ones.

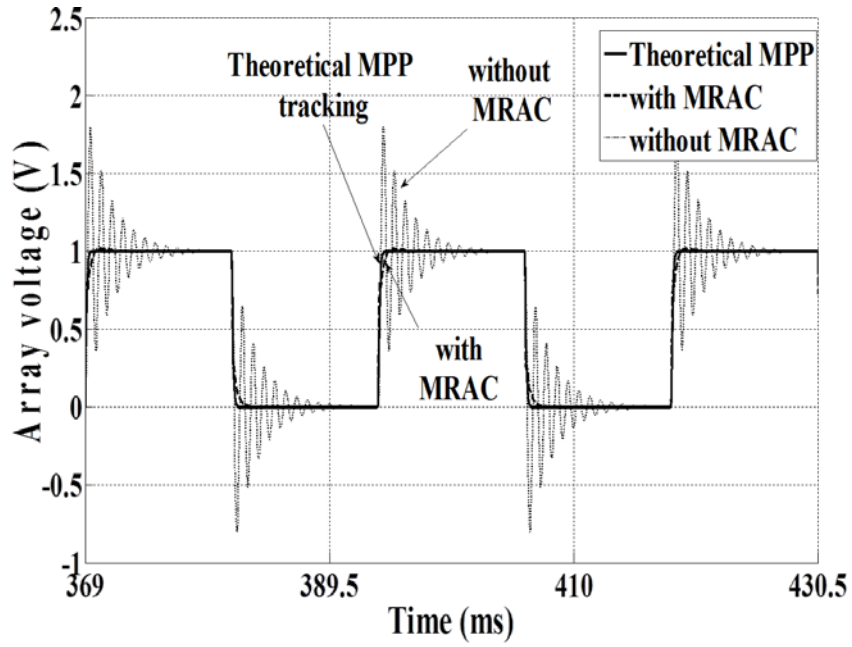


Figure 84: Late adaptation stage, with MRAC vs without MRAC.

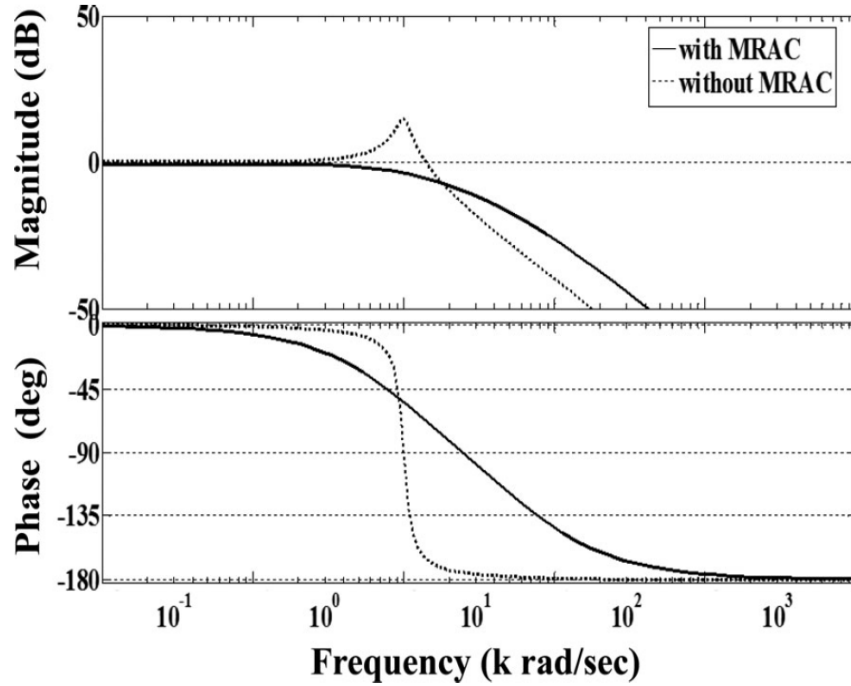


Figure 85: Frequency response of system with and without MRAC.

Table 9: Comparison between the nominal and actual controller parameters

	θ_0	θ_1	θ_2	θ_3
Nominal controller parameters	1.00	-7.95×10^3	-22.8	-3.00×10^{-4}
Updated controller parameters	1.00	-8.12×10^3	-20.4	-2.80×10^{-4}

8.3 SUMMARY OF CHAPTER 8.0

In order to improve the efficiency of photovoltaic systems, MPPT algorithms are used to deliver maximum available power from the solar array to the load. Critical issues to be considered in MPPT algorithms include system complexity, uncertainty, and dynamic performance. This work developed a two-level adaptive control architecture that can reduce complexity in system control and effectively handle the uncertainties and perturbations in the photovoltaic systems and the environment. The first level of control was RCC, and the second level was MRAC. This work focused mostly on the design of the MRAC algorithm, which compensated the underdamped characteristics of the power conversion system.

9.0 CONCLUSION

The objective of this dissertation was to investigate the effects that the parasitic converter components have on the performance of future generation power conversion systems. At the device level, the effect of the parasitic transistor capacitances was assessed analytically and experimentally. In Chapter 4.0 equivalent device models for GaN HFETs were developed in SaberRD in order to assess the effect of the parasitic capacitances on these devices. The methods used for this study followed model development algorithms similar to those previously reported in the literature. The models were validated by comparing simulated gate charge characteristics from the model with the experimental gate charge results as reported on the datasheets and good agreement has been obtained. The models were further validated by comparing extracted device model parameters with device parameters reported on the manufacturer's datasheets, again with adequate agreement. The device models were simulated in standard switching test circuits, from which the results are comparable with experimental results also reported in the literature for devices of similar ratings and sizes.

The results from the analysis presented in Chapter 4.0 support the remarks made in [31], where the manufacturers of the GaN devices reported that C_{GD} is most crucial in device switching. Clearly, the data reported in this chapter substantiate this claim. Also, it has been concluded that the optimization of both C_{GS} and C_{DS} is crucial for GaN power device switching applications. For C_{GS} , an optimal value must be found so that the device is capable of fast turn-on and so that the

device is not forced into conduction spuriously in synchronous buck converters and other multi-device converters. For C_{DS} , further optimization could significantly reduce the turn-off losses of the device while still allowing the device to retain its fast switching behavior. As the demand for faster, more efficient and more robust power switching devices continues to increase, designers of GaN power devices must consider the area of their intended device and how the resulting capacitance could affect the switching performance of the device. The data presented in Chapter 4.0 illustrates the effect that each parasitic capacitance can have on the switching performance of GaN power devices as well as the role each capacitance could play in GaN devices of higher voltage.

In Chapter 5.0 an analytical methodology for evaluating the Cdv/dt induced false turn-on in SiC MOSFETs was presented. The model presented in Chapter 5.0 enables one to assess the influence of the parasitic device parameters on the damping ratio and natural frequency of the drain-source voltage. In addition, the influence of the parasitic capacitances on the induced gate-source voltage has been investigated. The analytical results presented in Chapter 5.0 have been validated with experimental data and adequate agreement has been obtained. As device performance capabilities increase, the methods reported here can be beneficial in the design of high voltage synchronous buck converters, or other power conversion circuits containing multiple switching devices and high dv/dt . Again, it should be noted that the findings in Chapter 5.0 are unique to the particular circuit topology used, however those findings still provide a method for modeling Cdv/dt false turn-on which can be extrapolated to other desired circuits.

In Chapter 6.0 the occurrence of false turn-on in the synchronous buck converter was investigated, and the interaction between the two MOSFET devices was explored. It was shown that the interaction between the devices is non-trivial and cannot be predicted directly from the

device characteristics. Rather, an analytical model was developed based on state-space analysis of the circuit during the moments after application of voltage to the gate of Q_1 . It was shown that an equivalent circuit can be created for the converter at the time of the formation of the channel in Q_1 , allowing for analysis of the system without relying on complex physics models for the semiconductor devices. This model was shown to closely approximate the experimental response of the circuit during the turn-on of Q_1 , taking into account the impact of the parasitic components of Q_2 . As a result, it was concluded both analytically and experimentally that Q_2 should not be excluded from circuit models of Q_1 during turn-on. Furthermore, the voltages v_{gs1} , v_{ds2} , and v_{gs2} from the analytical model matched the experimental waveforms and clearly demonstrated the ability of the model to predict false turn-on in Q_2 . The ability to accurately model the false turn-on phenomenon will enable system designers to determine the optimal sizes of parasitic components for both Q_1 and Q_2 . This will allow for development of converters with parasitic components which have been optimized for their specific semiconductor devices, striking a balance between minimizing losses from intended switching and retaining enough capacitance to reduce transient high dv/dt effects like false turn-on in next generation faster wide bandgap semiconductor devices. An accurate analytical model is essential for such a process, reducing time and effort necessary to tune the converter to behave optimally. In developing such a model, it was shown that the complex interactions between devices can be accurately modeled and that false turn-on can be closely predicted. This model is intended to offer a better understanding of those interactions while also providing a path towards better design procedures for new generations of devices. Finally, the model and methods in Chapter 6.0 can serve as a basis for design optimization techniques for other converters containing faster wide bandgap devices and high dv/dt effects.

Chapter 8.0 presents a novel two level controller for maximum power point tracking (MPPT) in photovoltaic power conversion systems. MPPT technologies have been used in photovoltaic systems to deliver the maximum available power to the load under changes in solar insolation and ambient temperature. To improve the performance of MPPT, the work presented in Chapter 8.0 develops a two-level adaptive control architecture that can reduce complexity in system control and effectively handle the uncertainties and perturbations in the photovoltaic systems and the environment. The first level of control is ripple correlation control (RCC), and the second level is model reference adaptive control (MRAC). By decoupling these two control algorithms, the system achieves MPPT with overall system stability. The work presented in Chapter 8.0 compensates for the underdamped system inherent to photovoltaic power conversion circuits. The original transfer function of the power conversion system has time-varying parameters, and its step response contains oscillatory transients that vanish slowly. Using the Lyapunov approach, an adaptation law of the controller was derived for the MRAC system to eliminate the underdamped modes in power conversion. It was shown in Chapter 8.0 that the proposed control algorithm enables the system to converge to the MPP within milliseconds.

Finally, the work developed in this dissertation presents a unique opportunity to develop a high frequency power conversion system employing WBG devices and MRAC MPPT control. The ability of the WBG device to maintain adequate performance under high switching frequencies, in addition to the MRAC's ability to converge to the MPP faster under high switching frequencies allows for an optimized power density converter with minimal switching and conduction loss. This will be the subject of future work within the devices group in ECE Pitt as well as the subject of my future career work.

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