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Research Article

Comparative Study of Resistorless Filters Using Differential Voltage Current Controlled Current Feedback Operational Amplifiers and Differential Voltage Current Controlled Current Conveyors

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Differential Voltage Current Controlled Current Feedback Operational Amplifier is an attractive active element for realizing resistorless filters with a minimum active component count. This is verified through a design example, where a 3rd-order leapfrog filter has been realized using the AMS 0.35 μm CMOS process design kit. The performance of the Differential Voltage Current Controlled Current Feedback Operational Amplifier filter is evaluated and compared with that obtained by the corresponding filter, where Differential Voltage Current Controlled Current Conveyors have been employed.

1. Introduction

The Current Feedback Operational Amplifier (CFOA) is a four terminal active element which offers particularly higher speed, higher slew rate, and better bandwidth than those achieved by the conventional voltage-mode op amps [1, 2]. A number of CFOA topologies with terminals of single type have been already introduced in the literature [3–6]. Enhanced CFOA topologies, including Fully Differential CFOAs (FDCFOAs) [7–10], Differential Voltage CFOAs (DVCFOAs) [11, 12], have been also published. Comparative studies of CFOAs and DVCFOAs have been performed in [4, 13], respectively.

The realization of time-constants in filters, where the aforementioned types of CFOAs are utilized, is achieved by employing passive resistors. This is a drawback with respect to the nowadays analog filter realization trend, where resistorless filter structures with electronic tuning capability are preferred. As a solution, active resistors could be employed, but the performance of the resulted filter configurations in terms of linearity is worsened in this case.

Resistorless topologies using CFOAs could be realized by employing the current controlled CFOA (CCCFOA) in [14]. The core of this active cell is constructed from translinear loops formed by bipolar transistors. In addition, the minimum supply voltage requirement is equal to $2V_{BE} + 2V_{DS,sat}$, where V_{BE} and $V_{DS,sat}$ are the base-emitter voltage of a bipolar transistor and saturation voltage of an MOS transistor, respectively.

In order the CFOA filters to be compatible with the nowadays trend, a novel enhanced version of CFOA, mentioned as Differential Voltage Current Controlled Current Feedback Operational Amplifier (DVCCCFOA), will be employed for the realization of active filters. This cell has also the benefit for operating in a low-voltage power supply environment. As it will be proved through comparison results, the employment of the DVCCCFOA offers a reduced number of active component counts in comparison with the corresponding realizations, where Differential Voltage Current Controlled Current Conveyors (DVCCCIIs) are utilized as active elements.

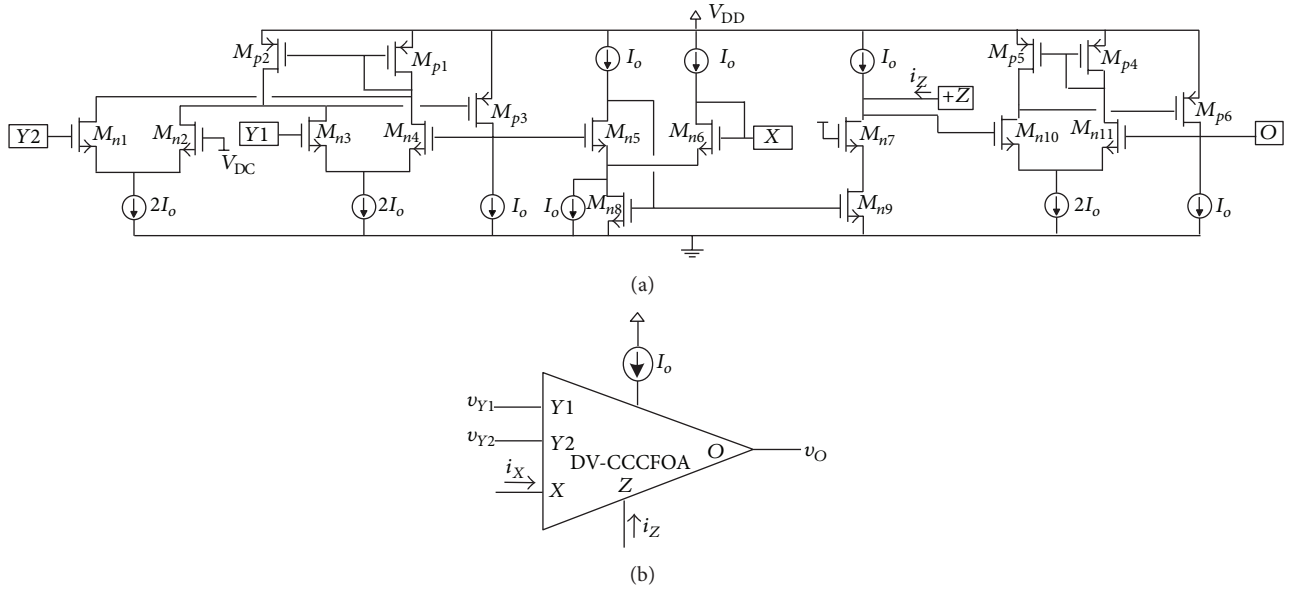

Figure 1: Low-voltage DVCCCFOA (a) topology and (b) its associated symbol.

The paper is organized as follows: the DVCCCFOA configuration is presented in Section 2, while integrator blocks are given in Section 3. As a design example, a 3rd-order leapfrog filter has been realized using the AMS 0.35 μm CMOS process design kit, and the most important performance factors have been evaluated in Section 4. In addition, the same filter topology has been realized using DVCCCIIs as active elements, and its performance has been compared with that of the DVCCCFOA filter. All the above have been achieved using the Analog Design Environment tool of the Cadence software.

2. Low-Voltage DVCCCFOA

A DVCCCFOA topology is depicted in Figure 1(a), while the corresponding notation is given in Figure 1(b). Due to the used single power supply voltage, a dc voltage mentioned as V_{DC} is employed in order to keep all the MOS transistors in saturation. This cell is constructed from the following three stages:

(a) a voltage subtraction input stage formed by transistors M_{n1}–M_{n4}, M_{p1}–M_{p3} and the associated dc current sources, in order to realize the following relationship: $v_X = v_{Y1} - v_{Y2}$,

(b) a current controlled current conveyor [15], which is formed by transistors M_{n5}–M_{n9} and the associated dc current sources. This stage realizes the following relationships between the currents that flow through terminals X and Z, and the voltages at terminals Z, Y_1, and Y_2: $i_Z = i_X$ and $v_X - (v_{Y1} - v_{Y2}) = i_X \cdot R_X$, where $R_X = 1/g_m$ and g_m is the value of the transconductance parameter of transistors M_{n5}-M_{n6}. Owing to the small-signal nature of transconductance, the value of the realized resistor is electronically controlled through a dc current, and this makes possible the realization of resistorless filters with electronic adjustments of their frequency characteristics,

(c) a voltage buffer realized by transistors M_{n10}-M_{n11}, M_{p4}-M_{p5} and the associated dc current sources. Obviously, this topology is a special case of the input stage where just one input is utilized. The established expression is $v_O = v_Z$, implying that the voltage at node Z is conveyed to node O through the buffer.

Concluding, the operation of DVCCCFOA could be desribed in matrix form by (1) as

$$\begin{bmatrix} v_X \\ i_{Y1} \\ i_{Y2} \\ i_Z \\ v_O \end{bmatrix} = \begin{bmatrix} R_X & +1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_X \\ v_{Y1} \\ v_{Y2} \\ v_Z \\ i_O \end{bmatrix}. \quad (1)$$

Another important point is that the DVCCCFOA in Figure 1(a) is capable of operating in a low-voltage power supply environment. This is originated from the fact that the minimum supply voltage requirement is $V_{TH} + 2V_{DS,sat}$, where V_{TH} and $V_{DS,sat}$ are the threshold and saturation voltages of an MOS transistor, respectively. Also, the minimum value of the voltage V_{DC} is equal to $V_{TH} + V_{DS,sat}$.

It should be mentioned at this point that the voltage subtraction stage has been already used for realizing the DVCCII [16, 17]. Thus, the combination of this stage with the CCCII stage described in (b) gives a low-voltage differential voltage current controlled conveyor (DVCCII). Adding a voltage buffer to that two-stage cell, a low-voltage DVCCCFOA is resulted. Therefore, a contribution of this work is that, for the first time in the literature, the DVCCCFOA is utilized for realizing low-voltage resistorless active filters.

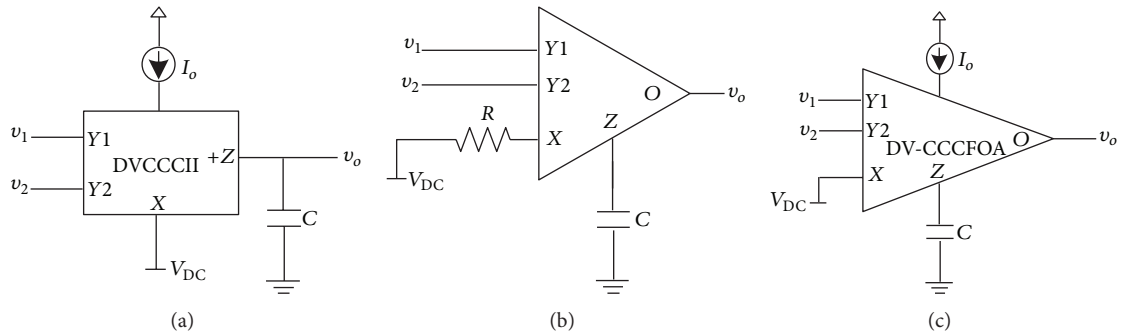

Figure 2: Differential input lossless integrator using (a) DVCCCII, (b) DVCFOA, and (c) DVCCCFOA.

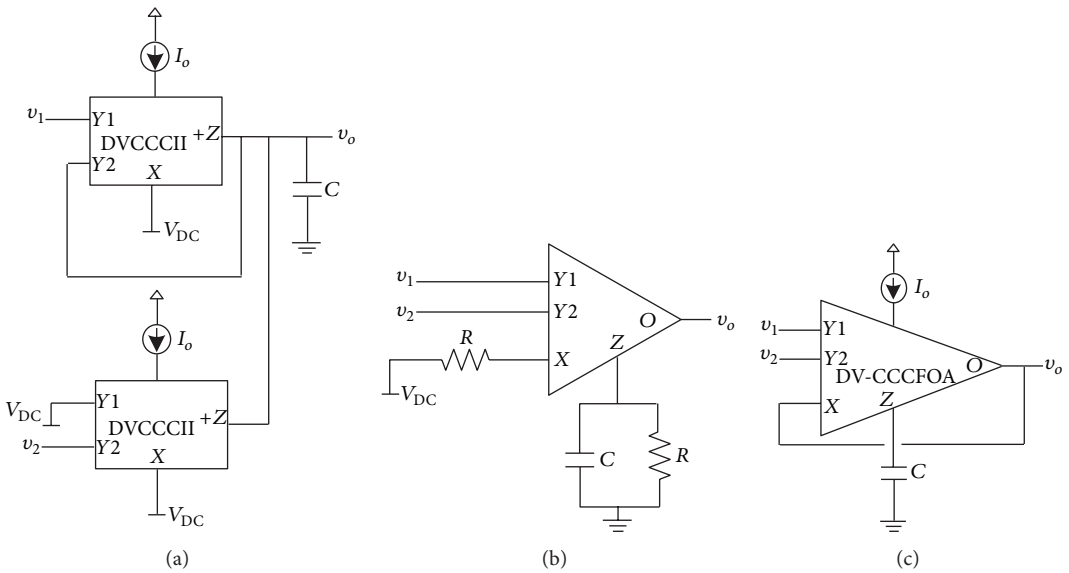

Figure 3: Differential input lossy integrator using (a) DVCCCII, (b) DVCFOA, and (c) DVCCCFOA.

3. Integration Blocks with the DVCCCFOA

Let us consider the input-output relationship for a differential input lossless integrator, given by (2) as

$$v_o = \frac{1}{\tau s}\left(v_1 - v_2\right), \tag{2}$$

where τ is the corresponding time-constant.

Using a DVCCCII as active element, the derived configuration is depicted in Figure 2(a), where the realized time constant is given by the formula: $\tau = C/g_m$, where g_m is the transconductance parameter of the corresponding MOS transistor. Taking into account that $g_m = [2K(W/L)I_o]^{1/2}$, where K is the intrinsic transconductance factor of the MOS transistor, W/L is its aspect ratio, and I_o is a dc current, it is obvious that the realized time constant has electronic tuning capability through the dc current I_o. A drawback of the topology in Figure 2(a) is that it is sensitive to the loading effect; in other words, a cascade connection is possible only with high-input impedance stages.

The integrated topology in Figure 2(b) does not suffer from this drawback due to the voltage buffering operation performed by the DVCFOA cell. On the other hand, the realized time-constant has now the form of $\tau = RC$, and, consequently, the benefit of resistorless realization is lost.

The lossless integrator configuration using DVCCCFOA, depicted in Figure 2(c), simultaneously offers a resistorless realization with a time-constant given by the same expression as that for the topology in Figure 2(a) and direct cascade connection capability. This has been achieved without losing the benefit of employing a grounded capacitor, which is also the case for the topologies in Figures 2(a) and 2(b).

The expression of a differential input lossy integrator is given by (3) as

$$v_o = \frac{1}{\tau s + 1}\left(v_1 - v_2\right). \tag{3}$$

The corresponding realizations using DVCCCII, DVCFOA, and DVCCFOA as active elements are demonstrated in Figures 3(a)–3(c), respectively. Inspecting the resistorless realizations in Figures 3(a) and 3(c), it is evident that the employment of DVCCCFOAs as active elements offers a reduction of the active component count. Also, it should be mentioned at this point that the integrator in

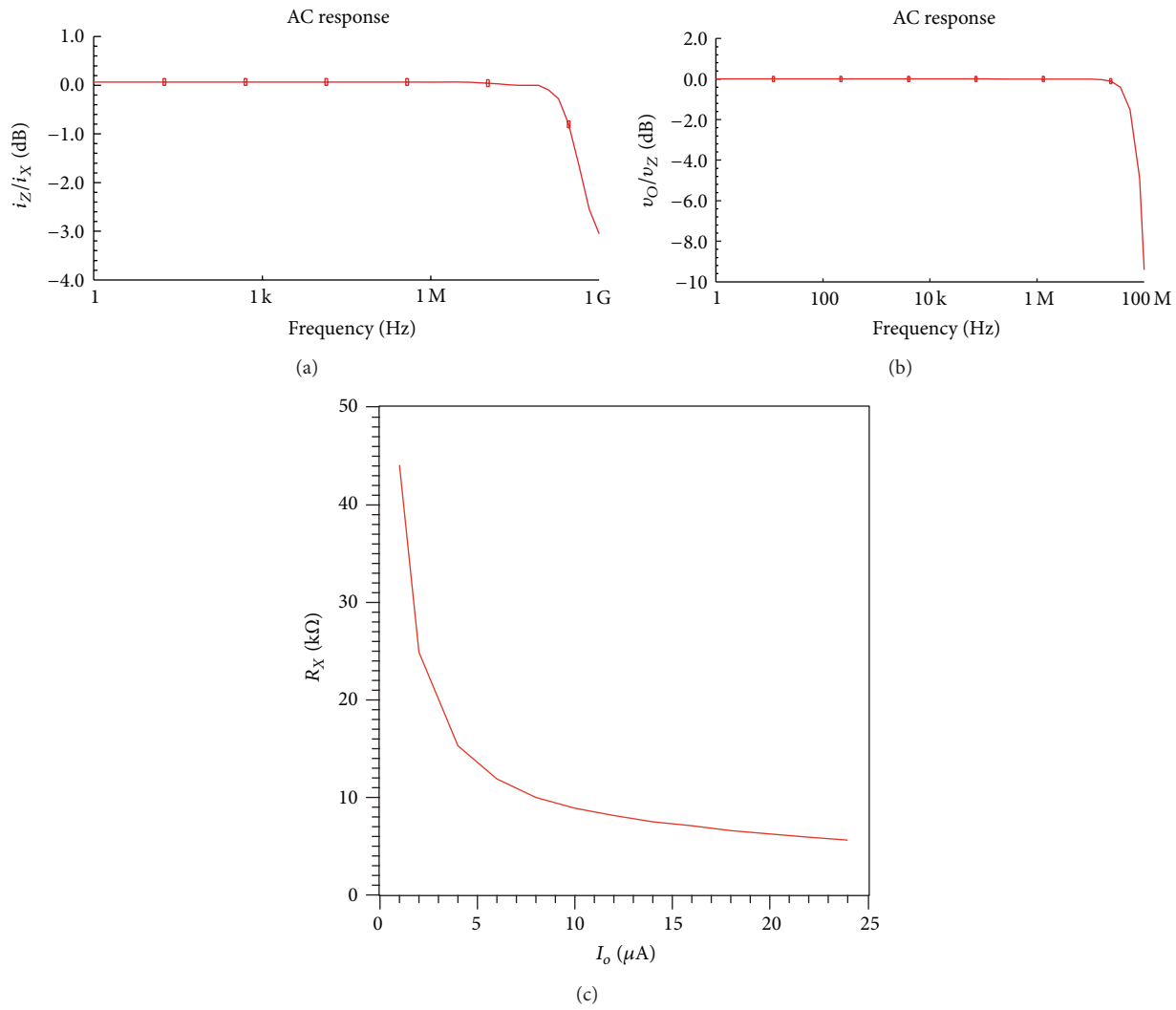

Figure 4: Evaluation of the performance of the DVCCCFOA in terms of (a) current conveying, (b) voltage conveying, and (c) intrinsic resistance.

Figure 3(c) preserves the cascade connection capability without the requirement of extra circuitry. Comparing the topologies in Figures 3(b) and 3(c), it is obvious that the employment of the DVCCCFOA leads to an absence of resistors without increasing the active component count.

4. Simulation and Comparison Results

The performance of the DVCCCFOA in Figure 1(a) has been evaluated through simulation results by employing the Analog Design Environment tool of the Cadence software. For this purpose, the MOS transistors models provided by the AMS 0.35 μm C35B4 CMOS process design kit have been utilized in simulations. The used bias scheme was V_{DD} = 1.5 V, V_{DC} = 1.15 V, and I_o = 12 μA. The aspect ratio of pMOS transistors M_{p1}–M_{p6} was 50 μm/2 μm, and the same ratio has been used for the pMOS transistors that realize the corresponding dc currents. The nMOS transistors M_{n1}–M_{n11} have an aspect ratio of 2.5 μm/0.4 μm, while for nMOS transistors used for the realization of the corresponding dc currents have 2.5 μm/1 μm.

The simulated frequency response of the current conveying between terminals X and Z is depicted in Figure 4(a), while the corresponding plot for the voltage conveying between nodes Z and O is given in Figure 4(b). The cutoff frequencies of these responses are 1 GHz and 66 MHz, respectively. The realized values of the intrinsic resistance R_X, as a function of the dc bias current, are given in the plot of Figure 4(c).

As a design example, a 3rd-order lowpass filter will be realized using the leapfrog method. The corresponding Signal Flow Graph (SFG) is depicted in Figure 5, while the obtained filter topology is presented in Figure 6. The obtained value of transconductance of transistors M_{n5}-M_{n6} was about 116.3 μS. In order to realize a Butterworth lowpass filter transfer function with a cutoff frequency f_o = 5 MHz, the calculated values of capacitors were C_{1a} = C_{3a} = 3.7 pF and C_{2a} = 7.4 pF.

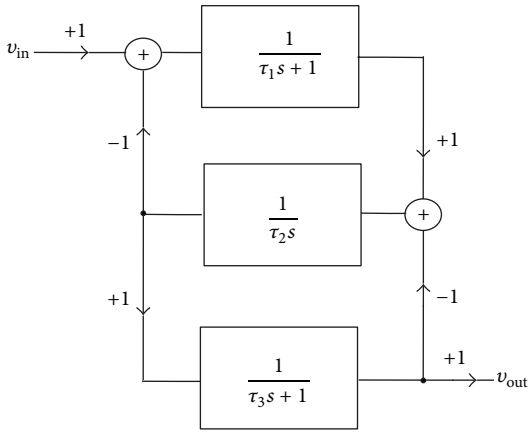

Figure 5: SFG of a 3rd-order lowpass leapfrog filter.

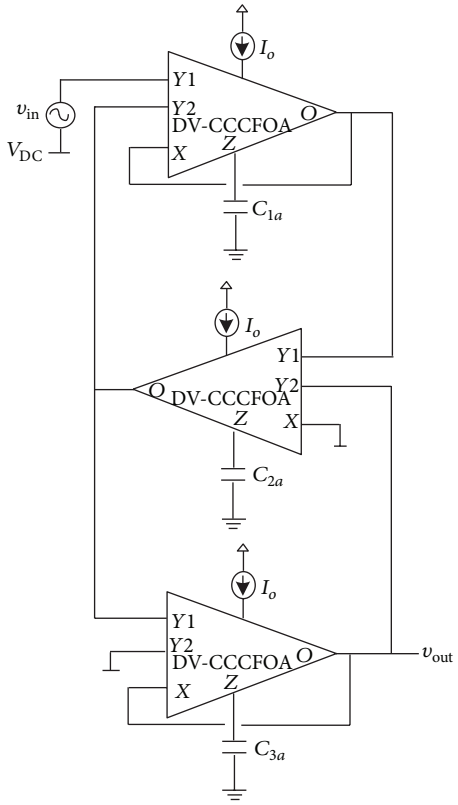

Figure 6: Realization of the SFG in Figure 5 using DVCCCFOAs.

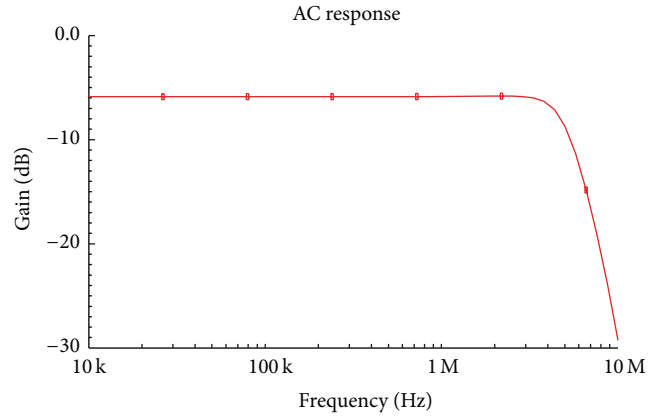

Figure 7: Frequency response of the filter in Figure 6.

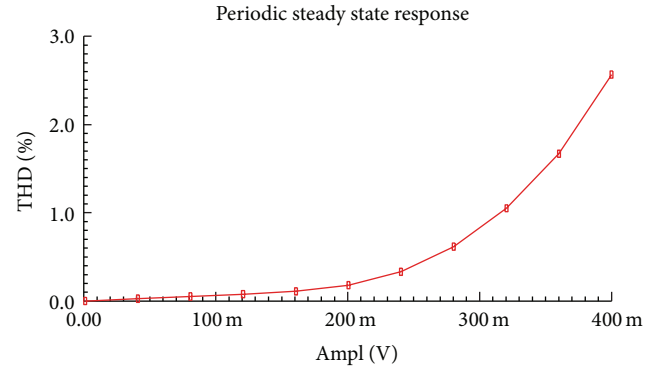

Figure 8: Linear performance of the filter in Figure 6.

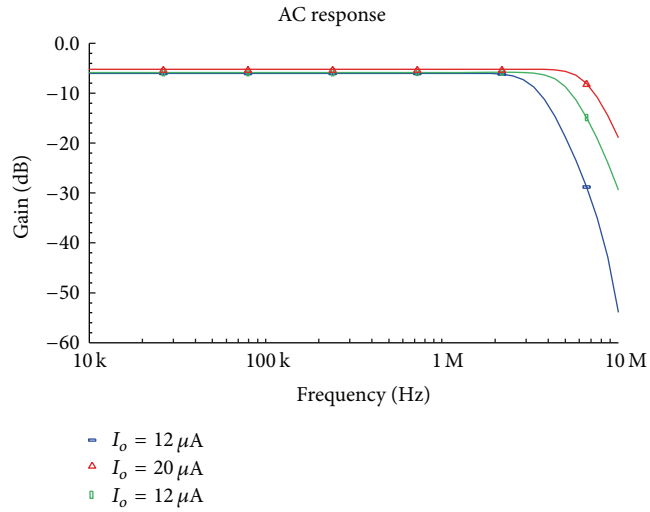

Figure 9: Demonstration of the electronic tuning capability of the filter in Figure 6.

The dc power dissipation of the filter was 720 μW. The simulated frequency response is given in Figure 7, where the cutoff frequency was 5.06 MHz. The linear performance of the filter has been evaluated by applying a 10 kHz input signal and variable amplitude. The Total Harmonic Distortion (THD) plot as a function of the amplitude of the input signal is given in Figure 8, where a THD equal to 1% has been measured for input signal amplitude equal to 320 mV.

Performing an integration of the noise within the pass-band of the filter, the obtained rms value of the input referred noise was 300 μV. Thus, the predicted value of the Dynamic Range (DR) of the filter will be 57.5 dB.

The tuning capability of the filter in Figure 6 has been demonstrated in Figure 9, where the frequency responses at I_o = 6 μA, 12 μA, and 20 μA are simultaneously given. The obtained cutoff frequencies were 3.4 MHz, 5.06 MHz,

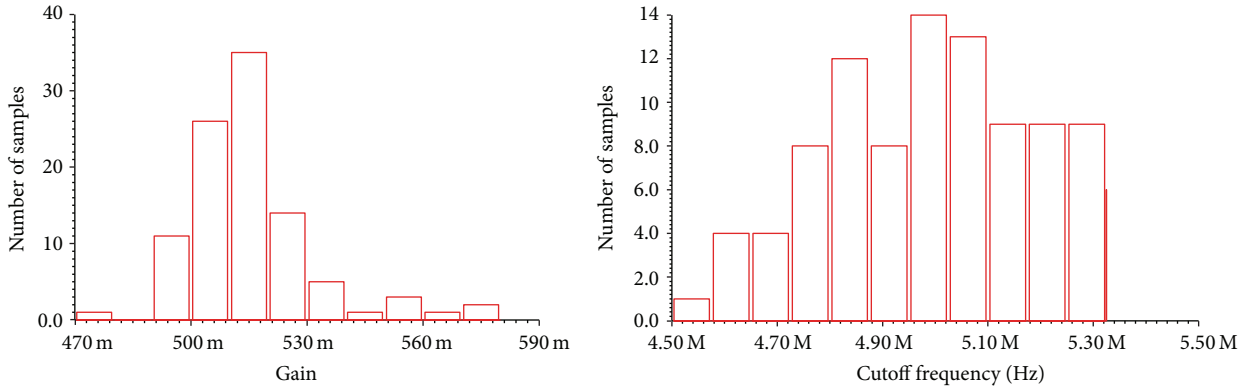

Figure 10: Sensitivity performance of the filter in Figure 6 with regards to the (a) low-frequency gain and (b) cutoff frequency.

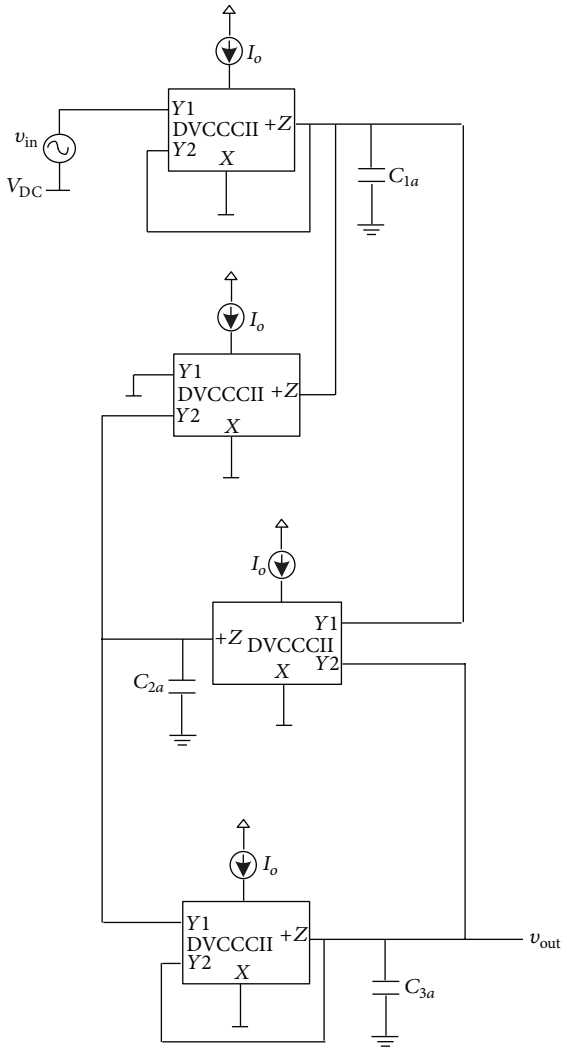

Figure 11: Realization of the SFG in Figure 5 using DVCCCIIs.

and 6.7 MHz, respectively, and they are close to the theoretically expected values 3.6 MHz, 5 MHz, and 6.5 MHz.

The sensitivity performance of the filter in Figure 6 has been evaluated through the utilization of the Monte-Carlo analysis offered by the Analog Design Environment of the Cadence software. The derived statistical histograms about the gain and the cutoff frequency of the filter are given in Figure 10, where the values of the standard deviation of the gain and cutoff frequency were 3.2% and 210 KHz, respectively. Thus, the filter in Figure 6 has reasonable sensitivity characteristics.

Table 1: Performance comparison results for the filters in Figures 6 and 11.

Performance factor	Figure 11	Figure 6
V_{DD}, V_{DC}, and I_o	1.5 V, 1.15 V, and 12 μA	1.5 V, 1.15 V, and 12 μA
Power dissipation	730 μW	720 μW
Number of active elements	4	3
Input amplitude at THD 1%	72 mV	320 mV
Noise	322 μV	300 μV
Dynamic range	44 dB	57.5 dB
Standard deviation of gain	3%	3.2%
Standard deviation of f_o	245 kHz	210 kHz

The performance of the filter realized using DVCCCFOAs as active elements will be compared with that offered by the corresponding filter where DVCCCIIs are used as active elements. The derived filter topology is depicted in Figure 11, where the DVCCCIIs are realized by omitting the buffer stage at the output of the cell in Figure 1(a). In order to achieve fair comparison results, the same bias scheme as in the case of the filter in Figure 6 has been employed. The obtained performance factors of the filter in Figure 11 are given in Table 1, where the corresponding factors of the filter in Figure 6 are also summarized. According to these results, the filter realized using DVCCCFOAs offers significant improvement in terms of linearity and Dynamic Range, while the other performance parameters have been also improved.

5. Conclusions

The introduced DVCCCFOA meets the nowadays trends for designing filters suitable for low-voltage operations and

electronic tuning capabilities of their frequency characteristics. The provided design example confirmed its benefits in terms of versatility and design flexibility. In addition, the comparison results confirmed the benefits of reduced active component count and improved linear performance. Thus, the DVCCCFOA could be considered as an attractive candidate for realizing high performance analog processing systems.

Conflict of Interests

The authors of the paper declare that they do not have any conflict of interests with the commercial identities mentioned in the paper.

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