Research Article

Simple Synthesis and Growth Mechanism of Core/Shell CdSe/SiOx Nanowires

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Core-shell-structured CdSe/SiOx nanowires were synthesized on an equilateral triangle Si (111) substrate through a simple one-step thermal evaporation process. SEM, TEM, and XRD investigations confirmed the core-shell structure; that is, the core zone is single crystalline CdSe and the shell zone is SiOx amorphous layer and CdSe core was grown along (001) direction. Two-stage growth process was present to explain the growth mechanism of the core/shell nanwires. The silicon substrate of designed equilateral triangle providing the silicon source is the key factor to form the core-shell nanowires, which is significant for fabrication of nanowire-core sheathed with a silica system. The PL of the product studied at room temperature showed two emission bands around 715 and 560 nm, which originate from the band-band transition of CdSe cores and the amorphous SiOx shells, respectively.

1. Introduction

In recent years, great efforts have been made to overcome the numerous challenges associated with the design of one-dimensional (1D) nanostructures with well-controlled size, phase purity, crystallinity, and chemical composition, due to their fascinating properties and unique applications [1–3]. With the ongoing development of nanodevices, the preparation of nanocables, such as semiconducting nanowires sheathed with an insulating shell which can passivate existing surface states, enables new interface properties and introduces unique electronic and photonic function that has attracted particular attention [2–7]. Amorphous silicon oxide is optically transparent for the visible absorption/emission of semiconductor nanowires and produces little destruction of their intrinsic optical properties; therefore it is widely used as passivation or insulation layers materials. So far, several kinds of 1D nanocables based on semiconductors sheathed with a silica system have been achieved by employing a thermal evaporation method, such as CdS/Si coaxial nanowires [8], SiO_2-sheathed ZnO nanowires [9], and ZnS/SiO_2 core-shell nanowires [10, 11]. In this context, the Si source of the passivation layers was provided by coevaporation of Si-based source and the core-semiconducting powder in high temperature (>1000°C) or by the pretreatment of Si wafer in HF solution, in which the high temperature and venenous solution should avoid in the developed growth technologies. Development of simple, low-cost, and environment-friendly growth processes is necessary.

CdSe, with a direct band gap of 1.7 eV at room temperature, is one of the most important materials in making optoelectronic devices [12–14]. As a selenide, unprotect nanostructured CdSe easily suffers surface degradation (such as oxidation) and contamination in atmosphere which severely damage there intrinsic properties. As a heavy metal Cadmium-compound, the decreasing toxicity of the nanostructures is highly desired especial for biorelated applications. Therefore, surface modification on CdSe nanostructures with coating a shell layer is very crucial and urgent
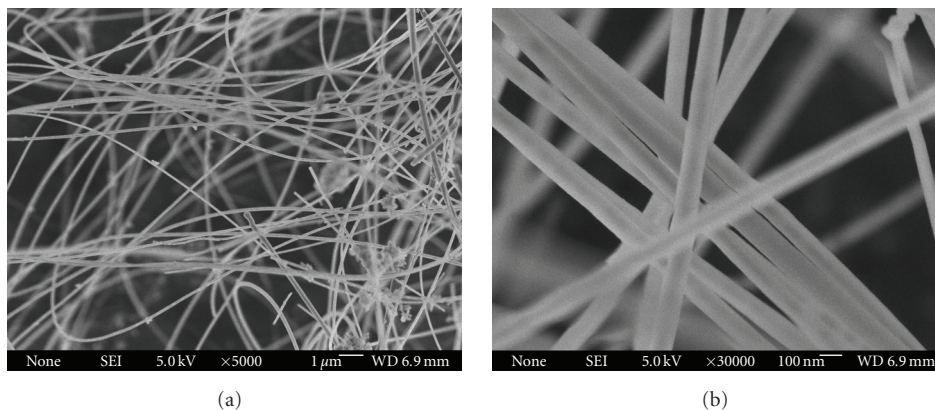
(a)

(b)

FIGURE 1: Typical scanning electron microscopy (SEM) images of the products: (a) at low magnification; (b) at high magnification.

for their commercial or industrial utilization. In the last few years, the majority of reports on the synthesis of CdSe-core/shell nanostructures were focused on nanoparticles [15, 16], and very few work has been done in the coaxial nanowires except for one paper report on the synthesis of CdSe/SiO$_2$ nanocables [17], in which the reaction source was added in the Si powder and was sublimated in the temperature above 1200°C. In this article, we report the synthesis of coaxial CdSe/SiO$_x$ nanowires on an equilateral triangle Si substrate through a simple one-step thermal evaporation process at 900°C. The effects of the equilateral triangle Si substrate and local temperatures on the coaxial nanowires growth are significant, which is in contrast to early publications. Photoluminescence properties of these coaxial nanowires were also briefly investigated at room temperature.

2. Experimental

Core-shell nanostructures were synthesized by thermal evaporation. The substrates used for the growth of CdSe nanowires with a coaxial silicon shell were p-type (111) Si wafers. Before used, the Si wafers were cut into an equilateral triangle (the vertex angle is about 60 degrees) and then cleaned ultrasonically for 30 minutes in acetone solution. An Au film about 20 nm in thickness was deposited onto the ultrasonically-cleaned Si wafers by sputtering. About 0.1 g commercial-grade CdSe powder (Strem Chemicals, 99.999+%-Cd purity) was placed in the center of a single zone tube furnace and evacuated for several hours to purge oxygen in the chamber. The treated Si substrates were placed 5 cm away from the CdSe powders and along the downstream side of the flowing Ar (90%) and H$_2$ (10%). Typically, the CdSe source temperature was controlled at about 900°C at a rate of 100°C /min. During the growth process, the mixture carrier-gas flow was kept at a constant rate of 10~20 sccm. After 60 minutes of typical deposition time the samples were cooled down to room temperature. Dark-brown products appeared on the Si wafers.
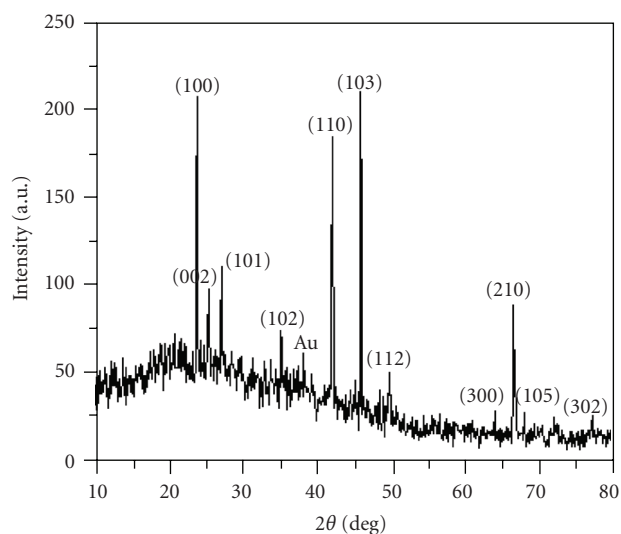

FIGURE 2: The XRD pattern of the products collected from the silicon substrate.

X-ray powder diffraction (XRD) data were obtained on a Siemens D-5000 type diffractometer equipped with graphite-monochromatized CuKa1 radiation (l = 1.54056 Å). The morphologies and chemical composition of the products were examined by a field emission scanning electron microscope (FE-SEM, JSM-6700F) and transmission electron microscopy (TEM, JEM-3010) with an energy-dispersive X-ray (EDX) spectroscope attached to the JEM. Room-temperature photoluminescence (PL) was taken on a Confocal Optical Microscope (Witec) using an Ar-ion laser (488 nm) as an excitation light source.

3. Results and Discussion

The as-deposited products were first examined by SEM observation. Figure 1(a) showed the typical low-SEM images taken from the as-prepared products on Si substrates. The image shows that samples were formed in long and wirelike
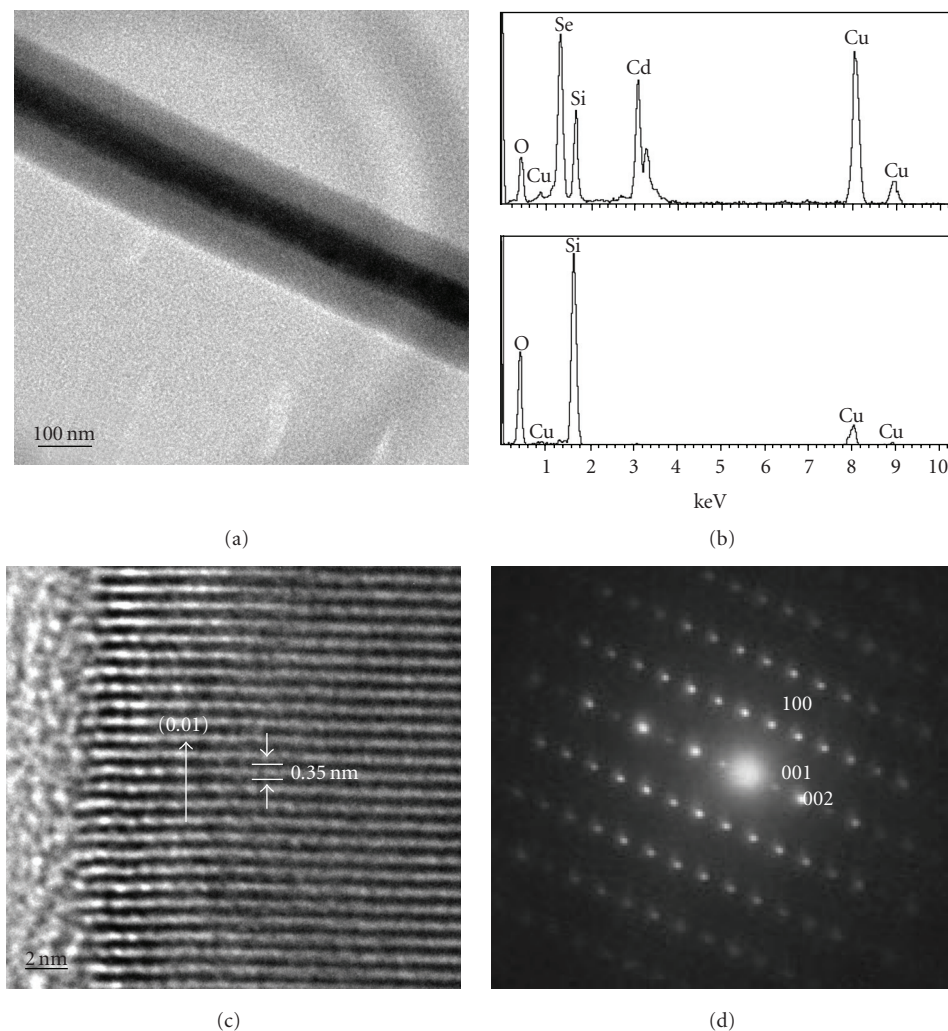
(a)

(b)

(c)

(d)

FIGURE 3: (a) Typical TEM images of nanowires, showing a core/shell structure. (b) The EDX patterns on the core and the shell areas of the nanowire signed by white box, respectively. (c) High-resolution TEM image of the interface between the crystalline core and amorphous sheath. (d) The SAED pattern of the core areas indicates a hexagonal wurtzite structure single crystalline layer and an amorphous layer.

nanostructures. The high-magnification SEM image was been given in Figure 1(b) which indicated that the diameter of the nanowire is about 100 nm. Furthermore, nanosized particles (marked with an arrow in Figure 1(b)) were found attached to the ends of the nanowires, indicating a likely vapor-liquid-solid (VLS) process for the formation of core nanowires [18]. XRD measurements were made on the nanowires to assess the structure and phase purity. A typical XRD pattern of the nanowires was shown in Figure 2. The main diffraction peaks match well with a wurtzite (hexagonal) structure of bulk CdSe with lattice constants of a = 4.299 Å and c = 7.010 Å (PDF No. 77–2307). A weak Au diffraction peak from catalytic Au nanoparticles was detected. Besides, a broad peak located at ∼22 degree, which indicates that there are some amorphous materials in the product.

Morphology and microstructural analyses were further performed using TEM. Figure 3(a) shows a typical TEM image of the nanowires. From this image we can identify clearly that the nanowires have a core-shell nanostructure; that is, a relatively thick sheath with light contrast is formed outside the surface of nanowires with dark contrast. Furthermore, the diameter of the core and the thickness of the shell of individual nanowire are uniform and the typical dimensions are all in the range of 30 to 40 nm. To further investigate the composition of the sample, EDX was taken of the core and shell areas of the nanowire and is presented in Figure 3(b). It can be found that the core of the nanowire is mainly composed of Se and Cd and the shell is mainly made up of Si and O. The extra Cu shown in the EDX spectrum stems from the Cu grid. HRTEM image was taken with the electron beam along a single nanowire, as is shown in Figure 3(c), which reveals the clear crystalline-core/amorphous-shell interface. Moreover, the measured lattice spacing of crystalline core is 0.35 nm, corresponding to the (001) lattice planes of hexagonal wurtzite CdSe. Figure 3(d) shows a selected-area electron diffraction (SAED) pattern taken from the core zone of
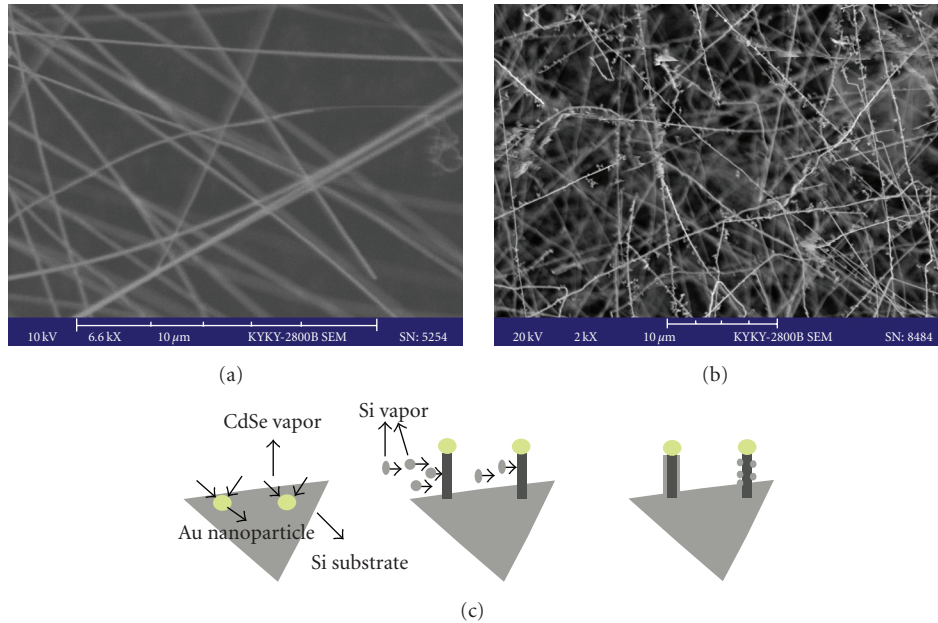
(a)

(b)

(c)

FIGURE 4: SEM image of the sample with different temperature region: (a) 750–800°C; (b) 700–750°C; (c) schematic illustration of the growth process of the core-shell CdSe/SiO$_x$ nanowires.

the nanowire, which could be indexed for the (001) zone axis of single crystalline CdSe. Since only one set of diffraction spots from wurtzite structure of CdSe was found, it can be inferred that the core zone is single crystalline CdSe and the shell zone must be amorphous layer. These results indicate that the nanowire composed of a crystalline CdSe core and an amorphous SiO$_x$ shell.

To investigate the growth mechanism of the core-shell CdSe/SiO$_x$ nanowires, we examined products on the different collection positions, that is, at distinctive deposition temperature. Figures 4(a) and 4(b) show the SEM image of the sample with a distinctive collection temperature region range of 750–800°C and 650–700°C, respectively. It can be seen from Figure 4(a) that the nanowires have the uniform diameter and smooth surface. These suggest that the core/shell nanowires form completely. However, at a comparatively low-temperature region, the nanowires, as given in Figure 4(b), with the coarse sheath would be obtained. Some snowflake-like aerosol adsorbed on the surface of the core wire. We suppose that the growth process of the core/shell nanwires is mainly divided into two stages. The first stage is an ordinary vapor-liquid-solid (VLS) growth process. The conclusion can be supported by nanosized particles marked with an arrow in Figure 1(b). During this process step, the density of CdSe vapor is far denser than the Si vapor which came from the special triangle Si substrate used in this experiment. The main two reasons are as follows. (1) The CdSe source is relatively sufficient in the initial stage and enough CdSe powder can sublime at a suitable temperature zone (∼900°C). (2) Addition of H$_2$ could accelerate the evaporation of CdSe powders as indicated in the following reaction equation: CdSe(s) ↔ CdSe(g) CdSe(s) + H$_2$(g) ↔ Cd(g) + H$_2$Se(g).

Thus, we can assume that the first step is a fast growth CdSe as guided by a gold catalyst based on the VLS growth process.

With the reaction continue and the CdSe powders exhausting, the Si vapor density starts to increase and is carried by the mixture carrier gas to a lower temperature zone, where it condenses. In the second stage, the CdSe nanowires serves as the preferable adsorption site for the Si in the vapor phase and eventually works as the template for the one-dimensional growth of Si. Meanwhile, the surface of the silicon was oxidized to form SiO$_x$ (the trace remnant of oxygen that was not eliminated completely by flushing with mixed gas and/or from the leakage of the furnace serves as the oxidant) during heating, resulting in the CdSe-core/SiO$_x$-sheath nanocable structure. Therefore, this process is mainly grows the SiO$_x$ shell on the CdSe-core nanowires via the vapor-solid (VS) mechanism. The growth of nanostructures always abides to the thermodynamic/kinetic issues [19]. In the high-temperature region, the dynamics effect is remarkable and the Si vapor is sufficient. The CdSe-core/SiO$_x$-sheath structure of the uniform diameter and smooth surface can be obtained (Figure 4(a)). However, in the comparatively low-temperature position where is far away from the CdSe powder, the situations are different. The intensity of Si steam is comparatively low and Si aerosol adsorbed on CdSe nanowire templat slowly and unorderly, liking semiwraps nanowires. (Figure 4(b)). Then, we can regard it as the intermediate state of the final core/sheath nanowires shown in Figure 4(a). The stage of the growth process can be seen in Figure 4(c).

We need to point out that the silicon source is provided by the silicon substrate. This was in contrast to early publication which added the silicon-based materials in the mixture source powder [17]. The supported experimental
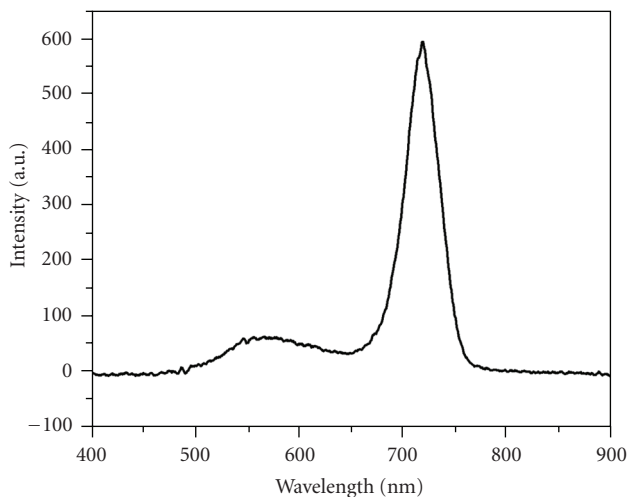
Figure 5: Room temperature PL spectrum of the core/shell-CdSe/SiO$_x$ nanowire. λ_{exc} was 488 nm.

facts are as follows: (1) no extra silicon source is provided; (2) the core/shell nanostructures are only found on the silicon substrate close to the precursor powder source, indicating that the Si substrate is the Si source. Moreover, the Si wafer used in the experiment was cut into equilateral triangle and has not corroded processing. In the deposition sample, the vertex angle of the Si wafer was facing to the CdSe powder source. We think that the triangle Si substrate is the only substance to produce the Si source, since only the CdSe nanostructures can be found under similar conditions except the shape of the Si substrate changing to the ordinary rectangle. On the one hand, the forefront silicon substrate of the triangle Si wafer reacts more intense at the same temperature when the shape of the Si substrate changes from the broad rectangle to narrow triangle. On the other hand, the substrates used for the growth were p-type (111) Si wafers and the active (111) planes were naked and reacted completely with the source vapor when it was designed in equilateral triangle. Therefore, the triangle Si substrate is easy to sublimate and provided the Si source even in the moderate reaction condition. The ways which provide the Si source by changing the shape of Si substrate may be useful for future design of other Si compound nanostructures.

One typical room-temperature photoluminescence (PL) spectrum of the CdSe/SiO$_x$ coaxial nanowires is shown in Figure 5, which reveals an intensive peak centered at 715 nm and a weak peak located at about 560 nm. The longer wavelength peak is explained as the band-to-band emission of CdSe-core nanowires with a bandgap of about 1.74 eV. There is a blue-shift of about 15 nm (0.04 eV) with respect to the emission of bulk CdSe (730 nm; 1.7 eV), which may be related to quantum-confinement effects [20]. The lower PL intensity peak may be attributed to the amorphous SiO$_x$ shell. Literatures [21] have reported the oxidized SiO$_2$ nanotubes emission peak at about 570 nm. The PL band around 550 nm also was indexed to the SiO$_x$ shell of Si/SiO$_x$ nanowires [22]. Here, we think that the visible emission at

560 nm also come from the amorphous silica shell, in which the dissimilar peak position may be linked to the different density of oxygen vacancies.

4. Conclusion

In summary, we synthesized coaxial CdSe/SiO$_x$ nanowires through simple one-step thermal evaporation process on an equilateral triangle Si substrate. The structures and growth mechanism have been presented. We found that the temperature and the Si substrates of designed equilateral triangle have the critical effect on the formation core/shell nanowires. The PL studies present two emission bands about 560 nm and 715 nm, which originate from the intrinsic transition of CdSe cores and the amorphous SiO$_x$ shells, respectively. We believe that this simple preparation technique can be useful for synthesis of other core-semiconductor/shell-Si nanostructures.
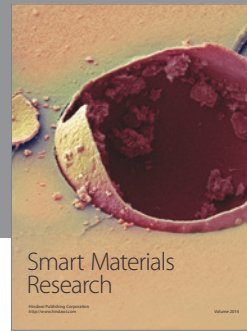
Acknowledgments

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