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Investigation of CNTFET Performance with Gate Control Coefficient Effect

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For the first time, a deep study of gate control coefficient (a_G) effect on CNTFET performance has done in this research. A new, analytical CNTFET simulation along with multiple parameter approach has executed with 3D output in MATLAB and that used it to examine device performance. It is found that, drain current and transconductance increases with high gate control coefficient. On the other hand, total capacitance decreases with high a_G value resulting improved charging energy. Likewise, drain induced barrier lowering (DIBL) decreases with a_G that provides less deviation from ideal device performance. Finally, subthreshold swing comes very close to the theoretical limit at high a_G which is desired for low threshold voltage and low-power operation for FETs scaled down to small sizes.

Keywords: Gate Control Coefficient, CNTFET, Drain current, Transconductance.

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1. INTRODUCTION

Since the invention in 1991 by S. Iijima [1], CNTs have drawn great attention of researchers in terms of FET application because of their extraordinary physical and electrical properties [2] [3]. Several researches have already conducted to analysis CNTFET performance [4-14]. Recently, CNTEFT performance dependency on dielectric constant, gate oxide thickness and temperature has investigated by Khan et al. [4, 5, and 6] with 3D simulation. It is seen that [4], I_{ON}/I_{OFF} ratio, transconductance and average carrier velocity increases with high K (dielectric constant) which leads to high on-state current. On the other hand, subthreshold swing increases with K. According to the previous research [5] [9] [15] and [16], there is a linear decreasing of output current with respect to oxide thickness. In conventional MOSFET, the gate oxide thickness has already entered into the nanometer range; channel scattering from the rough oxide interface and tunneling through the thin oxide are becoming prevalent problems [15]. Carbon nanotube transistors do not have these difficulties; all chemical bonds are satisfied in a carbon nanotube and thus, there is less oxide to channel interface problem. A multitude of oxide can be placed on the nanotube and thus, many high-k dielectrics can be incorporated into CNTFET to reduce the tunneling current. Therefore, it can be concluded that the I_{ON}/I_{OFF} ratio will increase as the gate oxide thickness is reduced [5, 15].

According to Ali Naderi et al. [10], by increasing the gate source voltage, at low drain source voltages, for higher temperature (550 K) the drain current is less than lower temperature (250 K). Therefore, in spite of the on-current increase, the device reliability declines due to large rise in leakage current [6, 9].

The resolution of this paper is to study the Gate Control Coefficient (a_G) effect on CNTFET performance and the core emphasis on the simulation of its current-voltage (I-V) characteristic, total capacitance, transconductance, drain conductance, subthreshold swing and drain induced barrier lowering (DIBL) effect with 3D simulation method.

2. CNTFET STRUCTURE AND SIMULATION METHOD

Considered structure for this simulation is MOSFET like CNTFET. Alike conventional MOSFET, drain and source terminal is heavily doped in this structure. This device is formed in order to overcome problems in SB-CNFET by operating like normal MOSFET. This device operates on the principle of modulation the barrier height by gate voltage application. The drain current is controlled by number of charge that is induced in the channel by gate terminal [17].

This device is able to suppress ambipolar conduction and also provides longer channel length limit because the density of metal-induced-gap-states is significantly reduced. Faster operation can be achieved since length between gate and source / drain terminals can be separated by the length of source to drain, which reduces parasitic capacitance and transistor delay metric. Previous research [16] on CNTFET has shown that this type of device gives higher on-current compared to SB-CNFET as it operates like SB-CNTFET with negative Schottky barrier height during on-state condition and therefore it can justify the upper limit of CNTFET performance. Based on the device performance, it is obvious that this device can be used to investigate the ballistic transport in CNTFET [18, 19].

A 3D simulation tool [20] was constructed based on ballistic Nanotransistors theory [17] and FETTOY simulation [21]. Figure 1, describes the total simulation procedure that has done by using MATLAB. Detail simulation procedure has discussed in our previous research [20].

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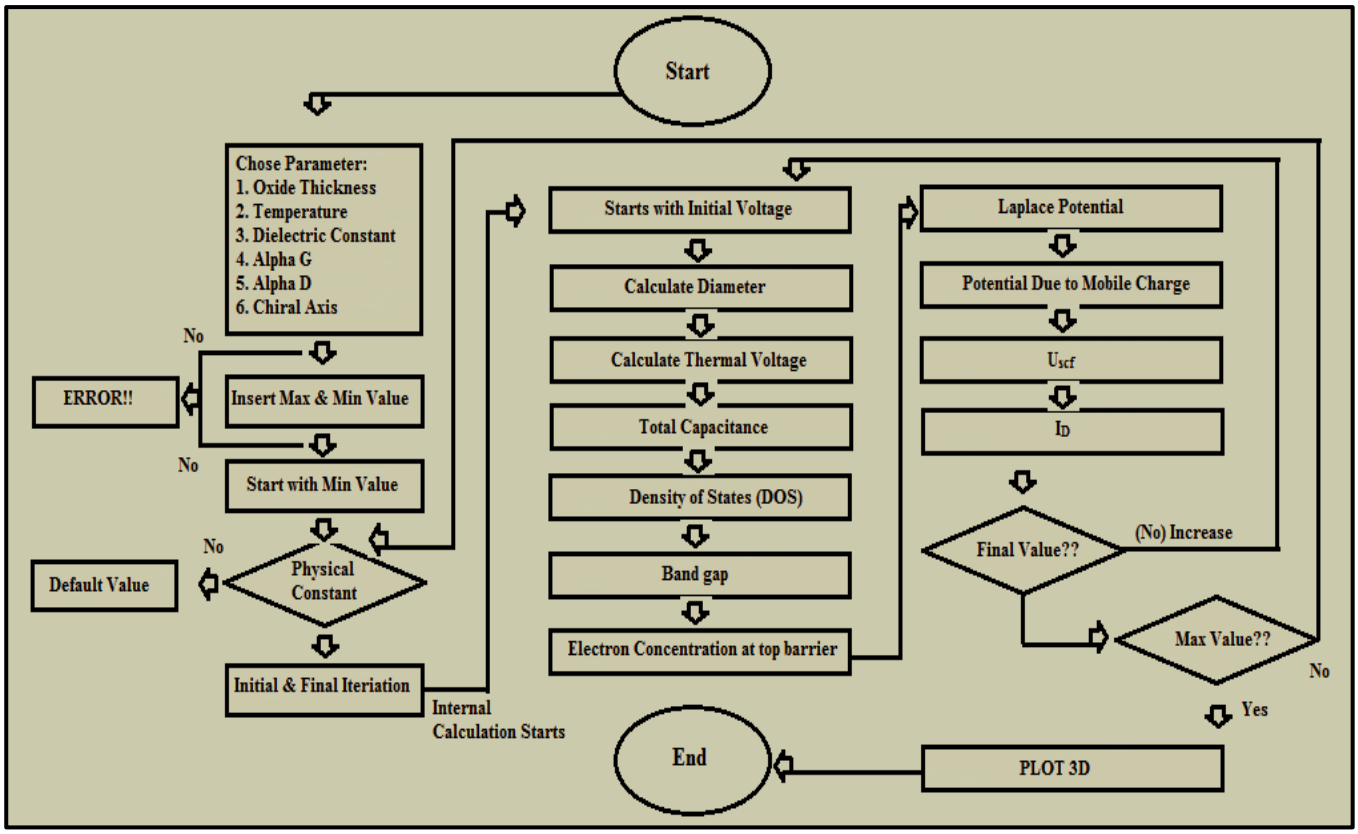

Fig. 1 – Flowchart used for 3D MATLAB simulation

3. RESULTS AND DISCUSSION

The research considered a (13, 0) CNT which results in a band gap of ~ 0.83 eV and a diameter of ~ 1.0184 nm. A coaxial gate was placed around the intrinsic part of the nanotube and separated by an oxide with thickness of 1.5 nm. At this inspect, the temperature was kept at 300 K and obtained drain control coefficient $\alpha_D = 0.035$. In addition, source Fermi level was – 0.32, dielectric constant was 3.9.

Figure 2 represents the I-V characteristics of CNT-FET with respect to gate control coefficient. Sanudin et al. [22] showed that the drain current remains zero until α_G reached to the 0.25, later it increased gradually till 0.85. To analyze the performance after 0.85, α_G was varied from 0.88 to 1.5 maintaining interval of 0.02. According to the Figure 2, drain current still maintain the increasing trends while reaching to 1.5. Hence, this result confirms the previous claim [22] that, there is a proportional relationship between drain current and gate control coefficient.

Analysis on gate control coefficient and total capacitance is given in Figure 3. Since, the capacitance and the gate control coefficient are incorporated with inverse relationship, the total capacitance decrease with the α_G. Mathematical relationship is shown in equations (1) and (2) where Cins is capacitance over the contact area. It is observed from Figure 4 that, at high α_G, total capacitance become very low resulting high charging energy. Hence, high α_G can be a positive phenomenon for overall CNTFET performance.

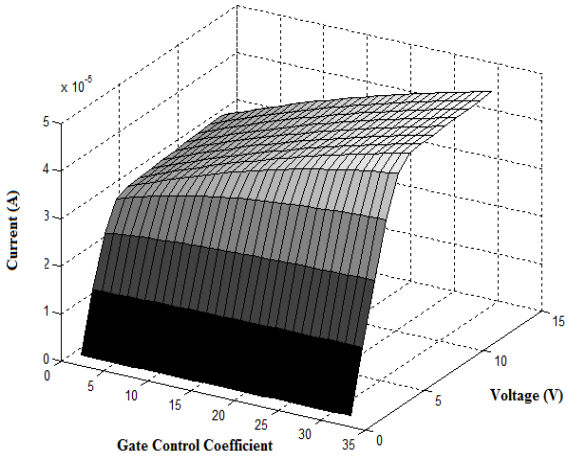

Fig. 2 – Current-Voltage output with respect to Gate Control Coefficient

$$\text{Csum} = \frac{\text{Cins}}{\alpha_g} \quad (1)$$

$$\text{Charging Energy} = \frac{q^2}{\text{Csum}} \quad (2)$$

Finally, Potential due to mobile charge

$$(U_p) = q^2 / C_\Sigma (N_1 + N_2) - N_0 \quad (3)$$

Relation between transconductance and gate control coefficient is shown in Figure 5 which is extracted from the slope of I_D-V_{GS}. As shown in the figure, with α_G, transconductance of CNTFET increases gradually. Hence, with increasing α_G, the I_{ON} / I_{OFF} ratio increases

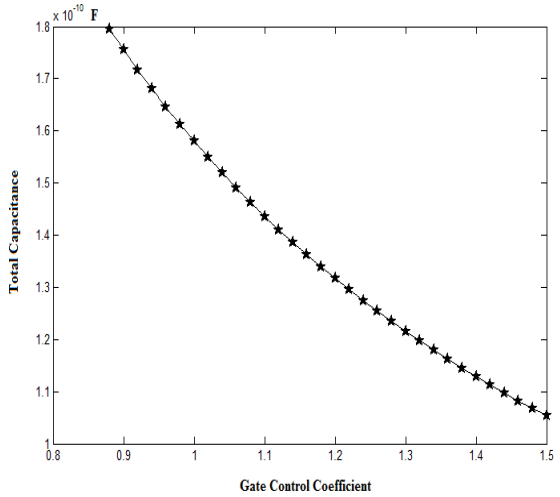

Fig. 3 – Relationship of Total capacitance and Gate Control Coefficient

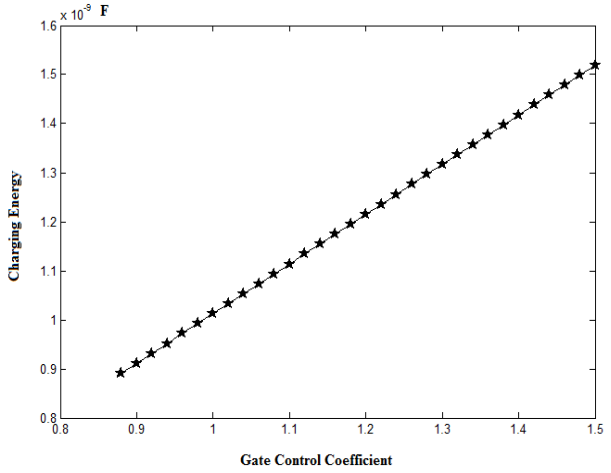

Fig. 4 – Relationship of Charging Energy and Gate Control Coefficient

and leads to a high on-state current and maintain the leakage current level. In addition, Drain conductance (g_d) is a function of drain current in on-state. As a result, increase in on-current results increase in drain conductance also.

The subthreshold swing is a key parameter to transistor shrinking. A small subthreshold swing (S) is required to provide an adequate value of the on / off current ratio. Also it is desired for low threshold voltage and low-power operation for FETs scaled down to small sizes. The lowest theoretical limit for S is $S = (K_B T / e)\ln(10) = 60$ mV / decade at room temperature [14]. Initially, subthreshold swing decreases with high gate control coefficient and its bottom out in between 1.2 to 1.3. Afterwards, swing starts increasing and comes close to its theoretical limit which is shown in Figure 6. This observation indicates that, higher gate control coefficient is desired in order to have fast CNFET response.

The DIBL effect is an electrostatic effect that can change the channel from a state of pinch-off to conduction and result in a substantial leakage current. It also shifts the threshold voltage and renders the gate ineffective in controlling the channel. Consequently, the

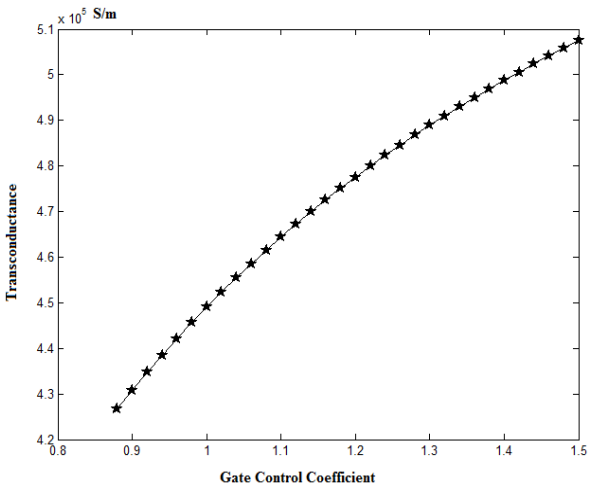

Fig. 5 – Transconductance as a function of Gate Control Coefficient

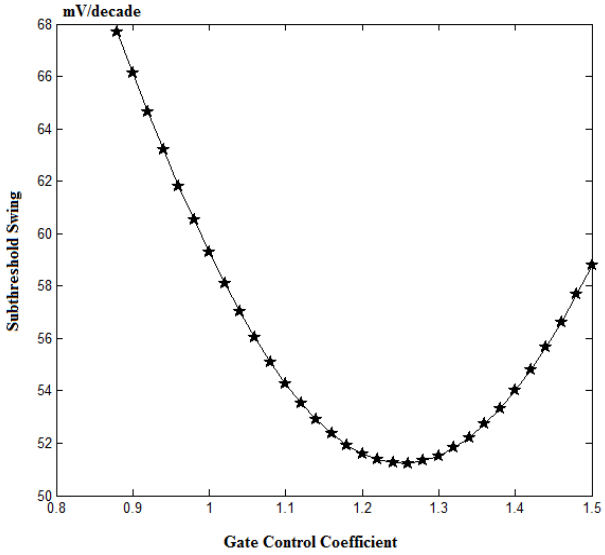

Fig. 6 – Subthreshold swing as a function of Gate Control Coefficient

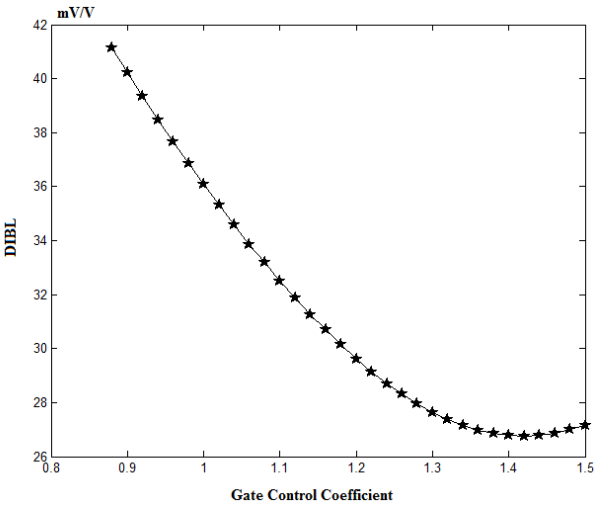

Fig. 7 – DIBL effect with high Gate Control Coefficient

DIBL effect degrades the device performance which should be avoided in device and circuit design [10]. Actually, DIBL effect occurs when the barrier height for channel carriers at the edge of the source reduces due to the influence of drain electric field, upon application of a high drain voltage. Figure 7, shows that, DIBL decrease with increasing gate control coefficient. In fact, it is an advantage of CNTFET while nanometer regime. Hence, with higher gate control coefficient value, CNTFET will exhibit less deviation from ideal performance.

4. CONCLUSION

In this research, gate control coefficient effect on ballistic CNTFET is characterized with an iterative 3D simulation. From above analysis it seems that, high a_G endorses improved drain current with fast device response. Moreover, high a_G maintains leakage current in almost same level. In addition, a_G increases charging energy by decreasing total capacitance which is a pure advantage for device performance. It is also seen that, with high a_G subthreshold swing comes very close to the theoretical limit that deserving for better CNTFET output. On the other hand, high a_G decrease DIBL significantly to have good control over channel. In short, we are suggesting higher value of gate control coefficient (a_G) for better CNTFET performance.

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