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A Comparative Performance Study of Hybrid SET-CMOS Based Logic Circuits for the Estimation of Robustness

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The urge of inventing a new low power consuming device for the post CMOS future technology has drawn the attention of the researchers on Single Electron Transistor [SET]. The two main virtues, ultra low power consumption [1] and ultra small dimension of SET [12, 13] have stimulated the researchers to consider it as a possible alternative. In our past paper [1] we have designed and simulated some basic gates. In this paper we have designed and simulated hybrid SET-CMOS based counter circuits, shift register to show that the hybrid SET-MOS based circuits consumes the lesser power than MOS based circuits. All the simulation were done and verified in Tanner environment using the MIB model for SET and the BSIM4.6.1 model for MOSFET.

Keywords: Single electron transistor (SET), CMOS, Hybrid CMOS-SET circuits, MIB, Noise margin (NM), T-Spice.

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1. INTRODUCTION

A promise of ultra-high integration densities and ultra-low power consumption comes with a term: "Single Electron Transistor". A high quality time of last few decades was afforded to understand the physics of this new promising candidate, in the era of low power VLSI circuits. The application of Single Electron Transistor (SET) is not only restricted for charge sensing applications [readout of few electron memories, readout of charge coupled devices] but it's wide applications are in metrology for precession measurement [2]. In the post CMOS regime, SET is most common among all the Single Electron Devices due to its several electrical characteristics and conceptually simplicity. There are different numerical simulators for the precise simulation of SET, like SIMON [3], KOSEC [4] and MOSES [5]. These all models are accurate from their side, but they are not as useful as circuit simulation purpose and they are high time consuming also. Operation of Single Electron Transistor is based on the transfer of one by one electron, through the channel. SET has unique characteristic like periodically increasing and decreasing of drain current with respect to gate voltage. To take the full advantage of this unique feature we need to analyze its behavior in circuits, whether the circuits working properly with low power consumption than before or not. SET has a major advantage over MOSFET i.e. low power consumption, along with its Nanoscale feature seize and unique Coulomb blockade characteristics. But it has some drawbacks also like low current drive, background charge effect and mainly lack of room temperature operable technology. But nowadays the drawback of room temperature operable technology has been overcome. Researchers have invented room temperature operable SET [6]. Apart from this by overcoming the drawbacks of SET and MOSFET a new device draw the attention of the researchers: Hybrid SET-CMOS technology, which comprises of the advantages of SET and CMOS [7]. Fig. 1 shows a circuital representation of SET. In our previous work [1] we have designed some basic gates and showed that the concept of hybridization is a new possibility in low power VLSI design.

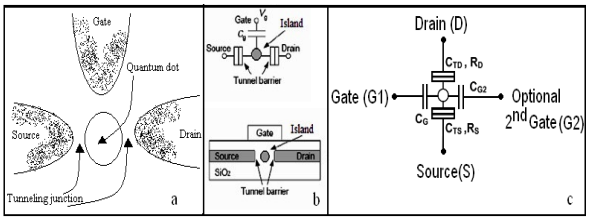

Fig. 1 – Schematic structure of SET

In the modern digital circuits and computing also, counters are such a device which stores and sometimes displays a number of times an event, happening with respect to a clock signal. A wide variety of classifications in counters exist. Each is different in application. Practically Counters count natural binary, though they are digital in nature. In our present paper we have designed Synchronous up counter, Synchronous down Counter, Synchronous up down Counter, Asynchronous up counter, Asynchronous down counter, Asynchronous up down counter, Synchronous Asynchronous decade counter, Shift Register. We have used MIB model. All the circuits are verified by means of T-Spice simulation software. The MIB compact model for SET devices and BSIM 4.6.1 model for CMOS are used in our paper.

2. SINGLE ELECTRON TRANSISTOR

The concept of Single Electronics comes from the thoughts of Quantum devices, better to say, "Quantum Dot". A portion of matter is called Quantum Dot, whose excitations are confined in three spatial dimensions. These types of materials have electronic properties intermediate between those of bulk semiconductors and those of discrete molecules. They were discovered at the beginning of the 1980s by Alexei Ekimov [8] in a glass matrix and by Louis E. Brus in colloidal solutions. The term "quantum dot" was coined by Mark Reed [9].

Researchers have studied quantum dots in transistors, solar cells, LEDs, and diode lasers. They have also investigated quantum dots as agents for medical imaging and hope to use them as cubits in quantum compu-

ting. Quantum dots are one type of semiconductors whose electronic characteristics are closely related to the size and shape of the individual crystal. Generally band gap seize is inversely proportional to the size of the crystal. Again, the smaller the size of the crystal means, the greater the difference in energy between the highest valence band and the lowest conduction band. Therefore more energy is needed for the excitation of the dot, and concurrently, more energy is released when the crystal returns to its resting state.

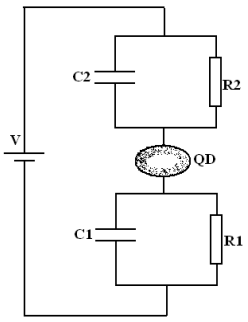

Fig. 2 – Quantum dot

2.1 Basic of Single Electronics

Let we take an example of small conductor, which is initially electro neutral; have exactly as many electrons as it has protons in its crystal lattice. In this condition any appreciable electric field is not generated by the island beyond its border and an additional electron may bring in due to a weak external force. Now the net charge is $-e$. The charging energy of the island is E_C, where the total capacitance is C and E_C can be calculated from [10].

$$E_C = \frac{e^2}{C} \tag{1}$$

When the size of the island becomes comparable with the de Broglie wavelength of the electron inside the island, energy quantization

$$E_N = \frac{(n\prod\hbar^2)}{2xw^2} + \frac{\hbar^2 k^2}{2x} \tag{2}$$

The electron addition energy (Ea) can be calculated from [10]

$$E_a = E_C + E_K \tag{3}$$

E_K – quantum kinetic energy of the addition electron [10]; for a degenerate electron gas

$$E_K = \frac{1}{g(\in_F)V} \tag{4}$$

Where V is the island volume and $g(\in_F)$ is the density of states on the Fermi surface. Where V is the island volume and $g(\in_F)$ is the density of states on the Fermi surface.

2.2 Transfer of Electron through a Quantum Dot

Electron transfer through a quantum dot is interplay of two effects: resonant tunneling effects and Coulomb Blockade effect. When the Fermi energy EF in the source lines up with one of the energy levels in the dot then the resonant tunneling happens. And in very low temperature the energy, required to charge the junction with one elementary charge is larger than the thermal energy of the charge carriers. This phenomenon is called Coulomb Blockade.

3. HYBRID MOS-SET

The concept of hybridization of SET with MOSFET was introduced to overcome the problems of SET, like, low current drive, lack of room temperature operable technology and back ground charge effects. This concept was totally based on the advantages of MOSFET and SET. All the simulations of hybrid circuits are done using MIB model [11], BSIM 4.6.1 model card.

4. HYBRID CMOS-SET COUNTERS

4.1 Hybrid Synchronous Up Counter

Fig. 3 shows the diagram of 4 bit (MOD-16) Hybrid synchronous up counter. Only LSB J K flipflop connected to Vdd. Initially $q_a = q_b = q_c = q_d = 0$. Flipflop changes its state when $q_a = q_b = q_c = q_d = 1$, which is depicted in Fig. 4.

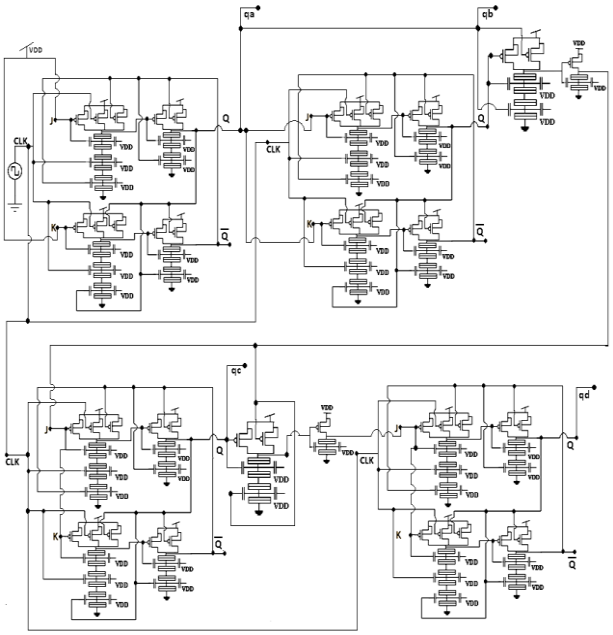

Fig. 3 – A 4 bit Hybrid SET-CMOS based synchronous up counter

4.2 Synchronous Down Counter

Fig. 5 shows the diagram of 4 bit (MOD-16) Hybrid synchronous down counter. Initially $q_a = q_b = q_c = q_d = 1$. The parallel counter counts down by inverted output of the J K flipflop. The output is reflected in Fig. 6.

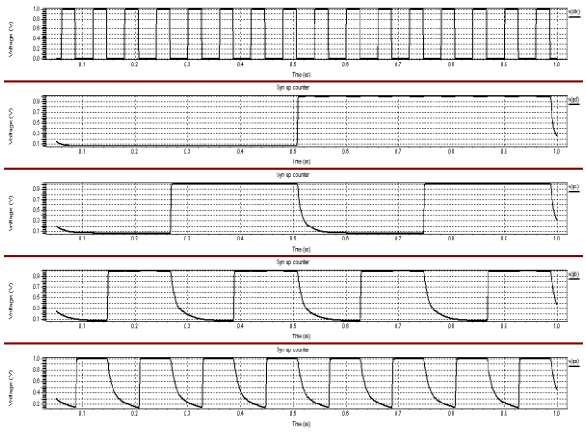

Fig. 4 – Simulation output of 4 bit hybrid synchronous up counter

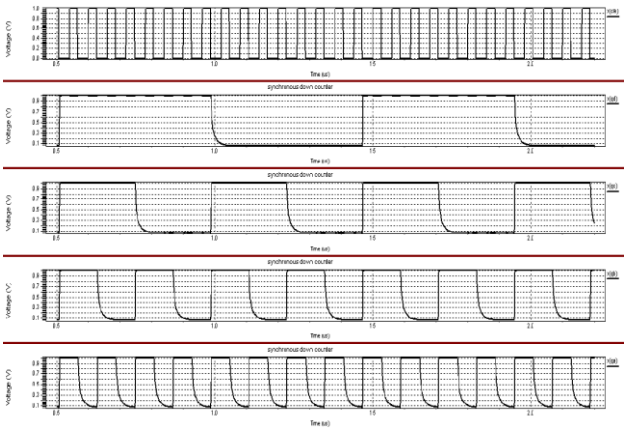

Fig. 6 – Simulation output of 4 bit hybrid synchronous down counter

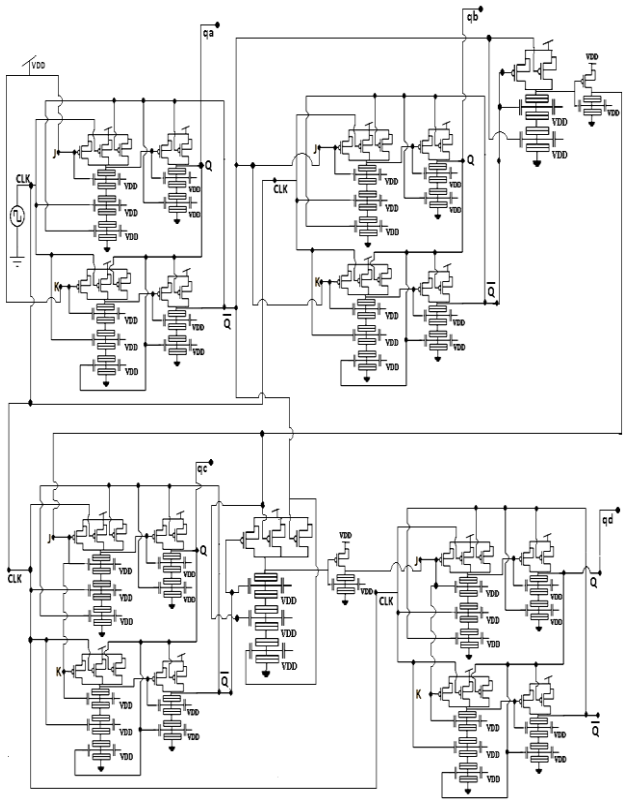

Fig. 5 – A 4 bit hybrid SET-CMOS based synchronous down counter

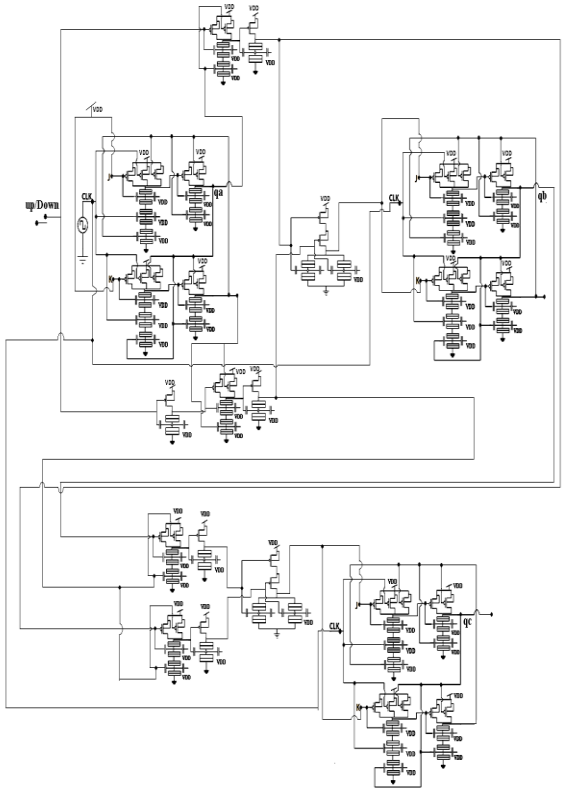

Fig. 7 – A 4 bit hybrid SET-CMOS based synchronous up down counter

4.3 Synchronous Up / Down Counter

A 3 bit (MOD-8) Hybrid Synchronous Up / Down Counter (Shown in Fig. 7) use control input COUNT-UP & COUNT DOWN to work as a multimode counter. When COUNT-UP = 1 & COUNT DOWN = 0 it counts from 000 to 111.The reverse action occurs with COUNT-UP = 0 & COUNT DOWN = 1.This counter produces same output as illustrated in Fig. 4 in up counting & Fig. 6 in down counting operation.

4.4 Asynchronous Up Counter

A 4 bit Hybrid Asynchronous (Ripple or Serial) Up Counter shown in Fig. 8 counts from logic 0 state ($q_a = q_b = q_c = q_d = 0$) to $q_a = q_b = q_c = q_d = 1$.

All inputs of the J K flipflops are connected to Vdd & clock inputs are connected to LSB flipflop. Therefore signal transmits through the asynchronous up counter in a ripple fashion.

4.5 Asynchronous Down Counter

A 4 bit hybrid asynchronous down counter illustrated in Fig. 10, each flipflop toggles its state according to the inverted output of the previous flipflop. It is decremented by 1 (initially $q_a = q_b = q_c = q_d = 1$) at each transition and reaches to zero state.

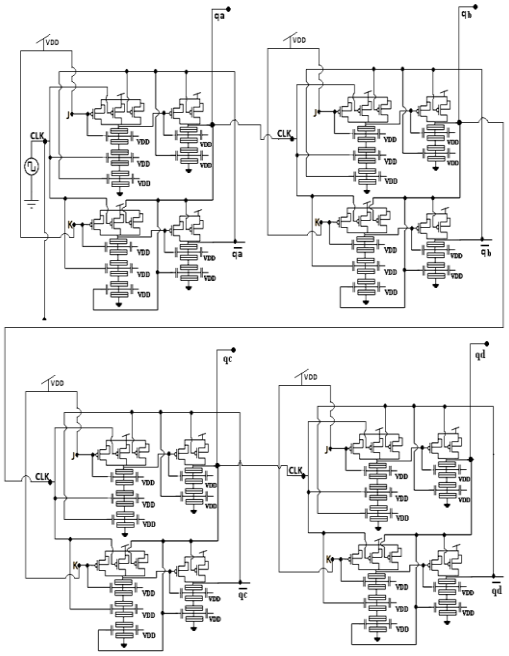

Fig. 8 – A 4 bit hybrid SET-CMOS based asynchronous up counter

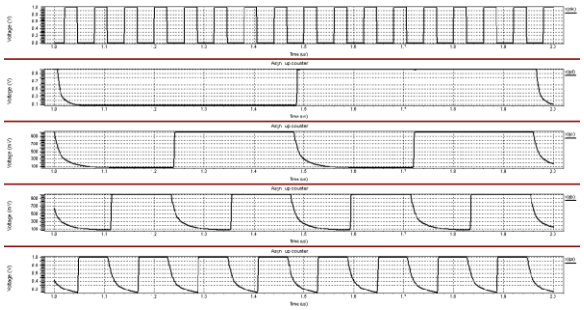

Fig. 9 – Simulation output of 4 bit hybrid asynchronous up counter

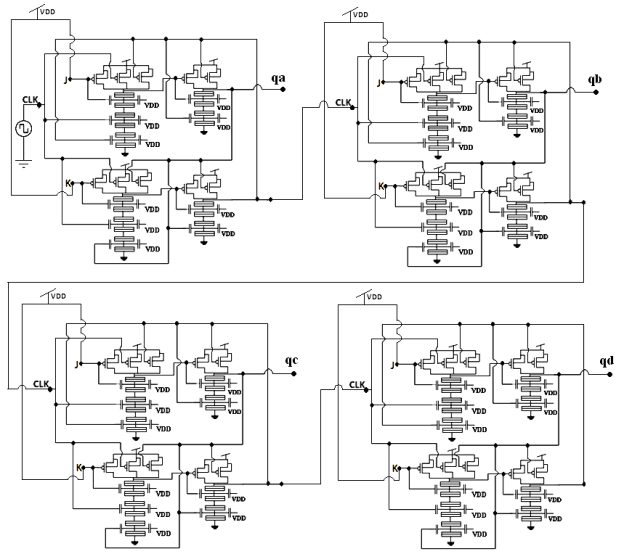

Fig. 10 – A 4 bit hybrid SET-CMOS based asynchronous down counter

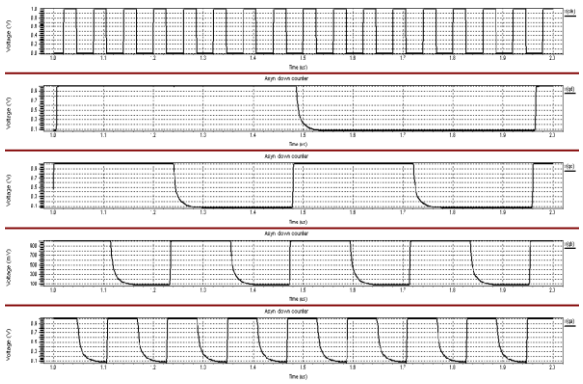

Fig. 11 – Simulation output of 4 bit hybrid asynchronous down counter

4.6 Hybrid Asynchronous Up / Down Counter

A 4 bit hybrid asynchronous up / down counter as described in Fig. 12 switch to multimode counter by using control input COUNT-UP & COUNT DOWN. It cannot count when both control inputs are 1 or 0.It produces same output as shown in Fig. 9 (up mode) & Fig. 11 (down mode).

4.7 Hybrid Synchronous / Asynchronous Decade Counter

Hybrid Synchronous/Asynchronous decade Counter, shown in Fig. 13, made by combining Synchronous & Asynchronous Counter, provides a comprise between the speed of Synchronous counter & simplicity of Asynchronous Counter. At the 10th pulse flip-flop will toggle & bring the counter back to 0000 state from 1001 state.

Table 1 – Comparison of average of power

Sl No.	Name of the Circuit	Power Consumed Using Hybrid SET-CMOS Model	Power Consumed Using MOSFET Model
1	Synchronous up counter	1.319269e-010 watts	2.115174e-009 watts
2	Synchronous down counter	1.080815e-010 watts	2.073577e-009 watts
3	Synchronous up / down counter	1.189205e-010 watts	2.585096e-009 watts
4	Asynchronous up counter	1.928327e-010 watts	1.355511e-008 watts
5	Asynchronous down counter	1.933616e-010 watts	1.356138e-008 watts
6	Asynchronous up / down counter	1.916439e-010 watts	9.035318e-009 watts
7	Synchronous asynchronous decade counter	1.325760e-010 watts	7.514414e-009 watts
8	Hybrid shift register	5.890781e-010 watts	3.100656e-009 watts

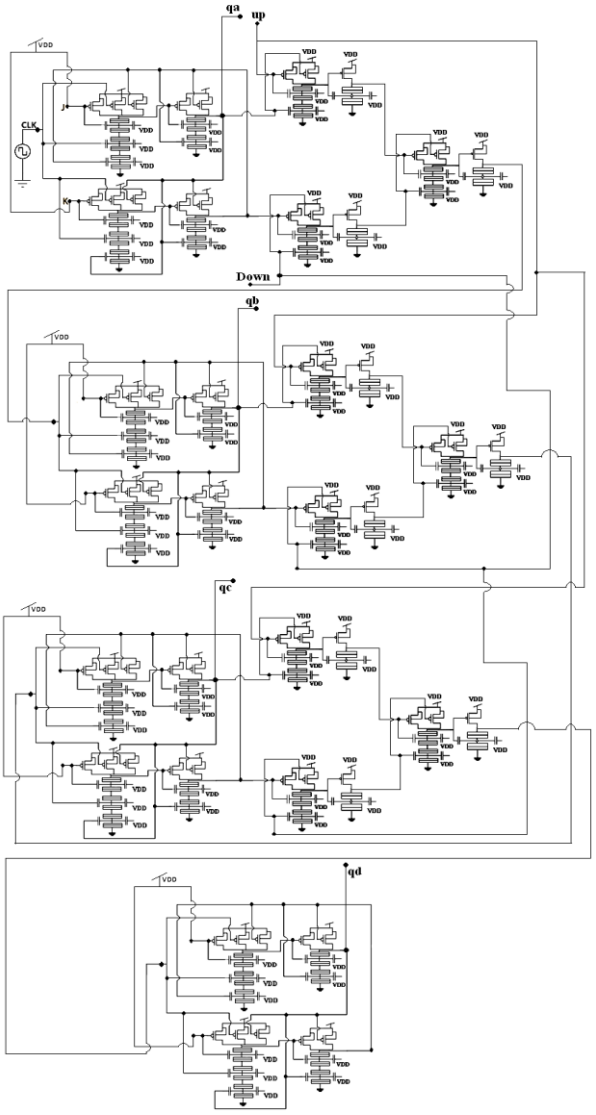

Fig. 12 – A 4 bit hybrid SET-CMOS based asynchronous up down counter

4.8 Hybrid Shift Register

Fig. 16 reflects the simulation output of hybrid SET-CMOS based 4 bit shift register circuit, which can shifts binary information in both direction or in same depending on the clock input.

5. RESULTS & DISCUSSION

We have simulated the above circuits using BSIM 4.6.1 and MIB model in tanner environment. The parameters used for the simulation are the room temperature parameters [1, 14, and 15], which are reflected in Table 1.

6. CONCLUSION

Employing a uniform interval of clock pulse, counter carries out a predetermined sequence of states. In this section we have projected the conception of hybrid SET CMOS architecture by designing counter. Also this module portrays the comparison of power consumption in hybrid SET-CMOS model & conventional MOS model. Thus we have shown the novelty and robustness of our model. The low power consumption of hybrid model attracts the attention of the entire VLSI designer. As the operating temperature becomes sub ambient regime, overall performance (switching speed, mobility, power dissipation) will be better. Here all the SET-CMOS design & simulation are done in room temperature so that it exhibits their full functionalities.

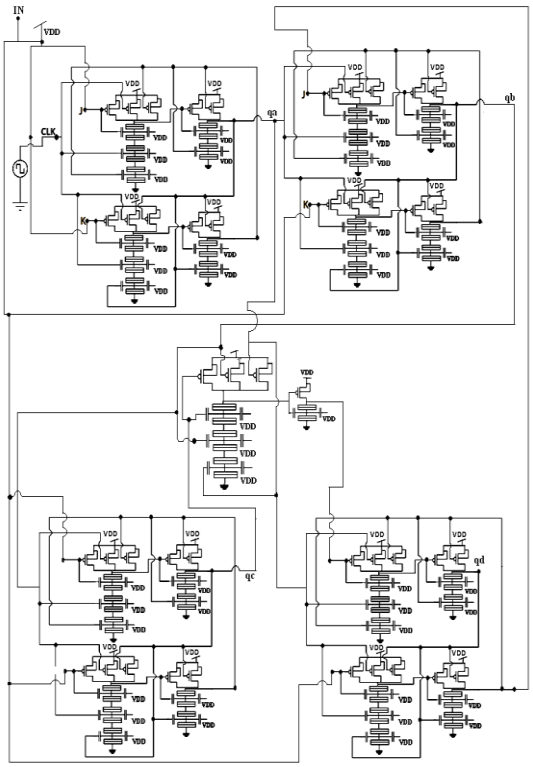

Fig. 13 – A 4 bit hybrid SET-CMOS based synchronous-asynchronous decade counter

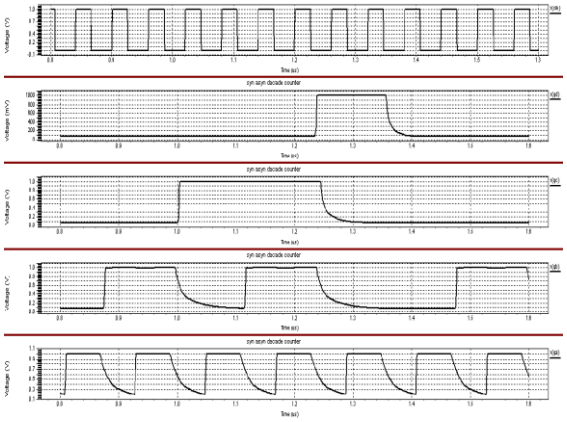

Fig. 14 – Simulation output of a 4 bit hybrid synchronous-asynchronous decade counter

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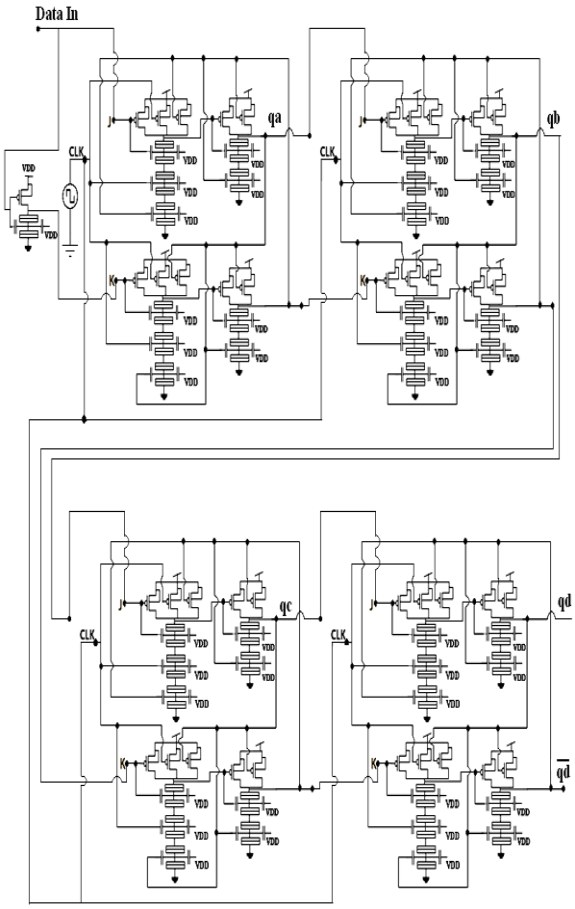

Fig. 15 – A 4 bit hybrid SET-CMOS based shift register

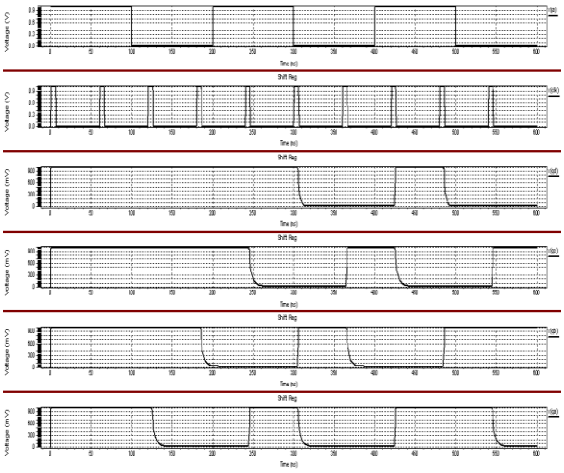

Fig. 16 – Simulation output of 4 bit hybrid shift register

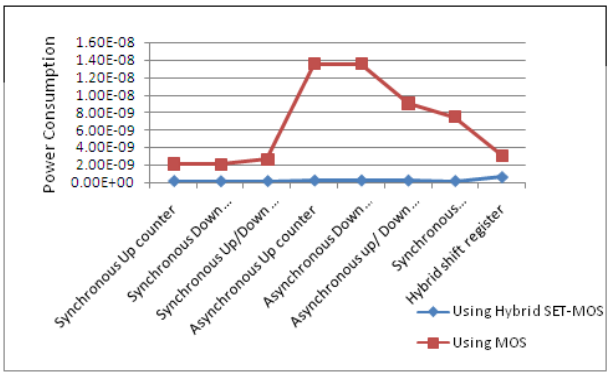

Fig. 17 – Comparison of power consumption hybrid model & MOS model

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